Mixed Signal Controlled Low Drop-Out Voltage Regulator

A Project Report

submitted by

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THESIS CERTIFICATE

This is to certify that the thesis titled **Mixed Signal Controlled Low Drop-Out Voltage Regulator**, submitted by **Angelo de Carmine**, to the Indian Institute of Technology, Madras, for the award of the degree of **Bachelor of Technology and Master of Technology**, is a bona fide record of the research work done by him under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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ABSTRACT

KEYWORDS: Low Drop-Out Regulator; Dual loop; Analog-Digital control; Limit cycle Oscillations(LCO); Transient response

This project implements an Analog-Digital dual loop architecture for a output-capacitor less Low Drop-Out (LDO) voltage regulator, with fast transients and a 10 mA load capacity. In this project, the output voltage is regulated by two loops, the digital and analog loops. The digital loop can supply a high load current, while the analog loop supplies low load current, only a fraction of the maximum load capacity. This helps eliminate Limit Cycle Oscillations (LCO) and enhances the overall transient performance. The LDO implemented in the project regulates an input voltage of 1.2V to an output voltage of 1V with a maximum load current of 10 mA.

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ABBREVIATIONS

IC	Integrated circuits
PMIC	Power Management Integrated Circuits
LDO	Low Dropout Voltage regulator
LCO	Limit Cycle Oscillations
PMOS	P-channel MOSFET
NMOS	N-channel MOSFET
PSRR	Power Supply Rejection Ratio
ADC	Analog to Digital Converter

NOTATION

V_{fb}	Feedback voltage
V_{ref}	Reference voltage for error correction
V_{gs}	Gate-source voltage difference in a MOSFET
V_{sd}	Source-drain voltage difference in a MOSFET
V_{out}	Output Voltage of the LDO
V_{in}	Input Voltage of the LDO
μ_n	Mobility of majority charge carriers in an N-channel
μ_p	Mobility of majority charge carriers in an P-channel
V_e	Error voltage
$V_{dropout}$	Dropout voltage between input and output of an LDO
β	Feedback factor

CHAPTER 1

INTRODUCTION

The future is filled with a lot of handheld, portable devices and the internet of things. This demands for a highly efficient Power management as they are mostly battery powered. Generally these devices are not sized for housing a large battery. This raises a critical necessity for a sophisticated Power Management Integrated Circuit(PMIC) designs which enhance rather than degrade the performance. A Mobile power system usually has one battery and a multitude of intellectual properties that require a variety of power levels for the application processor to run efficiently. This creates room for a lot of DC-DC regulators on the chip.

There are two types of DC-DC regulators namely Switching regulators and Linear regulators. Switching regulators are efficient at a larger voltage drop, expensive and noisy, while the Linear regulators are efficient at low voltage drop, are cheap, smaller and quiet. LDOs are linear regulators, they only supply a small portion of the power requirement($\approx 10\%$). But they vastly outnumber the switching regulators in a chip. Usually for one switching regulator there are 5-10 linear regulators on a chip. Due to the large number of LDOs in a chip, the area of an individual LDO becomes a luxury we can not afford. This brings a huge popularity for the digital LDOs in the place of their analog alternatives.

This report starts with the basic introduction to linear regulators. Pushing to the general topologies of LDOs namely Analog and Digital LDOs, the report discusses the advantages and limitations of each. Then goes to discuss about the type of architecture chosen for both the digital and analog loop individually. Then it discusses regarding the hybrid architecture and the motivation for one. This is followed by the advantages of the proposed hybrid architecture and then the simulation results.

CHAPTER 2

BACKGROUND

2.1 Linear Drop-out Regulator

The structure of an LDO is defined by the way the current through Pass element is controlled. The Analog LDO is controlled by varying the gate voltage V_{gs} of the pass transistor with an error amplifier. While the digital counterpart is controlled by quantising the current by the number of pass transistors which act as switches turning on and off, the number of pass transistors on at a particular instant decides the amount of current that passes through the pass element. This is achieved with a digital controller and a switch array.

The Analog LDO needs a large pass transistor as it requires a minimum headroom voltage to stay in saturation while active. They provide a very good supply noise rejection and accuracy. The Digital LDOs do not require large pass transistors as they fully turn on and off during the operations and hence can afford a large V_{gs} than the analog counterparts. Thus they are much smaller in area compared to the analog LDO's pass transistors. They also have a relatively low quiescent current. Digital LDOs are much better when it comes to process scalability and have relatively less stability issues.

Even though digital LDOs seem very advantageous over Analog LDOs they also carry some trade-offs with them. Digital LDOs have an intrinsic output voltage ripple called as Limit Cycle Oscillation(LCO) that arises due to the quantization error in the load supplied. The least significant bit that controls a pass transistor keeps turning it on and off constantly creating a ripple in the output. They also have a poor rejection towards power supply noise as their pass transistors operate in deep triode region. This makes the concern towards reliability of a Digital LDO a bit more than their Analog counterparts. Hence the Analog LDO is preferred when the circuits are designed to be precise and very sensitive.

2.2 Analog LDO

The design of an analog LDO consists of a voltage reference, an error amplifier, a pass element and a feedback voltage divider. The error amplifier controls the gate voltage of the PMOS transistor, that is used as the pass element. This in turn controls the current flowing through the PMOS transistor. The amplifier compares the scaled output voltage(feedback) and its voltage reference to control the gate voltage of the pass element. If the feedback is higher than the voltage reference, the amplifier increases the gate voltage of the pass element, making the V_{gs} of PMOS smaller. This reduces the current through PMOS, and helps in bringing the output voltage down. Similarly, if the feedback is lower than the voltage reference, it increases the V_{gs} in turn increases the current through the PMOS. This makes the output voltage, V_{out}, to lower down to the desired value, given by the equation 2.1.

$$V_{out} = (1 + \frac{R_1}{R_2})V_{ref} \tag{2.1}$$

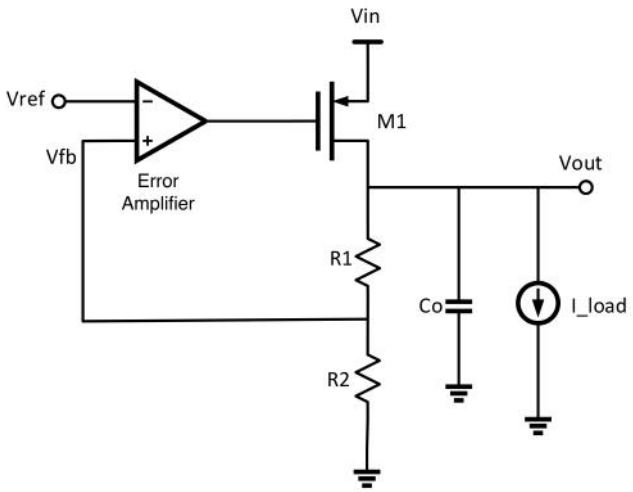


Figure 2.1: Conventional structure of an Analog LDO

The frequency response of an analog LDO is given by

$$H(s) = \beta \frac{A_1 A_2}{(1 + sR_e C_{gp})(1 + sR_0 C_0)} \tag{2.2}$$

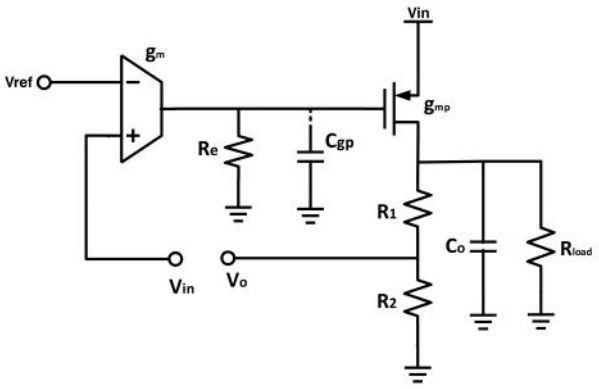


Figure 2.2: Small signal circuit of an Analog LDO

where,

$$\begin{aligned} \beta &= \frac{R_2}{R_1 + R_2}, \\ A_1 &= g_m R_e, \\ A_2 &= g_{mp} R_0, \\ R_0 &= \frac{R_{load}(R1 + R_2)}{R_{load} + (R1 + R_2)} \end{aligned} \tag{2.3}$$

The poles for the system are at

$$\begin{aligned} \omega_{p1} &= R_e C_{gp} \\ \omega_{p2} &= R_0 C_0, \end{aligned} \tag{2.4}$$

For a better stability in the closed loop the phase margin of the loop is preferred to be more than $60°$.

2.2.1 Pass Element

The pass element can either be a PMOS or an NMOS transistor. The PMOS pass transistors can degrade the Power Supply Rejection Ratio (PSRR) of the LDO at higher frequencies. An NMOS transistor can also be used as a pass transistor with its drain as the power supply and output at its source as shown in the fig -2.4a. This would have an improved load regulation and also a better power supply rejection. The compensation complexity required for an NMOS pass element is relatively less. But the downside to using a NMOS pass element is the high voltage head room required for it to be in

operation. The voltage dropout between the voltage source and the output is far more than when a PMOS pass element is used.

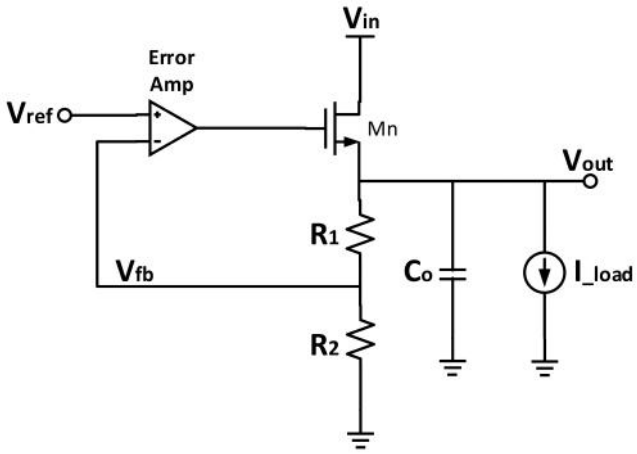
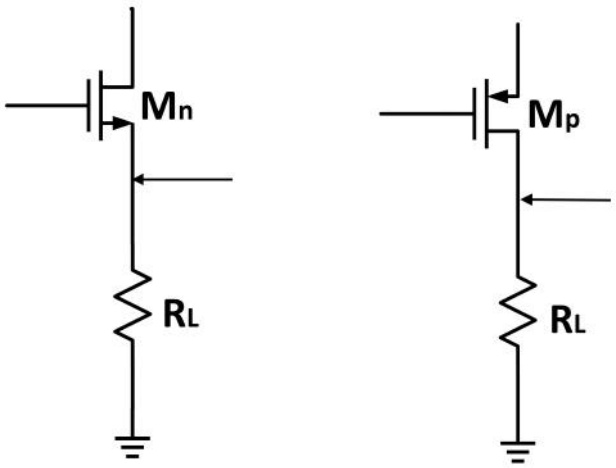


Figure 2.3: Analog LDO with an NMOS pass element

$$\begin{aligned} V_{dropout} &= V_{sd(sat)}\ for\ a\ PMOS. \\ V_{dropout} &= V_{sd(sat)} + V_{gs}\ for\ an\ NMOS\ pass\ element. \end{aligned} \tag{2.5}$$



(a) NMOS pass element (b) PMOS pass element

Figure 2.4: Pass elements

$$\begin{aligned} R_{out} &= R_L//r_{op}\ for\ PMOS. \\ R_{out} &= R_L//\frac{1}{g_{mn}}\ for\ NMOS. \end{aligned} \tag{2.6}$$

The size of the transistor also decreases by almost 50 % for an NMOS pass element, since

$$\mu_n \approx 2 * \mu_p \tag{2.7}$$

But this area will mostly be compensated by a charge pump used to maintain the large voltage headroom neccesary for the Pass element to be saturation region

2.3 Digital LDO

The Digital LDO uses the digital alternatives of the components used in an Analog LDO . It consists of a pass element, a feedback voltage divider, a voltage reference, a Analog to Digital converter (ADC), a digital controller and an accumulator. The error in the feedback voltage(V_{fb}) is processed by the ADC and a signal is sent to the digital controller. The digital controller processes this signal and decides how the accumulator adds it up to the pass element. The accumulator acts a "digital" integrator, it accumulates the error in the output voltage, with the commands given by the digital controller. The output of the accumulator is then pushed to the pass element.

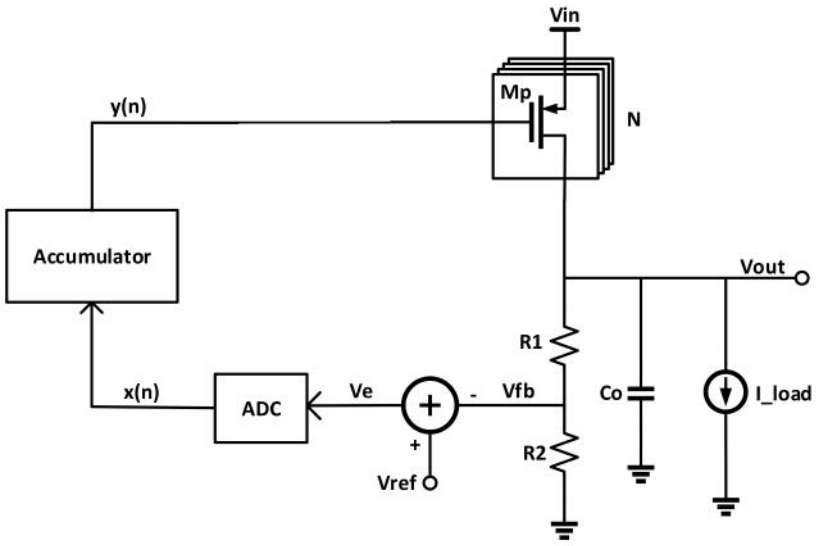


Figure 2.5: Conventional Structure of a Digital LDO

The ADC used could be as simple as an one bit ADC which is just a comparator. This comparator compares the V_{fb} to the voltage reference V_{ref} and outputs a digital one bit data. Depending on the polarity it either produces a digital low or high.

Lets say

$$\begin{aligned} V_{fb} > V_{ref} &\rightarrow 0 \\ V_{fb} < V_{ref} &\rightarrow 1 \end{aligned} \tag{2.8}$$

The digital controller processes this data and counts up when output is 1 and counts down when the output is 0.

$$y(n) = y(n-1) + x(n) \tag{2.9}$$

ADC is always trying to get a better resolution, hence keeps on updating the digital controller with a digital low or high. This makes the output to never settle. This results in a ripple in the output due to that one pass transistor that keeps turning on and off for every cycle. This ripple in the output is called as the Limit Cycle Oscillation(LCO) as shown in Fig 2.6.

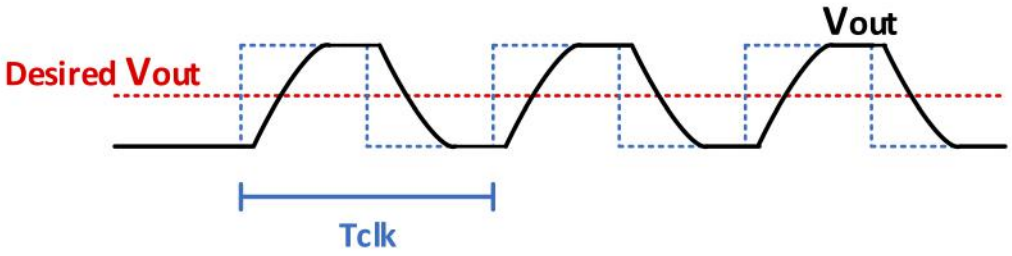


Figure 2.6: Limit Cycle Oscillations

This can be resolved by using a two bit ADC which has two levels of voltage reference, such that the ADC never updates the accumulator when the V_{fb} is in between these two levels. Let V_{ref1} and V_{ref2} be the two levels. The two bit output looks like

$$\begin{aligned} V_{fb} > V_{ref1} &\rightarrow 11 \\ V_{ref1} > V_{fb} < V_{ref2} &\rightarrow 01 \\ V_{fb} < V_{ref2} &\rightarrow 00 \end{aligned} \tag{2.10}$$

The update rate of the ADC should be atleast 5 times slower than the RC time constant at the output. This is to make sure that the output has been settled by the time

the digital controller decides to accumulate the error.

CHAPTER 3

Proposed architechure of the LDO

The architecture consists of two loops, digital and analog, aiding each other simultaneously. Any transients in the load requirement are first detected by the analog loop and the digital loop only turns on when the analog loops needs to be supported. The analog loop only supplies a 15% of the maximum load. This is to reduce the on-chip area as the analog loop requires a large PMOS pass element to supply all the load. The digital loop supplies more than a 85% of the maximum load capacity, with a lot lesser on-chip area. Hence any load supplement required more than the 15% that the analog loop offers is supplied by the digital loop.

3.1 Analog loop

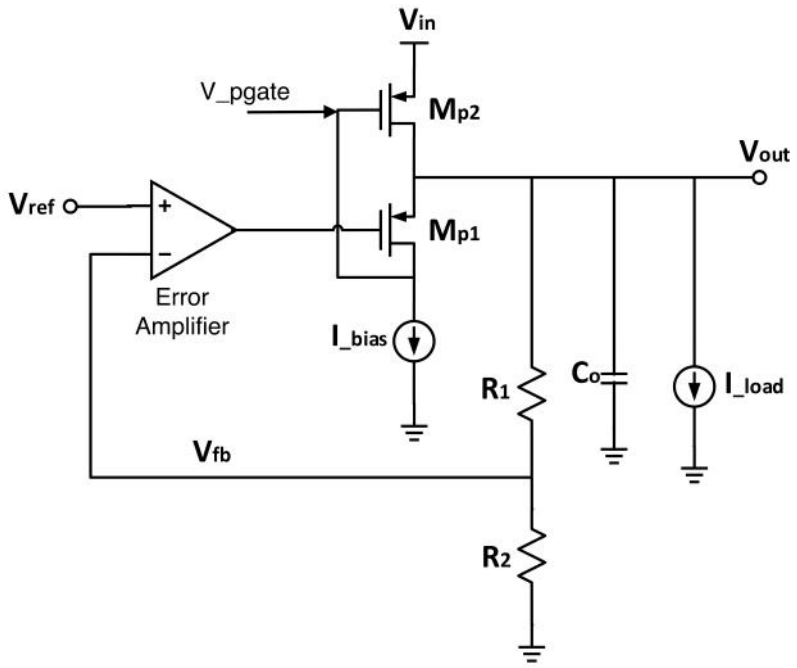


Figure 3.1: Proposed architecture of the Analog loop

This project implements the Flipped Source follower as its pass element as it has a better PSRR and a characteristic as an NMOS pass element with a much lower voltage drop-out when compared to the NMOS.

The load regulation is much better than an NMOS pass element. The M_1 acts as a sink that limits the current that flows through M_2 as per the load requirement. It eliminates the on resistance of the M_2 in the R_{out} equation which gives a better PSRR.

$$R_{out} = \frac{1}{g_{m1} g_{m2} r_{o1}} \tag{3.1}$$

3.2 Digital Loop

This loop comprises of a slightly altered digital LDO that uses the information about the analog Pass elements status regarding its saturation, to control the current through its pass element. It consists a digital controller, Accumulator, and a switch array.

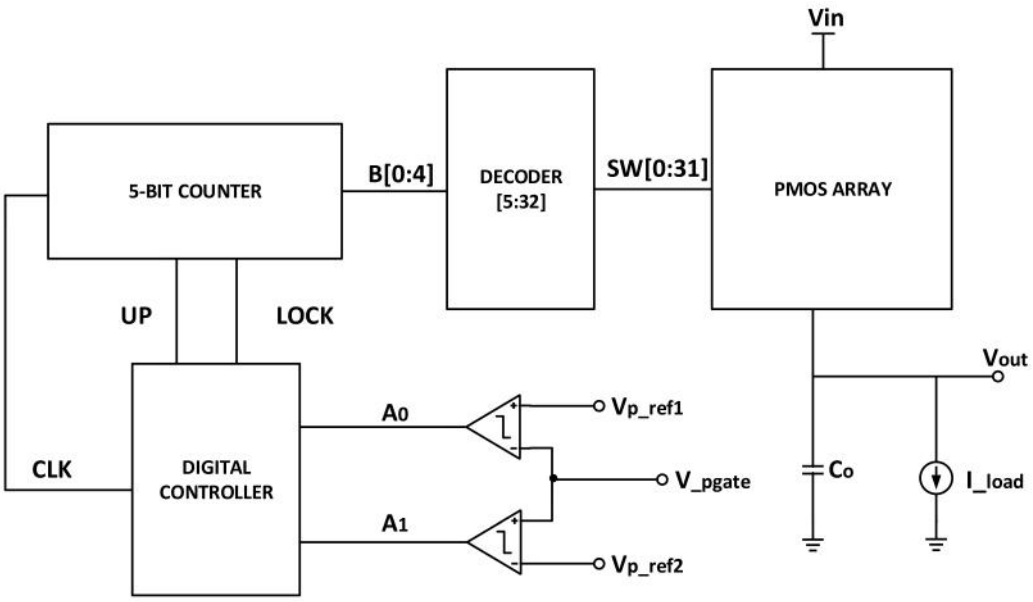


Figure 3.2: Proposed architecture of the Digital Loop

3.2.1 Digital Controller

The digital controller is two bit ADC which has a pair of comparators that compare the feedback from the analog loop with two levels of reference voltages. This two bit data is passed through certain logic to achieve the required signal for the accumulator.

$Case$	A_0A_1	UP	$LOCK$	$FUNCTION$
$V_{pgate} > V_{ref1}$	11	1	0	$Counts\ up$
$V_{ref1} > V_{pgate} > V_{ref2}$	01	X	1	$Freezes\ Count$
$V_{pgate} < V_{ref2}$	00	0	0	$Counts\ down$

3.2.2 Accumulator

The accumulator cascades a 5- bit counter and a [5:32] decoder. This acts as a makeshift - left right 32 bit shift register that can count up and down the number of pass transistors required to be turned on at any cycle. The counter is a synchronous bidirectional 5-bit binary counter that can count up and down at any cycle. The decoder makes the 5 bit binary code into a 32 bit unary or sometimes referred to as thermometer code. The number of digital '1's in this unary code is the number of transistors that are turned on in the switch array.

$$\begin{aligned} 00000 &\rightarrow 000....000 \\ 00001 &\rightarrow 000....001 \\ 00010 &\rightarrow 000....011 \\ &\ldots \\ &\ldots \\ 11111 &\rightarrow 111....111 \end{aligned} \tag{3.2}$$

3.2.3 Switch Array

The switch array is an array of all the PMOS transistors that are used to supply the load in the Digital loop.

CHAPTER 4

Mixed Signal / Hybrid Architecture

4.1 Merging the two loops

The analog loop is designed such that the current supplied by it is supposed to be within a certain bandwidth, say between I_1 and I_2. If the analog loop supplies a current higher than I_1 the digital controller up counts the accumulator making the switch array to supply more current, and there by reducing the current requirement of the analog loop. Whenever there is an excess of current being supplied the analog loop starts to decrease its current supply to the load. And when it goes below I_2 the digital controller understands that theres an excess supply of current and its starts to down count the accumulator making the switch array to supply less current.

We use the gate voltage(V_{pgate}) of the pass element in the analog loop, as the indicator of the digital controller, as its in loose terms just a scaled version of current supplied by the pass element. So the current levels I_1 and I_2 can be just scaled to voltage reference levels as V_{ref1} and V_{ref2}. V_{pgate} is inversely proportional to the current supplied by the pass element, implying higher the V_{pgate} lower the current through the pass element. Hence $V_{ref1} < V_{ref2}$.

$$\begin{aligned} V_{pgate} > V_{ref1} &\rightarrow Count\ up \\ V_{ref1} > V_{pgate} < V_{ref2} &\rightarrow Freeze\ count \\ V_{pgate} < V_{ref2} &\rightarrow Count\ down \end{aligned} \tag{4.1}$$

The digital controller sends the UP/DOWN and Lock information to the counter. The counter is frozen when the lock is high, it doesn't count. The counter counts up or down based on the UP/DOWN data only if the lock is low. The data from the counter is then pushed to the decoder which converts it into the unary code. This unary code acts as a representation of the number of Pass transistors turned on in the switch array. It is

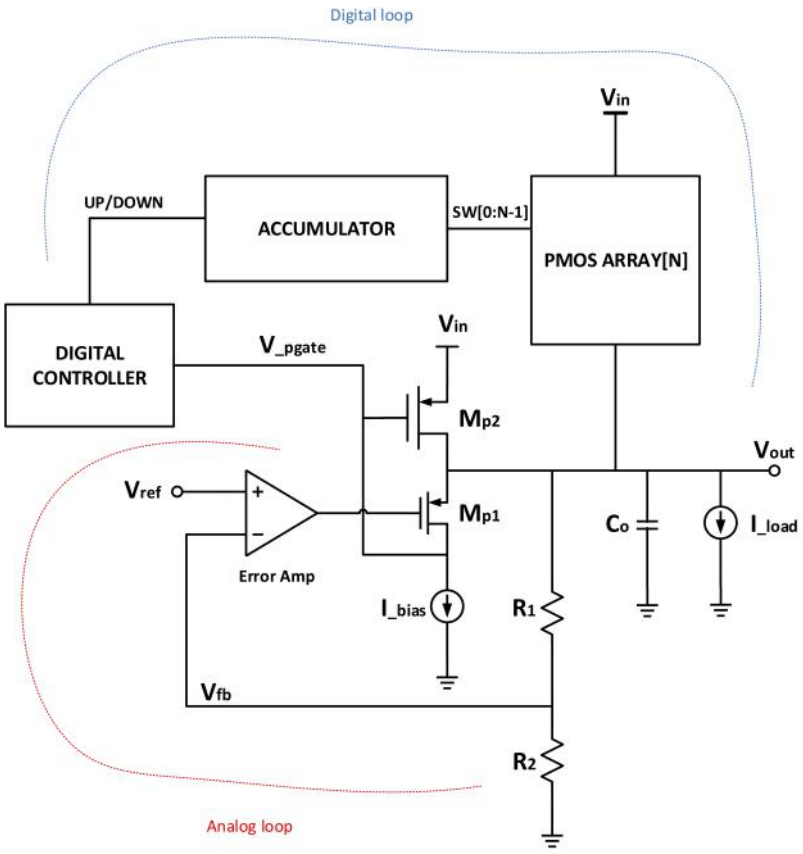


Figure 4.1: Proposed architecture of the Hybrid LDO

safe to say that the number of pass transistors turned on is a direct scaling of the current supplied by the switch array.

4.1.1 Dynamic clock

As discussed in the Section 2.3 the update rate of the ADC should be at least five times slower than the RC time constant at the output. But this can be overruled in this architecture during the transients as the input to the ADC is not the feedback voltage from the output, its rather from the gate voltage of the pass element from the Analog loop. This helps in increasing the update rate during the transients and settling it back to normal rate when its inactive in order to increase the efficiency of the digital blocks. Hence when current load needs to be matched up by the digital loop during a load transient, we can overclock the accumulator for faster transient response.

CHAPTER 5

Simulation results

The LDO has been designed for following specifications and parameters:

Input Voltage = 1.2V

Output Voltage = 1V

Output Capacitance(C_o) = 1pF

Feedback resistors : $R_1 = 400k\Omega$; $R_2 = 600k\Omega$

Feedback factor = 0.6

Reference Voltage (V_{ref}) = 0.6V

Clock period (T_{clk}) = 100nS

Overclock Time period (T_{clk1}) = 4nS

Load transient from $100\mu A$ to $10mA$ in 100nS

5.1 Load transient Behaviour

The load changes from $100\mu A$ to $10mA$ in 100nS.

An undershoot of 140mV is observed and an overshoot of 63mV. The transients take a little over 100nS to settle. Refer Fig 5.1

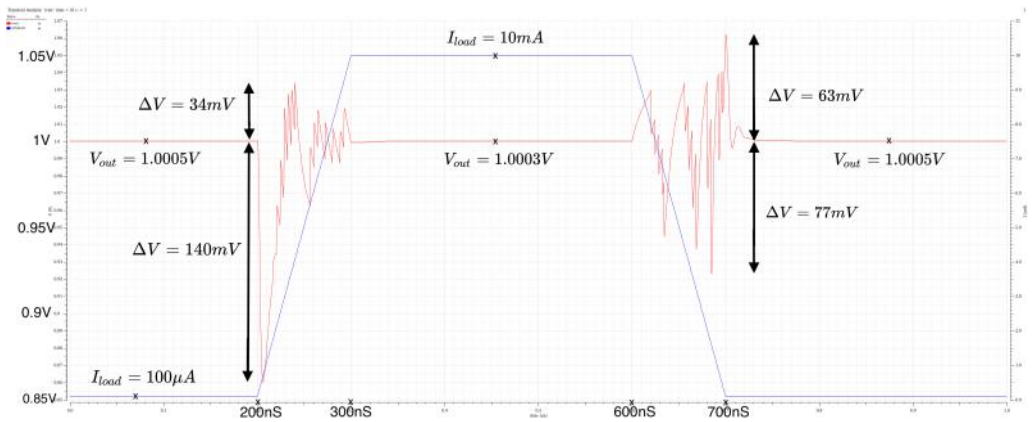


Figure 5.1: Transient response of the hybrid architecture at $V_{out} = 1V$

5.2 Loads supplied by the analog and digital loops

The digital loop supplies the major part of the loop, i.e., $I_{digital} = 8.74mA$, while the analog loop supplies $I_{analog} = 1.26mA$ at a $10mA(I_{load})$ load requirement. Refer Fig 5.2 and Fig 5.3

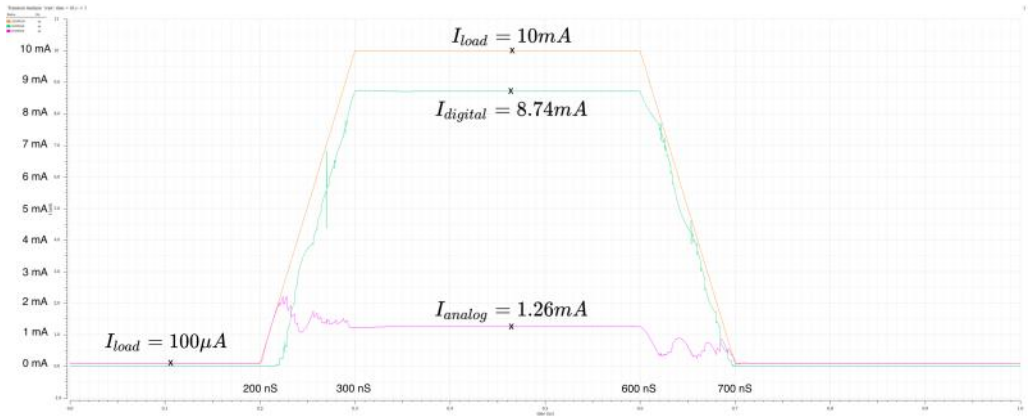


Figure 5.2: Loads supplied by each loop of the hybrid architecture at $V_{out} = 1V$

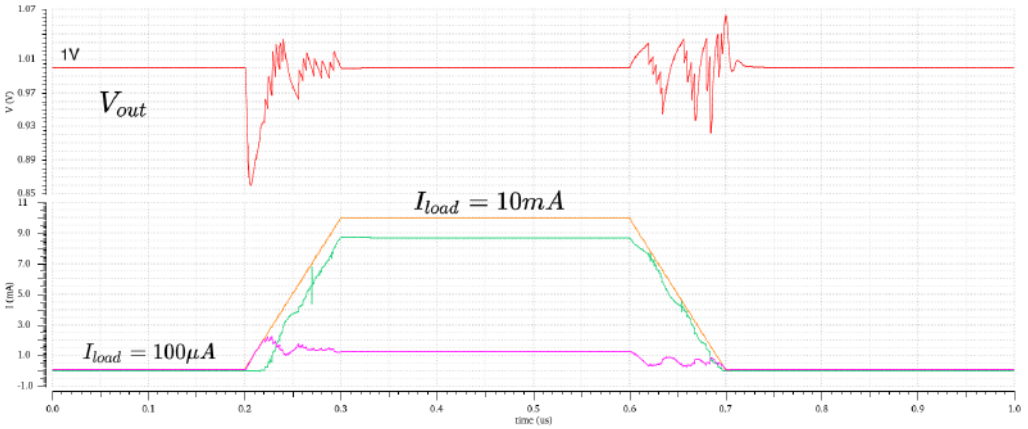


Figure 5.3: Loads supplied by each loop of the hybrid architecture at $V_{out} = 1V$

5.3 Counter output (Binary code)

The counter output when the digital loop supplies $8.74mA$ is 5'b 01110 translates as 14 in decoder.

And the output when it supplies no load ($0mA$) is 5'b 00000 translates as zero in decoder.

Refer Fig 5.4.

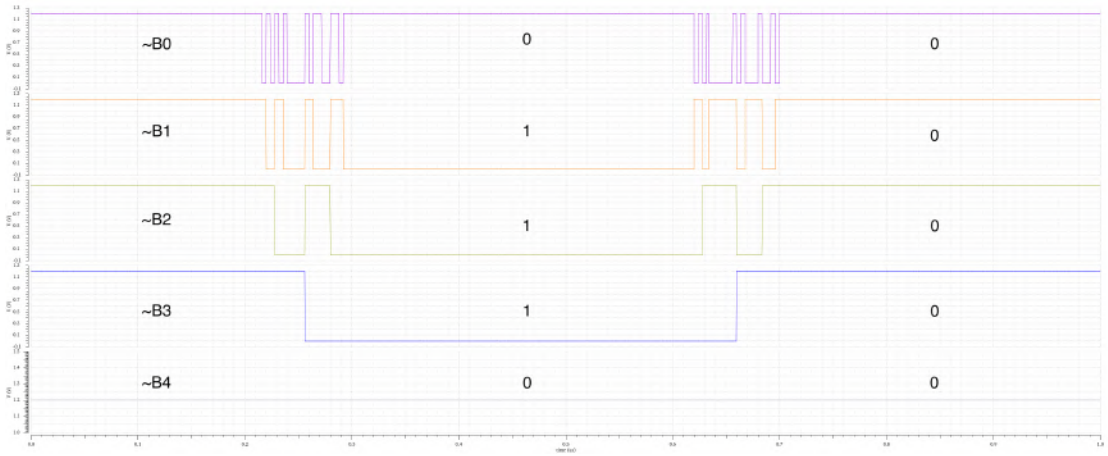


Figure 5.4: Counter output when the load shifts from $100\mu A$ to $10mA$ and back

5.4 Digital controller outputs

The digital controller processes the V_{pgate} to control the counter behaviour. It outputs UP, LOCK and Dynamic clock enable data to the counter. Fig 5.5 shows the dynamic clock and UP, LOCK behaviour with respect to the V_{pgate}.

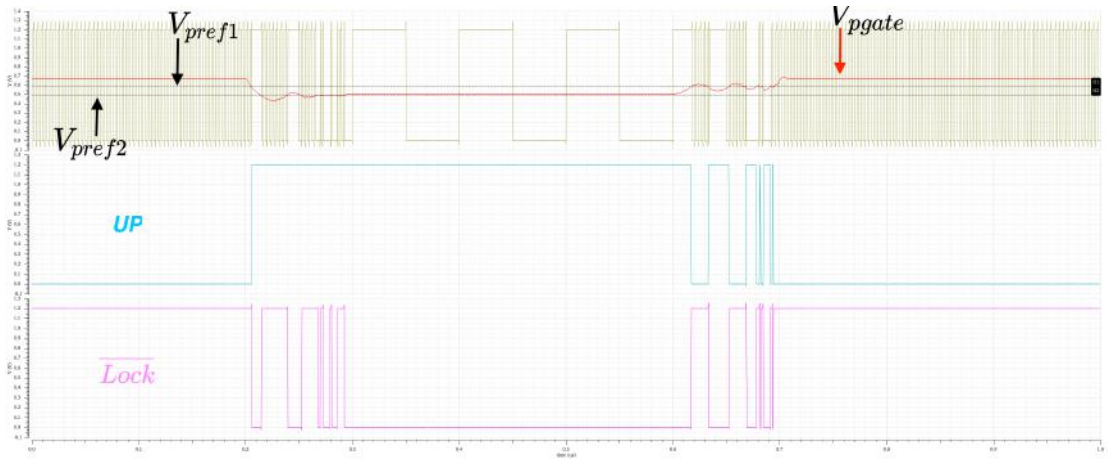


Figure 5.5: Digital controller outputs

5.5 Stability of Analog loop

Fig 5.6 shows the Gain and Phase plots of the stand alone analog loop. With a Phase margin of 80.6° and a unity gain bandwidth of 17MHz the analog loop has a good stability. The poles are at

$$\begin{aligned} f_{p1} &= 160KHz \\ f_{p2} &= 64MHz \end{aligned} \tag{5.1}$$

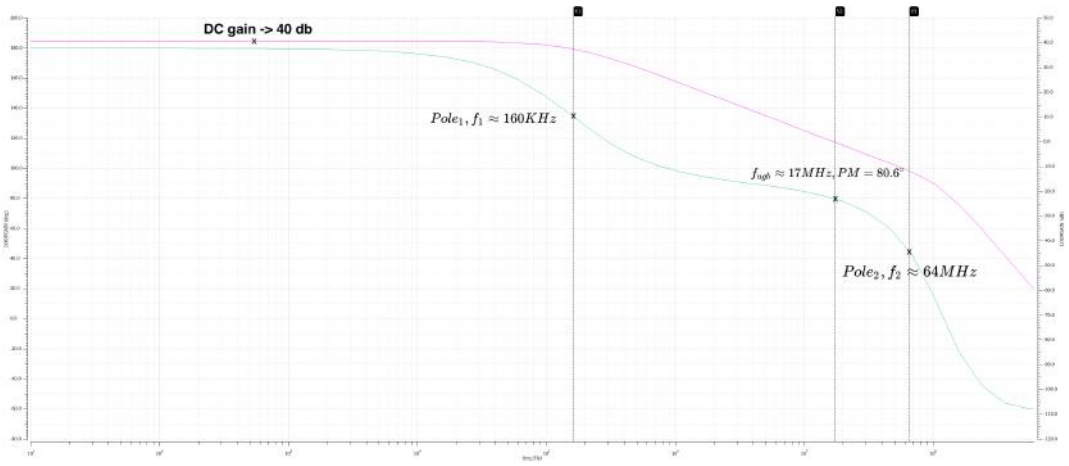


Figure 5.6: Gain and Phase bode plots of the stand alone Analog loop

CHAPTER 6

Conclusion and Future Work

The proposed architecture has adopted the better of the two topologies, i.e., digital and analog LDOs. With the digital loop supplying the major part of load, the analog loop supplies only a fraction of the maximum load capacity. This architecture provides very fast transients and a maximum load current of 10 mA with a much smaller on-chip area due to the digital loop. The output ripple, LCO, due to the digital loop has been eliminated with the addition of an analog loop. The undershoots and overshoots during transients need to be improved in the future work. The clock dynamic logic can be updated to suit better with the transients.

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