Single Input Dual Output Buck Converter With Constant On Time Architecture and FLL loop

A Project Report

submitted by

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in partial fulfilment of requirements
for the award of the degree of

BACHELOR OF TECHNOLOGY

DEPARTMENT OF ELECTRICAL ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY MADRAS

July 2018

THESIS CERTIFICATE

This is to certify that the thesis titled **Single Input Dual Output Buck Converter With Constant On Time Architecture and FLL loop**, submitted by **Ashok Reddy**, to the Indian Institute of Technology, Madras, for the award of the degree of **Bachelor of Technology**, is a bona fide record of the research work done by him under our supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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ABBREVIATIONS

EMI	Electromagnetic Interferences
SISO	Single Inductor Single output
SIDO	Single Inductor Dual output
CCM	Continous Conduction Mode
DCM	Discontinous Conduction Mode
PWM	Pulse Width Modulation
COT	Constant On-time
DCR	DC resistance
ERG	Emulated Ripple Generation
ESR	Equivalent Series Resistancee

CHAPTER 1

INTRODUCTION

With advancement in semiconductor industry, no.of ICs on a single circuit board are increasing rapidly and all these ICs are to be provided with a stable and regulated DC according to its specified voltage and power requirements using DC-DC converters. In portable applications, the output voltage from the battery varies depending on several factors, but the loading devices may need a constant supply voltage for proper operation.And also, the battery voltage declines as its stored energy is drained. Switched DC to DC converters offer a method to increase voltage from a partially lowered battery voltage thereby saving space instead of using multiple batteries to accomplish the same thing.

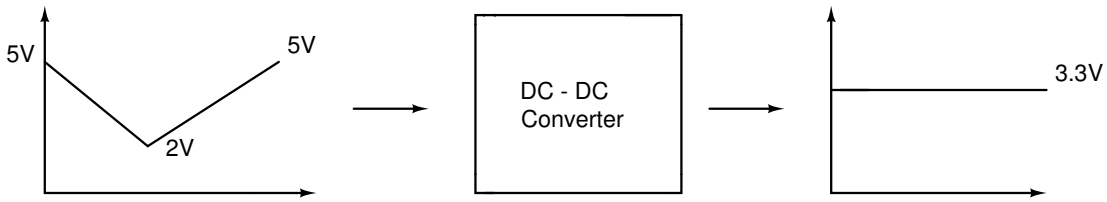


Figure 1.1: DC-DC conversion

The converters spend some amount of energy during voltage conversion. This energy spent should be kept to minimum for higher efficiency. Even though linear regulators occupy less area, they are not very efficient. They dissipate a power equals to difference in the input voltage to output voltage multiplied by amount of current drawn by the load. Hence they are not recommended for use in low power systems. A switching regulator uses inductors, capacitors and switches to do the conversion. As inductors and capacitors are ideally lossless, with less energy spent during switching and conduction, switching regulators can be designed to have better efficiency.

1.1 Single Input Single Output switching regulator

Unlike linear regulators, switching regulators can attain both lower(Buck converter) and higher(Boost converter) output voltages than input voltage. Buck converter works on the principle that when a switching voltage is passed through a low pass filter formed by L and C, a average DC voltage is obtained at capacitor output.

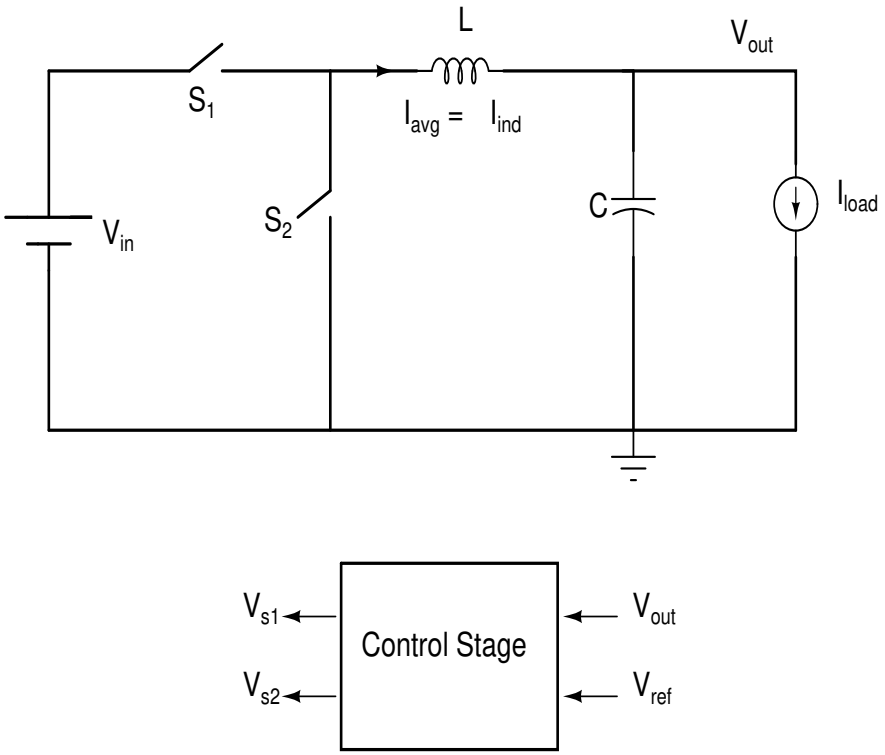


Figure 1.2: SISO converter

The input energy drawn from the supply is converted into the inductor current using switches $S_1$and S_2. When S_1 is ON and S_2 is OFF, the inductor current ramps up with the slope $\frac{(V_{in} - V_{out})}{L}$. And when S_2 is ON and S_1 is OFF, it ramps down with the slope $-\frac{V_{out}}{L}$. In steady state, the average inductor current as load current and the average voltage at the inductor input node as desired output voltage are maintained.

The output voltage needs to be regulated at the required voltage level irrespective of the variations at the battery supply voltage and load current. A control stage can be implemented to continuously monitor the output voltage and operates the switches by generating control signals V_{s1} and V_{s2}. The converter can be operated with several control schemes based on the feedback given to the control stage and the control action taken.

The detail study of the SISO converter is done in section 3.1

1.2 Motivation for Single Input Dual Output(SIDO) Converter

A typical IC has many functional blocks incorporated in it and each of them may require different supply voltages and power. A single power supply as to generate all these voltages through multiple DC-DC converters. The straight forward way is to use multiple switching regulators as shown in Figure 1.3.

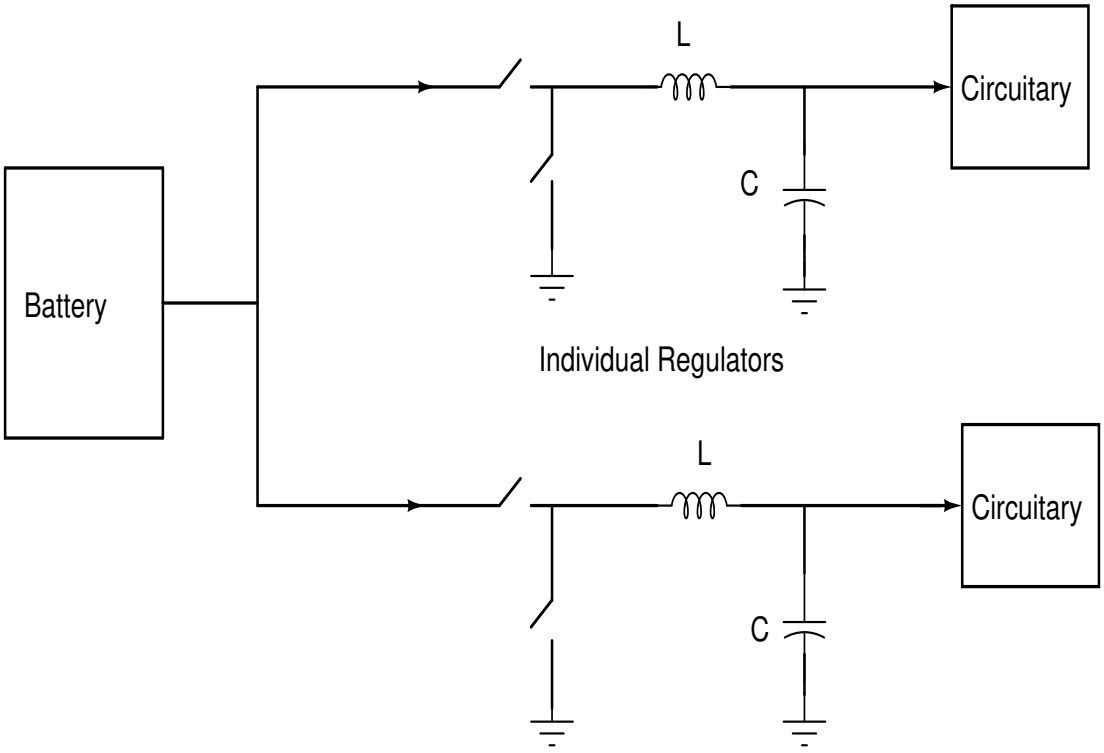


Figure 1.3: Multiple Outputs with multiple regulators

Using separate switching regulators for generating each voltage increases the total number of inductors and switches. As the inductors are bulky, the size and cost of the system increase. Moreover, as the number of magnetic storage elements increases, undesired Electromagnetic Interference (EMI) problems worsen and hence extra care is to be taken to place these elements. Thus, there is a necessity to reduce the number of inductors used in the generation of multiple supply voltages.

By switching at the output node, a single inductor can be used to generate dual output voltages as shown in Figure 1.4. These converters are referred to as Single Inductor Dual Output (SIDo) converters. These are of great demand on account of their compactness and efficient power management.

In a SIDO converter two extra output switches are added to regulate both the output

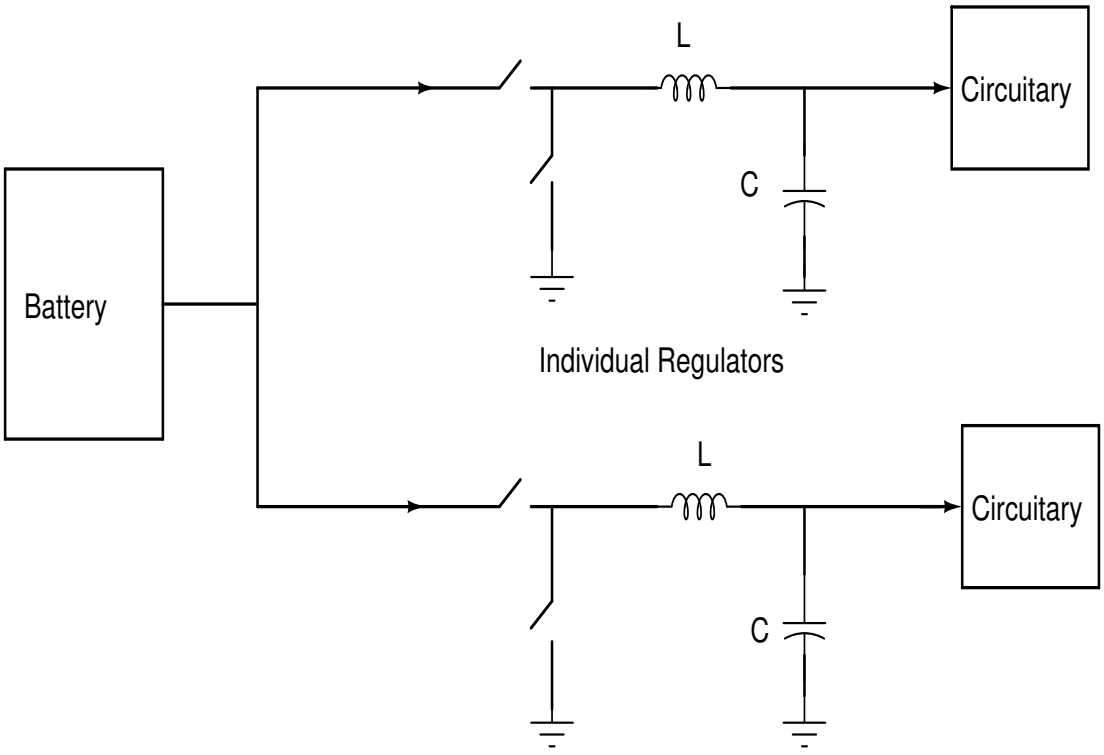


Figure 1.4: single inductor to generate multiple outputs

voltages. The average inductor current is equal to the sum of all the load currents. In steady state, the inductor current is switched between the outputs in different time slots to supply the required load current at each output. Since the inductor is an element that has memory, an undesired result of the above is cross talk between outputs, which causes variation in one output voltage due to a load transient at the other output. This variation is termed as cross-regulation.

In this work, a constant on-time (COT) scheme, which has fast transient response and good light-load efficiency, is applied to SIDo converters. Arbitration logic is proposed to control the output switches, which supports unbalanced load currents well, and with lower output ripples.

CHAPTER 2

Design Challenges

For any DC-DC Buck converter, high efficiency and output voltage regulation are the main challenges. Irrespective of the variation in load current, input voltage and other parameters, the converter should have high efficiency, small steady state output ripple and low transient overshoots and undershoots. In a SIDO converter, as the extra outputs are introduced, cross-talk between the outputs is introduced. It is of two types : steady state cross regulation and transient cross regulation. The design challenges associated with SIDO converter are discussed in this section.

2.1 Efficiency

Conduction and switching are the losses in a converter. Conduction losses increase with increased inductor DCR, switch resistances and load current. Switching losses increase with increase in parasitic capacitance of switches and frequency of operation.

In a SIDO, as the inductor current is shared between the output switches, conduction losses increases. And also as the no.of switching actions are increasing, switching losses also increase. Hence, SIDO converters will be less efficient compared to SISO, but can be designed to have more efficiency compared to a system with multiple switching regulators.

2.2 Steady state cross regulation

Output voltage should be as low as possible for a converter.As switching of the inductor current is introduced, the output ripple behaviour of the SIDO converter is different from that of the SISO converter.

The current flow in a SISO converter is shown in Figure. The output voltage ripple is formed by the inductor current ripple flowing into the output capacitor branch.

From the analysis, the steady state inductor current ripple in CCM operation is given by -

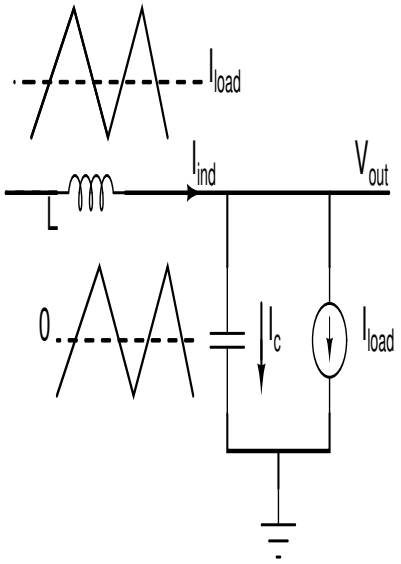


Figure 2.1: Current flow in SISO converter

$$\Delta I_{pp} = \frac{V_{out}(T_{sw} - T_{on})}{L}$$

In a SISO, the output voltage is independent of load current. Whenever there is a change in load current, the average load current in the steady state changes to load current but the ripple does not change. In a SISO converter, the inductor and output capacitor values are chosen to meet the output ripple specifications.

In a SIDO converter, the average inductor current is equal to the sum of all the average load currents, since it is time multiplexed among the outputs. When a particular output switch is ON, the inductor current flows through the corresponding output. When the switch is OFF, there is no current through the switch and in this duration the output capacitor provides the necessary load current. The average switch current is therefore equal to the corresponding load current.

The current ripple in the output switch and in the output capacitor branch are discontinuous, as shown in Figure. This output capacitor current I_{ca} depends on the steady state inductor current, which in turn depend on all the load currents. Thus, unlike in the SISO converter, the steady state output ripple is a function of all the load currents in the converter. This output ripple dependence on other output load currents is also referred as steady state cross regulation.

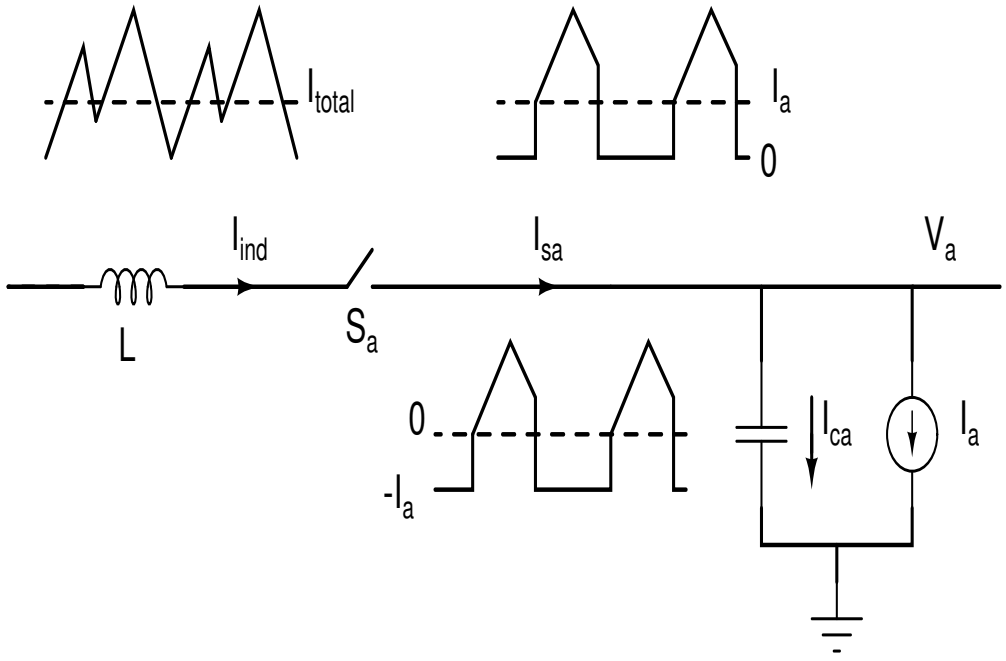


Figure 2.2: Current flow in SIDO converter

2.3 Transient cross regulation

In SISO converter, when load changes, the output experiences undershoot or overshoot as the inductor current try to adjust to the load current. In a SIDO, as there are two outputs, the adjustment is different.

In a SIDO, when load current corresponding to a output changes, the inductor tries to adjust the current to reach the new steady state. Because of this inductor current adjustment, it is not only the corresponding output but the other outputs too that experience overshoots and undershoots.This dependence is the transient cross regulation.This dependence of one output on the load currents of other outputs is harmful to the systems being powered by the converter, and hence has to be reduced.

2.4 Load current driving capability

A good power converter should be able to drive a large range of load currents. In a SIDO converter, multiple outputs should be regulated irrespective of their load currents. When the difference between load currents is large, it may not perform the conversion efficiently.The load current driving capability range of one output in the presence of dif-

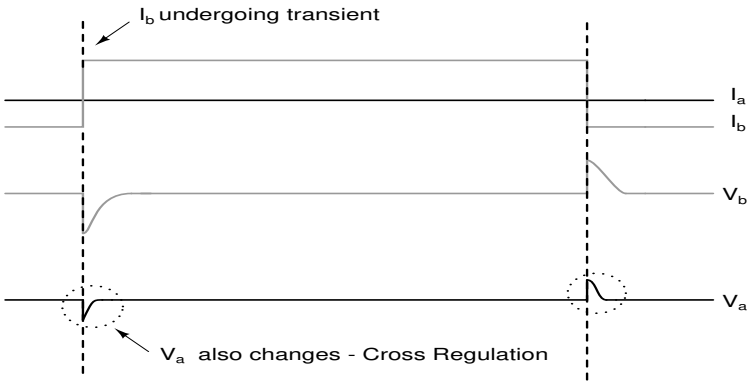


Figure 2.3: Transient cross regulation in multiple output converters

ferent combinations of other load currents is also a design concern in SIDO converters.

CHAPTER 3

Proposed architecture

Hysteric mode of control is fast and it has good light load efficiency(less switching losses as frequency decreases). So, a constant on time(COT) hysteric mode of control is proposed and implemented.In constant on-time control, the on-time for a period is kept constant. The off-time(so, the switching frequency) changes to regulate the output.

3.1 COT scheme for SISO converter

The circuit level implementation of SISO converter with COT scheme is as shown below.

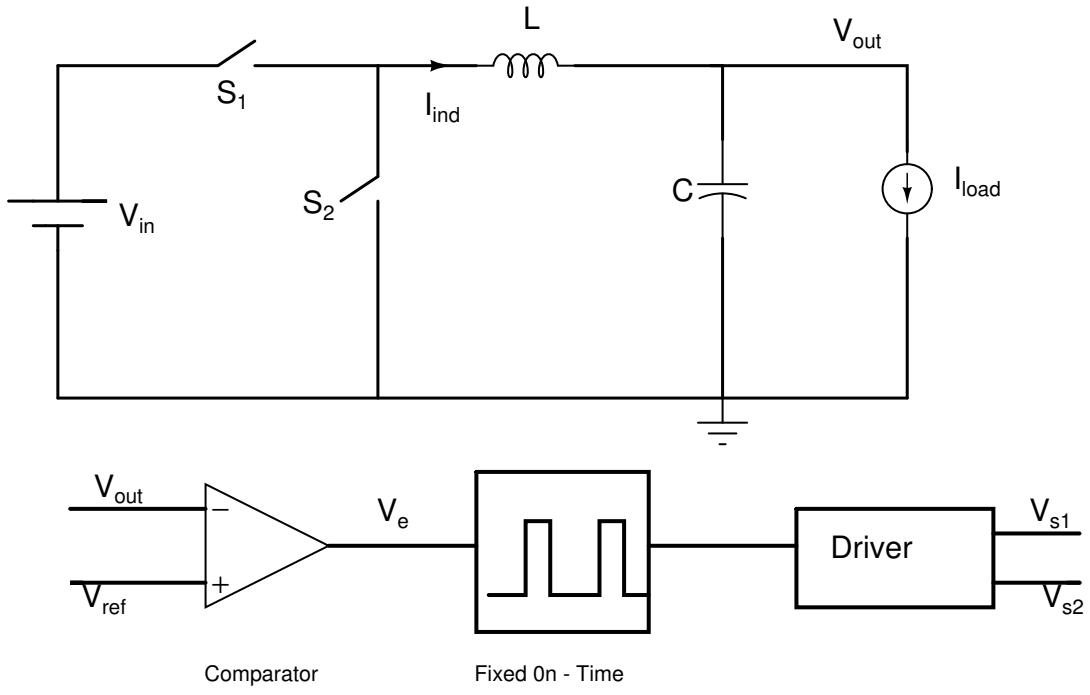


Figure 3.1: COT scheme for SISO converter

When Vout falls below Vref,S_1 is switched on for a constant time thereby increasing the inductor current. After fixed on-time duration S_2 is switched on and the inductor current starts decreasing.To stop the occurrence of immediate on-time pulses, a minimum off-time is introduced after every on-time.

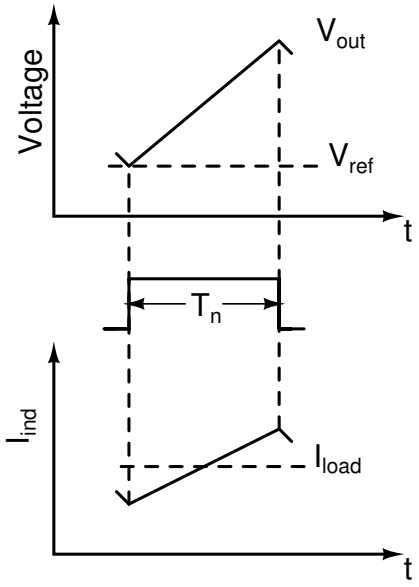


Figure 3.2: On-Time triggering

3.1.1 Time-domain analysis

CCM operation :

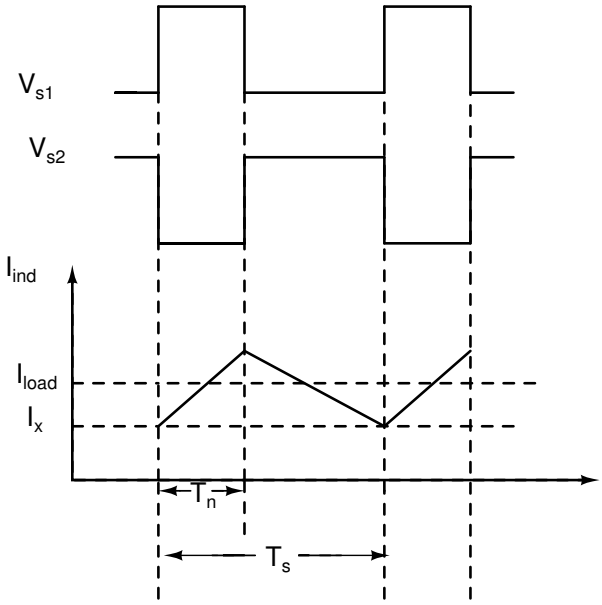


Figure 3.3: Inductor current for CCM opearation

From inductor volt-second balance -

$$\frac{(V_{in} - V_{out})}{L} T_{on} = \frac{(-V_{out})}{L}(T_{sw} - T_{on}) \quad \Longrightarrow \quad T_{sw} = \frac{V_{in} T_{on}}{V_{out}}$$

As average inductor current for one clock cycle is the load current -

$$I_{load}T_{sw} = I_xT_{sw} + \frac{1}{2}\frac{V_{out}(T_{sw} - T_{on})}{L}T_{sw} \quad \Longrightarrow \quad I_x = I_{load} - \frac{V_{out}(T_{sw} - T_{on})}{2L}$$

As T_{on} is fixed in COT scheme, Switching period T_{sw} gets fixed for any load current for a particular input and output voltage. As the load current varies, I_x varies but the ripple magnitude does not change. When I_x becomes zero, it enters DCM mode.

DCM operation :

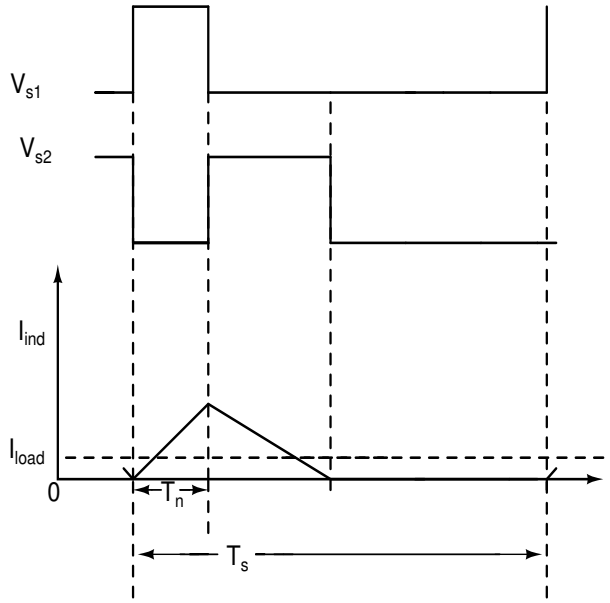


Figure 3.4: Inductor current for DCM opearation

From averaging inductor current :

$$I_{load}T_{sw} = \frac{1}{2}\frac{(V_{in} - V_{out})T_{on}}{L}\frac{V_{in}T_{on}}{V_{out}} \quad \Longrightarrow \quad T_{sw} = \frac{V_{in}(V_{in} - V_{out})T_{on}^2}{2LV_{out}I_{load}}$$

In DCM mode, the switching period depends on the load current. As the load current decreases, the switching frequency decreases and so switching losses decreases. So, it has good light load efficiency.

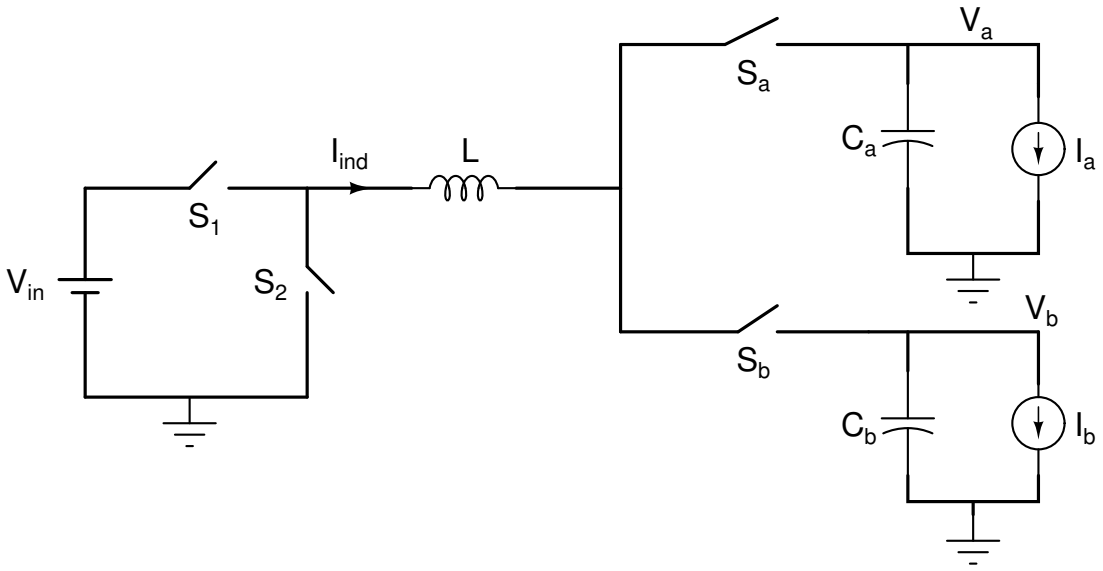


Figure 3.5: SIDO open loop circuit

3.2 COT scheme for SIDO converter

In SIDO converter, along with two power switches, two output switches are also to be controlled to regulate the output.

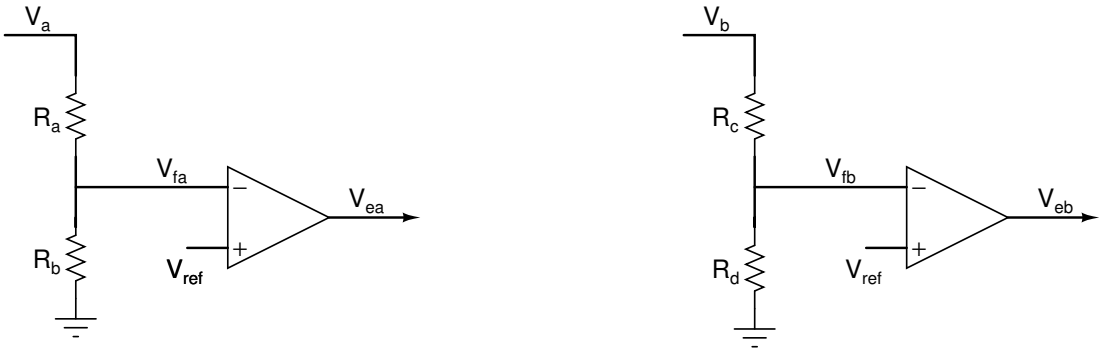


Figure 3.6: Error voltage generation

As there are two output voltages, both the outputs are to be compared to a reference voltage and two error voltages are to be generated. The outputs are normalized to reference voltage using a resistive divider as shown in figure 3.6. Even when one of the output voltages reaches reference voltage, the on-time should be triggered. So, the on-time is controlled by the 'OR'ed signal of both the output voltages as shown in figure

And for the output switches, the switch with maximum output error is selected whenever on-time is triggered as shown in figure 3.8. This is known as arbitration logic.By adopting this method, the error output voltage need not wait until the other output reaches the target voltage and the scheme maintains less error on both the outputs.

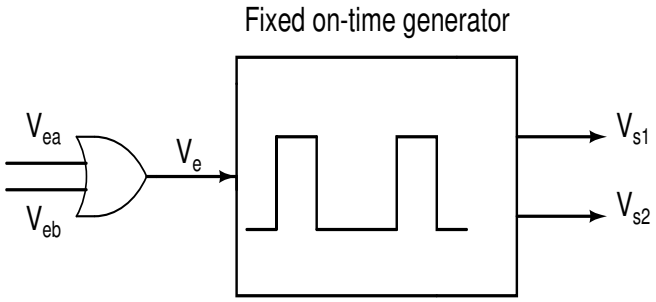


Figure 3.7: On-time triggering

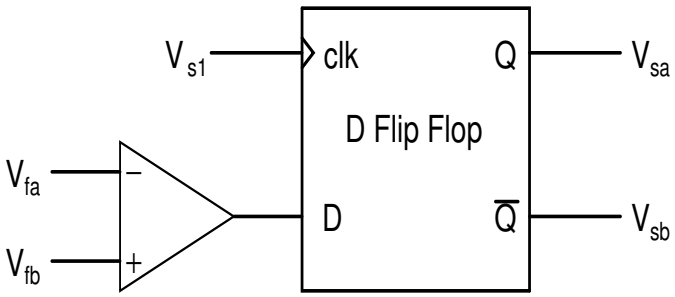


Figure 3.8: Arbitration logic for output switches

Image - Time domain waveforms of dual output converter.

The flow chart describing the functionality :

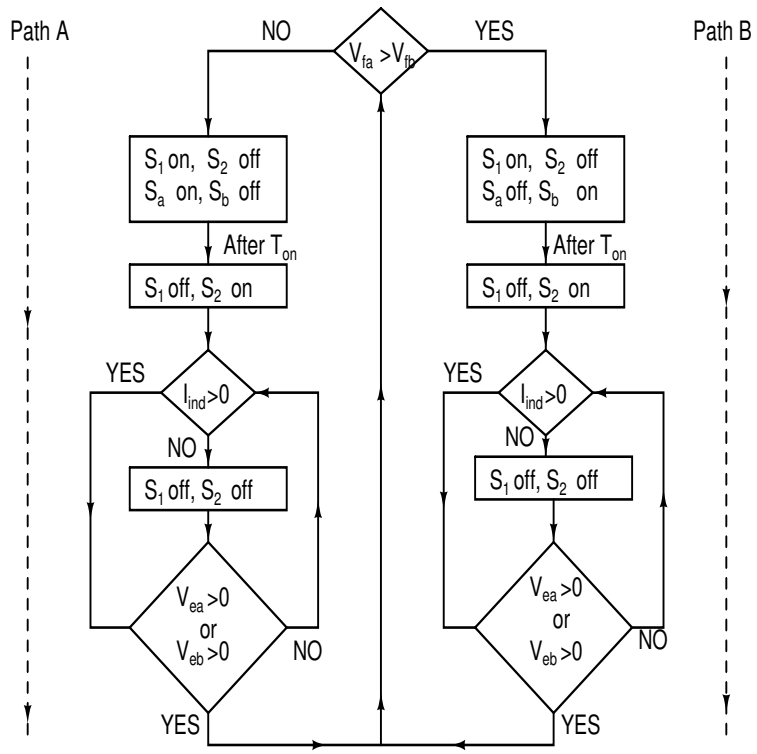


Figure 3.9: SIDO COT flow chart of operation

Depending on the feedback voltages, one of the output switches is turned ON and the inductor current is pumped to that output. Until the on-time gets over, the converter

switches do not change their state. Once the on-time is over, the converter enters into OFF duration, in which S1 is OFF and S2 is ON. In the OFF duration, the converter monitors the error voltages, and depending on the error, the next on-time is triggered. In the flow chart shown, path A serves output A, and path B serves output B. If the load currents are balanced, the operation switches between path A and path B alternately operating in AB steady state as shown in Figure

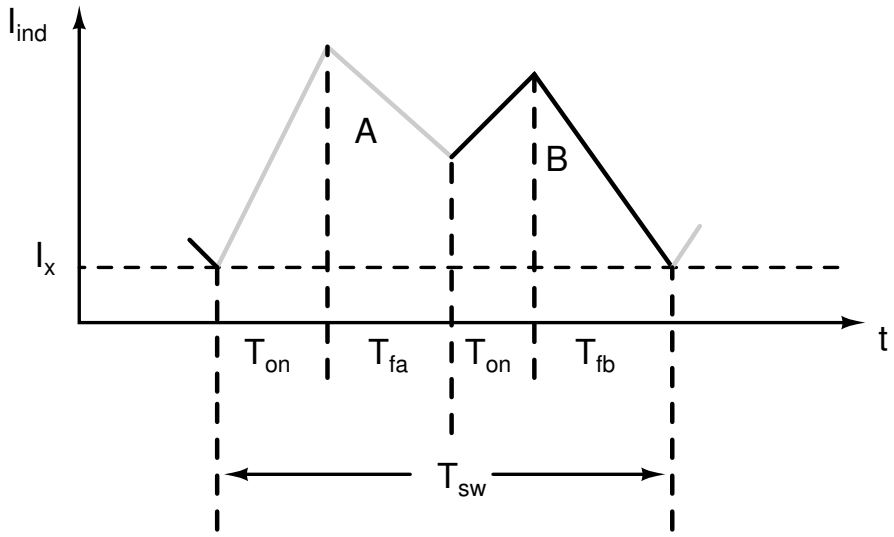


Figure 3.10: Inductor current waveform in AB steady state

With the proposed architecture, if the error on one output is large enough, then multiple continuous on-pulses can be allotted to single output. Thus, depending on the load currents, several cycles of path A followed by one or several cycles of path B may appear.

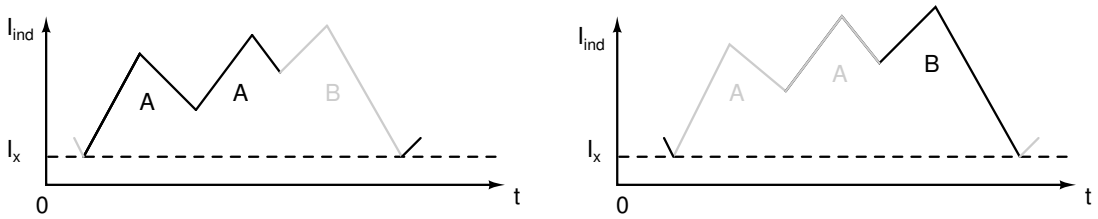


Figure 3.11: Inductor current waveform in AAB and ABB steady states

As shown in Figure, the other possible CCM steady states are AAB, ABB, . . . , etc. If the load current of A is higher than that of B, then the converter operates in steady state AA ... AB. Similarly for higher load current on output B, it operates in ABB...B. Thus, unbalanced loads are supported well and the supported independent load current range is high.

By introducing conditions on inductor current zero crossing value, DCM operations are also supported by the converter as shown in Figure. At any time during the off

duration, if the inductor current becomes zero, both the switches S_1 and S_2 are turned off to avoid reverse current. Thus, the inductor current stays at zero. In DCM, as shown in Figure, different steady states are possible depending on the load currents.

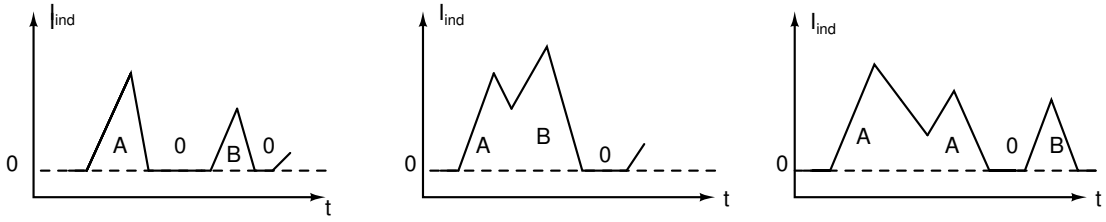


Figure 3.12: SIDO COT possible steady states in DCM

3.2.1 Time domain analysis for SIDO converter

Figure 4.9: SIDO converter inductor current waveform in AB steady state.

T_{sw} - switching period

T_{on} - on-time of architecture

ϕ_a - duration for which the output switch S_a is ON

ϕ_b - duration for which the output switch S_b is ON

T_{fa} - off-time of switch S_a

T_{fb} - off-time of switch S_b

I_x - Inductor current starting point in ϕ_a

I_y - Inductor current starting point in ϕ_b

As average current through each output switch is the corresponding load current -

$$I_a T_{sw} = I_x \phi_a + \frac{(V_{in} - V_a)}{2L} T_{on}^2 + \frac{V_a}{2L} T_{fa}^2 + T_{fa}\Big(\frac{(V_{in} - V_a)}{L} T_{on} - \frac{V_a}{L} T_{fa}\Big)$$

$$I_b T_{sw} = I_x \phi_b + \frac{(V_{in} - V_b)}{2L} T_{on}^2 + \frac{V_b}{2L} T_{fb}^2 + T_{on}\Big(- \frac{(V_{in} - V_b)}{L} T_{on} + \frac{V_b}{L} T_{fb}\Big)$$

From the AB steady state inductor current waveform, we have -

$$I_x + \frac{(V_{in} - Va)}{L} T_{on} - \frac{V_a}{L} T_{fa} \quad = \quad I_y$$

$$I_y + \frac{(V_{in} - Vb)}{L} T_{on} - \frac{V_b}{L} T_{fb} \quad = \quad I_x$$

$$T_{on} + T_{fa} \quad = \quad \phi_a$$

$$T_{on} + T_{fb} \quad = \quad \phi_b$$

On solving, the following expressions are obtained:

$$T_s \quad = \quad \frac{V_{in} T_{on}}{(I_a V_a + I_b V_b)} \Big[I_a + I_b - \frac{(V_a + V_b) T_{on}}{4L} + \sqrt{D} \Big]$$

where,

$$D \quad = \quad \Big[I_a + I_b + \frac{(V_a + V_b) T_{on}}{4L} \Big]^2 + \frac{(V_a - V_b)(I_a - I_b) T_{on}}{L}$$

$$I_x = I_a + I_b + \frac{V_{in} T_{on}^2}{L T_{sw}} - \frac{V_b \phi_b}{2L} \qquad ; \qquad I_y = I_a + I_b + \frac{V_{in} T_{on}^2}{L T_{sw}} - \frac{V_a \phi_a}{2L}$$

For $V_a \neq V_b \quad \Longrightarrow \quad \phi_a = \frac{2 V_{in} T_{on} - V_b T_{sw}}{V_a - V_b} \quad ; \quad \phi_b = \frac{2 V_{in} T_{on} - V_a T_{sw}}{V_b - V_a}$

For $V_a = V_b = V \quad \Longrightarrow \quad \phi_a = T_{sw} \left(\frac{2 I_a + \frac{V T_{on}}{2L}}{2(I_a + I_b) + \frac{V T_{on}}{L}} \right) ; \phi_b = T_{sw} \left(\frac{2 I_b + \frac{V T_{on}}{2L}}{2(I_a + I_b) + \frac{V T_{on}}{L}} \right)$

This is the behaviour of AB steady state current wave form. Here the switching time period and phase durations are dependent on load current whereas in CCM opearation of SISO converter, the switching time period is independent od load current i.e., $T_{sw} = \frac{V_{in} T_{on}}{V_a}$.

The conditions for SIDO to operate in AB steady state are -

$I_x > 0 \quad ; \quad I_y > 0 \quad ; \quad \phi_a > T_{on} \quad ; \quad \phi_b > T_{on}$

If the above conditions are not met, then the operation will be in other CCM steady

states such as AA...AB, ABB... B, or the converter might be in DCM operation.

3.3 ERG filter

We are comparing the normalized output voltage to the reference voltage to generate the error voltage. But the system is stable only when output voltage has higher ripple i.e. when output cap has higher ESR.For low ESR capacitors,the amount of inductor current ripple that gets added at the output is less, leading to instability. The ESR resistance helps in stabilising the system at the cost of higher voltage ripple.

Instead of sensing the inductor current ripple and adding it to the loop, the ripple can be emulated through an RC network. The RC network is called Emulated Ripple Generation(ERG) filter. It has two series connected R ans C connected over inductor as shown in figure. First R ans C circuit acts as low pass fliter as voltage is taken out from capacitor. This voltage contains small inductor ripple over V_{out}. The second R and C acts as high pass filter as voltage is taken out from resistor. It has just the ripple and no DC voltage.

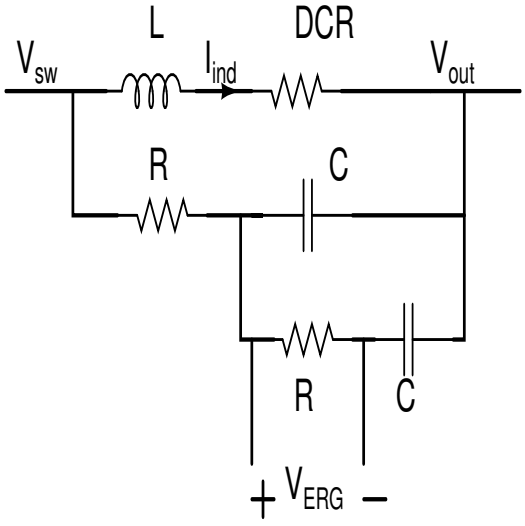


Figure 3.13: ERG filter

$$I_{ind} = \frac{1}{L}\int (V_{sw} - V_{out})dt$$

$$V_{ERG} = \frac{1}{RC}\int (V_{sw} - V_{out})dt$$

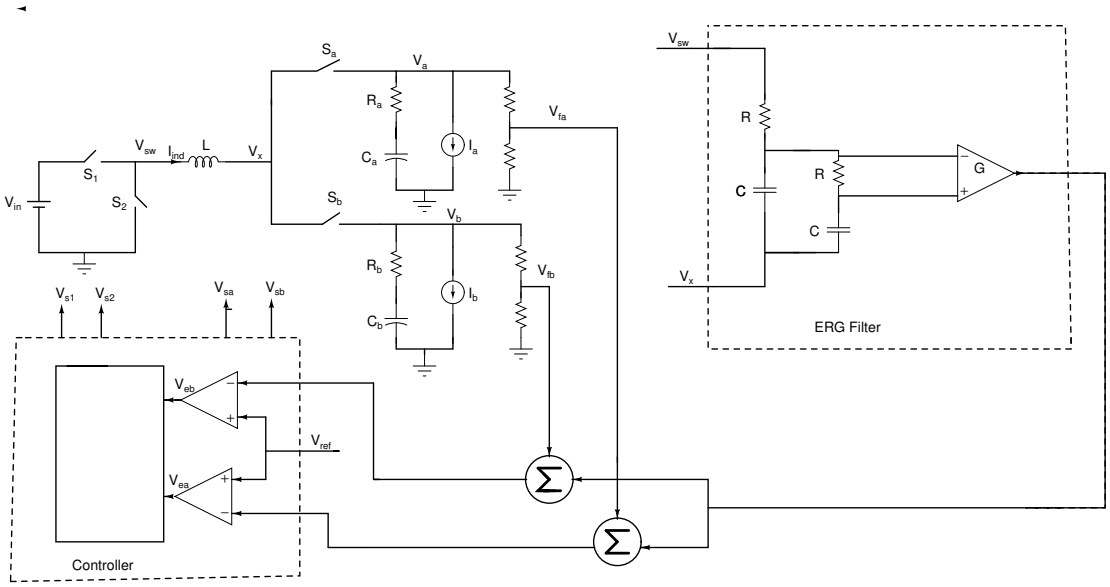


Figure 3.14: SIDO with controller and ERG filter

3.4 The constant on-time circuit implementation

The linear charging and discharging of a capacitor can be used to generate the constant on-time. whenever an error voltage is generated,its edge is detected by edge detector. Then it is fed to a SR-latch which controls the switch in parallel to the capacitor as shown in the figure. to control the charge and discharge states.

When an edge is detected, the switch controlled by Q_{bar} is open and the current source starts charging the cap linearly until it reaches V_{ref2}. The on-time is triggered during this period and it depends on the current and capacitor values. Then SR latch resets and the switch controlled by Q_{bar} closes forcing the charge on capacitor to zero.

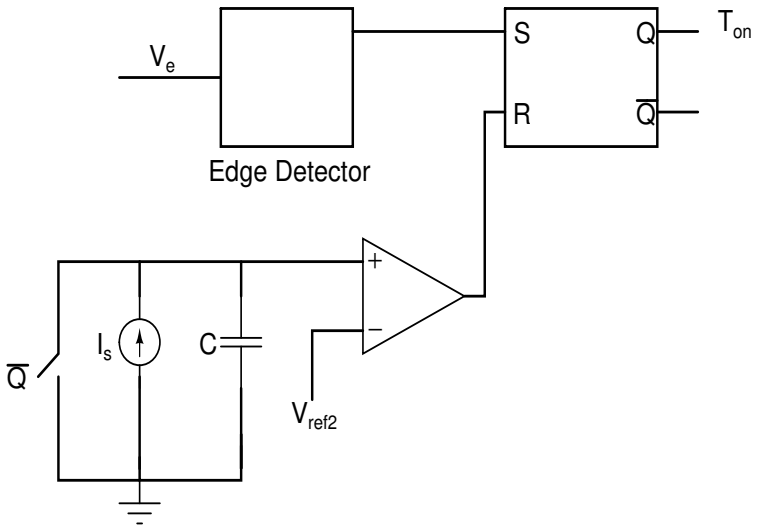


Figure 3.15: on-time implementation with capacitor charge and discharge circuit

$$\frac{dV}{dt} = \frac{I_s}{C}$$

$$\frac{\Delta V}{\Delta t} = \frac{I_s}{C} \quad \Longrightarrow \quad \frac{V_{ref2}}{T_{on}} = \frac{I_s}{C}$$

$$\Longrightarrow \quad T_{on} = \frac{C}{I_s} V_{ref2}$$

3.5 Frequency Regulaion loop

In constant on-time mode of control, the operating frequency varies a lot. As properties like inductance depends extensively on frequency of operation, a frequency regulation loop is implemented to maintain a constant frequency of 1MHz.

A Frequency Locked Loop(FLL) is an electronic system that compares the frequency of a signal to a reference signal and try to decrease or increase the frequency of the signal until it reaches to that of reference. It has four stages for correction of frequency:

3.5.1 Phase frequency detector:

It compares the phases of the two signals. The circuit implementation of PFD -

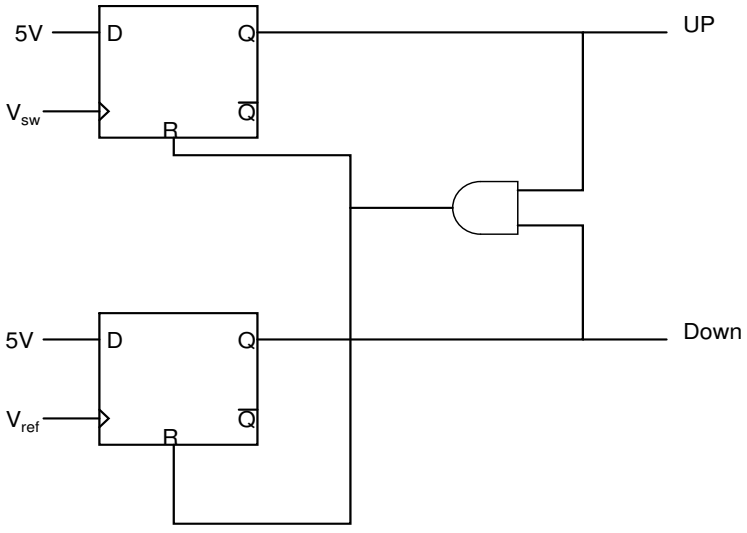


Figure 3.16: Phase Frequency Detector

The clock of one positive edge triggered D flipflop is connected to actual signal while the other to Reference signal. If the frequency of system is greater than that

of reference, then when system frequency changes from 'LOW' to 'HIGH', 'UP' also changes from 'LOW' to 'HIGH' but becomes 'LOW' as soon as reference signal becomes 'HIGH'. So, in this case signal 'UP' provides phase difference between two signals and vice-versa i.e., if the reference frequency is higher than frequency of the system the output 'down' gives the phase error.

3.5.2 Cycle Slip Dtector:

It detects the cycle slip between the frequencies of two signals i.e., it gets triggered when the PFD error reaches one time period. The outputs of PFD are given to cycle slip detectoe as shown in fig. along with the frequencies to determine the cycle slips.In FLL if the phase difference is constant, it doesnâĂŹt contribute to the error. Only the increasing or decreasing phase error which reaches the time period of the respective frequency (cycle slips) is accumulated.

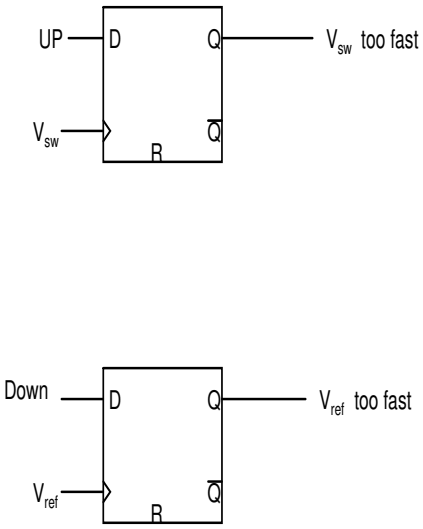


Figure 3.17: Cycle Slip Detector

3.5.3 Accumulator:

It accumulates the no. clock cycles FLL loop slipped. It is an up/down counter. The counter value basically gives the measure of frequency differnce between signals and which one is leading. If the system frequency is higher(cycle slip occurs at output corresponding to system frequency), the counter counts down ans vice-versa. The implementation of cycle slip detection and counter is as shown in the fig. the figure.

In the logic circuit makes sure that the error does not overflow beyond the maximum

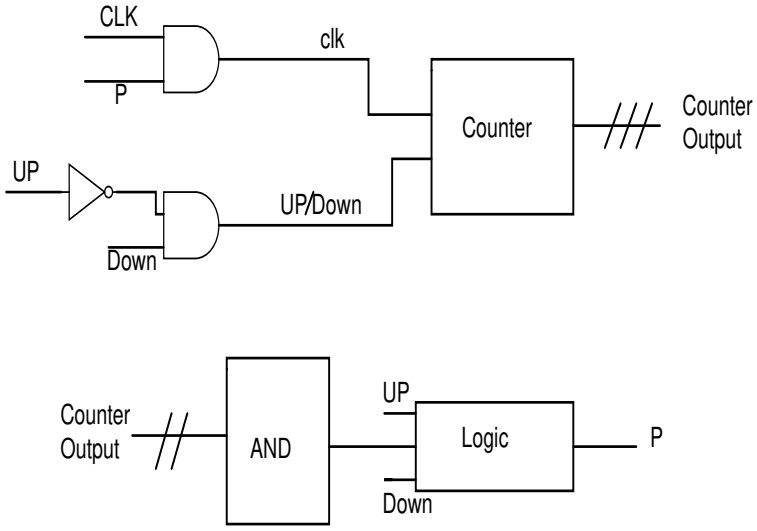


Figure 3.18: Counter for accumulating the error

value of counter(to avoid counter going to '0000' state from '1111' state). The logic stops the counter once it reaches the maximum value till it receives a cycle slip input to decrease the counter value.

3.5.4 Error Correction:

The frequency can be changed by changing the ON-time as the voltage regulation loop will take care of duty cycle. As on-time is a function of current, increase or decrease in current, increases or decreases its frequency. Current is controlled by the counter bits. A current DAC is used which takes counter bits as input and generate current according to binary weighted bits (1LSB, 2LSB, 4LSB, 8LSB).

The error in frequency greater than one time period i.e., error detected by cycle slip detector are corrected by current DAC through counter. The phase errors less than one cycle are corrected using proportional path with two current sources controlled by 'up' and 'down' pulses.

The current controlled by 'up' should decrease the system frequency; hence it should draw current from the circuit. And similarly the current controlled by 'down' should increase the system frequency; hence it should pump current into the circuit. Using proportional path the voltage slope of charging of the capacitor increases or decreases for some part of the charging curve of capacitor changing the value of ON-time.

Let the proportional path be active till the capacitor charges till V_1 i.e., up or down pulse is high till V_1 and turns off after that -

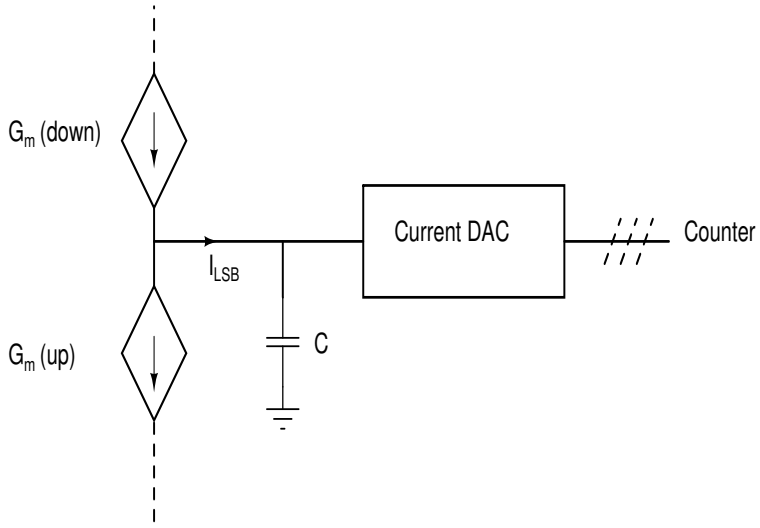


Figure 3.19: Proportional path of current in capacitor controlled by 'up' and 'down' pulses

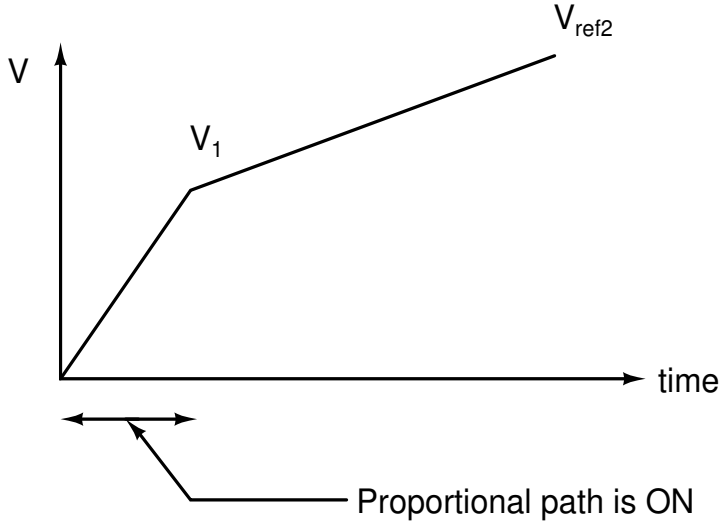


Figure 3.20: Charging curve with proportional path correction

$$T_{on} = \frac{C}{I_{DAC} \pm I_{LSB}} V_1 + \frac{C}{I_{DAC}} (V_{ref2} - V_1)$$

Where $I_p$current from the proportional path

I_{DAC} current from the current DAC

CHAPTER 4

Simulation Results

A SIDO converter with the following specifications is designed :

Input Supply Voltage - 3.3V

Output Voltages - 1.8V, 1.2V

Load Currents - upto 500mA on each output independently

Cross regulation - Low

Efficiency - High

Output ripples - Low

Switching frequency - 1 MHz.

A SIDO converter is designed using ideal SPICE models in Cadence. The chosen parameters are listed below -

Inductance = $3\mu H$ with DCR = $100m\Omega$

Output capacitance = $4.7\mu F$ with ESR = $10m\Omega$

On time = 240 ns

Minimum OFF time = 30 ns

Reference voltage = 0.7 V

Feedback resistors = 785 k, 500 k, 350 k, 500 k

When a output switch is OFF, as the corresponding output capacitor provides the required load current, the output voltage ripple can be given as -

$$\Delta V_a = \frac{I_a \phi_b}{C} \approx \frac{(2V_{in}T_{on})I_aI_b}{(I_aV_a + I_bV_b)C} \quad \text{and} \quad \Delta V_b = \frac{I_b \phi_a}{C} \approx \frac{(2V_{in}T_{on})I_aI_b}{(I_aV_a + I_bV_b)C}$$

So, with this control scheme, the ripple at both the output capacitors is approximately same. For the ripple to be minimum, the output capacitor value is selected accordingly.

The inductor current slopes down or up in all the four phases of a cycle and the maximum of them is the inductor ripple.

$$\Delta I = Max\left(\frac{(V_{in}-V_a)T_{on}}{L}, \frac{V_b(\phi_b - T_{on})}{L}, \frac{V_a(\phi_a - T_{on})}{L}, \frac{(V_{in}-V_b)T_{on}}{L}\right)$$

The inductor value is choosen to minimise the inductor current ripple.

4.1 Steady State Behaviour :

4.1.1 $I_a = 200mA \quad I_b = 400mA$

Loads as $I_a = 200mA$ and $I_b = 400mA$ comes under balanced load case and the outputs settle in AB mode.

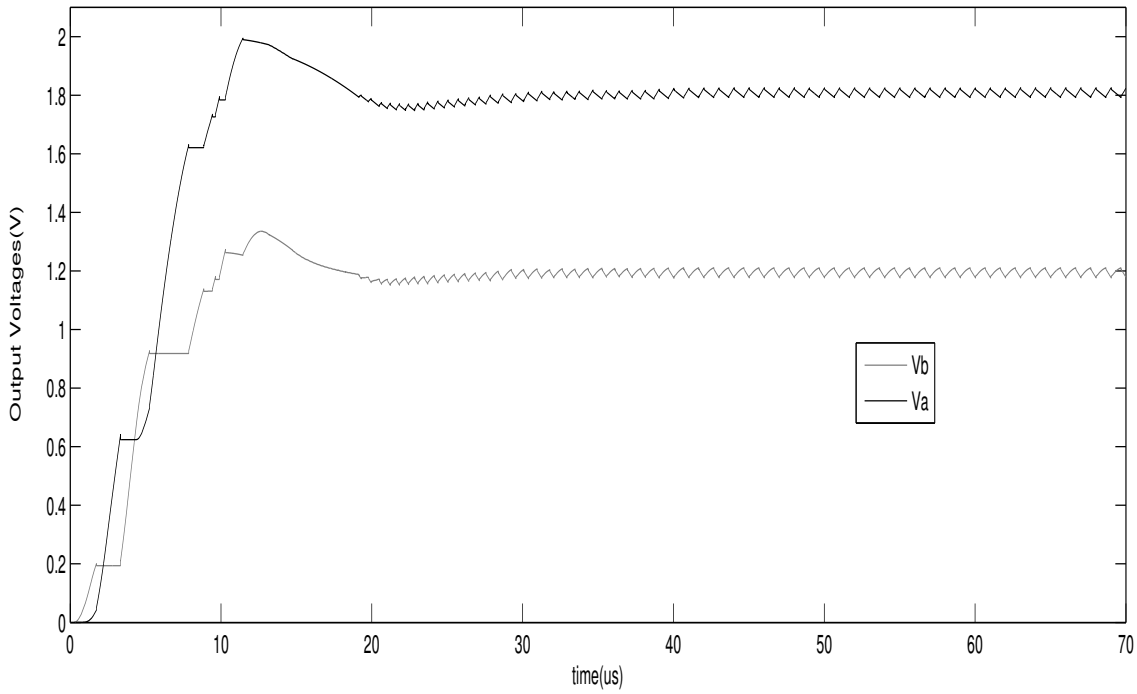


Figure 4.1: Startup and steady state waveforms of output voltages for $I_a = 200mA$ and $I_b = 400mA$

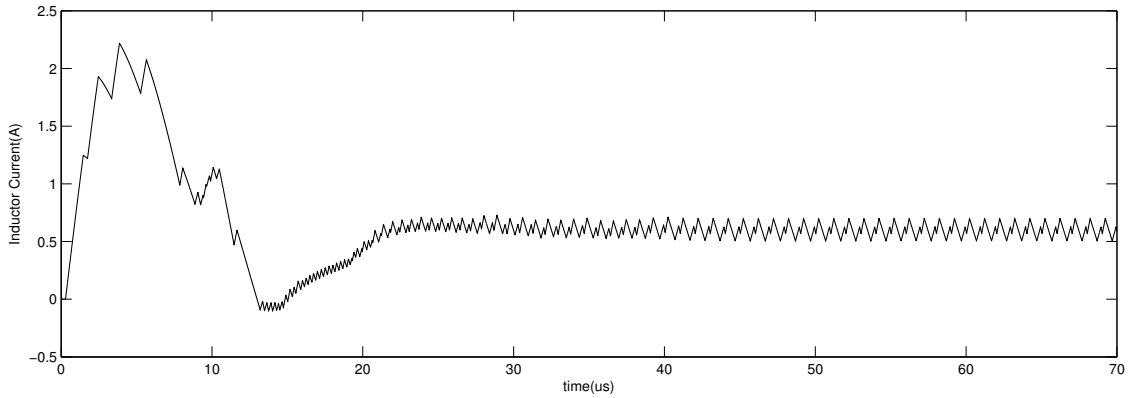


Figure 4.2: Startup and steady state waveforms of inductor current for $I_a = 200mA$ and $I_b = 400mA$

Output Voltages ripple:

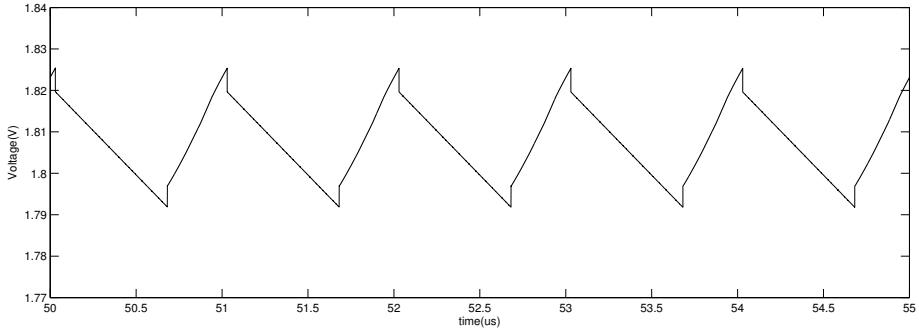


Figure 4.3: V_a ripple for $I_a = 200mA$ and $I_b = 400mA$

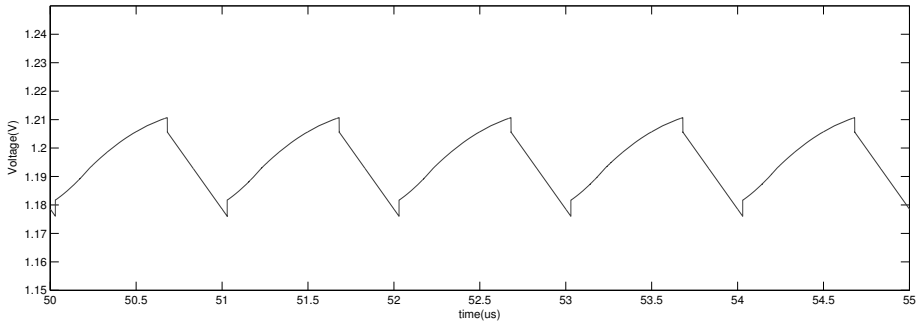


Figure 4.4: V_b ripple for $I_a = 200mA$ and $I_b = 400mA$

$\Delta V_a = 33mV$ and $\Delta V_b = 31mV$

Inductor ripple :

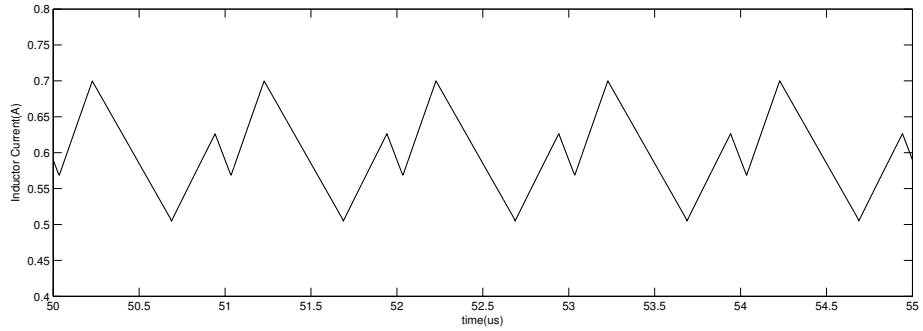


Figure 4.5: Inductor current ripple for $I_a = 200mA$ and $I_b = 400mA$

Inductor ripple = $190mA$

4.1.2 $I_a = 200mA \quad I_b = 30mA$

Loads as $I_a = 200mA$ and $I_b = 30mA$ comes under unbalanced load case and the outputs settle in AA...B mode.

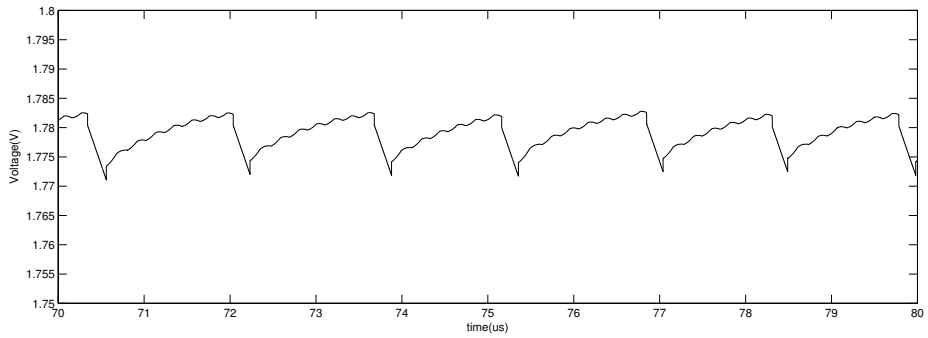


Figure 4.6: V_a for $I_a = 200mA$ and $I_b = 30mA$

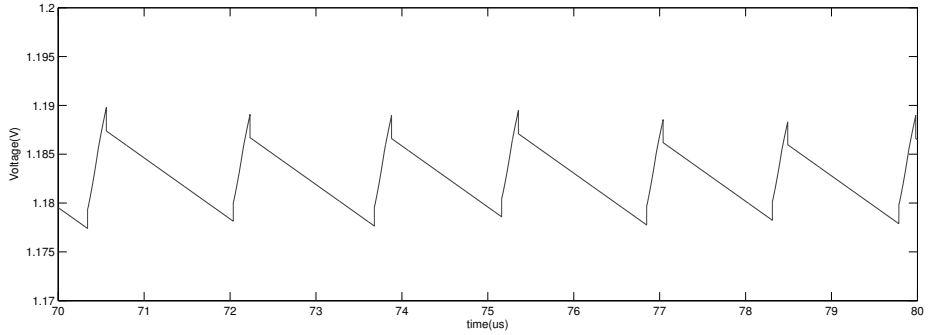


Figure 4.7: V_b for $I_a = 200mA$ and $I_b = 30mA$

$\Delta V_a = 12mV$ and $\Delta V_b = 13mV$

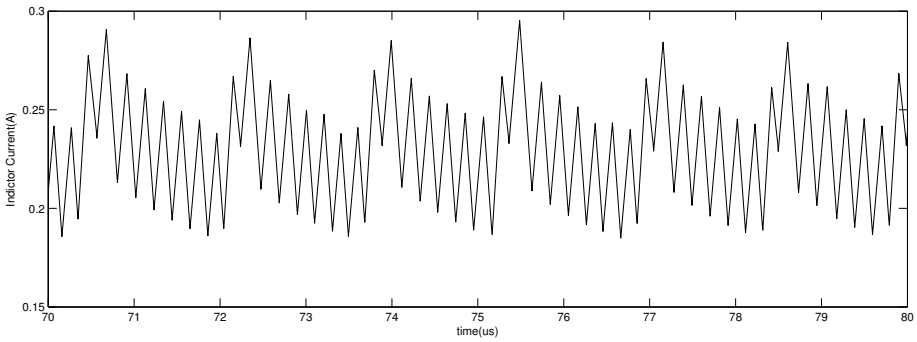


Figure 4.8: Inductor current for $I_a = 200mA$ and $I_b = 30mA$

Inductor ripple = $100mA$

4.1.3 $I_a = 10mA \quad I_b = 30mA$

For light load currents as $I_a = 10mA$ and $I_b = 30mA$, the converter operates in DCM mode.

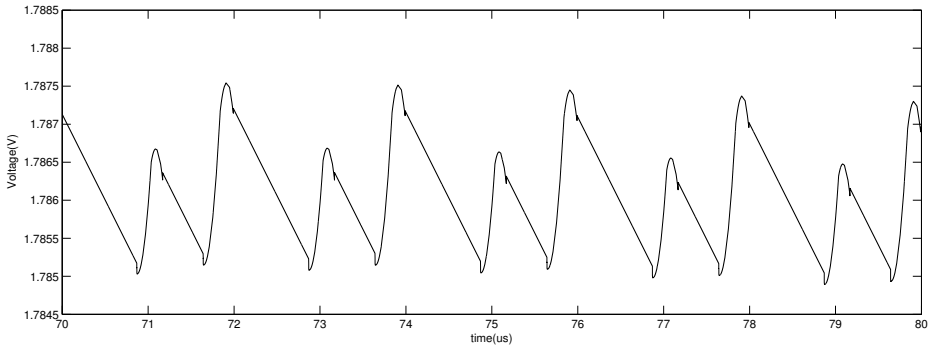


Figure 4.9: V_a for $I_a = 10mA$ and $I_b = 30mA$

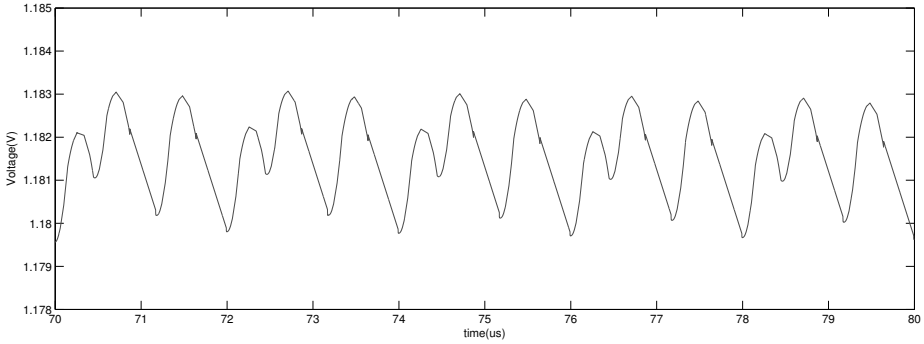


Figure 4.10: V_b for $I_a = 10mA$ and $I_b = 30mA$

$\Delta V_a = 2.5mV$ and $\Delta V_b = 3mV$

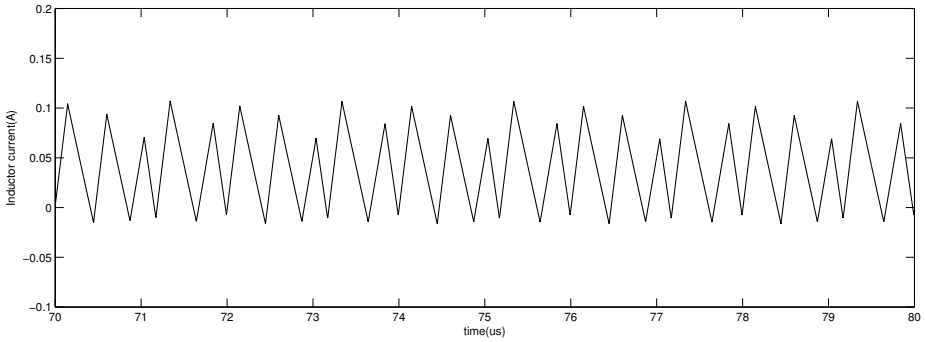


Figure 4.11: Inductor current for $I_a = 10mA$ and $I_b = 30mA$

Inductor ripple = $100mA$

4.2 Load transient Behaviour :

4.2.1 $I_a = 200mA \longrightarrow 300mA$ and $I_b = 400mA$

At balanced load currents of $I_a = 200mA$ and $I_b = 400mA$, a load step at I_a of $100mA$ is applied within $1\mu s$. The change in inductor and output voltages are as shown in figure below.

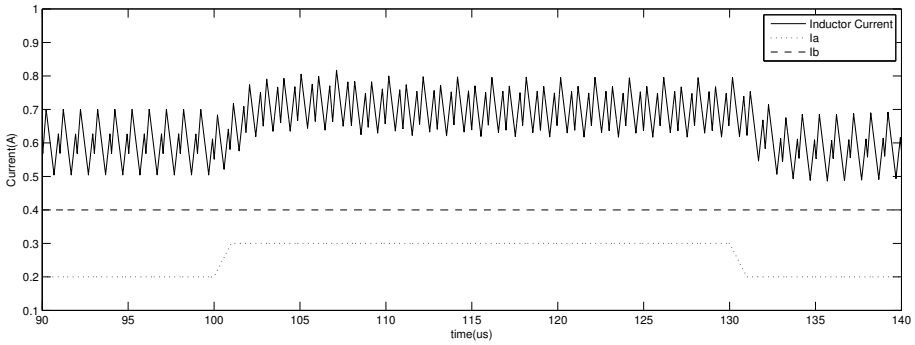


Figure 4.12: Load response: $I_a = 200mA \longrightarrow 300mA$ and $I_b = 400mA$

With the load increment, the steady state ripples have changed at V_a from 33mV to 44mV and at V_b from 31mV to 42mV. The undershoots at load increment are observed to be 16mV at V_a and 4mV at V_b.

The cross regulation performance, which is a ratio of output voltage variation to the load current variation of the other output is calculated to be 160μV/mA.

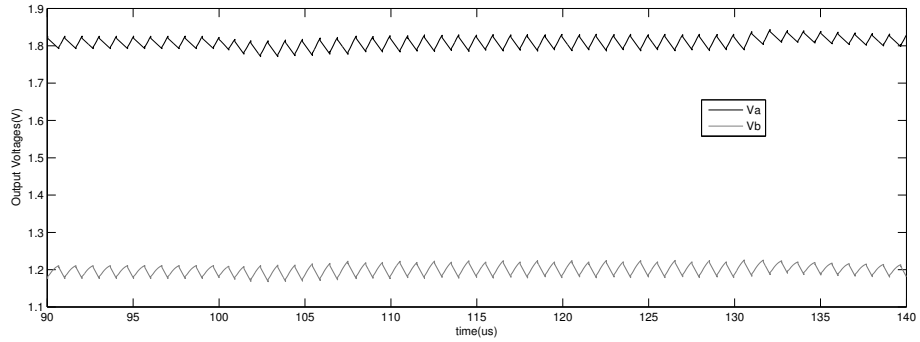


Figure 4.13: Output Voltages during load transient

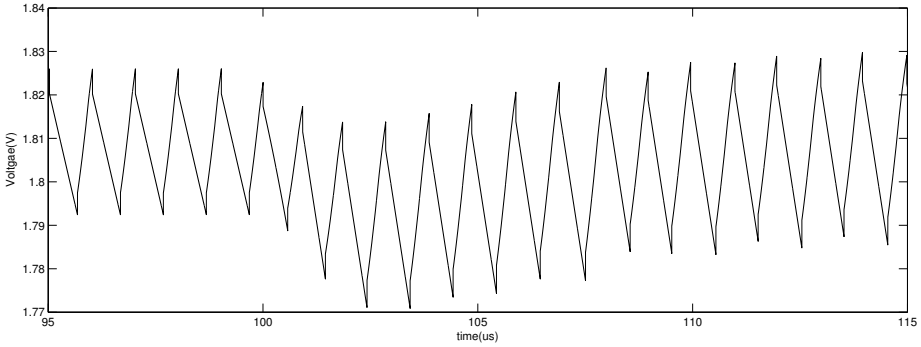


Figure 4.14: V_a ripple change for $I_a = 200mA \longrightarrow 300mA$ and $I_b = 400mA$

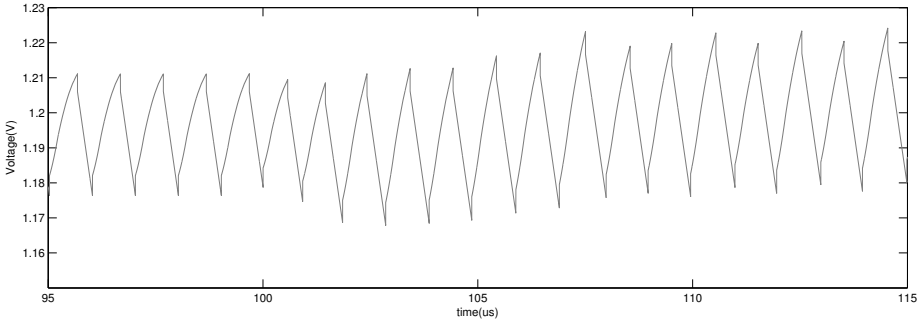


Figure 4.15: V_b ripple change for $I_a = 200mA \longrightarrow 300mA$ and $I_b = 400mA$

4.2.2 $I_a = 30mA \longrightarrow 200mA$ and $I_b = 30mA$

At low load currents of $I_a = 30mA$ and $I_b = 30mA$, a load step at I_a of $170mA$ is applied within $1\mu s$. The change in inductor and output voltages are as shown in figure.

With the load increment, the steady state ripples have changed at V_a from 4mV to 11mV and at V_b from 4mV to 12mV. The undershoots at load increment are observed to be 32mV at V_a and 15mV at V_b.
The cross regulation = 150μV/mA.

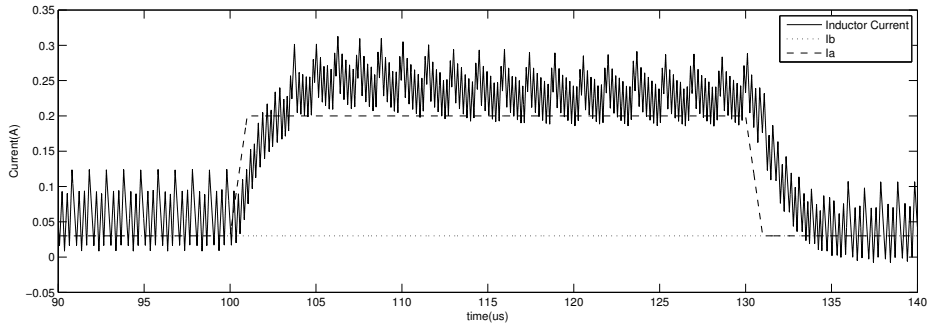


Figure 4.16: Load response: $I_a = 30mA \longrightarrow 200mA$ and $I_b = 30mA$

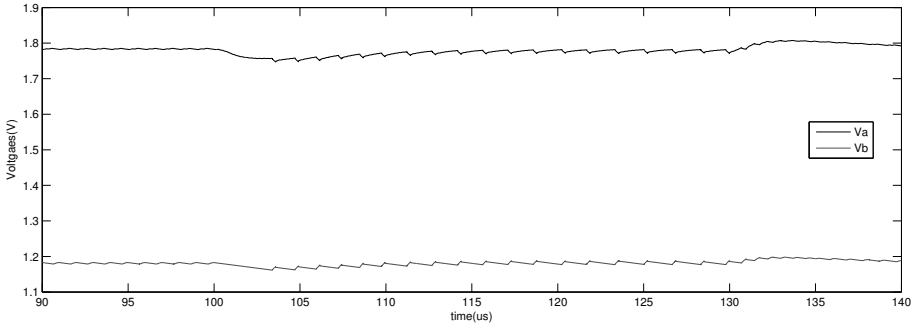


Figure 4.17: Output Voltages during load transient

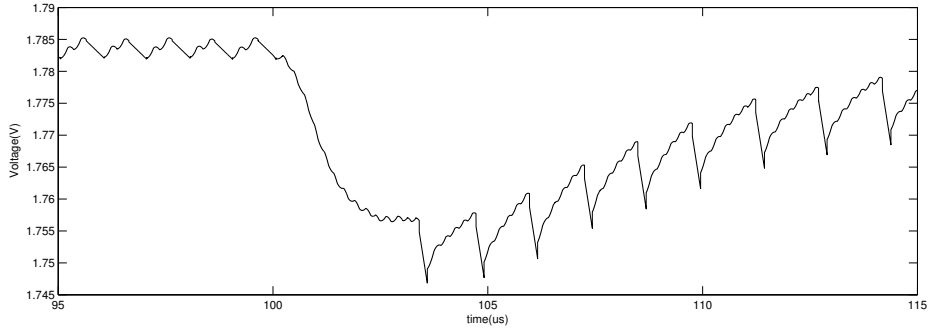


Figure 4.18: V_a ripple change for $I_a = 30mA \longrightarrow 200mA$ and $I_b = 30mA$

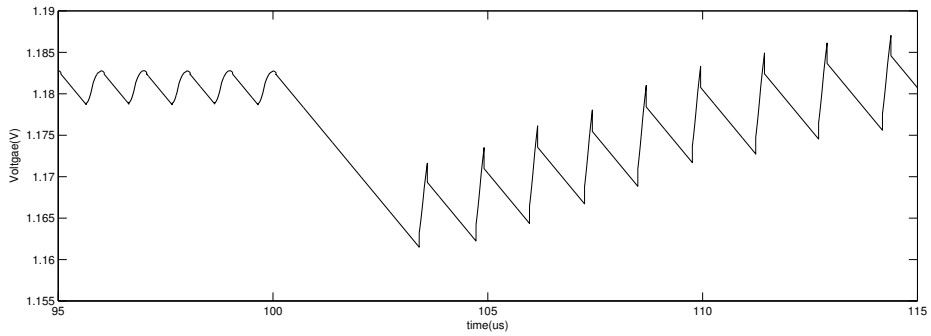


Figure 4.19: V_b ripple change for $I_a = 30mA \longrightarrow 200mA$ and $I_b = 30mA$

4.3 FLL loop response

FLL loop is simulated for $I_a = 200mA$ and I_b is changed from 100mA to 200mA at 500μs and back to 100mA at 1ms.

When the load is applied the frequency peaks to 1.5MHz from 1MHz. The frequency drops to 800KHz at load release.

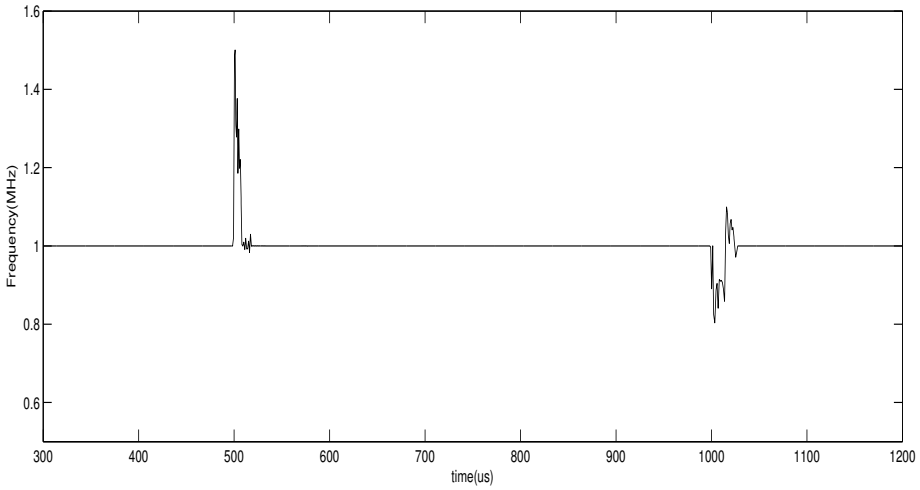
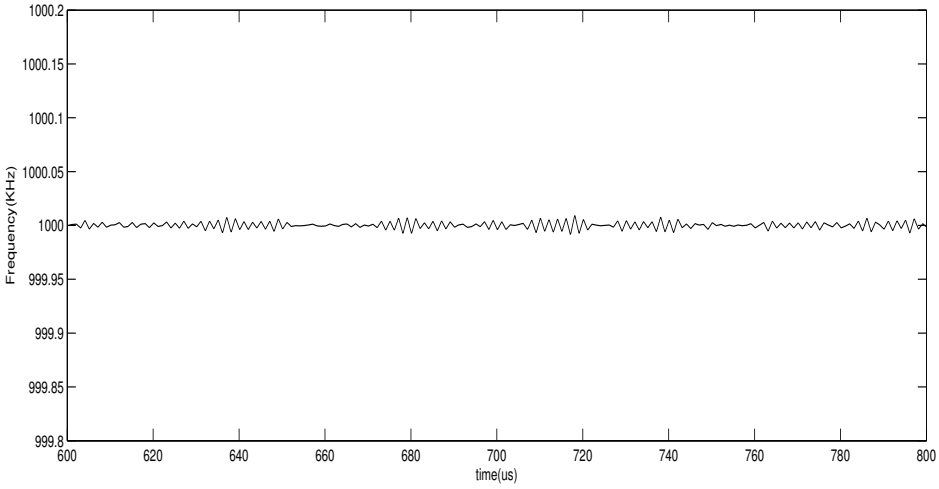


Figure 4.20: Frequency change with load transient

When loop is locked, there is an error of 15Hz of frequency



The output switch pulse is maintained at a time period of 1μ s

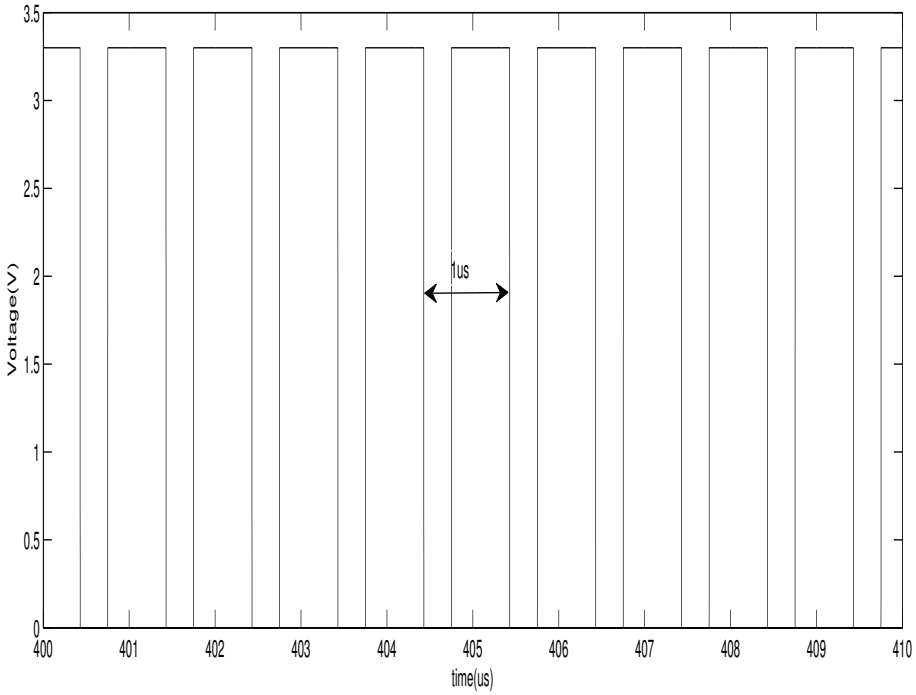


Figure 4.21: output switch pulse

The cycle slip detectors change with the load transient as shown -

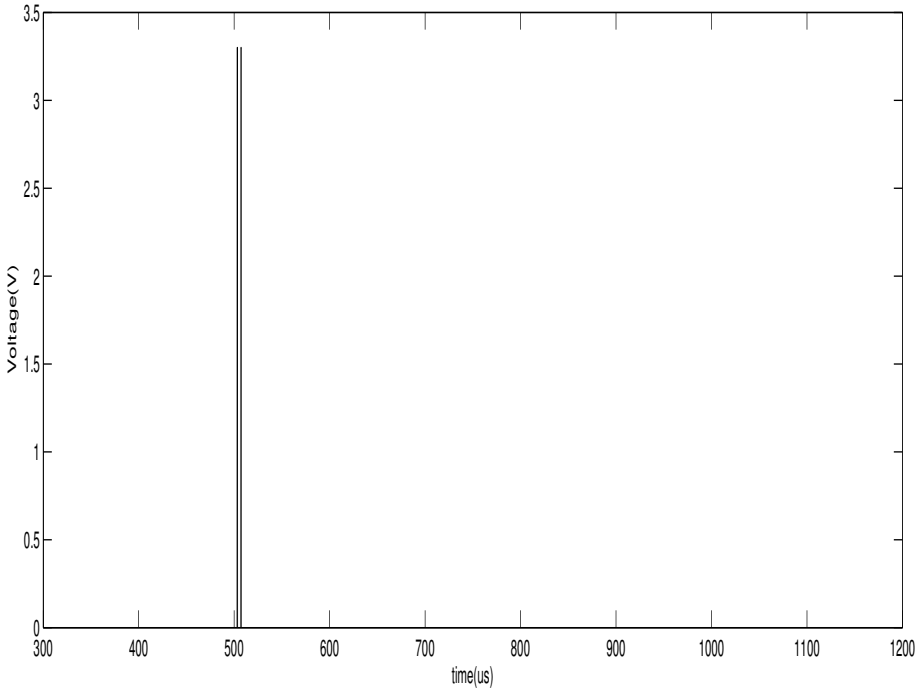


Figure 4.22: Cycle slip detector output(up)

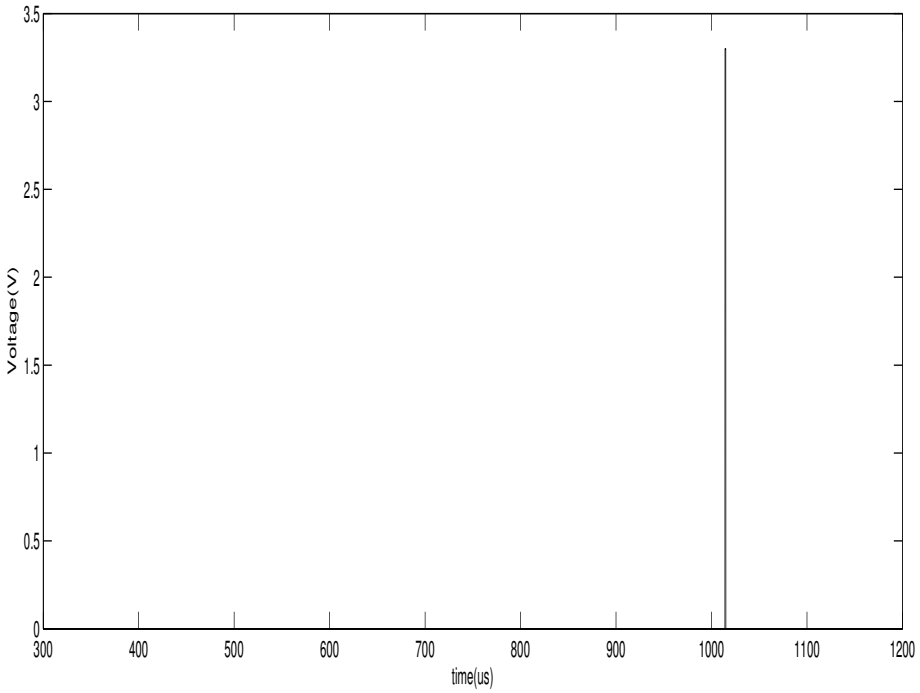


Figure 4.23: Cycle slip detector output(down)

The 4-bit counter outputs change with the transient as shown -

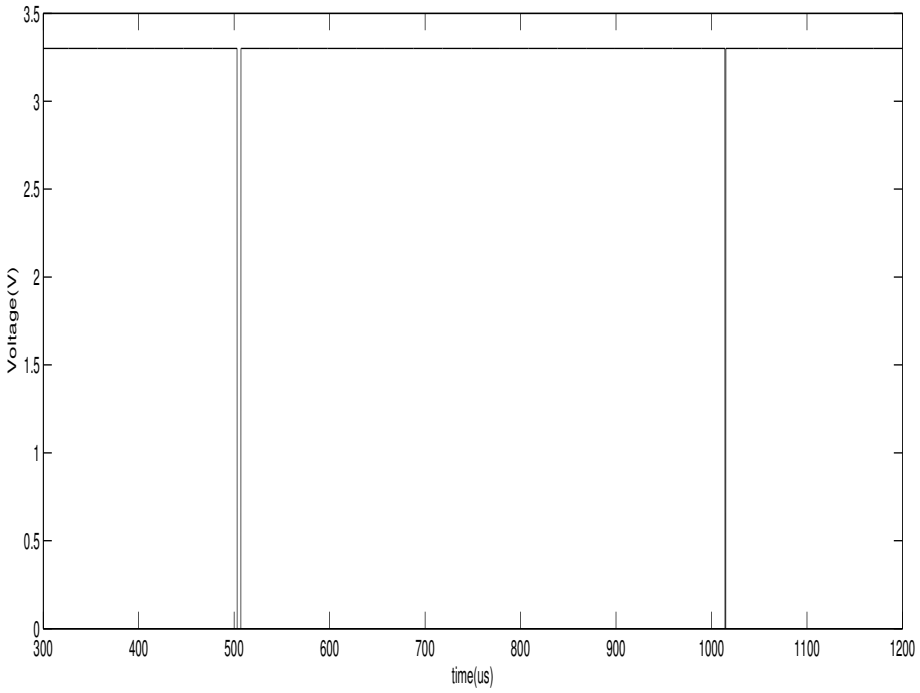


Figure 4.24: Counter Output - Q0

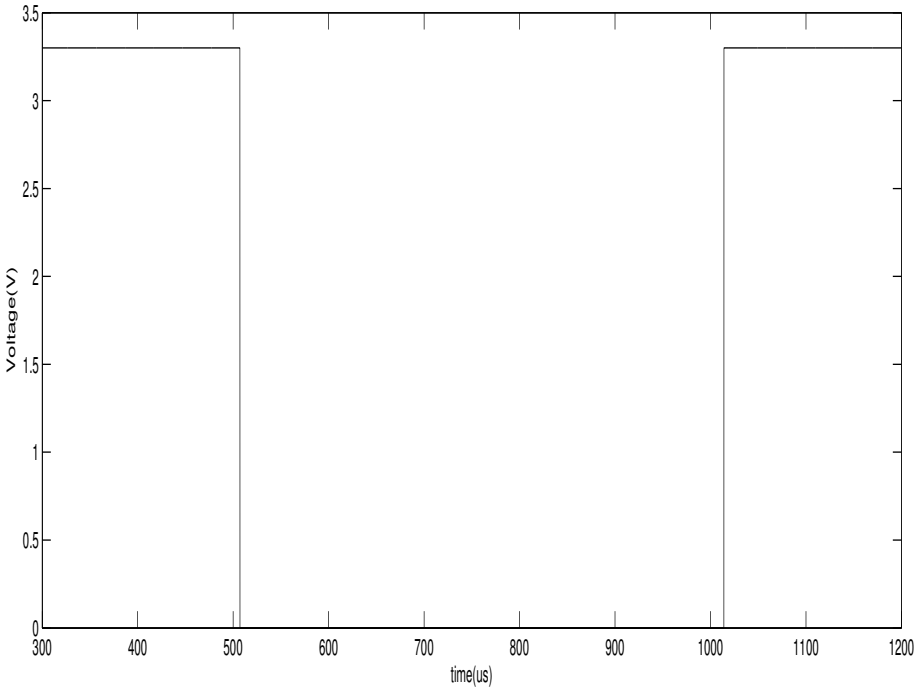


Figure 4.25: Counter Output - Q1

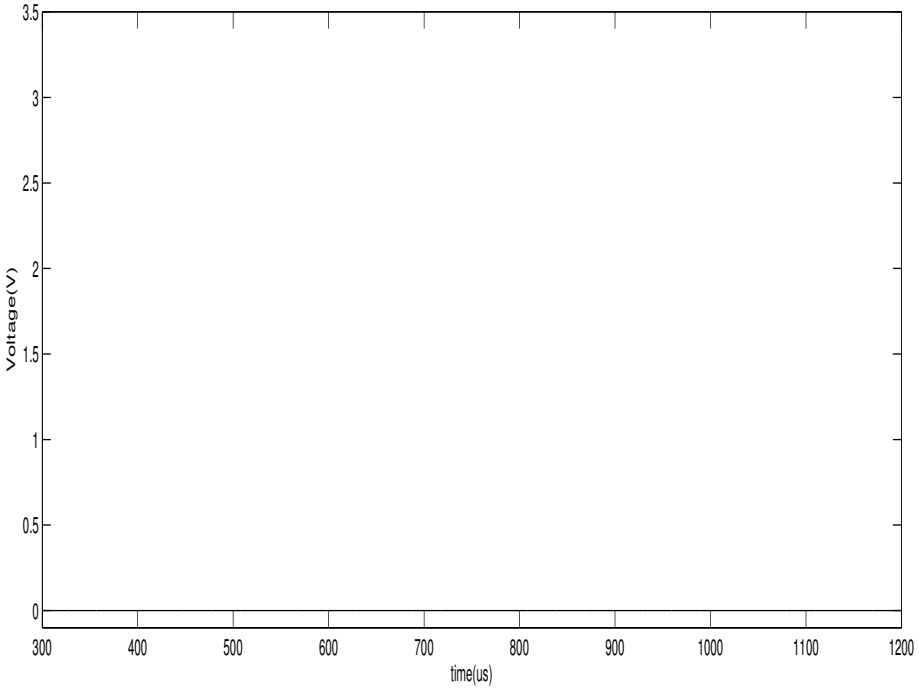


Figure 4.26: Counter Output - Q2

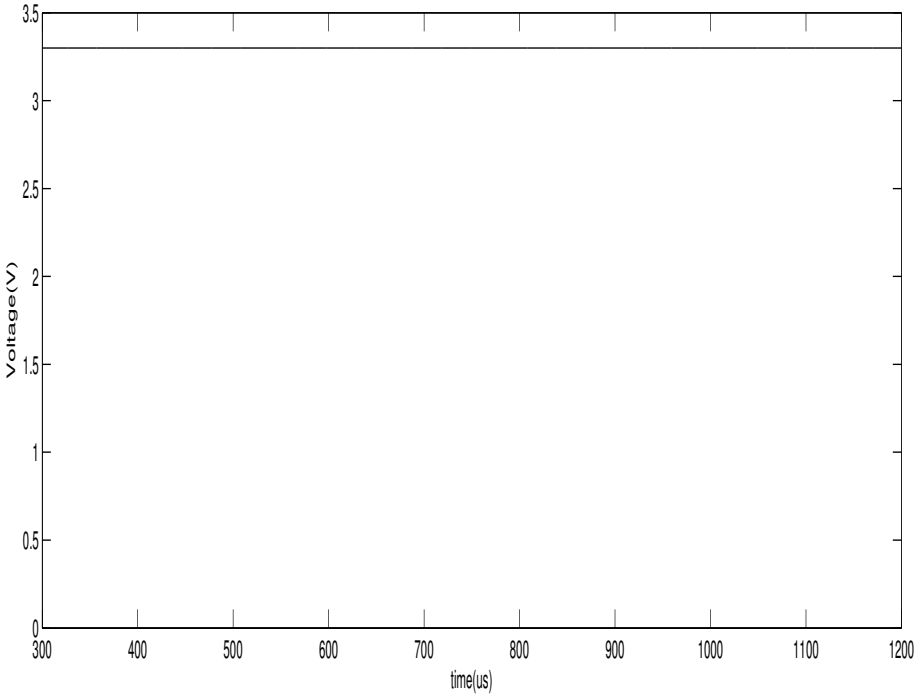


Figure 4.27: Counter Output - Q3