Energy and Reliability study of Full Adder Circuit

A Project Report

submitted by

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in partial fulfilment of requirements
for the award of the degree of

BACHELOR OF TECHNOLOGY

DEPARTMENT OF ELECTRICAL ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY MADRAS

MAY 2018

THESIS CERTIFICATE

This is to certify that the thesis titled **Energy and Reliability study of Full Adder Circuit**, submitted by **C.Sai Praneeth Reddy**, to the Indian Institute of Technology Madras, for the award of the degree of **Bachelor of Technology**, is a bona fide record of the research work done by her under our supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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Date: May 12, 2018

ABSTRACT

KEYWORDS: Full Adder, Sum, Carryout, Probability of error, Boolean Difference Calculus

The project is an analysis of gate level modelling of Full Adder circuit with errors in the gates, and with and without errors in the input signals. The results/formulae obtained can be used to study the probability of errors in the outputs of larger circuits, like Ripple Carry Adder, which uses Full Adder circuit. Also, Optimal energy/power required for the reliable working of the circuit can be determined.

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CHAPTER 1

Introduction

Understanding of errors in the circuits, analyzing them and coming up with strategies to minimize the errors is very important specially for the advancing new technologies. The goal is to come up with reliable components with unreliable/faulty/erroneous logic gates.

The aim of our project is to consider a particular (and important) component used in advance technologies and analyze the errors associated with that component and to understand the optimal energy allocation in the component. We studied the FULL ADDER circuit. We also worked towards understanding the Ripple Carry Adder.

Applications of Full Addder in larger circuits:

1. It can be used to build Ripple Carry Adder and to design Multiplication Unit.
2. Full Adder is one of the major components of Arithmetic Logic Unit (ALU).
3. To generate memory addresses inside a computer and to make the Program Counter point to next instruction, the ALU makes use of full adder.
4. For graphic related application, where there is a very much need of complex computations, the Graphic Processing Unit (GPU) uses optimized ALU which is made of full adders and other circuits.

As, Full Adder is one of the major components in many larger circuits, it is necessary to understand the errors associated with it. And, also it is necessary to study the energy distribution with in the circuit so as to minimize the overall power consumption of the device (or larger circuit).

CHAPTER 2

Model

In our project, we considered the gate level modelling of the Full Adder circuit and made our analysis.

Model in detail :

Circuit is made of 'n' gates say $gate_1, gate_2, gate_3, gate_5, ..., gate_n$, each gate has error say $\epsilon_1, \epsilon_2, \epsilon_3, \epsilon_4, ...\epsilon_n$. The errors are considered to be functions of energies associated with gates, that is, $\epsilon \propto f(E)$. The relation between gate error and the energy distributed to the gate is :

$$\epsilon \propto \frac{exp(-cE)}{2}$$

If the circuit/component has 'm' outputs, then the total probability of error of the circuit/component depends on probability of error in each of the outputs by the following relation. In turn, as the probability of error in the output depends on the energies associated with gates, total probability of error is a function of energies associated with all the gates of the circuit/component.

$$f(E_1, E_2, ..., E_n) = \lambda_1 P_e(output_1) + \lambda_2 P_e(output_2) + \lambda_3 P_e(output_3) + ... + \lambda_m P_e(output_m)$$

Then, optimal energy distribution in the circuit is obtained by optimizing the above function depending on the weights of the outputs and the energy budget given.

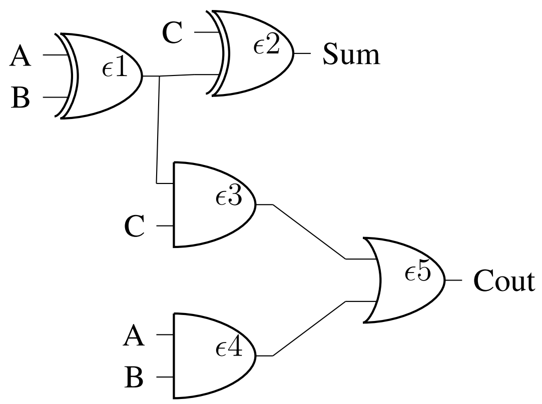


Figure 2.1: Full Adder Circuit with errors in the gates

Considering a FA circuit with errors in gates(only), ϵ_1 and ϵ_2 are the gate errors of XOR gates, ϵ_3 and ϵ_4 are the gate errors of the AND gates, ϵ_5 is the gate error of the OR gate.

The XOR gates are symmetric gates, whereas AND and OR gates are asymmetric gates. The behavior of these symmetric gates and asymmetric gates on the output error has to be analyzed separately. So in the following chapters a detailed analysis of FA has been done with each of the XOR gates having gate error ϵ_1 and each of the AND, OR gates having gate error ϵ_3.

Also, symmetric and asymmetric gates should be optimized separately for better energy-reliability trade-off, so two different energy E and E^1.

Gate error and energy relation of symmetric gates : $\epsilon_1 \propto \frac{exp(-cE)}{2}$

Gate error and energy relation of asymmetric gates : $\epsilon_3 \propto \frac{exp(-cE^1)}{2}$

The probability of error in calculating Sum (P_e(Sum)) and Carryout ($P_e(C_{out})$) are calculated using basic probability. Energy distribution in the FA circuit and Optimal Energy are measured using the following equations.

$$f(E, E^1) = P_e(Total) = \lambda * P_e(Sum) + P_e(C_{out})$$

$$f(E, E^1) = P_e(Total) = P_e(Sum) + \lambda * P_e(C_{out})$$

Further, Full Adder with errors in the input signals is also analyzed using Boolean Difference Gate Error Model. Detailed analysis has been mentioned in the next chapters.

CHAPTER 3

FULL ADDER Analysis

3.1 Calculating P_e in the outputs of FA

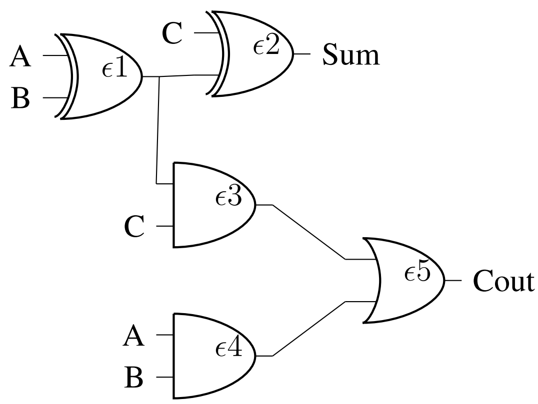


Figure 3.1: Full Adder Circuit with errors in the gates

Considering a Full Adder with five 2-input gates with $\epsilon_1, \epsilon_2, \epsilon_3, \epsilon_4$ and ϵ_5 being the errors in each of the gates. The XOR gates contribute for the error in calculating Sum. While XOR, AND and OR gates contribute for the error in calculating Carryout.

Probability of error in calculating Sum : P_e(S) = ϵ_1(1-ϵ_2)+ϵ_2(1-ϵ_1)

Probability of error in calculating C_{out} :

case 1 : When inputs are 000/010/100/110

$P_e(C_{out})$ = (1-ϵ_3)(1-ϵ_4)ϵ_5 + (ϵ_3+ϵ_4-$\epsilon_3\epsilon_4$)(1-ϵ_5)

case 2 : When inputs are 011/101

$P_e(C_{out})$ =[(1-ϵ_1)(1-ϵ_3)+$\epsilon_1\epsilon_3$]ϵ_5 + [(1-ϵ_1)ϵ_3+(1-ϵ_3)ϵ_1][$\epsilon_4\epsilon_5$+(1-ϵ_4)(1-ϵ_5)]

case 3 : When inputs are 111/001

$P_e(C_{out})$ = [ϵ_1(1-ϵ_3)+(1-ϵ_1)ϵ_3](1-ϵ_5) + [$\epsilon_1\epsilon_3$+(1-ϵ_1)(1-ϵ_3)][ϵ_4(1-ϵ_5)+(1-ϵ_4)ϵ_5]

In total,

$$P_e(C_{out}) = \frac{1}{8} * [4 * P_e(C_{out})|_{case1} + 2 * P_e(C_{out})|_{case2} + 2 * P_e(C_{out})|_{case3}]$$

$$P_e(C_{out}) = \frac{\epsilon_1}{2} + \epsilon_3 + \frac{3\epsilon_4}{4} + \epsilon_5 - \epsilon_1\epsilon_5 - 2\epsilon_3\epsilon_5 - \epsilon_1\epsilon_3 - \epsilon_3\epsilon_4 - \frac{\epsilon_1\epsilon_4}{2} + \frac{3\epsilon_4\epsilon_5}{2} + \epsilon_1\epsilon_3\epsilon_4 + 2\epsilon_1\epsilon_3\epsilon_5$$
$$+\epsilon_1\epsilon_4\epsilon_5 + 2\epsilon_3\epsilon_4\epsilon_5 - 2\epsilon_1\epsilon_3\epsilon_4\epsilon_5$$

Case I (ϵ_1, ϵ_2 = ϵ_1; ϵ_3, ϵ_4 = ϵ_3; ϵ_5 = ϵ_5)

$$P_e(C_{out}) = \frac{\epsilon_1}{2} + \frac{7\epsilon_3}{4} + \epsilon_5 - \epsilon_3^2 - \frac{7\epsilon_3\epsilon_5}{2} - \frac{3\epsilon_1\epsilon_3}{2} - \epsilon_1\epsilon_5 + \epsilon_1\epsilon_3^2 + 2\epsilon_3^2\epsilon_5 + 3\epsilon_1\epsilon_3\epsilon_5 - 2\epsilon_1\epsilon_3^2\epsilon_5$$

Case II (ϵ_1, ϵ_2, ϵ_3, ϵ_4, ϵ_5 = ϵ)

$$P_e(C_{out}) = \frac{13\epsilon}{4} - 7\epsilon^2 + 6\epsilon^3 - 2\epsilon^4, \text{and } P_e(Sum) = 2\epsilon(1-\epsilon)$$

Case III (ϵ_1, ϵ_2 = ϵ_1; ϵ_3, ϵ_4, ϵ_5 = ϵ_3)

$$P_e(C_{out}) = \frac{\epsilon_1}{2} + \frac{11\epsilon_3}{4} - \frac{9\epsilon_3^2}{2} - \frac{5\epsilon_1\epsilon_3}{2} + 4\epsilon_1\epsilon_3^2 + 2\epsilon_3^3 - 2\epsilon_1\epsilon_3^3$$

$P_e(S)$ increases with increase in gate error of the XOR gates. For a gate to be reliable the error, $\epsilon < 0.5$ so the maximum $P_e(S)$ is 0.5 . Similar increasing trend can be seen in the $P_e(C_{out})$, maximum $P_e(C_{out})$ is more than 0.5 so the gate energy has to be optimized to optimize the gate errors and thus optimizing the $P_e(C_{out})$. Refer to Figure 3.2 and Figure 3.3 for better understanding.

3.2 Plots of Probability of Error

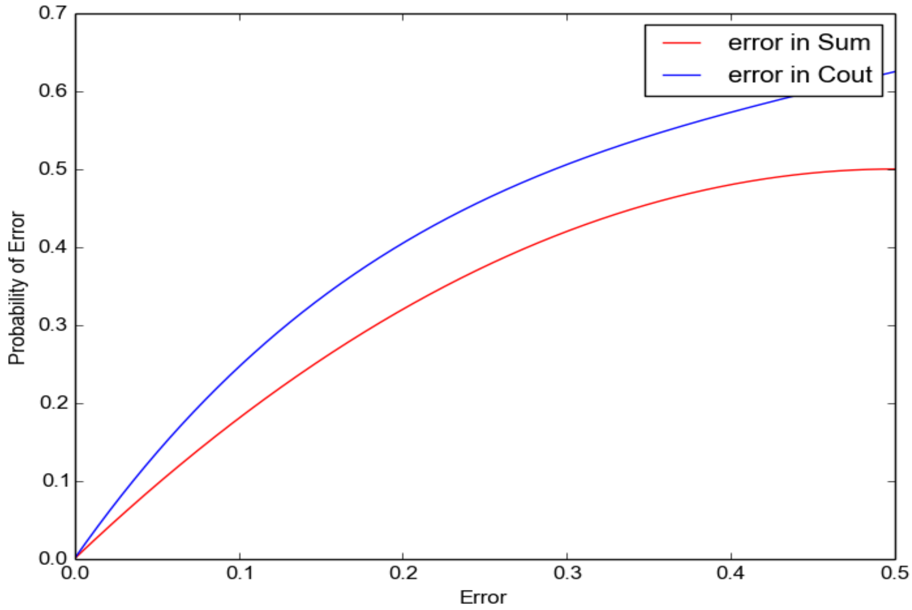
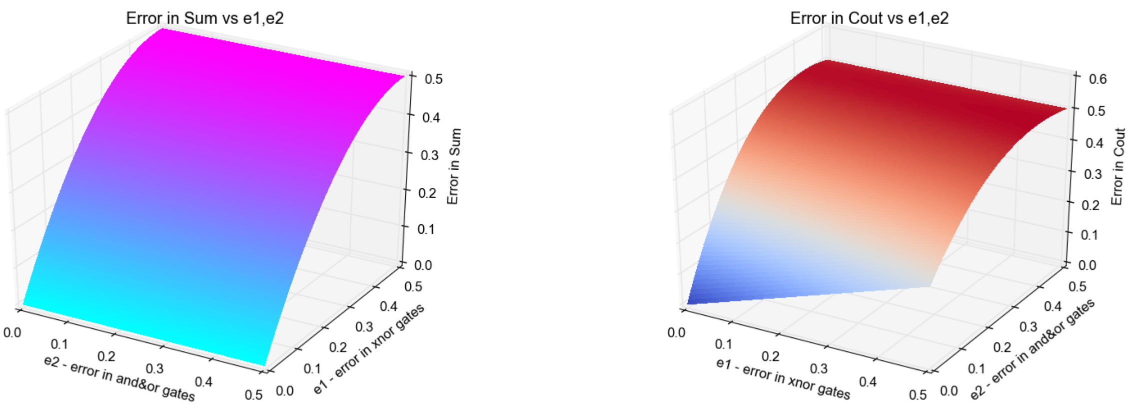


Figure 3.2: 2D plot of P_e Vs ϵ for caseII

The probability of error in calculating C_{out} is higher than the probability of error in calculating Sum.



(a) $P_e(Sum)$ Vs ϵ_1, ϵ_2

(b) $P_e(C_{out})$ Vs ϵ_1, ϵ_2

Figure 3.3: 3D plots of Probability of Error in calculating Sum and carryout Vs error in each of the gates. $P_e(Sum)$ depends only on the error in XOR gates, while $P_e(C_{out})$ depends on errors in XOR, OR and AND gates.

CHAPTER 4

Energy analysis of Full Adder and Results

4.1 Probability of error as a function of Energy:

In Case III (ϵ_1, ϵ_2 = ϵ_1; ϵ_3, ϵ_4, ϵ_5 = ϵ_3)

ϵ_1 = $\epsilon_2 \rightarrow E$, ϵ_3 = ϵ_4 = $\epsilon_5 \rightarrow E^1$

$E \rightarrow$ energy distribution on each of the XOR gates

$E^1 \rightarrow$ energy distribution on each of the AND/OR gates

Total Energy = E_0, and $2E + 3E^1 = E_0$

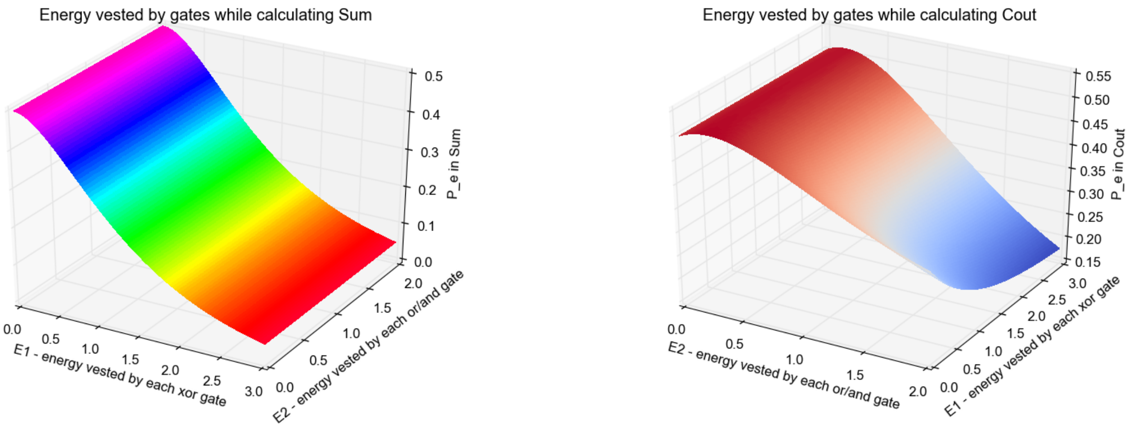
Considering error, $\epsilon \propto \frac{exp(-cE)}{2}$

$$P_e(Sum) = exp(-cE) - \frac{exp(-2cE)}{2}$$

$$P_e(C_{out}) = \frac{exp(-cE)}{4} + \frac{11exp(-cE^1)}{8} - \frac{5exp(-c(E+E^1))}{8} - exp(-2cE^1) + \frac{exp(-c(E+2E^1))}{2} + \frac{exp(-3cE^1)}{4} - \frac{exp(-c(E+3E^1))}{8}$$

4.2 3D plots of P_e as function of E, E^1

The probability of error in calculating Sum depends only on the energy distributed on the XOR gates, and it decreases as the energy on XOR gates increases. The probability of error in calculating Carryout depends on the energy distributed on XOR, AND and OR gates, it exponentially decreases as the energy on the gates increases. Finally, the total probability of error of the Full adder decreases as the energy on the gates increases. Thus, minimum total energy and the energy distribution on gates for that minimum energy can be obtained. This analysis helps in optimizing the energy of the circuit with higher reliability. Refer Figure 4.1 and Figure 4.2 .



(a) 3D plot of P_e while calculating sum (b) 3D plot of P_e while calculating Cout

Figure 4.1: 3D plots for Probability of Error as function of Energy to calculate Sum and Cout Vs Energy vested on each of the gates (E0 = 6 units)

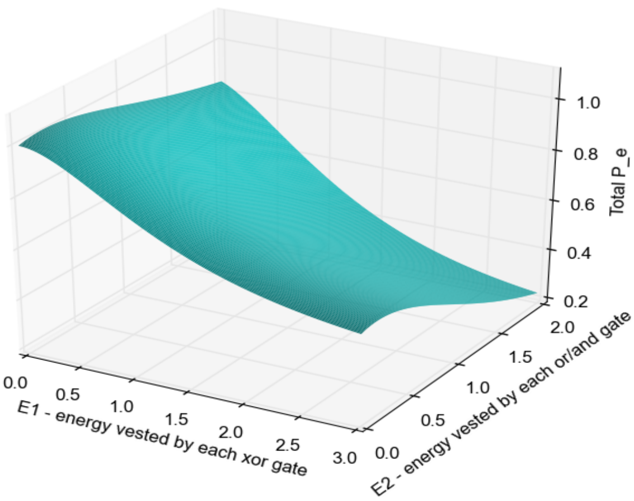
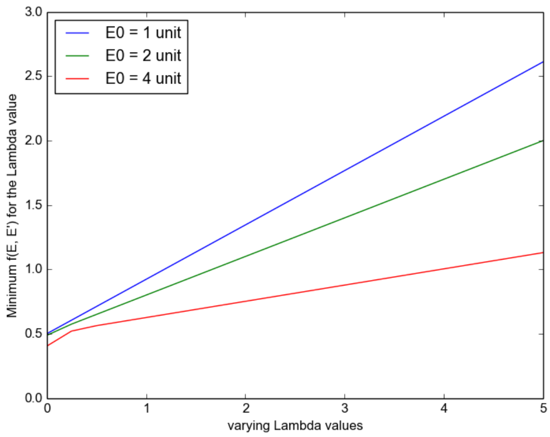


Figure 4.2: 3D plot for Total Probability of Error as function of Energy

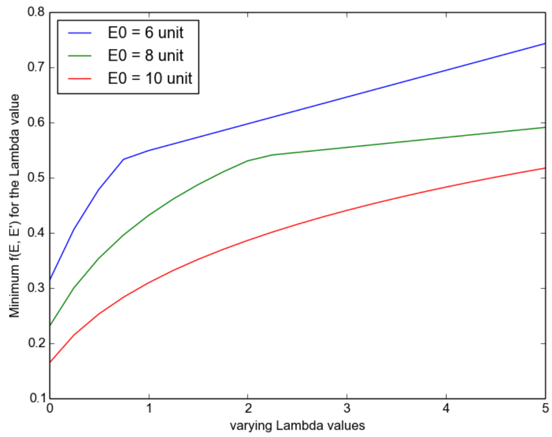
4.3 Analyzing $f(E, E^1) = \lambda * P_e(Sum) + P_e(C_{out})$

For different values of $E0$, the variation of minimum energy (or) optimal energy consumed by the full adder and lambda is plotted below. The idea behind doing this is to find out the energy distribution on each of the XOR/OR/AND gates for given Energy budget.

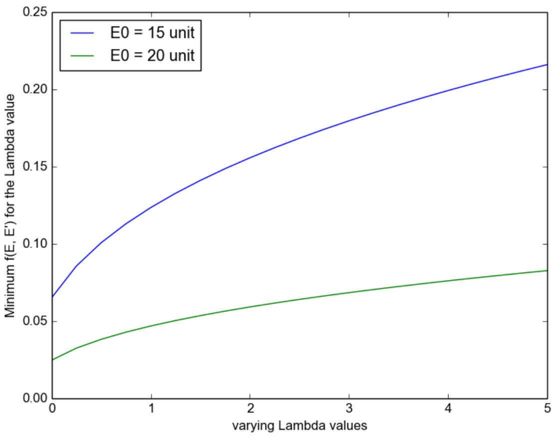
4.3.1 Error, $\epsilon \propto \frac{exp(-E)}{2}$



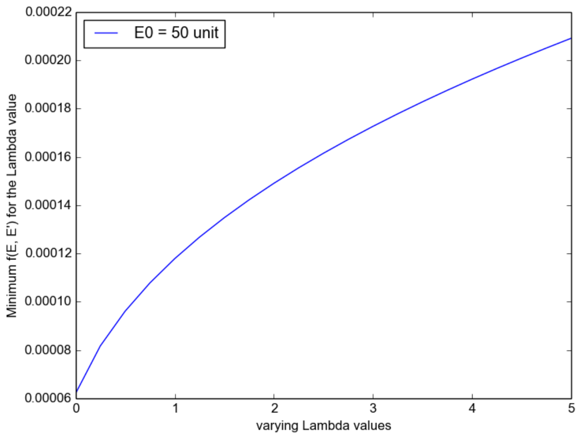
(a) Minimum f(E,E') Vs lambda



(b) Minimum f(E,E') Vs lambda



(c) Minimum f(E,E') Vs lambda



(d) Minimum f(E,E') Vs lambda

Figure 4.3: Minimum f(E,E') Vs lambda for varying values of E_0

Inferences from the above plots(Figure 4.3):

The optimal/minimum value of f(E, E^1) is calculated for varying E_0 (total energy/given energy budget) and λ values, the obtained minimum f(E, E^1) are plotted against λ.

At small budget (low E_0 values), the plot is almost linear.

At moderate budget, the curve is concave for lower λ values and then it becomes linear.

At high budget, the curve is concave (smoothly increasing) with increasing λ values.

Similar inferences can be made when the error , $\epsilon \propto \frac{exp(-\sqrt{E})}{2}$ and $\epsilon \propto \frac{exp(-E^2)}{2}$

From Table.4.1, we can understand the optimal energy distribution for a given budget of energy. In our case, depending on the weights of $P_e(S)$ and $P_e(C_{out})$ the optimal energy distribution for the reliable working of the circuit is determined.

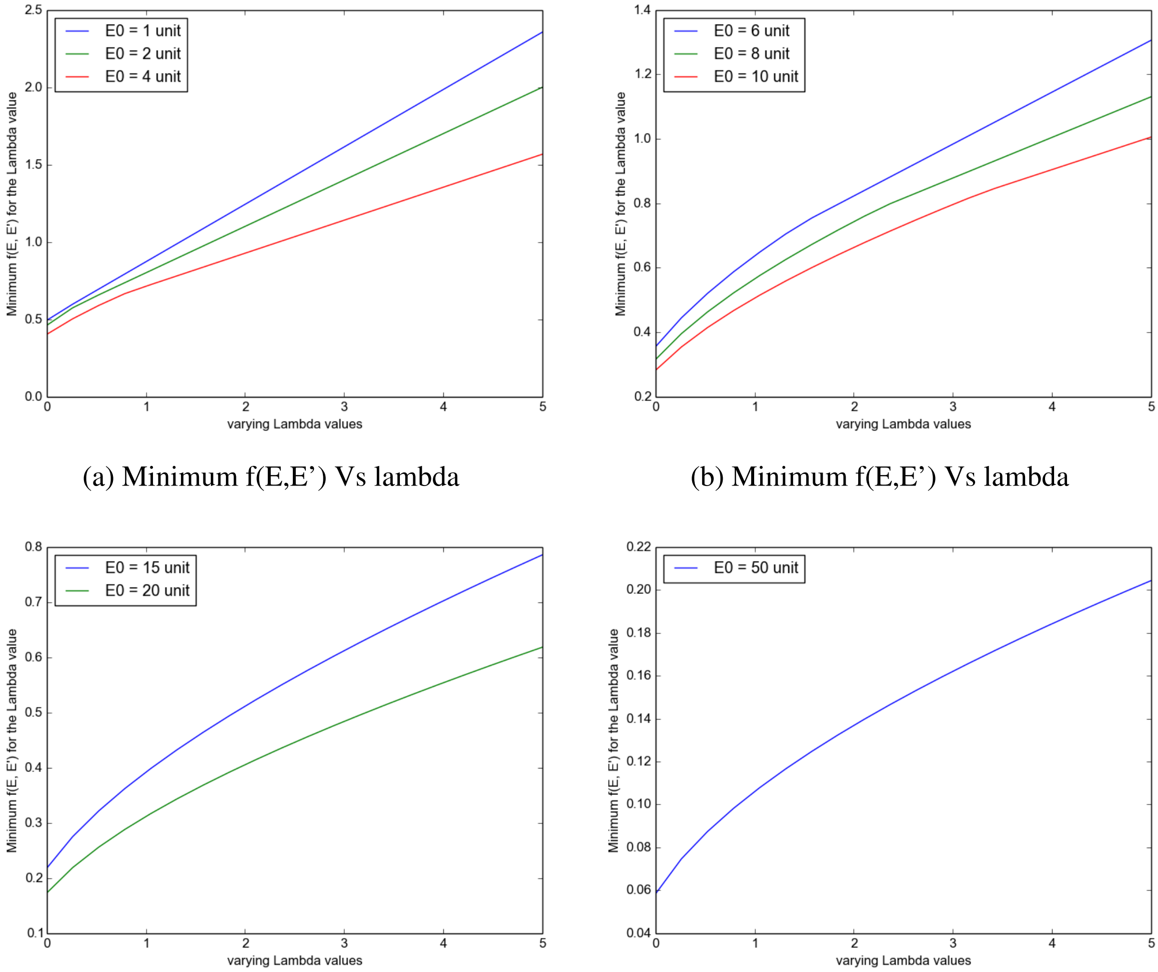
Table 4.1: Minimum E and E' for varying λ and E_0 values

	E0 values							
λ values	1	2	4	6	8	10	15	20
0.00	0.5	0.0	0.1562	0.5075	0.8809	1.2613	2.2372	3.2232
	0.0	0.6667	1.2292	1.6617	2.0794	2.4925	3.5085	4.5178
0.25	0.5	1.0	0.4625	0.8709	1.2613	1.6567	2.6426	3.6436
	0.0	0.0	1.0250	1.4194	1.8258	2.2289	3.2382	4.2375
0.50	0.5	1.0	2.0	1.2282	1.5576	1.9269	2.8979	3.8839
	0.0	0.0	0.0	1.1812	1.6283	2.0487	3.0681	4.0744
0.75	0.5	1.0	2.0	1.5405	1.7858	2.1321	3.0781	4.0641
	0.0	0.0	0.0	0.9729	1.4761	1.9119	2.9479	3.9573
1.0	0.5	1.0	2.0	3.0	1.9739	2.2923	3.2207	4.1942
	0.0	0.0	0.0	0.0	1.3507	1.8051	2.8529	3.8705
1.25	0.5	1.0	2.0	3.0	2.1341	2.4274	3.334	4.3043
	0.0	0.0	0.0	0.0	1.2439	1.7150	2.7773	3.7971
1.50	0.5	1.0	2.0	3.0	2.2783	2.5425	3.4309	4.4044
	0.0	0.0	0.0	0.0	1.1478	1.6383	2.7127	3.7304
1.75	0.5	1.0	2.0	3.0	2.4064	2.6426	3.5210	4.4845
	0.0	0.0	0.0	0.0	1.0624	1.5716	2.6026	3.6770
2.00	0.5	1.0	2.0	3.0	2.5305	2.7327	3.5961	4.5546
	0.0	0.0	0.0	0.0	0.9796	1.5115	2.6026	3.6303
2.25	0.5	1.0	2.0	3.0	4.0	2.8128	3.6637	4.6246
	0.0	0.0	0.0	0.0	0.0	1.4581	2.5576	3.5836
2.50	0.5	1.0	2.0	3.0	4.0	2.8879	3.7237	4.6847
	0.0	0.0	0.0	0.0	0.0	1.4081	2.5175	3.5435
2.75	0.5	1.0	2.0	3.0	4.0	2.9579	3.7838	4.3747
	0.0	0.0	0.0	0.0	0.0	1.3614	2.4775	3.5102
3.00	0.5	1.0	2.0	3.0	4.0	3.0230	3.8363	4.7848
	0.0	0.0	0.0	0.0	0.0	1.3179	2.4424	3.4768
3.25	0.5	1.0	2.0	3.0	4.0	3.0881	3.8814	4.8348
	0.0	0.0	0.0	0.0	0.0	1.2746	2.4142	3.4434
3.50	0.5	1.0	2.0	3.0	4.0	3.1431	3.9264	4.8748
	0.0	0.0	0.0	0.0	0.0	1.2379	2.3824	3.4167
3.75	0.5	1.0	2.0	3.0	4.0	3.1982	3.9715	4.9149
	0.0	0.0	0.0	0.0	0.0	1.2012	2.3523	3.3900
4.00	0.5	1.0	2.0	3.0	4.0	3.2532	4.0090	4.9449
	0.0	0.0	0.0	0.0	0.0	1.1645	2.3273	3.3700
4.25	0.5	1.0	2.0	3.0	4.0	3.3033	4.0465	4.9849
	0.0	0.0	0.0	0.0	0.0	1.1311	2.3023	3.3433
4.50	0.5	1.0	2.0	3.0	4.0	3.3534	4.0766	5.0150
	0.0	0.0	0.0	0.0	0.0	1.0978	2.2823	3.3233
4.75	0.5	1.0	2.0	3.0	4.0	3.4034	4.1141	5.0550
	0.0	0.0	0.0	0.0	0.0	1.0644	2.2573	3.2966
5.00	0.5	1.0	2.0	3.0	4.0	3.4485	4.1441	5.0850
	0.0	0.0	0.0	0.0	0.0	1.0344	2.2372	3.2766

And, for a given energy budget, the minimum energy to be vested in XOR gates(E) and the minimum energy to be vested in AND, OR gates (E') is determined.

Also, it can be observed that for lower energy budget, the energy is distributed over XOR gates and as the energy budget increases the energy is distributed over AND and OR gates as well. Depending on the λ value, the energy distribution changes. As the weight(λ) on $P_e(S)$ is increased, for a given energy budget, the energy distribution on the XOR gates increases and that on the AND and OR gates decreases.

4.3.2 Error, $\epsilon \propto \frac{exp(-\sqrt{E})}{2}$



(a) Minimum f(E,E') Vs lambda

(b) Minimum f(E,E') Vs lambda

(c) Minimum f(E,E') Vs lambda

(d) Minimum f(E,E') Vs lambda

Figure 4.4: Minimum f(E,E') Vs lambda for varying values of E_0

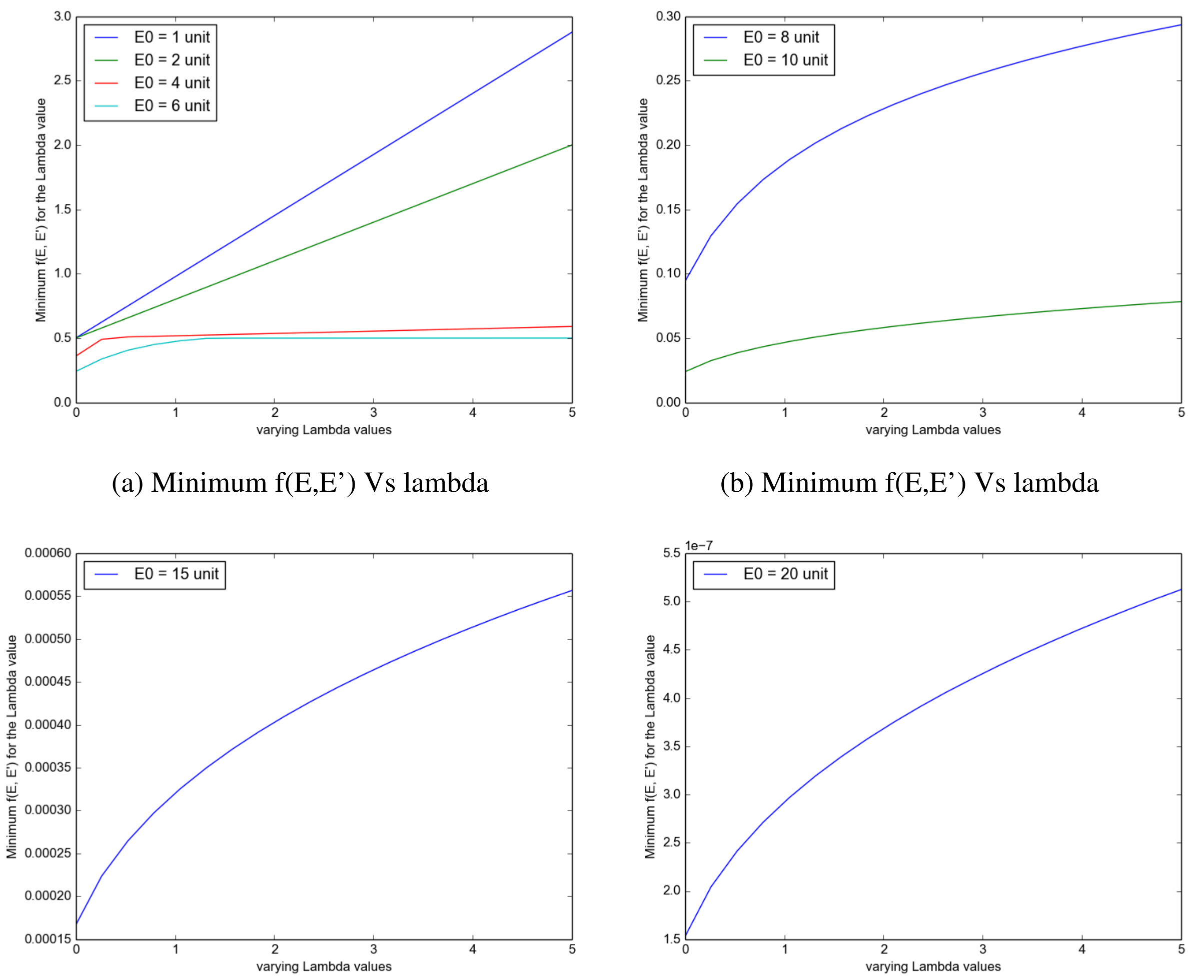
Inferences from the above plots(Figure 4.4):

The optimal/minimum value of f(E, E^1) is calculated for varying E_0 (total energy/given energy budget) and λ values, the obtained minimum f(E, E^1) are plotted against λ.

At very small budget (low E_0 values), the plot is almost linear.

As the energy budget increases, the curve becomes more concave(smoothly increasing).

4.3.3 Error, $\epsilon \propto \frac{exp(-E^2)}{2}$



(a) Minimum f(E,E') Vs lambda

(b) Minimum f(E,E') Vs lambda

(c) Minimum f(E,E') Vs lambda

(d) Minimum f(E,E') Vs lambda

Figure 4.5: Minimum f(E,E') Vs lambda for varying values of E_0

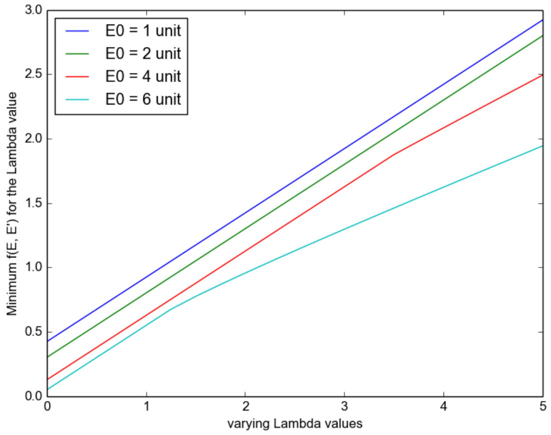
Inferences from the above plots(Figure 4.5):

The optimal/minimum value of f(E, E^1) is calculated for varying E_0 (total energy/given energy budget) and λ values, the obtained minimum f(E, E^1) are plotted against λ.

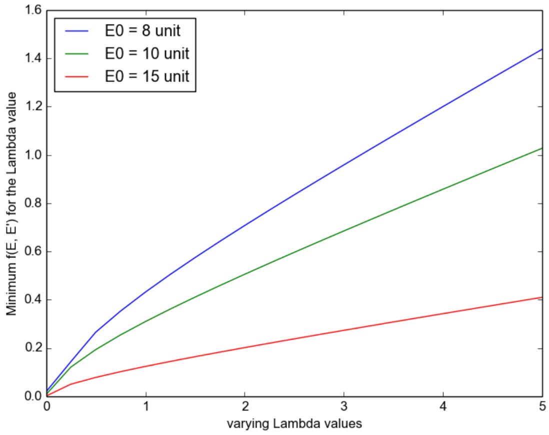
At very small budget ($E_0 < 4$ units), the plot is almost linear. At small budget ($E_0 \approx 4$ units), the curve is linearly increasing for $\lambda < 0.5$ then curve is linearly decreasing.

As the energy budget increases, the curve becomes more concave(smoothly increasing).

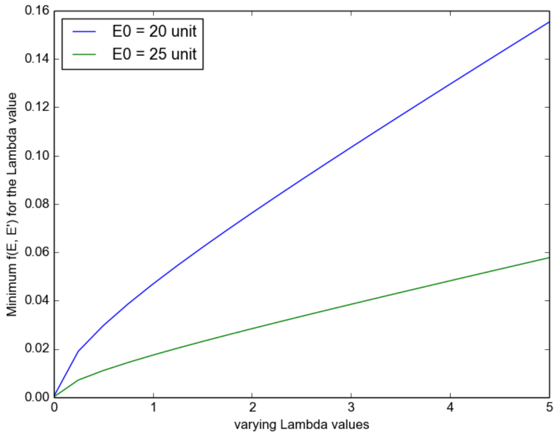
4.4 Analyzing $f(E, E^1) = P_e(Sum) + \lambda * P_e(C_{out})$ with $\epsilon \propto \frac{exp(-E)}{2}$



(a) Minimum f(E,E') Vs lambda



(b) Minimum f(E,E') Vs lambda



(c) Minimum f(E,E') Vs lambda

Figure 4.6: Minimum f(E,E') Vs lambda for varying values of E_0

Inferences from the above plots(Figure 4.6):

The optimal/minimum value of f(E, E^1) is calculated for varying E_0 (total energy/given energy budget) and λ values, the obtained minimum f(E, E^1) are plotted against λ.

At small budget (low E_0 values), the plot is almost linear.

As the energy budget increases, the curve becomes more concave(smoothly increasing).

From Table.4.1, we can understand the optimal energy distribution for a given budget of energy. In our case, for a given energy budget (E_0), the minimum energy on XOR gates(E) and the minimum energy on AND, OR gates (E') is determined.

Also, it can be observed that for lower energy budget, the energy is distributed over XOR gates and as the energy budget increases the energy is distributed over AND and OR gates as well. As the weight(λ) on $P_e(C_{out})$ is increased, for a given energy budget, the energy distribution on the AND and OR gates increases and that on the XOR gates decreases.

Table 4.2: For varying λ and E_0 values, minimum E and E' values

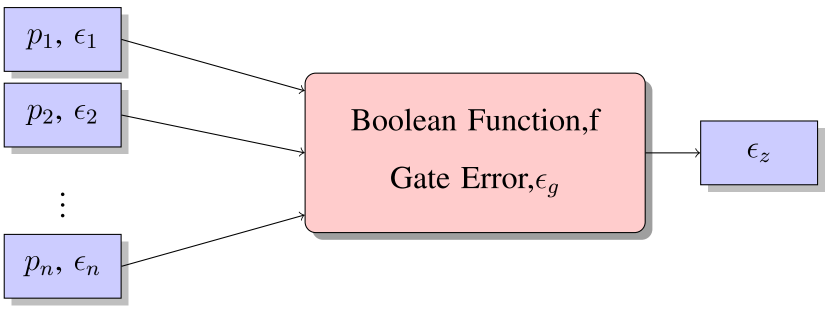
E0 values							
λ values	1	2	4	6	8	10	15
0.00	0.5 0.0	1.0 0.0	2.0 0.0	3.0 0.0	4.0 0.0	5.0 0.0	7.5 0.0
0.50	0.5 0.0	1.0 0.0	2.0 0.0	3.0 0.0	2.5305 0.9796	2.7327 1.5115	3.5961 2.6026
1.0	0.5 0.0	1.0 0.0	2.0 0.0	3.0 0.0	1.9739 1.3507	2.2923 1.8051	3.2207 2.8529
1.50	0.5 0.0	1.0 0.0	2.0 0.0	1.4414 1.0390	1.7177 1.5215	2.0670 1.9550	3.0180 2.9879
2.00	0.5 0.0	1.0 0.0	2.0 0.0	1.2282 1.1812	1.5576 1.6283	1.9269 2.0487	2.8979 3.0680
2.50	0.5 0.0	1.0 0.0	2.0 0.0	1.0900 1.2733	1.4494 1.7004	1.8268 2.1154	2.8078 3.1281
3.00	0.5 0.0	1.0 0.0	2.0 0.0	0.9969 1.3353	1.3694 1.7538	1.7568 2.1622	2.7402 3.1732
3.50	0.5 0.0	1.0 0.0	2.0 0.0	0.9249 1.3834	1.3093 1.7938	1.7017 2.1989	2.6877 3.2082
4.00	0.5 0.0	1.0 0.0	0.4625 1.0250	0.8709 1.4194	1.2613 1.8258	1.6567 2.2289	2.6426 3.2382
4.50	0.5 0.0	1.0 0.0	0.4044 1.0637	0.8288 1.4474	1.2252 1.8498	1.6106 2.2556	2.6051 3.2633
5.00	0.5 0.0	1.0 0.0	0.3644 1.0904	0.7958 1.4695	1.1932 1.8712	1.5866 2.2756	2.5826 3.2783

CHAPTER 5

Analysing Circuits with Input Errors

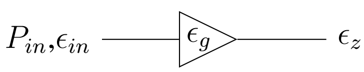
5.1 Boolean Difference Gate Error Model

In studying larger circuits (say Ripple Carry Adder), the error is propagated from one full adder to the other full adder, especially the error in carryout is propagated. So, it is necessary to study a model for circuits with errors in the input signals.
In our project, we used the Boolean Difference Gate Error Model to study the circuits with errors in Inputs.



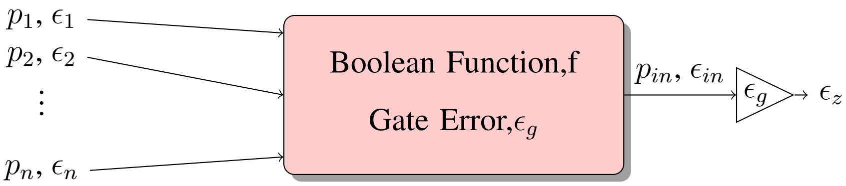
Probabilities for input signal being '1' are p_1,p_2,p_3,.....,p_n while the input error probabilities are ϵ_1,ϵ_2,ϵ_3,.....,ϵ_n. The output error probability is ϵ_z.

1 A Faulty Buffer With Erroneous Input



$\epsilon_z = \epsilon_{in}(1\text{-}\epsilon_g)+(1\text{-}\epsilon_{in})\epsilon_g \implies \epsilon_z = \epsilon_g+\epsilon_{in}(1\text{-}2\epsilon_g)$

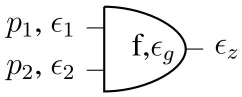
2 We can model each faulty gate with erroneous input as an ideal(no fault) gate with same functionality and the same inputs in series with a faulty buffer



$$\epsilon_z = \epsilon_g + (1-2\epsilon_g) * [\epsilon_1(1-\epsilon_2)P_r(\frac{\delta f}{\delta x_1}) + (1-\epsilon_1)\epsilon_2 P_r(\frac{\delta f}{\delta x_2}) + \epsilon_1\epsilon_2 P_r(\frac{\Delta f}{\Delta(x_1,x_2)})]$$

$$\boxed{\frac{\Delta f}{\Delta(x_i,x_j)} = \frac{\delta f}{\delta x_i} \oplus \frac{\delta f}{\delta x_j} \oplus \frac{\delta^2 f}{\delta x_i \delta x_j}, \text{where} \frac{\delta f}{\delta x_i} = f(x_i) \oplus f(\overline{x_i})}$$

5.2 2-Input AND gate



where, $f = x_1.x_2$

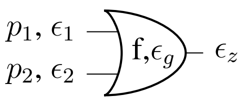
$$P_r(\frac{\delta f}{\delta x_1}) = x_2 = P_2$$

$$P_r(\frac{\delta f}{\delta x_2}) = x_1 = P_1$$

$$P_r(\frac{\Delta f}{\Delta(x_1,x_2)}) = P_r(x_1x_2 + \overline{x_1x_2}) = (1-P_1)(1-P_2) + P_1P_2 = 1-(P_1+P_2)+2P_1P_2$$

$$\epsilon_{and2} = \epsilon_g + (1-2\epsilon_g) * [\epsilon_1 P_2 + \epsilon_2 P_1 + \epsilon_1\epsilon_2(1-2(P_1+P_2)+2P_1P_2)]$$

5.3 2-Input OR gate



where, $f = x_1 + x_2$

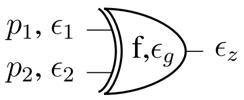
$$P_r(\frac{\delta f}{\delta x_1}) = \overline{x_2} = 1 - P_2$$

$$P_r(\frac{\delta f}{\delta x_2}) = \overline{x_1} = 1 - P_1$$

$$P_r(\frac{\Delta f}{\Delta(x_1,x_2)}) = P_r(x_1x_2 + \overline{x_1x_2}) = (1-P_1)(1-P_2) + P_1P_2 = 1-(P_1+P_2)+2P_1P_2$$

$$\epsilon_{or2} = \epsilon_g + (1-2\epsilon_g) * [\epsilon_1(1-P_2) + \epsilon_2(1-P_1) + \epsilon_1\epsilon_2(2P_1P_2-1)]$$

5.4 2-Input XOR gate



where, $f = x_1 \oplus x_2$

$$P_r(\frac{\delta f}{\delta x_1}) = x_2 \oplus \overline{x_2} = 1$$

$$P_r(\frac{\delta f}{\delta x_2}) = x_1 \oplus \overline{x_1} = 1$$

$$P_r(\frac{\Delta f}{\Delta(x_1, x_2)}) = 1 \oplus 1 \oplus \frac{\delta^2 f}{\delta(x_1, x_2)} = 1 \oplus 1 \oplus 0 = 0$$

$$\epsilon_{xor2} = \epsilon_g + (1 - 2\epsilon_g) * [\epsilon_1 + \epsilon_2 - 2\epsilon_1\epsilon_2]$$

The error probability at the output of the XOR gate is independent of the input signal probabilities.

Also, XOR gate exhibits large output error compared to OR and AND gates, since XOR gates show maximum sensitivity to input errors.

5.5 FULL ADDER with errors in Input Signals

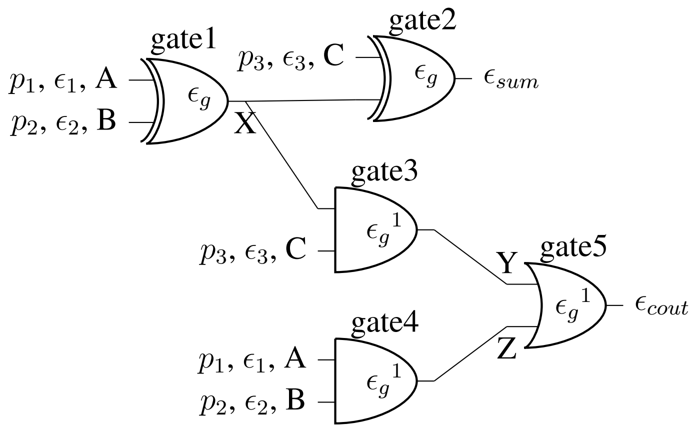
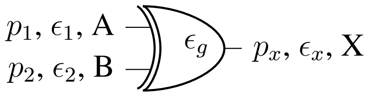


Figure 5.1: Full Adder Circuit with errors in gates and input signals

Assumptions : Both XOR gates (symmetric) have an error probability of ϵ_g. AND and OR gates (asymmetric) have the error probability of ϵ_g^1. Probabilities for input signals being '1', are P_1,P_2,P_3 while the input error probabilities are ϵ_1,ϵ_2,ϵ_3. The probability of errors in the outputs of the FA circuit are ϵ_{cout} and ϵ_{sum}.

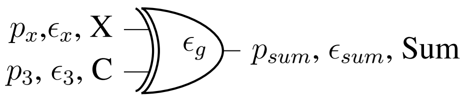
Finding errors in the output signals of FA with errors in input signals and gates

Gate 1 :



ϵ_x = ϵ_g + (1-2ϵ_g)(ϵ_1+ϵ_2-2$\epsilon_1\epsilon_2$)

Gate 2 :



ϵ_{sum} = ϵ_g + (1-2ϵ_g)(ϵ_x+ϵ_3-2ϵ_3 ϵ_x)

= ϵ_g + (1-2ϵ_g)[ϵ_g + (1-2ϵ_g)(ϵ_1+ϵ_2-2$\epsilon_1\epsilon_2$)+ϵ_3-2ϵ_3(ϵ_g + (1-2ϵ_g)(ϵ_1+ϵ_2-2$\epsilon_1\epsilon_2$))]

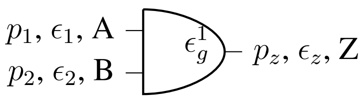
ϵ_{sum} = ϵ_g + (1-2ϵ_g)[ϵ_g+ϵ_3-2$\epsilon_g\epsilon_3$+(1-2ϵ_g)(ϵ_1+ϵ_2-2$\epsilon_1\epsilon_2$)-2ϵ_3(1-2ϵ_g)(ϵ_1+ϵ_2-2$\epsilon_1\epsilon_2$)]

= ϵ_g + (1-2ϵ_g)[ϵ_3+(ϵ_g+(1-2ϵ_g)(ϵ_1+ϵ_2-2$\epsilon_1\epsilon_2$))(1-2ϵ_3)]

$$\boxed{\epsilon_{sum} = \epsilon_g + (1-2\epsilon_g)(\epsilon_3 + \epsilon_g - 2\epsilon_3\epsilon_g) + (1-2\epsilon_g)^2(1-2\epsilon_3)(\epsilon_1 + \epsilon_2 - 2\epsilon_1\epsilon_2)}$$

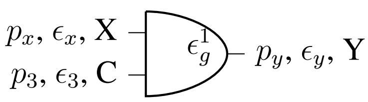
In the above equation, if there are no errors in the input signal then the we get back the old equation for error in sum ie., $\epsilon_{sum} = 2\epsilon_g(1-\epsilon_g)$.

Gate 4 :



ϵ_z = ϵ_g^1 + (1-2ϵ_g^1)($\epsilon_1 p_2$ + $\epsilon_2 p_1$ + 2$\epsilon_1\epsilon_2$[1 - 2(p_1 + p_2) + 2 $p_1 p_2$])

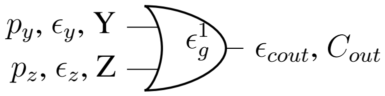
Gate 3 :



p_x = $p_1 \oplus p_2$ = $p_1 + p_2 - 2p_1p_2$

ϵ_y = ϵ_g^1 + (1-2ϵ_g^1)($\epsilon_x p_3$ + $\epsilon_3 p_x$ + 2$\epsilon_x\epsilon_3$[1 - 2(p_3 + p_x) + 2 $p_x p_3$])

Gate 5 :



$$\epsilon_{cout} = \epsilon_g^1 + (1 - 2\epsilon_g^1)[\epsilon_y(1 - p_z) + \epsilon_z(1 - p_y) + \epsilon_y\epsilon_z(2p_yp_z - 1)]$$

$$p_y = (p_1 \oplus p_2)p_3 = (p_1 + p_2 - 2p_1p_2)p_3$$

$$p_z = p_1p_2$$

$$\epsilon_z = \epsilon_g^1 + (1 - 2\epsilon_g^1)[\epsilon_1p_2 + \epsilon_2p_1 + \epsilon_1\epsilon_2(1 - 2p_1 - 2p_2 + 2p_1p_2)]$$

$$\epsilon_y = \epsilon_g^1 + (1 - 2\epsilon_g^1)[\epsilon_xp_3 + \epsilon_3p_x + \epsilon_x\epsilon_3(1 - 2p_x - 2p_3 + 2p_xp_3)]$$

$$\epsilon_x = \epsilon_g + (1 - 2\epsilon_g)(\epsilon_1 + \epsilon_2 - 2\epsilon_1\epsilon_2)$$

$$p_x = p_1 \oplus p_2 = p_1 + p_2 - 2p_1p_2$$

CHAPTER 6

Conclusion and References

CONCLUSION:

Using the FA circuit as the basic unit, and using the boolean difference gate error model, the error propagation in the larger circuits (like Ripple Carry Adder) can be determined. Depending on the errors in the output, the reliability of the circuit can be determined. Also, depending on the relation between the error and energy, the optimal energy distribution in the circuit can be determined with minimum probability of error in outputs.

REFERENCES:

1. PROBABILISTIC ERROR PROPAGATION IN A LOGIC CIRCUIT USING THE BOOLEAN DIFFERENCE CALCULUS by Nasir Mohyuddin, Ehsan Pakbaznia, Massoud Pedram