EFFICIENCY MODEL FOR DC-DC BUCK CONVERTER

A Project Report

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THESIS CERTIFICATE

This is to certify that the thesis titled **EFFICIENCY MODEL FOR DC-DC BUCK CONVERTER**, submitted by **Adepu Harshavardhan**, to the Indian Institute of Technology, Madras, for the award of the degree of **Bachelor of Technology**, is a bona fide record of the research work done by him under our supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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ABSTRACT

KEYWORDS: Voltage Regulator; Buck converter; modelling DC-DC converters
;.

Buck Converter are highly efficient with their efficiency often greater than 90%. However, the efficiency of a particular circuit depends on the choice of the components used and the frequency of operation. We propose to model the power loss in each component of Buck converter as a function of Operating Frequency. Using this model we derive an analytical expression for the Optimum frequency and the sizes of MOSFETs, that maximizes the Efficiency of the Buck converter.

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ABBREVIATIONS

PWM	Pulse Width Modulation
CCM	Continous Conduction Mode
DCM	Discontinous Conduction Mode
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
PMOS	p-channel MOSFET
NMOS	n-channel MOSFET
RMS	Root-Mean-Square

CHAPTER 1

INTRODUCTION

1.1 Voltage Regulators

With power being a key parameter in many designs, we need Voltage regulators to provide a stable output voltage irrespective of any changes in the input voltage or Load conditions. Apart from providing a steady voltage, Voltage regulators can also be used to step up or step down the input voltage. There are mainly two types of voltage regulators:

i. Linear Voltage Regulator

ii. Switching Voltage Regulator

1.1.1 Linear Voltage Regulator

Linear Voltage Regulator behaves as a voltage divider. The resistance of the voltage regulator varies in accordance with the load, resulting in a constant output voltage. Linear Voltage Regulators have low output voltage ripple and fast response to line or load changes. But, they cannot be used to step up voltage and have very low efficiency.

1.1.2 Switching Voltage Regulator

Switching Regulators rapidly switch the pass transistors between full-on and full-off states. The average value of the output voltage is controlled using Pulse Width Modulation. In switching Regulators, the pass transistors are used as "controlled Switches" and are operated in either cut off (where the current through the transistor is nearly zero) or triode (where the voltage drop across the transistor is very less) states, hence, dissipating almost no power. Even though Switching Regulators have high voltage ripple and low response time when compared to Linear Voltage regulators, they have very high Efficiency and unlike Linear Voltage regulators, they can be used to generate output voltage higher than input voltage or of opposite polarity. For this project we focus mainly on step down DC-DC Buck converter.

1.2 Buck Converter

The Buck Converter is a ubiquitous DC-DC Switching Voltage Regulator used to step down the input voltage. The simplified schematic for the power stage of Buck converter is shown in the Fig. 1.1. The course "Power Management Integrated Circuits" by Khan (2017) gives a deep insight into various concepts of Buck converter. The Buck Converter operates in two different modes. They are:

i. Discontinuous Conduction Mode (DCM)

ii. Continuous Conduction Mode (CCM)

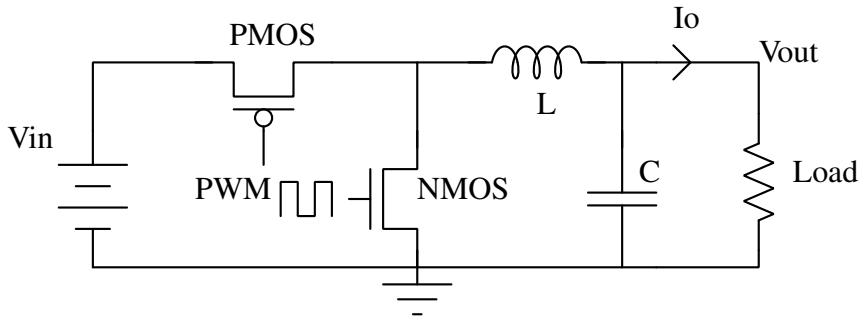

Figure 1.1: Schematic for Buck converter Power stage with Resistive Load

1.2.1 Discontinuous Conduction Mode (DCM)

In Discontinuous Conduction Mode, the current through the Inductor becomes zero for a fraction of the Switching period. This can be achieved at light load conditions, using a zero crossing detector for Inductor current and turning off the NMOS when the Inductor current becomes zero or by replacing the NMOS in Fig 1.1 with a Diode.

1.2.2 Continuous Conduction Mode (CCM)

In Continuous Conduction Mode, the Inductor conducts throughout the switching period. The operating principle for CCM is described in Fig. 1.2. In each cycle, the circuit operates in two states namely ON and OFF states.

- In On state, the PMOS is conducting and the NMOS is off. The voltage across the Inductor in this state is give by $V_L = V_{in} - V_{out}$.
- In off state, the NMOS is conducting and the PMOS is off. The voltage across the inductor in this state is given by $V_L = -V_{out}$.

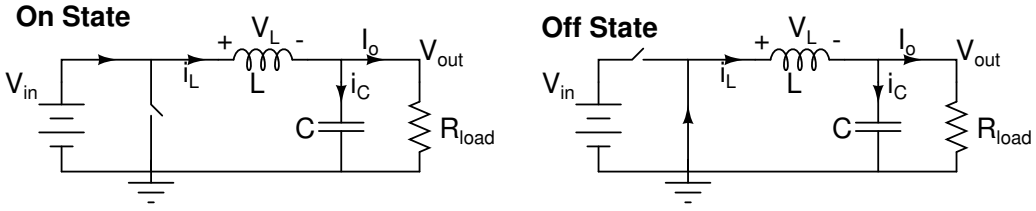

Figure 1.2: ON and OFF states of Buck converter

The current through the Inductor (I_L) is related to the voltage across it (V_L) as

$$V_L = L\frac{dI_L}{dt} \implies \int_0^{T_{sw}} di_L = \frac{1}{L}\int_0^{T_{sw}} V_L dt$$

In steady state i.e., when all the external conditions such as input voltage or Load does not change, all the quantities such as Inductor current, output voltage etc. repeat themselves in every cycle. In other words, the circuit behaves the same in each cycle. Hence, in steady state, the total change in Inductor current over one cycle is zero.

$$\int_0^{T_{sw}} di_L = 0 \implies \int_0^{T_{sw}} V_L dt = 0$$

This is called **Inductor Volt-Second balance**. Now,

$$\int_0^{T_{sw}} V_L dt = \int_0^{T_{on}} V_L dt + \int_{T_{on}}^{T_{sw}} V_L dt = (V_{in} - V_{out})T_{on} + (-V_{out})T_{off} = 0$$

$$\therefore V_{out} = \frac{T_{on}}{T_{on} + T_{off}} V_{in}$$

The **Duty cycle (**D**)** of a rectangular signal is defined as the ratio of T_{on} and Time period of the signal.

$$D = \frac{T_{on}}{T_{sw}} = \frac{T_{on}}{T_{on} + T_{off}}$$

Hence, The output and input voltages of a Buck converter are related as

$$V_{out} = \frac{T_{on}}{T_{on} + T_{off}} V_{in} = DV_{in}$$

Since $0 \leq D \leq 1$, $\qquad V_{out} \leq V_{in}$

Inductor Ripple Current: Fig. 1.3 shows the voltage and current through the Inductor

and Capacitor as a function of time.The peak to peak Inductor Ripple current(ΔI_L) is given by

$$\Delta I_L = \int_0^{T_{on}} di_L = \frac{1}{L}\int_0^{T_{on}} V_L dt = \frac{1}{L}\int_{T_{on}}^{T_{sw}} V_L dt = \frac{(V_{in} - V_{out})}{L} T_{on}$$

$$\therefore \Delta I_L = \frac{(V_{in} - V_{out})}{L} T_{on} = \frac{V_{in} D(1-D) T_{sw}}{L} = \frac{V_{in} D(1-D)}{L F_{sw}}$$

The maximum and minimum current through the Inductor are given by

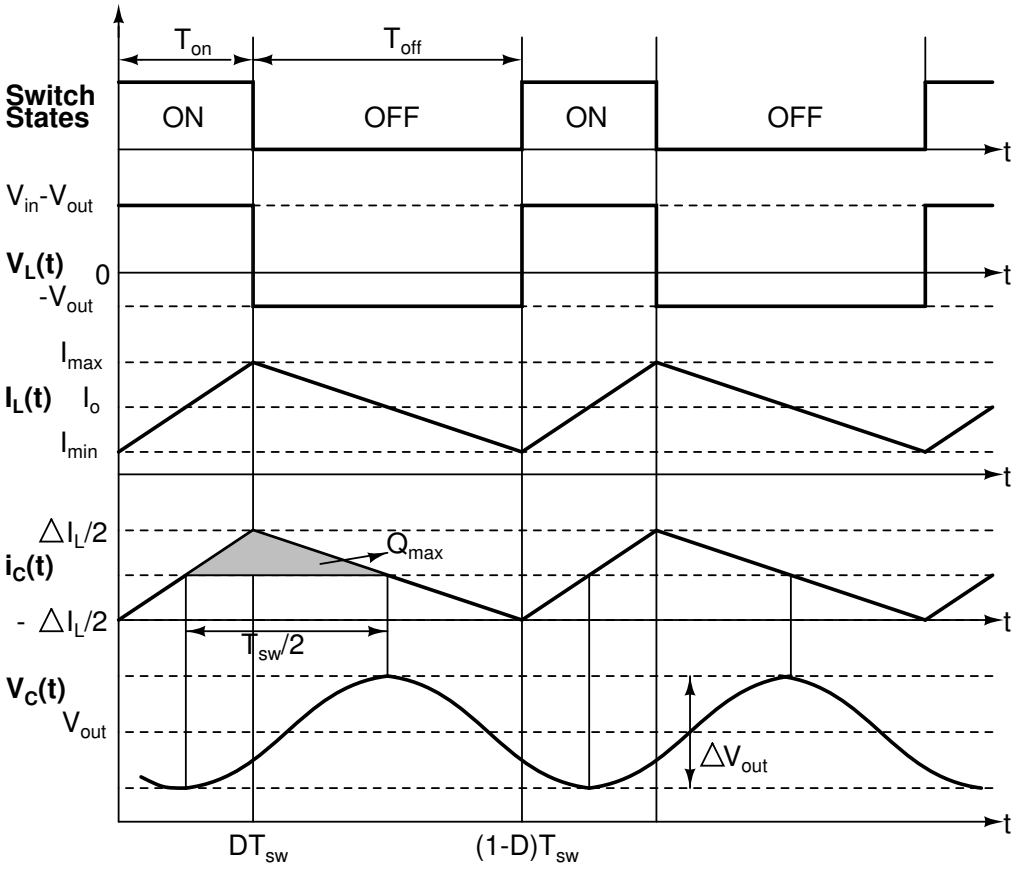

Figure 1.3: Inductor Current and Output voltage ripple in Buck Converter

$$I_L(max) = I_o + \frac{\Delta I_L}{2}$$

$$I_L(min) = I_o - \frac{\Delta I_L}{2}$$

Output Voltage Ripple: The Inductor current is divided into Load current and the current through the Capacitor(i_C). Hence, the Capacitor (C) carries the ripple current through the Inductor (L). The Voltage across the Capacitor (V_C) is related to its current

(i_C) as

$$i_C = C\frac{dV_C}{dt} \implies \int dV_C = \frac{1}{C}\int i_C dt = \frac{Q}{C}$$

where, Q is the charge stored in the Capacitor. Hence, the Output Voltage Ripple (ΔV_{out}) is given by the maximum charge stored in the Capacitor during a cycle divided by the Capacitance (C)

$$Q_{max} = \int_{\frac{T_{sw}}{2}} i_C dt = \frac{1}{2}\frac{T_{sw}}{2}\frac{\Delta I_L}{2} = \frac{\Delta I_L}{8F_{sw}} = \frac{V_{in}D(1-D)}{8F_{sw}^2 L}$$

$$\therefore \Delta V_{out} = \frac{Q_{max}}{C} = \frac{V_{in}D(1-D)}{8F_{sw}^2 LC}$$

Fig. 1.4 shows the Output Voltage ripple of the Buck converter as a function of Duty Cycle (D). We can see that the Output Voltage ripple is minimum at $D = 0$ and $D = 1$ and maximum ripple occurs at a Duty Cycle of $\frac{1}{2}$.

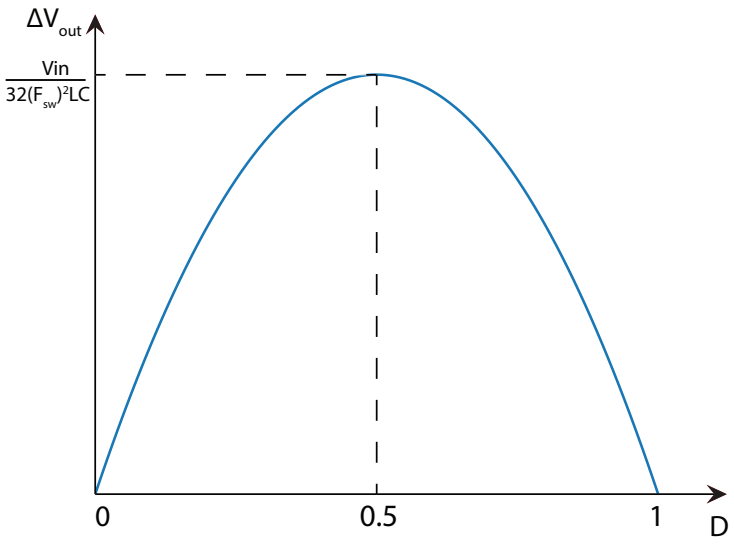

Figure 1.4: Output Voltage ripple Vs Duty Cycle (D)

CHAPTER 2

POWER LOSS IN BUCK CONVERTER

Buck Converters are highly efficient with their efficiency often higher than 90%. So far, we have seen the characteristics of an ideal Buck converter. In this chapter we will see the non-idealities associated with the Buck converter. Fig. 2.1 shows the schematic for a non-ideal Buck converter.

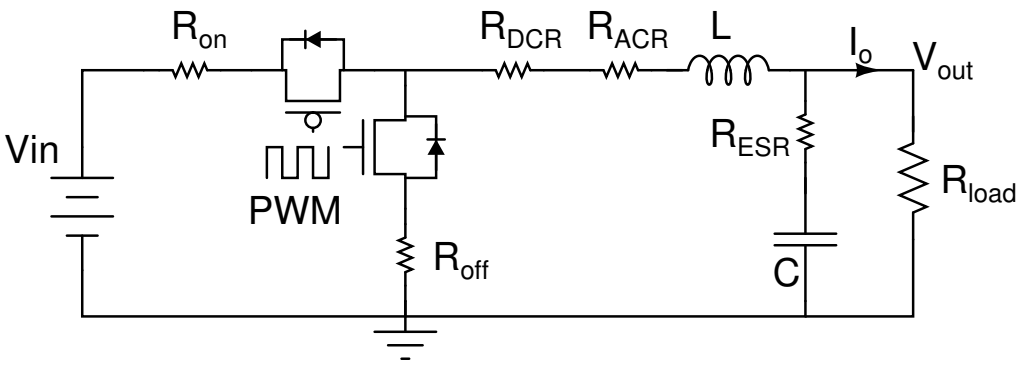

Figure 2.1: Buck Power stage schematic with lossy elements

2.1 Duty Cycle Correction

The practical switches have non-zero resistance when they are conducting. Hence, there is a voltage drop across the switches. There is also a finite voltage drop across the Inductor because of the winding Resistance. Fig. 2.2 shows the new ON and OFF states of Buck Converter. The new volt-second balance for the Inductor is given by

$$\int_0^{T_{sw}} V_L dt = (V_{in} - I_o(R_{on} + R_{DCR}) - V_{out})T_{on} - (V_{out} + I_o(R_{off} + R_{DCR}))T_{off} = 0$$

$$\therefore V_{out} = DV_{in} - I_o(DR_{on} + (1-D)R_{off} + R_{DCR}) = DV_{in} - V_{loss}$$

where $V_{loss} = I_o(DR_{on} + (1-D)R_{off} + R_{DCR})$ is the average voltage lost due to the drop across the switches and the Inductor. From the characteristics of the Ideal Buck

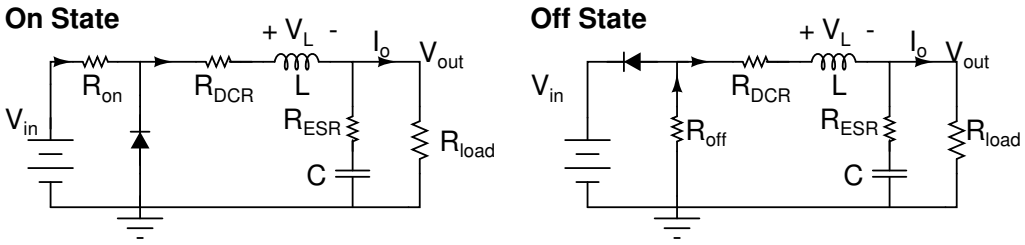

Figure 2.2: ON and OFF states of Buck Converter

converter, we have $D_{ideal} = \dfrac{V_{out}}{V_{in}}$. Let the new Duty cycle, $D = D_{ideal} + \Delta D$. The Switches and the Inductor for the Buck converter are chosen such that the drop across them is very low. Hence, we can approximate $\Delta D \approx 0$. The new Relation between V_{in} and V_{out} can be written as

$$V_{out} = (D_{ideal} + \Delta D)V_{in} - I_o(D_{ideal}R_{on} + (1 - D_{ideal})R_{off} + R_{DCR})$$

$$\therefore \Delta D = \frac{I_o(D_{ideal}R_{on} + (1 - D_{ideal})R_{off} + R_{DCR})}{V_{in}}$$

2.2 Element-wise losses in Buck Converter

In this section we look at the losses in each element of the Buck converter, namely switches, Inductor and Capacitor.

2.2.1 Power Loss in Switches

Gate Drive Losses: In each cycle, the Gate capacitance of the MOSFET switches are charged to V_{in} and back to zero. The power loss in the Gate Capacitance of the switches is given by

$$P_{GD} = C_{on}V_{in}^2F_{sw} + C_{off}V_{in}^2F_{sw} = C_{GATE}V_{in}^2F_{sw}$$

where, $C_{GATE} = C_{on} + C_{off}$ is the total Gate capacitance of the Switches. The Gate Drive losses are proportional to the frequency and are independent of the load. Hence, the Gate Drive losses dominate under low load conditions.

Conduction Losses: The switches have finite ON resistance. The average power dissipated by the switches while conducting is given by

$$P_{ON} = I_{rms}^2(DR_{on} + (1-D)R_{off})$$

where, I_{rms} is the rms current through the Inductor. $I_{rms}^2 = I_o^2 + \frac{\Delta I_L^2}{12}$. This shows that the conduction losses in the switches are directly proportional to the Load current. Hence at high Load conditions, the Conduction losses dominate.

Switching Losses: The Switching losses are the power dissipated in the Switches while switching from one state to another. The Switching losses are given by

$$P_{SWLOSS} = \frac{1}{2}\frac{(T_{ON} + T_{OFF})V_{in}I_o}{T_{sw}} = \frac{1}{2}(T_{ON} + T_{OFF})V_{in}I_oF_{sw}$$

where T_{ON} and T_{OFF} are the turn ON and turn OFF times for the switches. From the expression we can see that the switching losses are directly proportional to the Load current and the frequency of operation.

Dead Time Losses: To avoid both the switches conducting at the same time during switching, the switch that is conducting is turned off for a small fraction of the Time period before the other switch starts conducting. This duration where none of the switches are actively conducting is called **Dead Time**. Since the current through the Inductor cannot abruptly go to zero, The Body Diode of the MOSFETs conducts current during this period. The power dissipated during this period is due to the forward voltage drop accross the Body Diode. This is given by

$$P_{DEAD} = 2V_FI_o\frac{t_{DEAD}}{T_{sw}} = 2V_FI_ot_{DEAD}F_{sw}$$

where, V_F is the forward conduction voltage of the body diode of the MOSFETs. From the expression we can see that the Dead time losses are directly proportional to the Load current and the frequency of operation.

2.2.2 Power Loss in Inductor

DC Losses: The power losses in an Inductor at DC are due to the DC resistance of the Inductor windings (R_{DCR}) and the DC current through it.

$$P_{DCR} = I_o^2R_{DCR}$$

AC Losses: The Inductor AC losses are modelled as the power dissipated by a resistance R_{ACR}, in series with the the Inductor. The power dissipated in R_{ACR} is only due to the AC current through the Inductor.

$$P_{ACR} = I_{ACRMS}^2 R_{ACR} = \frac{\Delta I_L^2}{12} R_{ACR}$$

2.2.3 Power Loss in Capacitor

Practical Capacitors can be modelled as an ideal Capacitor in series with a resistor called Equivalent Series Resistance (ESR). Since, the Capacitor (C) carries only the ripple current through the Inductor, the power loss in the Capacitor is given by

$$P_{ESR} = I_{ACRMS}^2 R_{ESR} = \frac{\Delta I_L^2}{12} R_{ESR}$$

2.3 Classification of losses

Conduction loss: The Conduction loss is the power dissipated because of the finite resistance of the elements in the Buck converter circuit. Conduction Losses are directly proportional to the square of the Load current. The losses that contribute to Conduction losses are P_{ON} and P_{DCR}

$$P_{COND} = P_{ON} + P_{DCR} = I_{rms}^2(DR_{on} + (1-D)R_{off}) + I_o^2 R_{DCR}$$

Gate Drive loss: Gate Drive losses are the power loss because of charging the Gate Capacitance of the switches. Gate Drive losses are independent of the Load.

$$P_{GD} = C_{GATE} V_{in}^2 F_{sw}$$

Switching losses: These are the power dissipated while switching the from one state to other. The losses that contribute to the switching losses are P_{SWLOSS} and P_{DEAD}

$$P_{SW} = P_{SWLOSS} + P_{DEAD} = \frac{1}{2}(T_{ON} + T_{OFF}) V_{in} I_o F_{sw} + 2 V_F I_o t_{DEAD} F_{sw}$$

Other losses: Other losses include the Eddy current losses, residual losses etc., which are modeled using the AC resistance of the Inductor and the R_{ESR} of the capacitor.

$$P_{other} = P_{ACR} + P_{ESR} = \frac{\Delta I_L^2}{12}(R_{ESR} + R_{ACR})$$

Total Power Loss: The total power loss in the Buck converter is the sum of all the losses mentioned above. Fig. 2.3 shows the contribution of various losses to the total power loss as Load current is varied.

$$P_{TOTAL} = P_{COND} + P_{GD} + P_{SW} + P_{other}$$

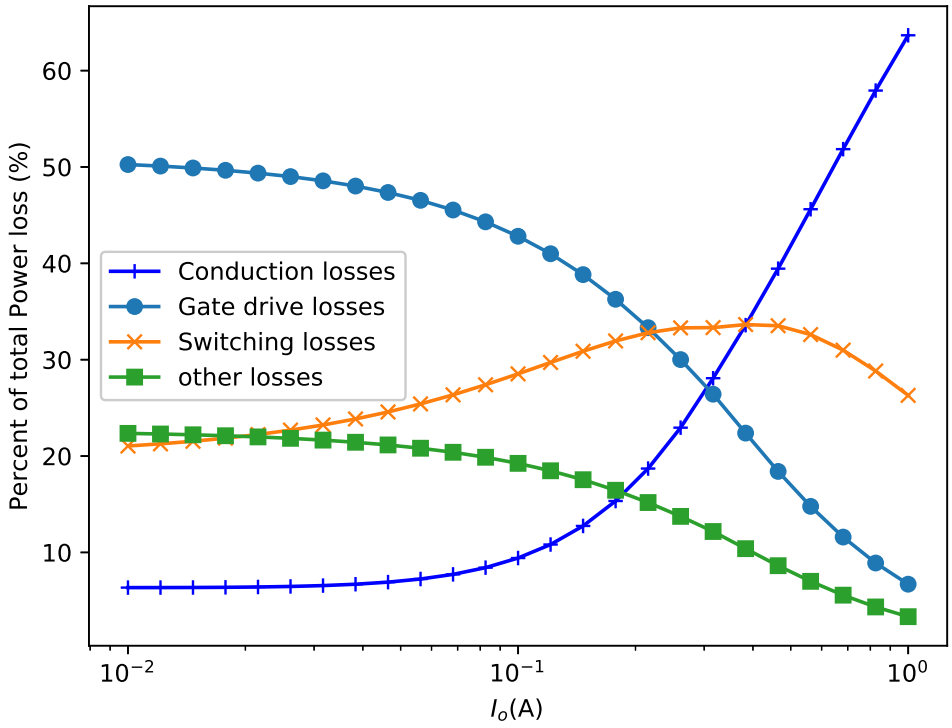

Figure 2.3: Contribution of various to total power loss

CHAPTER 3

MODELLING LOSSES IN BUCK CONVERTER

In this chapter we model different losses in the Buck converter using already available quantities such as the Technology parameters, Inductor parameters etc.,

3.1 Optimum size of Switches

In the Buck converter, the switches are implemented using MOSFETs.Volkan Kursun and Friedman (2003) gives an efficient way to calculate the optimum size of the MOSFETs that minimizes the losses. The Gate Drive losses and conduction losses in a MOSFET are given by

$$P_{MOS} = \frac{R_0}{W} I_{rms}^2 + C_{g0} W V_{in}^2 F_{sw}$$

where, R_0 and C_{g0} are the R_{DS_ON} and gate capacitor of 1μm wide transistor respectively. Now, differentiating P_{MOS} with respect to W and equating to zero gives the optimum width of the transistors for which the Losses are minimum.

$$\frac{dP_{MOS}}{dW} = 0 \implies \frac{-R_0 I_{rms}^2}{w^2} + C_{g0} V_{in}^2 F_{sw} = 0$$

$$\therefore W_{opt} = \sqrt{\frac{R_0 I_{rms}^2}{C_{g0} V_{in}^2 F_{sw}}} \qquad P_{MOS}(min) = 2\sqrt{R_0 I_{rms}^2 C_{g0} V_{in}^2 F_{sw}}$$

Now, the RMS current for NMOS and PMOS are given by

$$I_{rms}(PMOS) = \sqrt{D(I_o^2 + \frac{\Delta I_L^2}{12})}$$

$$I_{rms}(NMOS) = \sqrt{(1-D)(I_o^2 + \frac{\Delta I_L^2}{12})}$$

Hence, the total power loss in the switches is given by

$$P_{switches}(min) = \alpha\sqrt{(I_o^2 + \frac{\Delta I_L^2}{12}) F_{sw}}$$

where, $\alpha = 2\sqrt{DR_{0,PMOS}C_{g0,PMOS}V_{in}^2 + (1-D)R_{0,NMOS}C_{g0,NMOS}V_{in}^2}$ Here, the MOSFETs are used as switches. Hence, they are operated in Cut-off or Triode region. The Gate Capacitance of the MOSFETs in Cut-off or Triode region given by

$$C_{GATE} = C_{ox}WL$$

where, $C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$ is the Gate Capacitance of the MOSFET per unit area, W is the Width and L is the Length of the MOSFET. The $R_{DS_{ON}}$ of the MOSFET can be calculated as

$$R_{DS\_ON} = \frac{V_{DS}}{I_{DS}} = \frac{V_{DS}}{\mu C_{ox}\frac{W}{L}\Big((V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}\Big)}$$

Since, the switches have very small voltage drop across them when they are conducting, we can say $V_{DS}^2 \approx 0$. Hence the expression for R_{DS_ON} is given by

$$R_{DS\_ON} \approx \frac{V_{DS}}{\mu C_{ox}\frac{W}{L}\Big((V_{GS} - V_{th})V_{DS}\Big)} \approx \frac{1}{\mu C_{ox}\frac{W}{L}(V_{GS} - V_{th})}$$

The exact expressions for R_{DS_ON} of NMOS and PMOS are given below. Table 3.1 shows the mean and maximum error in the estimation of R_{DS_ON} based on the size of the MOSFTEs over 90 samples.

$$R_{DS\_ON}(PMOS) = \frac{1.11}{\mu_p C_{ox}\frac{W_p}{L_p}(V_{GSP} - V_{thp})}$$

$$R_{DS\_ON}(NMOS) = \frac{1.76}{\mu_n C_{ox}\frac{W_n}{L_n}(V_{GSN} - V_{thn})}$$

Table 3.1: Percentage errors in R_{DS_ON} estimation.

Parameter	Maximum Error (%)	Mean Error (%)
$R_{DS\_ON}(PMOS)$	0.422	0.107
$R_{DS\_ON}(NMOS)$	0.08	0.04

3.2 MOSFET Body Diode Voltage

The current through the diode (I_f), when a forward bias voltage of V_f is applied to it is given by

$$I_f = I_s\Big(e^{\frac{V_f}{V_T}} - 1\Big) \implies V_f = V_T ln\Big(\frac{I_f}{I_s} + 1\Big) = V_T ln(I_f + I_o) - V_T ln(I_s)$$

where, I_s is the saturation current and, $V_T = \dfrac{kT}{q}$ is the Thermal voltage of the diode. The saturation current I_s of the diode is directly proportional to its area of cross-section , which is directly proportional to the Width (W) of the MOSFET. Hence, the model used to find the Body diode voltage of the MOSFET is

$$V_f = A_1 ln(I_f + A_2 * W) + A_3 ln(W) + A_4$$

where, A_1, A_2, A_3, A_4 are constants, W is the width of the MOSFET. Based on the simulation results in LTSPICE, the forward bias voltage of NMOS, PMOS are given by

$$V_f(PMOS) = 0.0758 ln(I_f + 0.3364 W_p) - 0.0723 ln(W_p) + 0.4120$$

$$V_f(NMOS) = 0.1293 ln(I_f + 5.9309 W_n) - 0.1232 ln(W_n) + 0.1522$$

Table 3.2 shows the simulation results for the estimation of body diode voltage for PMOS and NMOS over 420 samples. The body diode conducts only when there is a

Table 3.2: Percentage errors in V_f estimation.

Parameter	Maximum Error (%)	Mean Error (%)
$V_f(PMOS)$	15.9	4.1
$V_f(NMOS)$	10.9	4.9

transition in circuit state from ON state to OFF state and vice versa. Since, during the transition, the current through the Inductor is either maximum or minimum, the power loss during dead time is given by

$$P_{DEAD} = (V_f(I_L(max))I_L(max) + V_f(I_L(min))I_L(min))T_{DEAD}F_{SW}$$

3.3 Inductor R_{ACR}

As the frequency of operation increases, the winding resistance of the Inductor increases due to skin effect. At higher frequencies, most of the current through the Inductor is confined to a small area near the surface of the Inductor determined by the penetration depth (D_{PEN}). The penetration depth (D_{PEN}) is defined as the radial distance from the surface of the Inductor where the current density is $\frac{1}{e}$ times the current density at the surface. The Penetration depth as a function of frequency is given by Eichhorn (2005) as

$$D_{PEN} = \sqrt{\frac{\rho}{\pi \mu F_{SW}}}$$

where, ρ is the resistivity of the conductor, μ is the permeability of the conductor. The R_{ACR} dissipates power only due to the AC current through the Inductor. Since the resistivity of the conductor remains constant, the ratio of R_{DCR} and R_{ACR} is simply the ratio of the effective area of cross-section for the respective currents.

$$\frac{R_{ACR}}{R_{DCR}} = \frac{\pi r_L^2}{\pi r_L^2 - \pi (r_L - D_{PEN})^2}$$

where, r_L is the radius of the Inductor coil. Hence, the AC power loss in the Inductor is given by

$$P_{ACR} = I_{ACRMS}^2 R_{ACR} = \frac{\Delta I_L^2}{12} R_{ACR}$$

3.4 Optimization Problem

3.4.1 Objective function

With the understanding of various losses in Buck converter, we can find the optimum sizes of switches and frequency of operation to minimize the Power loss. In section 3.1, we have established a relation between the optimum width of the MOSFET(W_{opt}) and the frequency of operation(F_{sw}). Hence, we just need to find the optimum frequency of operation for the Buck converter which will also give us the Optimum sizes of the MOSFETs. All the calculations are done at steady state conditions i.e., the input voltage and load conditions do not change with time. Also, the switching losses and Dead time losses and R_{ESR} losses are assumed to be constant as they contribute to a very small fraction of the total Power loss. Hence, the frequency dependency of the Power loss in

Buck converter is given by

$$P_{LOSS}(f) = \alpha\sqrt{(I_o^2 + \frac{\Delta I_L^2}{12})f} + \frac{\Delta I_L^2}{12}R_{ACR} + c$$

where, c is a constant which includes the Inductor DC losses, dead time losses, switching losses in MOSFETs and R_{ESR} losses. The Objective function can be written as

$$\underset{f}{\operatorname{argmin}}\, \alpha\sqrt{(I_o^2 + \frac{\Delta I_L^2}{12})f} + \frac{\Delta I_L^2}{12}R_{ACR} + c$$

Now,

$$\Delta I_L = \frac{(V_{in} - V_o)}{L}\frac{1}{f} = \frac{K_1}{f}$$

$$R_{ACR} = \frac{R_{DCR}}{1 - \left(1 - \frac{D_{pen}}{r_L}\right)^2} = \frac{R_{DCR}}{1 - \left(1 - \frac{1}{r_L}\sqrt{\frac{\rho}{\pi\mu f}}\right)^2} = \frac{R_{DCR}}{1 - \left(1 - \frac{K_2}{\sqrt{f}}\right)^2}$$

where, $K_1 = \frac{(V_{in} - V_o)}{L}$, $K_2 = \frac{1}{r_L}\sqrt{\frac{\rho}{\pi\mu}}$ are constants. The penetration depth of the Inductor is inversely proportional to the square root of frequency. Hence, at higher frequencies,

$$D_{pen} << r_L \implies \frac{D_{pen}}{r_L} << 1 \implies \frac{D_{pen}}{r_L} = \frac{K_2}{\sqrt{f}} << 1$$

Hence, we can approximate the R_{ACR} as

$$R_{ACR} = \frac{R_{DCR}}{1 - \left(1 - \frac{D_{pen}}{r_L}\right)^2} \approx \frac{R_{DCR}}{1 - \left(1 - \frac{2K_2}{\sqrt{f}}\right)} \approx \frac{R_{DCR}\sqrt{f}}{2K_2}$$

Now, the total power loss in Buck converter is given by,

$$P_{LOSS}(f) = \alpha\sqrt{I_o^2 f + \frac{K_1^2}{12f}} + \frac{K_1^2}{12f^2}\frac{R_{DCR}\sqrt{f}}{2K_2} = \alpha\sqrt{I_o^2 f + \frac{K_1^2}{12f}} + \frac{K_1^2 R_{DCR}}{24K_2 f^{3/2}}$$

At lower frequencies, $\frac{1}{f}$ and $\frac{1}{f^{3/2}}$ terms dominate and we can neglect the $I_o^2 f$ term. At higher frequencies, $I_o^2 f$ term dominates and we can neglect the $\frac{1}{f}$ and $\frac{1}{f^{3/2}}$ terms.Hence, at optimum frequency both are equal. The Optimum frequency that minimizes the above

expression is given by

$$f_{opt} = \frac{\sqrt{\frac{K_1^2}{12}} + \sqrt{\frac{K_1^2}{12} + \frac{I_o K_1^2 R_{DCR}}{6\alpha K_2}}}{2I_o}$$

3.4.2 Results

An example of this loss model can be developed using the circuit shown in Fig 3.4. Here the Buck converter is operated with the following specifications

Table 3.3: Buck Converter specifications for testing.

Technology	0.18μm CMOS process
Input Voltage (V_{in})	1.8V
Output Voltage (V_{out})	1V
Load Current (I_o)	0.5A
Inductor (L)	0.22μH
Inductor coil properties	$\rho = 1.72 \cdot 10^{-8}\Omega m, \mu = 4\pi \cdot 10^{-7} Hm^{-1}$
Inductor coil radius	0.1mm
Inductor R_{DCR}	20mΩ
Inductor saturation current (I_{sat})	2A
Capacitor (C)	47μF
Capacitor ESR	10mΩ

For this example the PWM Rise-time, fall-time and the dead time for the MOSFETs are fixed at 0.5% of the Switching period (T_{sw}). The Optimum operating frequency and the sizes of switches are calculated for the above circuit using different approaches and the results are available in table 3.2. Fig. 3.1 shows the Power loss in Buck converter as a function of frequency The Optimum frequencies obtained using mathematical ap-

Table 3.4: F_{opt} and switch sizes calculated using different approaches

Approach	$f_{opt}(MHz)$	W_p (mm)	W_n (mm)	Efficiency (%)
Mathematical	3.3	144.8	73.2	96.42
Power loss model	3.43	141.4	71.5	96.42
Simulations	2.58	169.3	85.5	96.8

proach and by iterating over a range of frequencies are very close to each other, even though we have approximated the switching losses and the Capacitor ESR losses to be constant. This is because the circuit spends very little time during transition from one

state to another (0.5% T_{sw}) and the R_{ESR} is also very low. The difference in the power loss from the simulations and that from our model is because of some of the losses that have been unaccounted for, such as, the core losses in the Inductor.

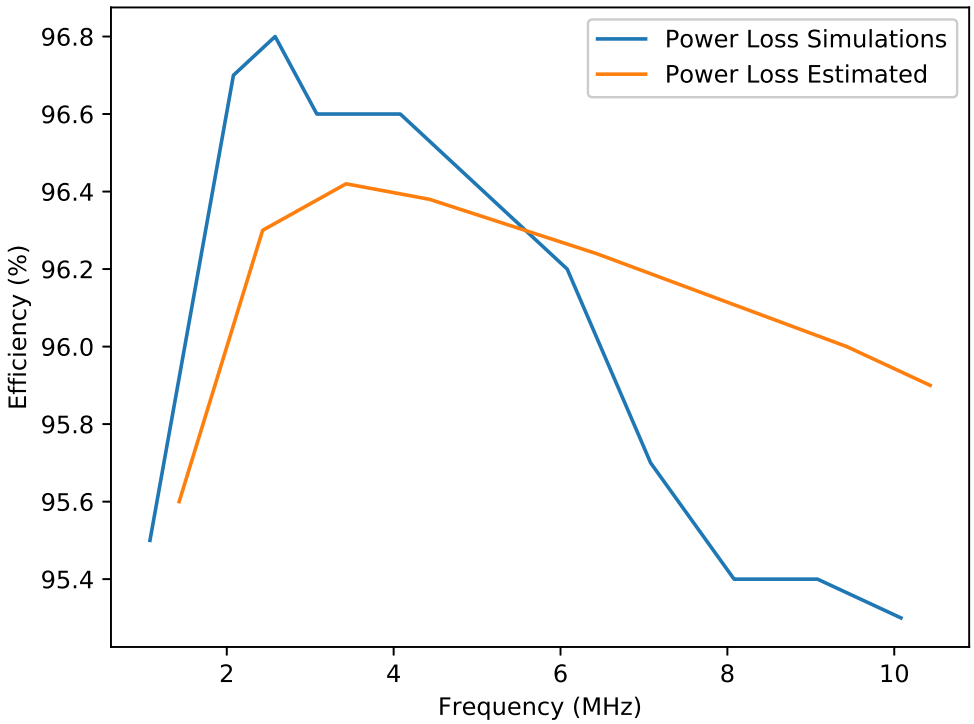

Figure 3.1: Power loss as a function of frequency

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