DESIGN OF AN AMPLIFIER WITH SINUSOIDAL GAIN AND ITS USE IN GENERATING SQUARE ROOT OF SUM OF SQUARES

A Thesis

Submitted By

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THESIS CERTIFICATE

This is to certify that the thesis titled "**Design of an Amplifier with Sinusoidal Gain and its use in generating Square Root of Sum of Squares**", submitted by **Mr. Shuvadeep Mitra**, to the Indian Institute of Technology Madras, Chennai for the award of the degree of **Master of Technology**, is a bona fide record of research work done by him under my supervision. The contents of this thesis, in full or a part has not been submitted to any other Institute or University for the award of any degree or diploma.

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EE13M108

ABSTRACT

The thesis focuses on hardware optimized implementation of an elegant method that performs the mathematical operation “square root of the sum of the squares” on two given inputs. The method involves amplitude modulation of two quadrature shifted carriers by the two given inputs and then envelope detection of the sum of the two amplitude modulated signals. The two inputs are required to be multiplied with sinusoidal and co-sinusoidal carriers. Then the maximum value of their sum gives the desired result.

The implementation requires designing an amplifier whose gain varies in sinusoidal fashion in uniform steps. This amplifier helps us in realizing the circuit without the need of multipliers which usually lack in accuracy. The prototype of the scheme is successfully implemented using Elvis board with discreet components. The data from the Elvis board are acquired by the Lab VIEW software and thereafter the performance of the circuit is examined.

This kind of scheme very often finds its application in the field of measurement. The applications include obtaining the magnitude of complex impedance [1], calculating the apparent power from measured values of active and reactive power [2], computing the magnitude in a lock-in amplifier [3] and etc.

TABLE OF CONTENTS

LIST OF FIGURES

ABBREVIATIONS

RMS	Root Mean Square
SQRSS	Square Root of Sum of Square
LOG	Logarithmic
OPAMP	Operational Amplifier
FPGA	Field Programmable Gate Array
LTI	Linear Time Invariant
IC	Integrated Circuit
CLK	Clock
INC	Increment
NI ELVIS	National Instruments Educational Laboratory Virtual Instrumentation Suite
SFP	Software Front Panel
AI	Analog Input
AO	Analog Output
DMM	Digital Multimeter
FGEN	Function Generator
VPS	Variable Power Supply
DSA	Dynamic Signal Analyzer
ARB	Arbitrary waveform generator

CHAPTER 1

INTRODUCTION

1.1 ROOT MEAN SQUARE

Root Mean Square or RMS is a very well-known mathematical operation in the field of physics and engineering. This is a statistical measure, sometimes also referred as Quadratic Mean. This function has got many applications. It is possible to calculate the RMS for a sequence of discreet values as well as continuously varying function. So, as the name suggests this function is actually the square root of the arithmetic mean of the squares of the samples. Therefore the mathematical definition RMS is given by (1.1)

$$x_{rms} = \sqrt{\frac{1}{n}(x_1^2 + x_2^2 + \cdots + x_n^2)} \tag{1.1}$$

In (1.1), $x_1, x_2, \ldots x_n$ constitute the set of "n" discreet values.

1.2 SQUARE ROOT OF SUM OF SQUARES

The works behind this thesis mainly consists of obtaining the square root of the sum of squares (SQRSS) for two inputs. This mathematical function can also be considered as a special case of RMS. The mathematical definition of SQRSS is given by (1.2)

$$v_{sqrss} = \sqrt{x^2 + y^2} \tag{1.2}$$

In (1.2), x and y denote the two inputs.

In the field of measurement often we come across the necessity for the computation of “square root of sum of squares” (SQRSS) of two given inputs. For instances (i) in obtaining magnitude of an impedance from its resistive and reactive parts [1]. (ii) Calculating the apparent power from measured values of active and

reactive power [2]. (iii) Computing the magnitude in a lock-in amplifier [3]. A simple implementation of the desired mathematical function would necessitate three multipliers and a summing amplifier with one of the multiplier being configured to work as a square rooting circuit with appropriate feedback [4]. However the same mathematical operation can also be realized with the aid of LOG and Anti-LOG amplifiers along with few summing amplifiers and normal gain amplifiers arranged in an appropriate configuration. But as obvious, the system becomes too hefty and thus the configuration hardly remains feasible for practical uses.

One smart but approximate method with only OPAMPs and switches which ideally gives an error of less than 2% and another technique with quadrature oscillator in conjunction with two multipliers gives in principle an accurate result are presented in [5]. But both of these methods suffer from the trade-off between hardware optimization and relative error in output. The second method in principle gives the accurate result but the measure of its accuracy relies vastly on the accuracy of the multipliers used and getting accurate as well as precise multipliers as discreet components is quite difficult. One implementation of the 1st method is found in [6] with the aid of FPGA board. So this thesis proposes a simple implementation which in principle is based on the basic ideas in [5] but relaxes the tradeoff remarkably and executes the mathematical function, namely, square root of sum of squares of two given inputs.

1.3 OBJECTIVE

The objective of this thesis is broadly centered on making a circuit to realize the mathematical operation, namely SQRSS. The principle which is used is same as shown in [5]. But as mentioned earlier the trade-off between the accuracy and hardware optimization is relaxed by the work presented in this thesis.

1.4 ORGANIZATION OF WORK

A brief introduction of the operation of root mean square “RMS” and square root of the sum of square, “SQRSS” is presented as a motivation of the work in chapter 1

along with a little bit of literature survey. Chapter 2 describes the methodology based on which rest of the work in this thesis is carried out. Chapter 3 and chapter 4 respectively explain the topology and design procedure of the main building block of the prototype, sine/cosine amplifier. Then a concise discussion on error analysis is carried out in chapter 5. Thereafter the experimental setup and results obtained from the prototype are shown in chapter 6 and finally chapter 7 concludes the thesis with conclusion and future work.

CHAPTER 2

METHODOLOGY

2.1 BASIC PRINCIPLE

Assuming x and y as the two input quantities we define another quantity, z as

$$z = ax + by \tag{2.1}$$

In (2.1) $a = \cos\alpha$ and $b = \sin\alpha$, so z can then be expressed as in (2.2) where $\theta = \arctan(y/x)$

$$z = \sqrt{x^2 + y^2}cos(\theta - \alpha) \tag{2.2}$$

If $\alpha = \theta$, then $z = \sqrt{x^2 + y^2}$. If not $z < \sqrt{x^2 + y^2}$. So the bottom line of the problem is to choose an appropriate value of α in order to maximize z and thus obtain $\sqrt{x^2 + y^2}$.

However (2.1) and (2.2) also imply one more thing. If x is multiplied with a sinusoid and similarly y is multiplied with a co-sinusoid then the summation of the two results in another sinusoid whose amplitude turns out to be $\sqrt{x^2 + y^2}$.

In order to do so, in the proposed method, the two inputs x and y are passed through two amplifiers whose gain varies in sinusoidal and co-sinusoidal fashions respectively. The outputs of these two amplifiers are added to obtain another sinusoid, whose amplitude gives the maximum value of z, given in (2.2), and the required result. Fig 2.1 shows one illustration of it.

Now another very crucial observation can also be made from Fig 2.1 and equation (2.2). Considering both x and y as positive, the α in (2.2) will come within $0 - 90^{\circ}$ so the maxima of the resulting sinusoid, z, will also occur in that range. The Fig 2.2 is another example to illustrate the same.

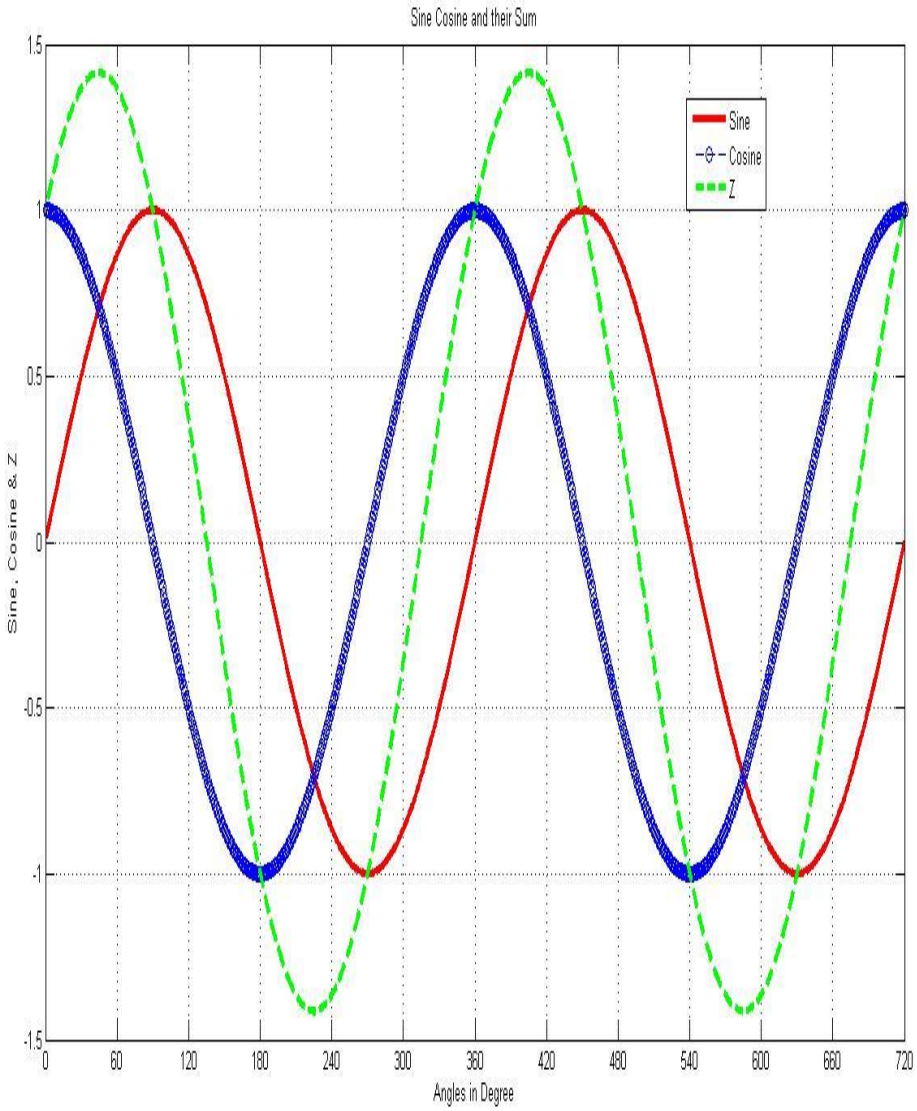


Fig 2.1: Sine and Cosine of unit amplitude are shown in red and blue plots respectively. The two add up to give another sinusoid of amplitude $\sqrt{\mathbf{2}}$ which is shown in the green plot. The horizontal axis denotes the angle in degree.

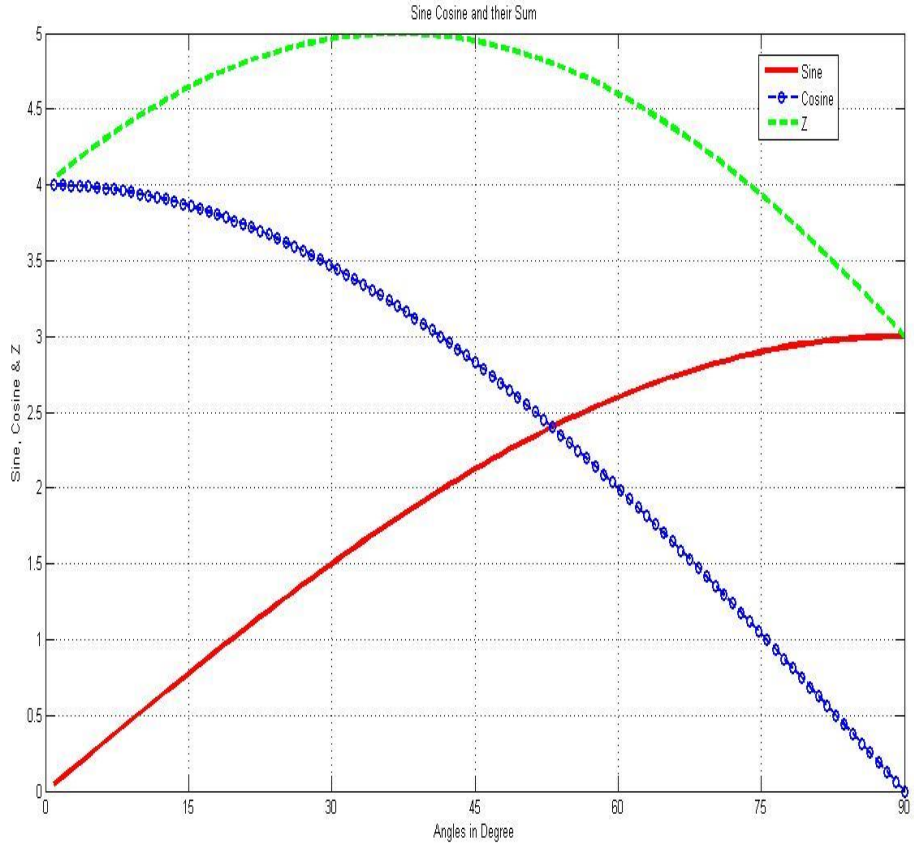


Fig 2.2: Sine and Cosine of amplitudes 3 and 4 are shown in red and blue plots respectively. The two add up to give another sinusoid of amplitude **5** which is shown in the green plot. The horizontal axis denotes the angle in degree.

CHAPTER 3

TOPOLOGY

3.1 AVAILABLE TOPOLOGIES

From the discussion in the previous chapter the bottom line of the condition is very clear. The key problem is to devise an amplifier whose gain varies in a sinusoidal manner. Now in usual practice we more often come across Linear Time Invariant (LTI) systems. Although no actual system is in principle LTI but modeling them as LTI works reasonably well for all practical purposes. LTI systems are characterized with a transfer function that does not change with time and thus make the analysis as well as the design easier. Therefore in this case the amplifier which is required provides a gain which varies in a sinusoidal fashion with time and thus does not belong to the set of LTI.

So far in the literature many procedures have been reported to obtain the pattern of sine without actually using any sinusoid. One such is piecewise linear approximation of sinusoid [8] which in principle is actually exploited in the 1st method, proposed in [5] and also in [6]. The basic principle is pretty simple. The entire pattern of sinusoid is broken into fragments. Each of those fragments gives the gain at that instant. So basically a sufficient number of LTI amplifiers are made and each of those amplifiers is chosen appropriately at the right instants. The Fig. 3.1 shows the gain characteristic of the sine amplifier, basic building block, as shown in the first method mentioned in [5].

The topology proposed in this thesis is broadly based on the idea of parabolic approximation of sinusoid [7]. The idea is more or less the following. A pattern is first obtained by approximating a parabola with a sinusoid. A 2nd order parabolic polynomial is framed taking angle as the independent variable such that the polynomial attains the same value as the original sinusoid at 0° and 90°. Now after this pattern is obtained it is compared with the original sinusoid at every angle and subsequently appropriate values are added or subtracted from the pattern for different

angles. Now this entire thing is done with digital system. Novelty of this technique lied in the fact that the parabolic approximation which was obtained in the 1st iteration was already quite close to the actual sinusoid. Thus the maximum error was also quite low and hence lesser memory is required for implementation.

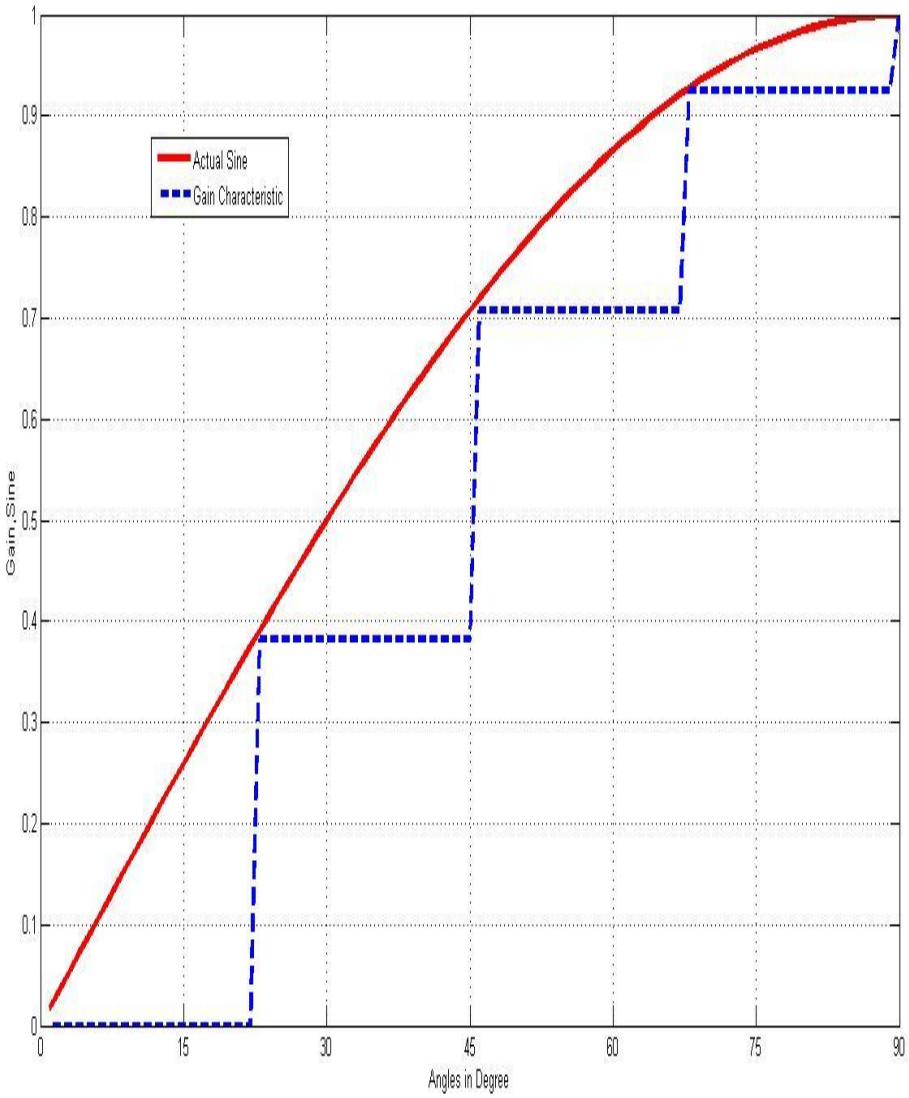


Fig 3.1: Gain characteristic, as depicted in [5], is shown in blue and the red plot shows the actual sinusoid. The horizontal axis denotes the angle in degree.

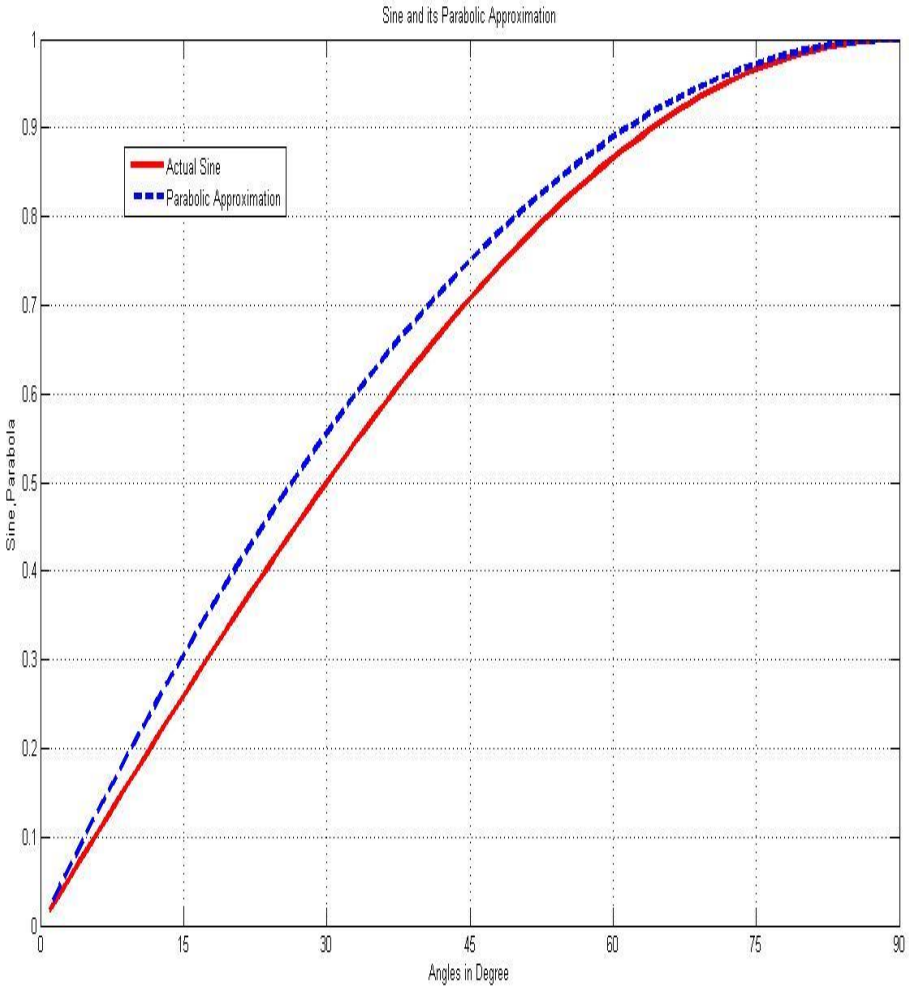


Fig 3.2: Pattern obtained from parabolic approximation is shown in blue. The red plot shows the actual sinusoid. The horizontal axis denotes angles in degree.

The underlying philosophy to design the sine amplifier as depicted in this thesis goes like this. In a simple OPAMP based inverting amplifier the gain turns out to be the ratio of the feedback and the input resistors employed. Keeping the input resistance constant, if the feedback resistance can be varied in a fashion that is close to sinusoid in 1st quadrant with a tolerable error, then that would give an amplifier with sinusoidal gain and potentially give a solution to the problem.

Let us consider we have two resistors $R_1(j)$ and r_1. $R_1(j)$ is a variable resistor whereas the value of r_1 is fixed. If the values of resistor R_{1_j} is varied in uniform steps, say for $j = 1, 2, 3, \ldots, n$ from zero to its maximum resistance in steps of S_1 with r_1

parallel to it, we would obtain an overall resistance curve which is parabolic in nature. By choosing this combination in the feedback path of an inverting amplifier and then choosing the input resistor, R_i, appropriately depending upon the value of S_1, we can obtain nearly sinusoidal gain for small angles, say less than 15°. Similarly, by choosing r_1 appropriately depending upon the maximum value of the variable resistor, say $R_{1_{max}}$ and already chosen R_i, we can obtain nearly sinusoidal behavior for higher angles, say between 65° and 90°, as well. Fig.3.3 shows the gain versus angle curve for $R_{1_{max}} = 10\ k\Omega$, $S_1 = 100\ \Omega/step$, $r_1 = 15\ k\Omega$ and $R_i = 6\ k\Omega$.

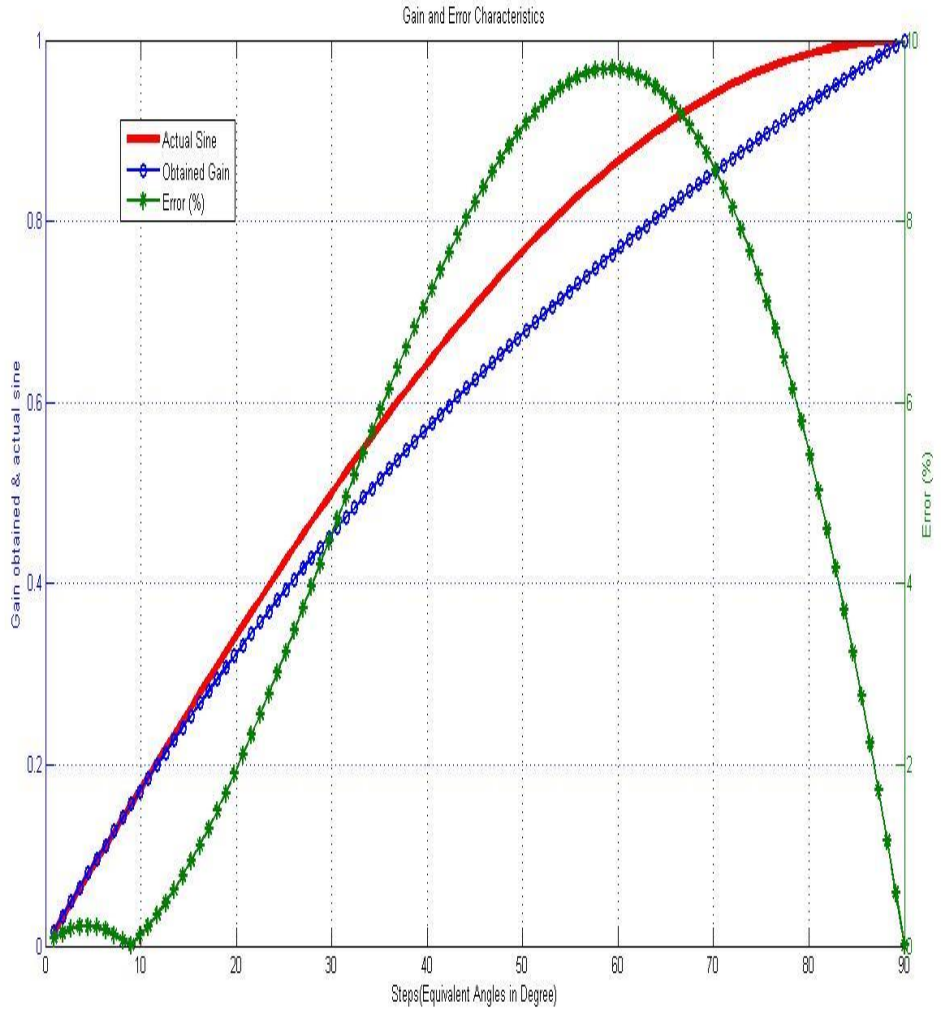


Fig 3.3: Gain characteristic. The plot in red shows the actual sinusoid and the plot in green shows the percentage error between actual sinusoid and the obtained gain. The horizontal axis denotes angle in degree.

But with this topology, designers are left with no option to control the gain in mid angles. In order to account for this one more tweaking parameter was needed. But also the freedom of setting the gain at 0° and 90° should also not be hampered. Thus another variable resistor, $R_2(j)$, was put in series with the r_1. But here often a problem is encountered as not all values of variable resistor are available industrially. So to overcome this difficulty another fixed resistor r_2 is chosen to put in parallel to $R_2(j)$. The new variable resistor $R_2(j)$ is reduced from some maximum value, $R_{2_{max}}$, to zero in equal number of steps as $R_1(j)$. A functional diagram of this topology is shown in Fig 3.4.

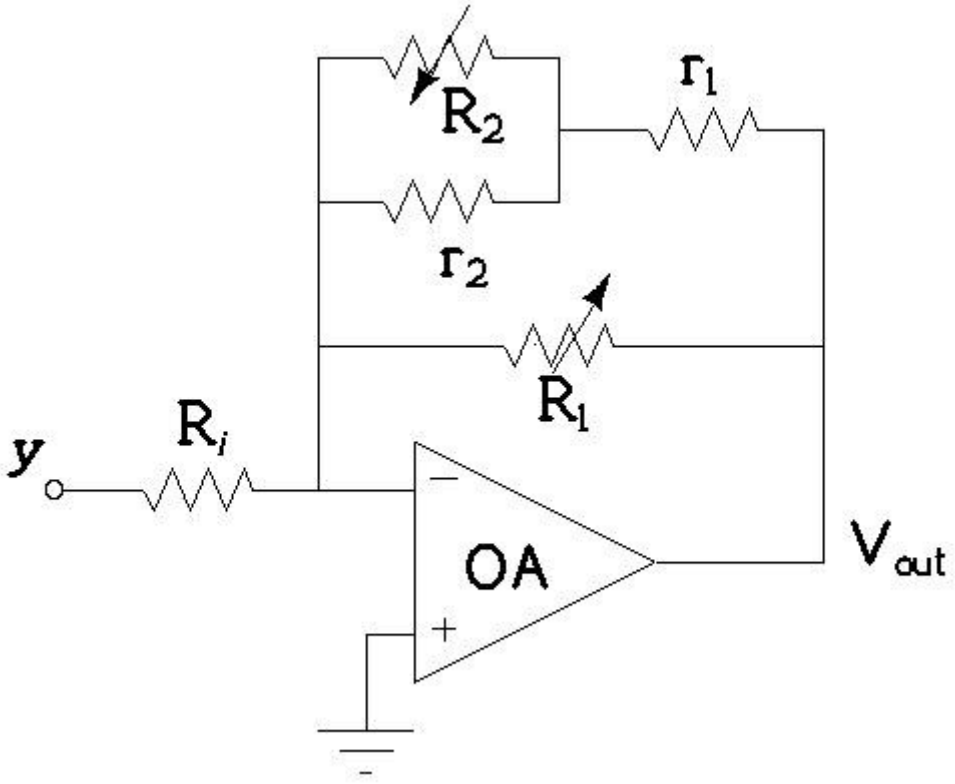


Fig 3.4: Functional Diagram of Sine amplifier topology.

CHAPTER 4

DESIGN PROCEDURE

4.1 STEPS TO DESIGN THE SINE AMPLIFIER

In the previous chapter a brief discussion was provided regarding how the topology to design the sine amplifier is finalized. Now that itself quite elucidate how is the design needed to be done. This thesis presents a procedure to design the sine amplifier that is not quite deterministic in nature however that still helps the designers in getting their purpose served. An iterative procedure is followed to design the parameters of proposed amplifier. The exact mathematical solution turns out to be quite complex due to the presence of too many variables and parameters.

Like all the iterative process here also a simple principle is followed. At first a starting point of the iteration is decided and then the things are tweaked based on the requirement. So naturally finding out the starting point turns out to be something which is very interesting and demands wise judgments and compatibility. The procedure is explained in the following steps.

4.1.1 CHOOSING R_1

The topology for the sine amplifier is decided in a way as shown in chapter 3. So from Fig.3.4 readers can notice the topology contains one OPAMP, two variable resistors and three fixed resistors. The variable resistors require a signal which dictates should it increase or decrease with every clock cycle and henceforth a clock is also required by it. So among those two variable resistors R_1 is the one which this particular section is going to focus on.

As R_1 is a variable resistor the factors which determine how to choose it are a) minimum resistance that it can provide b) the maximum resistance that it can provide c) number of steps it takes to reach from its minimum resistance to its maximum resistance. Another factor which is there is the maximum clock frequency that it can

work with. But that is not so relevant with our purpose so that is not taken into consideration.

Apart from these, the factor which really plays the deterministic role in choosing R_1 is the availability in the market. So keeping these in mind the IC X9C103 is chosen for using it in the prototype. As far as the circuit is concerned, R_1 is needed to have a minimum resistance of zero in order to match with actual sinusoid at 0° and so does this IC X9C103. It is in principle a digital potentiometer which gives the minimum resistance of 0Ω and the maximum of $10k\Omega$ in a total of 100 steps. So its step size and maximum resistance are given by following equations respectively.

$$S_1 = 100\ \Omega/step \tag{4.1}$$

$$R_{1_{max}} = 10k\Omega \tag{4.2}$$

4.1.2 CHOOSING R_i

The R_i determines the input resistance of the overall system. It also determines the instantaneous gain of the amplifier depending upon the instantaneous overall resistance in the feedback. Now however the input resistance in this case is not a constraint. So it is chosen depending upon the gain which is required.

Now the selection of R_i is largely based on R_1. So it is chosen in the following way. For small values of angle sine of that angle is given by the equation (4.3)

$$\sin\theta \cong \theta \tag{4.3}$$

In equation (4.3) θ is in radian.

In the configuration, used in this thesis to design the sine amplifier, the actual expression for gain is given by

$$A = \left[\frac{R_1R_2(r_1+r_2)+r_1r_2R_1}{R_2(r_1+r_2)+r_1r_2+R_1(R_2+r_2)}\right]/R_i \tag{4.4}$$

So from (4.4) and also from the configuration shown in Fig.3.4, it is intuitively conclusive that for small angles the effective resistance in the feedback path is mainly going to be the resistance offered by $R_1(j)$. This can be explained in the following way. The angle is going to be decided by the number of steps. For smaller angles the number of steps is also going to be less. So R_1 is going to offer a very small resistance. Thus overall resistance in the feedback path will be more or less equal to what R_1 offers.

Therefore for smaller angles the gain of the amplifier can be approximated as

$$A \cong \frac{R_1(j)}{R_i} \tag{4.5}$$

Therefore, considering R_1 as what is already chosen as, the gain after the 1st step is given by the following equation.

$$A = \frac{S_1}{R_i} \tag{4.6}$$

Now as R_1 takes total hundred steps to reach from its minimum to maximum value thus the angle represented by the 1st step is therefore given by the following equation.

$$\theta = \frac{\pi/2}{100} \tag{4.7}$$

So as depicted by equation (4.3), the gain at the end of 1st step will have to be equal to the RHS of equation (4.7). So with that note R_i is chosen on the basis of following equation.

$$R_i = \frac{S_1}{\pi/200} \tag{4.8}$$

Now as an iterative procedure is followed thus the solution of equation (4.8) is rounded off and R_i is chosen as 6kΩ.

4.1.3 CHOOSING r_1

The philosophy, adopted in determining the topology of the sine amplifier is not only helpful in that regard but it also helps the reader in gaining insight about how to choose these components used in the topology. Perhaps the reader should remember while determining the topology, the pattern of sinusoid in the 1st quadrant was broadly classified into three sections, which are as follows.

a) For smaller angles (say from 0° to 30°)
b) For larger angles (say from 65° to 90°)
c) For rest of the angles in the middle.

Now as equation (4.3) suggested for smaller angles, sine of that angle can be approximated by the angle expressed in radian. Therefore it also implies a straight line passing through the origin with a slope equal to that of sinusoid at 0° would give a reasonable approximation for the sinusoid up to certain angles depending upon the margin of error the designer is able to tolerate. Thus on the basis of this only, an approximated pattern of sinusoid is obtained for smaller angles.

Step 1 and step 2 give quite a lucid logical reasoning for choosing R_1 and R_i. Now having chosen those successfully implies the approximating pattern for smaller angles is obtained. Therefore now the obvious task is to move on to the next section of the sinusoid. So the next section is angles at the vicinity of 90°.

Now from the topology section it is clear that the pattern in this second section is obtained mainly by the resistor r_1. The role of the resistor r_1 is to determine the gain for angles close to 90°. Thus to choose a value for this resistor the gain required at 90° is taken as reference. At 90°, that is for j=100, the resistor R_2 would reach its minimum value of zero ohm. So the overall feedback resistance turns out to be $r_1 \parallel R_{1_{max}}$ and the gain required is 1. So for the prototype it is chosen as $15k\Omega$ following the equation (4.9).

$$\frac{r_1 \parallel R_{1_{max}}}{R_i} = 1 \tag{4.9}$$

4.1.4 CHOOSING R_2

So far few of the components have been chosen so as to obtain the gain pattern at smaller and larger angles. So the remaining section is third one, which is the middle section. Now as discussed in the chapter of topology each of the component used in the configuration which is decided, has got their role to play at some specific range of angles.

From equation (4.4) it is pretty understandable that how much equivocal is the original expression of the gain for the configuration which has been decided. So many factors appear implicitly at a time. Thus dealing with this expression of gain in order to obtain the required pattern is understandably difficult.

Thus keeping this in mind, the design procedure is formulated in such a way that it helps the designer to deal with different section of the pattern separately with ease. So in order to obtain the pattern in the middle section the $R_2 \parallel r_2$ combination is to be set appropriately. Now in this step, the variable resistor R_2 is chosen and the next step shows how to choose r_2.

Like the variable resistor R_1, this R_2 is also chosen with almost the same philosophy as discussed in step 1. Now having already chosen R_1 this variable resistor R_2 was to be chosen in a way which satiates the following constraints.

a) It had to be taking same number of steps as R_1 for reaching from its minimum value of resistance to its maximum value of resistance.
b) It also had to be offering the minimum resistance of zero ohm.
c) Its maximum resistance had to be certainly greater than that offered by R_1.

From the discussion we had so far, the reader may find a little difficulty in understanding how does the 3rd constraint come or where does it come from. But hopefully a better understanding regarding that can be found subsequently.

So like R_1 in case of R_2 also the biggest factor that was taken care of in choosing it was availability in market. Thus the next potentiometer of the same series, X9C503, is chosen as R_2. The number of steps it takes to reach from its minimum to maximum is same as R_1, which is hundred. Also as required it provides a minimum resistance of zero ohm and a maximum resistance of $50k\Omega$, which is greater than that of what is chosen as R_1.

So its step size and maximum resistance are given by following equations respectively.

$$S_2 = 500\ \Omega/step \tag{4.10}$$

$$R_{2_{max}} = 50k\Omega \tag{4.11}$$

4.1.5 CHOOSING r_2

So as mentioned in the previous step, this step is going to focus on how to choose the resistor r_2. So the last step depicts the choice of R_2. That was also a partial step in order to obtain the pattern in mid angles zone.

Having chosen R_2, choosing this resistor r_2 is just like doing subsequent steps of an equation. Now to obtain the pattern for these mid angles the value of sinusoid at an angle of 45° is chosen as reference. Now 45° is exactly halfway between zero and 90°. Now for both the variable resistors R_1 and R_2, the components which are chosen take a total of 100 steps to reach from its minimum to maximum value of resistance or vice-versa. Therefore the 0^{th} step corresponds to 0° and the 100th step corresponds to 90°. Therefore for 45° the corresponding step is the 50th one.

The 50th step is exactly the halfway between minimum and maximum for both the variable resistors. Thus at this step both the variable resistors will be offering resistance of magnitude which is half its maximum value. So R_1 will be offering a resistance of $5k\Omega$ and R_2 will be offering a resistance of $25k\Omega$. Thus r_2 is chosen as $27k\Omega$ by rounding off the solution of equation (4.12).

$$\frac{\left(\left(\frac{R_{2_{max}}}{2} \parallel r_2\right) + r_1\right) \parallel \frac{R_{1_{max}}}{2}}{R_i} = \frac{1}{\sqrt{2}} \tag{4.12}$$

So the starting point for our iteration is chosen as the following.

$R_i = 6\ k\Omega, R_{1_{max}} = 10\ k\Omega, r_1 = 15\ k\Omega, R_{2_{max}} = 50\ k\Omega, r_2 = 27\ k\Omega$

The following figure shows the gain characteristic that is obtained in the first iteration.

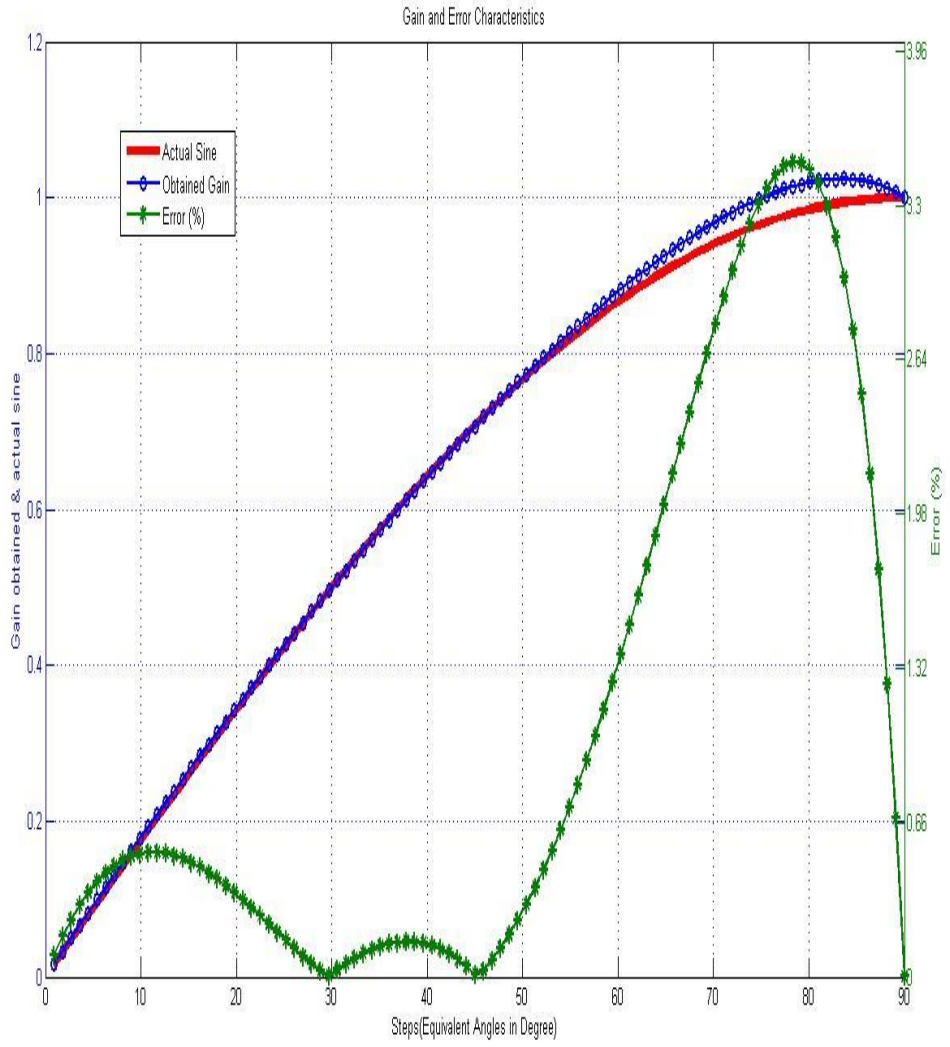


Fig 4.1: The plot in blue shows gain characteristics with equivalent angles. Plot in red shows actual sinusoid and the plot in green shows percentage error. The horizontal axis denotes the angle in degree.

4.1.6 ANALYSIS OF THE RESULT OBTAINED IN 1^{st} ITERATION

As the procedure shown in this thesis to design the sine amplifier, is iterative in nature thus analysis of the result obtained in every step is utterly important. So far only the starting point of the iteration is obtained and the result is what is shown in Fig.4.1. The green plot in the Fig.4.1 shows percentage error with respect to the maximum which is 1. So obviously the target is to reduce this relative percentage error. Now it can be noticed from Fig.4.1 that the error between the desired and the actual pattern is more between 45° and 90°. With a little more minute observation it can also be noticed that this is occurring mainly because the pattern which is obtained shows a peaking around 80° where the gain even goes beyond one. Now the reason behind this can be figured out very easily. The variable resistor R_2 starts off with a very high value and then gradually decreases with every step. Now the peaking implies at those steps or equivalent angles it has not yet got reduced sufficiently. This observation is actually a very useful guideline for designers to narrow down their choices of R_2 because it suggests choosing the $R_{2_{max}}$ as too high is going to cause a higher peaking and higher error. Following figure shows the gain curve obtained in 1st iteration with $R_{2_{max}}$ being chosen as $100k\Omega$, which evidently gives an exorbitantly high error.

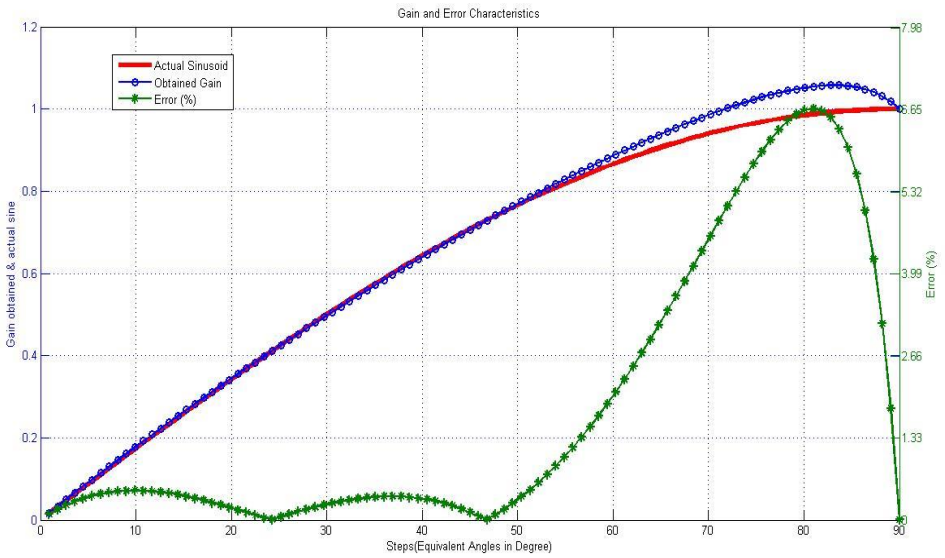


Fig 4.2: Plot in blue shows gain obtained. Plot in red shows actual sinusoid. Plot in green shows percentage error. The horizontal axis denotes the equivalent angles in degree.

4.1.7 FINE TUNING

Once starting point of iteration is obtained, the rest is about properly tweaking. But as there were too many resistors so it is necessary to first decide which one is to be used for tweaking and which one is better not to be touched. Now R_1 and R_2 are digital potentiometers and are not available in market in all values. Thus those are better not to be touched. Also tweaking R_i would either increase or decrease the gain for all angles. Given the pattern which is already obtained, increasing or decreasing the gain by the same amount for all angles was not so necessary. So R_i is also not changed from what it was chosen as in the 1st iteration. Thus the only remaining options were r_1 and r_2. With the already chosen values for other components, only tweaking the r_1 sufficed the purpose. Evidently the peaking was the biggest source of error. So to reduce its detriment the value of r_1 is reduced. This would definitely reduce the gain in final step but it would also reduce the error due to the peaking drastically.

But before coming to the final conclusion, one last thing is worth noticing. With a little bit of calculation it can be seen that with the values chosen for R_1, r_1 and R_i, for achieving a gain of $1/\sqrt{2}$ at angle 45° the $R_2 \parallel r_2$ combination needs to give a resistance of $13\text{k}\Omega$. Now this indicates in the first place that the maximum resistance to be offered by R_2 is expected to be greater than that of R_1. Also it justifies why choosing $R_{2_{max}}$ as $100\text{k}\Omega$ would make the design impossible. Because it would then require r_2 to be much low and make the gain at mid angles to be much more sensitive with it and thus no more allow the designer to use it as a tweaking parameter. From Fig. 4.2 it is evident how enormously high error is encountered with $R_{2_{max}}$ as $100\text{k}\Omega$ and it would be impossible to be reduced.

So following the afore stated steps the best result (less than 2% error) is obtained from 0° to 87° with

$R_i = 6\text{k}\Omega$, $R_{1_{max}} = 10\text{k}\Omega$, $r_1 = 13.5\text{k}\Omega$, $R_{2_{max}} = 50\text{k}\Omega$ and $r_2 = 27\ \text{K}\Omega$.

The following figure shows the final best possible result.

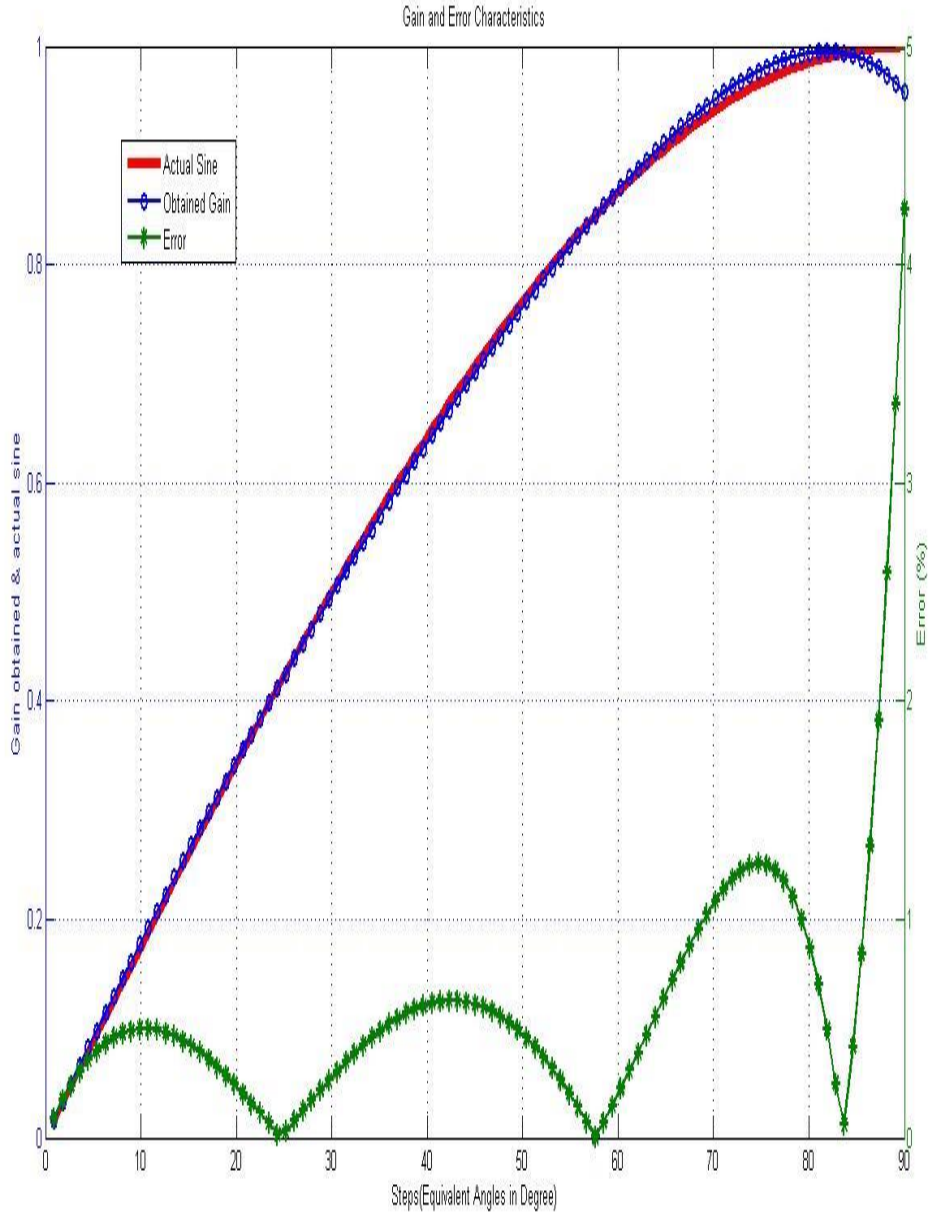


Fig 4.3: Plot in blue shows gain. Plot in red shows actual sinusoid and the plot in green shows percentage error. The horizontal axis denotes the equivalent angles expressed in degree.

4.1.8 DESIGNING THE COSINE AMPLIFIER

Once the sine amplifier is designed the cosine amplifier is obtained by giving complimented clock to variable resistors as its increment/decrement signal. The following figures show the sine and cosine amplifier respectively.

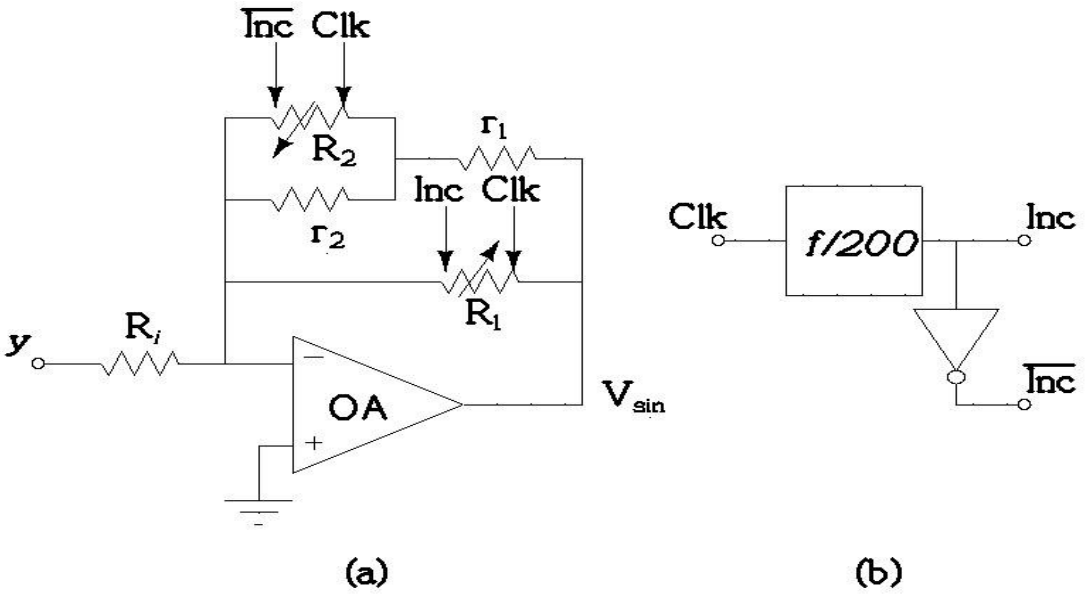


Fig 4.4: (a)Sine Amplifier (b) Clock circuit

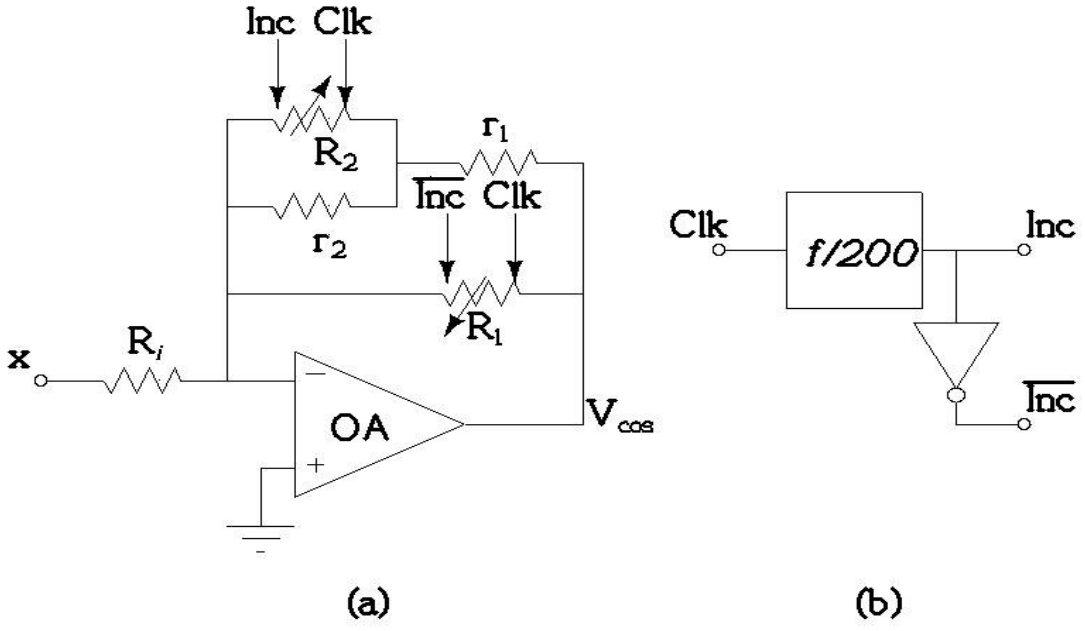


Fig 4.5: (a)Cosine Amplifier (b) Clock circuit

CHAPTER 5

ERROR ANALYSIS

In any board level circuitry one very important aspect is the error analysis. Even after putting and wiring up all the components appropriately on bread board, many a times designers fail to see the results which were in principle expected. Lot of factors comes into play. Parasitics from almost every node appear all at a time. Anyhow, so keeping all these things in mind it is extremely recommended to all designers to have a profound knowledge about different sources of error in the circuits they design.

So our primary objective is to now figure out the potential sources of error those are present in the circuit. Now in general there are ideally infinite sources of error that could be potentially present in the circuit. The connecting wires are often found to be adding huge parasitic capacitances; components used sometimes give some offset, few of them may also go out of its linear range and many more. And these kinds of sources usually add random errors to the final results. Apart from these there are examples of error sources which add systematic errors. Like error in measurements, parallax error, human error etc. In this chapter of the thesis mainly the random error are focused on. First the possible sources of errors are determined from the circuit and then a brief discussion is presented for each of the sources of error. The effects of each of those errors are shown and derived mathematically with appropriate assumptions in order to avoid not so relevant mathematical complexity. Now to figure out the possible sources of error one needs to check how the circuit looks like. The following figure shows the total circuit in block level.

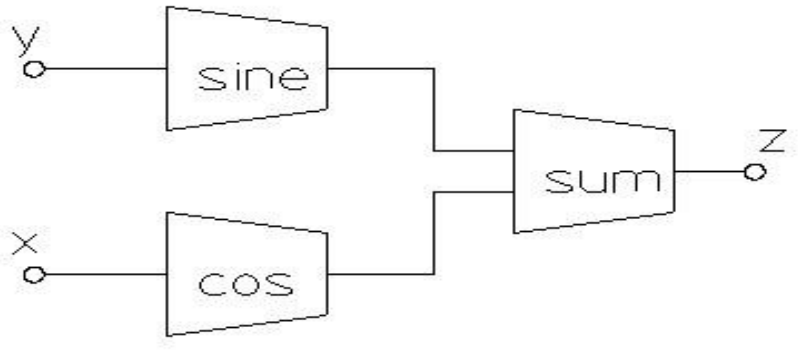


Fig 5.1: Block level diagram of the total circuit

The Fig. 5.1 shows the block level diagram of the circuit. The blocks, labeled as "*sine*" and "*cos*", are denoting the sine and cosine amplifier as shown in Fig. 4.4 and Fig. 4.5 respectively. The block, labeled as "*sum*" representing a usual summing amplifier.

So from the circuit it is clear one genuine source of error is the Offset of OPAMPs. Apart from that, in the circuits of sine and cosine amplifier one key element which is used is digital potentiometers which are assumed to have uniform steps. So non-uniformity in the steps would definitely add some errors.

Also even if everything works perfectly fine, the sine and cosine amplifier, which are designed, are only expected to give only an approximate pattern of sine and cosine in the 1st quadrant. Fig. 4.3 suggests the pattern which is obtained is by principle 2% off from the original. So this error would also add up to the final result.

Therefore the significant sources of error which are decided are the following

a) Offset of OPAMPs
b) Non-uniform step size of digital potentiometers
c) Theoretical error in designing the sine and cosine amplifier

5.1 OFFSET OF OPAMPS

For any commercial OPAMPs available in the market some offset will always be there. In fact the offset in OPAMP is a very commonly encountered problem. Many compensation techniques are also there to overcome the detriments of these offsets. However in the following discussions it is briefly described how the offsets in the OPAMPs, used in the circuit, would affect the final result.

Now in the circuit, let us assume the OPAMP used in realizing the summing amplifier are free from any offset. Anyway even if there indeed is any offset in the summing OPAMP then that would directly get added up to the output.

The sine and cosine amplifiers are also made up of OPAMPs. Now the effect of offset, associated with them, will not appear so directly in the output. So the analysis and effects of it on the output is presented as the following.

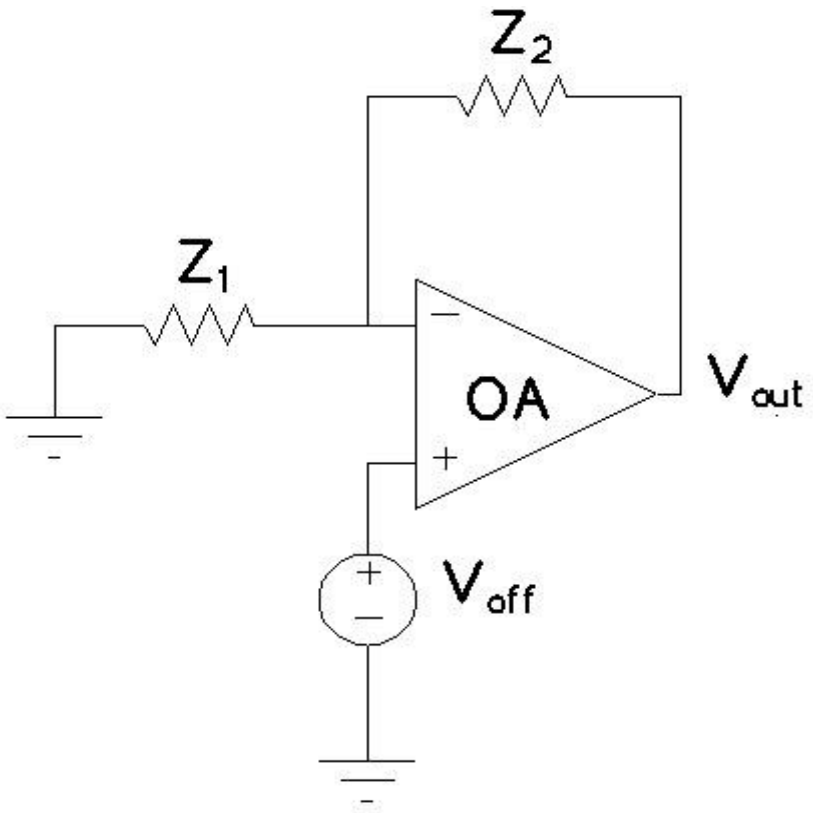


Fig 5.2: OPAMP in negative feedback configuration, modeled along with its offset voltage.

From Fig. 5.2 the output can be written as

$$V_{out} = \left(1 + \frac{Z_2}{Z_1}\right) V_{off} \tag{5.1}$$

Extending the same logic, by taking the offset into account, the total output of the sine amplifier can be written as the following.

$$V_{sin} = \left(1 + \frac{Z_{sin}(j)}{R_i}\right) V_{off_{sin}} - \frac{Z_{sin}(j)}{R_i} y \tag{5.2}$$

Where $Z_{sin}(j)$ denotes the total resistance in the feedback path of the sine amplifier in j^{th} step. Therefore rearranging the equation (5.2) a little bit, one can write

$$V_{sin} = V_{off_{sin}} + \left(V_{off_{sin}} - y\right)\frac{Z_{sin}(j)}{R_i} \tag{5.3}$$

Similarly for the cosine amplifier as well the output can be written as following equation.

$$V_{cos} = \left(1 + \frac{Z_{cos}(j)}{R_i}\right)V_{off_{cos}} - \frac{Z_{cos}(j)}{R_i}x \tag{5.4}$$

Where $Z_{cos}(j)$ denotes the total resistance in the feedback path of the cosine amplifier in j^{th} step. Therefore rearranging the equation (5.4) a little bit, one can write

$$V_{cos} = V_{off_{cos}} + \left(V_{off_{cos}} - x\right)\frac{Z_{cos}(j)}{R_i} \tag{5.5}$$

So equation (5.3) and (5.5) clearly depicts the output of sine and cosine amplifier respectively if the OPAMPs used in building those amplifiers suffer from offset.

Now therefore from the Fig. 5.1 it is conclusive that the voltage at the node "z" is basically the sum of the voltage at the output of sine and cosine amplifier. Therefore from equation (5.3) and (5.5), "z" can also be written as the following

$$z = -(V_{sin} + V_{cos}) \tag{5.6}$$

The negative sign comes due to the inversion of the summing amplifier. Therefore putting the expressions of V_{sin} and V_{cos} from the equation (5.3) and (5.5) in equation (5.6) one can easily obtain

$$z = -\left(V_{off_{sin}} + V_{off_{cos}}\right) + \left\{\left(y - V_{off_{sin}}\right)\frac{Z_{sin}(j)}{R_i} + \left(x - V_{off_{cos}}\right)\frac{Z_{cos}(j)}{R_i}\right\} \tag{5.7}$$

Now the final output is the maximum value of "z", as discussed in chapter 2, for "j" being varied from one to hundred. So with that token the final output would be written as

$$V_{SQRSS} = -\left(V_{off_{sin}} + V_{off_{cos}}\right) + \sqrt{\left(y - V_{off_{sin}}\right)^2 + \left(x - V_{off_{cos}}\right)^2} \quad (5.8)$$

So from equation (5.8) it is easily conclusive that if there is some positive/negative offset in the OPAMPs used to build the sine and cosine amplifier, then those are going to reduce or increase the output from its desired value in a manner described in equation (5.8).

5.2 NON UNIFORM STEPS OF DIGITAL POTENTIOMETERS

Two digital potentiometers are used in each of the sine and cosine amplifiers. Those are used as variable resistors. These variable resistors require one clock signal and another increment signal. If the increment signal is high then the potentiometers offer resistance which increases with every clock cycle and if this signal is low then it reduces its resistance with every clock cycle.

These potentiometers have got limits upon the minimum and maximum resistance it can provide. If the increment signal is still low even when the potentiometer has already reached its minimum value of resistance then it remains in minimum value itself and similarly if the increment is still high even when the potentiometer has reached the maximum value of resistance then it remains in its maximum value itself.

Now one very important aspect of these potentiometers is that they are supposed to increase or decrease their resistance in uniform steps. However due to many reasons like process limitations these potentiometers fail to achieve uniform steps. In reality these steps happen to be deviating from being uniform. Now of course these deviations are most of the time found to be within tolerable limit. Thus this section particularly focuses on the effects of this non uniformity in the step size of these potentiometers upon the output.

So for both sine and cosine amplifier the gain can be written as the following

$$A(j) = \left[\frac{R_1(j)R_2(j)(r_1+r_2)+r_1r_2R_1(j)}{R_2(j)(r_1+r_2)+r_1r_2+R_1(j)(R_2(j)+r_2)}\right]/R_i \qquad (5.9)$$

The equation (5.9) denotes the gain offered by the sine and cosine amplifier at j^{th} step. Thus with a little bit of more lucidity equation (5.9) can also be elaborated as follows.

$$A = \left[\frac{jS_1(R_{2_{max}}-jS_2)(r_1+r_2)+r_1r_2jS_1}{(R_{2_{max}}-jS_2)(r_1+r_2)+r_1r_2+jS_1(R_{2_{max}}-jS_2+r_2)}\right]/R_i \qquad (5.10)$$

Now the non-uniformity can happen in any of the step. Also it can occur in more than one step. Now the actual expression of the gain taking this non-uniformity into account would be too complex. Thus in order to avoid these difficulties one little assumption is made.

It is assumed that the non-uniformities are negligible compared to the step size of the variable potentiometers. With that argument it is also assumed that the total deviations, which all the non-uniformities would contribute cumulatively is effectively same as the sum of all the deviations which these non-uniformities would contribute individually. The analysis is carried out separately for R_1 and R_2.

- **Non Uniformity in R_1**: So to start it is considered that R_1 contains a small non-uniformity, Δr, at m^{th} step. Therefore the gain expression of the sine amplifier for j^{th} step can be written as the following equation.

$$A_{sin} = \left[\frac{(mS_1+\Delta r)(R_{2_{max}}-mS_2)(r_1+r_2)+r_1r_2(mS_1+\Delta r)}{(R_{2_{max}}-mS_2)(r_1+r_2)+r_1r_2+(mS_1+\Delta r)(R_{2_{max}}-mS_2+r_2)}\right]/R_i \qquad (5.11)$$

  Now considering the values which are chosen for the corresponding components and by applying a little bit of wise judgments, the equation (5.11) can be rewritten as the following.

$$A_{sin} \approx A_{sin_{exp}} + \frac{\Delta r}{R_i} \frac{R_{2_{max}} + r_1 \parallel r_2 - mS_2}{R_{2_{max}} - mS_2 + r_1 \parallel r_2 + mS_1 \frac{R_{2_{max}} - mS_2 + r_2}{r_1 + r_2}} \quad (5.12)$$

So the equation (5.12) gives a deep idea about how the gain of the sine amplifier would vary from its expected value if there is any non-uniformity. So from it one can easily notice that its effect is profound when j is small than what it is when j is large. Also this can be explained intuitively because when j is small the feedback resistance of the sine amplifier is effectively R_1 and the resistance offered by R_1 for these small values of j is also very less.

- **Non-Uniformity in R_2:** To analyze the effects of non-uniformity in R_2 a similar approach is taken. And to start here also it is considered that R_2 contains a small non-uniformity, Δr, at m^{th} step. Therefore the expression of the gain of sine amplifier can be written as the following.

$$A_{sin} = \left[\frac{mS_1(R_{2_{max}} - mS_2 + \Delta r)(r_1 + r_2) + r_1 r_2 mS_1}{(R_{2_{max}} - mS_2 + \Delta r)(r_1 + r_2) + r_1 r_2 + mS_1(R_{2_{max}} - mS_2 + \Delta r + r_2)}\right] / R_i \quad (5.13)$$

Similarly like R_1, considering the values which are chosen for the corresponding components and by applying a little bit of wise judgments, the equation (5.13) can be rewritten as the following

$$A_{sin} \approx A_{sin_{exp}} + \frac{\Delta r}{R_i} \frac{mS_1}{R_{2_{max}} - mS_2 + r_1 \parallel r_2 + mS_1 \frac{R_{2_{max}} - mS_2 + r_2}{r_1 + r_2}} \quad (5.14)$$

From equation (5.14) one can say for small values of m the effect of non-uniformity on the gain of sine amplifier is negligible. Also for high values of m as well it is not so severe because the deviation in gain from the expected value turns out to be only 0.1 times the Δr. So overall regarding non-uniformity in steps more care should be taken in choosing R_1 than R_2. But the intensity of the effect of this non-uniformity in the final output depends upon the inputs. If the inputs are given in such a way that z is maximized at the neighborhood of non-uniform steps then the result will be more erroneous compared to the case when z maximization occur not at the neighborhood of any non-uniformity containing step.

5.3 GAIN ERROR IN SINE AND COSINE AMPLIFIER

Talking about error, one inevitable source of error in the circuit discussed in this thesis is the gain error in sine and cosine amplifier. Ideally these amplifiers are expected to have a gain which varies with time like the sinusoid in 1st quadrant. But in reality the amplifier which is shown in this thesis has a gain which approximately varies like sinusoid. This error reflects itself directly in the output. From Fig. 4.3 one could verify the gain error in the sine and cosine amplifier is less than 2% till 87°. So considering the worst case one can write

$$z = x\cos\alpha + y\sin\alpha + 0.02 \times (x + y) \tag{5.15}$$

So doing the envelope detection the final output will be obtained as

$$z = \sqrt{x^2 + y^2} + 0.02 \times (x + y) \tag{5.16}$$

So as the equation (5.16) suggests larger the absolute value of inputs greater will be the error.

CHAPTER 6

EXPERIMENTAL SETUP & RESULTS

6.1 METHODOLOGY

The methodology followed to carry out the experiment and acquire the results is pretty simple. The prototype is built on the bread board that comes with NI ELVIS II training kit. The supplies are given from that kit only. After the experiments are carried out the data are viewed first in the PC through the LAB-VIEW interface.

6.1.1 NI ELVIS II

The National Instruments Educational Laboratory Virtual Instrumentation Suite II (NI ELVIS II) is a LAB-VIEW and computer based design and prototyping environment. NI ELVIS II consists of accustom-designed bench top workstation, a prototyping board, a multifunction data acquisition device, and LAB-VIEW based virtual instruments [9]. This combination provides an integrated, modular instrumentation platform that has comparable functionality to the DMM, Oscilloscope, Function Generator, and power Supply found on the laboratory workbench.

The NI ELVIS II Workstation can be controlled either vi manual dials on the stations front or through software virtual instruments. The NI ELVIS II software suite contains virtual instruments that enable the NI ELVIS II workstation to perform functions similar to a number of much more expensive instruments.

One can use NI ELVIS II in engineering, physical sciences, and biological sciences laboratories. The suite offers full testing, measurement, and data logging capabilities.

The following figure shows the snapshot of NI ELVIS II board.

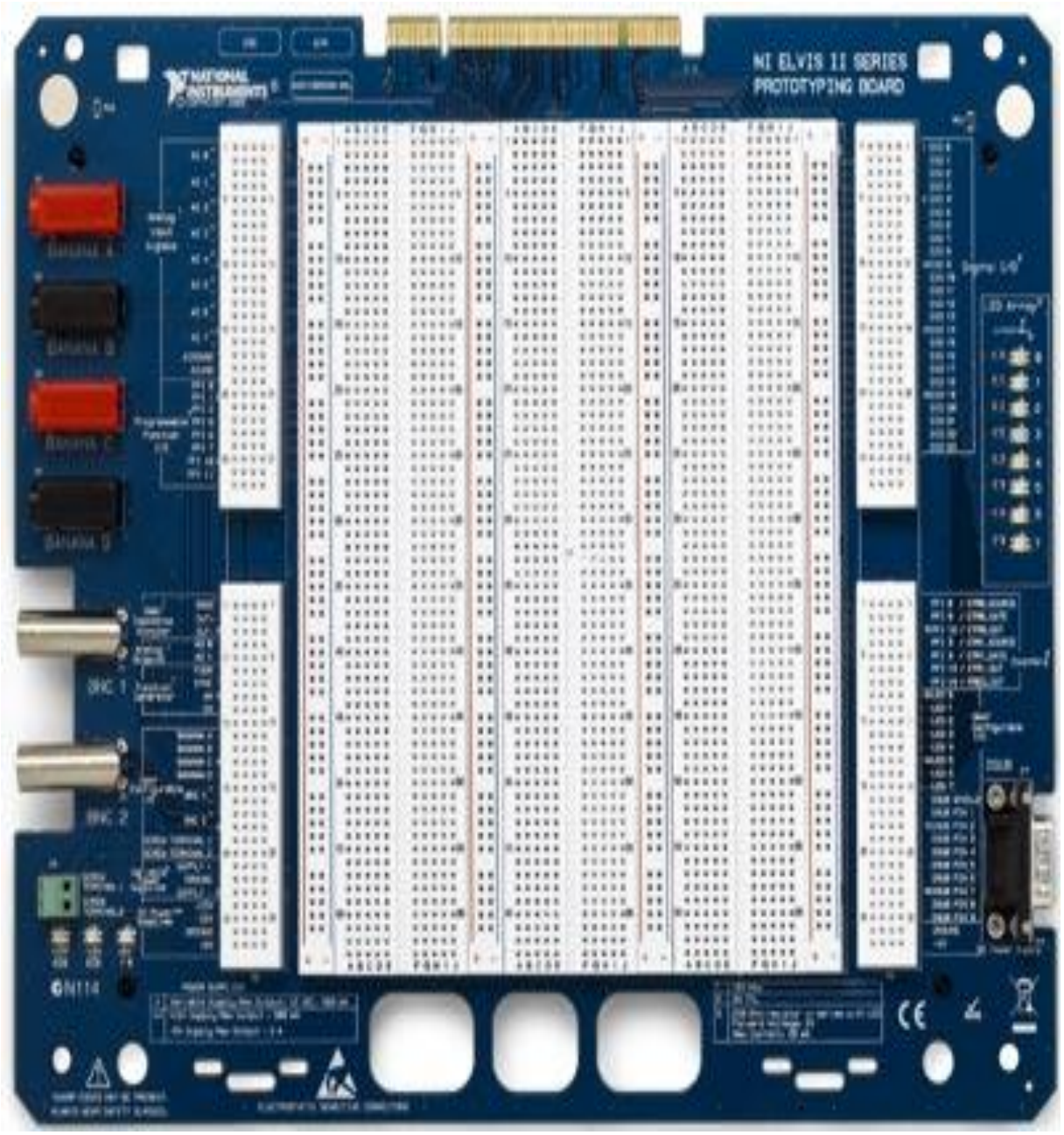


Fig 6.1: NI ELVIS II hardware [10].

Fig 6.2: NI ELVIS II Soft Panel

The environment consists of the following two components.

1. Bench top hardware workspace for building circuits, shown in Figure 5.5.

2. NI Elvis software interface consisting of twelve soft front panels (SFP) instrument, Figure 5.6.

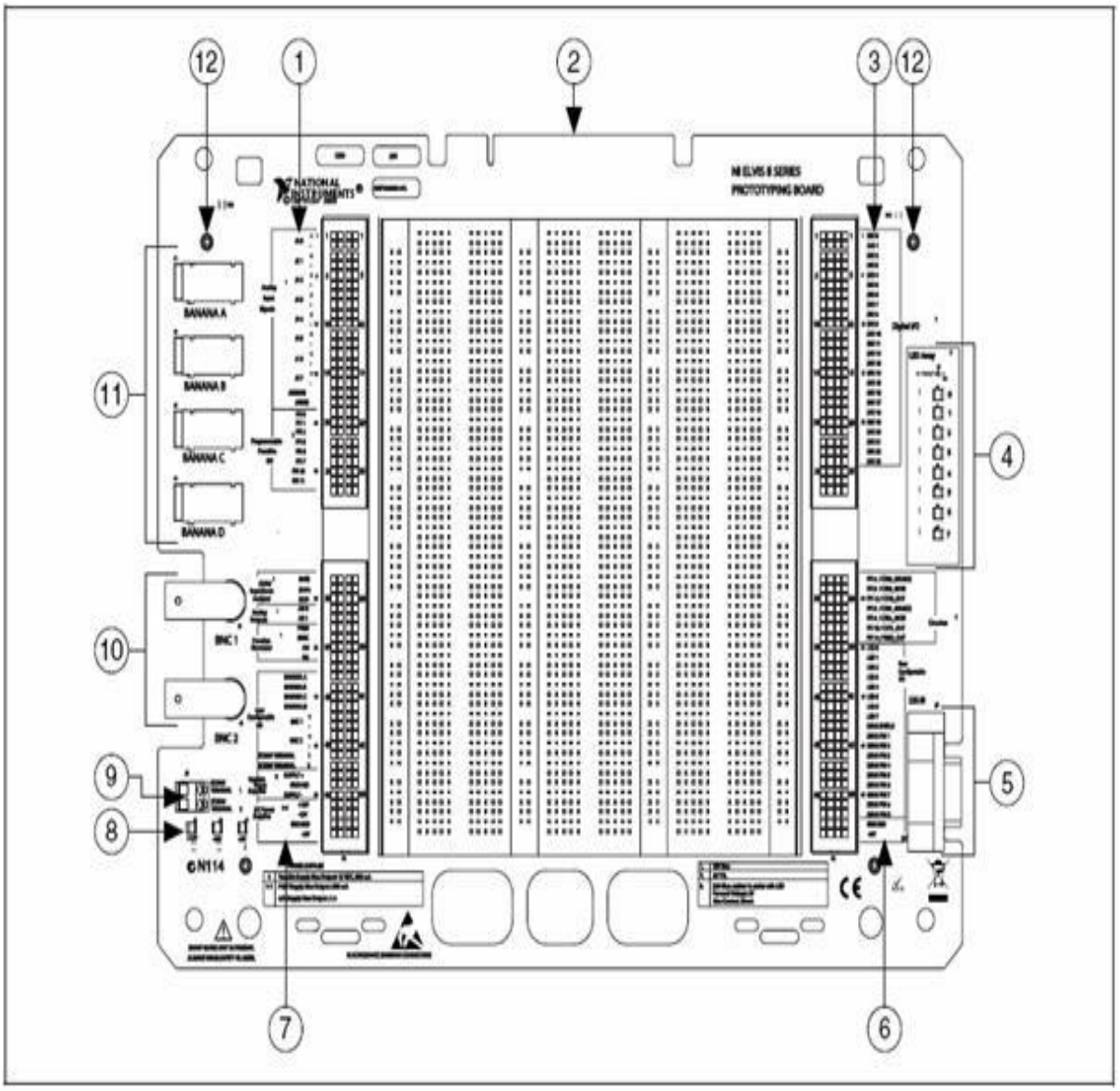
The soft panels are:

- Digital Multi-meter (DMM)
- Oscilloscope (Scope)
- Function Generator (FGEN)
- Variable Power Supply (VPS)
- Bode Analyzer
- Dynamic Signal Analyzer (DSA)
- Arbitrary Waveform Generator (ARB)
- Digital Reader (Dig In)
- Digital Writer (Dig Out)
- Impedance Analyzer
- Two –wire Current-Voltage Analyzer
- Three –wire Current-Voltage Analyzer

6.1.2 NI ELVIS II HARDWARE

NI ELVIS II hardware contains Bench top Workstation and Series Prototyping Board. A work station has a top panel, a Rear panel and a bottom panel. Series prototyping board is fixed on the top panel. The workstation control panel provides easy-to-operate knobs for the variable power supplies and function generator, as given in Fig. 6.1, and offers convenient connectivity and functionality in the form of BNC

and banana-style connectors, shown in Fig 6.1, to the function generator, scope, and DMM instruments at the left side of the bench top.



1 AI and PFI Signal Rows
2 Benchtop Workstation Interface Connector
3 DIO Signal Rows
4 User Configurable LEDs
5 User Configurable D-SUB Connector
6 Counter/Timer, User-Configurable I/O, and DC Power Supply Signal Rows
7 DMM, AO, Function Generator, User-Configurable I/O, Variable Power Supplies, and DC Power Supplies Signal Rows
8 DC Power Supply Indicators
9 User-Configurable Screw Terminals
10 User Configurable BNC Connectors
11 User Configurable Banana Jack Connectors
12 Screw Positions for Locking

Fig 6.3: Series Prototyping Board

6.1.3 NI ELVIS SERIES PROTOTYPING BOARD

This section describes the NI ELVIS II Series Prototyping Board and how to use it to connect circuits to NI ELVIS II. The NI ELVIS II Series Prototyping Board is connected to the bench top workstation. The prototyping board provides an area for building electronic circuitry and has the necessary connections to access signals for common applications. Figure 4.4 shows the prototyping board connected on a bench top work station with a brief description. You can use multiple prototyping boards interchangeably with the NI ELVIS II Bench top workstation, removing it from the bench top workstation. You can use the prototyping board connector to install a custom prototype boards you develop. This connector is mechanically the same as a standard PCI connector.

A diagram of the prototyping board is shown in the Fig. 6.2.

6.2 BUILDING THE PROTOTYPE

The prototype of the scheme presented in this thesis is built on NI ELVIS II trainer kit. The circuit mainly consists of three blocks which are as following

a) Sine Amplifier
b) Cosine Amplifier
c) Summing Amplifier

Now all the three above mentioned amplifiers are built using OPAMP in negative feedback inverting configuration. The IC TL084, manufactured by M/s Texas Instruments is used for realizing all the OPAMPs. This IC is particularly chosen because of its extremely low input current leakage. It is powered by $\pm 15\ V$ supply, obtained from the NI ELVIS II trainer kit.

The sine and cosine amplifier produced inverted output, as the OPAMP is in inverting negative feedback configuration. The summing amplifier added the two waveforms and then inverted once again because of the same reason. Thus there was not any need of separate sign inverter.

The sine and cosine amplifier basically have the same circuit. Only the increment signals to the digital potentiometers were different. As mentioned in the chapter 4 the IC X9C103, manufactured by M/s Intersil, was used as R_1 and the IC X9C503, from the same manufacturing house, was used as R_2 in both sine and cosine amplifier. The circuit is tested by giving these digital potentiometers a clock signal of frequency $10kHz$. For the increment signal a separate function generator is used to generate square wave of frequency $50Hz$. The R_1 of sine amplifier and R_2 were given the signal directly from the function generator. For the rest two potentiometers the signals were given after passing the function generator signal through an inverter. The potentiometers are all powered by $+5V$ supply and ground, taken from the NI ELVIS II trainer kit.

The inputs to the circuit are given from the variable power supply block provided by the NI ELVIS II trainer kit. The positive supply is directly tied to the sine amplifier and the voltage from the negative supply is first inverted by another inverting amplifier of gain -1 and then tied to the cosine amplifier. The outputs of sine and cosine amplifier are viewed in Scope, provided in NI ELVIS software panel, and the same outputs are sampled and acquired in Lab-VIEW and thereafter those are plotted using the software MATLAB from M/s Mathworks.

The output of the summing amplifier is also acquired in the same way by the LAB-VIEW for different combinations of inputs and thereafter the maximum value is chosen as the final result. The Table 6.1 shows the outputs obtained for different combinations of inputs. Now as TL084 can give a maximum output voltage of $4V$ staying within its linear range thus $4V$ is chosen as full scale output. Thus all the relative percentage errors are measured with respect to this full scale output only.

X	Y	$\sqrt{X^2 + Y^2}$	Measured	% Error
0.4	0.4	0.565	0.535	0.750
0.4	0.6	0.721	0.696	0.625
0.4	0.8	0.894	0.889	0.125
0.4	1	1.077	1.073	0.100
0.4	2	2.04	2.070	0.750
0.4	3	3.03	3.070	1
0.6	0.6	0.848	0.810	0.950
0.6	0.8	1	0.967	0.825
0.6	1	1.166	1.140	0.650
0.6	2	2.088	2.120	0.800
0.6	3	3.06	3.100	1
0.8	0.8	1.131	1.098	0.825
0.8	1	1.280	1.240	1
0.8	2	2.154	2.177	0.575
0.8	3	3.105	3.150	1.125
1	1	1.414	1.375	0.975
1	2	2.236	2.260	0.600
1	3	3.162	3.220	1.450
2	2	2.828	2.793	0.875
2	3	3.605	3.587	0.450

Table 6.1 Final Results obtained for different sets of Input Voltage.

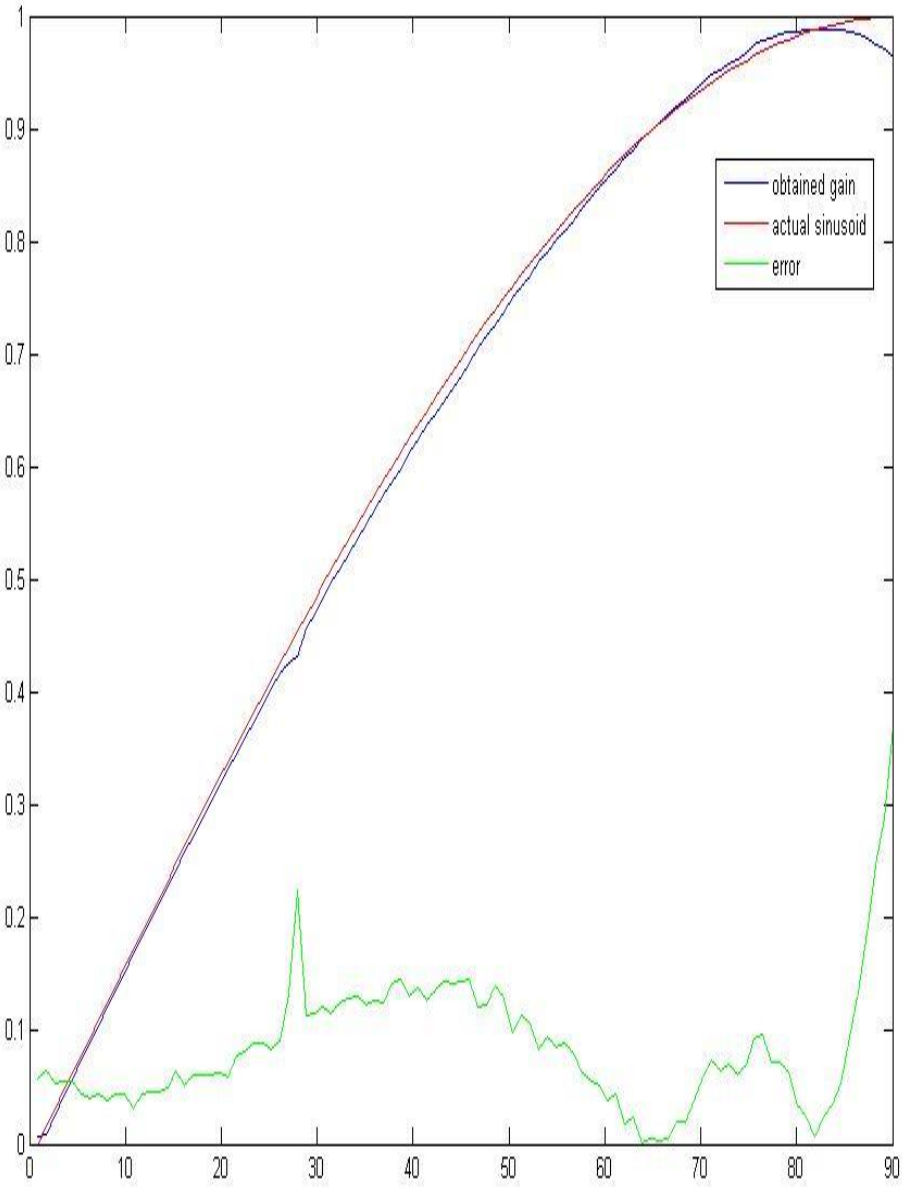


Fig 6.4: Gain characteristics obtained from the prototype sine amplifier is shown in blue. The red plot shows the actual sinusoid and the green plot shows the relative percentage error being divided by 10. The horizontal axis denotes steps, being converted to equivalent angle.

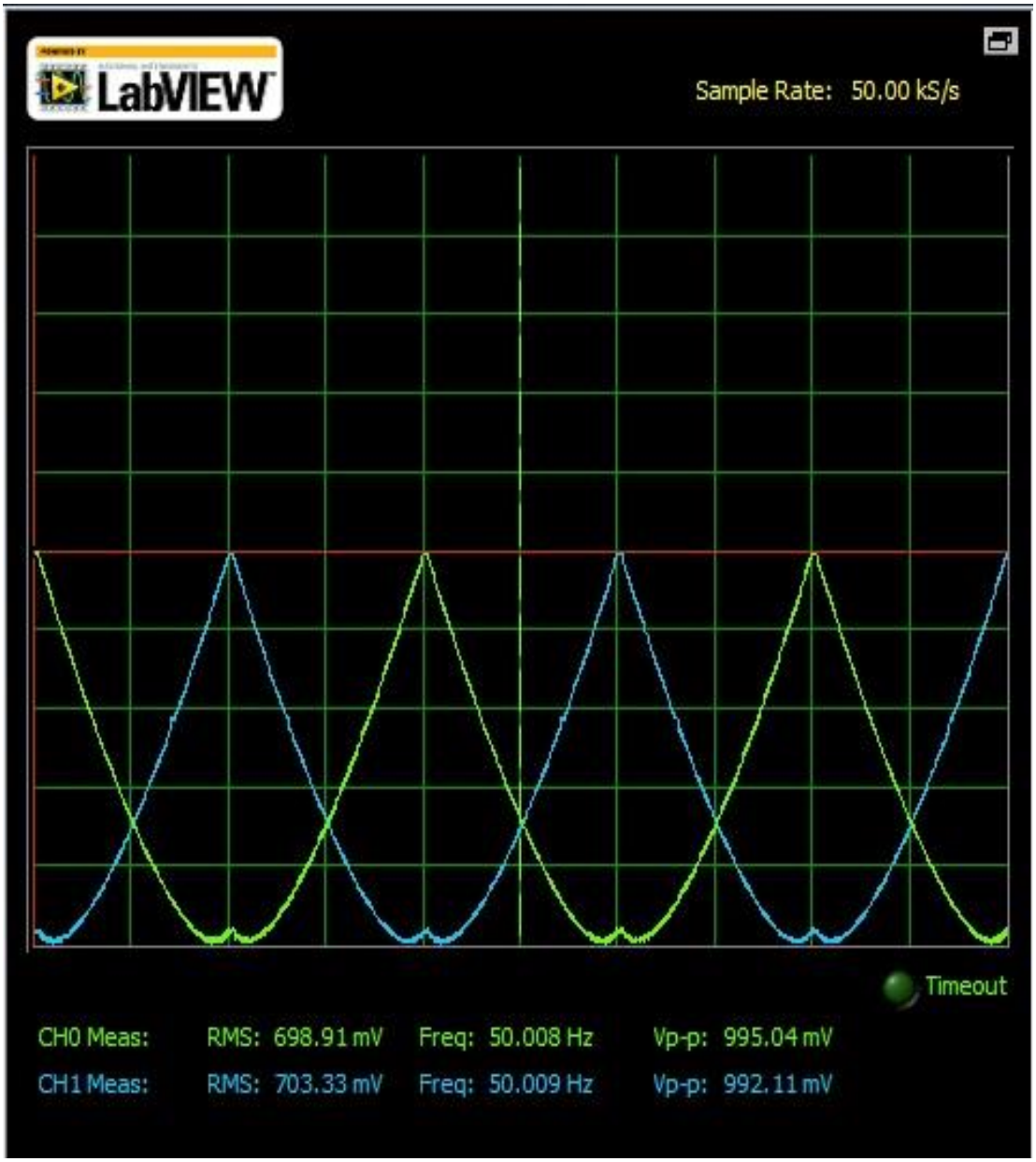


Fig 6.5: Gain characteristics of sine and cosine amplifier as viewed in scope. The Channel 0 shows the characteristic of sine amplifier and the Channel 1 shows the gain characteristic of cosine amplifier.

CHAPTER 7

CONCLUSION AND FUTURE WORK

7.1 CONCLUSION

A design of an amplifier is shown whose gain varies in a sinusoidal fashion in the 1st quadrant. The design is performed using OPAMP, fixed value resistors and two digitally variable resistors. The same amplifier is then used to generate the square root of the sum of two squares. The implementation is very simple and does not require any expensive and less accurate hardware like multipliers. The prototype has been built and tested. The accuracy can be improved by using variable resistors with more number of steps.

7.2 FUTURE WORK

There are few improvements which can be done for the work described in this thesis. Those are listed as the following

- The envelope detecting circuit is not included physically in the prototype. That can be done as a future work on this project.
- The design of sine/cosine amplifier which is shown in the circuit gives a maximum relative error of 2% up to 87°. However for the purpose of the work presented in this thesis, if one of the inputs is at least ten times bigger than other, then bigger input will give a good approximation of the final result with less than 1% error. Now if one input is ten times bigger than the other then it corresponds to 84°. So in such cases directly passing the bigger input as output would give a more accurate result than passing it through sine amplifier. So this provision can be included in the scheme as future work.
- A more detailed analysis may help people to figure out a more deterministic design procedure for the sine/cosine amplifier with the topology presented in this thesis.

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