Input Front End Current Source Rectifier Control for PWM Current Source Inverter Fed Induction Motor Drive for Sub-Sea Mining Application

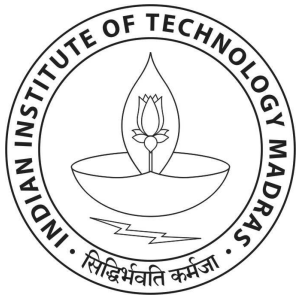
A Project Report

submitted by

PRATAP KUNATHI

in partial fulfilment of the requirements
for the award of the degree of

MASTER OF TECHNOLOGY



DEPARTMENT OF ELECTRICAL ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY MADRAS.

MAY 2015

THESIS CERTIFICATE

This is to certify that the thesis titled **Input Front End Current Source Rectifier Control for PWM Current Source Inverter Fed Induction Motor Drive for Sub-Sea Mining Application**, submitted by **PRATAP KUNATHI**, to the Indian Institute of Technology, Madras, for the award of the degree of **Master of Technology**, is a bona fide record of the project work done by him under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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ABSTRACT

KEYWORDS: PWM CSR, PWM CSI

A PWM Current Source Rectifier(CSR) acts as a front end converter for PWM Current Source Inverter(CSI) fed drives. CSI is chosen to drive induction motor for sub-sea mining application. The ocean mining sites are usually located about 6 to 7 km from ocean's surface. National Institute of Ocean Technology(NIOT) has been working on this sub sea mining, where a crawler based mining machine collects the nodules and pumps to ship which is located on sea surface. For this mining application it is intended to use 250 KW induction motor. Long transmission cables are used to give the supply as the machine is located deep under sea For this reason CSI is chosen over VSI, also CSI can inject sinusoidal currents and no additional filters are required. For smooth operation of drive a ripple free DC link current is required. A PWM CSR can give a smooth and ripple free DC link current to CSI fed induction motor drive.

In this project a PWM CSR is developed and required control technique is established in *TMS320F28335* digital platform. A new control technique has been proposed and validated with simulations and hardware results. The main objective of the proposed control method is instantaneous DC link current control. It is also ensured sinusoidal grid currents, reactive VAR compensation from the CSI while maintaining the DC link current . The rectifier can draw unity, leading and lagging power factor. The proposed control method is derived based on the power balance at input and output of the PWM CSR. Space vector Modulation technique is adopted to deliver the PWM current from the rectifier.

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ABBREVIATIONS

CSI	Current Source Inverter
VSI	Voltage Source Inverter
PWM	Pulse Width Modulation
SCR	Silicon Controlled Rectifier
CSR	Current Source Rectifier
IGCT	Intergrated Gate Commutated Thyristor
IGBT	Insulated Gate Bipolar Transistor
THD	Total Harmonic Distortion
SHE	Selective Harmonic Elimination
SVM	Space Vector Modulation
KVL	Kirchhoff's Voltage Law
PLL	Phase Locked Loop
SPWM	Sinusoidal Pulse Width Modulation
SVPWM	Space Vector Pulse Width Modulation
PC	Printed Circuit Board
DSC	Digital Signal Controller
DSP	Digital Signal Processor
CCS	Code Composer Studio
ADC	Analog to Digital Converter
I2C	Inter Integrated Circuits
DAC	Digital to Analog Converter
RPS	Regulated Power Supply
USB	Universal Serial Bus

NOTATIONS

L_d	DC Choke inductance
L_s	AC side inductance
V_{rec}	Rectifier voltage
I_{dc}	DC link current
$\vec{V^*_{sPI}}$	Power Invariant Voltage Space Vector
V_{sdPI}	Power Invariant direct axis voltage
V_{sqPI}	Power Invariant quadrature axis voltage
I^*_{sPI}	Power Invariant Current Space Vector
I_{sdPI}	Power Invariant direct axis current
I_{sqPI}	Power Invariant quadrature axis current
V_{ph}	Per Phase grid Voltage
V_{max}	Peak Value of per Phase grid voltage
I_{ph}	per Phase line current
I_{max}	peak value of per Phase line curent
V_{sd}	Power Variant direct axis voltage
I_{sd}	Power Variant direct axis current
V_i	Inverter Voltage
K_{pi}	Proportional constant of PI controller
τ_{pi}	time constant of PI controller
$V_{s\alpha}$	α axis voltage
$V_{s\beta}$	β axis voltage
I^*_{sd}	Reference direct axis current
I^*_{sq}	Reference quadrature axis current
I^*_s	Current Space Vector

CHAPTER 1

Introduction

After advent of power semiconductor devices, new control strategies were introduced for speed control of electrical machines. Among all the electric drives, induction motor drive is most widely used. It has several applications in both domestic and industrial applications. Sub-sea mining application is one among them. It is a relatively new mineral retrieval process that takes place on the ocean floor. Ocean mining sites are usually around large areas of polymetallic nodules or active and extinct hydrothermal vents at about 6 to 7 Km below the ocean's surface. The vents create sulfide deposits, which contain valuable metals such as silver, gold, copper, manganese, cobalt, and zinc. The deposits are mined using either hydraulic pumps or bucket systems that take ore to the surface to be processed.A crawler based mining machine collects, crushes and pumps nodules to the mother ship using a positive displacement pump through a flexible riser system.

It is expected that multiple mining machines will cover the mining field during large scale commercial mining operations. With this perspective, the integrated mining system is under development for deep-sea mining of polymetallic nodules. It is intended to use a 250 KW induction motor drive from pumping out the nodules from the seabed. Induction machine with pump will be placed at the seabed [1]. The machine will be driven from the ship with electric drives which is located on the sea surface through long transmission cables. At 250 KW power range generally low voltage(440/690 V) drive is preferred in the industry. But in this application, medium voltage(3.3/6.6 KV) is decided to use for reducing the current drawn by the motor. This lead to reduce in weight and cost of the power cables. A PWM CSI fed induction motor drive is chosen for the present study.

1.1 PWM Current Source Inverter

The induction motor can be fed through Voltage Source Inverter(VSI) or Current source Inverter(CSI). Today Medium Voltage drives with Voltage Source Inverter(VSI) based technology is commonly used. But considering the deep-sea mining application Current Source Inverter(CSI) is chosen because it can inject sinusoidal currents into the machine and no additional filters are required. As the machine is fed with long transmission cables line inductance drop will be there in case of VSI fed drives. They are required to be compensated. But for a CSI fed drive the inductance drop problem does not exist. VSI fed drives lead to motor over voltages. Apart from these operational advantages CSI has various advantages over VSI. Some of them are inbuilt shoot-through protection, efficiency, superior bidirectional power flow. Also the high $\frac{dv}{dt}$ problems associated with VSI does not exist in CSI[2].

1.2 Power Structure

A two level CSI inverter bridge consists of 6 switches. There are three inverter legs supplying controlled current to the three phases of the motor. Similarly a PWM CSI rectifier has 3 legs and draws power from the 3-phase voltage source. Each leg consists of two switches. For appropriate control of PWM CSI a controlled current source is required. Input side PWM rectifier develops the required controlled current source for the CSI. It can be realized with SCR or PWM based rectifier with current control and a DC link inductance in series. For better power quality at CSI it is desired to have a ripple free current source. Such kind of ripple free and smoother current is given by PWM based rectifier compared with SCR based rectifier. The power schematic of inverter and rectifier is shown in Fig.1.1. It shows the complete power structure of the CSI-fed induction motor drive. It consists of two converters. One is connected to grid(also called as front end converter) and the other one at motor side. The grid side converter is PWM Current Source Rectifier(CSR) and motor side converter is PWM Current Source Inverter(CSI). 3-phase capacitors are connected on both grid side and motor side to assist the commutation of switching devices and to filter out the current harmonics. The DC choke inductor(L_d) makes the DC current smooth and constant. The value of the inductance can be substantially reduced if PWM rectifier is used instead of a line commutated

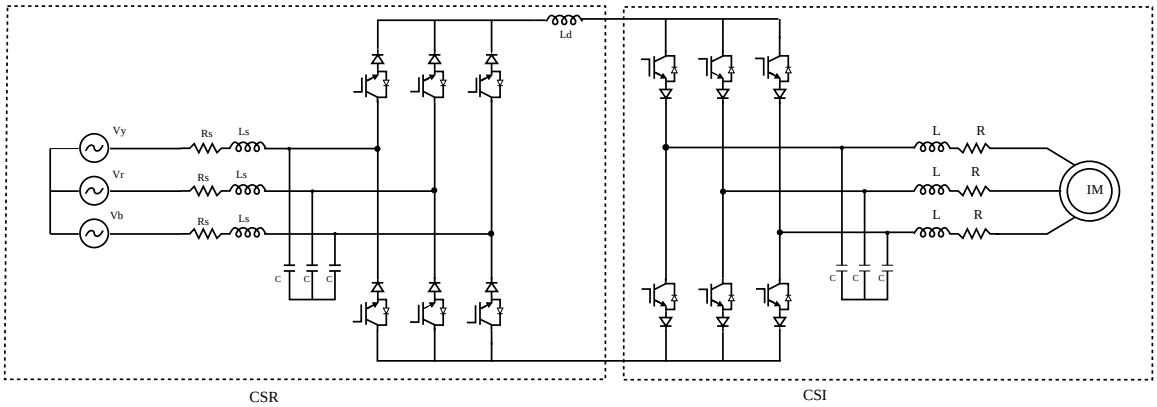

Figure 1.1: Power Structure of CSI-fed IM drive

SCR rectifier. In actual 250 KW drive, Integrated Gate Commutated Thyristor(IGCT) is the preferred device. Several manufacturers provide IGCT devices with ratings up to 6 KA. The IGCT device is most preferred choice for medium voltage drives because of its low switching losses and snubber less operation. Symmetric IGCT's are normally used over Asymmetric type for Current Source converters because of its reverse blocking capability**[2]**.

Design and implementation of hardware is experimentally carried out for a prototype of 0.75 KW(1 hp) induction motor. Since the prototype is for low rated machine the IGCT devices are realized by IGBT with series diode. The IGBT is not capable of blocking reverse voltage. Therefore a diode is connected in series to IGBT. The series diode makes the current to flow only in one direction. The entire CSI- fed induction motor drive is split into two parts, front end part and motor end part. The front end part i.e. PWM CSR is studied and tested using a resistive load and Motor end part is studied and tested using 3-ϕ thyristor bridge rectifier and inductor in series realized as DC current source. In this thesis only **input side PWM CSI rectifier** simulation and experimental verification is carried out.

1.3 PWM Current source Rectifier

Fig.1.2 shows the PWM Current Source Rectifier(CSR) with resistive load, The switches used in the circuit is IGBT with series diode. The series diode ensures the unidirectional current flow.The line inductance Ls on the AC side of the rectifier represents the total inductance between utility supply and rectifier including the equivalent inductance of the supply and leakage inductance of the transformer. The CSR normally requires a

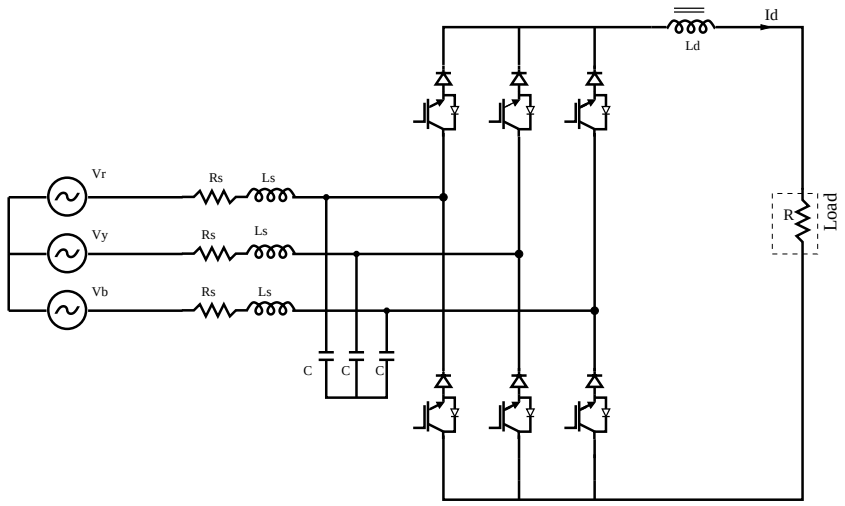

Figure 1.2: PWM Current Source Rectifier

three phase filter capacitors at its input. The capacitors function is to assist the commutation of switching devices and filters out harmonic currents. The DC side of the rectifier is connected to inductor L_d which is required to smooth the DC current and a resistor R is connected as load.

1.4 Organisation of Thesis

- **Chapter 2:** describes the modelling and proposed control method for PWM CSR. A new control method is proposed for PWM CSR.

- **Chapter 3** deals with the hardware organization. It explains the hardware design aspects for the PWM CSI rectifier.

- **Chapter 4** explains the hardware results and experimental verifications. All experimental results from actual hardware implementation are explained.

- **Chapter 5** concludes the report with future scope of work.

CHAPTER 2

Modelling and analysis of PWM Current Source Rectifier

2.1 Introduction

PWM CSI rectifier control and its design are the objectives of the thesis.The basic power structure of the PWM CSI based rectifier is discussed in *chapter 1*. In this chapter mathematical modelling of the system, description of the control system and its design are elaborated. The control system of PWM CSR has the following objectives:

- **Control of DC link current:** In order to attain ripple free torque by the induction motor it needs harmonic free, smooth and controlled DC link current. A Line commutated SCR rectifier contains lower order harmonics. If such kind of system is connected to an induction machine low order harmonics will appear in the line current. As the line currents have lower order harmonics they will cause unwanted heating of the machine and torque pulsation in the machine. Therefore the proposed control technique will try to ensure low frequency ripple free DC link current.

- **Sinusoidal grid current:** Now a days grid code for every country is becoming very stringent. Though the intended sub-sea drive is not connected to grid but improving the power quality of input current improves the total efficiency of the system. As per IEEE 519 standards the input current THD should be less than 5%.

- **Power factor correction and reactive power compensation:** Control system of the rectifier should be such a way that it should draw unity power factor from the grid irrespective of load connected. Also it should be able to draw both leading and lagging power factor current based on the reactive power requirement.

- **High dynamic performance.** In a CSI based induction motor drive, the speed control is implemented by either varying the DC link current and keeping modulation index fixed or by varying modulation index and fixing the DC link current. In case of speed control by varying DC link current the rectifier should quickly respond to the sudden change in DC link current requirement by the motor. Also in case of constant DC link current and varying modulation index the sudden change of inverter voltage may cause dip in the DC link current. PWM CSI rectifier should quickly respond and be able to maintain constant DC link current. It implies that the rectifier should have a better dynamic performance. A PWM CSI rectifier shows better dynamic performance than SCR based rectifier. Therefore by using PWM rectifier the dynamics of overall system improves.

A *new control technique* is proposed for the control of real and reactive power flow in PWM CSR. The proposed technique is explained in detail in the subsequent sections. There are different types of modulation techniques such as Trapezoidal modulation, Selective Harmonic Elimination(SHE), Space Vector Modulation(SVM) can be adopted for the control of CSI fed drive. In the present work **SVM technique** is implemented. However the control technique can be extended for other modulation methods also.

2.2 Theoretical basis for Control method of PWM CSR

Power supplied from the grid to input side of the rectifier remains same as that of DC side of the rectifier. The rectifier is assumed to be loss less. The energy stored at AC side line inductor and small filter capacitor during transient condition is neglected. With these assumptions it can be written as:

$$V_{rec} * I_{dc} = \vec{V_{sPI}} * \vec{I_{sPI}}^{*} \tag{2.1}$$

$\vec{V_{sPI}}$ = grid voltage space vector(Power Invariant)

$\vec{I_{sPI}}$ = grid current space vector(Power Invariant)

$$V_{rec} * I_{dc} = (V_{sdPI} + jV_{sqPI})(I_{sdPI} - jI_{sqPI}) \tag{2.2}$$

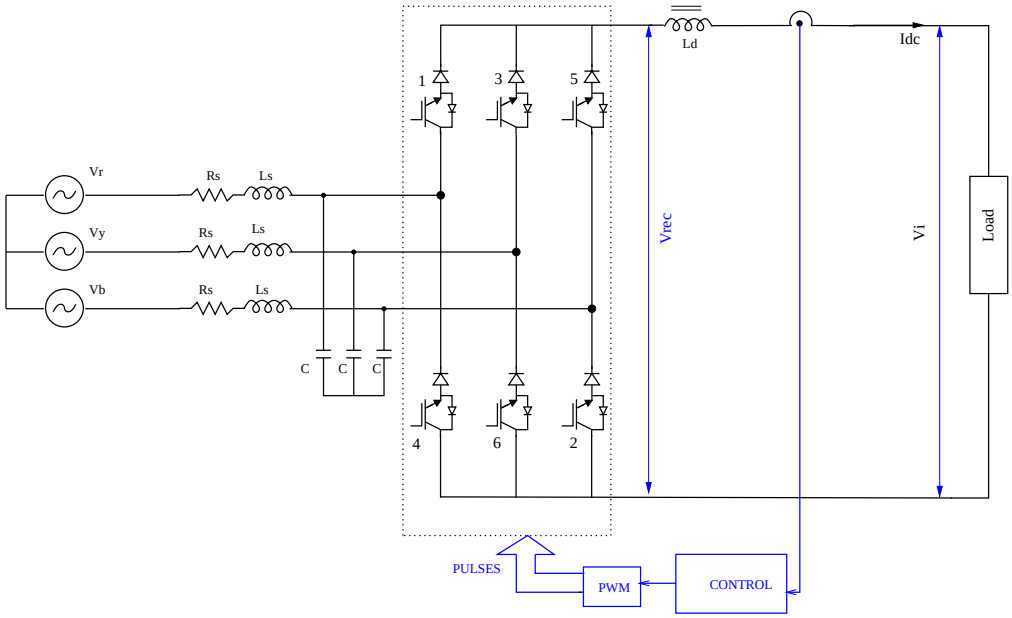

Figure 2.1: Schematic of PWM CSR

V_{sdPI}, V_{sqPI} are d and q axis voltages(power invariant) respectively.

similarly

I_{sdPI}, I_{sqPI} are d and q axis currents(power invariant) respectively.

$$V_{rec} * I_{dc} = [(V_{sdPI}I_{sdPI} + V_{sqPI}I_{sqPI}) + j(V_{sqPI}I_{sdPI} - V_{sdPI}I_{sqPI})] \tag{2.3}$$

$$V_{rec} * I_{dc} = (V_{sdPI}I_{sdPI} + V_{sqPI}I_{sqPI}) \tag{2.4}$$

With help of Phase Locked Loop(PLL), V_{sd} is aligned with R - Phase Voltage. Therefore q - axis component of the grid voltage(V_{sq}) equals to zero. Then Eq.(2.4) becomes

$$V_{rec} * I_{dc} = V_{sdPI} * I_{sqPI} \tag{2.5}$$

$$I_{dc} = (\frac{V_{sdPI}}{V_{rec}}) * I_{sdPI} \tag{2.6}$$

Eq.(2.6) implies that the DC link current can be controlled by controlling I_{sdPI} and therefore the real power flow is controlled by I_{sdPI}. Injecting reactive power to the system does not effect the real power flow because it effects only on the flow of I_{sqPI}

but not the flow of I_{sdPI}.

The control is developed with *power variant* voltage and current space vector definition. Therefore the relationship between *power variant* voltage and current space vector with power invariant voltage and current space vector is obtained as follows:

$$P = 3 * V_{ph} * I_{ph} \tag{2.7}$$

$$P = 3 * (\frac{V_{max}}{\sqrt{2}}) * (\frac{I_{max}}{\sqrt{2}}) \tag{2.8}$$

Where, P = total power supplied to the rectifier.

V_{ph} = per phase gird voltage.

I_{ph} = per phase line current.

V_{max} = Peak value of per phase grid voltage.

I_{max} = Peak value of per phase line current.

$$P = \frac{3}{2} * V_{max} * I_{max} \tag{2.9}$$

$$P = \frac{3}{2} * (V_{sd} * \frac{2}{3}) * (I_{sd} * \frac{2}{3}) \tag{2.10}$$

V_{sd} = Power variant d-axis voltage.

I_{sd} = Power variant d-axis current.

$$P = \frac{2}{3} * V_{sd} * I_{sd} \tag{2.11}$$

$$P = (\sqrt{\frac{2}{3}} V_{sd})(\sqrt{\frac{2}{3}} I_{sd}) \tag{2.12}$$

$$V_{sdPI} = \sqrt{\frac{2}{3}} V_{sd} \tag{2.13}$$

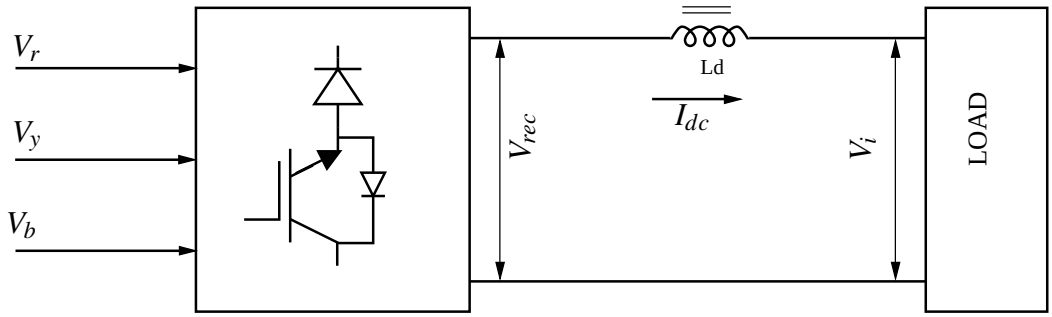

Figure 2.2: Block diagram of Power structure

$$I_{sdPI} = \sqrt{\frac{2}{3}} I_{sd} \tag{2.14}$$

Eq.(2.13), (2.14) shows that power invariant V_{sdPI}, I_{sdPI} in power balance has a scaling factor of $\sqrt{\frac{2}{3}}$ with power variant V_{sd}, I_{sd}. In control system design power variant voltages and currents are used.

2.3 Control Technique

The mathematical modelling of the converter is derived based on the power balance equations. The simple block diagram of the power circuit is shown in Fig.2.2.

The output voltage of the rectifier is V_{rec} and Voltage at load side is V_i(input voltage to inverter). From Fig.(2.2) the following equation is written using KVL.

$$V_{rec} = L_d \frac{dI_{dc}}{dt} + V_i \tag{2.15}$$

by multiplying with I_{dc} on both sides of Eq.(2.15)

$$V_{rec}.I_{dc} = L_d.I_{dc} \frac{dI_{dc}}{dt} + V_i.I_{dc} \tag{2.16}$$

from the powe balance equation $V_{rec}.I_{dc}$ can be replaced with $V_{sdPI}.I_{sdPI}$. Then the Eq.(2.16) becomes

$$V_{sdPI}.I_{sdPI} = L_d.I_{dc} \frac{dI_{dc}}{dt} + V_i.I_{dc} \tag{2.17}$$

$$I_{sdPI} = (\frac{L_d}{V_{sdPI}})(I_{dc})\frac{dI_{dc}}{dt} + (\frac{V_i}{V_{sdPI}})I_{dc} \tag{2.18}$$

Eq.(2.18) shows I_{dc} can be controlled by I_{sdPI} . But the Eq.(2.18) is non-linear, therefore to develop appropriate control Eq.(2.18) has to be linearized.

$$(I_{dc}.\frac{L_d}{V_{sdPI}})\frac{dI_{dc}}{dt} + (\frac{V_i}{V_{sdPI}})I_{dc} = I_{sdPI} \tag{2.19}$$

$$\frac{dI_{dc}}{dt} = -(\frac{V_i}{V_{sdPI}}I_{dc})(\frac{V_{sdPI}}{L_d}\frac{1}{I_{dc}}) + (\frac{V_{sdPI}}{L_d})(\frac{I_{sdPI}}{I_{dc}}) \tag{2.20}$$

$$\frac{dI_{dc}}{dt} = -(\frac{V_i}{L_d}) + (\frac{V_{sdPI}}{L_d})(\frac{I_{sdPI}}{I_{dc}}) \tag{2.21}$$

$$\dot{I_{dc}} = f(I_{dc}, I_{sdPI}, V_i) \tag{2.22}$$

by small signal analysis the non linear equation is linearized.

$$f((I_{dc0}+\Delta I_{dc}),(I_{sdPI0}+\Delta I_{sdPI}),(V_{i0}+\Delta V_i)) = f(I_{dc0}, I_{sdPI0}, V_{i0}) + \frac{\partial f}{\partial I_{dc}}.\Delta I_{dc} + \frac{\partial f}{\partial I_{sdPI}}.\Delta I_{sdPI} + \frac{\partial f}{\partial V_i}.\Delta V_i \tag{2.23}$$

where I_{dc0}, I_{sdPI0}, V_{i0} = operating points.

ΔI_{dc}, ΔI_{sdPI}, ΔV_i = small perturbations from the operating points.

$$\frac{\partial f}{\partial I_{dc}} = -(\frac{V_{sdPI}}{L_d})\frac{I_{sdPI}}{I_{dc}^2} \tag{2.24}$$

$$\frac{\partial f}{\partial I_{sdPI}} = (\frac{V_{sdPI}}{L_d})(\frac{1}{I_{dc}}) \tag{2.25}$$

$$\frac{\partial f}{\partial I_{dc}} = -\frac{1}{L_d} \tag{2.26}$$

Substituting Eq.(2.24),(2.25),(2.26) in Eq.(2.23)

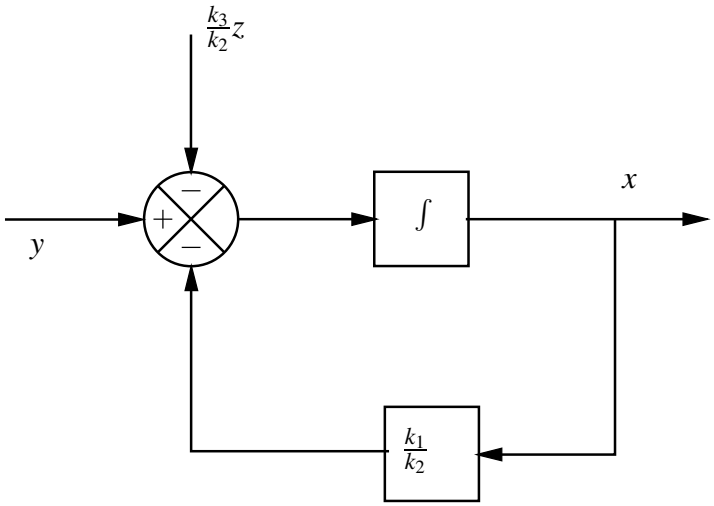

Figure 2.3: Plant model of the converter

$$I_{dc} + \dot{\Delta I_{dc}} = f(I_{dc0}, I_{sdPI0}, V_{i0}) - (\frac{V_{sdPI0}}{L_d})\frac{I_{sdPI0}}{I_{dc0}^2}.\Delta I_{dc} + (\frac{V_{sdPI0}}{L_d})(\frac{1}{I_{dc0}}).\Delta I_{sdPI} - \frac{1}{L_d}.\Delta V_i \tag{2.27}$$

$$\Delta \dot{I}_{dc} = -(\frac{V_{sdPI0}}{L_d})\frac{I_{sdPI0}}{I_{dc0}^2}.\Delta I_{dc} + (\frac{V_{sdPI0}}{L_d})(\frac{1}{I_{dc0}}).\Delta I_{sdPI} - \frac{1}{L_d}.\Delta V_i \tag{2.28}$$

$$\dot{I_{dc0}} = 0 = -\frac{V_{i0}}{L_d} + (\frac{V_{sdPI0}}{L_d})(\frac{I_{sdPI0}}{I_{dc0}} \tag{2.29}$$

let

$$x = \Delta I_{dc}, \qquad y = \Delta I_{sdPI}, \qquad z = \Delta V_i \tag{2.30}$$

let

$$k_1 = (\frac{V_{sdPI0}}{L_d})\frac{I_{sdPI0}}{I_{dc0}^2}, \qquad k_2 = (\frac{V_{sdPI0}}{L_d})(\frac{1}{I_{dc0}}), \qquad k_3 = \frac{1}{L_d} \tag{2.31}$$

Then the Eq.(2.28) reduces to

$$\dot{x} = k_1.x + k_2.y + k_3.z \tag{2.32}$$

$$y = (\frac{1}{k_2})\dot{x} - (\frac{k_1}{k_2})x - (\frac{k_3}{k_2})z \tag{2.33}$$

Fig.2.3 shows the plant model of converter. Here x is the output DC link current

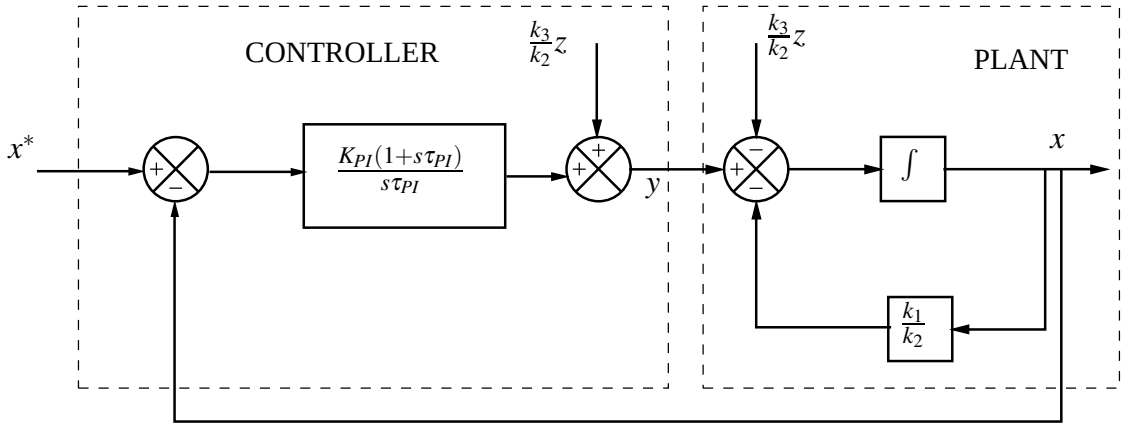

Figure 2.4: Controller with plant model

which needs to be controlled by y which is d-axis line current I_{sdPI} and $(-\frac{k_3}{k_2}z)$ is the feed forward term of the plant.

2.3.1 Design of DC link controller

The DC link current controller with plant model is shown in Fig.2.4 The PI controller transfer function is represented as:

$$PI = \frac{K_{pi}(1+s\tau_{pi})}{s\tau_{pi}} \tag{2.34}$$

After feed forward cancellation Eq.(2.32) reduces to

$$y = (\frac{1}{k_2})\dot{x} - (\frac{k_1}{k_2})x \tag{2.35}$$

Applying Laplace transform to the Eq.(2.34)

$$Y(s) = (\frac{1}{k_2})sX(s) - (\frac{k_1}{k_2})X(s) \tag{2.36}$$

$$Y(s) = X(s)(\frac{s}{k_2} - \frac{k_1}{k_2}) \tag{2.37}$$

$$Y(s) = \frac{X(s)}{k_2}(s - k_1) \tag{2.38}$$

$$\frac{X(s)}{Y(s)} = \frac{k_2}{s-k_1} \tag{2.39}$$

$$\frac{x(s)}{y(s)} = \frac{-k_2}{k_1}.\frac{1}{(1+\frac{s}{k_1})} \tag{2.40}$$

let $\frac{-1}{k_1} = \tau$

$$\frac{x(s)}{y(s)} = \frac{-k_2}{k_1}.\frac{1}{(1+s\tau)} \tag{2.41}$$

The value of τ_{pi} is chosen equal to τ so that zero of the entire transfer function$(1+s\tau_{pi})$ gets canceled to make the system simple.

Therefore

$$\tau_{pi} = \frac{-1}{k_1} \tag{2.42}$$

The value of K_{pi} is obtained based on the required band width of the system.

The entire control structure of PWM CSR is shown in Fig.2.5. It consists of 5 major blocks they are as following:

- Voltage transformations.
- DC link current controller.
- Phase Locked Loop(PLL).
- Current reference generation.
- Space Vector Modulation Technique.

2.3.2 Voltage transformations

The voltages are transformed from $3-\phi$ to $\alpha\beta 0$ using clarke's transformations. The transformation equations are as following:

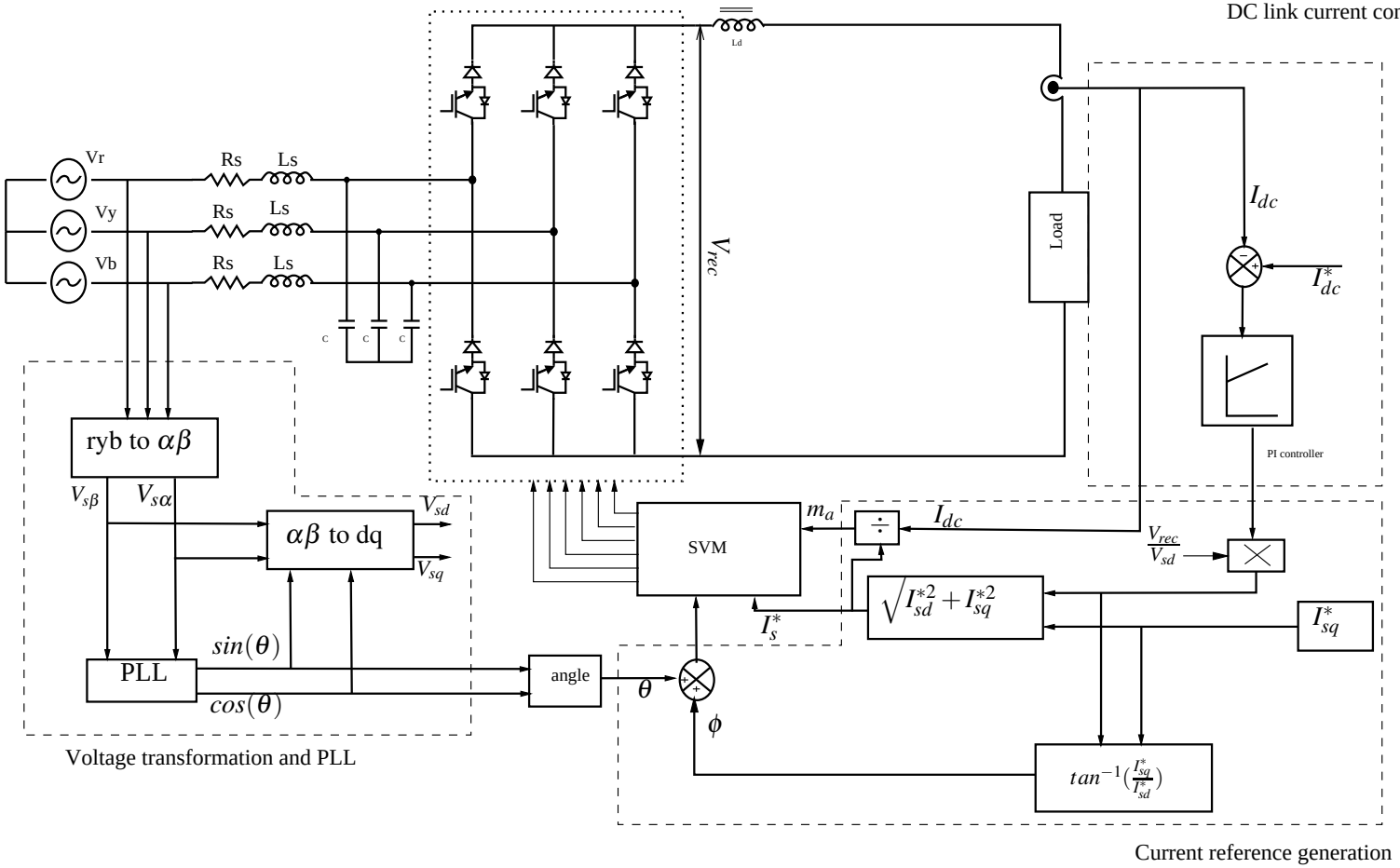

Figure 2.5: Control Structure

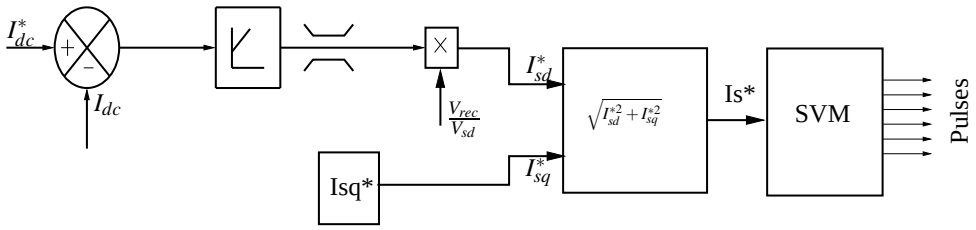

Figure 2.6: DC link current controller

$$\begin{bmatrix} V_{s\alpha} \\ V_{s\beta} \end{bmatrix} = \begin{bmatrix} \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ 0 & \frac{1}{\sqrt{3}} & -\frac{1}{\sqrt{3}} \end{bmatrix} \times \begin{bmatrix} V_r \\ V_y \\ V_b \end{bmatrix}$$

Using the above expressions the $V_{s\alpha}$, $V_{s\beta}$ are obtained and using PLL they can transform to dq axis.

2.3.3 DC Link Current Controller

The DC link current controller controls the DC link current as well as controls the real power flow in the system. One of the most important requirement of the CSR is the current cannot flow in reverse direction. The control technique should ensure that current cannot become negative.

A new control method is proposed for this system , Fig 2.6 shows its simple block diagram. I^*_{dc} is the reference DC link current and I_{dc} is the actual DC link current flowing in the circuit. The error in reference and actual DC link current is given to a Proportional - Integral (PI) controller. From the Eq.(2.6) it is clear that controller output with a scaling factor of $\frac{V_{rec}}{V_{sdPI}}$ gives I^*_{sd} which controls the real power flow. Similarly I^*_{sq} controls the reactive power flow. The value of I^*_{sq} depends on the requirement of the system. The power factor can be at unity by making I^*_{sq} value to zero. The reactive power flow depends on value of I^*_{sq}. The real power component(I^*_{sd}) and reactive power component(I^*_{sq}) is squared and added. I^*_s is the magnitude of the current space vector.

2.3.4 Phase Locked Loop(PLL)

PLL is generally described as a device that measures the phase angle of the grid voltages. The output of the PLL tracks one of the phase of input. This provides the frequency information along with phase angle. The PLL output gives unit sine and cosine

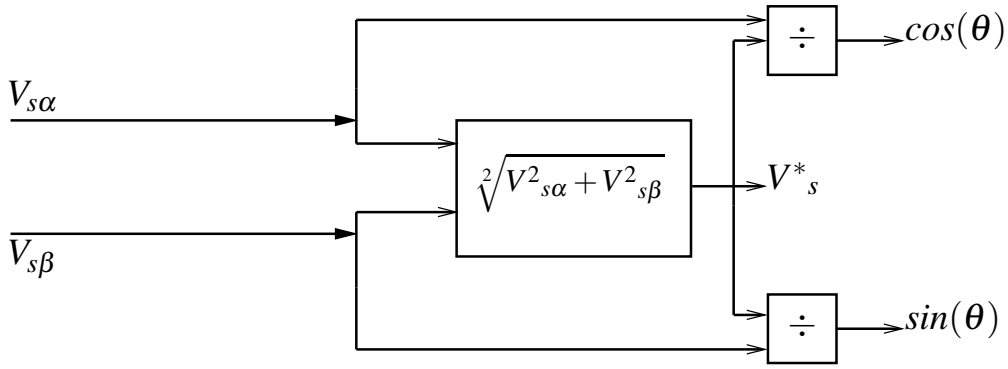

Figure 2.7: $\alpha\beta$ PLL

signals which are synchronized with supply voltage. PLL is an important part of controllers for grid connected converters. For this converter power factor control is the most important technique. The accurate phase information of the utility voltage is necessary for power factor control.

There are many types of PLL techniques such as Stationary reference frame PLL, Synchronous rotating frame PLL, $\alpha\beta$ PLL etc. In this report $\alpha\beta$ PLL is used. Fig. 2.7 shows the block diagram of the $\alpha\beta$ PLL. From the Voltage transformations $V_{s\alpha}$ and $V_{s\beta}$ are obtained and using the following equations the unit sine and cosine signals are obtained.

$$cos(\theta) = \frac{V_{s\alpha}}{\sqrt{V_{s\alpha}^2 + V_{s\beta}^2}} \tag{2.43}$$

Similarly

$$sin(\theta) = \frac{V_{s\beta}}{\sqrt{V_{s\alpha}^2 + V_{s\beta}^2}} \tag{2.44}$$

PLL described by Eq.(2.41),(2.42) cannot give accurate phase information in case of presence of harmonics in utility voltages. This can effect the entire system. A modified $\alpha\beta$ PLL is used which can provide proper phase information even with presence of grid harmonic voltage.

The modified PLL block diagram is shown in Fig 2.8. In this PLL $V_{s\alpha}$ and $V_{s\beta}$ are passed through 2 low pass filters, with a cut-off frequency of 50 Hz. Now the sine and cosine signals are obtained as earlier. After passing $V_{s\alpha}$ and $V_{s\beta}$ through two low pass filters their magnitude is reduced by half($\frac{1}{\sqrt{2}}$ for each filter) and a phase shift of 90

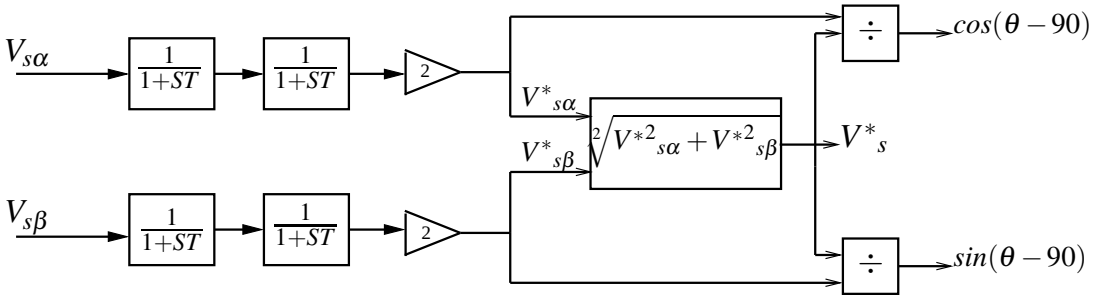

Figure 2.8: $\alpha\beta$ PLL with Low pass filters

degrees(45 degrees for each filter). So the modified unit sine and cosine signals are as follows.

$$cos(\theta-90) = \frac{V^*_{s\alpha}}{\sqrt{V^{*2}_{s\alpha}+V^{*2}_{s\beta}}} \tag{2.45}$$

$$sin(\theta-90) = \frac{V^*_{s\beta}}{\sqrt{V^{*2}_{s\alpha}+V^{*2}_{s\beta}}} \tag{2.46}$$

So the expressions for Sine and Cosine signals become:

$$sin(\theta) = \frac{V^*_{s\alpha}}{\sqrt{V^{*2}_{s\alpha}+V^{*2}_{s\beta}}} \tag{2.47}$$

$$cos(\theta) = -\frac{V^*_{s\beta}}{\sqrt{V^{*2}_{s\alpha}+V^{*2}_{s\beta}}} \tag{2.48}$$

It is important to notice that the harmonic voltages are completely eliminated by the 2 sets of low pass filters. The cut-off frequency is 50 Hz. As the 5th harmonic voltage component has frequency at 250 Hz, they are easily filter out by these two low pass filters.

Using the above expressions the proper phase information of the grid is obtained. With this phase information $\alpha\beta$ axis can be transform into dq axis.

2.3.5 Current Reference generation

The reference current vector I_{ref} is I^*_s in the proposed control technique. The angular displacement γ is sum of grid angle(PLL angle) and angle made by the space vector I^*_s

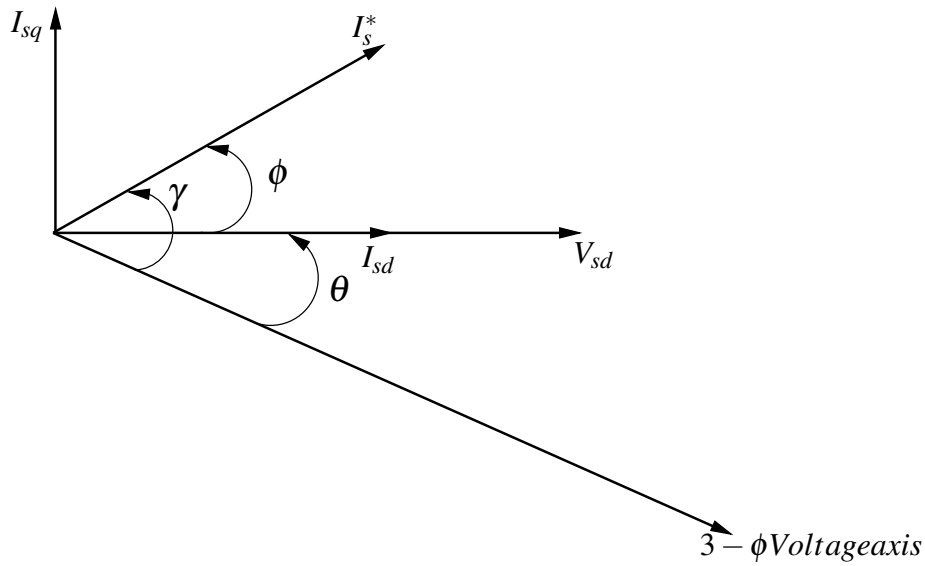

Figure 2.9: Phasor diagram for Current refernce generation

with reference. This is explained with help of a phasor diagram as shown in Fig. 2.9.

From Fig.(2.12),(2.5) the angle between 3-ϕ axis and V_{sd} is θ, it is the phase information from PLL. The angle ϕ is obtained by $tan^{-1}(\frac{I_{sq}^*}{I_{sd}^*})$. The PLL block gives the information of sin(θ), cos(θ) and the information of sin(ϕ), cos(ϕ) are availble from the required power factor calculation. From these information:

$$Sin(\gamma) = Sin(\theta+\phi) = Sin(\theta)Cos(\phi)+Cos(\theta)Sin(\phi) \tag{2.49}$$

$$Cos(\gamma) = Cos(\theta+\phi) = Cos(\theta)Cos(\phi)-Sin(\theta)Sin(\phi) \tag{2.50}$$

The information of sin(γ), cos(γ) are obtained from Eq.(2.49),(2.50). Along with this information modulation index(m_a) and I_s^* are given to SVM block.

2.3.6 Space Vector Modulation(SVM)

Generally for a VSI fed drive sinusoidal pulse width modulation technique is used. Space vector modulation is also used for VSI fed drive to utilize the DC bus voltage more effectively. Implementation of space vector modulation technique in digital platform is more complex when compared with SPWM. But unfortunately SPWM technique is not valid for a CSI rectifier. Because at any point of time one top switch and one bottom switch of the rectifier has to be remained ON. This condition can be eas-

Table 2.1: Switching states and Space Vectors

Type	Switching state	On state Switch	i_{wA}	i_{wB}	i_{wC}	Space Vector
Zero states	[14] [36] [52]	S1, S4 S3, S6 S5, S2	0	0	0	$\vec{I_0}$
Active states	[61]	S6, S1	I_{dc}	-I_{dc}	0	$\vec{I_1}$
	[12]	S1, S2	I_{dc}	0	-I_{dc}	$\vec{I_2}$
	[23]	S2, S3	0	I_{dc}	-I_{dc}	$\vec{I_3}$
	[34]	S3, S4	-I_{dc}	I_{dc}	0	$\vec{I_4}$
	[45]	S4, S5	-I_{dc}	0	I_{dc}	$\vec{I_5}$
	[56]	S5, S6	0	-I_{dc}	I_{dc}	$\vec{I_6}$

ily achieved if SVPWM technique is adopted for CSI fed drives. Therefore SVPWM technique is adopted for the PWM CSI rectifier.

As discussed earlier the most important constraint for switching pattern of current source rectifier is that only two switches must conduct at any instant. Therefore 9 switching states are possible for a Current Source rectifier. There are 3 zero switching states and 6 active switching states. The zero switching states are [14], [36], [52]. The notation [14] indicates that switches 1 and 4 are ON simultaneously and rest of the switches are OFF. This notation is followed in the entire report. In the zero switching state the PWM current is zero. Similarly [12] is an active switching state where switch 1 and 2 are conducting simultaneously and rest of the switches are OFF. In this state I_{dc} current flows through switch 1, load and switch 2. The active and zero switching states are listed in the table 2.1. The numbering of the switches can be referred from Fig.2.1.

Space Vectors

A typical Space Vector diagram for a two level CSI rectifier is shown in Fig 2.10.

Where $\vec{I_1}$ to $\vec{I_6}$ are active vectors and $\vec{I_0}$ is the Zero Vector. All the active vectors form a regular hexagon with six equal sectors and zero vector $\vec{I_0}$ lies at center of the hexagon.

The relation between space vectors and switching states is derived by assuming that the converter 3 phase currents are balanced.

$$I_{wA} + I_{wB} + I_{wC} = 0 \tag{2.51}$$

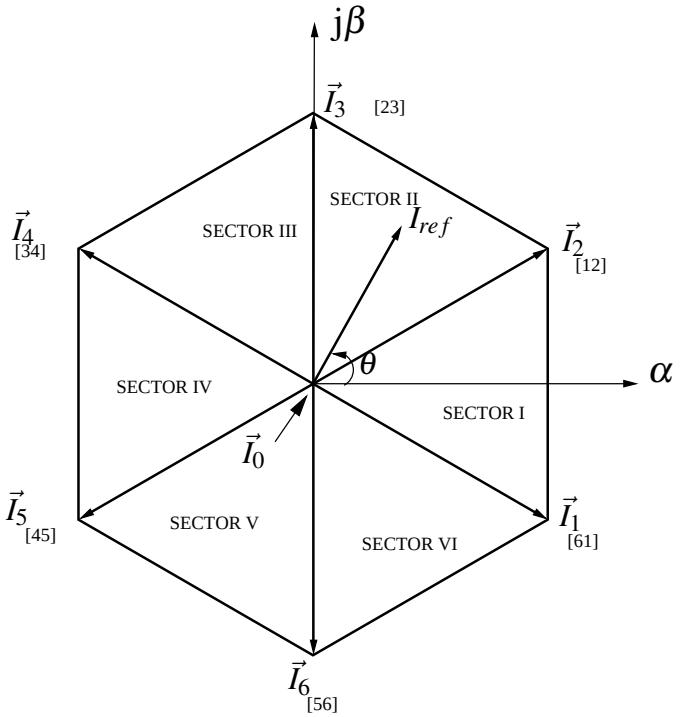

Figure 2.10: Space Vector diagram for CSR

Where I_{wA}, I_{wB}, I_{wC} are the instantaneous PWM currents in the converter phases R, Y, B. The three phase currents are transformed into $\alpha\beta$ plane using clarke's transformation. The current space vector can be expressed in terms of 3 phase PWM currents as

$$\vec{I}(t) = I_{wA}(t) + I_{wB}(t)e^{j\frac{2\pi}{3}} + I_{wC}(t)e^{j\frac{4\pi}{3}} \tag{2.52}$$

Current space vector is also expressed in $\alpha\beta$ plane.

$$\vec{I}(t) = I_{\alpha}(t) + jI_{\beta}(t) \tag{2.53}$$

For active state [61], switches 6 and 1 are conducting then the PWM currents are $I_{wA} = I_{dc}$, $I_{wB} = -I_{dc}$ and $I_{wC} = 0$. By substituting these values in Eq.(2.52) the current space vector expression yields to

$$\vec{I_1} = \sqrt{3}I_{dc}e^{j(-\frac{\pi}{6})} \tag{2.54}$$

Similarly other 5 vectors can be derived in similar way. The general expression of space vector for all active states is given in Eq.2.55.

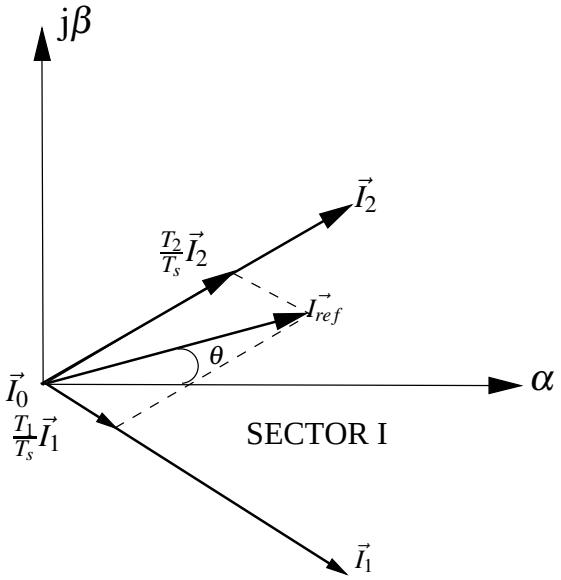

Figure 2.11: Synthesis of I_{ref} by I_1, I_2 and I_0

$$\vec{I_k} = \sqrt{3} I_{dc} e^{j((k-1)\frac{\pi}{3} - \frac{\pi}{6})} \tag{2.55}$$

here k = 1,2,...6.

Dwell time Calculation

The dwell time for the stationary vectors essentially represents the duty-cycle time (on-state or off-state time) of the chosen switches during a sampling period T_s.

The dwell time calculation is based on ampere-second balancing principle, that is, the product of the reference vector I_{ref} and sampling period T_s equals the sum of the current vectors multiplied by the time interval of chosen space vectors. Assuming that the sampling period T_s is sufficiently small, the reference vector I_{ref} can be considered constant during T_s. Under this assumption, I_{ref} can be approximated by two adjacent active vectors and a zero vector. For example, with I_{ref} falling into sector I as shown in Fig. 2.11 it can be synthesized by I_1, I_2 and I_0. The ampere-second balancing equation is given by

$$\vec{I_{ref}} T_s = \vec{I}_1 T_1 + \vec{I}_2 T_2 + \vec{I}_0 T_0 \tag{2.56}$$

$$T_s = T_1 + T_2 + T_0 \tag{2.57}$$

Where T_1, T_2, T_0 are dwell time for vectors $\vec{I_1}$, $\vec{I_2}$, $\vec{I_0}$ respectively.

Substituting

$$\vec{I_{ref}} = I_{ref}e^{j\theta}; \qquad \vec{I_1} = \sqrt{3}I_{dc}e^{-j\frac{\pi}{6}}; \qquad \vec{I_2} = \sqrt{3}I_{dc}e^{j\frac{\pi}{6}}; \qquad \vec{I_0} = 0 \tag{2.58}$$

into Eq.(2.56) and then splitting the resultant equation into α-axis and β-axis leads to

$$Re: \qquad I_{ref}(cos\theta)T_s = I_{dc}(T_1 + T_2) \tag{2.59}$$

$$Im: \qquad I_{ref}(sin\theta)T_s = \frac{1}{\sqrt{3}}I_{dc}(-T_1 + T_2) \tag{2.60}$$

Solving the equations together with $T_s = T_1 + T_2 + T_0$ gives

$$T_1 = m_a sin(\frac{\pi}{6} - \theta)T_s \tag{2.61}$$

$$T_2 = m_a sin(\frac{\pi}{6} + \theta)T_s \tag{2.62}$$

$$T_0 = T_s - T_1 - T_2 \tag{2.63}$$

where m_a is the modulation index given by

$$m_a = \frac{I_{ref}}{I_{dc}} \tag{2.64}$$

The above dwell time expressions are for sector I. Similarly for all sectors the dwell time expressions can be obtained. The general expressions for all the sectors is same as sector I but angular displacement θ is modified with θ'.

here

$$\theta' = \theta - (k-1)\frac{\pi}{3} \qquad for \quad k = 1,2...,6 \tag{2.65}$$

Then Eqn. (2.61), (2.62) becomes

$$T_1 = m_a sin(\frac{\pi}{6} - \theta')T_s \tag{2.66}$$

$$T_2 = m_a sin(\frac{\pi}{6} + \theta')T_s \tag{2.67}$$

Switching sequence

Similar to the space vector modulation for the two-level VSI, the switching sequence design for the CSI should satisfy the following two requirements for the minimization of switching frequencies:

- The transition from one switching state to the next involves only two switches, one being switched on and the other switched off.

- At any pint of time only two switches can conduct. One top switch and one bottom switch.

- The transition for I_{ref} moving from one sector to the next requires the minimum number of switchings.

Fig.2.12 shows a typical three-segment sequence for the reference vector I_{ref} residing in sector I, where V_{g1} to V_{g6} are the gate signals for switches S1 to S6, respectively. The reference vector I_{ref} is synthesized by I_1, I_2, and I_0. The sampling period T_s is divided into three segments composed of T_1, T_2, and T_0. The switching states for vectors $\vec{I_1}$ and $\vec{I_2}$ are [61] and [12], and their corresponding on-state switch pairs are (S6, S1) and (S1, S2). The zero state [14] is selected for $\vec{I_0}$ such that the design requirement is satisfied. To avoid the discontinuity of current in the circuit a small overlap angle(β) is introduced between outgoing and incoming switch. Typically an angle of 5μs is given in the experimental setup [2].

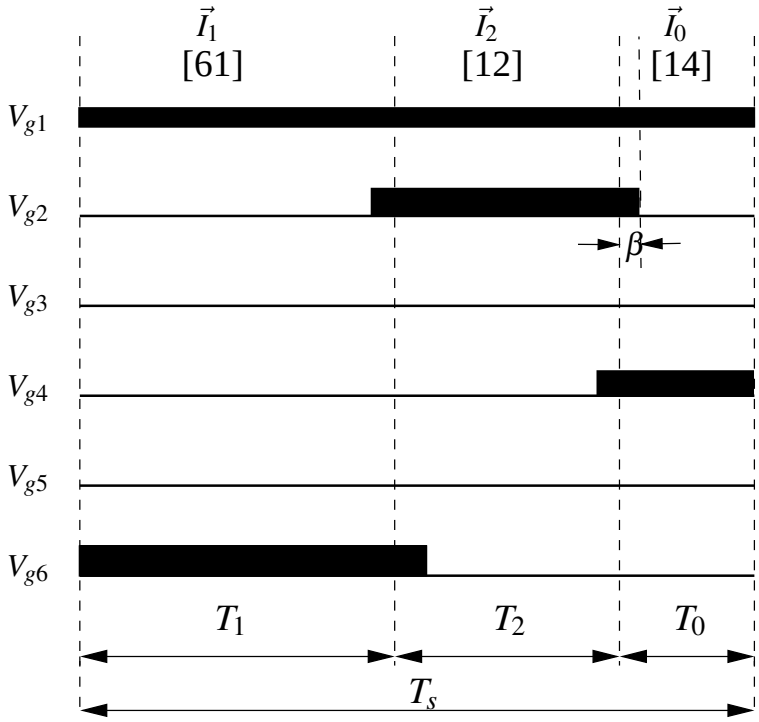

Figure 2.12: Switching Sequence

2.4 Filter Design

The PWM CSR operates at high switching frequencies. Therefore the current from the grid contains harmonic currents at switching frequency range. These harmonics in the current should be filtered out. An L-C filter is used to remove the harmonics.

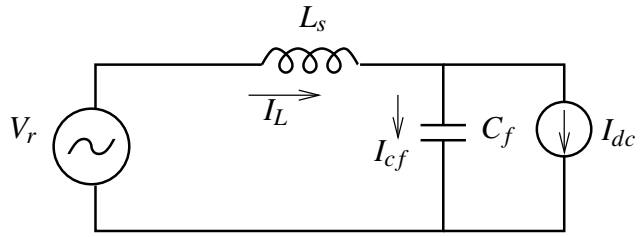

Figure 2.13: R-phase equivalent circuit with filter

Fig.2.13 shows the R - phase equivalent circuit with L - C filter. V_r is the R - phase source voltage, L_s is the line inductance on AC side. C_f is the filter capacitor and I_{dc} is the DC link current.

Considering only the DC link current, the equivalent circuit becomes as shown in Fig.2.14.

From Fig.2.14 ratio of current through inductor and capacitor can be written as:

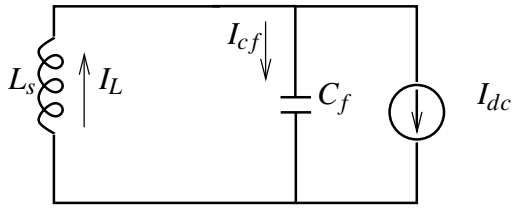

Figure 2.14: R-phase equivalent circuit with filter

$$\frac{I_L}{I_{cf}} = \frac{X_{cf}}{X_L} \tag{2.68}$$

$$\frac{I_L}{I_{cf}} = \frac{1}{\omega^2 LC} \tag{2.69}$$

The values of L_s and $C-f$ are chosen so that current at switching frequencies has to flow through capacitor. From this condition

$$\frac{I_L}{I_{cf}} \ll \frac{1}{10} \tag{2.70}$$

$$\frac{1}{\omega^2 L_s C_f} \ll \frac{1}{10} \tag{2.71}$$

$$L_s C_f \gg \frac{10}{\omega_{sw}^2} \tag{2.72}$$

Similarly, at fundamental frequency the current should flow through inductor. From this condition

$$\frac{I_L}{I_{cf}} \gg 10 \tag{2.73}$$

$$L_s C_f \ll \frac{1}{10\omega_f^2} \tag{2.74}$$

From the Eqn.(2.72),(2.74) the values of L_s and C_f are chosen by satisfying the two conditions.

2.5 Conclusion

A new control method is proposed and its objectives are discussed. The theoretical basis for the proposed control method(based on the power balance) is presented in this chapter. The plant model and the DC link current controller are derived. Various blocks of the entire control system is explained in detail. The hardware organisation of entire system is discussed in the next chapter.

CHAPTER 3

Hardware Organisation

3.1 Introduction

The hardware for PWM CSR is built based on the prototype requirement. The hardware set up consists of power module and control module. The control of PWM CSR is implemented in digital platform. In this chapter, the organisation of hardware setup, digital control implementation and various additional circuits developed for interfacing and protection is discussed in detail. The hardware setup consists of the following modules:

- Three Phase Current Source Rectifier Module.
- Gate driving circuit for IGBT.
- Voltage and Current Sensors.
- Digital Signal Controller.
- Protection hardware.
- Analog Conditioning card.

3.2 Three phase Current Source Rectifier Module

A three phase 2 level Current Source Rectifier(CSR) is built in laboratory. A Printed Circuit Board(PCB) for PWM CSR is designed and the required components are mounted on it by soldering. As discussed in *chapter 1* the switches for CSR is realized with IGBT and series diode. *IXA12IF1200HB* from *IXYS* is the IGBT used. It is a 1200 V and 20

A rated device. *DHG20I1200PA* from *IXYS* is the series diode used. It is also a 1200 V and 20 A rated device. The series connection of these two devices together is a single switch module for CSR. A total of 6 modules are used for three phase CSR. A snubber capacitor and snubber resistor are connected in series across each switching module for protection. The snubber connection across the switching module suppresses the rate of rise of forward voltage i.e. $\frac{dv}{dt}$ across the switching module. The IGBT and series diode are mounted on PCB along with a heat sink.

3.3 Gate driving circuit for IGBT

The IGBT devices operate at high power and high current ratings. Gate signals are generated from digital signal controllers are given to the gate driver circuit. Gate driver circuit isolates them and provide appropriate gating signal to the IGBT.

Skyper 32 PRO R from Semikron is used as gate driver for driving IGBT switches. Additional to gate driver, its corresponding adapter board is also used for giving power supply to gate driver and terminals for input and output are provided in the adapter board. *Skyper 32 PRO R* is the gate driver circuit which is designed for VSI(complementary with dead band), where single gate driver can be used for each leg. But for CSR the switching pattern is different, so a single gate driver cannot be used for one leg. For each switch one gate driver is used, a total of 6 gate drivers are used.

3.4 Voltage and Current Sensing

The closed loop control system of CSR requires feedback signals. The proposed control technique is for DC link current control, therefore DC link current feedback signal is required for closed loop control. Also for PLL the grid voltage information is required. All these informations are provided by the high precision Hall effect Sensors. In this work LA 55P current sensors and LV 25P Voltage sensors from *LEM* is used. The current sensors can sense up to 50 A of current and gives output of 50 mA current signal. Voltage sensor can sense up to 500 V and gives a 10 V output signal.

3.5 Digital Signal Controller

The proposed control technique is implemented in a digital platform based on *TMS320F28335 DSC*, from *Texas Instruments*. This DSC is capable of doing 6 basic operations in a single instruction cycle. It is a 32-bit floating point processor, it enables the floating point computations to be performed in hardware. Code Composer Studio(CCS) Integrated Design Environment(IDE)V4 is software used to develop control algorithms. The control algorithm for PWM CSR is developed using CCS in C-language.

The computations of the control algorithm are done in digital platform, so it needs digital information from the hardware but the real time hardware provides only analog information. So an ADC module is provided in the DSC where the analog signals from real time hardware are converted into digital data and the computation process is carried out. *TMS320F28335* has built-in 12 bit 16 channel ADC. The ADC module converts the analog data to 12 bit digital value and saves it into one of the result registers from whee the processor can access the data. From the computations DSC generates PWM signals from ePWM module. *TMS320F28335* has six enhanced PWM modules. Each ePWM module has two output channels, channel A and channel B. *TMS320F28335* provides Inter Integrated Circuits(I2C) interface, it communicates between two Integrated circuits. The I2C interface is used to communicate between DSP and DAC.

3.6 Protection Hardware

A protection circuit is developed to protect the power circuit from over voltages and over currents. The protection is provided to 3-ϕ line voltages, line currents, DC link current and rectifier voltage.

3.6.1 Brief overview of Protection circuit

The supply to the protection board is given from Regulated Power Supply(RPS). It gives +15 V, -15 V, +5 V to protection board. The line voltages, line currents, DC link current, Rectifier Voltage sensed signals are given as input. The logic implemented with these signals should indicate the fault and enable protection.

- **Fault indication:** The sensed signal is given as input to a unity gain operational amplifier(op-amp). This op-amp avoids the voltage drop of the sensed signal. *RC4136N* IC is used for unity gain op-amp.

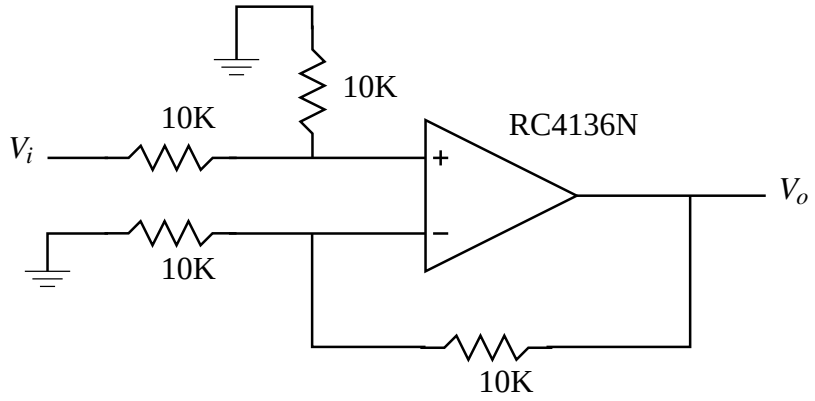

Figure 3.1: Unity gain op-amp circuit

Fig 3.1 shows the unity gain op-amp circuit. V_I is the input sensed signal, V_0 is the output of op-amp. Using a variable pot resistor the reference signals are generated. These reference signals are the limits of sensed signals.

The op-amp output and reference signal are given to comparator. *LM339* IC is used as comparator. The output of the comparator gives the information of fault. If the sensed signal value is above the reference signal the comparator gives output high, else low. The comparator output high indicates fault. This fault signal is given to R pin of SR latch(*HEF4044B* IC). A 5 V signal thorugh a mechanical reset switch is level shifted to 15V and given to S pin of SR latch IC. The reset signal to SR latch is always high until the reset switch is pressed. The output of SR latch Q is connected to non inverting buffer IC(CD4050BC) and its output is connected to cathode of LED light. 15V supply is connected to anode of LED light. The LED light glows only if non inverting buffer IC output is low. This implies whenever the sensed signals are crossing the value of reference signal the LED glows.

- **Protection Enable:** All the fault signals(output of comparators) are given to R pin of SR latch and RESET signal is given to S pin. The RESET signal is obtained as discussed earlier, similarly another 5V signal is passed through mechanical ON/OFF switch to level shift IC(*CD4504B*), it gives the PWR ON signal. The output of SR latch, RESET, PWR ON signals are given to a 3 input AND gate(*HEF4073B*), its output is ENABLE signal. Fig.3.2 shows the logic to obtain

ENABLE signal The inverted signal of ENABLE is ENABLENOT.

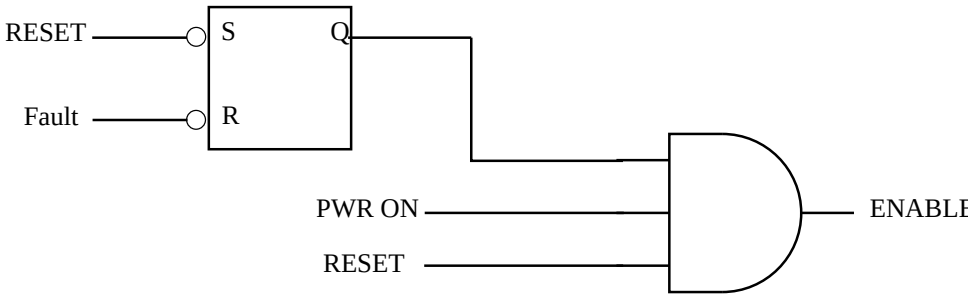

Figure 3.2: Logic to obtain ENABLE signal

The PWM signals generated by DSC is of 3.3 V level. But 15V gate pulses are required to turn ON the switch. The PWM signals are given to a level shifter IC(*CD4504B*). It shifts the level of 3.3 V to 15 V. These PWM signals are given to OR gate(*CD4071B*), and another input is ENABLENOT signal. The output signals of OR gate is given to AND gate IC(*CD4081B*) with PWR ON signal as another input. The output of AND gate are given to gate driver circuits. In case any fault occurred ENABLE signal becomes low correspondingly ENABLENOT signal becomes high. If ENABLENOT is high, irrespective of other input the output is always high. The AND gate output gives the same output as OR gate if PWR ON signal is high. Fig.3.3 shows it logic diagram.

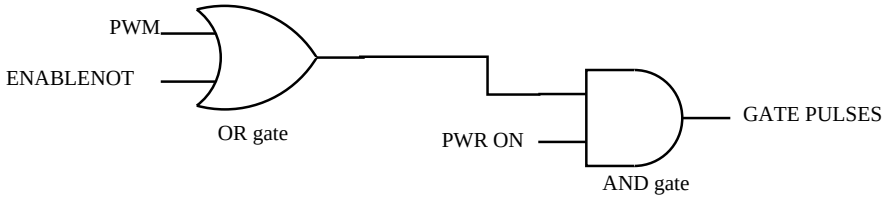

Figure 3.3: Protection Enable logic

This implies, in case of fault the gate drivers receive continuous high signals from protection board, so that all the IGBT switches are turned ON.

When a fault occurred in the circuit the protection board indicates fault and enables protection. Even after the fault is cleared in the circuit the protection board still indicates fault and provides protection until the RESET switch is pressed.

3.7 Analog Conditioning Card

Analog conditioning card acts as interface between DSC and protection board. It has an signal conditioning circuitry, it can filter, attenuate and level shift. The Hall sensors gives an output signal of $\pm$ 10 V, which cannot give directly to ADC interface of DSC. This signal conditioning circuit converts the bipolar signal to a level of 0 to 3 V which is required by the DSC. Also a 12-bit 4 channel Digital to Analog Converter(DAC) is provided in the board. The intermediate calculated variables in DSC can be viewed using DAC. A level shifting IC is provided in the board to convert 0 - 3.3 V level of DSC output to 15 V level.

3.8 Testing of Hardware

Testing of CSR module: The CSR switching modules are tested in CSI mode. 3-ϕ supply is given to a SCR based rectifier with certain firing angle. The DC output of it is connected to a DC choke inductance which acts as a DC link current source to the inverter. From DSC 120 degrees pulses of 50 Hz frequency and overlap duration of 320 μsec are generated and given to switching modules through protection circuit and gate drivers. The ac side of the inverter is connected to a star connected resistive load. As the pulses are 120 degrees the line current on AC side of the inverter is a quasi square wave.

3.9 Starting Sequence of Hardware setup

The hardware setup consists of various circuits which gets power supply from different sources. The method of start up and shut down of the entire system is as follows.

- Firstly the control power supply is switched ON. The control supply is from RPS which is given to protection card, analog conditioning card, gate driver circuits, voltage and current sensor cards.

- After the control supply, the DSC is switched ON. The supply to DSC is given from Universal Serial Bus(USB) Emulator connected from computer. The control code

is debugged by dumping into the processor.

- The 3-ϕ power supply is switched ON and using the auto-transformer the required voltage is supplied to CSR.

- Finally the mechanical ON/OFF switch is turned ON. Once this switch is turned ON the CSR start running.

3.10 Hardware Setup

The hardware setup of PWM CSR is discussed earlier. Apart from these, a 3-ϕ auto transformer is used for supplying the voltage from grid to CSR and a DC choke inductance of 30 mH is used. Photographs of various hardware circuits are shown in this section.

Fig.3.4 shows the Protection board.

Fig.3.5 shows the Analog Conditioning Card.

Fig.3.6 shows the Current Source Rectifier Module.

Fig.3.7 shows the Semikron IGBT gate driver board along with its adapter board.

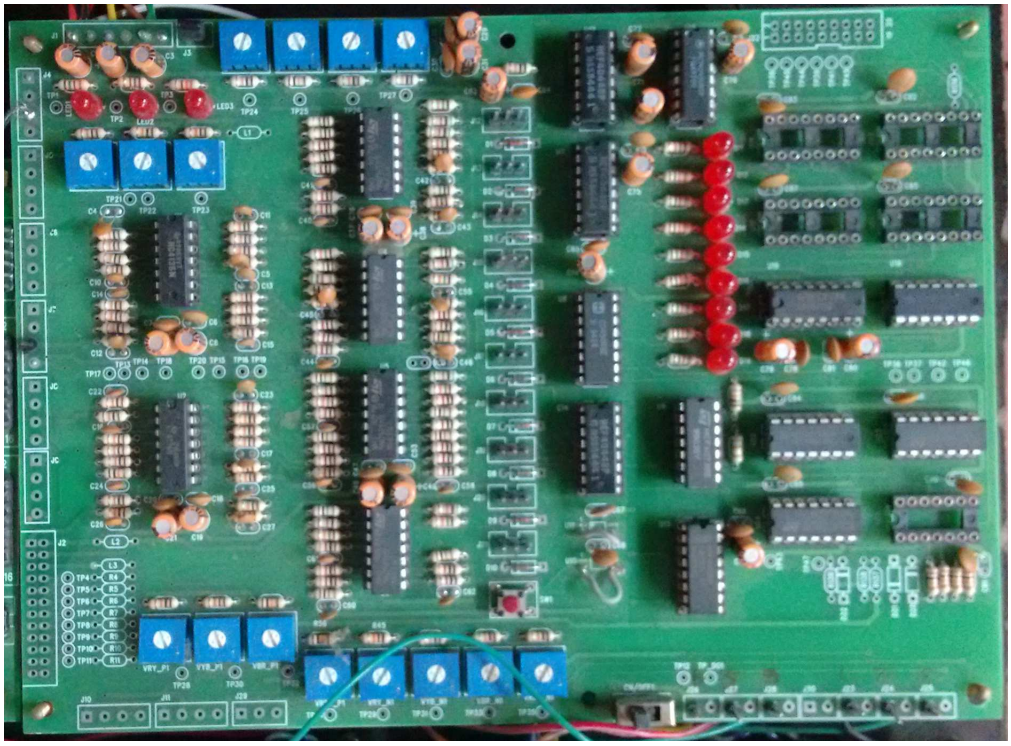

Figure 3.4: Protection board

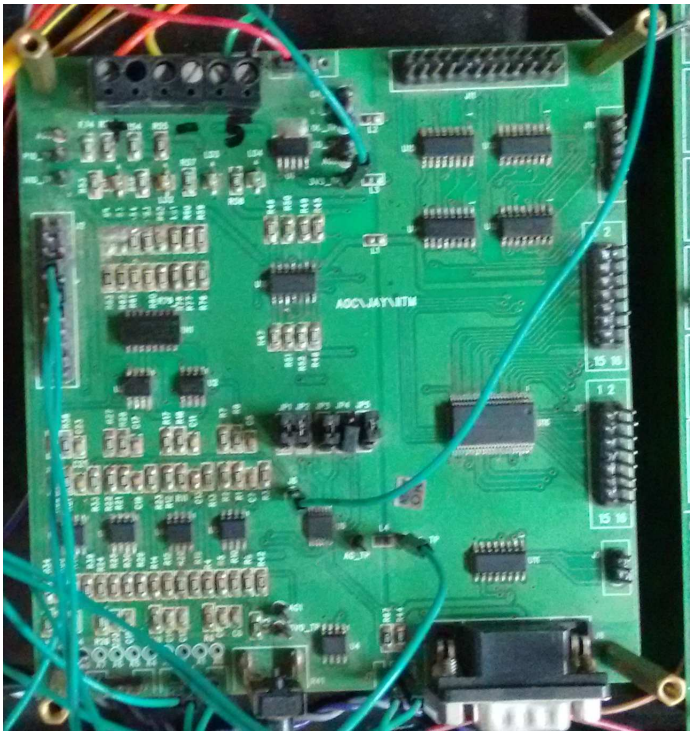

Figure 3.5: Analog Conditioning Card

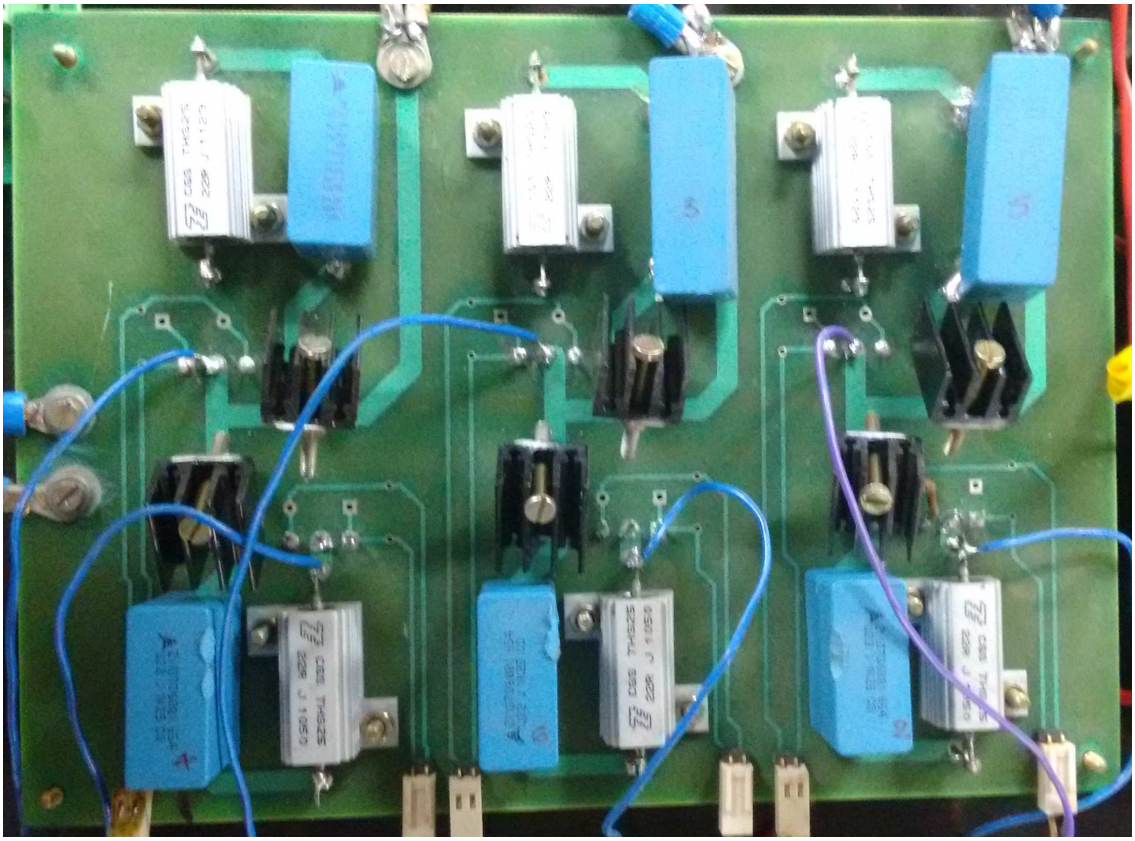

Figure 3.6: Current Source Rectifier Module

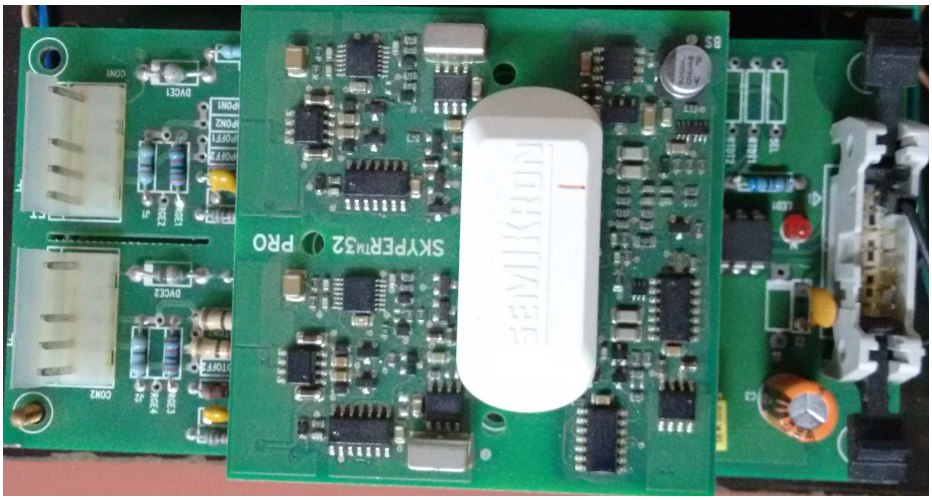

Figure 3.7: Semikron IGBT gate driver(*Skyper 32 PRO R*)

3.11 Conclusion

In this chapter, various hardware circuits used for PWM CSR are discussed. The additional circuits used in the hardware are also discussed, and a brief overview of protection card is presented. The testing of CSR switching board is done in CSI mode. Finally the steps followed for startup and shutdown of the entire hardware is mentioned. The Simulation and hardware results of PWM CSR is presented in the next chapter.

CHAPTER 4

Results and Inferences

4.1 Simulation Results

A PWM CSR as discussed in chapter 2, chapter 3 is connected to 3-ϕ grid. A resistive load is connected at the DC side of the rectifier. The simulation of PWM CSR is done in MATLAB/SIMULINK. The parameters chosen for the simulation of the circuit are shown in Table.4.1.

Table 4.1: Parameters of the circuit

S.No	Parameter	Value
1	Source voltage(Phase)	230 V
2	frequency	50 Hz
3	DC choke Inductance	300 mH
4	Load Resistance	1 Ω
5	Switching Frequency	3 kHz
6	Line side inductance	2 mH
7	Filter Capacitance	10 μF
8	Reference DC link Current	10 A

The values of PI controller parameters are obtained by the design method which is discussed in Chapter 2. The controller limiter value is estimated from actual I_{dc} current flowing in the circuit and 1.5 times of it is taken as limiter value.

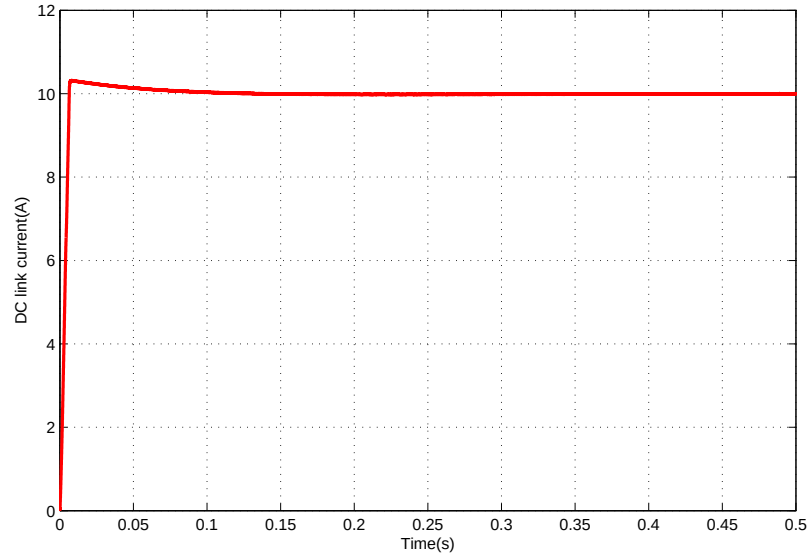

Figure 4.1: DC link controlled current including transients *(Scale: X axis: 50 msec/div, Y axis: 1 A/div)*

Fig.4.1 shows the simulated controlled DC link current of PWM CSR. The reference current is 10 A and the controller obtained the desired reference.

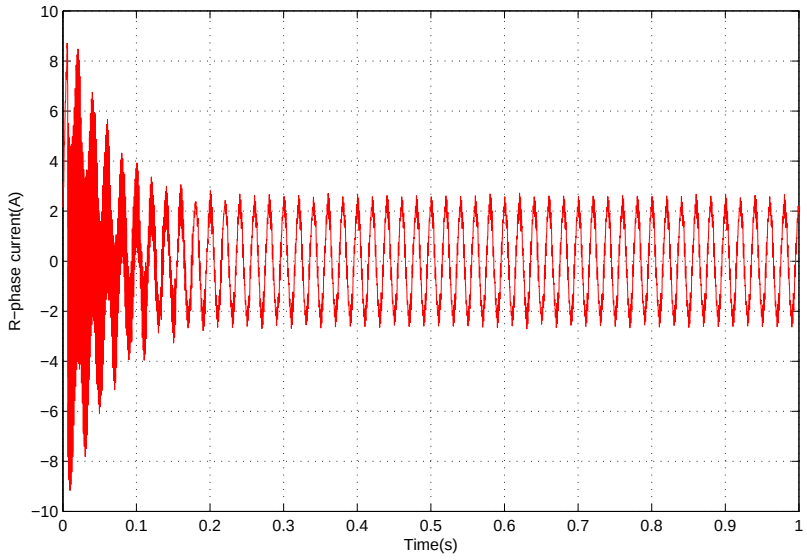

Figure 4.2: R phase line current including transients *(Scale: X axis: 100 msec/div, Y axis: 1 A/div)*

Fig.4.2 shows the simulated R phase line current. One of the objective of control method proposed is to achieve sinusoidal line current. It is obtained by simulation. The initial inrush current is responsible for quick charging of the DC link inductor to DC link current reference.

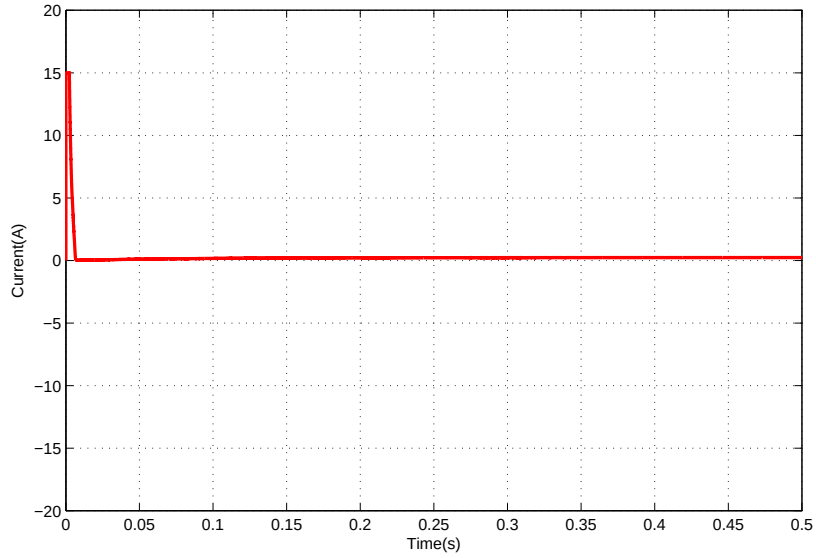

Figure 4.3: d-axis current reference by the controller output. *(Scale: X-axis: 50 msec/div, Y-axis: 1 A/div)*

Fig.4.3 show the simulated reference d-axis current I^*_{sd}, it is the controller output with scaling of $\frac{V_{rec}}{V_{sd}}$. It is important to notice that at beginning I^*_{sd} shoots up to a high value. This is for charging the DC link inductor. After that I^*_{sd} is supplying only the real power demand by the rectifier.

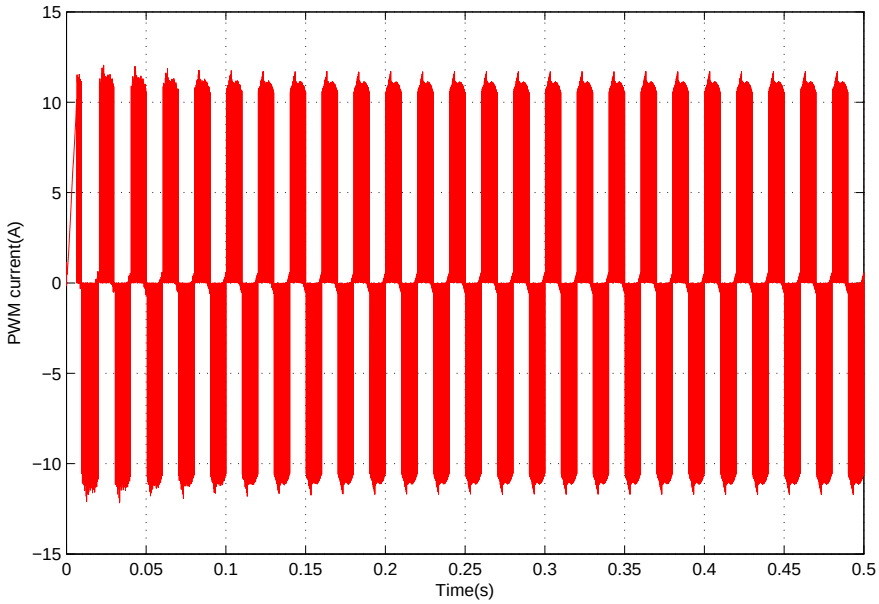

Figure 4.4: R phase PWM current. *(Scale: X-axis: 50 msec/div, Y-axis: 1 A/div)*

Fig.4.4 shows the simulated R phase PWM current which is PWM square wave in shape. This is the PWM output current just after the inverter.

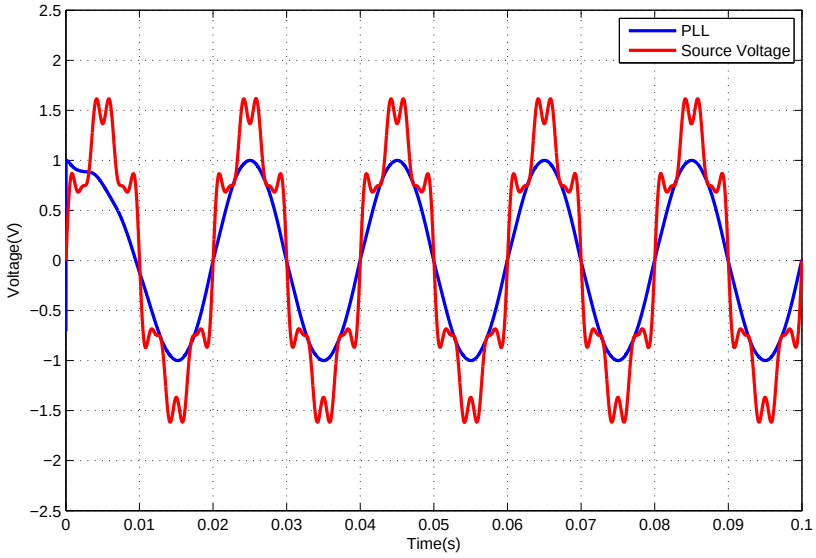

Figure 4.5: PLL output(blue) and Source voltage with harmonics(red). *(Scale: X-axis: 10 msec/div, Y-axis: 1 V/div(blue) and 200 V/div(red))*

Fig.4.5 shows the output of the $\alpha\beta$ PLL with low pass filters and source voltage with harmonics. The PLL output(blue) is in proper sine wave shape even with presence of harmonics in source voltages. Fig.4.5 justifies that the PLL with low pass filters provides proper PLL output even with source voltage harmonics.

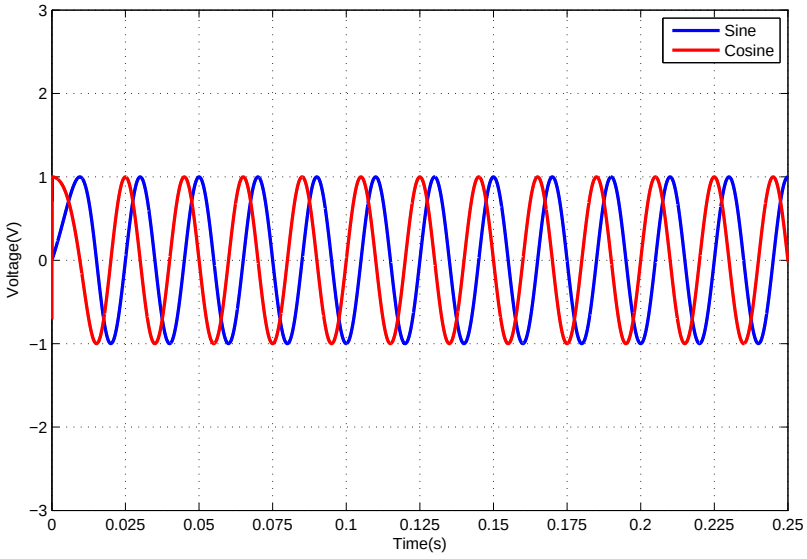

Figure 4.6: PLL output: unit sine(blue) and cosine(red) voltages. *(Scale: X-axis: 25 msec/div, Y-axis: 1 V/div)*

Fig.4.6 shows the simulation output of $\alpha\beta$ PLL with low pass filters from the actual simulation circuit.

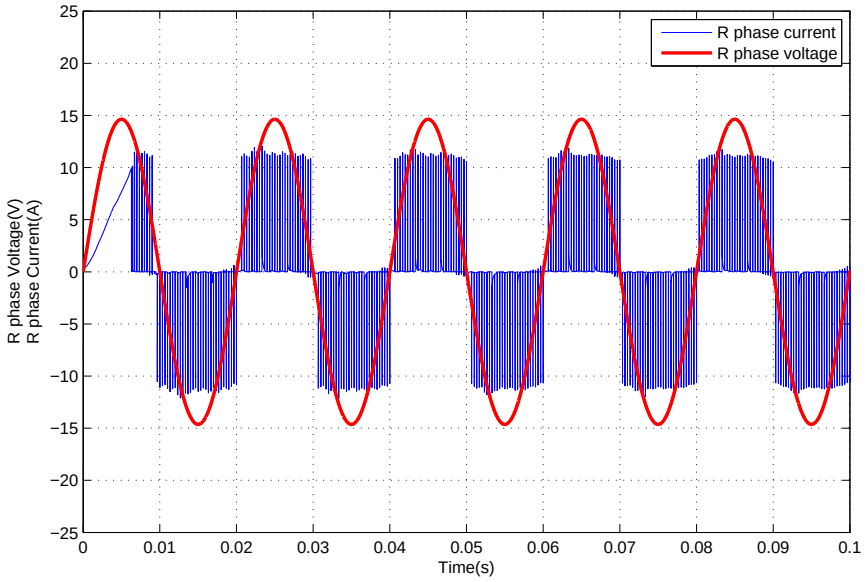

Figure 4.7: Voltage(red) and current(blue) waveforms for unity Power factor control. *(Scale: X-axis: 10 msec/div, Y-axis: 1 A/div and 22 V/div)*

Fig.4.7 shows the current and voltage waveforms together to show the phase difference between them. As the q-axis current reference I_{sq}^{*} kept at zero the power factor is unity.

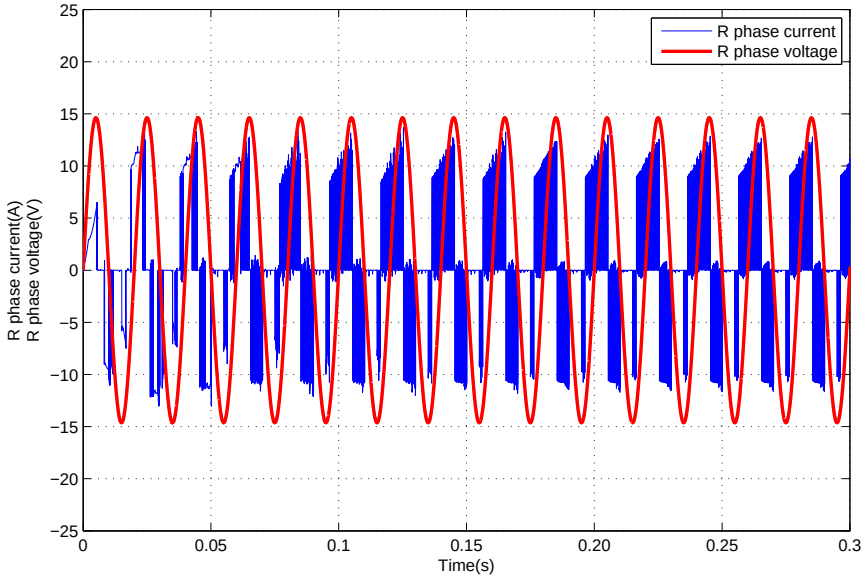

Figure 4.8: Voltage(red) and current(blue) waveforms for leading Power factor control. *(Scale: X-axis: 50 msec/div, Y-axis: 1 A/div and 22 V/div)*

Fig.4.8 shows the current and voltage waveform together to show the phase difference between them. As the q-axis current reference I_{sq}^{*} is kept at -5 A the power factor is leading.

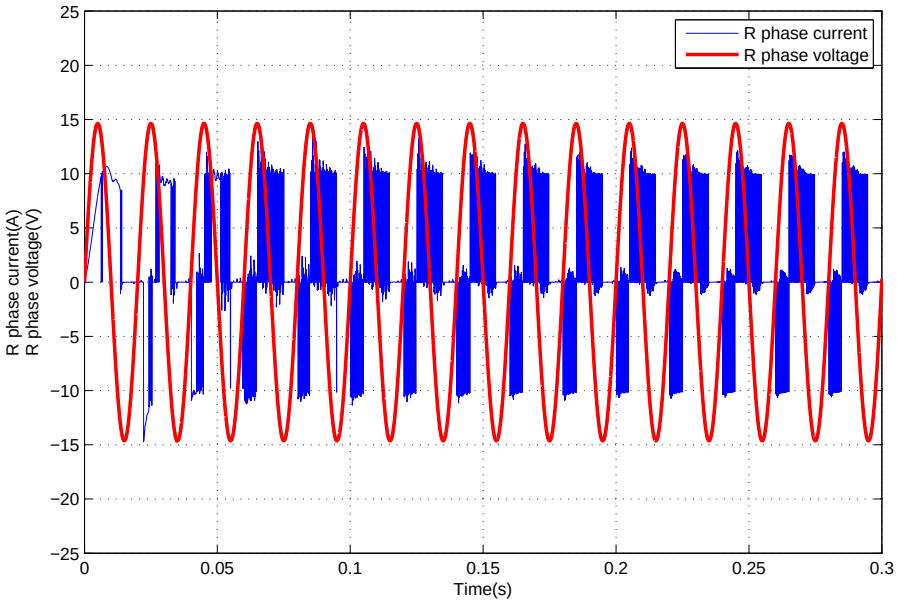

Figure 4.9: Voltage(red) and current(blue) waveforms for lagging Power factor control. *(Scale: X-axis: 50 msec/div, Y-axis: 1 A/div and 22 V/div)*

Fig.4.9 shows the current and voltage waveform together to show the phase difference between them. As the q-axis current reference I_{sq}^{*} is kept at 5 A the power factor is lagging.

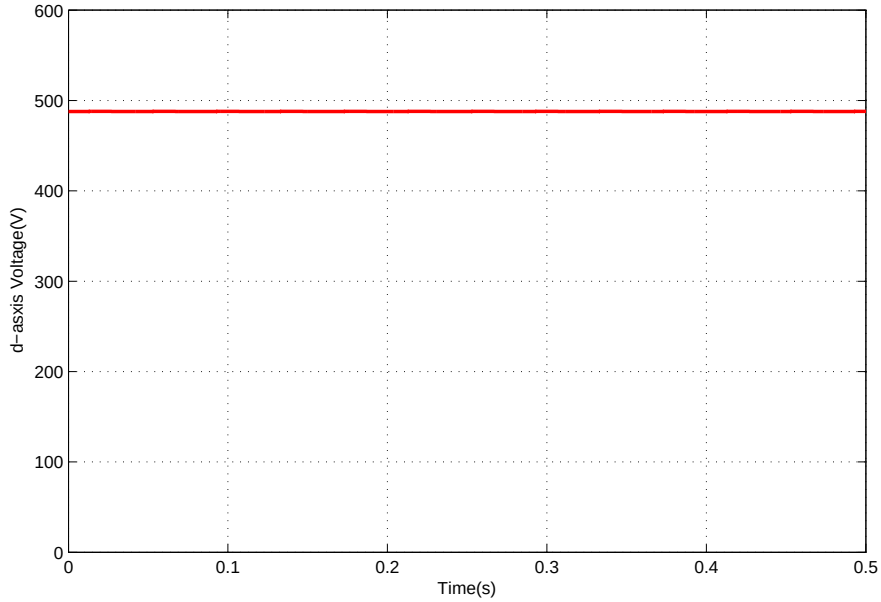

Figure 4.10: d-axis component of source voltage. *(Scale: X-axis: 100 msec/div, Y-axis: 1 V/div)*

Fig.4.10 shows the simulated d-axis voltage V_{sd}.

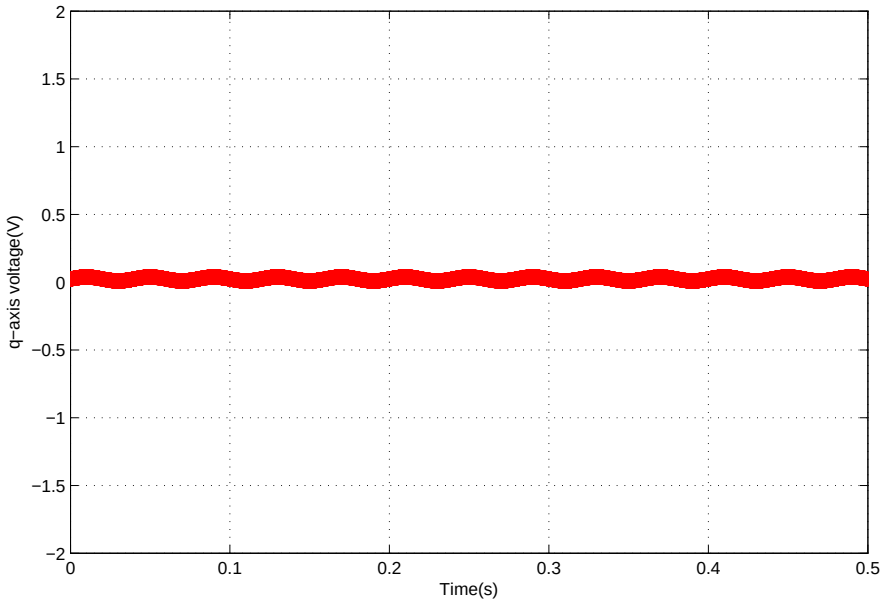

Figure 4.11: q-axis component of source voltage. *(Scale: X-axis: 100 msec/div, Y-axis: 1 V/div)*

Fig.4.11 shows the simulated q-axis voltage V_{sq}. Since V_{sd} is aligned with R- phase voltage V_{sq} is zero.

4.2 Hardware Results

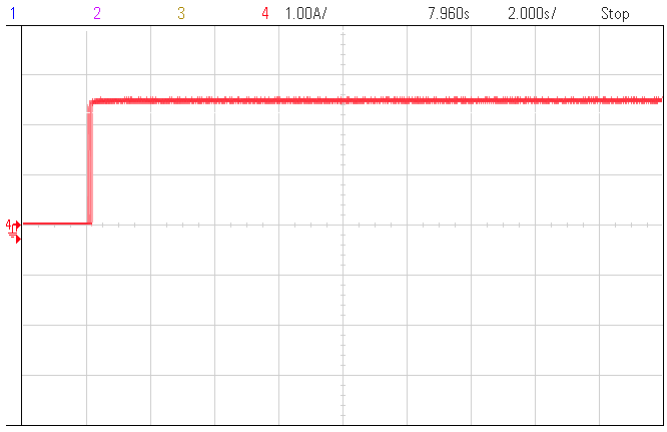

Figure 4.12: DC link current including transients. *(Scale: X-axis: 2 sec/div, Y-axis: 1 A/div)*

Fig 4.12 shows the hardware result of controlled DC link current. The reference current is given at 2.5 A and the controller is able to track the reference DC link current value.

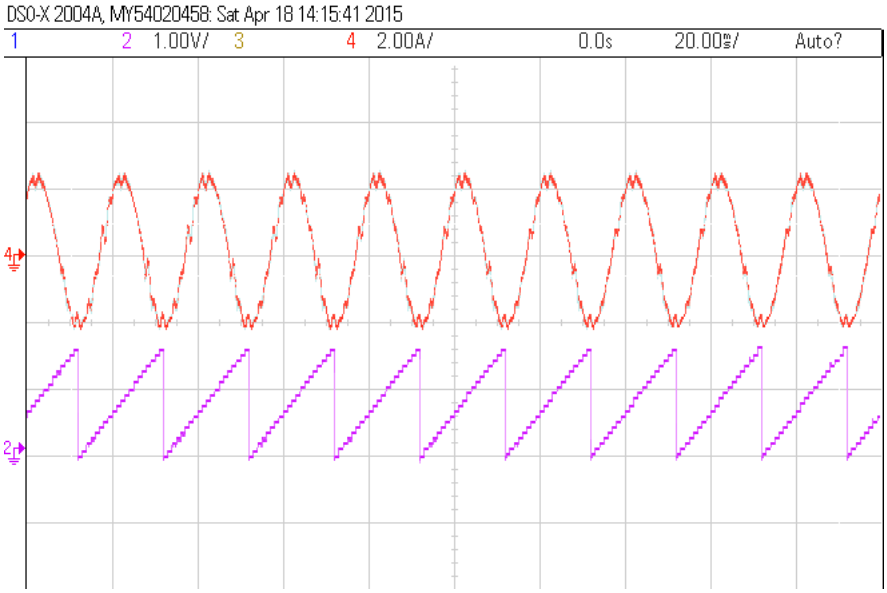

Figure 4.13: Steady state R phase line current. *(Scale: X-axis: 20 msec/div, Y-axis: 1 A/div(brown) and 1 V/div(blue))*

Fig.4.13 shows the hardware result of R phase line current along with phase information from PLL. The line current is almost sinusoidal in shape. The saw tooth waveform is the phase angle information from PLL. It is important to note that the harmonic currents are absent in the line current due to presence of capacitive filter.

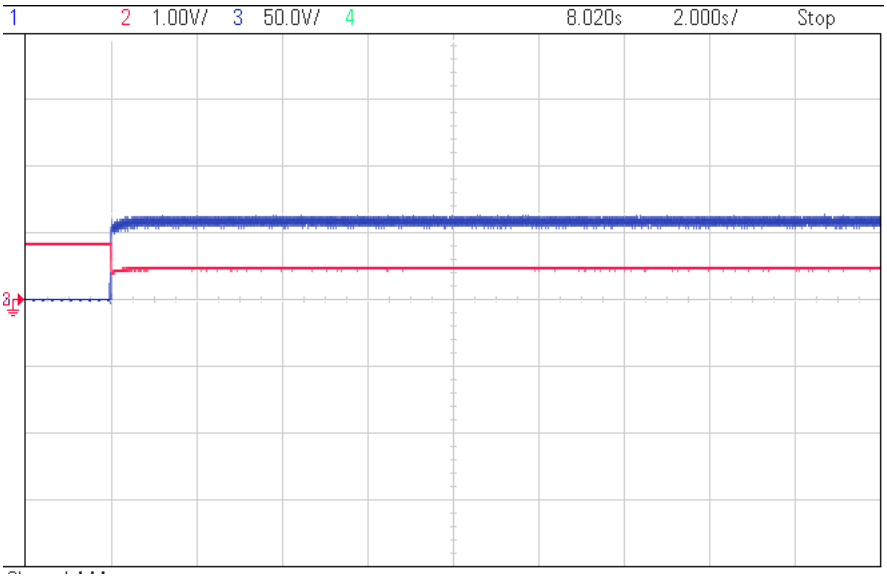

Figure 4.14: d-axis reference current from controller output and DC link current. *(Scale: X-axis: 20 msec/div, Y-axis: 1 A/div(brown) and 1 V/div(blue))*

Fig.4.14 shows the hardware result of I_{sd}^{*} compared with DC link current with transients. Initially I_{sd}^{*} is very high to charge the DC link inductor and once it is done I_{sd}^{*} is supplying only real power demand.

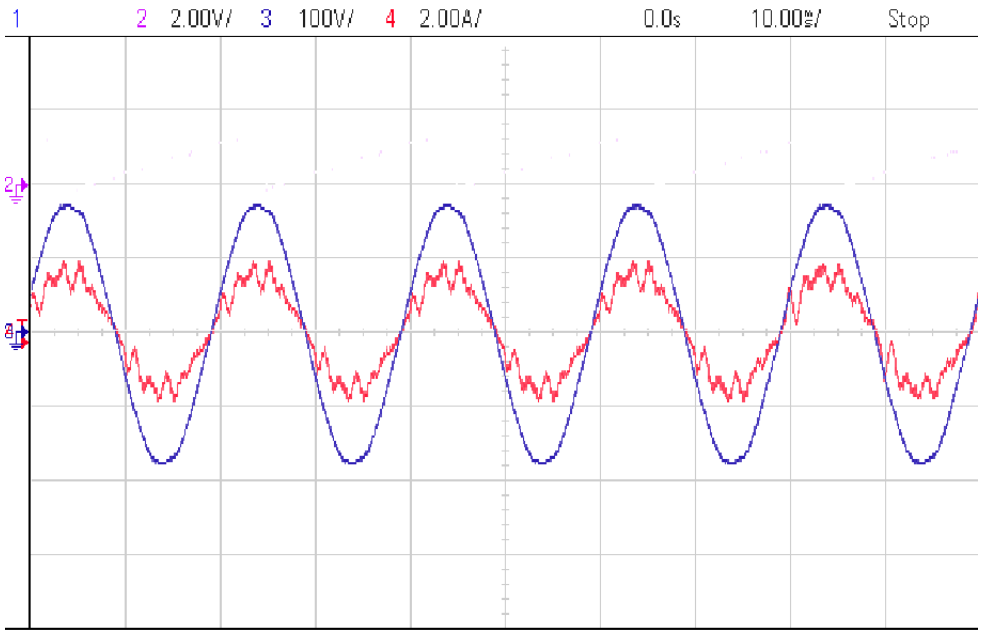

Figure 4.15: R phase voltage(blue) and current(red). *(Scale: X-axis: 10 msec/div, Y-axis: 2 A/div(red) and 100 V/div(blue))*

Fig.4.15 shows the R phase voltage and current together. Since the q-axis reference current I_{sq}^{*} is given zero there is no phase difference between voltage and current. It implies that converter is operating at unity power factor.

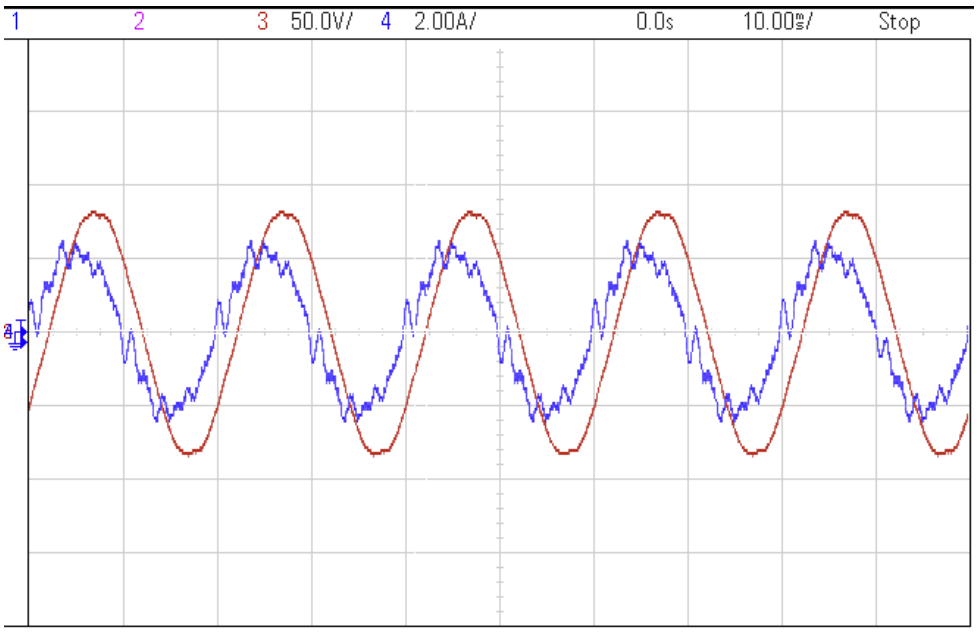

Figure 4.16: R phase voltage(brown) and current(blue). *(Scale: X-axis: 10 msec/div, Y-axis: 2 A/div(red) and 50 V/div(blue))*

Fig 4.16 shows the R phase current and voltage. Since the q-axis reference current I_{sq}^{*} is given some value there is a phase difference between voltage current in which current is leading. It implies to a leading power factor.

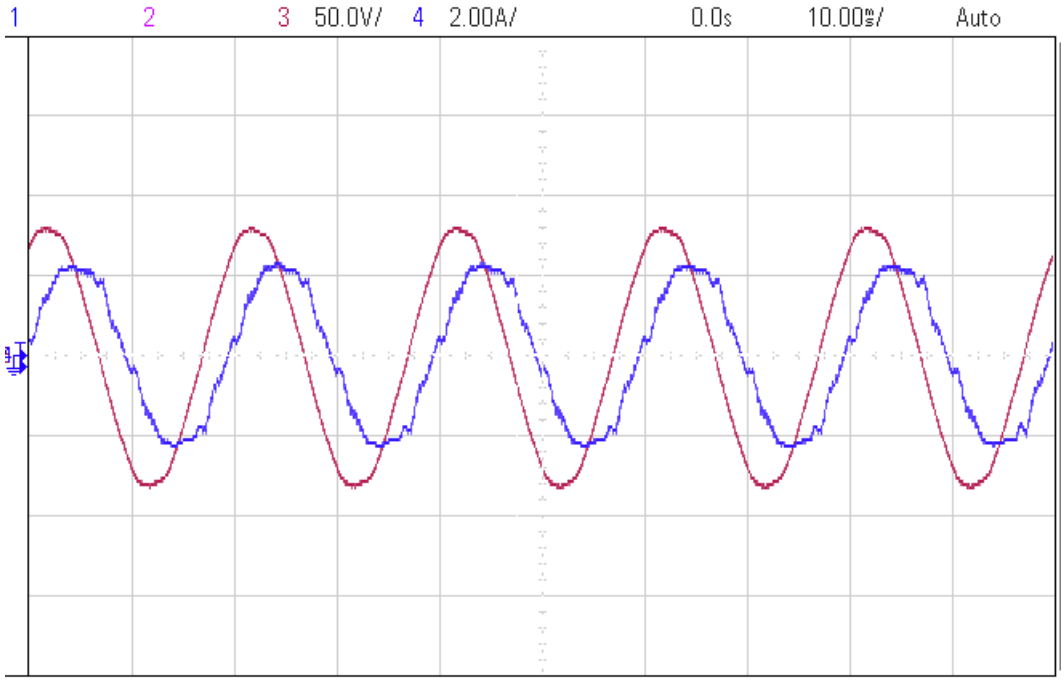

Figure 4.17: R phase voltage(brown) and current(blue). *(Scale: X-axis: 10 msec/div, Y-axis: 5 A/div(red) and 100 V/div(blue))*

Fig.4.17 shows the R phase current and voltage. Since the q-axis reference current I_{sq}^{*} is given some value there is a phase difference between voltage current in which current is lagging. It implies to a lagging power factor.

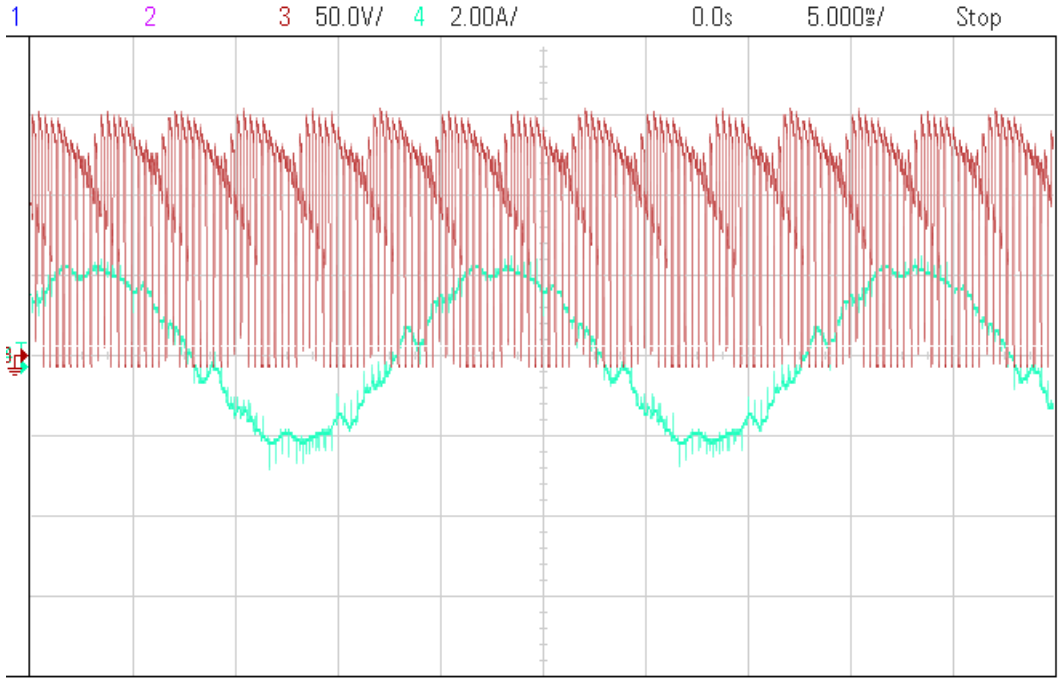

Figure 4.18: Rectifier voltage(brown) on DC side with R phase line current(green) *(Scale: X-axis: 10 msec/div, Y-axis: 2 A/div(red) and 50 V/div(blue))*

Fig.4.18 shows the rectifier voltage on DC side. Also the R phase line current is shown(green).

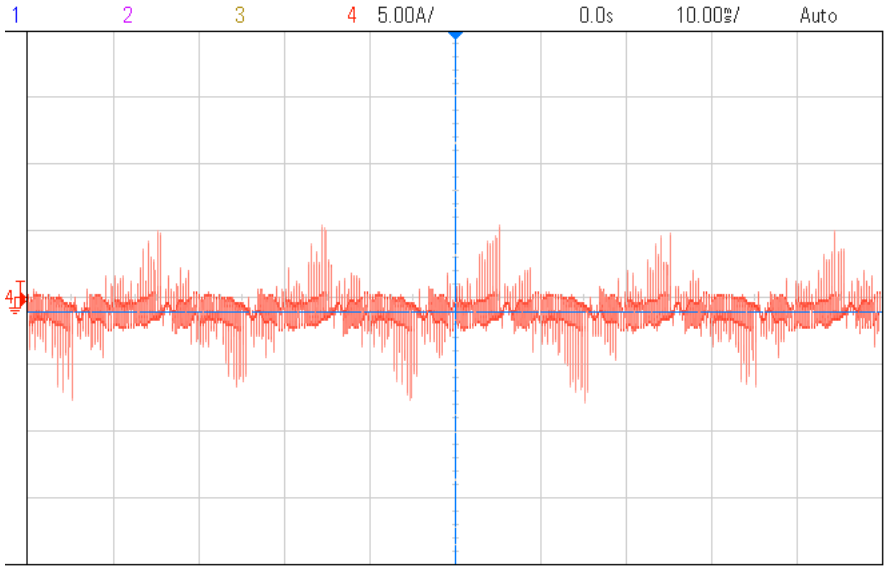

Figure 4.19: Current through filter capacitors. *(Scale: X-axis: 10 msec/div, Y-axis: 5 A/div)*

Fig.4.19 shows the filter current through capacitors. It contains high frequency harmonic currents.

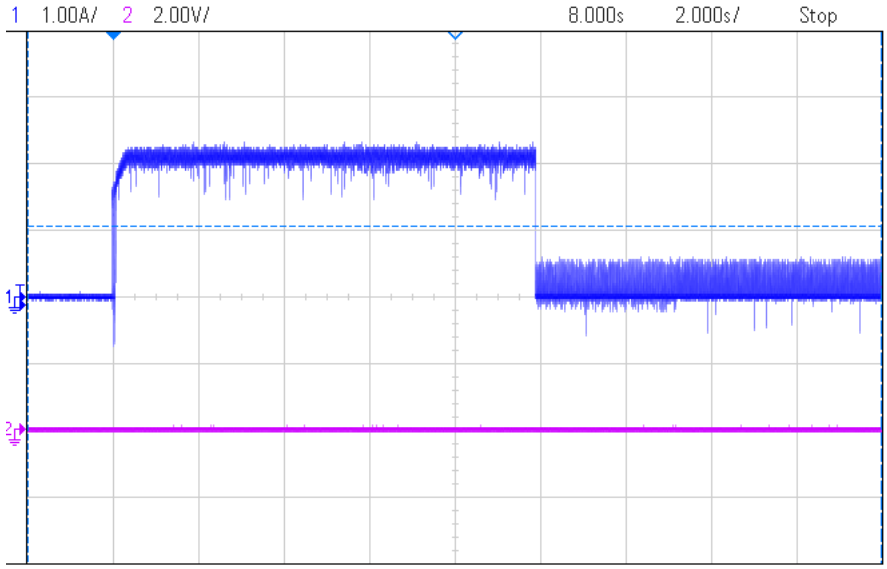

Figure 4.20: DC link current at phase-back mode. *(Scale: X-axis: 2 sec/div, Y-axis: 2 A/div)*

Fig.4.20 shows the DC link current suddenly shifting into phase back mode. The control system of PWM CSR is designed in such a way that when a fault occurred in the system, the rectifier has to go into phase back mode i.e. power flow should be in reverse direction. So in this kind of mode the DC link current reduces to zero.

4.3 Conclusion

The simulation and hardware results are presented in this chapter. A new control method is proposed and implemented in both simulation and hardware. The results obtained by simulation and hardware validates the proposed control technique. The DC link current shown in the hardware result can be much smoother if a DC choke inductance of high value is used. The phase back mode of the rectifier is tested when fault is occurred in the system and the hardware result is presented. Finally the experimental results are close to simulation waveforms. The summary of the entire report and the future scope of the work is discussed in next chapter.

CHAPTER 5

Conclusion

5.1 Summary of the present work

The proposed control technique for PWM CSR is successfully implemented in both simulation and hardware. The experimental and simulation results validates the proposed control technique. For the proposed control technique proper theoretical analysis is presented. The objectives of control method like DC link current control, sinusoidal line currents and reactive power control are obtained in both simulation and hardware. Also $\alpha\beta$ PLL with low pass filters was implemented. The hardware setup is tested for each part separately and also the entire setup before implementing the control method. When a fault occurred in the system the direction of power flow is reversed(phase back mode), so that the DC link current reduces to zero and load connected to CSR gets protection.

5.2 Future Scope of Work

The PWM CSR is tested with a resistive load. This project can be extended by connecting to CSI fed drive. PWM CSR acts as front end converter to CSI fed drive.

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