POWER QUALITY IMPROVEMENT IN POWER DISTRIBUTION SYSTEM

A Project Report

submitted by

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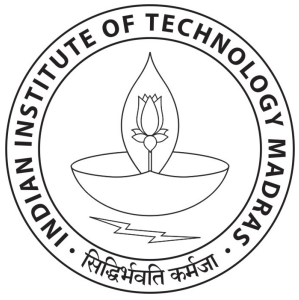
in partial fulfilment of the requirements
for the award of the degree of

MASTER OF TECHNOLOGY



DEPARTMENT OF ELECTRICAL ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY MADRAS.

JUNE 2018

THESIS CERTIFICATE

This is to certify that the thesis entitled **" POWER QUALITY IMPROVEMENT IN POWER DISTRIBUTION SYSTEM "** submitted by **K CHAKRADHAR** to the Indian Institute of Technology, Madras for the award of the degree of Master of Technology is a bona fide record of the research work done by him under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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Date: 14/6/18

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ACKNOWLEDGEMENTS

I am heartily thankful to my guide, Prof. Mahesh Kumar, whose encouragement, guidance and support through out my research work enabled me to develop an understanding of the subject. I consider myself quite privileged to work under his supervision. I appreciate his sincere help in terms of contributions of time, ideas so as to make my working experience stimulating and productive. I would like to acknowledge the financial, academic and technical support of the Indian Institute of Technology Madras.

I am grateful to my friends who has contributed immensely to my personal and professional life in my period of institute. I am extremely thankful for the support of my lab mates in the power quality laboratory during the project.

Above all, I am very grateful to the support and encouragement provided by my parents and family members. They have always stood beside and supported me during ups and downs in my life. What small or big things, I have achieved today and will be achieving in future, are because of their encouragement and blessings.

I take this opportunity to acknowledge my heartfelt gratitude to all those people who directly or indirectly helped me to carry out this research work successfully.

K Chakradhar

ABSTRACT

Power quality (PQ) has become a major concern with the wide application of power electronic loads in distribution system. These loads result in power quality problems like harmonic distortion in utility source currents, excessive neutral current, poor utility power factor, voltage harmonics, voltage unbalance and interference with communication systems. To avoid these problems passive filters were used but, due to their inability of solving all the power quality issues, customs power devices (CPDs) have emerged as reliable technology. Distribution Static Compensator (DSTATCOM) and Dynamic voltage restorer (DVR) are popular CPDs used to mitigate current and voltage related power quality issues.

DSTATCOM is a shunt connected active power filter, which is used to overcome current related PQ problems. It is connected at point of common coupling (PCC) to supply harmonic, reactive components of load currents and also provide neutral current compensation. This makes the source currents balanced and sinusoidal with Unity Power Factor (UPF) operation.

DVR is a series connected active power filter (APF), used to mitigate voltage related power quality problems. When connected to power system at PCC, DVR maintains load voltage constant by injecting appropriate voltage under voltage disturbance.

The work presented in the thesis deals with topologies of voltage source inverter (VSI), theories for generation of reference signals and current/voltage controllers for generation of switching pulses. Instantaneous reactive power theory and instantaneous symmetrical component theory used for reference currents generation for DSTATCOM are analyzed. For DVR, reference voltages generation schemes like in-phase compensation, pre-sag compensation, etc. are investigated. Switching control schemes are presented with their merits and demerits. Simulation studies are performed in MATLAB/Simulink environment to validate different reference signal algorithms.

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ABBREVIATIONS

AC	Alternating Current
APF	Active Power Filter
CCM	Current Control Mode
CPD	Custom Power Device
CSI	Current Source Inverter
DC	Direct Current
DSTATCOM	Distribution Static Compensator
DVR	Dynamic Voltage Restorer
IEEE	Institute of Electrical and Electronics Engineers
IGBT	Insulated Gate Bipolar Transistor
MAF	Moving Average Filter
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MTTF	Mean Time To Failure
PCC	Point of Common Coupling
PI	Proportional Integral
PLL	Phase Locked Loop
PQ	Power Quality
PWM	Pulse Width Modulation
RMS	Root Mean Square
SRF	Synchronous Reference Frame
SPWM	Sinusoidal Pulse Width Modulation
SSTS	Solid State Transfer Switch
SVM	Space Vector Modulation
THD	Total Harmonic Distortion
UPQC	Unified Power Quality Conditioner
VCM	Voltage Control Mode
VSI	Voltage Source Inverter

NOTATIONS

C_{dc1}, C_{dc2}	DC storage capacitances
C_f	Shunt capacitor value
f_{sw}	Switching frequency
h	Width of the hysteresis band
i_{la}, i_{lb}, i_{lc}	Instantaneous load currents in phase-a, b and c respectively
$i(t)$	Instantaneous current
i_{fa}, i_{fb}, i_{fc}	Instantaneous injected DSTATCOM filter currents in phase-a, b and c respectively
i^*_{fa}, i^*_{fb}, i^*_{fc}	Reference DSTATCOM filter currents in phase-a, b and c respectively
i_{sa}, i_{sb}, i_{sc}	Instantaneous source currents in phase-a, b and c respectively
i_α, i_β, i_0	Currents in $\alpha\beta 0$ reference frame
i_{fd}, i_{fq}, i_{f0}	Actual filter currents in $dq0$ reference frame
i^*_{fd}, i^*_{fq}, i^*_{f0}	Reference filter currents in $dq0$ reference frame
L_f	Value of the interfacing inductance
P_{lavg}	Average load power
P_{loss}	Loss in compensator
R_f	Value of the interfacing resistance
S_a, S_b, S_c	Switching pulses of the VSI top switches in phase-a, b and c respectively
S'_a, S'_b, S'_c	Switching pulses of the VSI bottom switches in phase-a, b and c respectively
V	rms voltage
$v(t)$	Instantaneous voltage
V_{dc1}, V_{dc2}	DC voltage of across capacitors C_{dc1} and C_{dc2}, respectively
v_{la}, v_{lb}, v_{lc}	Instantaneous load voltages in phase-a, b and c respectively
V_{lrms}	RMS value of line voltage
v_{sa}, v_{sb}, v_{sc}	Instantaneous source voltages in phase-a, b and c respectively
v_{ta}, v_{tb}, v_{tc}	Instantaneous terminal voltages in phase-a, b and c respectively
v_α, v_β, v_0	Voltages in $\alpha\beta 0$ reference frame

CHAPTER 1

INTRODUCTION

According to IEEE, Power quality (PQ) is the concept of powering and grounding sensitive equipment in order to protect the sensitive equipment as well as source of electric power from the disturbances. In simpler words, power quality is the combination of voltage quality and current quality. It can be stated that the power quality is good, when steady state supply voltage/current within the prescribed range, frequency close to the rated value, and smooth voltage/current waveforms (which are sinusoidal). In the recent years, the quality and reliability of power supply in distribution system is becoming a growing concern due to increased use of power electronic based equipment like computer related loads, rectifier loads, consumer electronic appliances, adjustable speed motor drives. This semiconductor devices play an important role in development of efficient and sustainable technology for power conversion and power conditioning but they introduce nonlinear characteristics which causes contamination to voltage and current waveforms at the point of common coupling (PCC) which is a matter of great concern for utility and consumer. This non-linearity along with unbalance and reactive loads have aggravated power quality problems on almost every part of the network directly or indirectly. They cause excessive neutral currents, overheating of electrical apparatus, poor power factor, voltage distortion and interference with communication systems [1]–[3]. Some of the reasons for power quality problems are:

- Faults and failure of switching operations which may result in dips, interruptions and transients
- Disturbances from loads that result in flicker, harmonics and phase imbalance
- More usage of non-linear loads resulting in higher reactive power oscillations.

1.1 Various Power Quality Issues

In general, an electrical utility is expected to maintain balanced voltages at consumer end. Similarly, consumer is expected to draw balanced current from source. Any deviation in voltage and current waveforms causes a power quality Issue. Power quality

issues manifest themselves in different forms at PCC. Broadly, these can be classified as following:

- Voltage/current unbalance
- Voltage/current distortion
- Voltage sag and swell
- Voltage fluctuations
- Power-frequency variation

Definitions of above presented issues from IEEE std. 519-1992 [4] and IEEE std. 1159-2009 [5] are mentioned and brief explanation have been provided below.

1.1.1 Voltage/Current Unbalance

Voltage/current unbalance in a three-phase system is defined if the root mean square (RMS) values of the voltages and phase angles between two consecutive phases are not equal. The severity of the unbalance in a three-phase system can be expressed as ratio of negative sequence component to the positive sequence component. The ratio is usually expressed as a percentage [1]. The major source unbalance in a power system network is due to different loads in three phases. This can be due to uneven spread of single-phase loads over the three phases. Unbalance also leads to additional production of heat in windings of induction and synchronous machines. This causes downfall of efficiency and derating of the machine.

1.1.2 Voltage/Current Distortion

In general waveform should be sinusoidal but this may not always be sinusoidal due to the presence of harmonics. This results in voltage distortion. This distortion is caused mainly by two factors. The first one is the generated source voltages is not sinusoidal. This can happen due to small deviations from the ideal shape of machine resulting a small amount of harmonics at the generation. The second factor is voltage distortion at PCC. This happens because of combination of linear and non-linear loads therefore the total current drawn from supply is distorted and as a result, the drop across source

impedance will be non-linear and voltage at terminal bus will be distorted. Because of this distorted voltage, linear load connected through PCC bus will also get affected. The classical example is the power transformer, where the non-linearity is due to saturation of the magnetic flux in the iron core of transformer. The amount of harmonics generated by power system is considerably low but extensive usage of electronics increase harmonics in the power system. Broad applications of adjustable speed drives also contributes to voltage distortion in power systems.

1.1.3 Voltage Sag and Swell

Voltage sag/swell is a sudden decrease/increase in the RMS voltage at any point in an electrical system for a duration ranging from half cycle to a maximum of one minute. The principal cause for voltage sag is a short term increase in current usually appearing during the starting of a motor, energizing of a transformer and faults on high voltage side or low voltage side of transmission lines (mostly due to line-ground fault). Voltage swell results from sudden reduction in load or switching of capacitor banks. A prolonged and excessive swell can be dangerous to power transformer as it can enter into saturation region and get subjected to high electromagnetic stress.

1.1.4 Voltage Fluctuations

Voltage fluctuations can be defined as a series of voltage changes or a cyclic variation of the voltage envelope. These occur due to continuous and rapid variations in the current magnitudes of loads. With variation of voltage, power flow also varies. Beyond 10 Hz frequency, human eye becomes sensitive to the fluctuation, which can be disturbing.

1.1.5 Power Frequency Variation

Power frequency variation is deviation from fundamental frequency, or from its specified nominal value. This term often referred to as voltage frequency variation. This happens due to unbalance between load and generation. At any instant, frequency depends on the balance between load and capacity of available generation. The size of frequency shift and its duration depend on the load characteristics and response of gen-

eration system to load changes.

1.2 Measures to Enhance Power Quality

Different schemes for mitigating power quality issues have evolved in literature. To reduce the PQ issues conventionally, passive filters are used for compensation. Passive filters consist of inductors and capacitors which are tuned for a particular frequency. For elimination of multiple harmonic components separate filters are installed for each harmonic frequency. Even though they are simple in operation, low cost and high efficiency, these filters include disadvantages of bulk in size, need of high rating and they often require coordination with reactive power requirements and harmonics of the loads. In principle, these passive filters filtering characteristics are determined by impedance ratio of source and the filter [6]. The source impedance which varies with the system configuration, strongly influences the passive filters operation. Passive filters are not suitable for real time management as these are firmly fixed at particular location in the system and neither size of filter nor tuned frequency can be changed so easily. To overcome the above problems, a viable solution has been proposed with Active Power Filters (APFs). When proposed, the technology was unable to mitigate the same, but due to the rapid advancements in power and semiconductor technology has enabled practical realization of APFs. The active power filters employed in power distribution systems are referred to as Custom Power Devices (CPDs). Popular CPDs are Distribution Static Compensator (DSTATCOM), Dynamic Voltage Restorer (DVR), etc.

1.3 Motivation and Objectives

In many AC distribution systems due to more sensitive loads users continue to demand high power quality. On the other hand loads which are responsible for power quality issues have become numerous. This has more impact on critical loads and rating of power system. Therefore, compensatory techniques to alleviate these issues need to be analyzed. Realization of DSTATCOM involves mostly three major important aspects. First one is selection of suitable Voltage Source Inverter (VSI) topologies based on load and network configuration. Second part is generation of filter currents to be injected at PCC to ensure that current from source is balanced and sinusoidal. Third one is devel-

opment of current control strategy for VSI in order to generate desired filter currents. Merits and demerits of these topologies are studied. Comparisons of current generation techniques of DSTATCOM need to be analyzed. The dynamic voltage restorer (DVR) is a series APF which is designed to correct voltage sag and swell. The performance of DVR is mainly dependent on voltage control strategy. The drawbacks during transient responses are studied and it was concluded that a simple closed loop control technique has a better transient response and easy to implement. The control schemes are studied and analyzed. The objectives of the work are:

- Algorithm for generating reference filter currents/voltages to obtain desired source currents and load voltages
- To maintain DC link capacitor voltage for better performance of VSI
- A control strategy requirement for generating pulses to VSI
- Structure and operation of DSTATCOM and DVR need to be investigated
- To achieve proper shaping of voltage/current while injecting at PCC, interface filters plays an important aspect which should be explored further

1.4 Organization of Thesis

Chapter 1 describes various power quality effects on loads and power distribution system and need for improvement. Various power quality events are described individually. Mitigating techniques using passive filters and active power filters are introduced.

Chapter 2 is a description of CPDs and their role in mitigating power quality issues. It provides a literature survey of various custom power devices, active filter topologies and fundamental principles of the working of the same.

Chapter 3 presents various algorithms for generating reference currents and voltages of these CPDs. These generated waveforms are injected into power system at load terminal with filters. In this chapter DSTATCOM is operated in current control mode for current compensation and DVR for voltage compensation. Detailed simulation results are illustrated.

Chapter 4 presents conclusions of the work done and scope for future work is outlined.

CHAPTER 2

LITERATURE SURVEY

As custom power devices were introduced in the earlier chapter to mitigate power quality issues, detailed descriptions of these devices are provided and studied in this chapter. The emergence of these CPDs has been documented in literature. Custom power devices are a group of devices, which compensate current-voltage related PQ problems. These custom power devices generally include components like a power inverter, energy storage devices (capacitors, inductors, etc.), interface filter parameters, master control module which ensures control and distribution of high quality power to consumers. Popular CPDs are distribution static compensator (DSTATCOM), dynamic voltage restorer (DVR), Unified power quality conditioner (UPQC), solid state transformer switch (SSTS) and solid-state fault current limiter (SSFCL) [7]–[9]. Brief description and role of some of these CPDs are presented in the following sections.

2.1 Distribution Static Compensator (DSTATCOM)

DSTATCOM is a shunt custom power device connected in power system distribution network for mitigation of current related problems. The major functions of this device are compensating reactive power, absorbing harmonic components and compensating voltage sag. Generally this device is supported by short-term energy stored in a DC capacitor. When a load is applied, it can generate compensatory currents to meet load requirements. In literature, DSTATCOM presents various VSI topologies, different control techniques and various switching strategies for compensation. The general schematic of DSTATCOM connected to power system at PCC is displayed in Fig. 2.9

Source voltage (v_s) is compatible with both linear and non-linear loads, and in the absence of DSTATCOM source supplies both linear and non-linear current combined. The supplied source current (i_s) is similar to load current (i_l) is of non-sinusoidal, unbalanced and of low power factor. To avoid these hassles, DSTATCOM injects filter current (i_f) at load bus. The compensation makes source currents balanced and sinusoidal with unity power factor even though load is unbalanced and non-linear in nature.

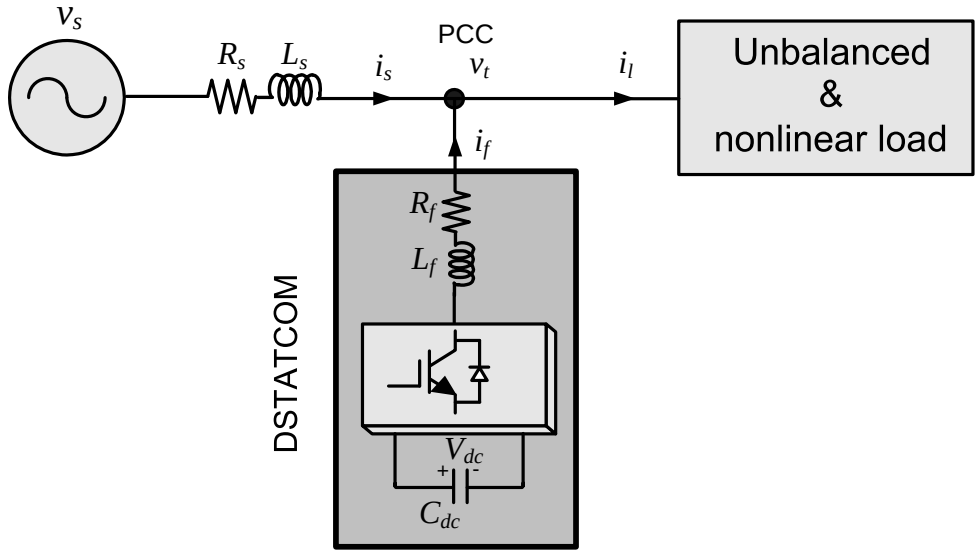

Fig. 2.1 Schematic diagram of DSTATCOM

The required compensating current i_f is injected using VSI through interfacing filter which has an inductance L_f and resistance R_f. The operation of VSI is assisted by DC storage capacitor C_{dc} with DC link voltage V_{dc} across it. Feeder impedance are represented by the inductor L_s and resistor R_s. DSTATCOM is a flexible PQ compensator as it can operate in Voltage Control Mode (VCM) or Current Control Mode (CCM).

2.1.1 DSTATCOM in Voltage Control Mode

Voltage at PCC can be distorted or unbalanced if the loads are nonlinear or unbalanced. As a result, PCC voltage deteriorates from ideal conditions. DSTATCOM, when operated in voltage control mode (VCM) injects an appropriate fundamental reactive current to maintain load voltage constant, balanced and sinusoidal during voltage disturbances like swell, sag, unbalance. The DSTATCOM can inject leading or lagging current based on the nature of disturbance at PCC. During decrease in source voltage (sag) DSTATCOM acts as a capacitive load and supplies reactive current into the source to improve load voltage. During increase in source voltage (swell) DSTATCOM acts like an inductive load and draws reactive current from the source to keep load voltage at a constant value. Therefore, DSTATCOM in voltage control mode injects either leading or lagging fundamental reactive current for maintaining load voltage constant during voltage pollution at PCC. The illustration of DSTATCOM in voltage control mode of three phase four wire neutral point clamped VSI topology connected in a distribution system is

shown in Fig. 2.2. In the above figure, v_{sa}, v_{sb} and v_{sc} are source voltages of phases

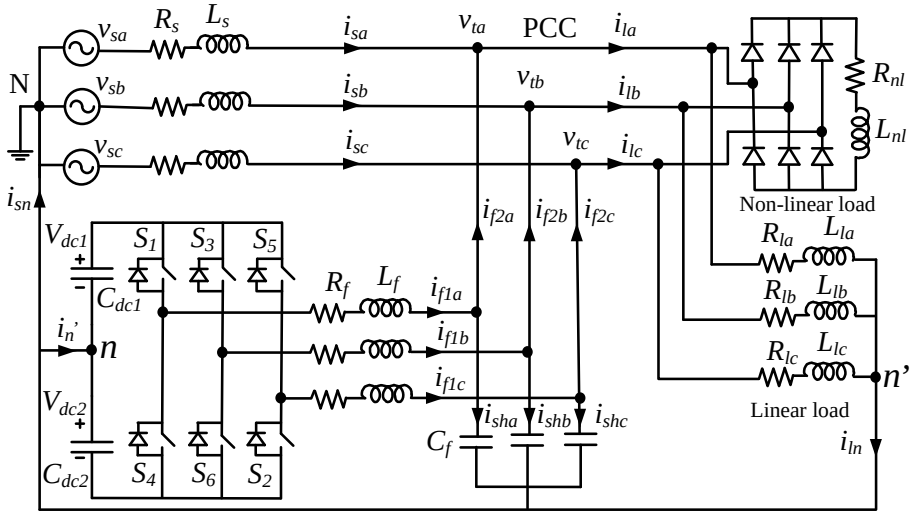

Fig. 2.2 Schematic for DSTATCOM in VCM operation.

a, b and c, respectively. Similarly, v_{ta}, v_{tb} and v_{tc} are load voltages at PCC. The loads, source, and compensator together are connected at the PCC. The source currents in three phase are represented by i_{sa}, i_{sb} and i_{sc}, load currents are represented by i_{la}, i_{lb} and i_{lc}. The VSI currents are denoted by i_{fla}, i_{flb} and i_{flc} in respective phases. The interfacing inductance and resistance of the shunt active filter are represented by L_f and R_f, respectively. The shunt capacitor C_f, connected at the load terminal, absorbs the higher switching harmonics present in the filter currents. Currents through the shunt capacitors are given by i_{sha}, i_{shb}, and i_{shc}. The dc link capacitance and voltages across them are represented by$C_{dc1} = C_{dc2} = C_{dc}$ and $V_{dc1} = V_{dc2} = V_{dc}$, respectively. The dc side capacitor serves mainly two purposes, it serves as an energy storage element to supply a real power difference between the load and source during the transient period. In steady state complete compensation is achieved but transient state response is slow when DSTATCOM is operated in VCM. In normal operation DSTATCOM has to operate in CCM but during faults VCM comes into operation.

2.1.2 DSTATCOM in Current Control Mode

The primary focus of DSTATCOM in current control mode is to mitigate current related problems. The objective of the compensator connected at PCC in current control mode is to correct the imbalances in source current by supplying harmonic current. The schematic shown in Fig. 2.3 is ideal current compensator with three-phase cur-

rent sources connected to system at PCC. However,a practical compensator is designed

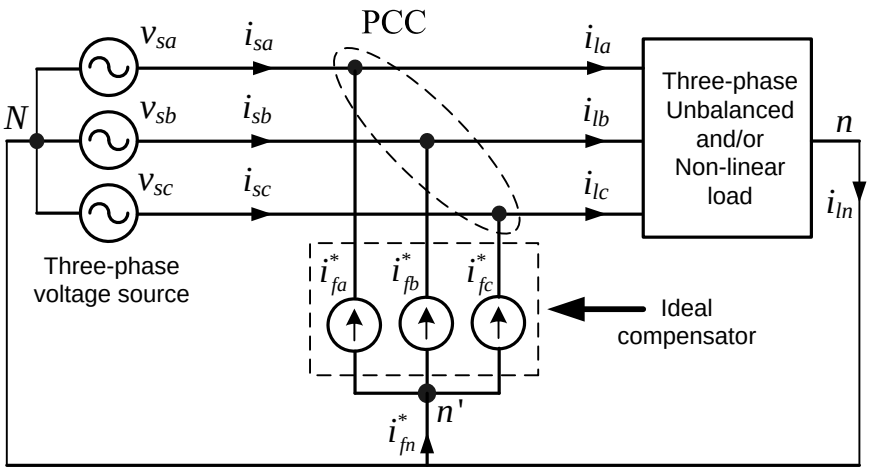

Fig. 2.3 Schematic of DSTATCOM acting as an ideal current compensator

using voltage source inverter operating in CCM through a suitable control method to realize these current sources. Elaborate description of custom power devices can be divided and studied as the following: VSI topologies, control theories for generation of reference quantities and switching control techniques for VSI.

2.1.3 Control Schemes for Generation of Reference Signals

Control of DSTATCOM deals with two major tasks, which are generation of reference quantities and determining these through voltage source inverter. Various theories for generation of reference currents are proposed in literature. Some of these theories are instantaneous reactive power theory, instantaneous symmetrical component theory, generalized instantaneous reactive power theory, synchronous reference theory. These theories are most commonly used for generation of reference components. Brief description of some of these theories are as follows

Instantaneous Reactive Power Theory

Instantaneous reactive power theory was proposed by Akagi et.al. in 1983-84 [10], [11] and it is also known as *pq* theory. This theory aims to develop a mathematical formulation for realization of reference compensator currents using powers present in load, reactive and harmonic powers. The reactive power can be compensated not only in steady state but also in transient conditions. The *pq* theory uses Clarke transfor-

mation to convert *abc* to mutually orthogonal $\alpha - \beta$ and inverse clarke transformation to convert $\alpha - \beta$ to *abc*. Definitions of instantaneous active and reactive powers after transformation are presented and discussed in this theory. Detailed explanation of instantaneous reactive power theory with simulation results is explained in next chapter.

Generalized Instantaneous Reactive Power Theory

Instantaneous reactive power theory was generalized for three phase systems by Peng and Lai [12]. It was done by considering zero sequence components to the active power and non-active power. Instead of decomposing the current components into alpha-beta orthogonal components, Power components were defined at first and then current is decomposed. The instantaneous phase voltages and currents are expressed as instantaneous space vectors.

$$\mathbf{v} = \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} ; \ \mathbf{i} = \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{2.1}$$

The instantaneous active power is defined as

$$\mathbf{p} = \mathbf{v}.\mathbf{i} = v_a i_a + v_b i_b + v_c i_c. \tag{2.2}$$

The instantaneous reactive power vector is defined as

$$\mathbf{q} = \mathbf{v} \times \mathbf{i} = \begin{bmatrix} q_a \\ q_b \\ q_c \end{bmatrix} = \begin{bmatrix} \begin{vmatrix} v_b & v_c \\ i_b & i_c \end{vmatrix} \\ \begin{vmatrix} v_c & v_a \\ i_c & i_a \end{vmatrix} \\ \begin{vmatrix} v_a & v_b \\ i_a & i_b \end{vmatrix} \end{bmatrix} \tag{2.3}$$

The instantaneous active current is defined as

$$\mathbf{i}_p = \begin{bmatrix} i_{ap} \\ i_{bp} \\ i_{cp} \end{bmatrix} = \frac{\mathbf{p}}{\mathbf{v}.\mathbf{v}}\,\mathbf{v}. \tag{2.4}$$

The instantaneous reactive current vector is defined as

$$\mathbf{i}_q = \begin{bmatrix} i_{aq} \\ i_{bq} \\ i_{cq} \end{bmatrix} = \frac{\mathbf{q}\times\mathbf{v}}{\mathbf{v}.\mathbf{v}}\,\mathbf{v}. \tag{2.5}$$

The active and reactive power defined on instantaneous basis is facing criticism as it is not possible to estimate the nature of the load with these two definitions [13].

Synchronous Reference Frame (SRF) Theory

Synchronous reference theory was introduced by R. H. Park in 1920s and is based on time domain reference signal estimation techniques. The cardinal structure of synchronous reference theory consists of direct $dq0$ and inverse $dq0$ park transformation. The reference frame transformation is formulated from a three-phase abc stationary system to the direct axis (d) and quadratic axis (q) rotating coordinate system [14]. Using park transformation three phase space vectors stationary coordinates are easily transformed into $dq0$ rotating frame coordinates as shown in below equations. Equation 2.6 is used for voltage transformation while equation 2.7 is used for current transformation.

$$\begin{bmatrix} v_{tq} \\ v_{td} \\ v_{t0} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} cos(\omega t) & cos(\omega t - 2\pi/3) & cos(\omega t + 2\pi/3) \\ sin(\omega t) & sin(\omega t - 2\pi/3) & sin(\omega t + 2\pi/3) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} v_{ta} \\ v_{tb} \\ v_{tc} \end{bmatrix} \tag{2.6}$$

$$\begin{bmatrix} i_{lq} \\ i_{ld} \\ i_{l0} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} cos(\omega t) & cos(\omega t - 2\pi/3) & cos(\omega t + 2\pi/3) \\ sin(\omega t) & sin(\omega t - 2\pi/3) & sin(\omega t + 2\pi/3) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} i_{la} \\ i_{lb} \\ i_{lc} \end{bmatrix} \tag{2.7}$$

The dq transformation output signals depends on the performance of the phase locked loop (PLL). The PLL circuit provides the rotational speed (rad/sec) of the rotating reference frame, where ωt is set as fundamental frequency component. The analysis of

the dq components and appropriate filtering can support the generation of the filter current references as required by the control. The dq components consist of DC and AC components as given below.

$$\begin{aligned} i_{ld} &= \bar{i}_{ld} + \tilde{i}_{ld} \\ i_{lq} &= \bar{i}_{lq} + \tilde{i}_{lq} \end{aligned} \tag{2.8}$$

The DC components $\bar{i}_{ld}$ and $\bar{i}_{lq}$ correspond to the fundamental positive sequence load currents and the AC components $\tilde{i}_{ld}$ and $\tilde{i}_{lq}$ correspond to the load currents harmonics. Component $\bar{i}_{lq}$ corresponds to the reactive power drawn by the load. The reference for the compensator can be obtained as follows

$$\begin{aligned} i^*_{fd} &= \tilde{i}_{ld} \\ i^*_{fq} &= \bar{i}_{lq} + \tilde{i}_{lq} \\ i^*_{f0} &= i_{l0} \end{aligned} \tag{2.9}$$

The compensator references in abc reference frame are obtained using inverse Park transformation as given below

$$\begin{bmatrix} i^*_{fa} \\ i^*_{fb} \\ i^*_{fc} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} cos(\omega t) & sin(\omega t) & \frac{1}{\sqrt{2}} \\ cos(\omega t - 2\pi/3) & sin(\omega t - 2\pi/3) & \frac{1}{\sqrt{2}} \\ cos(\omega t + 2\pi/3) & sin(\omega t + 2\pi/3) & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} i^*_{fq} \\ i^*_{fd} \\ i^*_{f0} \end{bmatrix} \tag{2.10}$$

The calculation of reference filter currents using SRF theory is simple, which involves direct Park transformation from abc to $dq0$ coordinates system and dealing with only DC quantities in $dq0$ frame. However, a proper PLL circuit is required in this method to obtain the transformation angle (ωt) information from the three phase supply voltages.

Instantaneous Symmetrical Component Theory

The theory of instantaneous symmetrical components can be used for load balancing, harmonic suppression and power factor correction [15]. Control algorithm of this theory can compensate any kind of unbalance and harmonic in the load. The compensation is done with high bandwidth current sources to track the filter reference currents. According to this theory any three phase instantaneous quantities can be expressed into

positive, negative and zero sequence

Out of various theories,the instantaneous symmetrical component theory with extraction of fundamental positive sequence components is simple in formulation. In addition to this, compactness of the control algorithm, flexibility to work under circumstances and computational efficiency make this scheme a very attractive choice and hence can be used for reference filter current generation for DSTATCOM.

2.2 Various VSI Topologies for CPDs

In DSTATCOM applications, VSI are used to track generated reference currents. Current source inverters (CSI) can also be used instead of VSI. But, due to bulky DC inductors, high dc link losses, requirement of voltage clamp circuit and reduced efficiency at normal operating point VSIs are prefereed over CSIs. Also, mean time to failure (MTTF), which is considered important in industrial applications is really low in case of CSI. The insulated gate bipolar transistor (IGBT) used in VSI has an inherent freewheeling diode to allow current flow in reverse direction of switch current and are cost effective when compared to IGBTs in CSI. Various VSI topologies are presented in literature [16], [17] . Some of the VSI topologies for DSTATCOM and DVR application are described below. The common notations used in these topologies and figures are v_{sa}, v_{sb} and v_{sc} represents source voltages of phases a, b and c respectively. Similarly, v_{ta}, v_{tb} and v_{tc} are the terminal voltages . The source currents in three phase are represented by i_{sa}, i_{sb} and i_{sc}, load currents are represented by i_{la}, i_{lb} and i_{lc}. The DSTATCOM injected filter currents are denoted by i_{fa}, i_{fb} and i_{fc}. The interfacing inductance and resistance of the active filter are represented by L_f and R_f respectively. The load constituted of both linear and nonlinear loads as shown in these figures. The DC link capacitor capacitance and voltage across it are represented by C_{dc} and V_{dc} respectively.

2.2.1 Three phase Three leg topology

This topology consists of six switches each with an anti-parallel diode and a single DC storage capacitor. It has a disadvantage of not able to compensate zero sequence currents in the load. Hence these currents flow in the neutral wire $(n-N)$ between

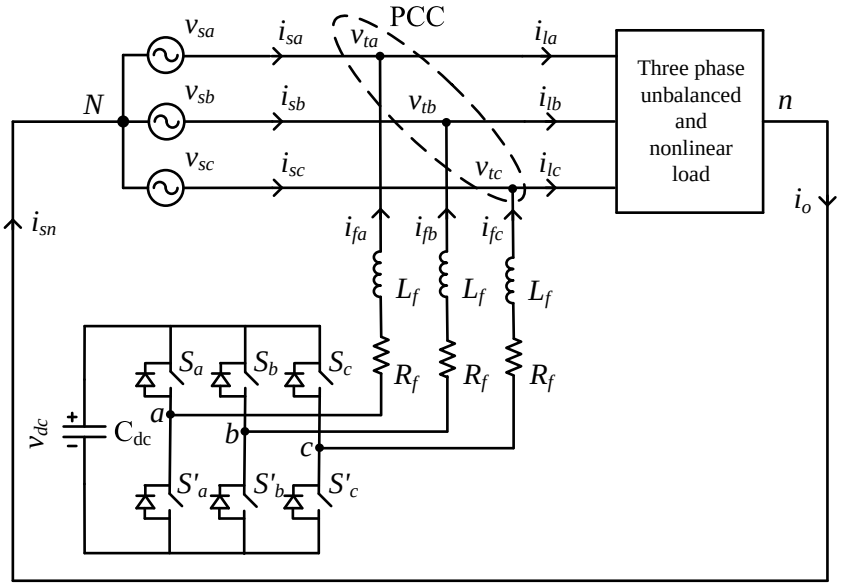

Fig. 2.4 Schematic diagram of three phase three leg VSI topology

the load and the system degrading power quality. The generation of the three compensator currents is not independent. Hence, this scheme is not suitable for three phase four wire distribution system with load currents containing zero sequence components. Schematic of this compensator is shown in Fig. 2.4.

2.2.2 Neutral Clamped VSI Topology

Neutral clamped voltage source inverter has six switches, each with an anti-parallel diode, two DC storage capacitors,and the junction of the two capacitors is connected to the neutral of the load as shown in Fig. 2.5. It is also known as split capacitor topology. Unlike the above topology, the neutral clamp at the junction of capacitors allows the path for zero sequence current and three injected currents at PCC can be independently controlled. The zero-sequence component of load current is circulated between load and DSTATCOM. This topology is equipped to compensate DC components of the load too, but due to the presence of DC component in VSI, the two DC capacitors are charged to different voltages. Hence the major challenge of this topology is balancing of the DC link voltage across two capacitors. However, this is rectified using a proportional-integral (PI) voltage control loop. This voltage unbalance is quite less when zero sequence current on the neutral has only AC components. But, when load demands any DC component, injection of this DC component current through capacitors effects charging one of the capacitors below its reference value and discharging the

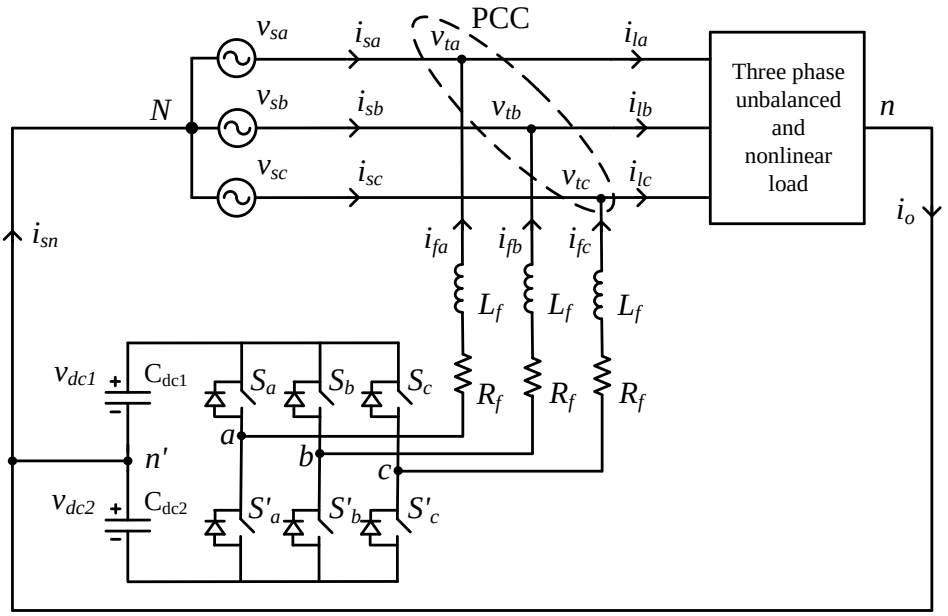

Fig. 2.5 Schematic diagram of three phase neutral clamped VSI topology

other above the reference value. Hence apart from applying dangerously high voltages across some of the switches, VSI loses its tracking ability, therefore degrading the performance of the compensator.This topology is the best choice in a distribution system because of its independent control, less number of switches and no transformer.

2.2.3 Three Phase H-Bridge VSI Topology

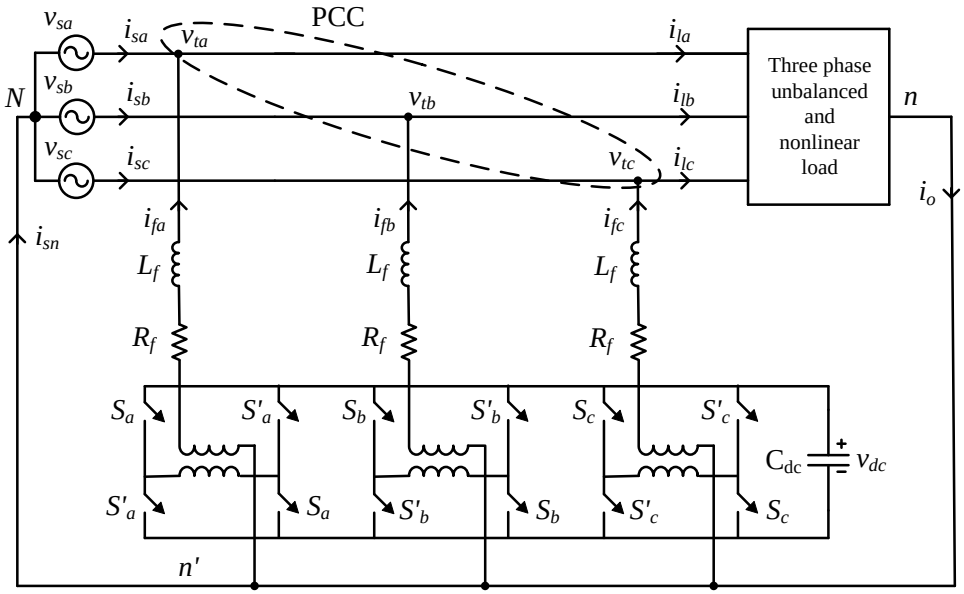

Fig. 2.6 Schematic diagram of three phase H bridge topology

This topology contains three H-bridge inverters that are connected to a common DC

storage capacitor. The schematic of this topology is shown in Fig. 2.6. Each switch shown in the figure is the combination of a power semiconductor device and an anti-parallel diode. This topology is realized by three interfacing transformers and three H-bridge inverters. VSI connected at PCC injects filter currents which are independent of each other. This interfacing transformer not only provides isolation between inverter legs but also prevents DC capacitor from getting shorted during the operation of switches in different legs. The output terminals of the transformer have the flexibility to compensate star connected load or delta connected load by connecting the terminals in star or delta. Due to the presence of transformers, if load draws any DC component this topology fails to compensate, because the DC component current saturates the transformers causing heating and increased losses thereby reducing their life. Another drawback is more switching losses in VSI as this uses more number of switches compared to other topologies.

2.2.4 Three phase Four leg Topology

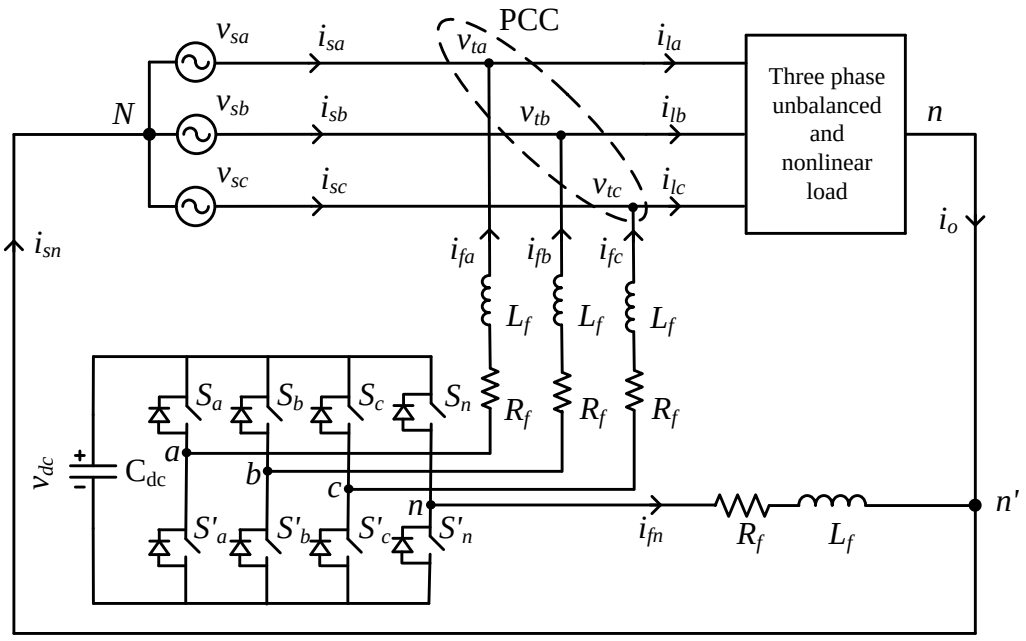

Fig. 2.7 Schematic diagram of three phase four leg VSI topology

Fig. 2.7 illustrates three phase four leg topology with a single unit of DC storage capacitor and extra leg in an inverter, which is connected between source and load neutral through interface reactance and helps in eliminating zero sequence components as well as DC components of source currents [18]. The other three legs are connected to three

phases at PCC. The reference current for the fourth leg is the negative sum ($i_{fn} = -i_o$) of the three phase load currents. To maintain DC link voltage a PI controller is used which regulates the power flow between source and compensator. Since the fourth leg tracks negative of the zero sequence current, it needs a higher bandwidth VSI to track the neutral current. Major drawbacks of this topology are higher number of switches and inability to control each leg of VSI independently. Therefore, each VSI topology has its own load compensation capabilities, merits and demerits, hence the choice of VSI topology is to be done based on the customer requirements and load configuration.

2.3 Switching Control Techniques for VSI

To realize these generated filter currents, DSTATCOM or any practical compensator uses a VSI in an actual distribution system. To achieve desired currents as close as possible to the reference currents, a suitable control scheme is required. Depending on the application, control technique may vary but the primary requirements necessarily remain the same. Some of the fundamental requirements are as follows [19]:

- Ease of implementation
- No phase and amplitude errors for an ideal tracking over a wide frequency bandwidth of operation.
- Low or minimum harmonic content in the compensated quantities
- Good dynamic response of the system
- Constant switching frequency operation of the VSI to ensure safe operation of the power semiconductor switches.
- Effective utilization of input DC link voltage of VSI.

The current control scheme inherently involves a closed loop control in which actual current quantity is compared with a reference quantity and generates switching states. These switching states are appropriately selected in order to minimize error between generated and required currents. Open loop voltage control VSI pulse width modulation (PWM) methods like sinusoidal pulse width modulation (SPWM) and space vector modulation (SVM) strategy have advantages of constant switching frequency of operation resulting in a well-defined harmonic spectrum, optimum switching patterns and

good DC link utilization. Some commonly used current control techniques are Hysteresis current control, Linear PI controller, Ramp comparator control, prediction based hysteresis control, space vector based hysteresis controller, etc. Hysteresis control is reported as one of the most widely used current control technique for active power filter applications. Literature suggests that linear PI controller, ramp techniques and dead beat implementations are also used widely. Hysteresis controller and its improved variations are well suited for high speed applications, while not forsaking dynamic performance. A detailed explanation of the Hysteresis control algorithm used in simulation is explained in the next chapter.

2.4 Dynamic Voltage Restorer (DVR)

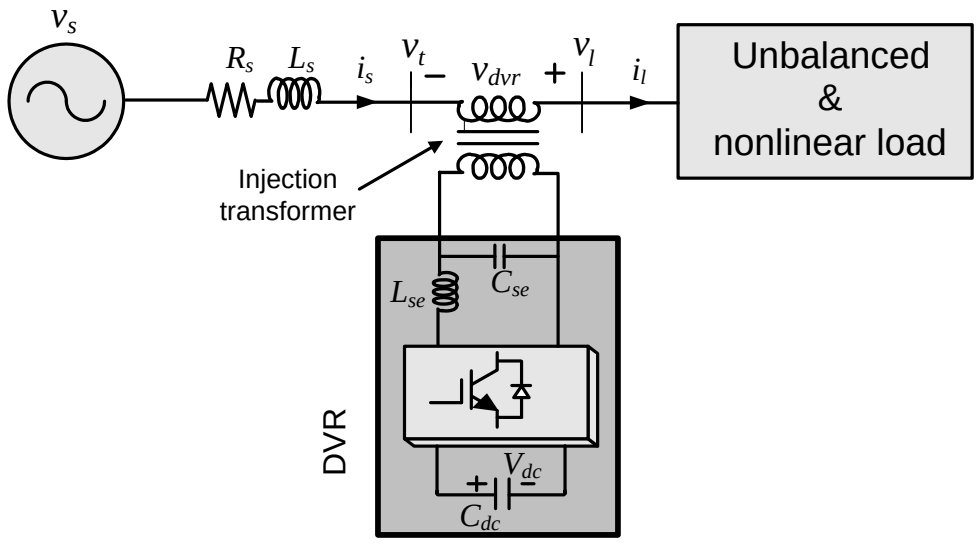

Fig. 2.8 Schematic diagram of DVR

Dynamic voltage restorer belongs to the family of series CPDs which compensates voltage related PQ problems. The basic function of DVR is to inject appropriate voltage to maintain load voltage as desired [20]. DVR has the ability to supply both reactive power and real power. When the voltage sag is small it can be restored through reactive power only. In order to achieve complete compensation during high voltage sag real power supply from DVR is required. Schematic of DVR is shown in Fig. 2.8. Brief description of DVR structure, various topologies, control schemes and compensation techniques are described in following subsections.

2.4.1 Structure of DVR

DVR mainly consists of energy storage device, VSI, Low pass filter and injection transformer. The basic function of VSI is to convert the DC voltage to AC voltage with desired magnitude, phase angle and frequency. The injection transformer low voltage side is connected at VSI while high voltage side is connected in series with the distribution line. The transformer not only provides isolation between inverter and line but also reduces the voltage requirement of the inverter and prevents shorting of capacitor through switches in different legs. Low pass filters are used to filter out higher order harmonic components generated from VSI. These filters can be placed either on the low voltage side or high voltage side of the injection transformers [21]. If filter is connected at low voltage side, higher order harmonics will be filtered out. But, due to the voltage drop across filter inductor, phase angle shift in fundamental component is observed which may compromise the control scheme of DVR. A filter placed at high voltage side of transformer avoids this issue but higher order harmonic currents penetrating into the transformer causes heating and also requirs higher rating of transformer.

2.4.2 Topologies and Control Schemes of DVR

In literature, three-leg, four-leg, split capacitor with neutral point clamped and H-bridge VSI topologies are used. A brief explaination of these topologies are presented in earlier sections. Each VSI topology has its own merits and demerits, but Split capacitor and H-bridge topologies are most commonly used because of their ability to compensate zero sequence component.

DVR control strategies can be divided into reference voltage injection and inverter control. Numerous reference signal generation schemes are presented in literature. Some of the reference voltage injection schemes are closed-loop state variable control, synchronous reference frame based techniques etc. These schemes are required by DVR for restoration of load voltage magnitude and phase. Synchronous reference based control strategies are well used for the purpose.

Inverter control is required by DVR to synthesize switching pulses required for VSI. Switching band controller (Hysteresis voltage controller), Sinusoidal PWM technique etc. are some of the well known techniques. Literature suggests that some of the

schemes require much information about system parameters. Hysteresis voltage control technique is a widely used control technique to synthesize switching signals due to its advantages like, fast dynamic response, zero magnitude/phase error, independent of system parameters and ease of implementation. Detailed discussion on hysteresis controller is presented in chapter 3.

2.4.3 Compensation Techniques of DVR

In power system when a fault occurs, supply voltage fundamental component phase shift and amplitude variation is observed. To compensate this voltage magnitude and phase angle it is required to inject voltage in series. DVR is popularly used to inject compensation voltages. Some of the compensation techniques are in-phase compensation, pre-sag compensation scheme and energy optimized compensation.

In-phase compensation

In-phase compensation compensates voltage sag/swell to same voltage as before voltage disturbance. A phase locked loop (PLL) is used for implementation of this scheme. PLL is a control system that generates an output signal whose phase is related to the phase of an input signal. This PLL should not be locked and it has to be synchronized with the grid. This scheme minimizes the magnitude of injected voltage for mitigation of voltage sag/swell as compared to other compensation techniques. It demands more active power to restore the voltage which results in increment of DC storage equipment. In-phase compensation compensates only voltage but not phase shift i.e., phase jump in source voltage is reflected in load voltage after compensation. It is not advisable to use this scheme under very sensitive loads. Implementation of this scheme with phasor diagram is explained in next chapter.

Pre-sag compensation

A standard solution for compensating voltage sag is to maintain the same load voltage as before the sag. Therefore, the voltage magnitude and phase angle of the load voltage has to be restored exactly as pre sag condition. Unlike In-phase compensation PLL will

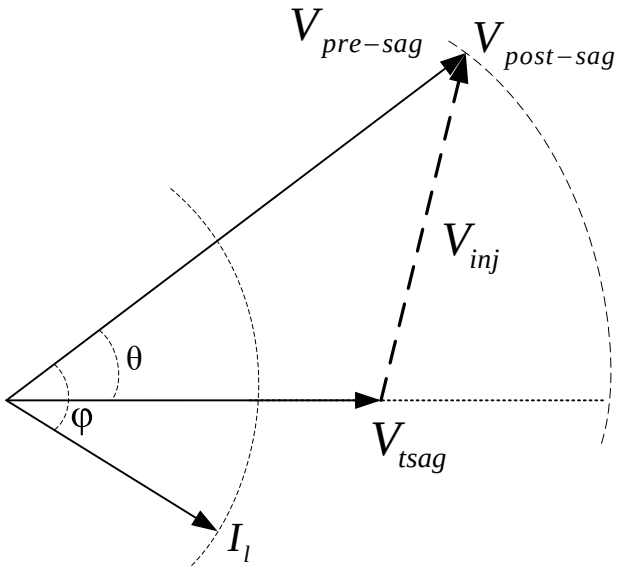

Fig. 2.9 Schematic diagram of Pre-sag compensation

be locked as soon as soon as sag is detected. Restored load voltage is in phase with pre-sag voltage $V_{pre-sag}$. In phasor diagram Fig. 2.9, V_{tsag} is terminal voltage during the sag, θ is phase jump, I_l is load current, and φ is load power factor angle.

$$|V_{dvr}| = \sqrt{V_{presag}^2 - 2V_{presag}V_{sag}\cos\theta + V_{sag}^2} \tag{2.11}$$

$$\alpha = -(\frac{V_{sag}\sin\theta}{V_{presag} - V_{sag}\cos\theta} \tag{2.12}$$

$$P_{dvr} = |V_{dvr}|I_l\cos(\alpha+\theta) \tag{2.13}$$

$$Q_{dvr} = |V_{dvr}|I_l\sin(\alpha+\theta). \tag{2.14}$$

Depending upon the phase jump of the grid voltage and sag depth, magnitude of DVR voltage, the phase of DVR injection voltage i.e., α and corresponding active and reactive power associated with the load voltage compensation are calculated and given in (2.11) - (2.14). This compensation scheme is the better choice due to its performance in transient conditions. If load is very sensitive pre-sag compensation is preferred as it compensated both phase angle and voltage magnitude. injected voltage magnitude $|V_{inj}|$ will be higher than that required for in-phase compensation. The injected voltage increases if the phase jump increases. For larger values of phase jumps compensator ratings should be more, even to compensate for small voltage sags.

Energy Optimized Compensation

In order to reduce the active power requirement for the DVR circuit, energy optimized compensation technique can be used. The DVR is controlled in such a way that the DVR compensation voltages are maintained perpendicular to load currents, which indicates zero active power supply through DVR. The basic idea of this strategy is to draw maximum possible part of the load active power from the grid during the voltage disturbance resulting in minimization of active power requirement from DVR. This technique has a limitation of minimum sag depth. The phasor diagram of the energy optimized voltage compensation is shown in Fig. 2.10.

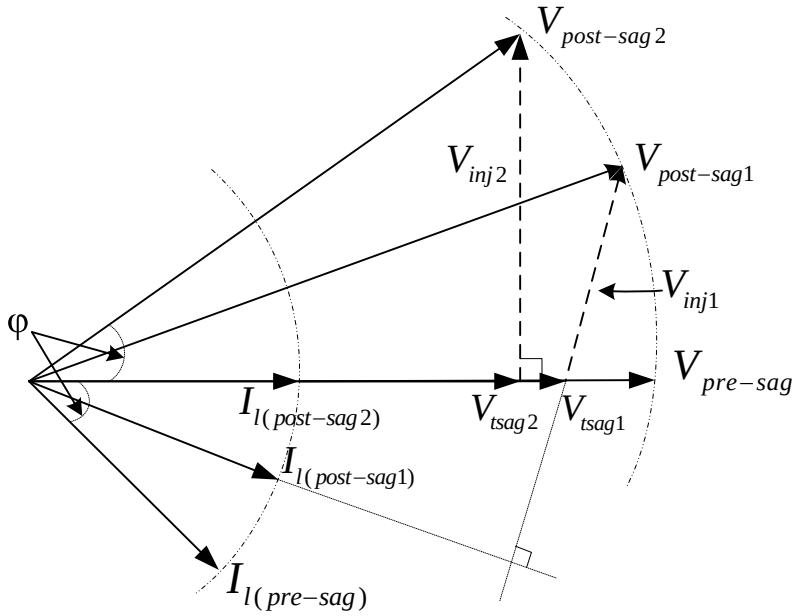

Fig. 2.10 Schematic diagram of Pre-sag compensation

2.5 Unified Power Quality Conditioner (UPQC)

Unified power quality conditioner is the latest device in the family of custom power devices. It is basically a hybrid power quality compensator which improves voltage and current quality issues experienced in power system [22]. In simpler words, a combination of both shunt (DSTATCOM) and series (DVR) compensating devices as shown in Fig. 2.11. The main purpose of series compensation is to mitigate voltage related problems and shunt filters compensates current related problems. UPQC is best suited for simultaneous compensation of above stated power quality problems. UPQC consists of

two VSIs with common DC link and are connected back to back.

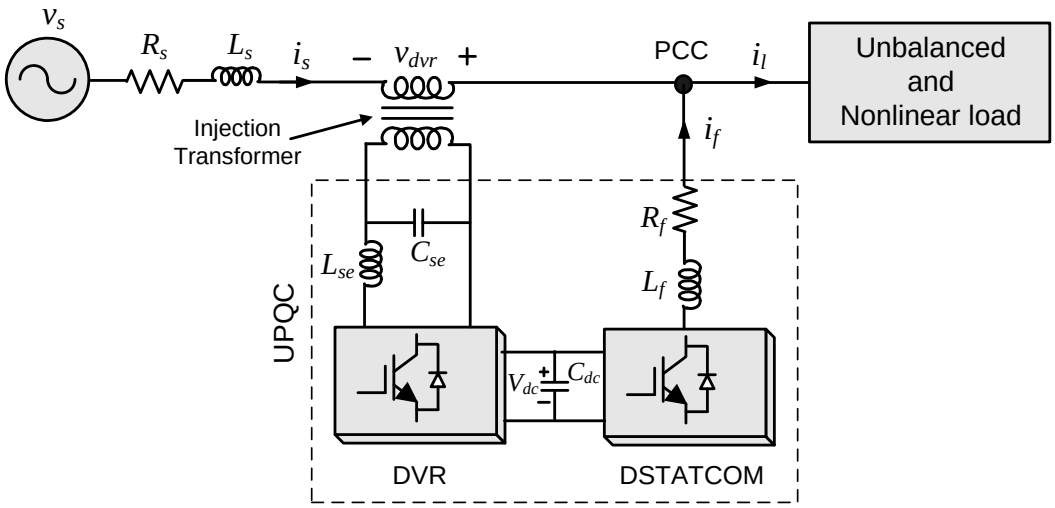

Fig. 2.11 Schematic diagram of UPQC

2.5.1 Topology of UPQC

The configuration of UPQC can be done in many ways depending on the type of inverters and its application. The two types of inverters are VSI and CSI. DC current source in series with large inductor used as input to CSI while a DC voltage source is used as input for VSI. The advantage of VSI over CSI is presented earlier when topologies for VSI are explained. Most commonly used topology is neutral clamped with six switches of IGBT with an anti parallel diode. DC link voltage is maintained constant using PI controller. Brief description of basic blocks in UPQC is explained below. DC link contains two capacitors with grounded midpoint, charged to equal value before initializing UPQC. Compensation of harmonic active powers causes oscillations in dc link voltages. Losses during switching and in interfacing inductors causes VSI to consume real power which deviates dc link voltage from constant value. Real power consumption by series APF occurs during voltage sag depending on sag magnitude and a phase-angle jump can also cause a decrease in dc link voltage. The injection transformer of series APF has to be designed for harmonic voltage in addition to fundamental voltage, positive and negative-sequence compensation.A low pass filter is used in shunt and series APF to filter out higher order harmonic content of the output of VSI.

2.5.2 Compensation of Load using UPQC

The aim is to use UPQC to compensate PQ issues which can fulfill the requirement of consumers and utility. Control of UPQC is implemented in a way that supply only generates average load power to load while the other requirements are met by UPQC. Series APF of UPQC acts as a controlled voltage source as injected voltage needs to be equal to the difference of load voltage and terminal voltage. Shunt APF operated in current control mode can be utilized to maintain dc link voltage to constant level. At PCC shunt APF makes source current harmonic free, balanced and in phase with the fundamental voltage. Hence, UPQC gains the advantage of compensating voltage and current related problems thus meeting the requirements of load, maintaining unity power factor.

2.6 Conclusions

In this chapter, a detailed view of some of the most commonly used custom power devices for compensating voltage and current are described. Principle of operation of DSTATCOM in VCM and CCM has been presented in detail. Various topologies of VSI for DSTATCOM applications are illustrated. Theories for generation of reference currents and control schemes to track these current in order to inject desire voltage are also presented briefly. Out of various theories in the literature for CCM operation of DSTATCOM, the instantaneous symmetrical component with extraction of fundamental positive sequence components is simple in formulation, flexible and can work under all circumstances. Due to this, it a very attractive choice to implement in a real time system. Structure, main components of DVR and their functions are explained. It is shown that voltage sag restoration requires energy injection and in case of a voltage swell, energy is absorbed. In-phase compensation is used as in generation of reference voltages for simulations as it is observed that magnitude of injected voltage at PCC is minimized under voltage disturbances. Structure, topology of UPQC and load compensation using UPQC are explained. It is observed that various topologies have their own merits, demerits in terms of compensation capabilities and the choice of topology is to be done based on the nature of the load to be compensated.

CHAPTER 3

POWER QUALITY IMPROVEMENT USING DSTATCOM AND DVR

Load compensation in power systems is achieved by passive compensation techniques. But this can only eliminate fundamental reactive power and unbalances in steady state. Passive compensation is implemented using passive LC filters and thyristor controlled devices. However, when harmonics are present in the system, these methods fail to provide correct compensation. To correct this unbalance and harmonics, instantaneous theories are used. Two important and commonly used theories for current related problems named instantaneous reactive power theory and instantaneous symmetrical component theory are introduced and discussed in this chapter. Compensation of voltage related problems is explained using in-phase compensation.

Using the theories mentioned, compensation achieved in simulations are explained in the following order:

- Design and Topology of VSI
- Generation of reference currents
- scheme for generating switching pulses

3.1 VSI Parameters

VSI is mainly utilized for injecting required signal at PCC using switching pulses. Widely used topology and control scheme for generation of pulses are used in simulation simulations studies are briefed below. Design parameters are also presented. In simulations ideal DC voltage sources are considered instead of capacitors for better understanding of compensation in distribution systems.

3.1.1 Topology of VSI

One of the common VSI topology used is neutral clamped inverter. A brief description of the topology shown in Fig. 2.5 is as follows. The topology has two DC storage capacitors (C_{dc1}, C_{dc2}) with voltages V_{dc1} and V_{dc2} respectively. Together these capacitors form DC link with voltage $V_{dc} = V_{dc1} + V_{dc2}$ for the inverter. It consists of six switches (S_1 to S_6) with anti-parallel diodes ($D_1$to D_6) to provide freewheeling path for the respective phase currents. The switches shown in the figure are realized using Insulated Gate Bipolar Transistors (IGBTs) or Metal Oxide Field Effect Transistor (MOSFETs) depending of their voltage, current, switching frequency and many other important parameters. The voltage source inverter is connected to the PCC through interface filter L_f and R_f in each phase.

3.1.2 Design of VSI

The compensation capability of an active filter depends on various parameters such as DC link voltage (v_{dc}), DC storage capacitor (C_{dc}), interface inductor (L_f) etc. In order to drive the filter currents, the value of individual DC link voltage (v_{dc}) should have a minimum value of 1.6 times the peak ac system voltage as discussed in [16]. Once the value of v_{dc} is selected, the value of C_{dc} ($C_{dc} = C_{dc1} = C_{dc2}$) can be determined based on the ability to regulate DC link voltage under transients or voltage disturbances. Consider the active filter is connected to an x kVA system and deals with twice ($2x$) and half ($x/2$) kVA handling capability under transient conditions for p cycles. The energy in x kVA system in joules is $x \times 1000$ joules. An increase in system kVA load results a decrease in v_{dc} during transient and vice versa. Allowing a maximum of 12.5% variation in actual v_{dc} ($v_{dc} = v_{dc1} = v_{dc2}$) during transients, the differential energy (ΔE_c) across each capacitor (for increase in load) is given as

$$\Delta E_c = \frac{C_{dci}[(1.6V_{mp})^2 - (1.4V_{mp})^2]}{2}. \tag{3.1}$$

In the above equation, C_{dci} is the capacitor value required to support VSI operation during increase in load. The change in system energy (ΔE_s) for load change from x

kVA to $2x$ kVA in joules is

$$\Delta E_s = (2x - x)1000\ p\ T \tag{3.2}$$

where, T is the time period of system voltage and 'p' is the period of transient. Therefore, using (3.1) and (3.2), each capacitor value C_{dc} can be obtained by equating ΔE_c = ΔE_s /2 (here divided by 2 is used as single capacitor value is being calculated)

$$C_{dci} = \frac{(2x - x)1000\ p\ T}{[(1.6V_{mp})^2 - (1.4V_{mp})^2]}. \tag{3.3}$$

Similarly, C_{dcd} is calculated for the case of decrease in load from x kVA to $0.5x$ kVA, where v_{dc} is allowed to increase up to $1.8V_{mp}$ from a reference value of $1.6V_{mp}$, is given as

$$C_{dcd} = \frac{(x - 0.5x)1000\ p\ T}{[(1.8V_{mp})^2 - (1.6V_{mp})^2]} \tag{3.4}$$

$$C_{dc} = maximum\ of\ (C_{dci}, C_{dcd}). \tag{3.5}$$

The maximum of the obtained C_{dci}, C_{dcd} values is chosen as the DC storage capacitor C_{dc}, as given in (3.5).

The conventional method to interface VSI to PCC is through first order low pass filter (inductor-L_f). This filter inductor is required for proper shaping of current being injected at the PCC. L_f (L_{fa}=L_{fb}=L_{fc}=L_f) is determined by combining two KVL loop equations, applying from midpoint of DC link voltage to terminal voltage v_t at the PCC. KVL loop is applied to the Fig. 3.1.

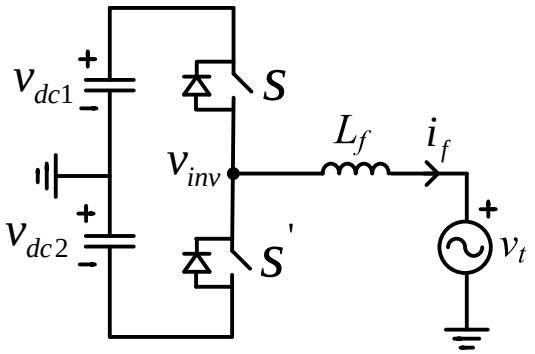

Fig. 3.1 Single phase diagram of VSI connected to grid

Therefore, the interface inductance L_f is given as

$$L_f = \frac{V^*_{Tdc} D\,(1-D)}{f_{sw}\,\delta i_p} \tag{3.6}$$

where, V^*_{Tdc} is the total DC link voltage and δi_p is the allowable peak to peak ripple in filter current which is expressed as the percentage of maximum current in inductor. The term f_{sw} is the switching frequency of triangular carrier signal. The term D is the duty cycle of the switch. Detailed calculation of inerface inductace L_f and capacitance selection is given in [23].

Design of PI Controller to Maintain DC link Voltage

For a practical compensator, switching and ohmic losses are considered. These losses should be met from the source in order to maintain the dc link voltage constant. Let us consider source supplies ploss to maintain dc link voltage. The average voltage variation of dc link may be an indicator of P_{loss} in the inverter. If losses are more than what is supplied by the inverter, the dc link voltage, i.e., $V_{dc} = V_{dc1} + V_{dc2}$, will decline towards zero and vice versa. For proper operation of compensator, we need to maintain dc capacitor voltage to two times of the reference value of each capacitor voltage i.e., $V_{dc1} + V_{dc2} = V_{dc} = 2V_{dcref}$. Thus, we have to replenish losses in inverter and sustain dc capacitor voltage to $2V_{dcref}$ with each capacitor voltage to V_{dcref} . This is achieved by using proportional integral (PI) controller described below.

$$e_{V_{dc}} = 2V_{dcref} - (V_{dc1} + V_{dc2}) \tag{3.7}$$

The term P_{loss} is computed as following

$$P_{loss} = K_p e_{V_{dc}} + K_i \int_0^T e_{V_{dc}} dt \tag{3.8}$$

In the above equation, k represents the kth sample of error, $e_{V_{dc}}$

$$P_{loss}(k) = P_{loss}(k-1) + K_p[e_{V_{dc}}(k) - e_{Vdc}(k-1)] + K_i e_{V_{dc}}(k) T_d \tag{3.9}$$

Thus P_{loss} (error) is generated from PI controller. PI controller is tuned in such way to make error signal to zero which results in maintaing constant capacitor voltage. The control action can be updated at every positive zero crossing of phase voltage. For understanding purposes DC voltage source is considered in all simulations.

3.2 Generation of Reference Signals

Unlike Passive filters, CPDs provide compensation when unbalance and harmonics are present in system. As explained, reference signal generation algorithms plays a part in CPDs for compensation. Instantaneous theories like reactive power theory and symmetrical component theory are used in this chapter for generation of reference currents where as in-phase compensation is used for reference voltages.

3.2.1 Instantaneous Reactive Power Theory

Instantaneous reactive power theory was proposed by Akagi et.al. in 1983-84 [24] and it is also called as *pq* theory. To understand *pq* theory one should know $\alpha\beta 0$ transformation (also known as the Clarke transformation). One main application of transforming in this theory is to generate reference currents used for control of three-phase inverters. The instantaneous supply voltages and load currents in natural *abc* coordinates are transformed into mutually orthogonal $\alpha\beta 0$ coordinates and are given as follows, along with definitions of active and reactive powers after transformation.

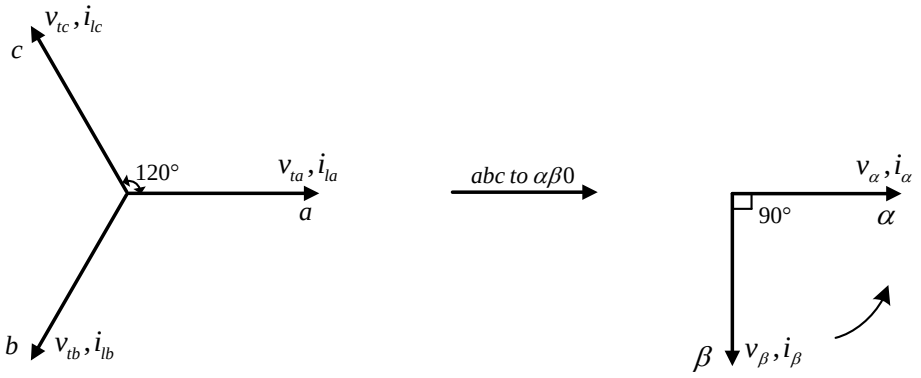

Fig. 3.2 *abc* to $\alpha\beta 0$ transformation

$$\begin{bmatrix} v_\alpha \\ v_\beta \\ v_0 \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} v_{ta} \\ v_{tb} \\ v_{tc} \end{bmatrix} \tag{3.10}$$

$$\begin{bmatrix} i_\alpha \\ i_\beta \\ i_0 \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} i_{la} \\ i_{lb} \\ i_{lc} \end{bmatrix} \tag{3.11}$$

Let the instantaneous real, reactive and zero sequence powers be denoted by p, q and p_0 respectively. Then the three phase instantaneous power is given by

$$p_{3\phi} = v_{ta} i_{la} + v_{tb} i_{lb} + v_{tc} i_{lc}. \tag{3.12}$$

After clark transformation, the instantaneous real power, defined as product of instantaneous voltage on one axis and instantaneous current on the same axis, is given as

$$\begin{aligned} p_{3\phi} &= v_\alpha i_\alpha + v_\beta i_\beta + v_0 i_0 \\ &= p + p_0. \end{aligned} \tag{3.13}$$

The instantaneous reactive power (q) is defined by using cross product of the instantaneous voltage in one axis and the instantaneous current in the other axis. Therefore q is given as [25]

$$\begin{aligned} q &= \vec{v}_\alpha \times \vec{i}_\beta + \vec{v}_\beta \times \vec{i}_\alpha \\ &= v_\alpha i_\beta - v_\beta i_\alpha \end{aligned} \tag{3.14}$$

Using (3.10) and (3.11), instantaneous reactive power in *abc* coordinates is given as

$$\begin{aligned} q &= -\frac{1}{\sqrt{3}}[(v_a - v_b) i_c + (v_b - v_c) i_a + (v_c - v_a) i_b] \\ &= -\frac{1}{\sqrt{3}}[v_{ab} i_c + v_{bc} i_a + v_{ca} i_b]. \end{aligned} \tag{3.15}$$

The reactive power in 3.15 is proportional to the quantity of energy that is being exchanged between the phases of the system. This implies that q does not contribute to the energy transfer between the source and the load at any time. From (3.13) and (3.14),

p and q can be rearranged as following.

$$\begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} v_\alpha & v_\beta \\ v_\beta & -v_\alpha \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \tag{3.16}$$

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \begin{bmatrix} v_\alpha & v_\beta \\ v_\beta & -v_\alpha \end{bmatrix}^{-1} \begin{bmatrix} p \\ q \end{bmatrix} \tag{3.17}$$

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \frac{1}{v_\alpha^2 + v_\beta^2} \begin{bmatrix} v_\alpha & v_\beta \\ v_\beta & -v_\alpha \end{bmatrix} \begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} i_{\alpha p} \\ i_{\beta p} \end{bmatrix} + \begin{bmatrix} i_{\alpha q} \\ i_{\beta q} \end{bmatrix} \tag{3.18}$$

The various terms in the above equation are defined as follows.

α- axis instantaneous active current, $i_{\alpha p} = v_\alpha p/(v_\alpha^2 + v_\beta^2)$

α- axis instantaneous reactive current, $i_{\alpha q} = v_\beta q/(v_\alpha^2 + v_\beta^2)$

β- axis instantaneous active current, $i_{\beta p} = v_\beta p/(v_\alpha^2 + v_\beta^2)$

β- axis instantaneous reactive current, $i_{\beta q} = -v_\alpha q/(v_\alpha^2 + v_\beta^2)$.

The instantaneous power in the α - axis and β - axis are defined as follows.

$$\begin{bmatrix} p_\alpha \\ p_\beta \end{bmatrix} = \begin{bmatrix} v_\alpha i_\alpha \\ v_\beta i_\beta \end{bmatrix} = \begin{bmatrix} v_\alpha i_{\alpha p} \\ v_\beta i_{\beta p} \end{bmatrix} + \begin{bmatrix} v_\alpha i_{\alpha q} \\ v_\beta i_{\beta q} \end{bmatrix} \tag{3.19}$$

$$p = \frac{v_\alpha^2}{v_\alpha^2 + v_\beta^2} p + \frac{v_\alpha v_\beta}{v_\alpha^2 + v_\beta^2} q + \frac{v_\beta^2}{v_\alpha^2 + v_\beta^2} p + \frac{-v_\alpha v_\beta}{v_\alpha^2 + v_\beta^2} q \tag{3.20}$$

$$p = p_{\alpha p} + p_{\alpha q} + p_{\beta p} + p_{\beta q} = p_\alpha + p_\beta \tag{3.21}$$

where,

α- axis instantaneous active power $p_{\alpha p} = v_\alpha^2 p/(v_\alpha^2 + v_\beta^2)$

α- axis instantaneous reactive power $p_{\alpha q} = v_\alpha v_\beta q/(v_\alpha^2 + v_\beta^2)$

β- axis instantaneous active power $p_{\beta p} = v_\beta^2 p/(v_\alpha^2 + v_\beta^2)$

β- axis instantaneous reactive power $p_{\beta q} = -v_\alpha v_\beta q/(v_\alpha^2 + v_\beta^2)$.

Similarly, the reactive power q can be divided into two components corresponding to

the products of voltage along α axis and current along β axis and vice versa.

$$q = v_\beta i_\alpha - v_\alpha i_\beta. \tag{3.22}$$

From eqns. 3.13 and 3.21, the instantaneous three phase active power is given by

$$p_{3\phi} = p_\alpha + p_\beta + p_0. \tag{3.23}$$

The instantaneous active and reactive powers consists of two parts, a DC or average value part indicated by overbar (-) and an oscillating component indicated by overtilde. These can be written as follows

$$\begin{aligned} p &= \bar{p} + \tilde{p} \\ q &= \bar{q} + \tilde{q} \\ p_0 &= \bar{p_0} + \tilde{p_0} \end{aligned} \tag{3.24}$$

Now, the load powers that can be compensated in terms of $\alpha\beta 0$ coordinates are $\tilde{p_l}$, $\bar{q_l}$, $\tilde{q_l}$ and $p_0 = \bar{p_0} + \tilde{p_0}$. Let us assume that the compensator supplies complete reactive power required by the load. Thus compensator reactive power is given as

$$q_f = q_l. \tag{3.25}$$

Similarly, instantaneous active power supplied by the compensator to the load is

$$p_f = \tilde{p_l} + \bar{p_0}. \tag{3.26}$$

The reference currents for the compensator using (3.18), can be written as

$$\begin{bmatrix} i^*_{f\alpha} \\ i^*_{f\beta} \end{bmatrix} = \frac{1}{v_\alpha^2 + v_\beta^2} \begin{bmatrix} v_\alpha & v_\beta \\ v_\beta & -v_\alpha \end{bmatrix} \begin{bmatrix} p_f \\ q_f \end{bmatrix} \tag{3.27}$$

Using (3.25), (3.26) and (3.27), the reference filter currents in $\alpha\beta 0$ frame is given as

$$\begin{bmatrix} i^*_{f\alpha} \\ i^*_{f\beta} \end{bmatrix} = \frac{1}{v_\alpha^2 + v_\beta^2} \begin{bmatrix} v_\alpha & v_\beta \\ v_\beta & -v_\alpha \end{bmatrix} \begin{bmatrix} \tilde{p_l} + \bar{p_0} \\ q_l \end{bmatrix} \tag{3.28}$$

The reference filter currents in *abc* phase system can be obtained using inverse Clark

transformation and is given as

$$\begin{bmatrix} i^*_{fa} \\ i^*_{fb} \\ i^*_{fc} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 & \frac{1}{\sqrt{2}} \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & \frac{1}{\sqrt{2}} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} i^*_{f\alpha} \\ i^*_{f\beta} \\ i^*_{f0} \end{bmatrix} \tag{3.29}$$

where, i^*_{f0} (= i_{l0}) is the zero sequence load current and is given as

$$i_{l0} = \frac{1}{\sqrt{3}}(i_{la} + i_{lb} + i_{lc}). \tag{3.30}$$

For a practical compensator, switching and ohmic losses are considered. These losses should be met from the source in order to maintain the dc link voltage constant. Let these losses are denoted by Ploss, then the following formulation is used to include this term.

$$\Delta\bar{p} = \bar{p_{l0}} + p_{loss} \tag{3.31}$$

Compensator supplied power equations after including power loss component

$$\begin{aligned} p_{f0} &= p_{l0} \\ p_{f\alpha\beta} &= \tilde{p_{l\alpha\beta}} - \Delta\bar{p} \\ q_{f\alpha\beta} &= q_{l\alpha\beta} \end{aligned} \tag{3.32}$$

Once these compensator powers are obtained, compensator currents are computed. Inverse clarke transformation to these currents results in abc frame using equations 3.29 and 3.30.

Once reference currents are generated they have to be synthesized by voltage source inverter (VSI). To synthesize, switching pulses are required. Required pulses are generated using control scheme explained above.

3.2.2 Theory of Instantaneous Symmetrical Components

The theory of instantaneous symmetrical components can be used for the purpose of load balancing, harmonic suppression, and power factor correction [2], [4]. The control algorithms based on instantaneous symmetrical component theory can practically

compensate any kind of unbalance and harmonics in the load, provided we have a high bandwidth current source to track the filter reference currents. Any three phase quantity can be divided into positive, negative and zero sequence component.

$$\begin{bmatrix} \boldsymbol{v}_{sa}^{0} \\ \boldsymbol{v}_{sa}^{+} \\ \boldsymbol{v}_{sa}^{-} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \begin{bmatrix} v_{sa} \\ v_{sb} \\ v_{sc} \end{bmatrix} \tag{3.33}$$

$$\begin{bmatrix} \boldsymbol{i}_{sa}^{0} \\ \boldsymbol{i}_{sa}^{+} \\ \boldsymbol{i}_{sa}^{-} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \begin{bmatrix} i_{sa} \\ i_{sb} \\ i_{sc} \end{bmatrix} \tag{3.34}$$

In (3.33) and (3.34), 0, + and −, indicates zero, positive and negative sequence components respectively. The quantity 'a' is a complex operator and is equal to $e^{j\frac{2\pi}{3}}$. It is to be noted that the instantaneous positive sequence ($\boldsymbol{i}_{sa}^{+}$) and the negative sequence ($\boldsymbol{i}_{sa}^{-}$) are complex conjugates of each other and the zero sequence component ($\boldsymbol{i}_{sa}^{0}$) is a real quantity which is zero if the currents are balanced. Like *pq* theory, we assume that the supply voltages are balanced.

The objective of three phase four wire system is to provide balanced source currents such that its zero sequence components is zero. We therefore have

$$i_{sa} + i_{sb} + i_{sc} = 0. \tag{3.35}$$

To have a predefined power factor from the source, the relationship between the angle of source current ($\boldsymbol{i}_{sa}^{+}$) and the source voltage ($\boldsymbol{v}_{sa}^{+}$) is assumed as shown in equation 3.36. This power factor angle (φ^{+}) can be explicitly set to any desired value in the control algorithm. But it is not directly expressed as in *pq* theory described earlier.

$$\angle v_{sa}^{+} = \angle i_{sa}^{+} + \varphi^{+} \tag{3.36}$$

$$\angle\left\{v_{sa} + a v_{sb} + a^2 v_{sc}\right\} = \angle\left\{i_{sa} + a i_{sb} + a^2 i_{sc}\right\} + \varphi^{+} \tag{3.37}$$

The above equation is expanded after substituting the values for a and a^2, it is given as

follows

$$\angle\left\{(v_{sa}-\frac{1}{2}v_{sb}-\frac{1}{2}v_{sc})-j\frac{\sqrt{3}}{2}(v_{sb}-v_{sc})\right\}=\angle\left\{(i_{sa}-\frac{1}{2}i_{sb}-\frac{1}{2}i_{sc})-j\frac{\sqrt{3}}{2}(i_{sb}-i_{sc})\right\}+\varphi^{+}. \tag{3.38}$$

Equating the angles, we can write from the above equation

$$tan^{-1}(K_1/K_2)=tan^{-1}(K_3/K_4)+\varphi^{+} \tag{3.39}$$

where,

$$K_1=\frac{\sqrt{3}}{2}(v_{sb}-v_{sc}) \qquad K_2=(v_{sa}-\frac{1}{2}v_{sb}-\frac{1}{2}v_{sc})$$
$$K_3=\frac{\sqrt{3}}{2}(i_{sb}-i_{sc}) \qquad K_4=(i_{sa}-\frac{1}{2}i_{sb}-\frac{1}{2}i_{sc}).$$

Taking tan on both sides of (3.39), we get

$$\frac{K_1}{K_2}=tan\left[tan^{-1}(K_3/K_4)+\varphi^{+}\right]=\frac{K_3/K_4+tan\,\varphi^{+}}{1-(K_3/K_4)tan\,\varphi^{+}} \tag{3.40}$$

substituting values of K_1, K_2, K_3 and K_4 in the above equation we get

$$\begin{aligned}(v_{sb}-v_{sc}-3\gamma(v_{sa}-v_0))i_{sa}+(v_{sc}-v_{sa}-3\gamma(v_{sb}-v_0))i_{sb}+\\ (v_{sa}-v_{sb}-3\gamma(v_{sc}-v_0))i_{sc}=0.\end{aligned} \tag{3.41}$$

where $\gamma\equiv tan\varphi^{+}/\sqrt{3}$. For unity power factor φ^{+} = 0, hence $\gamma=0$. It is well known that the instantaneous power in a balanced three phase circuit is constant while for an unbalanced circuit it has a double frequency component in addition to the DC or mean value. The presence of harmonics adds higher frequency oscillating components to the instantaneous power. The objective of the compensator is to supply the oscillating component of the instantaneous load power, while the source supplies the average value of the load power, P_{lavg}. Therefore, we obtain as following.

$$v_{sa}i_{sa}+v_{sb}i_{sb}+v_{sc}i_{sc}=P_{lavg} \tag{3.42}$$

This P_{lavg} is calculated using moving average filter (MAF). Although low pass filter can be used to find P_{lavg} but dynamic response is quite slow. This dynamic performance

plays a prominent role in compensation. For this reason moving average algorithm is used.

$$P_{lavg} = \frac{1}{T}\int_{t_1-T}^{t_1} (v_{la}i_{la} + v_{lb}i_{lb} + v_{lc}i_{lc})dt \tag{3.43}$$

Now combining the equations (3.35), (3.41) and (3.42), we get the reference source currents

$$\begin{bmatrix} i^*_{sa} \\ i^*_{sb} \\ i^*_{sc} \end{bmatrix} = M^{-1} \begin{bmatrix} 0 \\ 0 \\ P_{lavg} \end{bmatrix} \tag{3.44}$$

where,

$$M = \begin{bmatrix} 1 & 1 & 1 \\ (v_{sb} - v_{sc} - 3\gamma(v_{sa} - v_0)) & (v_{sc} - v_{sa} - 3\gamma(v_{sb} - v_0)) & (v_{sa} - v_{sb} - 3\gamma(v_{sc} - v_0)) \\ v_{sa} & v_{sb} & v_{sc} \end{bmatrix} \tag{3.45}$$

Therefore, the reference compensator currents are given as

$$\begin{aligned} i^*_{fa} &= i_{la} - i^*_{sa} = i_{la} - \frac{(v_{sa} - v_0) + \gamma(v_{sb} - v_{sc})}{\Delta_1}(P_{lavg}) \\ i^*_{fb} &= i_{lb} - i^*_{sb} = i_{lb} - \frac{(v_{sb} - v_0) + \gamma(v_{sc} - v_{sa})}{\Delta_1}(P_{lavg}) \\ i^*_{fc} &= i_{lc} - i^*_{sc} = i_{la} - \frac{(v_{sc} - v_0) + \gamma(v_{sa} - v_{sb})}{\Delta_1}(P_{lavg}) \end{aligned} \tag{3.46}$$

where,

$$\Delta_1 = \left[\sum_{j=a,b,c} v^2_{sj}\right] - 3v_0^2,\ v_0 = \frac{1}{3}\sum_{k=a,b,c} v_{sk},\ \gamma = tan\,\varphi/\sqrt{3} \tag{3.47}$$

The average power supplied by the source according to the above equation will be equal to the average power required by the load. Apart from the load average power, the source has to supply VSI losses also. When the inverter power loss P_{loss} is also incorporated in the above equations, the modified reference currents of the compensator

changes to equation 3.48.

$$
\begin{aligned}
i^*_{fa} &= i_{la} - i^*_{sa} = i_{la} - \frac{(v_{sa} - v_0) + \gamma(v_{sb} - v_{sc})}{\Delta_1}(P_{lavg} + P_{loss}) \\
i^*_{fb} &= i_{lb} - i^*_{sb} = i_{lb} - \frac{(v_{sb} - v_0) + \gamma(v_{sc} - v_{sa})}{\Delta_1}(P_{lavg} + P_{loss}) \\
i^*_{fc} &= i_{lc} - i^*_{sc} = i_{la} - \frac{(v_{sc} - v_0) + \gamma(v_{sa} - v_{sb})}{\Delta_1}(P_{lavg} + P_{loss}).
\end{aligned}
\tag{3.48}
$$

The term P_{lavg} is obtained using simple moving average filter and P_{loss} is obtained from the PI controller. The error between DC voltage reference and actual DC voltage are processed through PI controller to obtain P_{loss}. This will control the DC link voltage by adjusting the small amount of real power absorbed by the inverter of DSTATCOM. This small amount of real power is adjusted by changing the amplitude of the fundamental component of the reference current. The AC source provides some active current to recharge the DC capacitor. Thus, in addition to reactive and harmonic components, the reference current of the DSTATCOM has to contain some amount of active current as compensating current. This active compensating current flowing through the shunt active filter, regulates the DC capacitor voltage [23]. When the source voltages are balanced $v_0 = 0$ in the above equations.

3.2.3 In-phase Compensation

In-phase compensation is used to mitigate voltage related issues in power system. In this technique load voltage is assumed to be in-phase with the pre-sag voltage. In contrast to the pre-sag compensation, the voltage is now compensated in phase to the grid voltage after the sag. Hence, the required voltage amplitude is minimized. To realize this strategy, the PLL has to be synchronized to the grid voltage itself, and therefore, must not be locked to the pre-sag grid voltage during the compensation. Therefore, the reference voltage of the control system will always be in phase with source voltage (v_s). During Voltage sag, DVR has to supply power into the system in order to compensate [26]. Conversely under voltage swell, power injected is negative indicating DVR will absorb power from external system. The absorbed power would have to be stored in the energy storage storage system and the result would be rise in the dc capacitor voltage. Therefore while designing capacitance above factors should be considered. Phasor diagram of in-phase compensation is shown Fig 3.3.

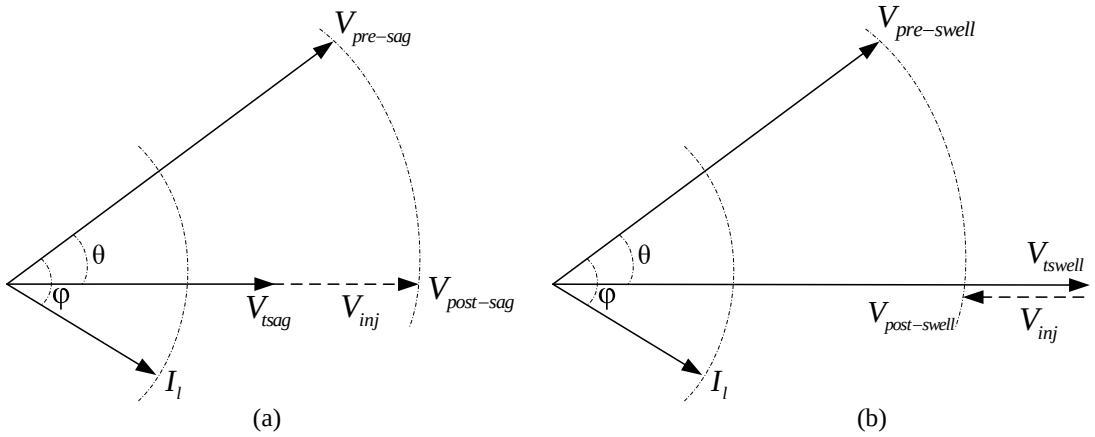

Fig. 3.3 Phasor diagram for in-phase compensation (a) sag compensation (b) swell compensation

Using above mentioned scheme reference signals generation is as follows. Secondary side of injection transformer is connected between terminal voltage (v_t) and load voltage (v_l) as shown in Fig. 2.8. Voltages sensed at terminal voltage are given as input to phase-locked loop (PLL) which outputs phase angle. This phase angle is multiplied with sine wave of desired amplitude to generate sinusoidal balance waveforms with same phase as terminal voltage. Difference between sensed terminal voltage waveforms and generated waveforms gives the reference signal. The illustration is of this process is shown in Fig. 3.4.

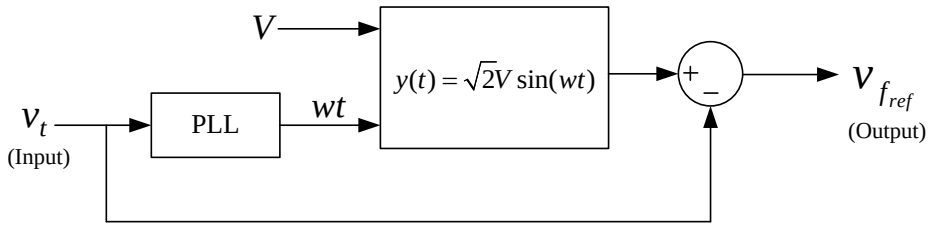

Fig. 3.4 Block diagram representation of reference signal generation

In the above figure V represents desired constant voltage amplitude while $v_{f_{ref}}$ is obtained reference signal. Reference signal and actual injected signal sensed is given to hysteresis voltage control. Here actual waveform is varied over reference signal with upper and lower bound thus generating switching pulses to VSI. Neutral clamped VSI is used with low pass filter to inject required compensating voltage. Merits and demerits of filter on either side of transformer is discussed in chapter 2.

3.3 Switching Control of VSI

Commonly used control scheme named hysteresis control has been used for generation of pulses. This is closed loop control technique with a fast transient response. Hysteresis controller has the advantage of peak current limiting capacity apart from the other merits such as ease of implementation, good dynamic response and independent from the load parameter variations. It is to be noted that in the case of a three phase system with neutral conductor, the current error remains within the tolerance band because the hysteresis comparators are independent. But, in the absence of the neutral conductor, the instantaneous current error may at most reach twice the value of the hysteresis band. This is due to the interaction between the comparators, since the comparator state change in one phase influences the voltage applied across the coupling inductor in other phases [23]. The switching signals $S_a, S_a^{'}, S_b, S_b^{'}, S_c$ and $S_c^{'}$ for VSI are generated using a hysteresis band current control. The switching commands for switches is generated when error signal (e_f) between reference current (i_f^*) and actual current (i_f) exceeds a specific tolerance band h. Boundaries of reference filter current (say phase-a) are formed using hysteresis h i.e., $i_{fa}^* + h$ and $i_{fa}^* - h$.

Matlab code for implementation of control logic for a phase switches

if $i_{fa} \geq \mathrm{i}_{fa}^* + h$

$S_a = 0$ and $S_a^{'} = 1$

else if $i_{fa} \leq \mathrm{i}_{fa}^* - h$

$S_a = 1$ and $S_a^{'} = 0$

end

$S_a = 0$ and $S_a^{'} = 1$ implies that the top switch is open and bottom switch is closed and, $S_a = 1$ and $S_a^{'} = 0$ implies that the top switch is closed and bottom switch is open. The two logic signals S_a and $S_a^{'}$ are complementary to each other. This logic also holds for b and c phases. While in case of switching for voltage controller same principle as current controller is used. But, instead of reference current (i_f^*), reference voltage (v_f^*) is used in algorithm.

3.4 Simulation Studies

This section includes simulation results of Compensating power quality issues using reference quantities generation theories. Tabulated values have been considered for all the simulations. All the simulations are done in MATLAB/Simulink environment and schematic is shown in 2.5.

Table 3.1 System Parameters for Simulation Studies

System Parameters	**Experimental values**
System voltage	V_{lrms} = 398.371 V, f = 50 Hz
Feeder impedance	R_s = 0.01 Ω, L_s = 3 μH
Linear load	$Z_{la} = 300 + j0.003$ Ω, $Z_{lb} = 275 + j0.03$ Ω, $Z_{lc} = 420 + j0.1$ Ω
Addition of parllel load for load change	$Z_{la_1} = 250 + j0.003$ Ω, $Z_{lb_1} = 175 + j0.3$ Ω, $Z_{lc_1} = 300 + j0.1$ Ω
Nonlinear load	Three phase diode bridge rectifier with R-L load of 300 Ω - 50 mH
VSI parameters	$V_{dc1} = V_{dc2}$ = 350 V
Filter parameters	L_f = 20 mH, R_f = 0.5 Ω

Fig. 3.5 illustrates currents drawn by load and supplied by source without any compensating devices. It is observed that source currents are not balanced and sinusoidal as load consists of both linear and non-linear loads. The total harmonic distortion (THD) of source waveforms are in the range of $11.3\% - 14.8\%$. But, allowable THD in power system is 5% according to IEEE std 1547 [27]. Therefore, compensation is required, which is achieved in simulations by using above mentioned theories.

Fig 3.6 represents compensation achieved using *pq* theory. It is observed that source currents supplied by the source are sinusoidal and THD is 0.79% in all the three phases. It is also observed that waveforms of load currents are as desired and harmonics are supplied by compensator which is shown in fig 3.6 (b) and (c). Although *pq* theory is able to compensate the power quality issues but it has some setbacks. If the nature of load is linear and harmonics are absent, still resolutions of active and reactive components of the current based on *pq* theory gives harmonics. Source currents majorly consists of third harmonic which is not possible for linear loads. Also, instantaneous reactive power $q(t)$ as defined by *pq* theory does not really identify the power properties of load instantaneously. Both powers $p(t)$ and $q(t)$ are time varying quantities, so that a

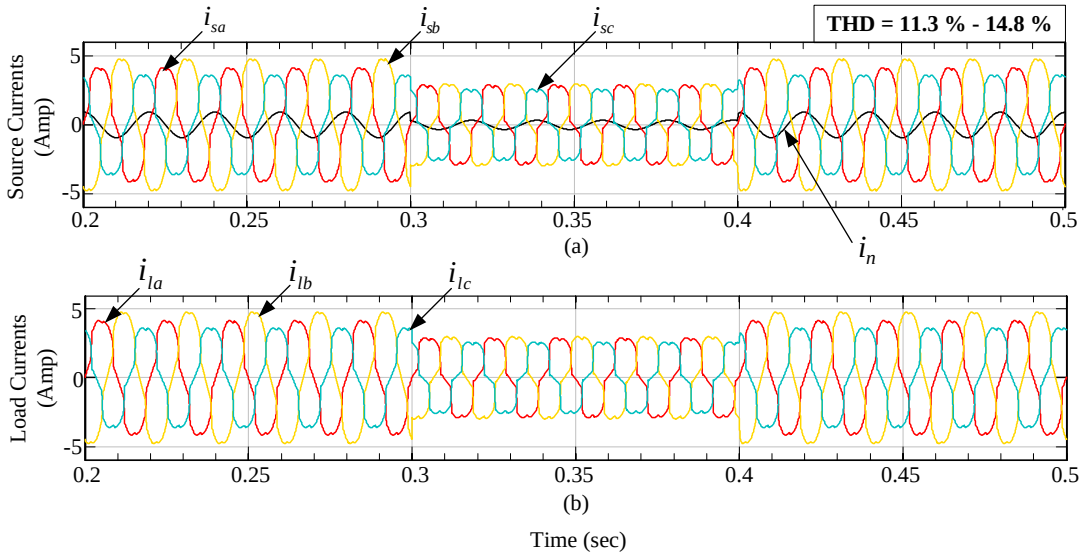

Fig. 3.5 Simulation results before compensation (a) Source currents before compensation, (b) Load currents before compensation

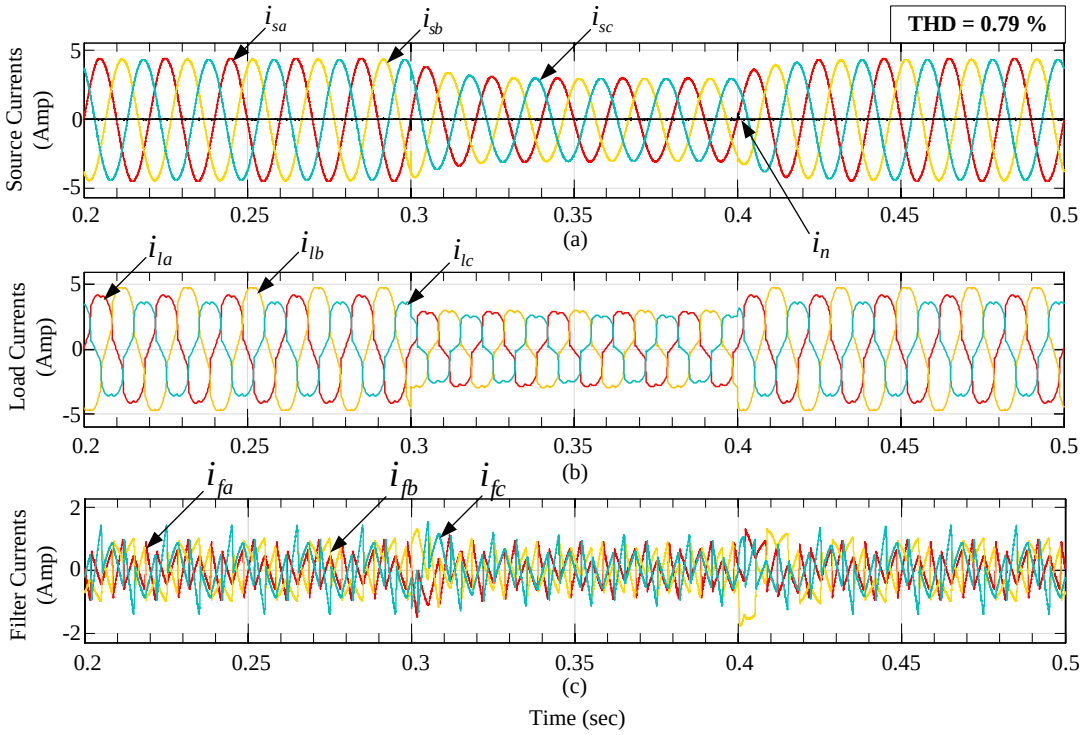

Fig. 3.6 Simulation results of compensation using *pq* theory (a) source currents after compensation, (b) load currents after compensation, (c) injected filter currents

pair of their values at any single point of time does not identify the power properties of load [25]. Thus it is observed that *pq* theory is unable to achieve complete compensation. Hence symmetrical component theory is considered and used widely for complete compensation.

Compensation achieved by using symmetrical component theory is shown in fig 3.7. It

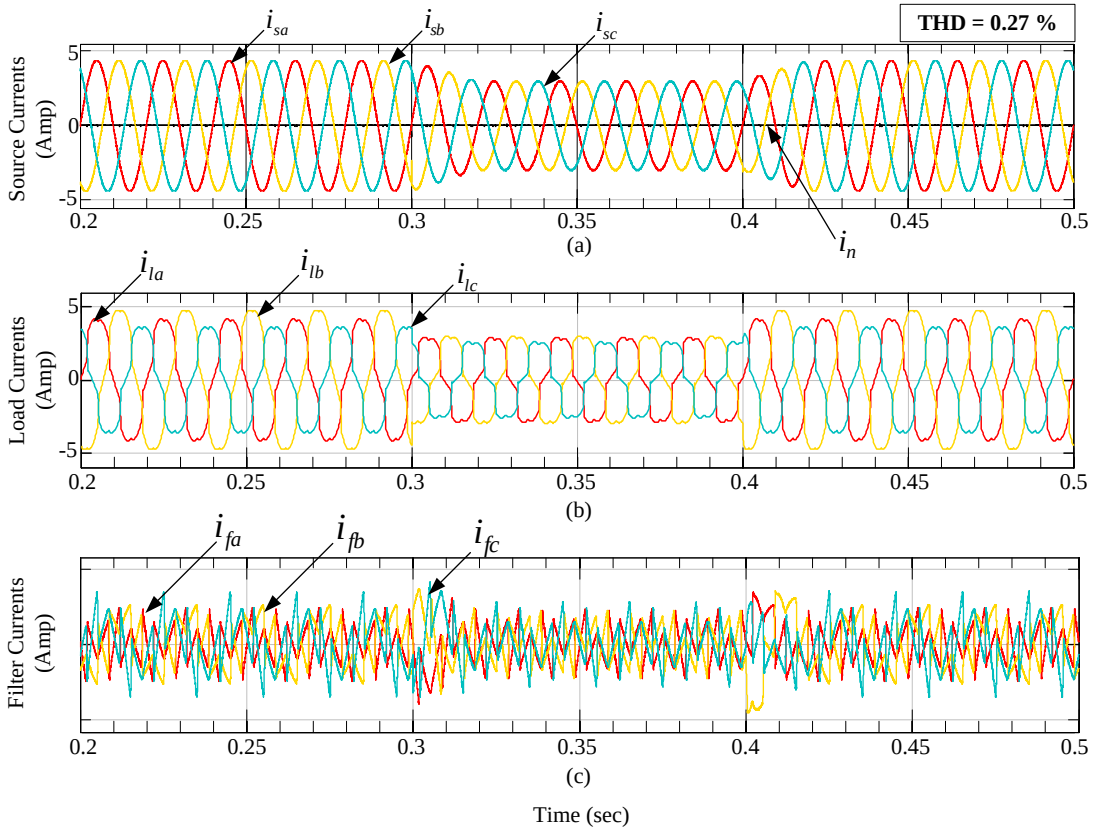

Fig. 3.7 Simulation results of compensation using symmetrical component theory (a) Source currents after compensation, (b) Load currents after compensation, (c) Injected filter currents

is observed that waveforms are balanced, sinusoidal and harmonic free. Neutral current is very close to zero as balanced currents are supplied by source. The THD value of source waveforms are 0.27%. Thus compensation using symmetrical component theory is achieved with almost unity power factor. The above simulation studies represents current compensation which is achieved by DSTATCOM. Voltage compensation is done using DVR by in-phase compensation is shown.

In Fig. 3.8 source voltages and load voltages before compensation simulation studies are shown. It is observed that load voltage is similar to source voltage, so if there are any changes in source voltages load voltages are affected. In order to compensate this DVR is used. Simulations using DVR for voltage compensation is shown in fig 3.9. In the Fig. 3.9, from simulation studies it is shown that load voltages are not similar to source voltages in presence of sag/swell. Filter voltages shown is injected at load terminal is able to maintain desired voltage.

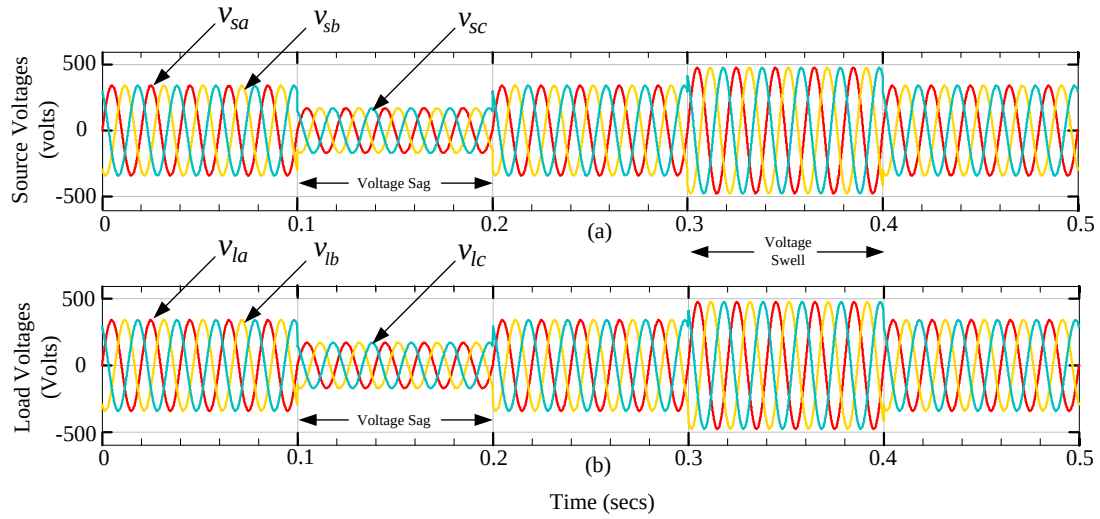

Fig. 3.8 Simulation results before compensation (a) Source voltages before compensation, (b) Load voltages before compensation

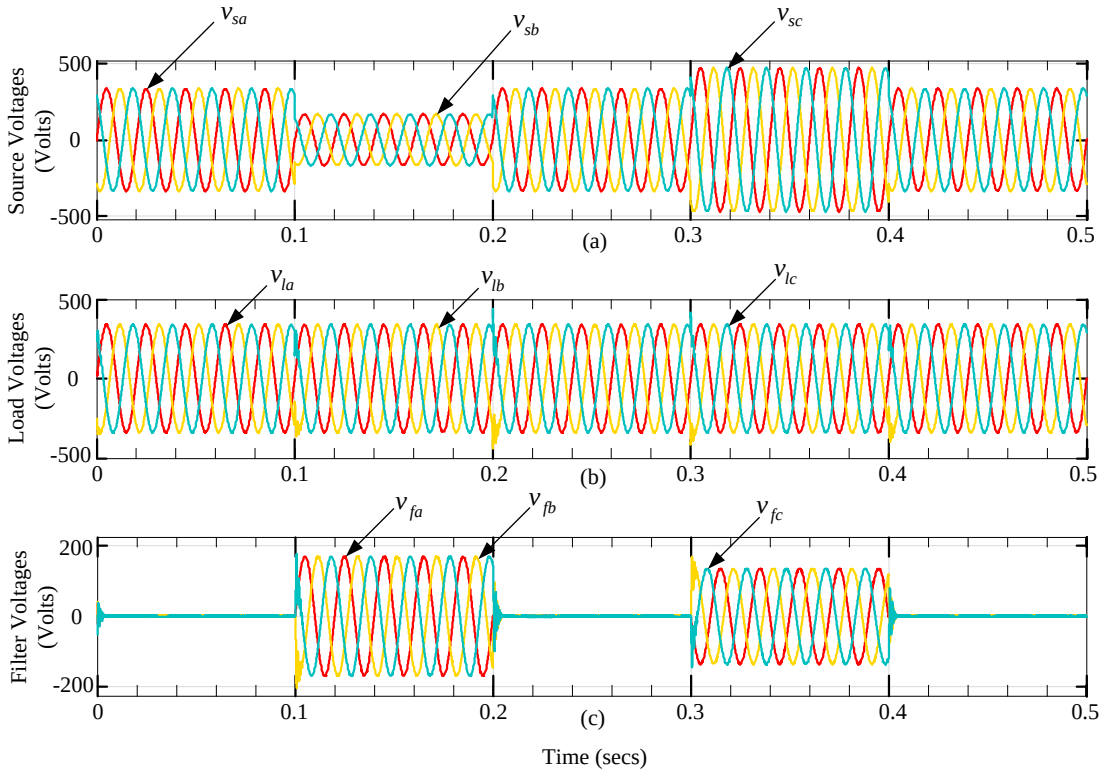

Fig. 3.9 Simulation results of compensation using in-phase compensation (a) Source voltages after compensation, (b) Load voltages after compensation, (c)Filter Voltages injected for compensation

3.5 Conclusions

The chapter concludes a detailed illustration of compensation with simulation studies.

Explanation of topology and design parameters of VSI and hysteresis current/voltage

controller algorithm for generating switching pulses is presented. It is observed that instantaneous symmetrical component theory is better than instantaneous reactive power theory in order of compensating neutral current. In current compensation simulations, source currents THD is in the range of $0.27\% - 0.79\%$ which is less than the prescribed standard i.e., 5%. It can be observed that *pq* theory has some drawbacks in compensation. In case of DVR compensation simulations, load voltages are unchanged when disturbances like sag and swell are present in utility supply but phase shift is not compensated in case of in-phase compensation. Thus Power Quality issues related to voltage and current compensation is understood from simulation studies.

CHAPTER 4

CONCLUSIONS

4.1 Summary

The extensive use of power electronic loads and unbalanced loads in power system has deteriorated power quality. Some of the power quality issues are voltage/current unbalance, distortion, voltage sag/swell, fluctuations and frequency variation. To overcome this effects passive filters were used but due to their inability to compensate harmonics, custom power devices have emerged. Among the custom power devices, DSTATCOM for current related problems and DVR for voltage related problems are used popularly. Compensation of voltage/current related power quality issues, simulations are done in MATLAB/Simulink environment. Compensation achieved by custom power devices in simulations is explained by dividing into three major blocks such as topology and design of VSI, reference signal generation and synthesization of switching pulses. A Neutral clamp inverter topology has been chosen for VSI because of its independent control, less number of switches and path for zero sequence. Hysteresis controller has been used for synthesizing switching pulses which are given as input to VSI switches. This controller was preferred in this work because of fast dynamic response, zero magnitude/phase error, independent of system parameters and ease of implementation. For reference signal generation in-phase compensation was used in DVR while in case of DSTATCOM *pq* theory and instantaneous symmetrical component theory have been used.

4.2 Conclusions

Simulations based on above theories concludes that

- THD of source current is in the range of $0.27\% - 0.79\%$ which should be less than 5% as per standard

- *pq* theory has drawbacks of supplying harmonic current in case of linear load and definitions presented for $p(t)$ and $q(t)$ does not identify the power properties of the load instantaneously.
- Symmetrical component theory is able to achieve complete compensation
- In-phase compensation for DVR simulations is able to compensate load voltages and are obtained as desired
- This theory has setback of inability to compensate phase shift. Due to this, phase jump in source voltage is reflected in load voltage after compensation.

4.3 Scope for Future Work

Topologies used for VSI and controllers have its own merits and demerits because of this depending on load conditions and requirements topology is selected. Further more investigation into topologies may overcome this. Renewable energies have emerged into power distribution in recent years integration of these sources with distribution systems may reduce the burden on utility. Renewable energies replace DC capacitors when connected to system. These sources can act as micro grid. To achieve integration and efficient power supply, theories are needed to be explored.

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