A Novel FinFET with Dyanmic Threshold Voltage

A Project Report

submitted by

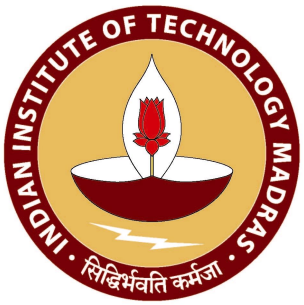
SELWIN KUMAR P

in partial fulfilment of the requirements

for the award of the degree of

MASTER OF TECHNOLOGY

(MICROELECTRONICS AND VLSI DESIGN)



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JUNE 2014

THESIS CERTIFICATE

This is to certify that the thesis titled **A Novel FinFET with Dyanmic Threshold Voltage**, submitted by **Selwin Kumar P, Roll no EE12M073**, to the Indian Institute of Technology, Madras, for the award of the degree of **Master of Technology**, is a bona fide record of the research work done by him under our supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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ACKNOWLEDGEMENTS

It is a great honor for me to have done my thesis work with the guidance of Dr. Amitava Dasgupta and Dr. Deleep Nair, professors with great magnitudes of technical knowledge and achievements. I would like to express my sincere gratitude to them for explaining me lot of device physics, advanced CMOS technology aspects with such great patience, and I am indebted to them for the same.

The experience of Dr. Amitava Dasgupta and the exuberance of Dr. Deleep Nair is a great combination. I would like to thank them for the weekly discussions or sometimes more than once a week, which enlightened me. The freedom they gave me to walk into their office room anytime and ask technical clarifications is truly remarkable.

I would like to thank my father, my brother and my fiancee for their constant support and encouragement.

ABSTRACT

KEYWORDS: Bulk FinFETs; Isolation; DTMOS;

Modern day transistors have feature sizes of sub hundred nanometers. It has become increasingly difficult to turn off these transistors. As a result the standby power dissipation increases. In these small transistors, by scaling the size alone it is not possible to get higher on-current for same off-current. Dynamic Threshold MOSFETs (DTMOS), with their gate connected to the substrate, have higher on-current (I_{dsat}) and lower off-current (I_{off}) compared to conventional devices due to lower (higher) threshold voltage (V_{th}) at higher (lower) gate bias (V_{gs}). In DTMOS, the body effect is responsible for the threshold voltage variation (ΔV_{th}), which increases with increase in substrate doping concentration. However, since the present generation of FinFETs have undoped channels, ΔV_{th} is very small. On the other hand, DTMOS devices are now viable as reduction in supply voltage to sufficiently low values eliminates the problem of substrate current due to the forward biased substrate-source junction. Intel's 22 nm transistors work with a supply voltage of 0.75 V making the leakage current due to DTMOS within acceptable limits. In this work we have proposed a new FinFET device which enables DTMOS operation and provides an on-current benefit of 10 %.

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ABBREVIATIONS

MOSFET	Metal Oxide Semiconductor Field Effect Transistor
CMOS	Complementary MOSFETs
BJT	Bipolar Junction Transistor
ITRS	International Technology Roadmap for Semiconductors
DTMOS	Dynamic Threshold MOSFET
FDSOI	Fully Depleted Silicon on Insulator
SOI	Silicon On Insulator
SCE	Short Channel Effect
DIBL	Drain Induced Barrier Lowering
MuGFET	Multi-gate electric field Effect Transistor
DELTA	Depleted Lean channel Transistor
PTS	Punch Through Stoppers
EOT	Equivalent Oxide Thickness
SEM	Scanning Electron Microscope
RDF	Random Dopant Fluctuations
BTBT	Band to Band Tunneling

NOTATION

V_{gs}	Gate to source voltage
V_{ds}	Drain to source voltage
V_{TH}	Threshold Voltage of a MOSFET
I_{dsat}	Drain current at V_{gs}=V_{dd} and V_{ds}=V_{dd}
I_{off}	Drain current at V_{gs}=0V and V_{ds}=V_{dd}
V_t	Thermal Voltage
I_D	Drain current

CHAPTER 1

Introduction

The remarkable advancement in electronics is driven mainly by MOS technology which accounts for 90 % of all integrated circuits. Because CMOS circuits consume lower standby power, MOSFETs progressively replaced the BJTs in integrated circuits. Gordon Moore predicted (Gordon Moore, 1965) that transistor density will double approximately every two years. This prediction is now a beacon for semiconductor industries and ITRS to have research targets to scale down the size of transistors. Transistor sizes have scaled down from millimeters to few nanometers, and integrated circuits are made with billions of transistors in the same area. This work is targeted at exploring options to achieve higher performance MOSFET.

1.1 Overview of scaling in MOSFETs and related issues

Till a decade ago, transistors were scaled based on Dennards scaling rule (Dennard *et al.*, 1972), by maintaining constant vertical and horizontal fields in the channel region. This led to very short channel length transistors. As the channel length became shorter, source and drain are brought close to each other. The drain electric field starts impacting the energy barrier at the source causing Drain Induced Barrier Lowering (DIBL). This is more pronounced in regions farther away from gate, as the regions closer to gate are more effectively controlled by the gate electric field. Another problem in short channel devices is, part of channel depletion charge is contributed by depletion charge from source/drain to substrate junction, this is called as Short Channel Effect(SCE). All these increases the off-current. Off-current is the drain current at V_{gs}= 0 V and V_{ds}=V_{dd}, denoted as I_{off}. Across successive technology nodes, the increase in off-current led to near saturation of on-current when compared at fixed off-current. On-current is the drain current at V_{gs}=V_{dd} and V_{ds}=V_{dd}, denoted as I_{dsat}.

1.1.1 Need for Dynamic Threshold Voltage

The I_{dsat} and I_{off} of MOSFETs are dependent on threshold voltage as,

$$I_{ON} \propto (V_{gs} - V_{TH})^2. \tag{1.1}$$

$$I_{OFF} \propto exp(\frac{(V_{gs} - V_{TH})}{mV_t}). \tag{1.2}$$

where,

m is inverse of rate of change of channel surface potential with gate electric field,

V_t is the thermal voltage,

V_{gs} is gate to source potential,

V_{TH} is the Threshold Voltage of a MOSFET.

Higher V_{TH} is required for lower off-current as exponential factor in I_{off} expression will decrease for higher V_{TH}. Lower V_{TH} is required to have higher on-current as V_{gs}-V_{TH} factor will increase. Given such a requirement, a dynamic threshold voltage MOSFET is an attractive option. DTMOS gives higher I_{dsat}/I_{off} ratio and better subthreshold slope. Subthreshold slope is given in mV/decade, represents how fast the gate voltage is able to increase the drain current (I_D) when transistor switches from OFF condition to ON condition or how fast the I_D falls to a lower value when transistor switches from ON condition to OFF condition.

1.2 Multi-gate MOSFETs

To maintain the off-current targets for a particular technology node, threshold voltages are not scaled down as per Dennard's scaling rule. This in turn prevented supply voltage scaling to have a higher V_{gs}-V_{TH} factor and on-current. Using a higher supply voltage increases the active power. This led to process innovations like mobility enhancement techniques to increase the on-current (Ghani *et al.* (2003)). Complex doping profiles are used around source/drain regions and substrate to reduce off-current due to drain electric field.

Increased complexity in engineering the conventional MOSFETs, the associated in-

crease in cost of this technology and need for better control of the channel by gate, gave rise to multi-gate FETs (MuGFETs). Compared to single gate transistor, MuGFETs provide better control over the channel, as same channel region is being controlled by gate electric field from more than one direction.

1.2.1 What is a FinFET?

Amongst the many proposed multi-gate structures, the one which in production recently is the FinFETs. Named as FinFETs as they resemble the dorsal fin of shark, they were proposed by Sekigawa and Hayashi (1984) and was successfully fabricated by Hisamoto *et al.* (1989). Compared to conventional MOSFETs, FinFETs offer exceptional control over the channel by the gate, resulting in better short channel characteristics(Colinge (2004)).

FinFETs can be made on SOI (Silicon on Insulator) or bulk wafers. FinFETS on bulk wafers have lower initial wafer cost. But SOI FinFETs have almost negligible source/drain to substrate junction capacitance and lower source to drain leakage. In bulk FinFETs the source and drain are connected through the substrate. So it needs an isolation to prevent drain electric field lines from affecting the barrier at the source side. The two methods of isolation possible in bulk FinFETs are material isolation and doping isolation. The first realized FinFET, the DELTA (Depleted Lean channel Transistor), was material isolated. After the fin was formed, source and drain are isolated by forming an oxide at the fin to substrate interface. The commercially produced FinFETs use doping isolation.

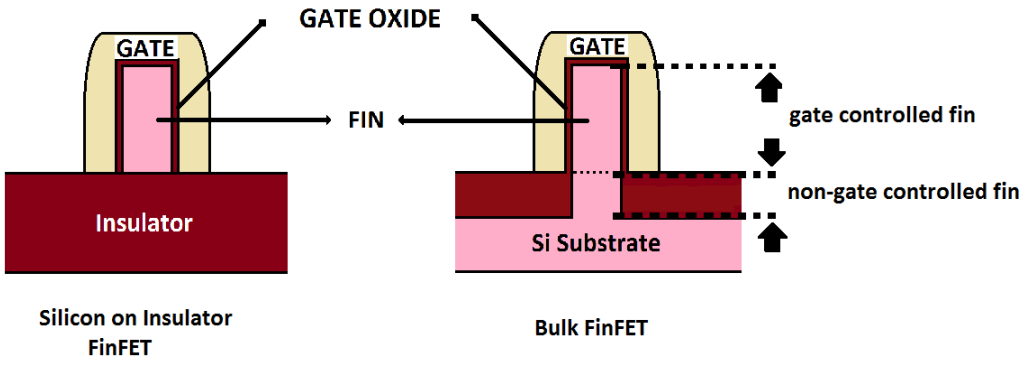

Figure 1.1: Schematics of FinFETs on different substrates

Conventionally, channel length and width of the transistor are scaling parameters, which are scaled down in successive technology nodes to bring down the area of the transistors. But in FinFETs, transistor width is function of fin height and is independent of area scaling: fin thickness is an additional scaling parameter. Figure 1.2 explains the conventions of channel length and width in conventional MOSFETs and MuGFETs.

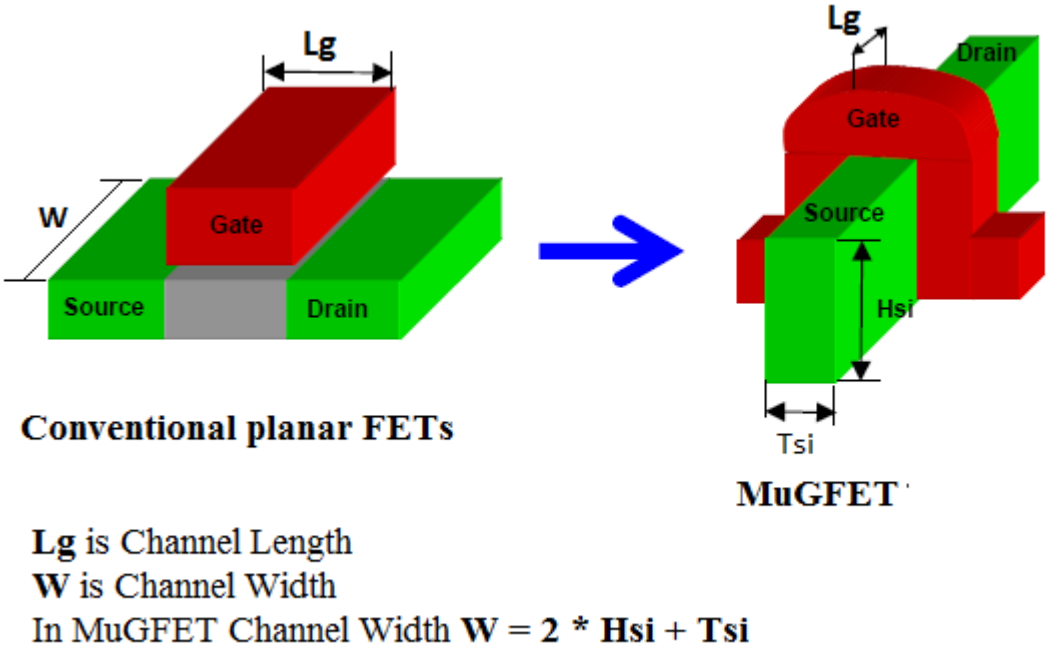

Figure 1.2: Channel length and width in MuGFETs (Kuhn (2008))

1.3 Objective of this thesis

It has become increasingly difficult to increase the I_{dsat} for same I_{off} in MOSFETs (Bohr and El-Mansy, 1998). As discussed, DTMOS is a simpler way to increase the performance without adding processing cost. DTMOS is achieved by connecting gate terminal to the substrate. In DTMOS, the body effect is responsible for the threshold voltage variation (ΔV_T), which increases with increase in substrate doping concentration (Assaderaghi *et al.*, 1997). Since DTMOS operation turned on the source to substrate p-n junction, the supply voltage was limited to 0.7 V. DTMOS operation is explored in FinFETs with doped channel (Han *et al.*, 2006), (de Andrade *et al.*, 2011). However, since the present generation of FinFETs have undoped channels, ΔV_T is very small.

On the other hand, DTMOS devices are now feasible as reduction in supply voltage to sufficiently low values eliminates the problem of substrate current due to the forward biased substrate-source junction. In bulk FinFETs, enabling DTMOS will create a problem as the substrate is common for all FETs. In SOI FinFETs, even though each fin is isolated, making substrate contact is not possible as fin is on oxide. In this work, a novel DTMOS FinFET device with undoped channel and the gate shorted to the substrate is proposed. The proposed device structure is similar to the bulk FinFET, but on a SOI substrate, which is required for isolation between devices.

In our device, source and drain are connected through the bulk. To isolate the source and drain, we have studied four different doping isolation scheme and seven different doping values and found the best isolation technique, ie. the one which gives highest on-current for same off-current. Then we studied DTMOS in best isolation in each scheme.

1.4 Structure of the thesis

The thesis is organized as follows.

- **Chapter 2: Present Generation of MOSFETs**
  This chapter introduces the Field Effect Transistors, how field effect causes transistor action in MOSFETs and the evolution of MOSFETs. Also the issues related to scaling, which led to current generation of MOSFETs are discussed. This is followed by an introduction to FinFETs which are current generation of MOSFETs.

- **Chapter 3: Simulation Details**
  Sentaurus TCAD tool was used for simulating the device. The device was created using Sentaurus structure editor, meshed and required equations were solved by Sentaurus device tool to obtain the device characteristics.

- **Chapter 4: Isolation Schemes to reduce Punch Through Leakage**
  To enable dynamic threshold bulk FinFET is required. But in bulk FinFETs, source and drain are connected through the substrate. So it needs to be isolated using Punch Through Stopper implants. Four different isolation schemes were evaluated.

- **Chapter 5: Dynamic Threshold in FinFETs**
  Problems in making gate connection to substrate in bulk FinFETs and SOI FinFETs led us to propose a novel structure. Dynamic Threshold was seen even in undoped FinFETs and the reason was increase in conduction area modulated by gate bias.

- **Chapter 6: Conclusion**
  The summary of contributions of this work and the scope for future work is presented.

CHAPTER 2

Present Generation of MOSFETs

2.1 Introduction to MOSFETs

2.1.1 Field Effect Transistor

Lilienfeld (1930) proposed a method for controlling electric currents, the idea is to form a conductive channel and control it by external field - Field Effect. Figure 2.1 shows the schematic of the Field Effect transistor.

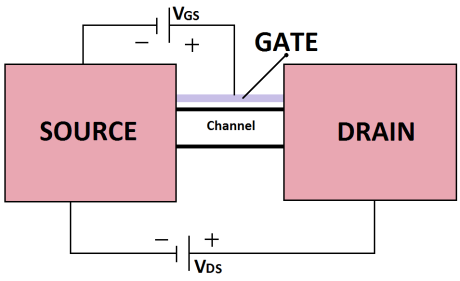

Figure 2.1: Schematic of Field Effect Transistor.

The conductivity of the channel region is modulated by the gate electric field. The gate electric field determines whether or not current flows and also the amount of current through the channel. In transistor OFF state, the channel region offers a very high resistance and so less current flows through the channel. In transistor ON state, the channel region resistance is low allowing large current to flow through the channel.

2.1.2 Metal Oxide Semiconductor FET

MOSFET stands for Metal Oxide Semiconductor Field Effect Transistor. Figure 2.2 shows a n-Channel MOSFET (NMOS). It has p substrate, n^+ source and drain, a di-electric between gate and semiconductor. Gate electric field influences the channel region passing through the gate oxide. Going from source to the drain we have two n-p diodes connected back to back.

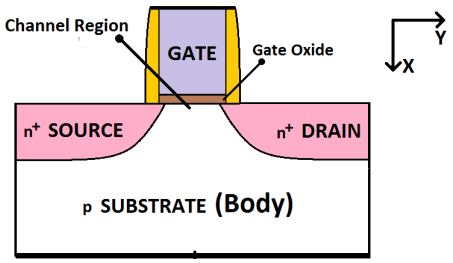

Figure 2.2: Schematic of MOSFET.

The primitive MOSFETs had a metal gate, SiO_2 gate oxide and substrate made of Silicon which is semiconductor, making a MOS structure. SiO_2 was an important reason why Silicon was favored over Germanium for MOSFETs, as making an oxide with such remarkable Oxide-Semiconductor interface on Germanium was not possible. Metal gates had problem of alignment with source/drain overlap which reduced the yield. No overlap of gate over source/drain metal gates will increase the MOSFET resistance in ON condition and decreases the current. So metal gates were replaced with poly Silicon gates, idea being doping source/drain and poly Silicon at the same lithography step. The nature of dopant atoms to diffuse in lateral direction ensures alignment. Kahng (1976) in his review paper on development of MOS technology states that poly Silicon and SiO_2 are the prime reason for the explosion of MOS technology.

2.1.3 MOSFET as a barrier controlled device

Figure 2.3 shows the conduction band energy(E_c) from source to drain terminal, in the channel region near the interface for a n-channel MOSFET. At the source to channel, there is energy barrier for electrons to flow from source into the substrate. Source to substrate junction barrier(many times it is simply referred as source barrier) is the reason for high resistance offered by the MOSFETs in OFF condition. On applying gate electric field, conduction band energy in the channel region is reduced and this barrier is lowered. Physically, this means the channel region becomes depleted of holes at first, and then electrons are injected into the channel region once the barrier is sufficiently lowered. The particular value of gate potential which indicates source barrier is sufficiently lowered is referred as Threshold Voltage (V_{TH}), physically meaning that the

electron concentration in the channel region is now same as the hole concentration in the p-substrate.

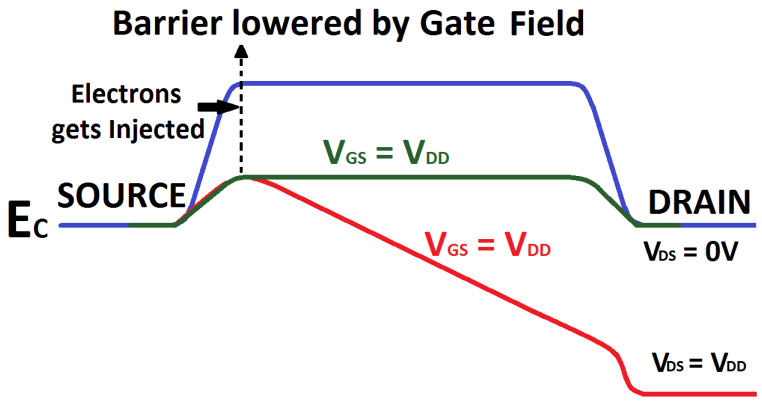

Figure 2.3: MOSFET - A barrier controlled device.

Now a channel consisting of electrons is formed in the surface near the gate oxide to substrate interface and thus MOSFETs offer a very low resistance in transistor ON condition. The electrons in the channel are drifted into the drain terminal by the drain electric field. Applying drain electric field alone, without any gate electric field will not cause any current flow. This is because the barrier in the source to substrate junction can not be lowered by the drain electric field and hence there is no path for the carriers(electrons in NMOS, holes in PMOS) to flow from the source region to the drain region. MOSFET is said to be in ON condition when gate potential is larger than V_{TH} and drain potential is non-zero, OFF condition is when gate potential is smaller than V_{TH}. Body terminal can be used to alter some electrical characteristics of the MOSFET as will be evident later.

2.1.4 Threshold voltage of MOSFET

The threshold voltage of n-channel MOSFET is given as

$$V_{TH} = V_{FB} + 2\phi_B + \frac{\sqrt{2\epsilon_{Si} q N_a (2\phi_B - V_{BS})}}{C_{OX}} \tag{2.1}$$

where V_{FB} is the Flat band voltage given as

$$V_{FB} = \phi_{ms} - \frac{Q_f}{C_{OX}} - \frac{Q_m}{C_{OX}} - \frac{Q_{ox}}{C_{OX}} \tag{2.2}$$

and

$$C_{OX} = \frac{\epsilon_{OX}}{t_{OX}} \tag{2.3}$$

ϕ_B is the difference between Fermi Level of the doped substrate and Intrinsic Fermil Level,

N_a is the substrate doping,

V_{BS} is the substrate potential w.r.t source terminal,

ϕ_{ms} is the difference between fermi Level of gate and substrate,

Q_f is the fixed charge is gate oxide,

Q_m is the mobile charge in the gate oxide,

Q_{ox} is the gate oxide trapped charge,

C_{ox} is the gate oxide capacitance per unit area,

T_{ox} is the gate oxide thickness,

ϵ_{Si} permitivity of Silicon,

ϵ_{ox} permitivity of gate oxide,

$\frac{\sqrt{2\epsilon_{Si}qN_a(2\phi_B - V_{BS})}}{C_{OX}}$ is the depletion charge.

It is important to note that in the threshold voltage expression that only V_{BS} is not fixed by technology. Some of the parameters gets fixed by scaling rule and others by the process technology.

2.1.5 Dynamic Threshold MOSFETs

DTMOS is achieved by connecting gate terminal to the substrate. By doing so, the substrate potential rises as gate potential is increased. As it can be seen from Equation 2.1, that increase in substrate potential lowers the threshold voltage. So when there is no gate bias there will be higher threshold voltage, which is required to have lower off-current. When gate bias is applied, the threshold voltage decreases, which is desired to have higher on-current.

2.2 Advancements in MOSFETs

2.2.1 Issues in short channel MOSFETs

To have elaborated functionalities done by a single chip and with higher speeds, cramming more number of MOSFETs in the same area is done. Consequently, channel length, channel width, lengths of source and drain regions came down. Length of source and drain regions are restricted by dimensions required to make a good enough metal contact. These dimensions do not influence the electrical characteristics of the MOSFET significantly. Channel length scaling directly affects the electrostatics in the channel region. Shorter channel length meant the lateral drain electric field exceeded the critical electric field which can cause velocity saturation of carriers in the channel region. This high electric field can accelerate the carriers to an instantaneous velocity which is higher than the saturation velocity(called as Hot carriers), meaning these carriers are now with higher energy, causing Hot Carrier Effects. Hot Carriers cause impact ionization near the drain region causing electron-hole pair generation leading to increase in drain current. Drain current must be controlled only by gate field, and drain field influencing the drain current is not desired. Hot carriers can also penetrate the gate oxide, get stuck in the oxide thus altering the threshold voltage besides increasing the gate leakage. This is fixed by having a Lightly Doped drain(LDD) as shown in the Figure 2.4 and by reducing the supply voltage. The depletion width of drain to substrate gets spread, reducing the peak electric field in the channel.

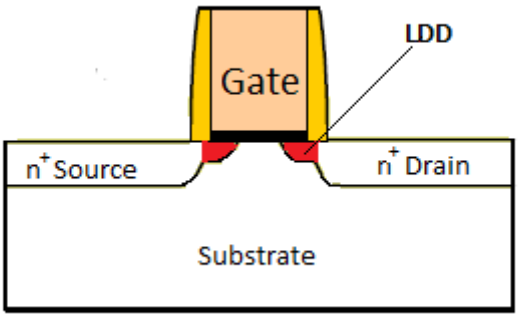

Figure 2.4: Lightly Doped drain to reduce the peak electric field in the channel.

Also shorter channel length increased the influence of drain electric field in the channel region and thereby decreasing the gate electric field's control over the channel as evident

from Poisson equation.

$$\frac{dE_x(x,y,z)}{dx} + \frac{dE_y(x,y,z)}{dy} + \frac{dE_z(x,y,z)}{dz} = Constant. \tag{2.4}$$

where,

E_x is electric field in vertical direction - gate electric field,

E_y is electric field in channel direction - drain electric field,

E_z is electric field in transistor width direction.

In the channel region, the entire depletion charge and the inverted carrier charge should be controlled by the gate electric field. But as the channel lengths became shorter, the drain potential is getting dropped in shorter distance, the spatial variation in drain electric field in the channel region can not be neglected. So, for short channel devices the channel charge became a function of drain electric field resulting in undesired DIBL and SCE.

In conventional MOSFETs, $\frac{dE_z(x,y,z)}{dz}$ is almost zero. If we have lateral gates also, $\frac{dE_z(x,y,z)}{dz}$ will be non-zero and the control of gate over the channel charge is increased.

Drain Induced Barrier Lowering

In shorter channel devices, the source barrier height is impacted the drain electric field and is lowered because of drain electric field. Drain Induced Barrier Lowering gives the measure of how much the barrier in the source side is impacted by the drain electric field. It is calculated as difference in threshold voltage when drain voltage is 50 mV and V_{dd}, normalized to 1 V. It is measured in mV/V(mV change in V_{TH} for 1V change in drain voltage).

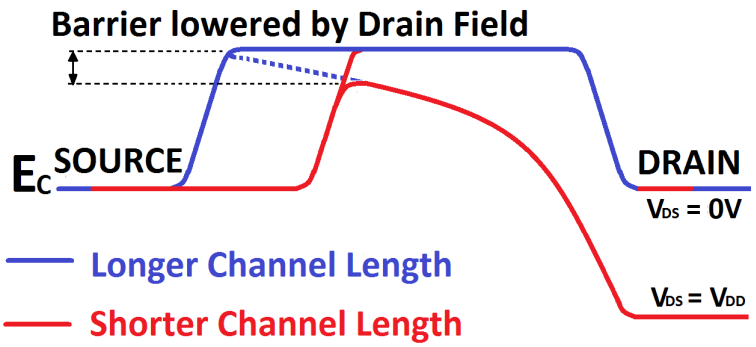

Figure 2.5: Illustration of Drain Induced Barrier lowering in short channel devices.

The blue line is the conduction band energy from source to drain along the channel in a longer channel device, solid blue line is under zero gate and drain potential, and the dotted blue line is for non-zero drain potential. In long channel devices, gate electric field is zero and in the presence of only drain potential, there is no change in barrier height in the source side. It can be seen that the change in barrier height is small for the blue line. The red line is for a shorter channel device, the dotted line has smaller barrier compared to the thick line, indicating the source barrier being reduced by drain electric field itself. This effect is prominent in regions below the channel where the gate electric field variation will be less (gate control will be less) and causes current to flow without gate control - $\boldsymbol{I_{off}}$ increases. In order to reduce the DIBL, the barriers of source/drain to substrate below the channel region is increased by having the p^+ implant, referred as Halo.

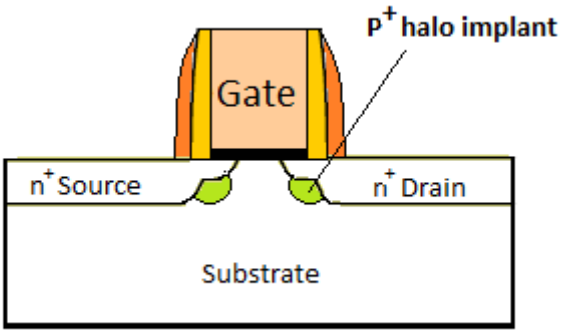

Figure 2.6: Halo doping to reduce DIBL.

Short Channel Effect

Because of the p-n junctions of source to substrate and drain to substrate, the depletion charge in these junctions come below the gate region also. Some part of depletion charge which is supposed to be controlled by the gate entirely is now being contributed source/drain depletion charge. This proportion of charge is larger for shorter channel devices.

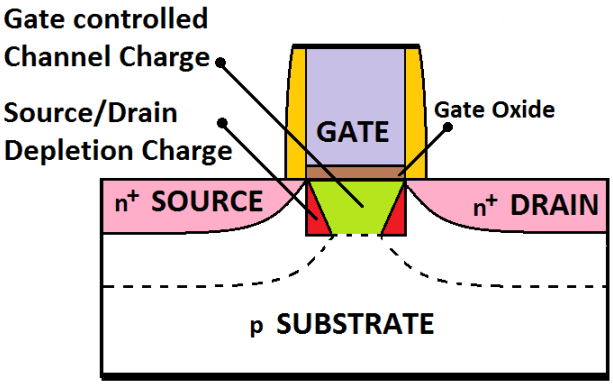

Figure 2.7: Illustration of Short Channel Effect

In regions farther away from gate, where the gate influence is lesser, drain electric field can cause DIBL significantly and increases I_{off}.

Both DIBL and SCE increases the I_{off}. In order to meet the I_{off} targets for a particular technology node, the threshold voltage needs to be increased. But increasing the threshold voltage will decrease the I_{dsat}, to maintain higher I_{dsat} V_{dd} should be kept high, that in turn increases the power dissipation.

2.2.2 Changes in gate stack

To have a good transistor operation, the gate should have greater control over the channel compared to drain. This can be achieved by decreasing the thickness of the gate oxide. But with scaling, gate oxide thickness has decreased so much that it increases the tunneling through the gate oxide. Direct tunneling of carriers from channel through the oxide into the gate has exponentially dependence on gate oxide thickness (Lo *et al.*, 1997). Also increase in field in the oxide increases the Fowler Nordheim tunneling.

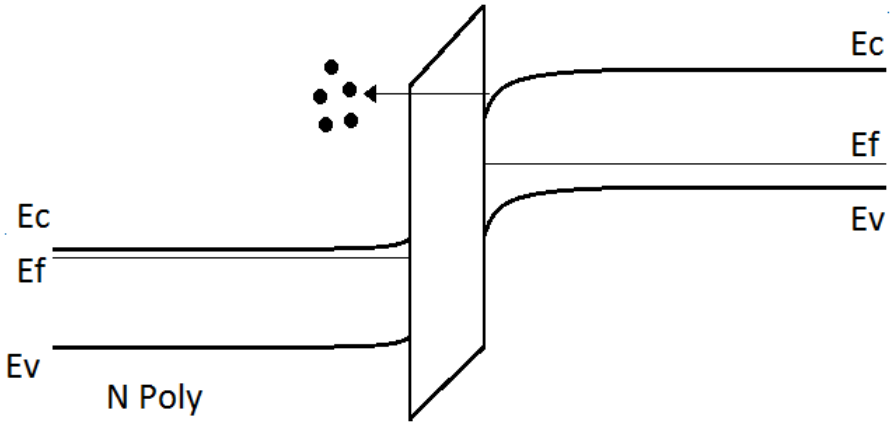

Figure 2.8: Electron tunneling through gate oxide

To decrease the gate tunneling current, high permitivity (high K) gate oxides are used. Higher permitivity gate oxide allows to have much thicker oxide compared to SiO_2 without compromising the gate control. But the gate oxide to Silicon interface still has SiO_2 because of its unmatched interface quality.

High K gate oxides have the problem of Fermi level pinning (Hobbs *et al.*, 2004) and mobility degradation (Robertson, 2004) when used along with Poly Silicon gates. So this mandated change to metal gates, and with the advancement in technology, alignment is no more an issue which plagued the primitive MOSFETs with metal gates. Use of metal gate also eliminates the poly depletion capacitance, improving the inversion region capacitance and thus increasing the on-current. High K gate oxides have other problems like thermodynamic stability and lower bandgaps (Wong and Iwai, 2006).

2.3 Evolution from Single gate to MOSFETs Multi-gate MOSFETs

2.3.1 Multi-gate FETs

From Equation 2.4, it is clear that one way of reducing the effect of spatial variation of drain electric field, is to have spatial variation of electric field in z-direction also. In a conventional MOSFETs, the electric field in z-direction is almost zero. In Multi-gate FETs we accomplish spatial variation of electric field in z-direction also, by having additional gate electrodes. Hence, the contribution of gate electric field in the Poisson equation is much larger compared to conventional MOSFETs, and hence, most of the channel charge is now controlled by gate electric field. In the Figures 2.9, 2.10 violet color region is the channel.

Having better electrostatic control over the channel reduces the off-current and static power dissipation. As illustrated in Figure 2.11, for same threshold voltage we will have lower leakage or for same leakage we can reduce the threshold voltage and have same on-current at reduced supply voltages. Reducing the supply voltage will reduce the power dissipation.

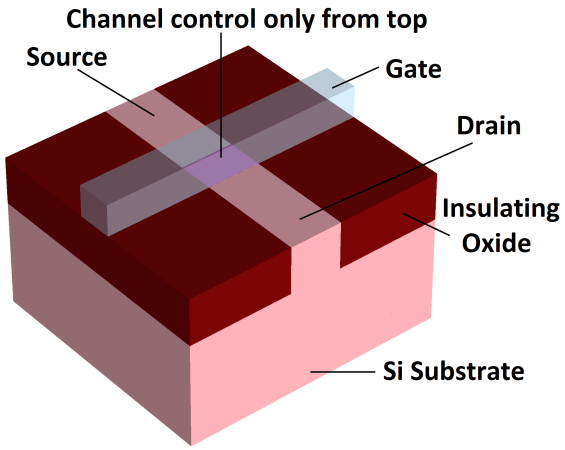

Figure 2.9: Channel in a conventional MOSFET

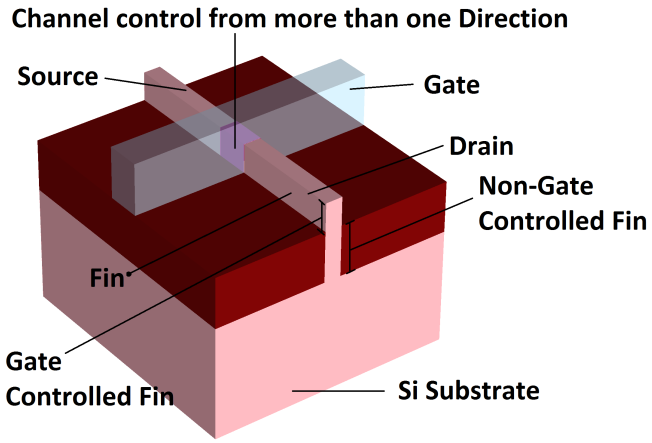

Figure 2.10: Channels in a Trigate FET

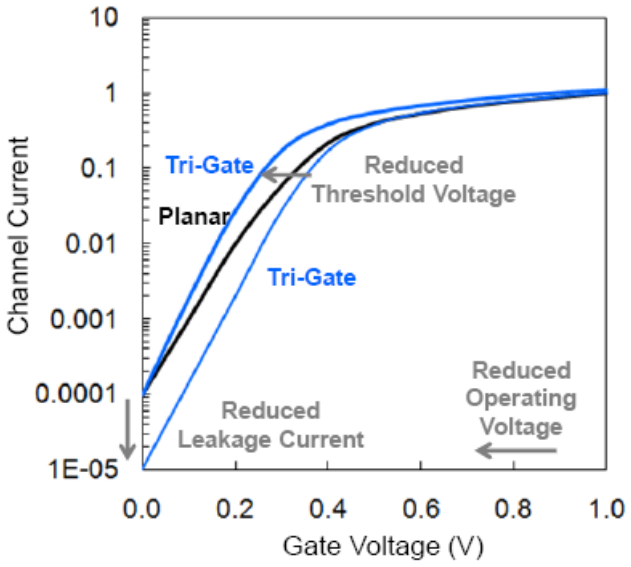

Figure 2.11: Comparison between the I_d Vs V_{gs} characteristics of trigate and planar technology (http://www.realworldtech.com)

2.3.2 Present generation of MOSFETs

FinFETs is the most advanced device architecture in MOS technology. FinFETs have lightly/undoped channel region, and thus show significant reduction in Random Dopant fluctuations (RDF). RDF is proportional to the doping in the channel region, and is a concern in conventional MOSFETs. Lightly/undoped channel region is possible only because of the exceptional control of the channel region by the gate electric field. Because of high degree of gate control, FinFETs show remarkably lower DIBL and near ideal subthreshold slope.

As the channel region is lightly doped, they become fully depleted in the presence of gate field. As the channel doping is less, depletion charge is negligible compared to conventional MOSFETs, and doesn't play any role in determining the threshold voltage of the device. So it needs a gate work function in middle of the silicon bandgap as opposed to band edge work functions requirements of conventional MOSFETs. Different work functions for NMOS and PMOS are achieved by using tunable metal gates (Liu *et al.*, 2006).

In conventional/planar MOSFETs, channel lies only in the surface. In FinFETs, if the thickness of the fin is smaller than 20 nm, the maximum electron density will occur in the middle of the channel region (Colinge, 2004) and not along the surface. This leads to increase in mobility as scattering from the surfaces and various oxide charges are lesser. Lightly doped channel also increases mobility as there is much lesser scattering from channel dopant atoms. Thinner fins are desired for better gate control. But much thinner fin will suffer from mobility degradation because of increase in inter-carrier scattering as we will have high electron density in the fin and increased extrinsic resistance (Auth *et al.*, 2012).

FinFETs offered huge technological challenges (Kuhn, 2008) starting from patterning of the fin, process challenges with non-planar structures, implementing NMOS/PMOS strain and requirement for very tight process control to minimize variation between fins.

The disadvantage for a circuit designer designing with FinFETs is the quantization of the width of the transistor (Gu *et al.*, 2006). In FinFETs, the channel width is dependent on height of the gate controlled fin region which can't be altered. For higher channel widths, more number of transistors are connected in parallel, and designers can have channel widths integer multiples of channel width of a single transistor.

CHAPTER 3

Simulation details

Sentaurus TCAD tools are used for device simulation.

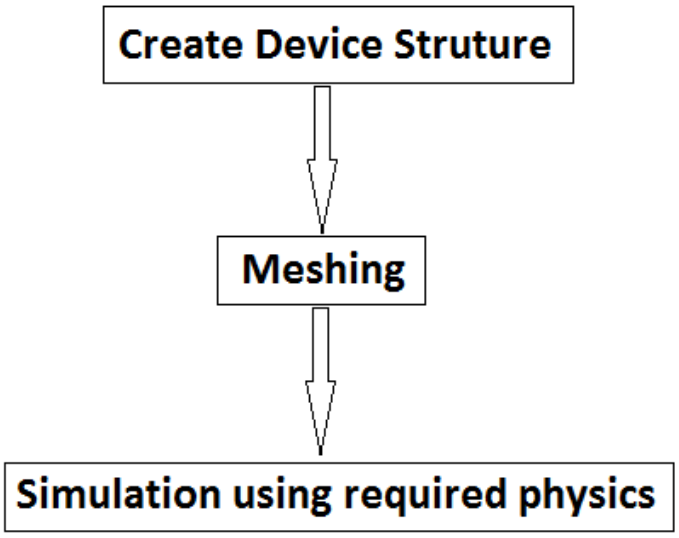

Figure 3.1: Flow chart for simulating devices.

Flow chart for simulating devices using Sentaurus TCAD tools is shown in Figure 3.1. Device is created using the Sentaurus Structure editor. Then the device is divided into infinitesimal small volumes (this is called meshing) to solve for the necessary equations. Finally, the poisson and transport equations are solved along with the appropriate physics for the carriers to obtain the device characteristics.

3.1 Simulated Device structure

First step is to create the needed device structure using Senaturus Structure editer (sde). The script for creating the device is written in sde and the created device file is in .tdr format. This .tdr file is given as input to Sentaurus Device to solve for the required physics. Figure 3.2 is the device structure used for our simulations.

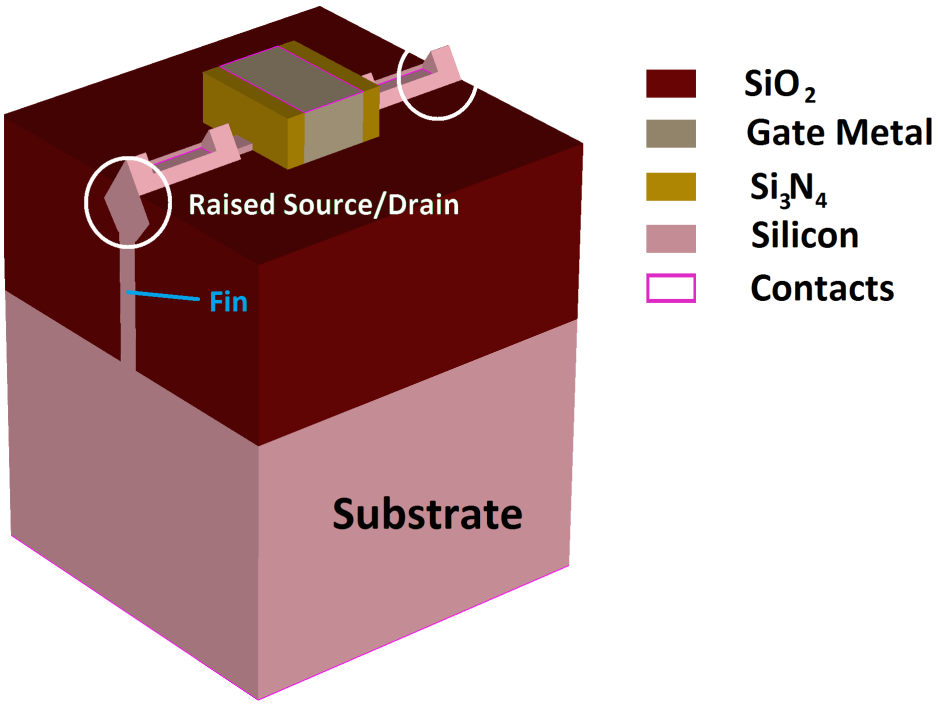

Figure 3.2: 3D view of the simulated NMOS device.

The device dimensions are,

channel length = 31 nm

gate controlled fin height = 25 nm

non-gate controlled fin height = 60 nm

fin thickness = 10 nm

substrate height = 120 nm

channel width = 60 nm (2 * fin height + fin thickness)

gate oxide HFO_2 and SiO_2 combined EOT = 1 nm

fin doping = 10^{13} cm^{-3} same as that of substrate, dopant is Boron

source and drain doping = 10^{20} cm^{-3} of Arsenic

Constant doping with a decay slope of 2 nm/decade is assumed for source/drain doping. The isolation oxide is kept almost till the fin height to account for the fringe fields from gate and drain regions. Compared to having isolation oxide along the sides of raised source/drain, having no isolation oxide around the raised source/drain gives lesser off-current

3.1.1 Fin dimensions

The reported channel length and EOT of Intel's 22 nm Trigate device are 34 nm and 0.9 nm respectively (Auth *et al.*, 2012). In the simulated devices, the channel length is decreased and EOT is increased by 10% to compensate for the improved performance observed in simulations due to ideal doping profiles and geometries.

Gate controlled fin height, non-gate controlled fin height, and fin thickness dimensions are similar to Intel′s 22 nm device. But important difference is that Intel′s fin is triangular in shape, and we used a rectangular fin in our simulations as having a curved structure increases the number of mesh points alarmingly. Also, a rectangular fin is desired (Kavalieros *et al.*, 2006).

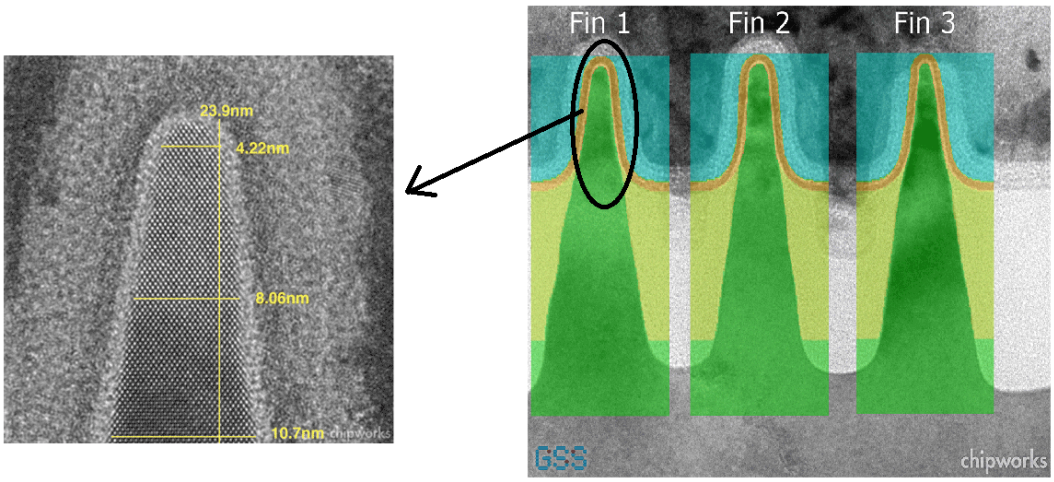

Figure 3.3: Intel′s 22nm fin and its dimensions as reported by Gold Standard Simulations.

3.1.2 Raised source and drain

The raised source/drain is similar in shape to that of Intel′s 22 nm device. The SEM image in Figure 3.4 is Intel′s 22 nm Raised source/drain and the structure on the right is the raised source/drain of our device. Raised source/drain is used to reduce series resistance (Auth *et al.*, 2012) and has depth till the gate controlled fin.

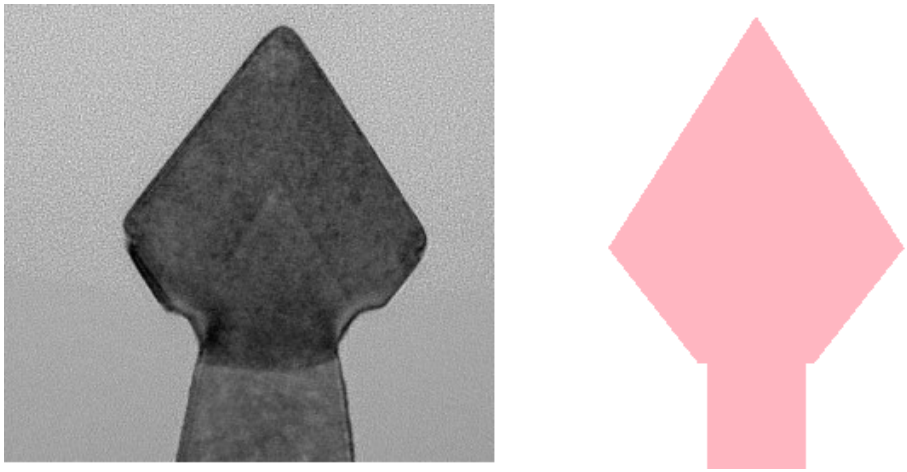

Figure 3.4: Comparison in shapes between raised source/drain of our device and Intel's 22 nm device.

3.1.3 Gate stack

EOT (Equivalent Oxide Thickness) is the equivalent thickness of SiO_2 which allows the same electric field as that of high K gate oxide. We have used an EOT of 1 nm, in HfO_2 and SiO_2 combination. HfO_2 thickness of 2 nm and SiO_2 thickness of 0.7 nm are used. SiO_2 is directly on the Silicon, followed by HfO_2, followed by gate. Gate is of Metal having work function in the middle of Silicon bandgap. The work function of the gate metal is varied to achieve different threshold voltage.

$$EOT = t_{highK}\left(\frac{\epsilon_{SiO_2}}{\epsilon_{highK}}\right) \tag{3.1}$$

where,

ϵ_{SiO_2} - is permitivity of SiO_2,

ϵ_{highK} - is permitivity of high K gate oxide, HfO_2 in our case,

t_{highK} - is thickness of high K gate oxide.

3.2 Meshing of device

It is required to divide the device into infinitesimal volumes to solve for semiconductor equations in the device. This process is called Meshing. Mesh size should be smaller where the spatial variation in electric field is large. So channel regions, drain region, p-n junction of source/drain to PTS have much smaller size meshes. Isolation oxide,

deep into substrate where the field variation is smaller are meshed at larger size.

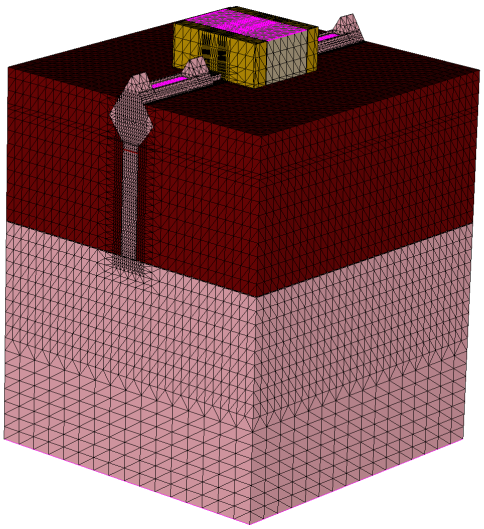

Figure 3.5: 3D view of the meshed device.

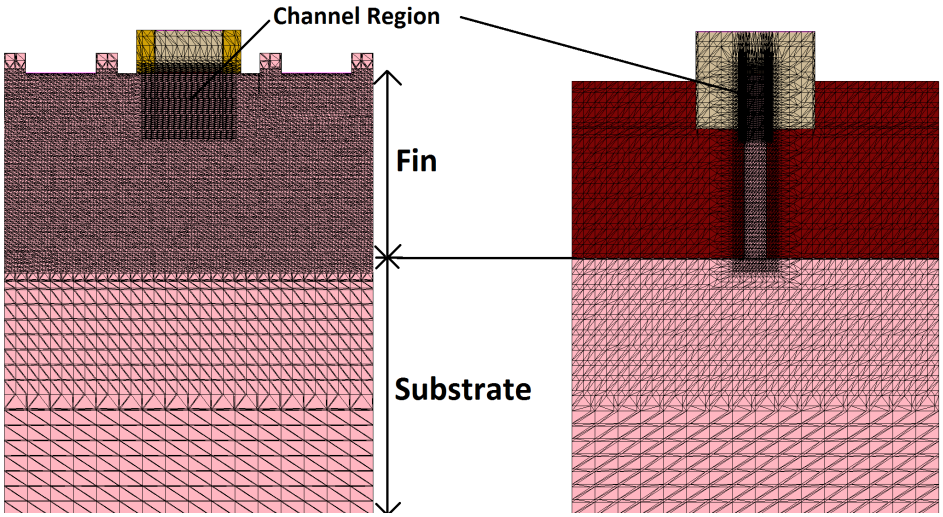

Figure 3.6: Meshing along different cross sections.

In Figure 3.6, the left meshed structure is cross section along channel (along the current flow direction), and one in the right is the cross section perpendicular to the channel (perpendicular to the current flow direction).

3.3 Physics used for device simulations

For device simulations we used Fermi statistics, drift diffusion transport model, Philips mobility model with doping dependence and lateral field dependence (Canali model),

Darwish model for normal field dependence, Schenk band to band tunneling model (Schenk BTBT model), Slotboom bandgap narrowing, Shockley Read Hall recombination with doping and electric field dependence and solved Poisson electron and eQuantumpotential equations.

Fermi Statistics - governs the carrier generation and recombination.

Drift diffusion transport model - governs the carrier transport under all possible scenarios. In subthreshold regime the current is dominated by diffusion-current and above threshold it is mostly drift current.

Philips mobility model with doping dependence and lateral field dependence - accounts for mobility degradation due to doping and carrier velocity saturation due to high lateral field.

Darwish model for normal field dependence - accounts for mobility degradation due to normal field, resulting from increased carrier scattering due high carrier density, accomplished by high normal field. By default, Darwish model (also known as Lucent model) is not available in Sentaurus. Lomardi model with Darwish parameters (Darwish *et al.*, 1997) makes it Darwish model.

Schenk band to band tunneling model - accounts for band to band tunneling in the PN junctions of source/drain with PTS and gate induced BTBT in the drain overlap.

Slotboom bandgap narrowing - Doping values higher than 10^{18} cm^{-3} narrows the Silicon bandgap, thereby altering the carrier statistics, Slotboom bandgap narrowing model is invoked to account for the same.

Shockley Read Hall Recombination with doping and electric field dependence - governs the recombination statistics of the carriers.

eQuantumpotential correction accounts for band gap discretization due to carrier confinement in the thin silicon fin and also because of electric field. These Quantum mechanical effects are included as correction to the local potential.

3.4 Measuring Threshold voltage, DIBL and Subthreshold slope

Threshold voltage and Subthreshold slope are extracted using built in libraries in the inspect tool of Sentaurus. In fully depleted MOSFETs, the physical explanation of thresh-

old voltage as the gate potential when inverted carrier concentration becomes same as the majority carriers in the substrate is not valid. Also in fully depleted MOSFETs, the depletion charge will be too less and doesn't contribute to threshold voltage. Threshold voltage is measured by constant current method (which is common method in industry to measure threshold voltages), the reference current was taken as 100 nA * (Transistor width/Channel Length) as stated in (chapter 6 in Chenming (2010)). For the channel length and width of our device, the reference current comes to be 1.935x10^{-7} A.

As said earlier, DIBL is calculated as difference in threshold voltage when drain voltage is 50 mV and V_{dd}, normalized to 1 V. It is measured in mV/V (mV change in V_{TH} for 1V change in drain voltage).

Subthreshold slope is extracted from the I_s Vs V_{gs} curve(from source current Vs gate voltage as done in industry). It is the slope of the curve at V_{gs} of 50 mV.

3.5 Calibration of Simulator

As the channel length of our device is comparable to mean free path of carriers, the carries experience reduced scattering. Also the strain engineering techniques used to increase mobility reduces carrier scattering. To account for the above factors in our simulated device, the V_{sat} and beta values in the Sentaurus TCAD simulator are adjusted to 2.2x10^7 cm^2/V-s and 1 respectively (Bude, 2000), (Granzner *et al.*, 2006). We also benchmarked our device against Intel′s 22 nm device. Intel′s standard power device has an on-current of 710 μA/μm and off-current of 1000 pA/μm (Jan *et al.*, 2012). Our device at same off-current has on-current of 660 μA/μm.

CHAPTER 4

Isolation Schemes to reduce Punch Through Leakage

For DTMOS, we need to connect gate to the substrate. In SOI FinFETs, making substrate contact is not possible as the fin is on oxide. A bulk FinFET is required to make substrate contact. In a bulk FinFET, the source and drain are connected through the substrate. The absence of doping in the non-gate controlled fin allows the drain potential to lower the barrier at source side and it increases the I_{off}. Isolating the source and drain using Punch Through Stopper (PTS) implants to reduce this leakage current is important. We studied four different isolation schemes in doping isolation technique and seven doping values. The doping considered are 10^{20} cm^{-3}, 10^{19} cm^{-3}, 5x10^{18} cm^{-3}, 2.5x10^{18} cm^{-3}, 10^{18} cm^{-3}, 5x10^{17} cm^{-3} and 10^{17} cm^{-3}. Constant doping with a decay slope of 2 nm/decade is assumed.

Without any isolation of source and drain, most of the I_{off} flows through non-gate controlled fin region near the gate controlled and non-gate controlled fin interface. There is lower leakage current through the gate controlled fin region. Under no isolation condition, the drain electric field has much stronger influence in the non-gate controlled fin region. This reduces the source barrier, resulting in large I_{off}.

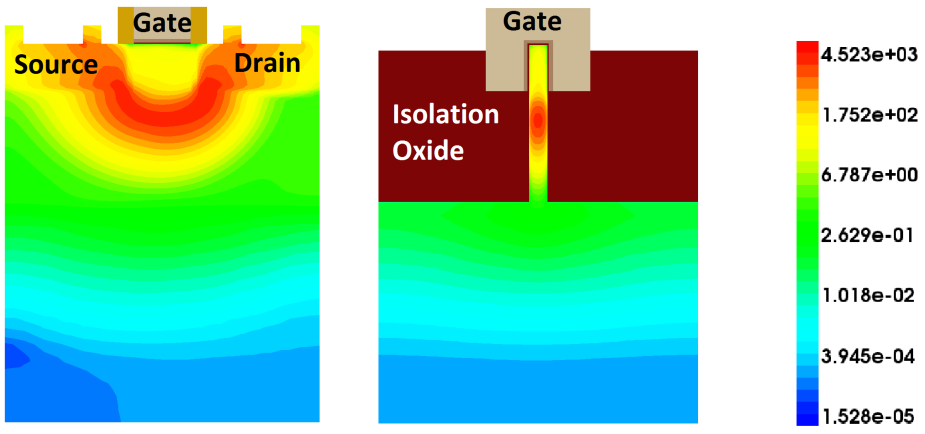

Figure 4.1: Leakage current in A/cm-2 at Vgs = 0 V and Vds = Vdd along different cross sections when there is no isolation between source and drain.

4.1 Four different isolation schemes

Figure 4.2 lists the four different Punch Through Stoppers studied by us. For different values of doping, the best device from each scheme is found. The best device is the one that gives highest I_{dsat} for same value of I_{off}.

Case A:

Case A is the Punch Through Stoppers found in literature, for doped FinFETs (Okana *et al.*, 2005) as well as for undoped FinFETs (Manoj *et al.*, 2007). But, this type of PTS in undoped fin poses problems like high source/drain to substrate junction capacitance and Random Dopant Fluctuations (RDF). RDF causes mismatch between transistors, resulting from the statistical nature of the change in threshold voltage due to variable number of PTS dopant atoms entering the gate controlled fin. The volume of the gate controlled fin is small, very few PTS dopant atoms are sufficient to create large threshold voltage variations. This mismatch is more pronounced as the supply voltages are scaled down.

Case B:

This PTS is aimed at addressing the RDF issue. Though it doesn't entirely eliminate the problem, it will reduce it as we are not doping the region below the gate controlled fin. It is still possible for the dopant atoms below the source/drain regions, that are close to the gate controlled fin to enter the gate controlled fin. But, similar to case A, this PTS has the problem of junction capacitance.

Case C:

This PTS reduces the source/drain to substrate junction capacitance as there is no PTS below the source/drain regions. But, the RDF issue still exists.

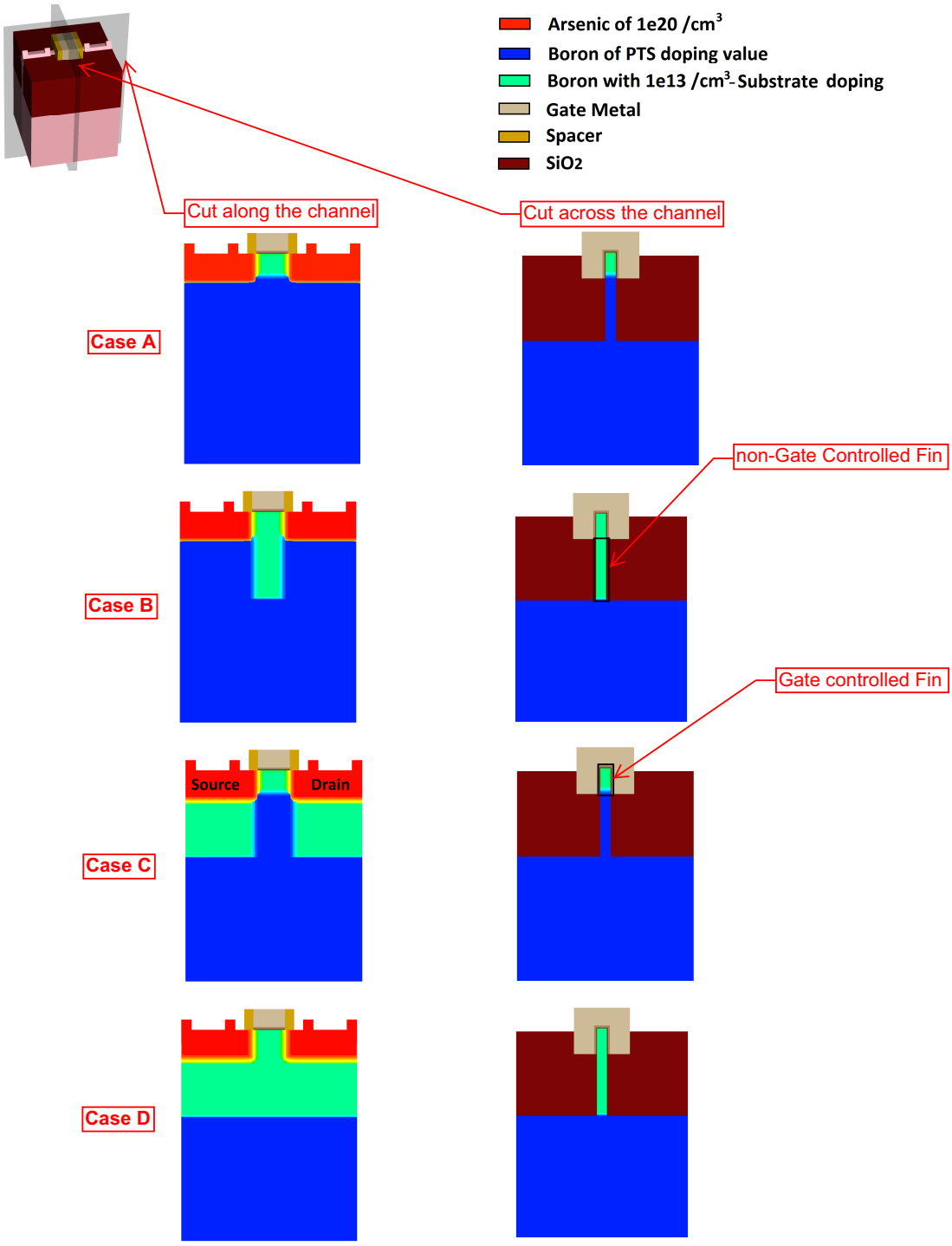

Figure 4.2: The four different isolation schemes.

Case D:

This PTS is easy to achieve (doping the fin region is not easy (Okana *et al.*, 2005)), as we are not doping the narrow fin. Case D will not have RDF, as there is no doping in non-gate controlled fin. As PTS is farther away from the gate controlled fin, it needs

a high value of doping to stop the leakage. For reasons which will be explained later, moderate value of PTS is desired in cases A,B and C. In case D, the depletion width ends just where substrate starts because of very high doping in the substrate. In other cases, if the source/drain to substrate junction depletion widths extend into the substrate through the fin, then case D will have higher junction capacitance.

It should be noted that presence of PTS dopant atoms below the gate controlled fin region is not a mandate. All that is required is to increase the conduction band energy in the non-gate controlled fin region near the gate controlled fin region. Increasing the conduction band energy in these regions will increase the barrier at the source and will reduce the leakage due to drain field. So even cases B and D can stop leakage.

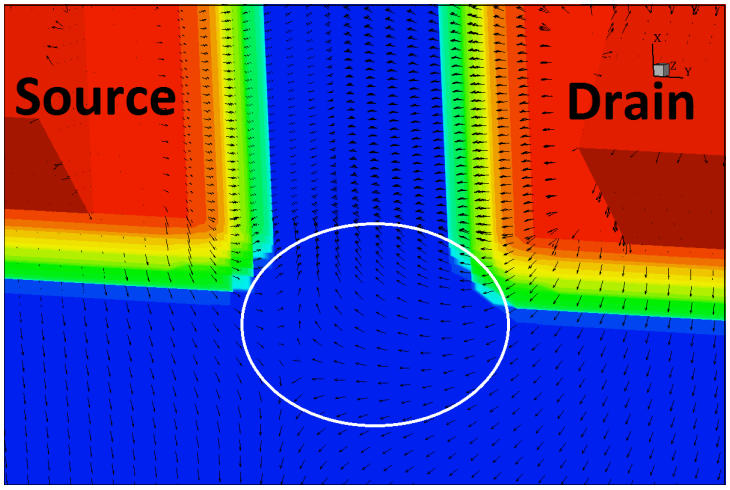

Figure 4.3: Field lines without isolation at V_{gs}=0V and V_{ds}=V_{dd}

It can be seen that in the encircled region the drain electric field lines are able to reach the source region, causing punch through.

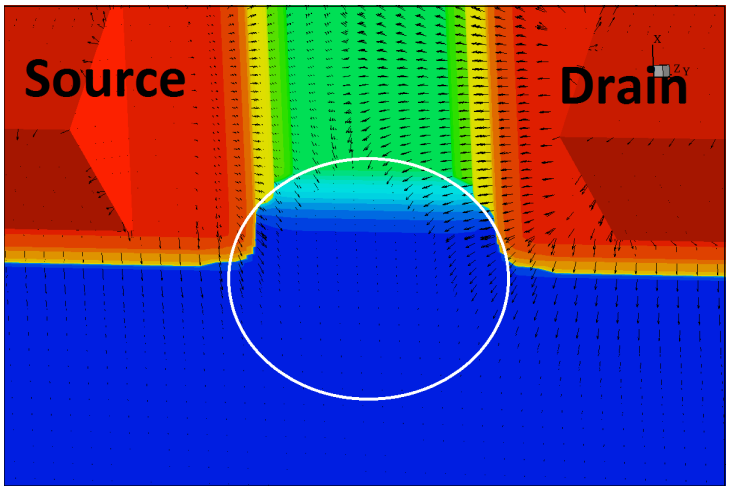

Figure 4.4: Field lines with Isolation at V_{gs}=0V and V_{ds}=V_{dd}

As can be seen in Figure 4.4, electric field lines from drain are stopped from reaching the source by the PTS.

4.2 Analysis of four PTS schemes

The best isolation is the one that gives highest on-current for same off-current. To compare devices for same off-current, threshold voltage of the device is varied by changing the gate work function and I_{off} (in $pA/\mu m$ in log scale) Vs I_{dsat} (in $\mu A/\mu m$) is plotted. For a fixed I_{off}, the device farthest to the right is the best device ie. the one with the highest I_{dsat} for fixed I_{off}.

4.2.1 Very high value of doping

PTS with doping values higher than 10^{19} cm^{-3} in cases A and B increases the I_{off} as a result of band to band tunneling (BTBT). BTBT is much higher in the drain side because of the reverse biased drain to substrate p-n junction. In case C, there is very little BTBT, as there is no highly doped p-n junction below the source/drain. Little BTBT in case C is due to the small overlap between the PTS and the source/drain near the gate controlled fin. In case D, there is no chance for BTBT, as the highly doped PTS is far away. As the PTS is farther away in case D, high value of PTS doping is required to stop leakage.

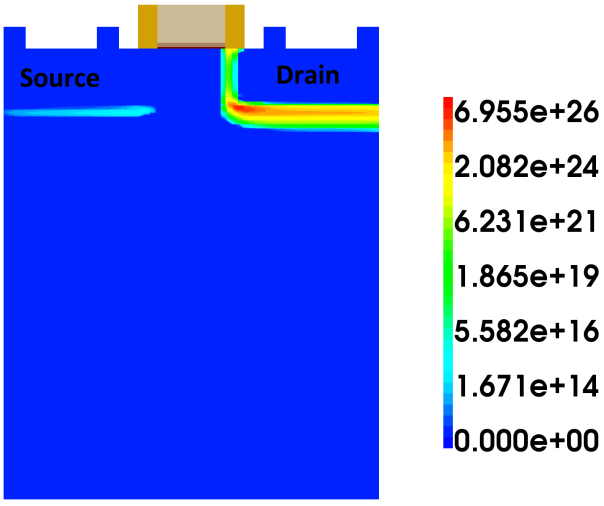

Figure 4.5: Band to Band tunneling in $cm^{-3}s^{-1}$ in case A PTS doping of 10^{19} cm^{-3} at V_{gs}=0V and V_{ds}=V_{dd}.

4.2.2 Moderately high value of doping

PTS with doping values higher than 10^{18} cm^{-3} in cases A, B and C increases the conduction band energy in the non-gate controlled fin region. This results in higher energy barrier at the source, near the gate controlled and non-gate controlled fin interface and thus reduces I_{off}. This increase in the conduction band energy in the non-gate controlled fin region extends into the gate controlled fin region and increases the local threshold voltage in those regions.

As seen in the Figure 4.8, there is no difference in conduction band energy between PTS doping of 2.5x10^{18} cm^{-3} and 5x10^{17} cm^{-3}. But as seen in the Figure 4.7, along the lower part of gate controlled fin, PTS doing of 2.5x10^{18} cm^{-3} has higher conduction band energy and so higher source barrier, and consequently, a higher local threshold voltage. This leads to reduction in electron-current density in lower part of gate controlled fin regions. So, in ON condition, current doesn't flow through the entire gate controlled fin region. As shown in Figure 4.8, in case of PTS doping of 2.5x10^{18} cm^{-3} there is no current flow through the lower part of gate controlled fin. For higher values of PTS doping, electron current density in lower part of gate controlled fin reduces further. But on the positive side, it also brings down the off-current.

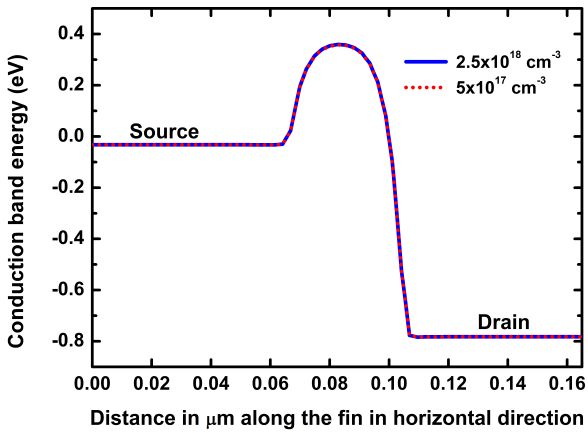

Figure 4.6: Conduction band energies in case A PTS doping of 2.5x10^{18} 5x10^{17} cm^{-3} at V_{gs}=0V and V_{ds}=V_{dd} along cut upper part of gate controlled fin.

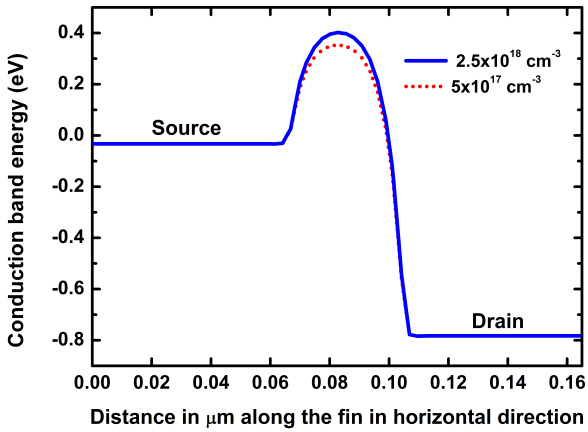

Figure 4.7: Conduction band energies in case A PTS doping of 2.5x10^{18} 5x10^{17} cm^{-3} at V_{gs}=0V and V_{ds}=V_{dd} along cut lower part of gate controlled fin.

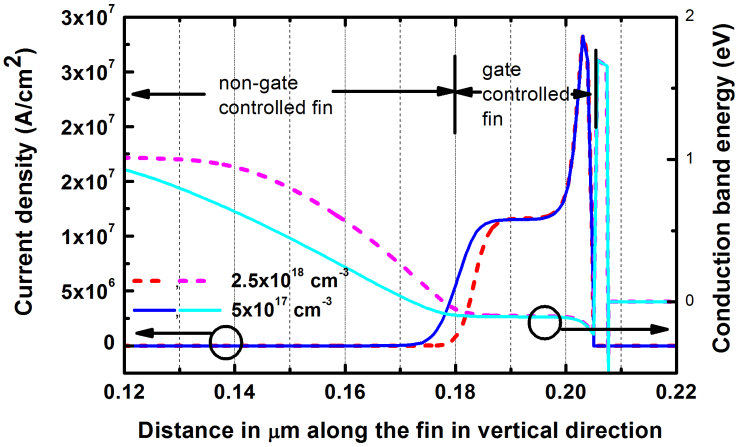

Figure 4.8: Conduction Band Energies snd electron-current density for PTS of case A 2.5x10^{18} cm^{-3} and 5x10^{17} cm^{-3} at V_{gs}=V_{dd} and V_{ds}=V_{dd} along vertical cut.

In Figure 4.8, dotted majenta line shows the conduction band energy in case A PTS doping of 2.5x10^{18} cm^{-3}. It is higher in the lower part of the gate controlled fin region. The red dotted line which is the electron-current density of case A PTS doping of 2.5x10^{18} cm^{-3} shows there is no current flow in lower part of the gate controlled fin.

4.2.3 Moderate value of Doping

As seen in Figure 4.8, moderate value of doping, such as 5x10^{17} cm^{-3}, shows almost no change in conduction band energy in the gate controlled fin region. So in ON condition, this allows current conduction through all of gate controlled fin region. Also the conduction band energy increases in the non-gate controlled fin and reduces the leakage current. But it doesn't reduce I_{off} effectively compared to higher values of PTS

doping. PTS doping value of 10^{18} cm^{-3} in cases A and C allows conduction through almost all of the gate controlled fin but not as much as 5x10^{17} cm^{-3}. So in cases A and C, 5x10^{17} cm^{-3} was the best PTS. But in case B, as there are no PTS dopant atoms directly below the gate controlled fin, it needs slightly higher value of PTS doping than 5x10^{17} cm^{-3} to reduce leakage current. In case B, PTS doping of 10^{18} cm^{-3} gives optimum of allowing current through entire gate controlled fin and reducing the leakage current.

4.2.4 Low value of doping

Low value of PTS doping in cases B and C (PTS with doping value of 10^{17} cm^{-3}) is not efficient in reducing the I_{off}. But in case A, it is able to reduce leakage better than cases B and C. The reason is, in case A, PTS is there in non-gate controlled fin and also below source/drain. So drain electric field lines starting from close to non-gate controlled fin as well as directly below drain are stopped.

Varying the threshold voltage changes both the ON and off-current. To compare on-current for same off-current, the threshold voltage is changed by varying the gate work function (WF). Gate work functions of 4.41 eV, 4.45 eV, 4.49 eV are used. On and off-currents of the three best devices from each case is tabulated and plotted.

Table 4.1: **Case A**

PTS doping value in cm^{-3},gate work function	I_{dsat} in A	I_{off} in A	V_{th} in V	SS in $mV/decade$	I_{dsat} $\mu A/\mu m$	I_{off} $\mu A/\mu m$
10^{18}cm^{-3}, WF 4.41 eV	4.324x10^{-5}	1.882x10^{-10}	0.195	63.979	720.635	3135.933
10^{18}cm^{-3}, WF 4.4 0eV	3.873x10^{-5}	4.446x10^{-11}	0.235	63.875	645.453	741.020
10^{18}cm^{-3}, WF 4.49 eV	3.431x10^{-5}	1.051x10^{-11}	0.275	63.842	571.890	175.125
5x10^{17} cm^{-3}, WF 4.41 eV	4.472x10^{-5}	2.442x10^{-10}	0.19	64.954	745.357	4070.383
5x10^{17} cm^{-3}, WF 4.45 eV	4.014x10^{-5}	5.943x10^{-11}	0.23	65.026	669.057	990.478
5x10^{17} cm^{-3}, WF 4.49 eV	3.566x10^{-5}	1.456x10^{-11}	0.27	65.236	594.270	242.635
10^{17} cm^{-3}, WF 4.41 eV	4.661x10^{-5}	4.310x10^{-10}	0.182	68.643	776.810	7183.717
10^{17} cm^{-3}, WF 4.45 eV	4.196x10^{-5}	1.168x10^{-10}	0.222	69.576	699.298	1947.117
10^{17}, WF 4.49 eV	3.739x10^{-5}	3.273x10^{-11}	0.262	70.952	623.193	545.582

Table 4.2: **Case B**

PTS doping value in cm^{-3}, gate work function	I_{dsat} in A	I_{off} in A	V_{th} in V	SS in $mV/decade$	I_{dsat} $\mu A/\mu m$	I_{off} $\mu A/\mu m$
2.5x10^{18} cm^{-3}, WF = 4.41 eV	4.355x10^{-5}	2.093x10^{-10}	0.193	64.379	725.827	3487.917
2.5x10^{18} cm^{-3}, WF = 4.45 eV	3.905x10^{-5}	5.001x10^{-11}	0.233	64.327	650.878	833.528
2.5x10^{18} cm^{-3}, WF = 4.49 eV	3.465x10^{-5}	1.198x10^{-11}	0.273	64.362	577.480	199.595
10^{18} cm^{-3}, WF = 4.41 eV	4.502x10^{-5}	2.735x10^{-10}	0.189	65.522	750.268	4558.633
10^{18} cm^{-3}, WF = 4.45 eV	4.045x10^{-5}	6.771x10^{-11}	0.229	65.715	674.122	1128.455
10^{18} cm^{-3}, WF = 4.49 eV	3.597x10^{-5}	1.693x10^{-11}	0.269	66.076	599.440	282.163
5x10^{17} cm^{-3}, WF = 4.41 eV	4.575x10^{-5}	3.341x10^{-10}	0.186	66.757	762.447	5568.633
5x10^{17} cm^{-3}, WF = 4.45 eV	4.115x10^{-5}	8.585x10^{-11}	0.226	67.255	685.772	1430.837
5x10^{17} cm^{-3}, WF = 4.49 eV	3.663x10^{-5}	2.245x10^{-11}	0.266	67.981	610.527	374.105

Table 4.3: **Case C**

PTS doping value in cm^{-3}, gate work function	I_{dsat} in A	I_{off} in A	V_{th} in V	SS in $mV/decade$	I_{dsat} $\mu A/\mu m$	I_{off} $\mu A/\mu m$
2.5x10^{18} cm^{-3}, WF = 4.41 eV	4.187x10^{-5}	1.533x10^{-10}	0.2	63.496	697.833	2555.667
2.5x10^{18} cm^{-3}, WF = 4.45 eV	3.741x10^{-5}	3.577x10^{-11}	0.24	63.353	623.542	596.228
2.5x10^{18} cm^{-3}, WF = 4.49 eV	3.306x10^{-5}	8.335x10^{-12}	0.28	63.264	551.013	138.911
10^{18} cm^{-3}, WF = 4.41 eV	4.425x10^{-5}	2.183x10^{-10}	0.192	64.47	737.445	3638.950
10^{18} cm^{-3}, WF = 4.45 eV	3.968x10^{-5}	5.235x10^{-11}	0.232	64.447	661.303	872.532
10^{18} cm^{-3}, WF = 4.49 eV	3.520x10^{-5}	1.259x10^{-11}	0.272	64.526	586.730	209.882
5x10^{17} cm^{-3}, WF = 4.41 eV	4.537x10^{-5}	2.820x10^{-10}	0.188	65.741	756.112	4700.767
5x10^{17} cm^{-3}, WF = 4.45 eV	4.076x10^{-5}	7.044x10^{-11}	0.228	66.03	679.260	1173.955
5x10^{17} cm^{-3}, WF = 4.49 eV	3.623x10^{-5}	1.984x10^{-11}	0.268	66.538	603.892	330.655

Table 4.4: **Case D**

PTS doping value in cm^{-3}, gate work function	I_{dsat} in A	I_{off} in A	V_{th} in V	SS in $mV/decade$	I_{dsat} $\mu A/\mu m$	I_{off} $\mu A/\mu m$
10^{20} cm^{-3}, WF = 4.41 eV	4.599x10^{-5}	3.587x10^{-10}	0.185	67.241	766.558	5978.600
10^{20} cm^{-3} , WF = 4.45 eV	4.138x10^{-5}	9.341x10^{-11}	0.225	67.846	689.705	1556.858
10^{20} cm^{-3}, WF = 4.49 eV	3.685x10^{-5}	2.481x10^{-11}	0.265	68.685	614.248	413.572
10^{19} cm^{-3}, WF = 4.41 eV	4.615x10^{-5}	3.811x10^{-10}	0.184	67.695	769.097	6351.617
10^{19} cm^{-3}, WF = 4.45 eV	4.153x10^{-5}	1.005x10^{-10}	0.224	68.402	692.152	1674.750
10^{19} cm^{-3}, WF = 4.49 eV	3.700x10^{-5}	2.711x10^{-11}	0.264	69.362	616.597	451.905
5x10^{18} cm^{-3}, WF = 4.41 eV	4.621x10^{-5}	3.908x10^{-10}	0.184	67.888	770.120	6512.867
5x10^{18} cm^{-3}, WF = 4.45 eV	4.159x10^{-5}	1.036x10^{-10}	0.224	68.635	693.137	1726.233
5x10^{18} cm^{-3}, WF = 4.49 eV	3.705x10^{-5}	2.814x10^{-11}	0.264	69.651	617.540	468.932

Best device in case A is PTS doping of 5x10^{17} cm^{-3}.

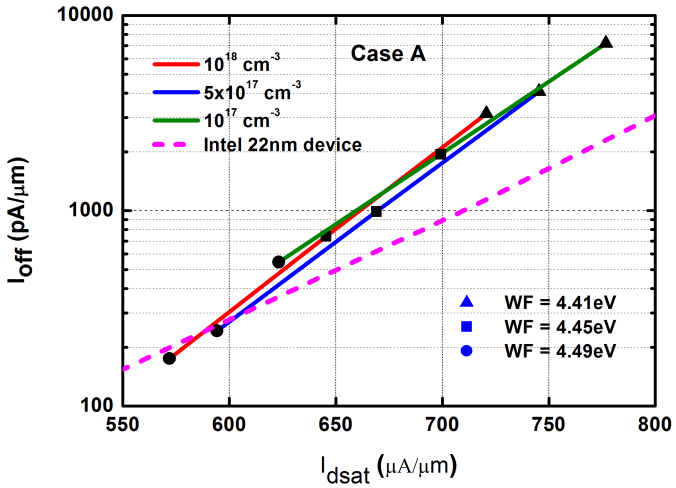

Figure 4.9: Case A : Plot showing increase in I_{dsat} for different threshold voltages

Best device in case B is PTS doping of 10^{18} cm^{-3}.

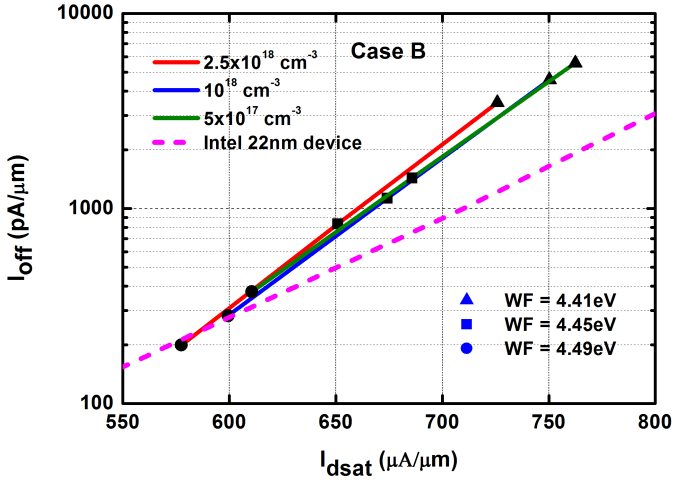

Figure 4.10: Case B : Plot showing increase in I_{dsat} for different threshold voltages

Best device in case C is PTS doping of 5x10^{17} cm^{-3}.

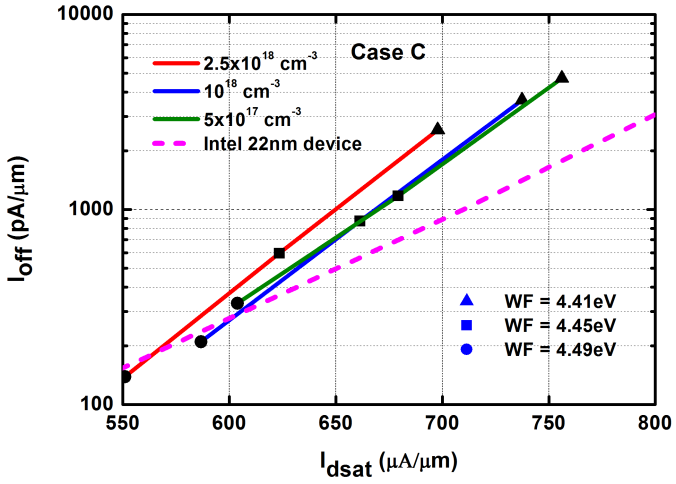

Figure 4.11: Case C : Plot showing increase in I_{dsat} for different threshold voltages

Best device in case D is PTS doping of 10^{20} cm^{-3}.

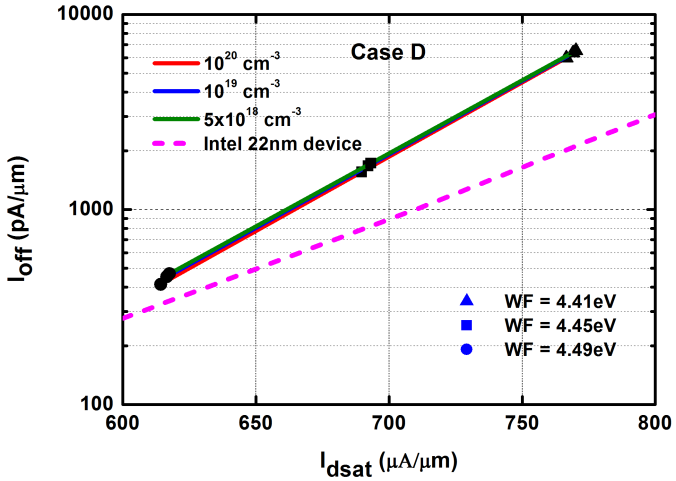

Figure 4.12: Case D : Plot showing increase in I_{dsat} for different threshold voltages

It shows that the increase in I_{dsat} is present across all V_{TH}. This means these punch through stoppers can be used for low power, standard power and high power logic transistors.

CHAPTER 5

Dynamic Threshold Voltage in FinFETs

DTMOS operation is studied for the best device from each case. As required for DTMOS operation, the gate is connected to the substrate through the isolation oxide as shown in Figure 5.1.

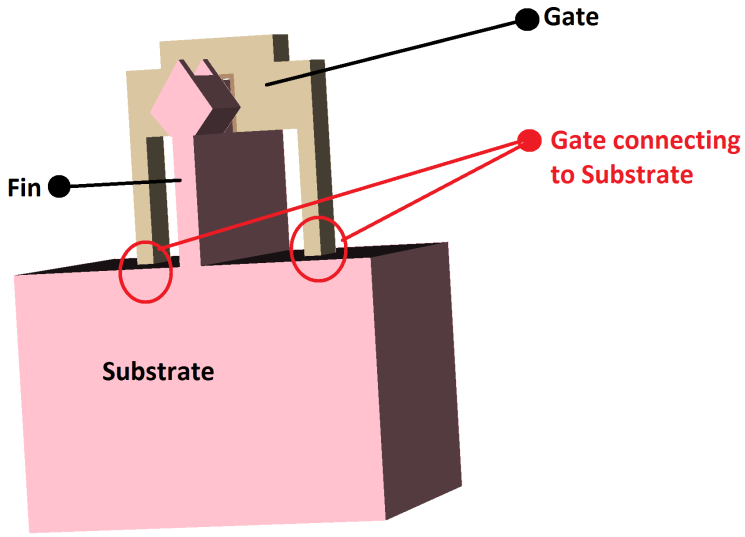

Figure 5.1: Gate making contact with the substrate

5.1 Proposed Novel structure

In bulk FinFET, DTMOS operation is not possible as gate is connected to common substrate for all FETs. In SOI FinFETs, making substrate contact is not possible as the fin is on oxide. Our device is like a Bulk FinFET sitting on a SOI. Compared to the Bulk FinFET which we studied till now, in normal operation our proposed device shows very less change in I_{dsat} and I_{off} (0.5 %). The reason for this change is unclear, but since the change is not significant it can be ignored. All PTS schemes perform in the same way in our proposed structure also.

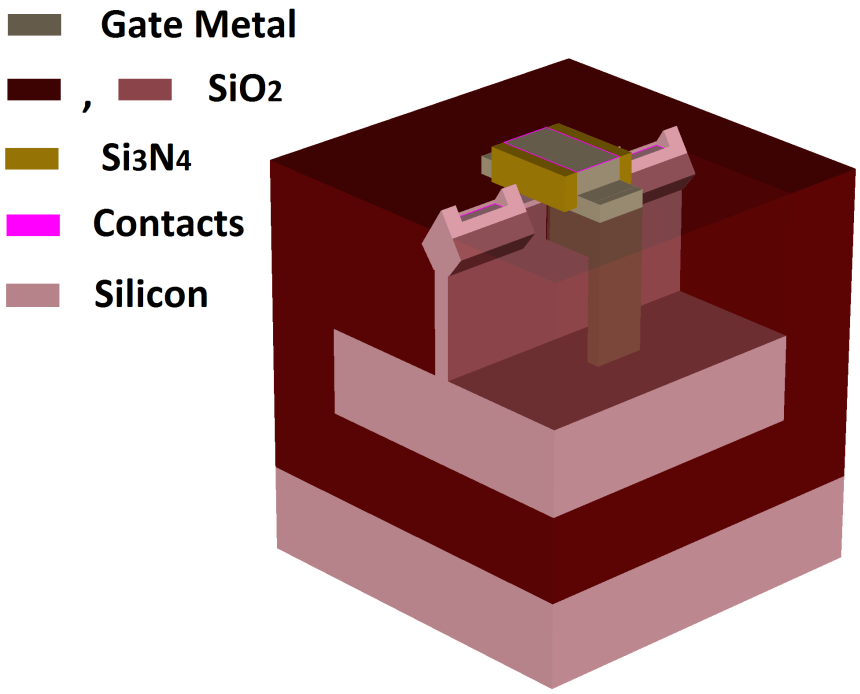

Figure 5.2: 3D view of our proposed device structure

SOI MOSFETs has problems of heat dissipation, buried oxide instabilities (Chaudhry and Kumar, 2004). Though our device needs an SOI substrate, our device is persumed to be devoid of the issues in SOI MOSFETs. As the conduction area is not near to insulator, hot carriers will not cause buried oxide instability. As there is a bulk, volume of atoms handling the heat is more, so our device will have much better heat dissipation capabilities.

5.2 Dynamic Threshold Voltage

DTMOS showed significant increase in the I_{dsat} for almost I_{off} in all the four best devices from each case.

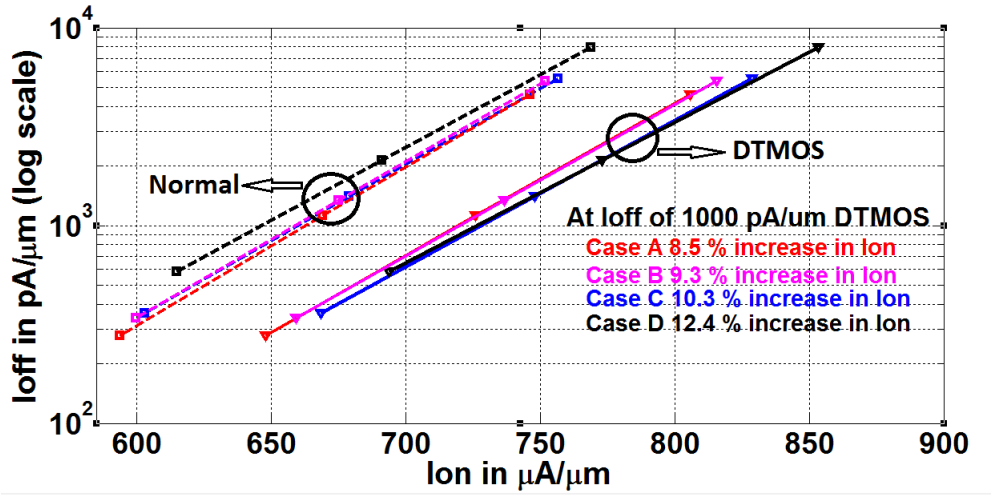

Figure 5.3: Presence of DTMOS in all the four cases

As an example in best device, from case C, $\boldsymbol{I_{dsat}}$ increased from 4.074e-5 A (679 $\boldsymbol{\mu}$A/$\boldsymbol{\mu}$m) in normal operation to 4.487e-5 A (748 $\boldsymbol{\mu}$A/$\boldsymbol{\mu}$m) in DTMOS mode. While $\boldsymbol{I_{off}}$ changed from 8.436x10^{-11} A to 8.437x10^{-11} A. Thus, there is 10.1 % increase in $\boldsymbol{I_{dsat}}$ for almost same $\boldsymbol{I_{off}}$. SS improved from 67.71 mV/decade to 65.32 mV/decade.

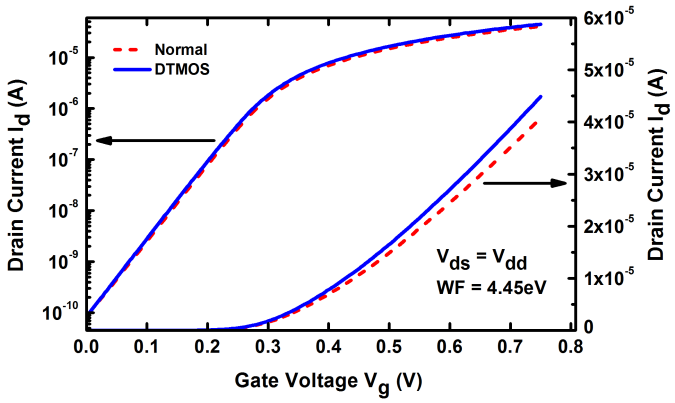

Figure 5.4: I_d Vs V_{gs} in best device from case C

From the log scale in Figure 5.4, it can be seen that there is almost no change in $\boldsymbol{I_{off}}$. While from the linear scale it is evident that the $\boldsymbol{I_{dsat}}$ has increased.

DTMOS in undoped FinFETs are due to increase in area of conduction. The substrate bias decreases the energy barrier near the gate controlled and non-gate controlled fin interface. This results in electron-current density extending into the non-gate controlled fin and hence $\boldsymbol{I_{dsat}}$ increases. Current conduction area has increased as seen from Figure 5.5.

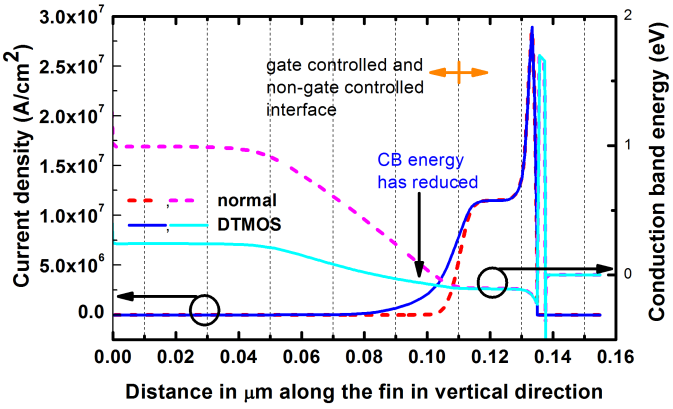

Figure 5.5: Electron-current density comparison in a cut line at middle of the fin, 10 nm from source showing increase in conduction area at V_{gs} = V_{dd} and V_{ds} = V_{dd}

Conventional body effect would have increased the current density in the gate controlled fin region. But here, there is no change in current density in gate controlled fin region. This is different from the conventional body effect. Also even at $\boldsymbol{V_{gs}}$ = $\boldsymbol{V_{dd}}$ and $\boldsymbol{V_{ds}}$ = $\boldsymbol{V_{dd}}$, the substrate current in DTMOS operation is four orders of magnitude lower than $\boldsymbol{I_{dsat}}$ which is accepatable.

5.2.1 PTS doping dependence for DTMOS operation

To study the DTMOS gain dependence on PTS doping, case C was considered. The Figure 5.6 shows the comparison between normal and DTMOS operation in PTS with doping values of 2.5x10^{18} cm^{-3} cm^{-3}, 10^{18} cm^{-3} cm^{-3}, 5x10^{17} cm^{-3} and 10^{17} cm^{-3}. In DTMOS operation, PTS with higher doping values show lower increase in $\boldsymbol{I_{dsat}}$, PTS with lower doping values show higher increase in $\boldsymbol{I_{dsat}}$. 2.5x10^{18} cm^{-3} cm^{-3} shows 5.5% increase: 10^{18} cm^{-3} cm^{-3} shows 8% increase: 5x10^{17} cm^{-3} shows 10.1% increase: 10^{17} cm^{-3} shows 12.7% increase. In DTMOS operation, at $\boldsymbol{I_{off}}$ of 1000 pA/ $\boldsymbol{\mu}$ m, PTS with doping of 5x10^{17} cm^{-3} gives the higher $\boldsymbol{I_{dsat}}$.

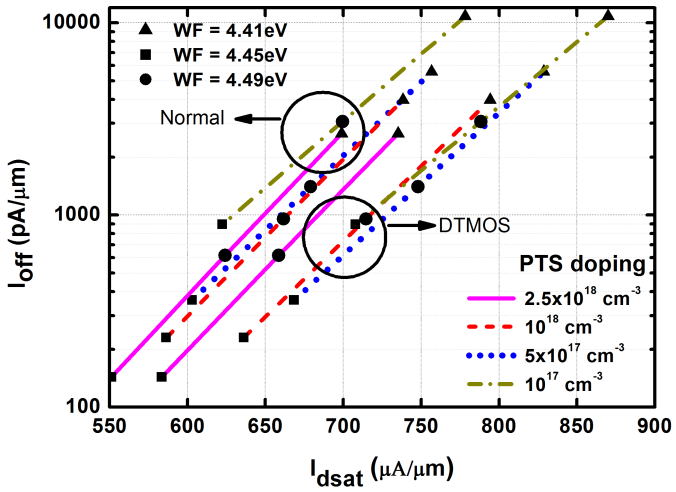

Figure 5.6: Comparison between DTMOS and normal operation for different threshold voltages

PTS with higher doping values have higher conduction band energy and thus higher energy barrier near the gate controlled to non-gate controlled fin interface. The region in which the energy barrier is sufficiently lowered due to substrate bias for electron injection from source is lesser. Therefore, increase in current conduction area due to substrate bias is lesser. For PTS with lower doping values, region in which energy barrier is sufficiently lowered by the substrate bias is larger. So increase in conduction area is more. Figure 5.7 shows the trend in variation in DTMOS gain in on-current with PTS doping value.

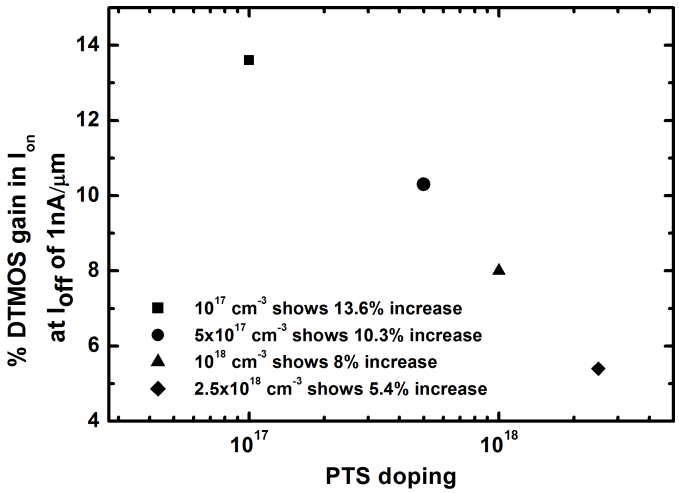

Figure 5.7: DTMOS gain in on-current for different PTS doping values

CHAPTER 6

Conclusion

6.1 Conclusion

The DTMOS operation in lightly doped FinFETs is due to modulation of cross-sectional area of current flow with change in gate bias. It is demonstrated through simulations that DTMOS has higher I_{dsat}/I_{off} ratio and lower subthreshold slope compared to a conventional FinFET. To enable DTMOS operation a novel device structure is proposed. The proposed device structure is similar to a bulk FinFET, but on a SOI substrate, which is required for isolation between devices. Hence, to realize these devices, only minor changes are necessary in the process flow for bulk FinFETs.

6.2 Scope for future work

- To evaluate DTMOS on a triangular fin. DTMOS effect could be more on a triangular fin as the base of the gate controlled fin is broader.
- DTMOS gain dependence on fin width and fin height could be evaluated.
- Coming up with a process sequence for the simulated device.
- PTS schemes could be evaluated for different fin width and fin height.
- In this work, the device performances are evaluated using simulator, instead device should be fabricated and then evaluation of different PTS schemes, DTMOS operation should be done.

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