Analog Front End Design of Bluetooth Transmitter

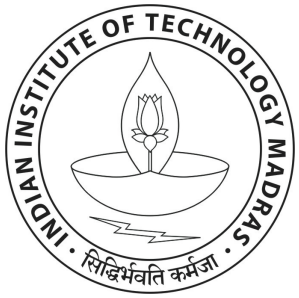
A THESIS

submitted by

KATTA UMAMAHESWARA REDDY

for the award of the degree of

MASTER OF TECHNOLOGY



DEPARTMENT OF ELECTRICAL ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY, MADRAS.

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THESIS CERTIFICATE

This is to certify that the thesis titled **Analog Front End Design of Bluetooth Transmitter**, submitted by **Katta Umamaheswara Reddy**, to the Indian Institute of Technology, Madras, for the award of the degree of **Master of Technology**, is a bona fide record of the work done by him under our supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

Dr. S. Aniruddhan

Advisor,

Assistant Professor,

Dept. of Electrical Engineering,

IIT-Madras, 600 036

Place: Chennai

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This thesis is dedicated to my parents, my brother and to all my loved ones.

ABSTRACT

A direct conversion transmitter complying with the IEEE 802.15.1 (Bluetooth) standard is designed. The radio frequency (RF) analog front-end blocks of the transmitter are power amplifier (PA), quadrature upconversion mixer and base-band filter. The main idea of this work is to reduce the power consumption and the area of chip. By choosing the passive mixer as upconverter the power is majorly dissipated in power amplifier only. The number of inductors in the design is minimized to reduce the area of chip. The transmitter is designed and verified through simulations, in UMC 65 nm CMOS process, and found to satisfy the system requirements with sufficient margin.

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ABBREVIATIONS

ACPR	Adjacent Channel Power Ratio
AM	Amplitude Modulation
APC	AM/PM conversion
BPF	Band Pass Filter
BR	Basic Rate
CMFB	Common Mode FeedBack
DAC	Digital to Analog Converter
dB	decibel
DAC	Digital to Analog Converter
DC	Direct Current
DPSK	Differential Phase-Shift Keying
DQPSK	Metal-Oxide-Semiconductor Field Effect Transistor
EDR	Enhanced Data Rate
IEEE	Institute of Electrical and Electronics Engineers
IF	Intermediate Frequency
ISM	Industrial, Scientific and Medical
LO	Local Oscillator
LTI	Linear Time-Invariant
MFB	Multiple FeedBack
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
P1dB	Power at 1 dB compression
PA	Power Amplifier

PAE	Power Added Efficiency
PAPR	Peak-to-Average Power Ratio
PAR	Peak-to-Average Ratio
PM	Phase Modulation
RF	Radio Frequency
TDD	Time-Division Duplexing
UGB	Unity Gain Bandwidth
UMC	United Microelectronics Corporation
VCO	Voltage-Controlled Oscillator

CHAPTER 1

Introduction

1.1 Bluetooth

The Bluetooth is a short-range wireless connection between different electronic devices without using any cords, cables, adapters. The distance among the communicating devices is small in comparison to other modes of wireless communication. Bluetooth operates in the 2.4-2.48 GHz band which is the globally unlicensed but regulated Industrial, Scientific and Medical (ISM) band. The radio technology used in Bluetooth is frequency-hopping spread spectrum. The transmitted data are divided into packets and each packet is transmitted on any one of the designated Bluetooth channels. The transceiver architecture is based on time-division duplexing (TDD) scheme, which in turn effects some design specifications of transmitter. In TDD systems, transmitter and receiver do not operate at same time.

1.2 Modulation schemes of Bluetooth

Initially Gaussian frequency shift keying (GFSK) modulation was the only modulation scheme available. GFSK is a constant envelope modulation where information is sent only in phase. Devices functioning with GFSK are said to be operating in basic rate (BR) mode with an instantaneous data rate of 1 Mbit/s. Since the introduction of Bluetooth 2.0, $\pi/4$-DQPSK and 8DPSK with a data rate of 2 and 3 Mbit/s respectively are also used. These two are variable envelope modulations where information is sent in both amplitude and phase. These Bluetooth

Class	Max. permitted power	Typ. range(m)
1	100 mW (20 dBm)	~ 100
2	**2.5 mW (4 dBm)**	$\sim$ **10**
3	1 mW (0 dBm)	~ 1

Table 1.1: Different classes of Bluetooth

devices use spectrum efficiently by transmitting more data in the available frequency band. So these Bluetooth versions are said to be operating in Enhanced Data Rate (EDR). The combination of BR and EDR modes in Bluetooth radio technology is classified as a BR/EDR radio. With channel bandwidth of 1 MHz, Bluetooth has 79 designated channels in the 2.4-2.48 GHz band. The latest Bluetooth v4.0 allows for 40 channels with 2 MHz channel spacing. In the present design, Transmitter is implemented for Bluetooth 4.0.

1.3 Types of Bluetooth devices

There are three different types of bluetooth devices available based on the distance between the two communicating ends. The classification is shown in Table 1.1. In this work, transmitter is designed for class 2 Bluetooth. The maximum and minimum permitted powers of class 2 Bluetooth are 4 dBm and -6 dBm respectively.

1.4 Design Objective

The main objective of this work is to design an analog front end transmitter for Bluetooth with low power and minimum area.

1.5 Thesis organization

The rest of the thesis is organized as described below.

Chapter 2 discusses the architectural considerations of RF transmitter

Chapter 3 discusses the design of Power amplifier and the principle behind the choice of power amplifier in detail

Chapter 4 deals with the design of the voltage mode passive mixer with 25% duty cycle LO signal and LO generator circuit

Chapter 5 deals with the baseband filter and opamp used for implementation of filter

Chapter 6 summarizes the integration of different blocks in the transmitter and final results of entire chain

CHAPTER 2

Transmitter Architecture

2.1 Types of transmitter architectures

An RF transmitter performs upconversion and power amplification. A good understanding of modulation schemes is necessary for transmitter design because of their influence on the choice of architecture and such building blocks as upconversion mixers and power amplifiers (PAs) [1]. There are two types of modulation formats available. They are constant-envelope (nonlinear) and variable envelope-modulation (linear) formats. Any modulation signal x(t) can be represented in two ways. They are

Polar form

$$x(t) = a(t)\cos\left(\omega_{LO}t + \phi(t)\right) \tag{2.1}$$

Cartesian form

$$x(t) = x_I(t)\cos\omega_{LO}t + x_Q(t)\sin\omega_{LO}t \tag{2.2}$$

A third representation called complex envelope representation is also there, but the above two are sufficient in the present context.

Constant envelope modulation schemes have constant amplitude and it does not vary with time. Information will be carried in only the zero-crossing points. Phase and frequency modulations are constant envelope modulations. A phase locked loop can be used as upconverter in this case and the RF signal can be processed

by a nonlinear power amplifier. This type of transmitter architecture is called as polar architecture. The very first Bluetooth versions have GFSK as the only modulation scheme. As earlier mentioned these Bluetooth devices are said to be operating in basic rate. So there were some published implementations reporting polar architecture for basic rate Bluetooth transmitter.

Variable envelope modulation schemes have information in amplitude also. Their amplitude varies with time. Modulation schemes such as QPSK have information in both amplitude and phase. This is done in order to utilize the spectrum efficiently. In such cases polar architecture will not do the required job as it is not possible to track the amplitude variations with polar architecture. Cartesian architecture on the other hand can track both amplitude and phase variations. In Cartesian architecture, two signals (in phase and quadrature phase) coming from DAC are to be followed by two separate mixers with LO signals in quadrature phase. Here mixer will be used as upconverter. The two upconverted RF signals from mixers are added to get the required modulated signal. In general DAC is implemented in fully differential structure, so four output lines will be sent into analog front end. Cartesian architecture can handle both constant envelope and variable envelope modulation signals. But for constant envelope modulation schemes, polar architecture is generally better.

2.2 Homodyne and Heterodyne architectures

Based on the number of steps of upconversion, two types of transmitter architecture are possible. They are homodyne and heterodyne architectures. Homodyne architecture is also called as direct conversion architecture. In homodyne architecture, upconversion will be happened in single step. It is simple and high levels of integration will be achieved with this architecture. But there is a serious problem with this homodyne architecture. The power amplifier and LO generator will be

operating at the same frequency. The modulated spectrum output of mixer will corrupt the pure sinusoid that is coming from LO generator (VCO) and it will give very noisy LO. This effect is called as PA pulling. It will happen either through electro-magnetic coupling if they are close enough or through supply if they share same supply or through substrate if they are same chip. It is like a parasitic feedback. The phenomenon of pulling the VCO is called injection locking. If PA output is just a single tone, then its not a serious problem. But as PA output will never be a single tone, the VCO will produce sidebands also.

This problem can be eliminated by performing upconversion in two steps. The mixers in the two steps will be operating with different LO frequency than that of power amplifier. So PA pulling problem will not arise here. This type of architecture is called as heterodyne architecture. The second mixer in this architecture will produce two sidebands here. One sideband has to be eliminated as the information in it is redundant. But to eliminate this frequency, the band pass filter needed should have high quality factor. But it is very difficult to implement a BPF with high Q value at GHzs of frequency. So this type architecture will not result in high levels of integration like in the case of homodyne architecture.

2.3 Direct conversion architecture

The major problem of the direct conversion architecture is PA pulling. The LO generator which is operating at the same frequency that of PA is the main reason for this problem. If it is managed to design VCO at the different frequency that of PA, then this problem will not arise at all. This can be done by designing VCO at double the frequency that of PA, followed divide by two circuit. Nowadays divide by two circuits that are giving in phase and quadrature phase, are widely used in the transceiver architectures. As the PA pulling problem is solved by this technique, direct conversion architecture is widely used in RF transmitters. So

this architecture is implemented here. The block diagram of transmitter chain is shown in Fig. 2.1.

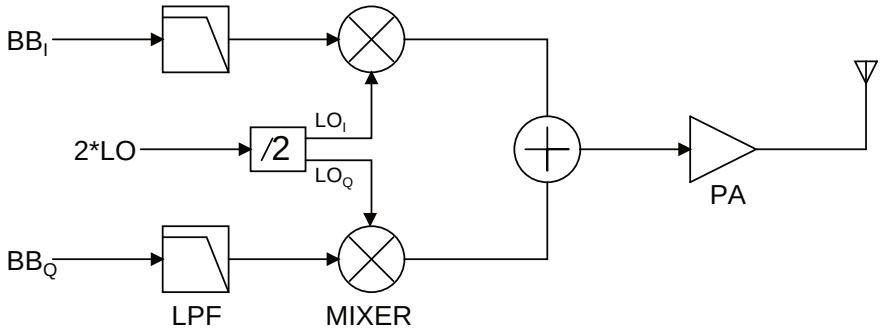

Figure 2.1: Direct-conversion architecture

Entire transmitter is implemented fully differential in order to make the design insensitive to package model parasitics.

CHAPTER 3

Power Amplifier

3.1 Choice of power amplifier

Broadly power amplifier can be categorized into two major types. They are linear and nonlinear (switching) power amplifier. Linear power amplifiers are used for handling variable envelope modulation formats with sacrifice of efficiency. Nonlinear power amplifiers are used for handling constant envelope modulation formats with high efficiency. Efficiency (drain efficiency) is one of the important metrics of power amplifier. It is the ratio of PA output power to its DC power dissipation. Nonlinear power amplifiers cannot be used for variable envelope modulation schemes as their output is saturated. To track the incoming amplitude variations, the power amplifier output amplitude should vary in accordance with the input. So the use of linear power amplifier is inevitable in the case of variable envelope modulation schemes even though it results in poor efficiency. Here linear power amplifier is used because $\pi/4$-DQPSK and 8DPSK are variable envelope modulation schemes. In any RF power amplifier, inductor is used as load to facilitate the output to swing above the supply. This will help in getting more output power for the given power supply.

In linear power amplifiers, there are sub categories based on the conduction angle. They are class A, B, AB and C power amplifiers. The class A conducts for full cycle (360°), class B conducts for half cycle (180°), class AB conducts for more than half cycle, class C conducts for less than half cycle. Obviously class A power amplifier is superior in terms of linearity. As linearity is important concern in the case of variable envelope modulation, class A topology is implemented here.

3.2 Class A power amplifier

Power amplifier schematic is shown in the Figure 3.1.

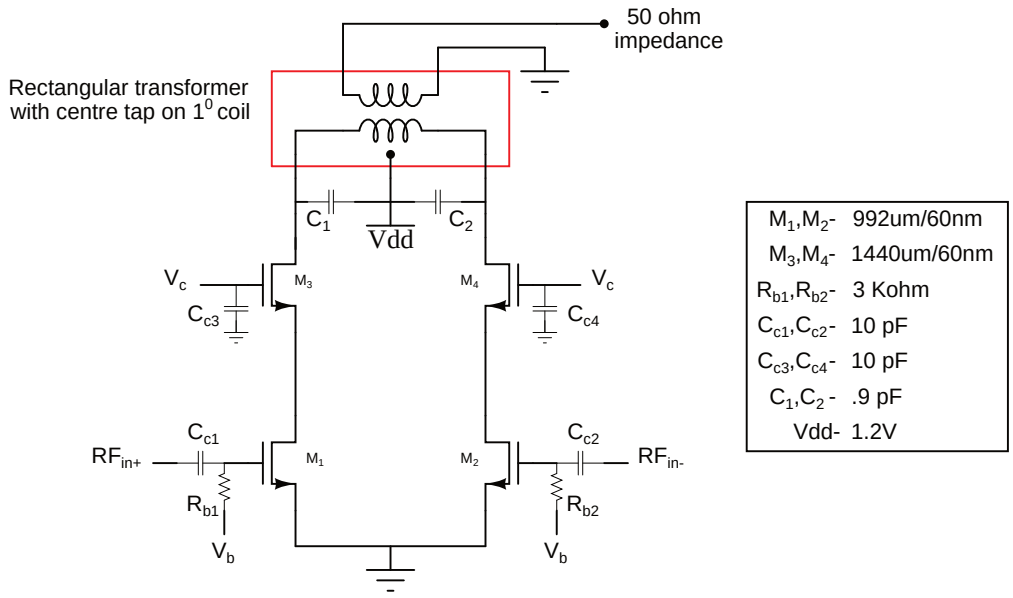

Figure 3.1: Power Amplifier

The cascode scheme assures the stability of the PA and isolates the PA output from the mixers. The MOS transistors used are 1.2V transistors. If cascode is not used then the transistor will go into breakdown. In cascode structure, swings of output will be shared by the two transistors so that none of them will go in to breakdown. Both common source and common gate transistors are thin oxide transistors only. The antenna is single ended so balun is needed to perform the differential to single ended conversion. A scalable rectangular transformer with input center tap from umc 65 nm is used as balun here. The transformer converts the 50 ohm antenna impedance to 35 ohm at the output of each half of power amplifier. Capacitors are connected across the transformer to tune out the parasitics at the differential output nodes.

PAR or PAPR is the important factor of modulation schemes in the context of power amplifier. It is defined as follows.

$$PAPR = \frac{|\ x\ |_{peak}{}^2}{x_{rms}{}^2} \tag{3.1}$$

As the power amplifier is class A, some minimum amount of DC current should be there in power amplifier to ensure 360° conduction angle. The class A is inferior among all the power amplifiers in terms efficiency. If PAR is high, then efficiency would be even worse. Among all the three modulation schemes, 8DPSK has high PAR of 6.3 dB. So this value decides the DC current in the power amplifier.

For a linear power amplifier, the output power should linearly vary in accordance with the input power. Gain should be same for all levels of input powers. But the output voltage levels will be limited by power supply and inherent nonlinearity of the device. Because of these reasons, gain compression will happen at higher output power levels. Gain compression can be seen in Figure 3.2

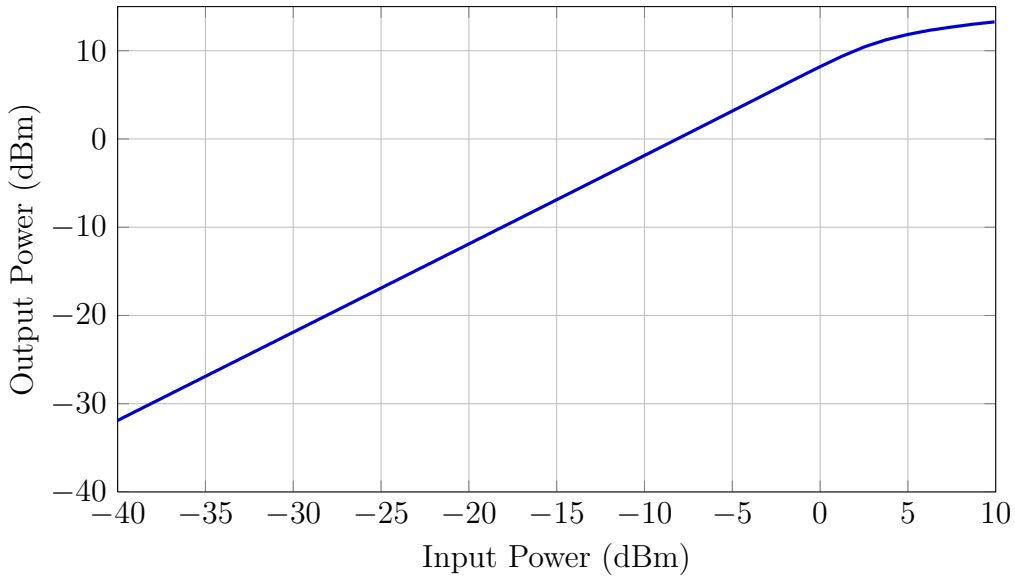

Figure 3.2: Output Power versus Input Power

3.3 Efficiency

efficiency (η) can be calculated as follows,

$$\begin{aligned}\eta &= \frac{Output\ Signal\ Power(P_{sig})}{DC\ Power(P_{dc})} \\ &= \frac{2.5\ mW}{1.2\ V \times 22\ mA} \\ &= 9.47\%\end{aligned}$$

Fig.3.3 shows the drain efficiency of power amplifier.

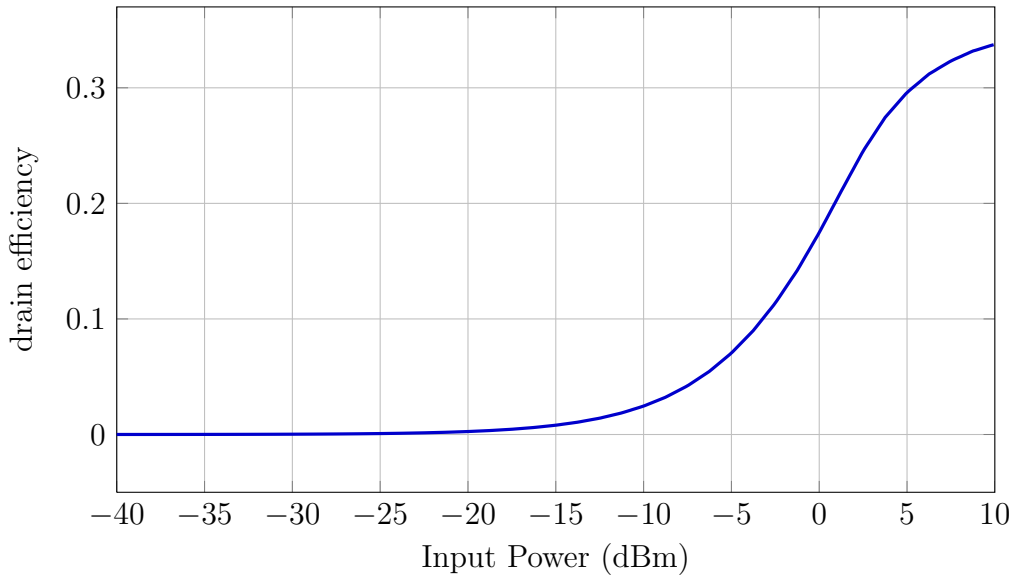

Figure 3.3: drain efficiency

Power added efficiency(PAE) is another metric for rating the efficiency of a power amplifier. It takes the effect of the gain of the power amplifier. It is calculated as follows

$$\begin{aligned}PAE &= \frac{P_{sig} - P_{in}}{P_{dc}} \\ &= \eta\left(1 - \frac{1}{gain}\right)\end{aligned}$$

where P_{in} is the input power. As the gain of power amplifier is not high, the PAE is not same as drain efficiency. It is shown in the Fig. 3.4

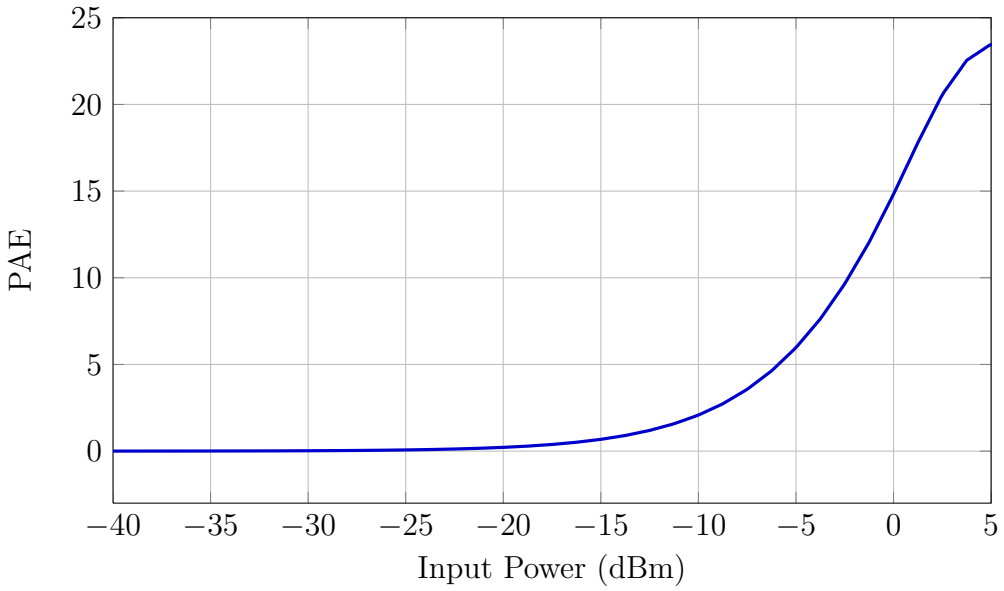

Figure 3.4: Power Added Efficiency

3.4 Linearity

Linearity is very important concern in RF transmitters and it is mainly limited by power amplifier. To model all the nonlinearities of PA, three different parameters are used here. They are output referred P1dB, AM/PM conversion and ACPR. The P1dB point refers to the gain compression by 1 dB. The P1dB point will set a limit to the region of power amplifier operation where the power levels above this point are prohibited to operate. The input power corresponding to the output referred P1dB is input referred P1dB. The output referred P1dB will be decided by both maximum output power of transmitter chain and PAR of modulation scheme.

$$\begin{aligned} Required\ Output\ referred\ P1dB &= Maximum\ P_{out} + PAPR \\ &= 4\ dBm + 6.3\ dB \\ &= 10.3\ dBm \end{aligned}$$

Fig.3.5 shows the P1dB plot of power amplifier.

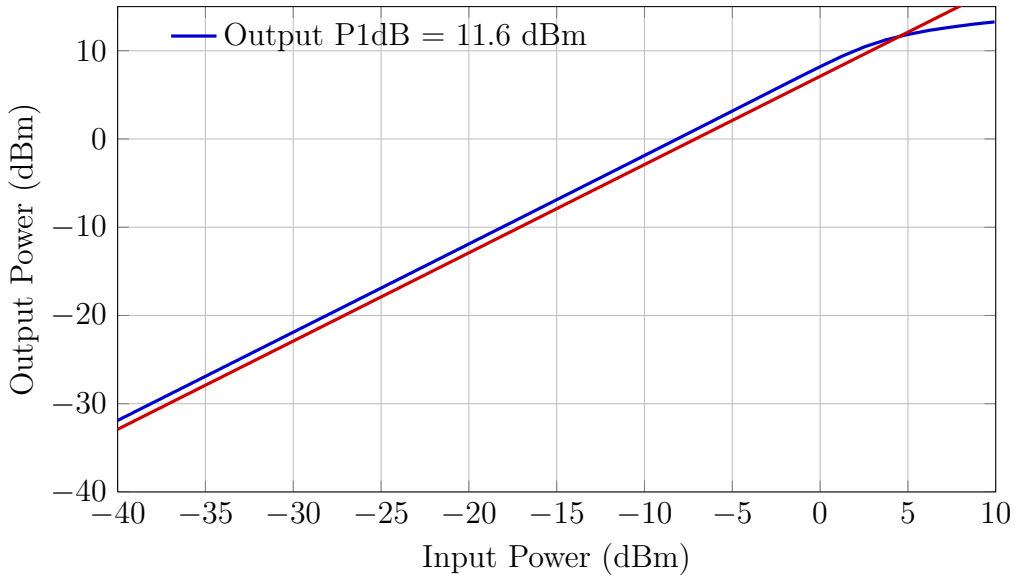

Figure 3.5: 1 dB compression point

AM/PM conversion is one more metric to quantify the nonlinearity of RF circuits. In power amplifiers, amplitude modulation may be converted to phase modulation, thus producing undesirable effects. Because of AM/PM conversion, output has amplitude-dependent phase shift. This does not occur in LTI system. It arises if a system is both dynamic and nonlinear. So AM/PM conversion has to be considerably less for good performance. AM/PM conversion of power amplifier is given in the Fig. 3.6

ACPR is very important parameter to quantify the nonlinearity of PA. The transmitter should produce a band limited output with sidebands at considerably low level. It is the ratio of in band power to side band power. ACPR requirement is specified for any transmitter though spectrum mask definition. As power amplifier is the more nonlinear block in the transmitter chain, the ACPR of PA alone should be verified. The ACPR of PA alone is shown in Fig .3.7

The ACPR of Bluetooth transmitter has to be more than 26 dBc. The ACPR of PA alone is at reasonable value to meet the 26 dBc requirement.

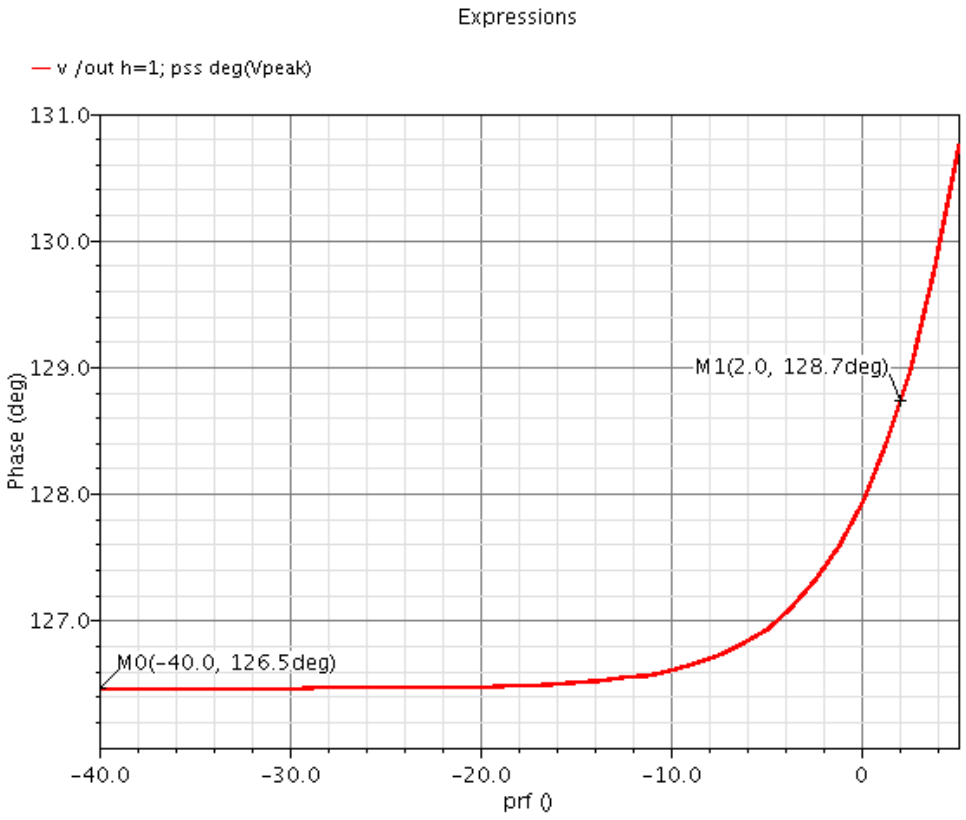

Figure 3.6: AM/PM conversion

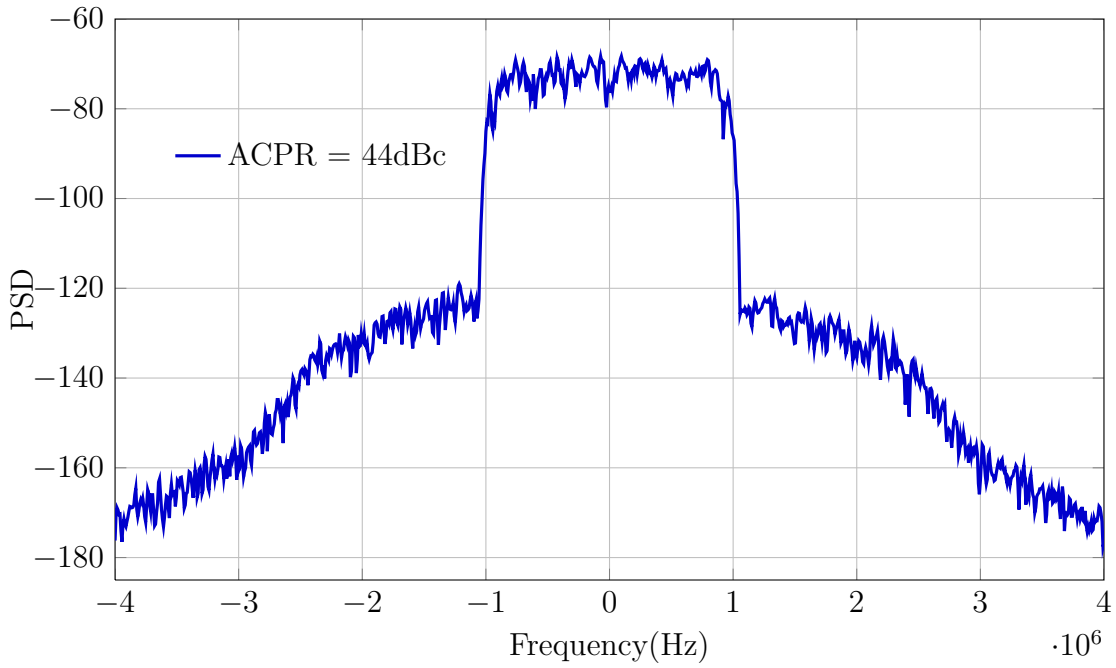

Figure 3.7: ACPR of power amplifier

CHAPTER 4

Mixer

4.1 Choice of mixer

Baseband information is shifted to RF band by mixer. Mixer performs frequency translation by multiplying two waveforms. They can be broadly categorized into passive and active topologies. Active mixers consume DC power whereas passive mixers do not consume. Passive mixer is implemented here to reduce the power consumption of transmitter chain. It is superior in terms of noise and linearity also. The mixer drives the power amplifier input which is nothing but capacitance [2]. So the mixer implemented hare is called as a sampling mixer because such arrangement operates as a sample-and-hold circuit.

4.2 Upconversion passive mixer

In passive mixer, the MOS transistor operates in either triode or cutoff region. It does not operate in saturation region. Mixer is a three terminal device. They suffer from unwanted coupling (feedthrough) from one port to another because of device capacitances. The gate-source and gate-drain capacitances create feedthrough from the LO port to the RF and IF ports. The LO-RF feedthrough produces LO signal at the mixer output which is considerably large. Similarly all other feedthroughs are undesirable. To eliminate feedthroughs caused by capacitances, double balanced structure is implemented.

In double balanced passive mixer, the base band and LO signals (ω_{IF} and ω_{LO}) are applied as inputs. The two upconverted signals ($\omega_{LO} \pm \omega_{IF}$) are produced

at the output of mixer. One band has to be eliminated as both contain the same information. It is possible to get single sideband output with cartesian architecture. Double balanced IQ passive mixer is shown in Fig. 4.1. It has two double balanced mixers for I and Q channel. The outputs of the mixers are added directly because of the 25% duty cycle of LO waveform. With 50% duty cycle LO, it is not possible to add the two outputs directly. Because I and Q channel will be ON for some part of time. But With 25% LO duty cycle, I-channel and Q-channel MOS switches do not ON at same instant. This is the great advantage of using 25% duty cycle for LO. It makes the circuit so simple. A baseband active RC filter is going to drive the mixer. Mixer operates in voltage mode because of the low output impedance of filter.

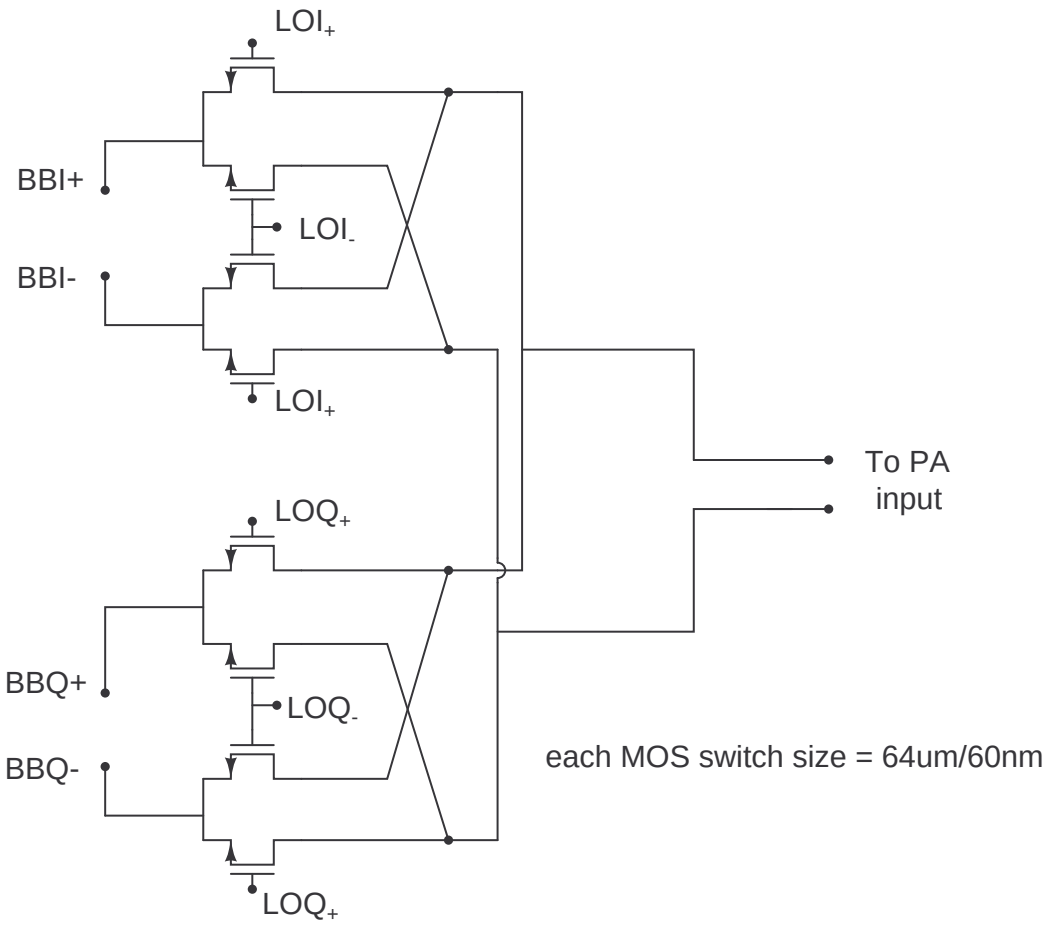

Figure 4.1: Double-balanced upconversion passive mixer

Power amplifier input capacitance, mixer switch ON resistance and filter output

impedance are the deciding parameters of MOS switch size. Because they form a RC network and the its bandwidth has to be more than LO frequency. The transistors will be switching at the speed of LO frequency. The capacitor at mixer output has to be charged with in this period. This will set constraint on the values of filter output impedance and mixer switch ON resistance for a certain power amplifier input capacitance. Moreover the the output stage of filer opamp should have enough dc current to drive the capacitor load.

4.3 Mixer gain

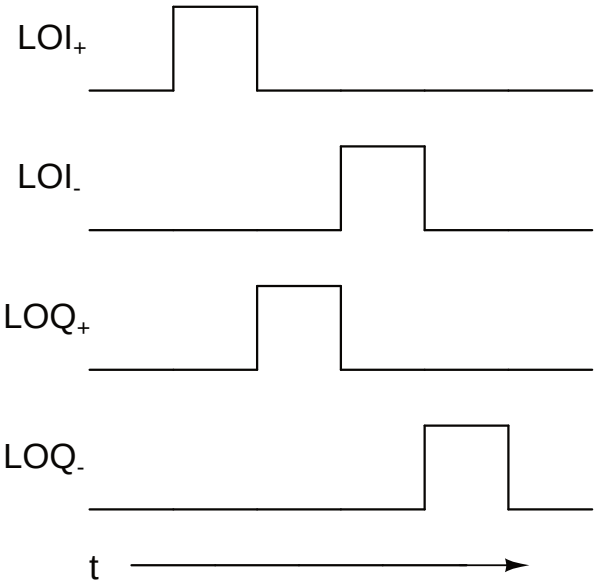

Figure 4.2: Quadrature LO waveforms

The Fourier series expansion of a 25% duty-cycle LO waveform shown in Fig. **??**, with frequency ω_{LO} is given by,

$$x_{LO}(t) = \frac{2\sqrt{2}}{\pi}\left\{\sin\omega_{LO}t - \frac{1}{3}\sin 3\omega_{LO}t - \frac{1}{5}\sin 5\omega_{LO}t + \frac{1}{7}\sin 7\omega_{LO}t + \ldots\right\} \quad (4.1)$$

Ideally the gain of IQ mixer should be -0.9 dB. But due to finite switch ON

resistance (9.5 Ω), the gain is found to be -3.9 dB. But it is tolerable because of the low output power of Bluetooth transmitter.

At power amplifier output P1dB required is 10.3 dB. The gain of PA is 8 dB. So at the mixer output, gain compression should not happen till 2.3 dBm (10.3-8). From the Fig. 4.3, it is clear that there is no gain compression till the output power of 2.3 dBm. So the passive mixer is very good in terms of linearity. The nonlinearity at the transmitter output is mainly caused by the power amplifier.

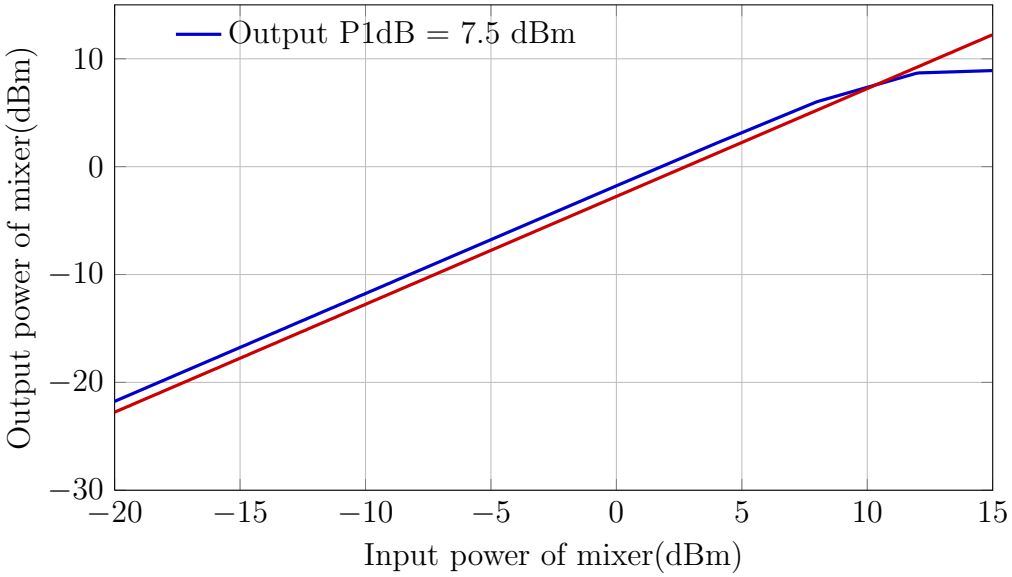

Figure 4.3: Compression curves of mixer

4.4 Frequency divider with 25% duty cycle outputs

The frequency divider employs two D-latches in a master-slave configuration with negative feedback. The two identical D-latches are driven by complementary clocks. The basic principle of divider circuit is shown in Fig. 4.4. It looks like a counter operating at GHzs of frequency. As there are two latches, there can be four possible outputs.

The circuit implementation for the frequency divider was proposed by Razavi [3].

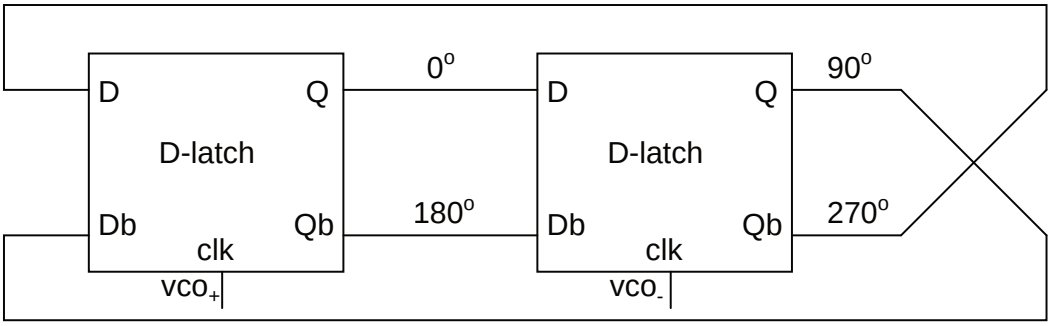

Figure 4.4: Basic principle of frequency divider

Its circuit diagram is shown in Fig. 4.5. Each latch consists of two sense devices (M_{s1} and M_{s2} in the master and M_{s3} and M_{s4} in the slave), a regenerative loop (M_{c1} and M_{c2} in the master and M_{c3} and M_{c4} in the slave), and two pull-up devices (M_{p1} and M_{p2} in the master and M_{p3} and M_{p4} in the slave). A 4.8 GHz square signal drives the four PMOS transistors. When CLK is high, M_{p1} and M_{p2} are OFF and the master is in the sense mode, while M_{p3} and M_{p4} are ON and the slave is in the store mode. When CLK goes low, the reverse occurs. Out of four, two PMOS transistors turn ON at a time. They try to pull their drain terminals to Vdd. But a cross coupled NMOS in the same latch, tries to pull only one of them to Vdd and other to ground. The Vdd output is decided by the sense MOS transistors. Thus the circuit inherently generates a four-phase clock with 25%-duty-cycle signal. The waveforms of divider is shown in Fig. 4.6.

There is a small ripple in the zero state for divider output waveforms. To remove that ripple, four buffers are added next to the divider. The entire block diagram of LO generator circuit is given in Fig. 4.7. The buffer is a two-stage inverter to enhance the drive capability. VCO produces differential 4.8 GHz sinusoidal signals. Two buffers follow the VCO and convert sinusoids into rail-rail square waves. The output waveforms of the complete LO generator is shown in Fig. 4.8.

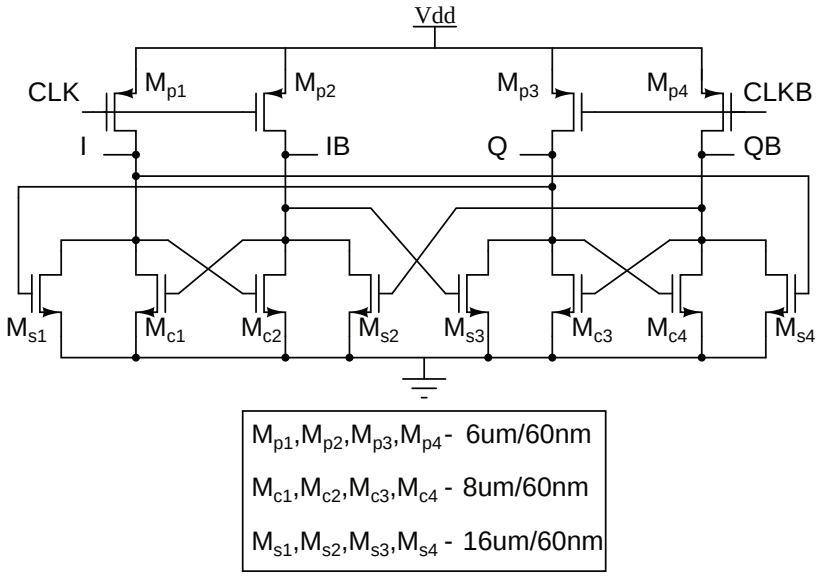

Figure 4.5: 25%-duty-cycle LO generator

They are quadrature in phase with no ripple in the zero state.

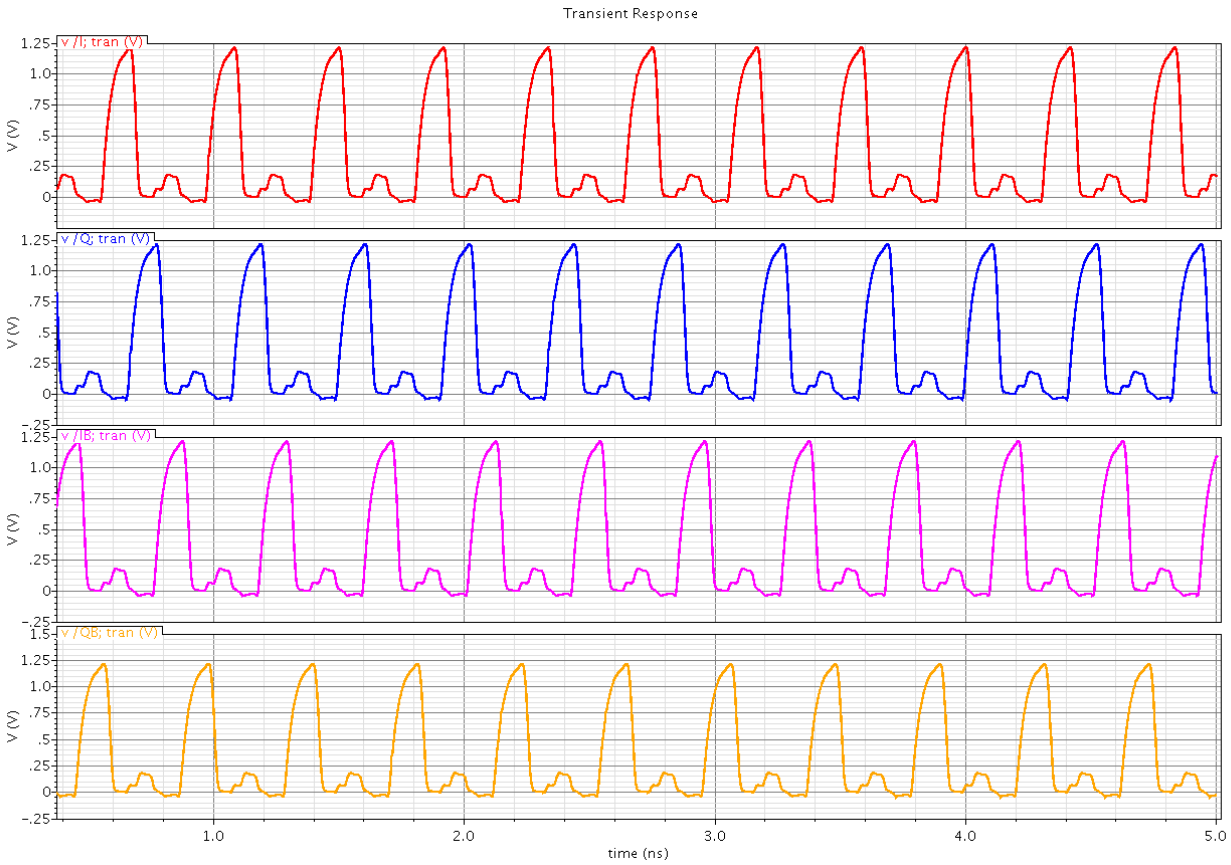

Figure 4.6: Output waveforms of frequency divider

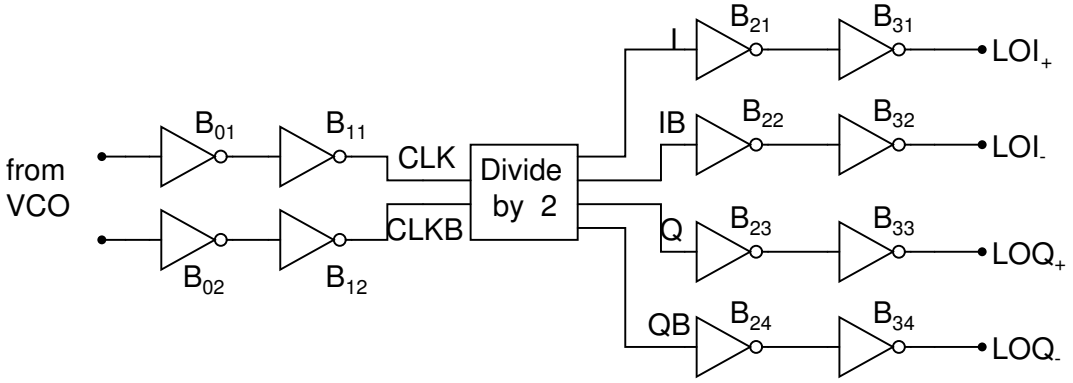

Figure 4.7: Complete LO generator

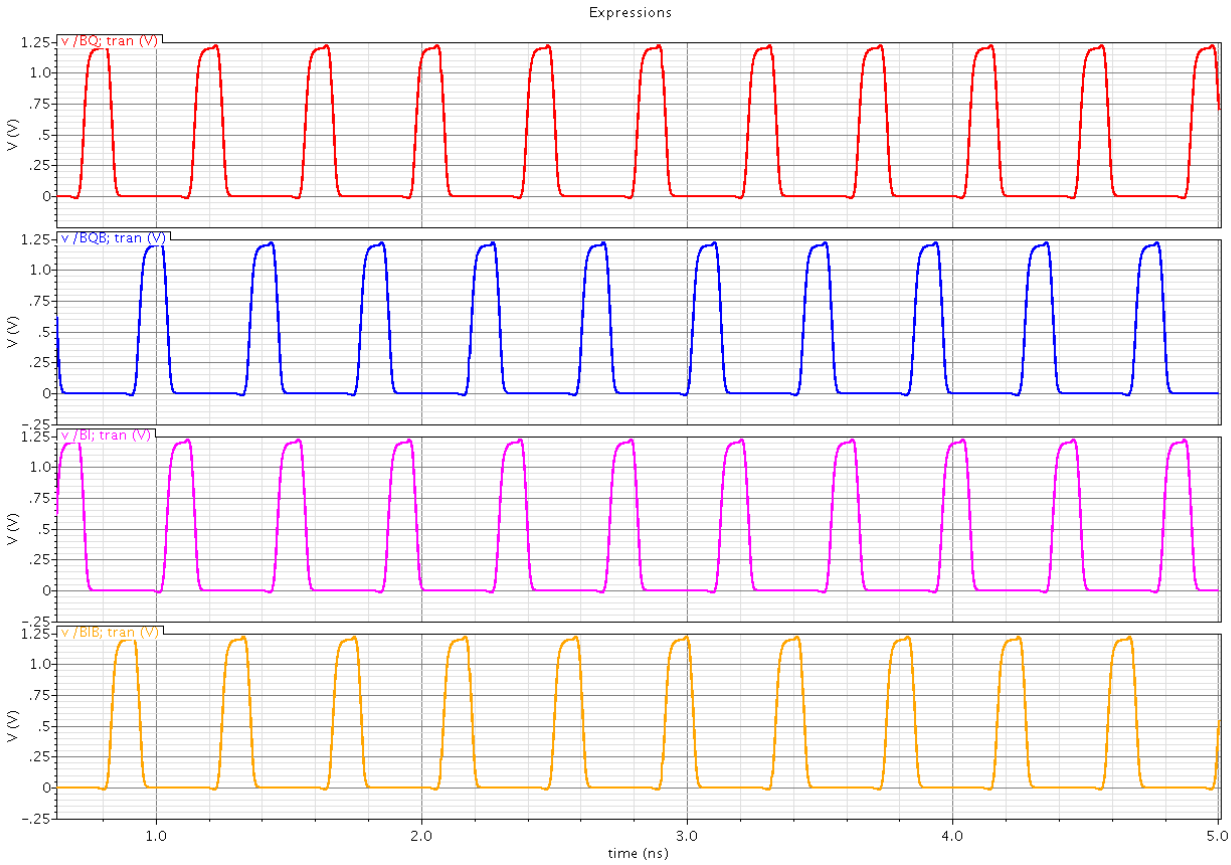

Figure 4.8: Output waveforms of complete LO generator

CHAPTER 5

Baseband filter

5.1 Role of baseband filter

A DAC drives the transmitter analog front end. It converts digital baseband information to analog form. But it produces images also at the multiples of conversion frequency. They are undesired and have to be attenuated. The role of the filter is to suppress all these DAC images. Filter has to provide required attenuation at conversion frequency without attenuating any in band information. The amount of attenuation required can be calculated from the spectrum mask defined for transmitter. Spectrum emission mask for Bluetooth is given in Fig. 5.1

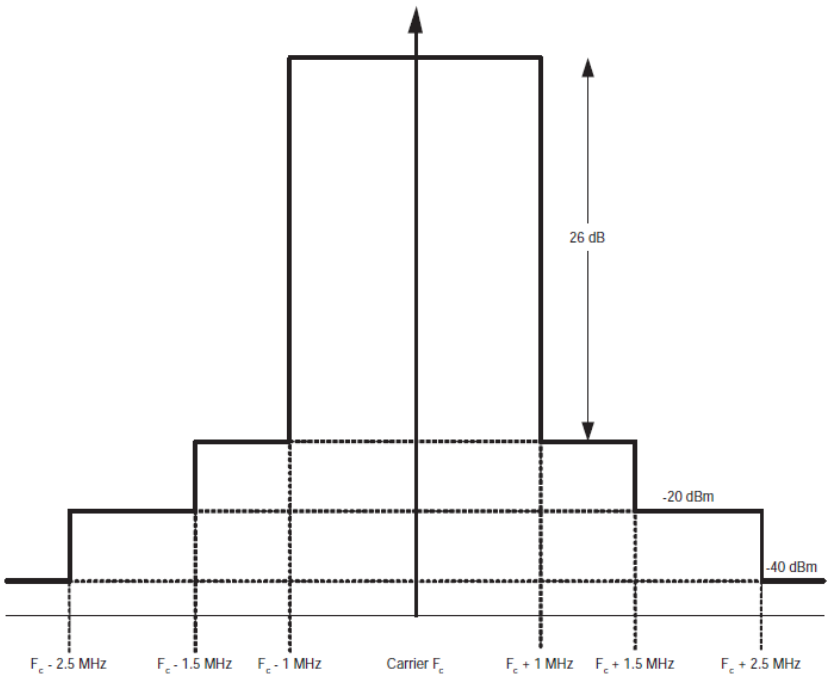

Figure 5.1: Spectrum mask

From the spectrum mask figure, it is clear that the ACPR requirement of Bluetooth transmitter is 26 dBc.

$$
\begin{aligned}
Maximum\ in\ band\ signal\ level &= 4\ dBm \\
Maximum\ out\ of\ band\ signal\ level &= -40\ dBm \\
Attenuation\ required\ at\ an\ offset\ of\ DAC\ conversion\ frequency &= 4 + 40 \\
&= 44\ dB
\end{aligned}
$$

In most of research works for Bluetooth, DAC operating at 50 MHz conversion frequency is used. So the baseband filter has to provide a minimum attenuation of 44 dB at 50 MHz. At the same time, filter cutoff frequency should be sufficiently larger than 1 MHz. The design is started with a second order filter. Chebyshev filter is superior in terms of stop band performance. But even a 2^{nd} order Chebyshev filter with small ripple (0.1 dB) in the pass band fails to provide an attenuation of 44 dB in R_{min}-C_{min} corner. A 3^{rd} filter is providing the required attenuation across all process, temperature, resistor and capacitor corners. Butterworth filter is implemented for maximally flat magnitude response in the pass-band.

5.2 Filter architecture

Typical topologies of filter implementation include the Gm-C and Active-RC architectures. The poles of Gm-C filter depend on the transconductance value which in turn is a non-linear function of the input. So Gm-C architecture based filters suffer from nonlinearity at high signal swings. Compared to Gm-C, Active-RC architectures are more linear, less noisy and result in lesser distortion for the same amount of power consumption. In RF transmitters, linearity is very important concern. For these reasons, an Active-RC topology is chosen in the design of filter.

Opamp is the main block in active-RC filters. Fully differential opamp is im-

plemented to reject the common node noise. A fully differential implementation requires cmfb loop for stable operation. At the same time, the filter has to handle large swings in the order of hundreds of millivolts. A resistive common mode detector is used at the output for better linearity. A two stage opamp is generally preferred, as single stage opamps do not provide sufficient gain with resistive loading. Design of two-stage opamp involves frequency compensation complications. Feed forward technique and Miller compensation are the two different types of frequency compensation techniques. In the Feed forward technique, a zero is introduced by adding a parallel path from the input to the output. Then opamp behaves as a second order system at low frequencies and as a first order system near its unity gain frequency. In the Miller compensation technique, the opamp is stabilized by pole-splitting. By means of pole-splitting, the opamp behaves mainly as a first order system. This technique results in a lesser bandwidth compared to the former, but the output swings are limited in the feedforward architecture. So the two-stage Miller compensated opamp is used to realize the filter.

5.3 Opamp design

: To reduce the flicker noise of the opamp, PMOS transistors are used as the input pair for first stage. If the opamp is implemented with two common mode feed back loops, then eight capacitors are required (two for cmfb1, two for cmfb2, two for miller compensation of opamp, two for resistive common mode detection at cmfb2 loop). These eight capacitors will occupy large area. To decrease the number of capacitors, single cmfb loop is used. Here only four capacitors are required. But this opamp might face start up problems. To eliminate the start up problem, one half of the error amplifier of cmfb loop can be implemented as a part the first stage. Opamp circuit diagram is shown in Fig. 5.2

Magnitude response of opamp is shown in Fig. 5.3. Phase response of opamp is

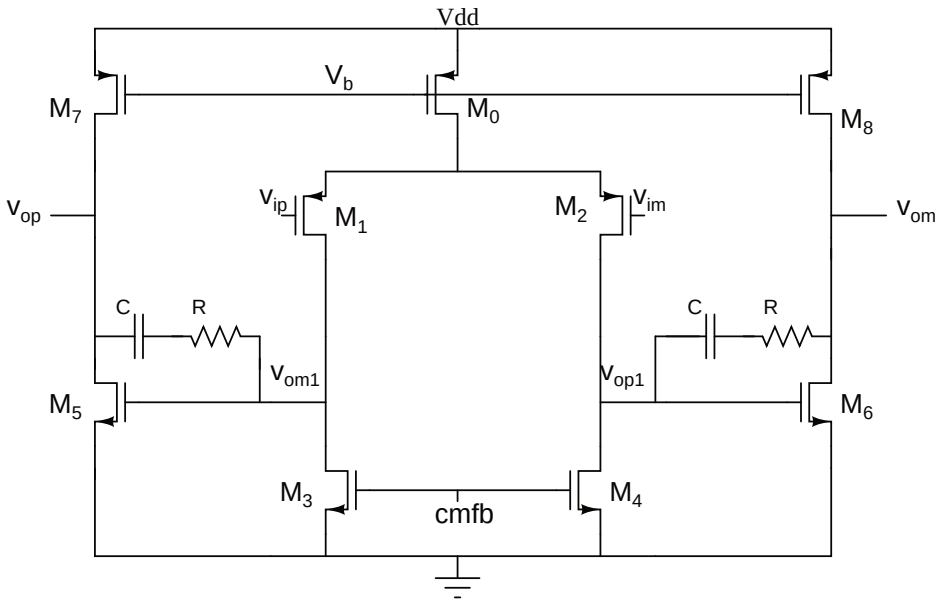

Figure 5.2: Two stage opamp

Table 5.1: Opamp component values

Component	Value
M_0	10μm/360nm
M_1,M_2	5μm/360nm
M_3,M_4	5μm/360nm
M_5,M_6	5μm/180nm
M_7,M_8	10μm/180nm
R	1.3KΩ
C	130fF

shown in Fig. 5.4

Table 5.2: Measurement results of opamp

DC gain	44.9 dB
Unity gain frequency	100.6 MHz
Phase margin	79 °
Power consumption	780μW

The opamp with UGB of 100 MHz is sufficient for the filter design. The phase margin value states that the opamp is stabilized properly.

Common mode feedback loop used for the two stage opamp is shown in Fig. 5.5. The cmfb loop is a three stage amplifier. The cmfb circuit does not give gain to get rid of stability problems. The same set miller compensating capacitors used for opamp can act as the same for cmfb loop. It is already mentioned that resistive

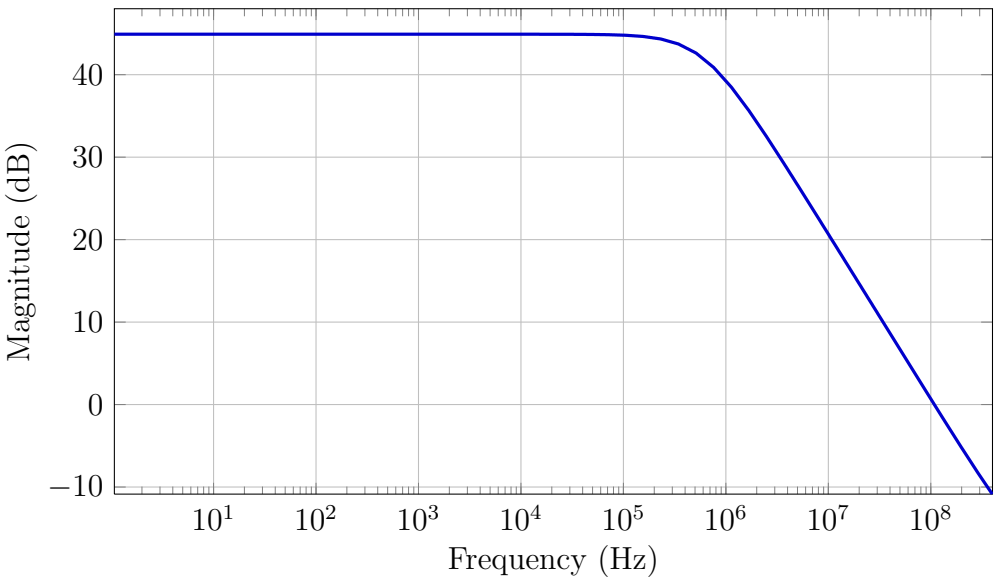

Figure 5.3: Magnitude response of opamp

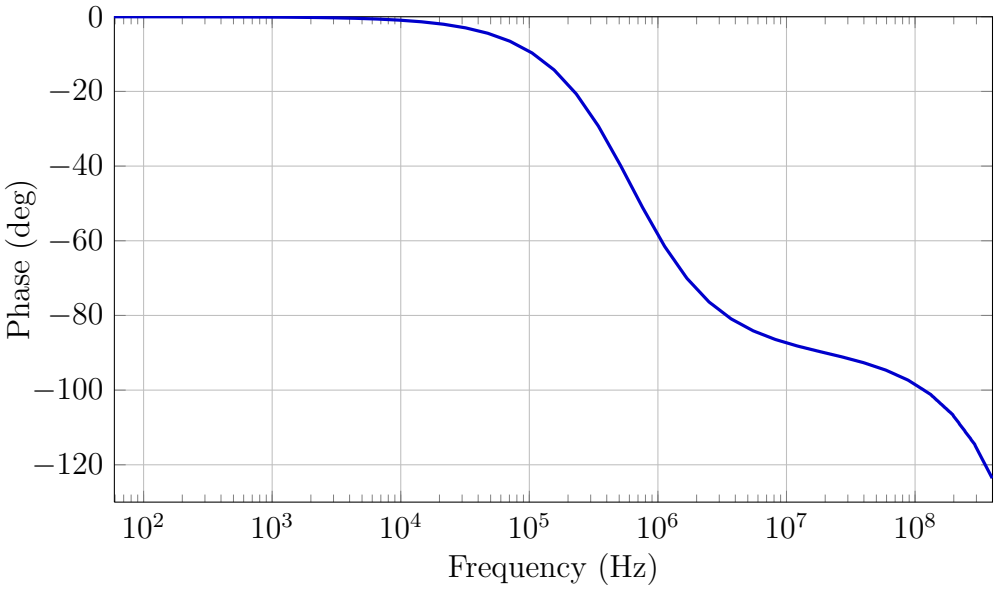

Figure 5.4: Phase response of opamp

common mode detector is used to enhance linearity. Capacitors are connected across common mode sensing resistors, to decrease the delay of the common mode feedback circuit. The detected common mode is compared with a reference voltage.

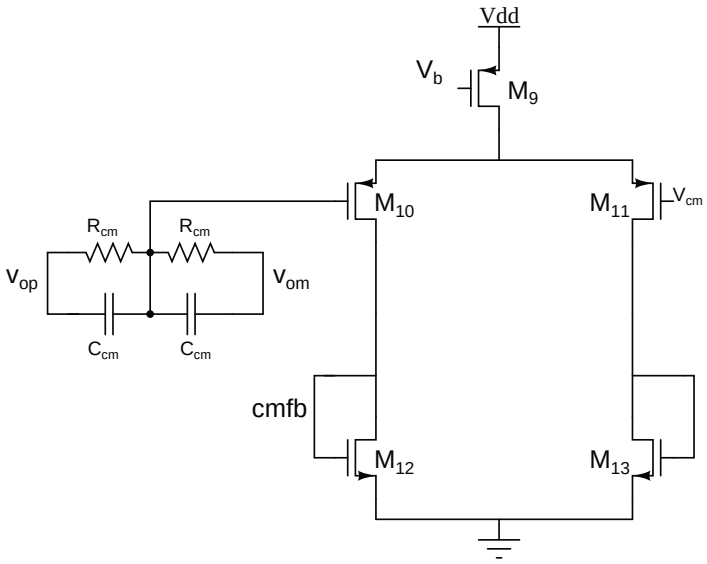

Figure 5.5: Schematic of the common mode feedback loop

Table 5.3: cmfb loop component values

Component	Value
M_9	4μm/360nm
M_{10},M_{11}	2μm/360nm
M_{12},M_{13}	2μm/360nm
R_{cm}	20KΩ
C_{cm}	50fF

Magnitude response of cmfb loop is shown in Fig. 5.6. Phase response of opamp is shown in Fig. 5.7

Table 5.4: Measurement results of cmfb loop

DC gain	54.5 dB
Unity gain frequency	132 MHz
Phase margin	59 $^\circ$
Power consumption	12μW

From the phase margin value, it is understood that the cmfb loop is stabilized.

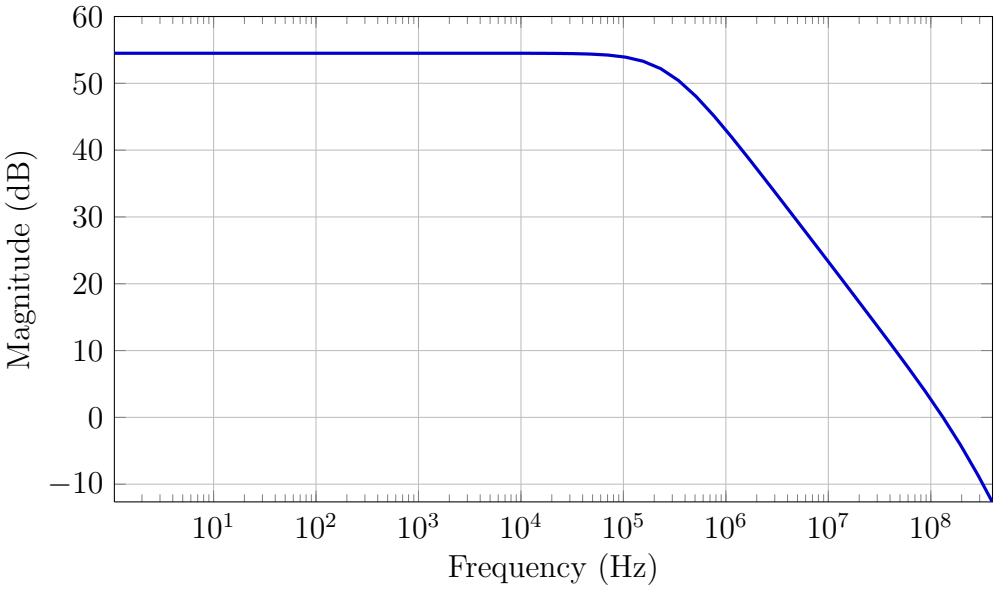

Figure 5.6: Magnitude response of cmfb loop

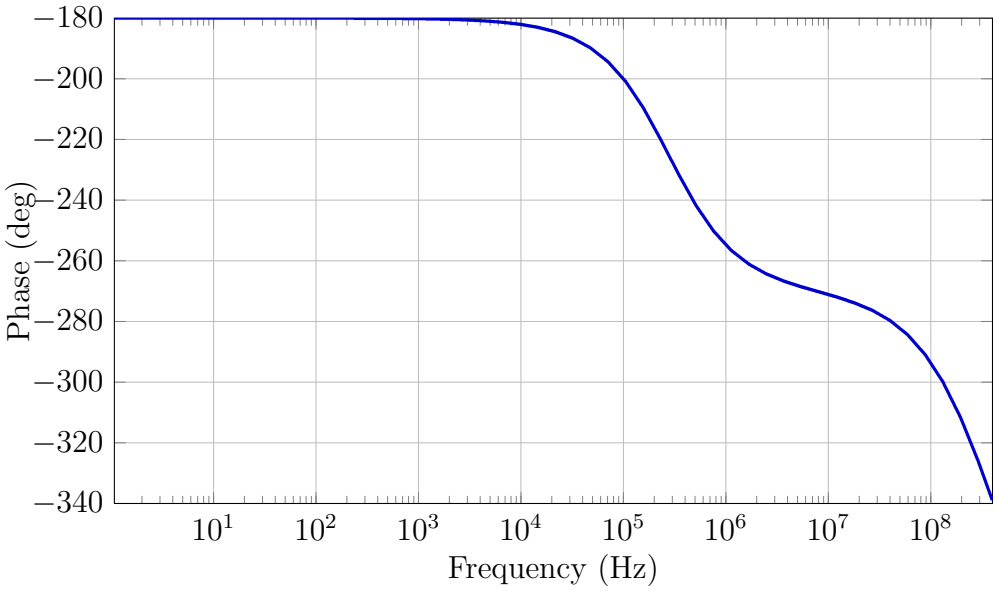

Figure 5.7: Phase response of cmfb loop

5.4 3^{rd} order butterworth filter

3rd filter is realized by cascade of one RC filter and one biquad. For the butterworth filter,

$$\begin{aligned} The\ denominator\ of\ filter\ transfer\ function &= (s+1)(s^2+s+1) \\ Q\ of\ the\ biquad &= 1 \end{aligned}$$

The 3^{rd} order baseband filter is shown in Fig. 5.8. A_1 and A_2 are the two stage miller compensated opamps. The first filter is a single pole RC filter. The second filter is a biquad. Biquad is implemented with single opamp to minimize the power consumption. Active Rauch or Multiple FeedBack (MFB) topology is used to build the biquad because active RC filter can be implemented in fully differential structure.

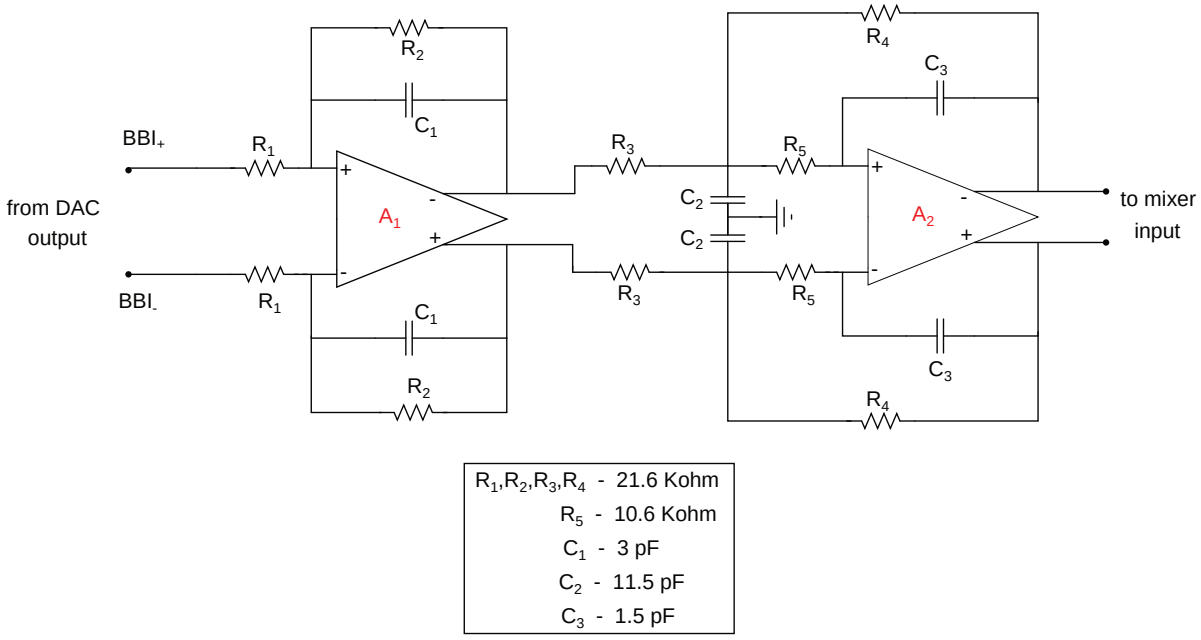

Figure 5.8: 3^{rd} order low pass filter

Magnitude response of baseband filter is shown in Fig. 5.9. The filter gives more than 44 dB attenuation at 50 MHz frequency across all corners. The plot given corresponds to R_{min}-C_{min} corner.

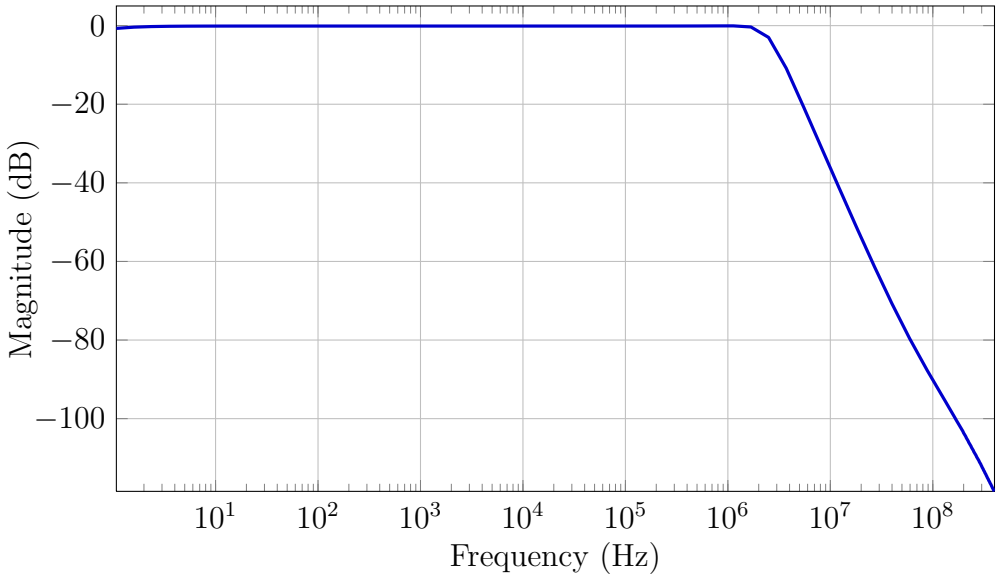

Figure 5.9: Magnitude response of baseband filter

All the three Bluetooth modulation schemes have information in phase also. So the filter should not disturb the relative positions of zero crossing points of modulated signal. All the zero crossing points should get equal delay. For this reason, filter should have linear phase. Fig. 5.10, Phase response of the filter is reasonably linear in the 1 MHz signal band.

At power amplifier output P1dB required is 10.3 dB. The gain of PA and mixer is 8 dB and -3.9 dB respectively. So at the filter output, gain compression should not happen till 6.2 dBm (10.3-8+3.9). From the Fig. 5.11, it is clear that there is no gain compression till the output power of 6.2 dBm. So it is proved that active RC filer is very good in terms of linearity. The nonlinearity at the transmitter output is mainly caused by the power amplifier.

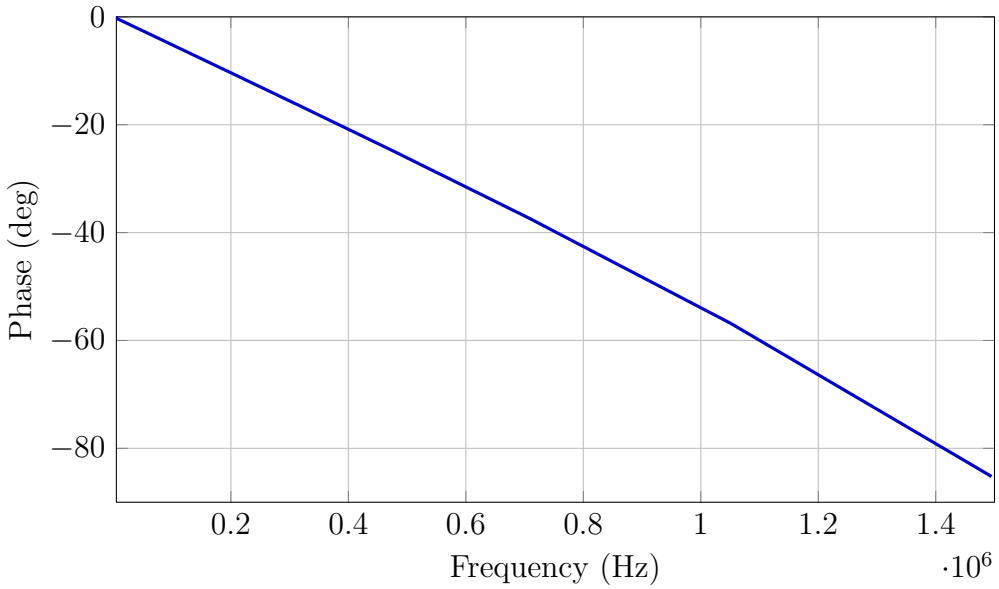

Figure 5.10: Phase response of baseband filter

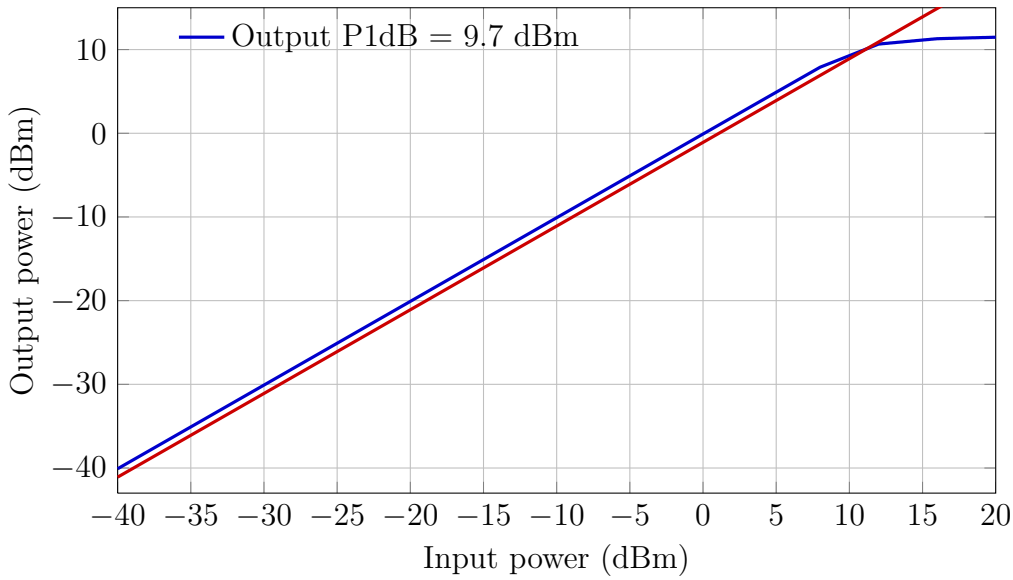

Figure 5.11: Compression curves of baseband filter

CHAPTER 6

Results and Conclusion

6.1 Results

6.1.1 ACPR

The class A power amplifier, double balanced voltage mode upconversion passive mixer and the 3^{rd} order low pass butterworth filter are combined and formed the transmitter for Bluetooth. ACPR of the entire transmitter is found to be 36 dBc, whereas the required ACPR value is 26 dBc. So the ACPR specification is met with good margin. ACPR plot of entire transmitter is shown in Fig. 6.1

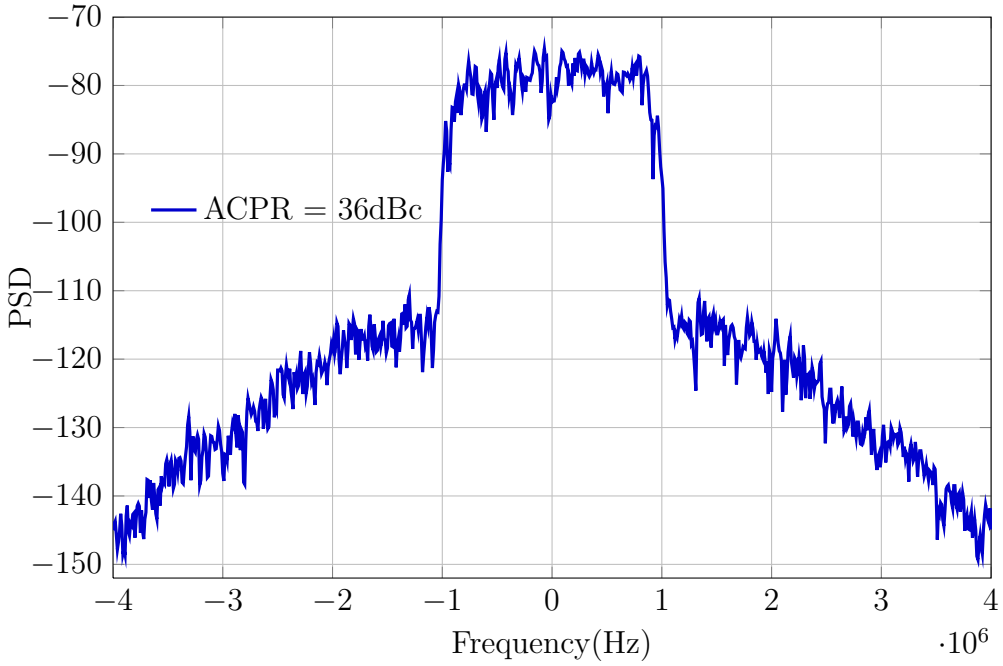

Figure 6.1: ACPR of entire Transmitter chain

6.1.2 Phase noise at transmitter output

Generally in transmitters, linearity is the important concern than noise, because the signals coming from DAC itself are several hundreds of millivolts. But noise of transmitter is also an important concern for FDD systems because of the limited isolation provided by the duplexer filter. In FDD systems, transmitter and receiver are working at same time with a frequency offset. The transmitter output noise should not rise the noise floor of receiver. Thats why FDD transmitters have an important output phase noise specification. In TDD systems, transmitter and receiver are not working at same time. A RF switch connects any one of the transmitter and the receiver to antenna. So the output noise of TDD transmitter doesn't effect on noise floor of its corresponding receiver. But it is not supposed to desensitize some other user's receiver. So generally the noise specification for TDD transmitters is much more relaxed than compared to that of FDD transmitters.

Bluetooth is a TDD system. There is not any specification mentioned for output phase noise of transmitter in Bluetooth official document. But for completeness sake, the transmitter output noise is measured at offsets of 1 MHz and 20 MHz. The phase noise plot is shown in Fig. 6.2. As the VCO is not implemented for this design, the phase noise is measured with ideal LO source.

6.1.3 Corner simulations

The important results of entire transmitter is simulated across all corners. Five process corners (tt, ss, ff, snfp, fnsp) and three temperature corners (-40°, 27°, 110°,) are giving 15 total corners.

From Fig. 6.3, ACPR is more than 36 dBc across all corners.

From Fig. 6.4, the maximum DC power consumption is 30.6 mW.

From Fig. 6.5, the gain of transmitter chain is varying from 3.2 dB to 5.4 dB.

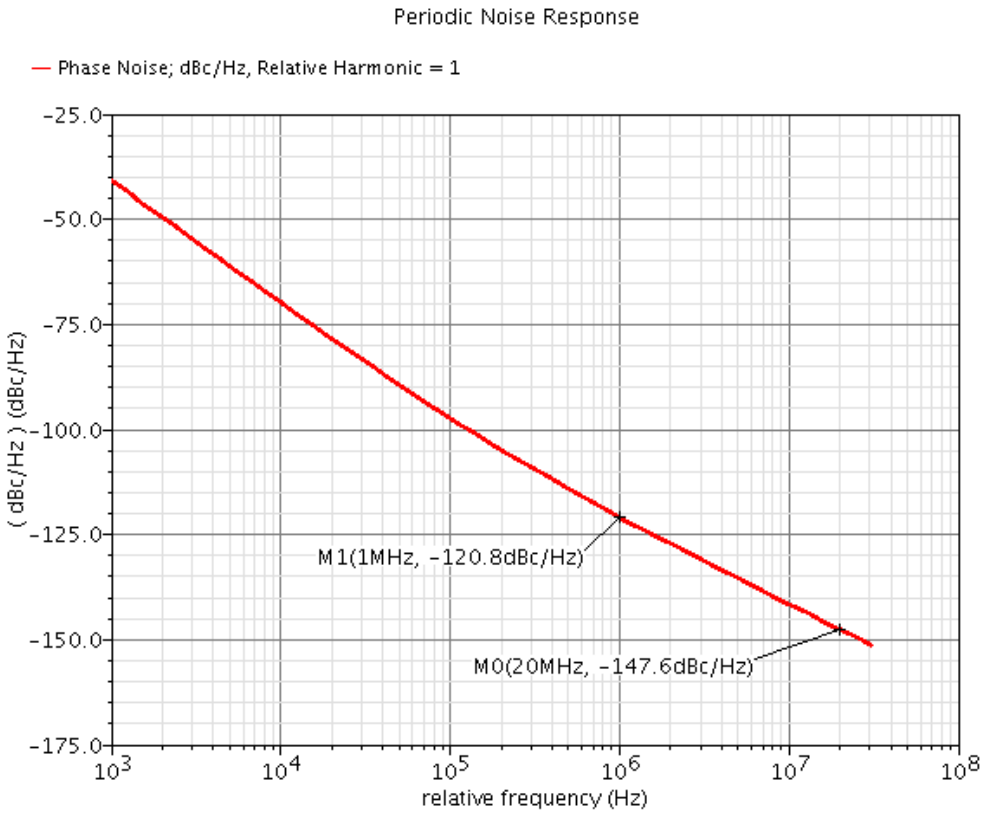

Figure 6.2: Phase noise at the transmitter output

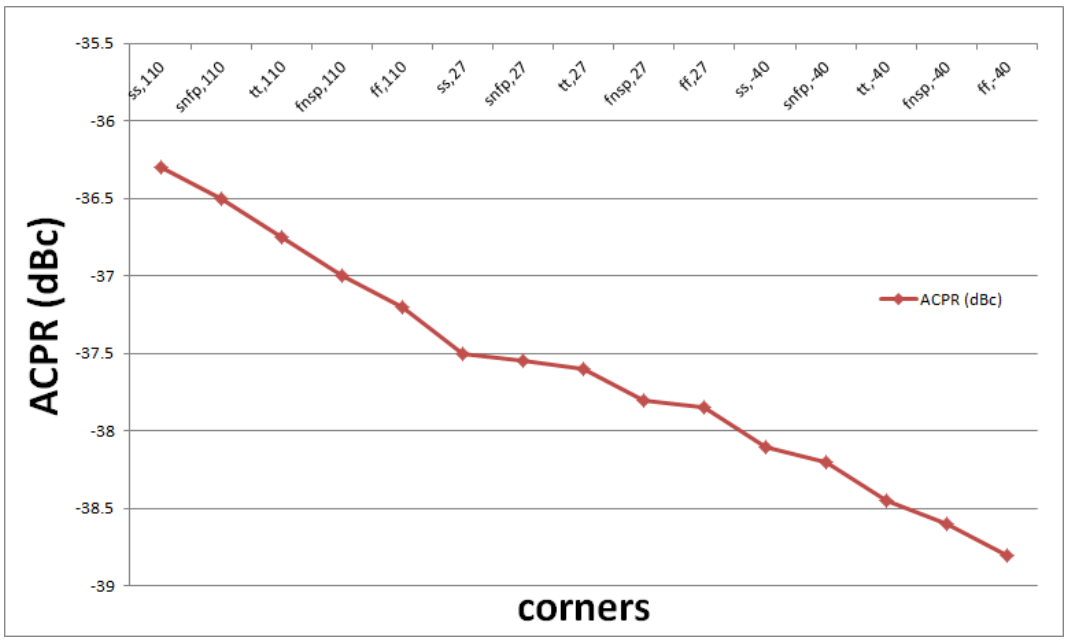

Figure 6.3: ACPR variation across corners

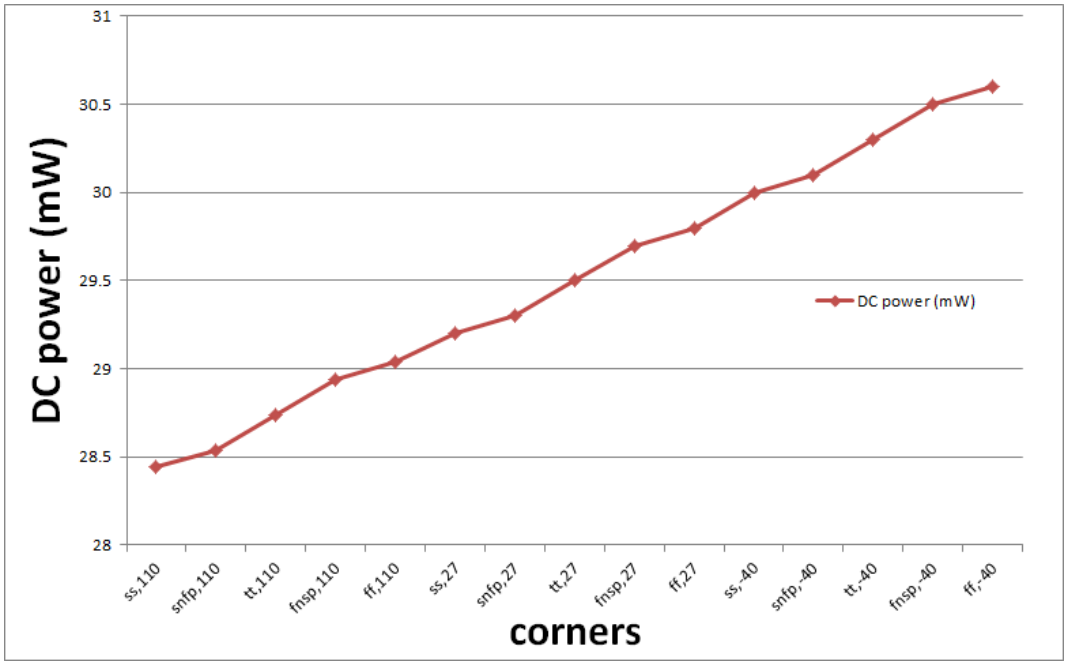

Figure 6.4: DC power variation across corners

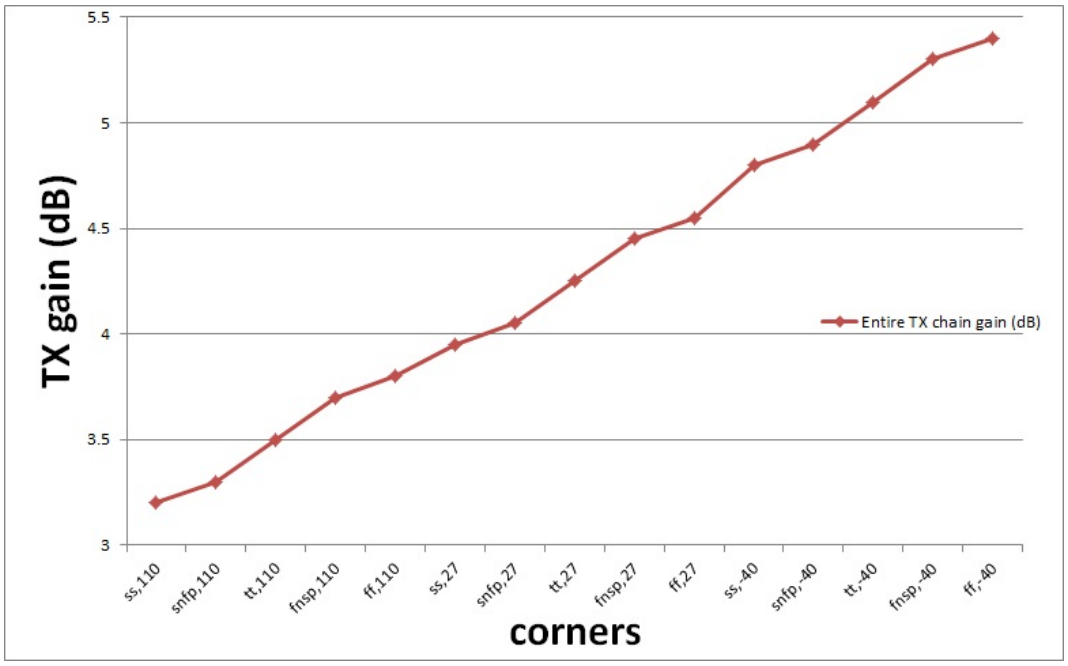

Figure 6.5: Transmitter gain variation across corners

Other important results of the transmitter chain is given in Table 6.1.

Table 6.1: Other Important Results

Parameter	Value
Supply	1.2
PA gain	8 dB
Mixer gain	-3.9 dB
Filter gain	0 dB
Total gain	4.1 dB
PA dc current	22.5 mA
Filter dc current	3 mA
Total dc current	25.5 mA

6.1.4 Package model parasitics

All the above results are simulated with a 3 nH bond wire inductance at supply, ground, input and output nets. Because the circuit is made fully differential, the effect of package model parasitics is minimized.

6.2 Conclusion

The transmitter parameters are compared with other published transmitters in Table 6.2. Power consumption is optimized by considerable amount.

Table 6.2: Comparison of power dissipation to published transmitters

Parameter	This Work	[4]	[5]	[6]	[7]
Technology	65nm	0.18-μm	0.13-μm	0.18-μm	65nm
Supply (V)	1.2	1.5/2.5	1.2/3.3	1.8/2.5	1.2/3.3
Power Diss. (mW)	30.6	100	89	91	78
ACPR (dBc)	36	50	35	36	Not specified

The main reason for power optimization is the use of 1.2 V supply for power amplifier. Other published implementations used higher supply voltage for power amplifier whereas it is the same supply used for entire transmitter here. Because of

the differential implementation, transformer is used. It occupies some considerable area. However usage of inductor is inevitable in power amplifier implementation

EVM is another important specification of transmitters like ACPR. The peak EVM of Bluetooth transmitter has to be less than 25% and RMS EVM has to be less than 15%. EVM is not measured for the transmitter here, because of the unavailability of the set up to measure it.

6.2.1 Other possible implementation - balun less transmitter

If single ended power amplifier is implemented with single balanced passive mixer, then balun can be removed from the transmitter [8]. The transmitter contains only one inductor. But some techniques are required to eliminate the effect of package model parasitics.

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