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THESIS CERTIFICATE

This is to certify that the thesis titled Design of Analog front end for a Bluetooth Receiver in UMC 65nm CMOS,to the Indian Institute of Technology, Madras, for the award of the degree of **Master of Technology**, is a bonafiderecord of the research work done by him under our supervision. Thecontents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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ABSTRACT

Analog front end for a bluetooth receiver is designed. The motivation behind the design is to achieve the most important expectations from a bluetooth receiver namely:compactness,high sensitivity,low power dissipation,high linearity.A Direct conversion receiver architecture is chosen to achieve compactness by eliminating need for off chip Image reject Filter.The front end contains a Broadband noise cancellation low noise amplifier without any inductors which saves area making receiver compact .The receiver architecture is current mode,which avoids voltage compression at various internal noded in the circuit and helps achieve high linearity.The bluetooth receiver designed achieves a Noise figure of just 4db giving a high sensitivity of -96 dbm and an IIP3 of -10.3 dbm.Power consumption is just 20.4 mW (Vdd =1.2 V), which is very less as compared to bluetooth receivers designed so far.

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ABBREVIATIONS

DCR	Direct Conversion Receiver
IRF	Image Reject Filter
LNA	Low Noise Amplifier
TCA	Fully Differential Transconductor
NF	Noise Figure
L.O	Local Oscillator
TIA	Transimpedance Amplifier
ISM	Industrial, Scientific, Medical

CHAPTER 1

INTRODUCTION

Bluetooth is a wireless technology standard for exchanging data over short distances (from 5cm to 10m).Bluetooth operates in ISM(Industrial,Scientific,Medicine) frequency band from 2.4 Ghz to 2.48 Ghz.A total of 79 channels are present, with each channel having a bandwidth of 1Mhz.Accurately, the carrier frequency of the 79 channels can be shown as:(2402 + k)Mhz , k= 0.....78. Modulation schemes used for bluetooth are:1) GFSK- It is the Basic date rate modulation scheme, having a date rate 0f 1Mbps.It is the conventional modulation scheme used. 2) 8-DPSK and $\Pi/4$ DQPSK with data rate of 3 and 2 Mbps respectively.They constitute the Enhanced data rate modulation schemes. As stated in the abstract the main metrics of a bluetooth receiver are its compactness(high level of integration on Silicon),low power consumption , high sensitivity and linearity , in order to have a large dynamic range.A small explanation of how these are achieved in design is given in the introducion.Section 1.1 describes the Specifications given in the Bluetooth standard document version 4.0.In section 1.2 these standard specifications are translated to system level specifications for easy understanding and design at the circuit level.Section 1.3 describes the architecture of the Bluetooth receiver at block level.

1.1 Bluetooth standard document version 4.0 specifications

1.Sensitivity : The reference sensitivity for a Bluetooth signal shall be better than or equal to -70 dbm at a bit error rate 10^{-3}. 2.Interference performance: The interference performance is measured with the wanted signal at -67dbm. The magnitude of the interferer is given in the table below: 3.Out of Band Blockers: The out of band blockers applies to signals outside the band 2400- 2483.5 Mhz.In the table given below, information on the out of band blockers power levels and their respective band is given:

Table 1.1: The left coloumn shows the position of the interferers and the right coloumn shows the ratio of the interferers to the signal(which is at -67dbm)

$Frequency of interference$	$Ratio$
Co-Channel	21db
Adjacent Channel(1Mhz)	15db
Adjacent Channel(2Mhz)	-17db
Adjacent Channel(>3Mhz)	-27db

Table 1.2: The left coloumn shows the frequency of the interferers and the right coloumn shows the magnitude of the interferers.

$Frequency of interference$	$Interfererpowerlevel$
30 Mhz - 2000 Mhz	-30 dbm
2003 Mhz - 2399 Mhz	-35 dbm
2484 Mhz - 2997 Mhz	-35dbm
3000 Mhz - 12.75 Ghz	-30dbm

4.Intermodulation Characteristics: The intermodulation characteristics are checked in the following way: a.The wanted signal is kept at 6db above the reference sensitivity level, i.e at -64 dbm.It's frequency is f_0.

b.Static sine wave signal shall be at a frequency f_1 with a power level of -50 dbm.

c.An interfering signal shall be at a frequency f_2 with a power level of -50 dbm . f_0 is frequency in the band of interest , i.e 2.402 Ghz - 2.48 Ghz

f_1,f_2,f_0 are chosen such that $2 * f_1$ -f_2 = f_0 and $|f_1 - f_2|$=n * 1 Mhz, where n can be 3,4 or 5.

5.Maximum usable level: The maximum usable input power level shall be -20 dbm or better.

1.2 Translating Bluetooth standards to system level specifications

1.Deriving Noise Figure (NF)from Sensitivity : The sensitivity expected out of a bluetooth receiver is -70 dbm or less.The project aims at a sensitivity of -96 dbm. Sensi-

tivity(S) of any reciever chain is given as : S = -174 dbm/Hz + 10 log (B) + NF + $(SNR)_o$

B = bandwidth of bluetooth signal (1Mhz), NF is the integrated Noise figure of the receiver(from corner frequency to 1 Mhz),$(SNR)_o$ is the minimum signal to noise ratio required at the output of the receiver.This number is typically 14 db for bluetooth signal(with GFSK modulation scheme). Therefore,S = -100 + NF , in order to achieve S of -96 dbm or less , NF must be less than or equal to 4 db.

2.Deriving 1 db Compression point from out of band interferer level :As can be seen in Table 1.1 and Table 1.2 the largest blocker is an out of band blocker of magnitude -30 dbm in frequency range 30 Mhz to 2000 Mhz.In order to avoid compression due to the blocker the 1 db compression point of the bluetooth receiver must be more than -30 dbm.

3.Input referred third order intercept point(IIP_3):The derivation of the required IIP_3 is a little complicated. Referring to standard specifications of bluetooth on intermodulation, the input bluetooth signal should be at -64 dbm. From the input signal level, we can find the magnitude of the integrated noise floor, which is -64 - SNR_o=-64 - 14= -78 dbm. In a two tone test to determine the IIP_3 , two tones(very closely spaced in-band interferers) are applied and their levels are raised until the third order intermodulation components equals the integrated noise floor.

In our case, the closely spaced tones are at frequency f_1 and f_2 which are given as: f_1,f_2,f_0 are chosen such that $2 * f_1$ -f_2 = f_0 and $|f_1 - f_2|$=n * 1 Mhz, where n can be 3,4 or 5.(f_o is the frequency of the input bluetooth signal)

IIP_3 = $P_{int} + \frac{(P_{int}-IM_{in})}{2}$

P_{int} = Level of interferer is specified in the intermodulation test as -50 dbm.

IM_{in} = integrated noise floor which is -78 dbm.

Therefore IIP_3 = -36 dbm.

1.3 Block level Architecture of the Bluetooth receiver

The figure of the architecture of the analog front end of bluetooth receiver is shown below(Figure 1.1)

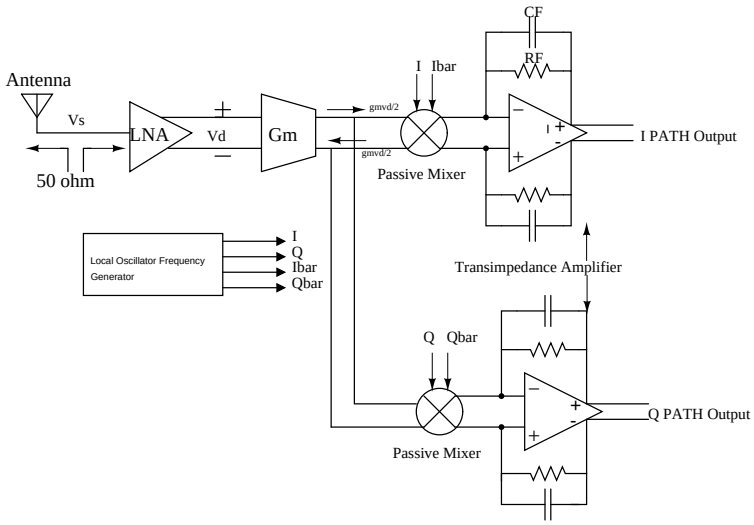

Figure 1.1: Architecture of the Bluetooth receiver

The architecture chosen for bluetooth receiver here is a Direct conversion receiver(DCR) architecture.Two reasons for choosing this architecture are:

1.There is no concept of image in a DCR,so there is no requirement of an Image reject filter.The image reject filter is placed before the mixer and needs a Q factor of more than 2400(i.e 2.4Ghz/1Mhz) for very high IF receiver and to even high values for low I.F receivers.Such high Q bandpass filters cannot be designed on chip and hence implemented off chip.Hence,non requirement of an Image Reject Filter helps in implementing the entire receiver(RF plus baseband blocks) on chip,hence making the receiver compact.

In the case of non zero I.F receiver,the LNA has to drive an off chip Image reject filter, where issues of maximum power transfer arise between the on chip LNA and off chip image reject filter.Similarly filter has to drive the mixer which should be designed to have an input impedance of 50 ohm for matching.This makes the design of a non-zero I.F complex compared to a DCR architecture.

2.In baseband part of the architecture the channel selection filtering is done by simple low pass filters with cutoff frequency of 2-3Mhz which are easily implemented on chip.Whereas in case of a high I.F receiver, a high Q channel select bandpass filter

would be needed,though a high I.F will help in a better image rejection.Similarly a low I.F will make the channel selection filtering easy but it leads to requirement of very high Q Image reject filter.So, there are tradeoffs in Image reject filtering and Channel select filtering.In DCR we avoid playing with these tradeoffs as a simple low pass filter is needed for channel select filtering.

If the spectrum of the signal received is antisymmetric, then direct frequency translation to baseband will lead to self corruption of the signal, hence two paths are chosen for the output namely in-phase path(I- path) and quadrature-phase path(Q-path).With I path and Q path amplitude and phase can be attained correctly.

A current mode architecture is used as it helps us reduce the volage swings to ideally zero at some of the internal nodes in the reciever.This helps avoid compression at the input for some of the blocks giving a higher 1-db compression point.

A brief qualitative overview on the presence of LNA, transconductor ,Mixer and TIA is explained in the following paragraphs.

The signal received by the antenna has to travel a considerable distance on the chip before reaching the LNA and as the distances the incoming R.F signal has to travel becomes comparable to the wavelength of the signal, we have care about signal reflections at the input of the R.F front end.LNA, Low noise amplifier provides an input impedance matching to the antenna for minimising the reflections.

One of the aim of the project is to avoid use of inductors in the R.F front end.So,a broadband LNA is chosen.But as compared to conventional LNA designs which consist of cascode Common source LNA the broadband LNA doesn't have a tuned input, and can't reject a lot of out of band noise(S/N noise ratio is enhanced by passive signal amplification at the input in Common source cascode LNA's)which intuitively leads to higher noise figure contribution by LNA.So, a technique known as Noise cancellation is utilised which helps in achieving a low Noise figure contribution from LNA at the cost of little higher current consumption.The LNA is designed to have a variable gain step of 6db to achieve a high dynamic range.Detailed design of variable gain LNA is explained in Chapter1.

As the LNA differential outputs have different output impedances , the output R.F currents can't be fed directly to a current mode passive mixer.So, a fully differential

transconductor is used to feed equal signal currents into the current mode passive mixer.

The current mode passive mixer translates the incoming R.F signal to baseband.As the R.F currents from the transconductor are differential a fully differential passive mixer is chosen.Also the mixer chosen is of 25% duty cycle in order to avoid I-Q crosstalk.It will be discussed in detail in chapter 2 that a 25% has a better noise performance as compared to a 50% duty cycle mixer.The switches in the mixer are sized in such a way that the mixer contributes low noise and high linearity to the receiver.A detailed noise analysis of a current mode passive mixer is discussed in chapter 2.

The down converted currents are converted to differential output voltages using a transimpedance amplifer(TIA).As bluetooth signal has frequency component at dc the TIA is dc coupled to the mixer.Because the TIA is dc coupled to the mixer, flicker noise of input transistors in the TIA becomes the topic of key importance in it's design.This leads to sizing the input transistors in the TIA in a way to minimise the flicker noise, otherwise the flicker noise may completely drown out the signal near dc to few hundred kilohertz.TIA is also designed for the receiver to have a high dynamic range,as the input baseband currents are converted to the voltages at the output stage of the two-stage opamp.Hence, if we ensure a high 1-db compression point of the output stage the linearity of the receiver can be improved.

Also ideally a TIA has zero input impedance due to which there are zero input voltage swings at it's input,hence there is no compression caused to the input differential pair in TIA.This enhances the overall linearity of the receiver chain and is the main feature of the project. A simple first order low pass filter is implemented with the TIA to have a cut off of 2.5Mhz to pass the bluetooth signal of bandwidth 1 Mhz.

CHAPTER 2

LOW NOISE AMPLIFIER(LNA)

The LNA chosen for the receiver is a broadband LNA to avoid usage of any inductors in the design(i.e one with tuned input and output).The circuit diagram of the noise cancellation LNA is shown below:

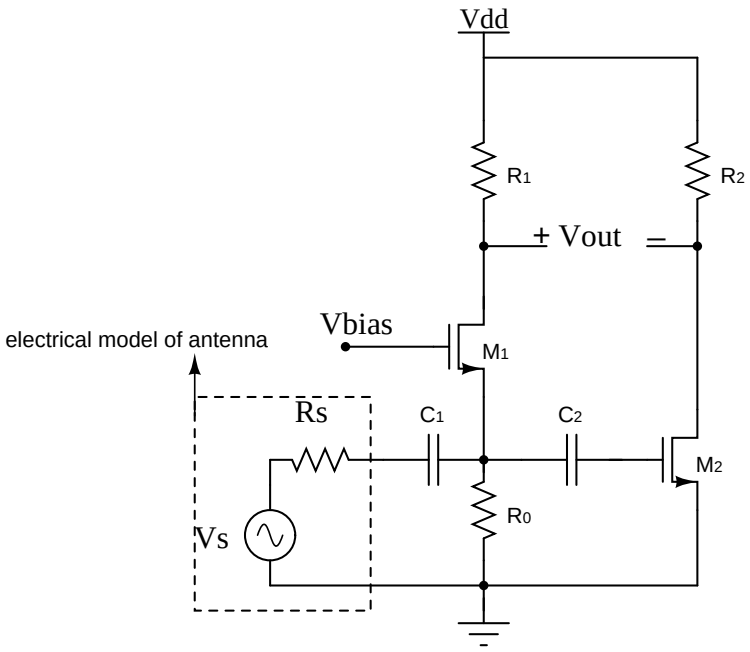

Figure 2.1: Low noise amplifier

The following are the key design aspects of an LNA:

2.1 Input Return Loss

The signal received by the antenna has to travel a considerable distance on the PCB before reaching the receiver front end,which may result in voltage reflections and hence attenuation.If the antenna is terminated in a 50 ohm load then the reflections can be minimised, just similar to terminating a transmission line (let's say of characteristic impedance of 50 ohm) to a 50 ohm load to make reflections zero.Hence input impedance

matching is of prime concern in design of LNA.The quality of the input match is expressed by the "input return loss"(Γ) defined as ratio of reflected power to incident power with the output of LNA matched to 50 ohm. Γ is given as:

$\Gamma = \frac{(Z_{in}-R_s)^2}{(Z_{in}+R_s)^2}$ where Z_{in} is the input impedance of the LNA and R_s is the source impedance , in this case antenna's source impedance is 50 ohm. The input impedance matching is explained with help of figure 2.2

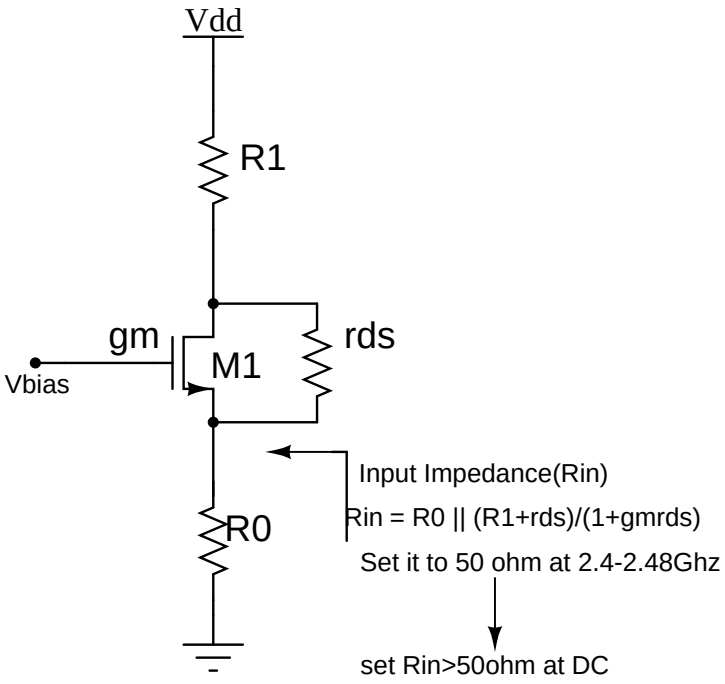

Figure 2.2: Input impedance matching of LNA

The LNA is designed is designed with minimum channel length of 60nm in order to preserve nodal bandwidths to at least equal to signal frequency(i.e 2.4 - 2.48 Ghz).The common gate (CG) and common source (CS) transistors M1 and M2 respectively in figure 2.1 are biased at a current density of 12.5 uA/um which gives a maximum dc gain of 10 and f_t of 30 Ghz.The importance of biasing the transistor at high dc gain is described in the design aspect of "Noise figure" in the chapter.The input and output nodal bandwidths of the LNA are about 4 Ghz , i.e little higher than the frequency of operation (2.4-2.48 Ghz).Had the channel lengths been higher we could have lost out on nodal bandwidths in the LNA because the nodal capacitors would be quadrupled in order to keep the same G_m.

The matching is done by the C.G section of the LNA in fig2.1.As the channel length chosen is 60nm channel length modulation effect also plays a role in determining the

input impedance of the LNA.The input impedance R_{in} of the ciruit in figure 2.2 at D.C is given as: $R_{in} = \frac{(R_1+r_{ds})}{(1+g_m r_{ds})} || R_0$....(eqn1)

A maximum d.c gain $(g_m r_{ds})$ is chosen according to the below plot of dc gain versus current density(I/W) for a 60nm channel length transistor set for V_{ds}= 600mV.

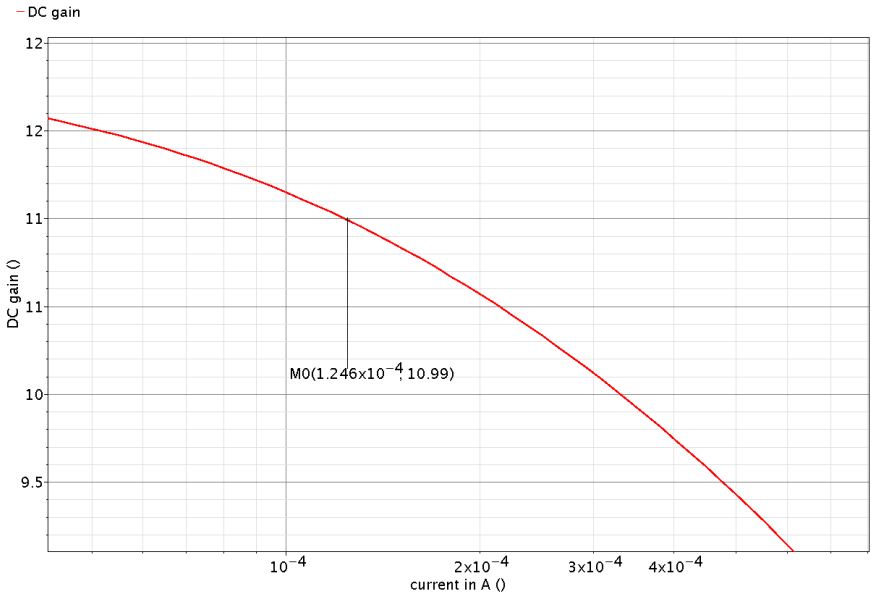

Figure 2.3: DC gain versus current plot in a 10u/60nm transistor

Choice of g_m:It looks from the formulae of R_in that g_m can be chosen in a way to minimise the current consumption in common gate part of LNA.But,the input referred noise of R_1 is inversely proportional to the square of g_m hence g_m can't be made arbitrarily small to reduce current consumption.

How to choose g_m? Looking at the long channel counterpart of figure 2.2 ,the input impedance is simply $\frac{1}{g_m}$.To have R_{in} of 50 ohm ,g_m is set to 20 mS.Taking this hint,the g_m of M_1 is chosen to be 20 mS.

M_1 is biased at a Vd_{sat} of approximately 75 mV to maximise IIP_3.So the current required in M_1 can be calculated from:$g_m = \frac{I_d}{Vd_{sat}}$($g_m$ for a short channel transistor) which comes out to be 1.5 mA. R_1 and R_0 is chosen as 424 ohm and 300 ohm in order to minimise their noise figure contribution and also in such a way,that a current consumption of 1.5 mA gives a Vds of at least 200 mV for M_1.Hence from equation 1,R_{in} is 85 ohm at D.C. R_{in} is purposefully kept higher at D.C to get the required(with some additional room of 10 ohm for to burn more current in M_2 to lower it's noise figure contribution) 50 ohm input impedance at the frequency band of interest(2.4 - 2.48 Ghz).

The plots for input impedance and S_{11}(input reflection coefficient) can be seen below respectively:

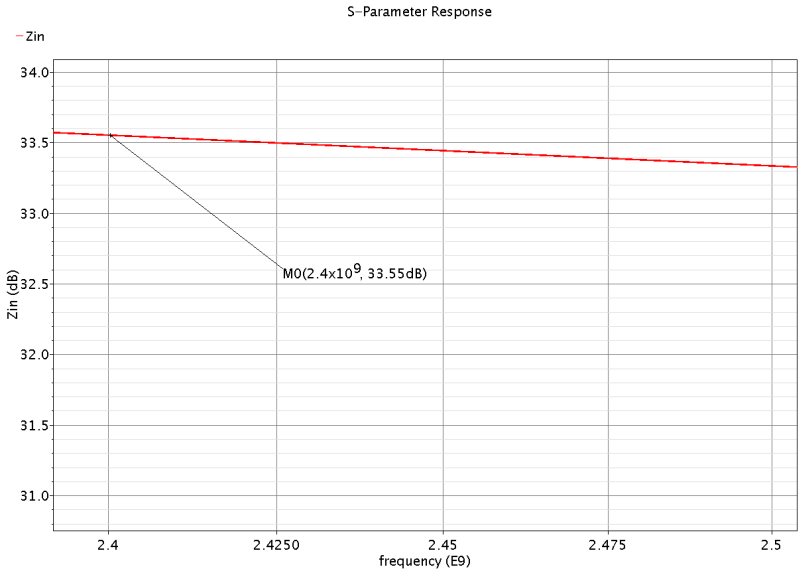

Figure 2.4: Input impedance of LNA matched to 50 ohm

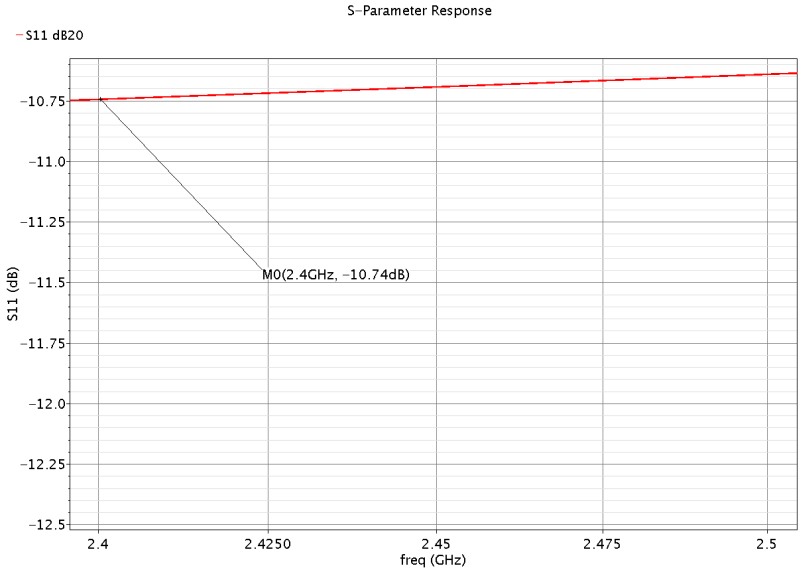

Figure 2.5: S_{11}

2.2 Noise Figure

The LNA chosen is a broadband LNA, i.e without any tuned input and output.So, we are using a technique of noise cancellation by which the drain thermal noise of common gate transistor M_1 is cancelled.Then the components which cause noise are M_2,

R_1,R_2.The design of these components to minimise the overall noise figure of LNA is discussed in detail.

Noise cancellation of M_1 is explained with the help of figure 2.6

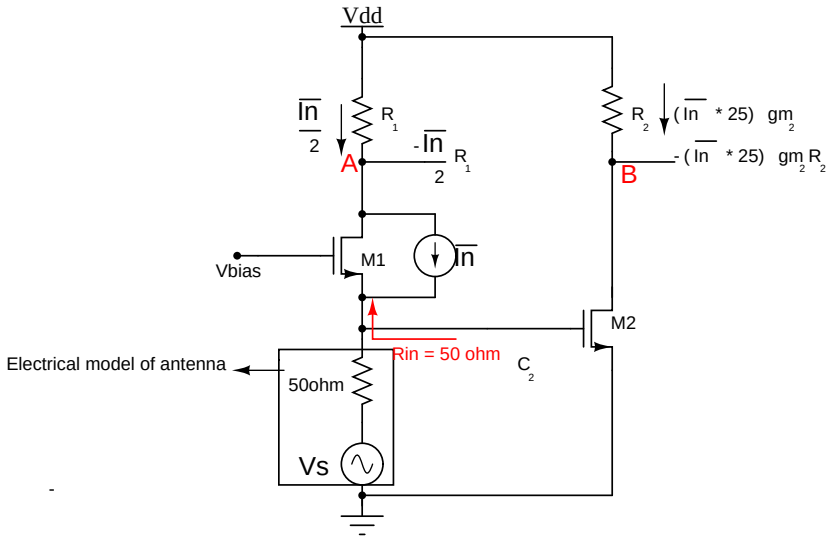

Figure 2.6: Noise cancellation of M_1

The aim is to identify two nodes in the circuit(node A and B),on which the drain thermal noise of M_1 appears in the same polarity and the the signal V_s appears with opposite polarity, so that when a differential output is taken across these two nodes , then noise of M_1 is cancelled and signal is added.

The figure shows only the signal picture, biasing details of the transistors is not shown.Neglecting channel length modulation,the input impedance looking into the source node of M_1 is matched to antenna's 50 0hm impedance.As shown in the figure, the noise of M_1 appears as -$\frac{I_n}{2}$ R_1 on node A and as (I_n * 25) g_{m2} R_2 on node B. If we set R_1 = 50 g_{m2} R_2 the drain thermal noise of M_1 is cancelled. The result can also be formulated as R_1 = R_s g_{m2} R_2 as R_s is the antenna's resistance of 50 ohm.But $g_{m1} = \frac{1}{R_s}$.Hence,if gains of the two sides that is the Common Gate side(g_{m1} R_1) and Common source side(g_{m2} R_2) are equal then the noise of M_1 is cancelled.

Hence ,our aim is to make the gains of the CG side and CS side in figure 2.1 as exact as possible to cancel the noise of M_1.After cancelling the noise of M_1 the noisy components are R_0,R_1,M_2 and R_2.

How to decide a value for the biasing resistor R_0 to minimise it's noise contribution? Let the thermal noise current power spectral density(PSD) of R_0 be ${I_{R0}}^2$. The contribu-

tion of noise of R_0 to the NF of the LNA is given as $\frac{Rs}{R_0}$.Therefore, R_0 is selected large as compared to R_s(antenna source resistance 50 ohm).The upper limit of R_0 is fixed by the voltage headroom assigned to it.The voltage headroom assigned to it is around 400 mV.The voltage headroom is so assigned because, we need a larger headroom for R_1 as it is the dominant noise contributor in the LNA and it has to be made larger for reducing it's noise contribution. In our design R_0 is fixed to a value of 300 ohm.Thus R_0 contributes only 16 % to the NF of the LNA.

How to decide a value for the biasing resistor R_1 to minimise it's noise contribution? The contribution of R_1 to the NF of the LNA is $\frac{1}{g_{m1}R_1}$.For a fixed g_{m1} of 20 mS, only way to reduce the noise of R_1 is to keep it to a value of $\frac{600mV}{1.4mA}$= 428 ohm. So, R_0 is set to a value around 420 ohms.

How to bias M_2 to minimise it's noise contribution?

The V_{dsat} of M_2 is fixed to a value of 75mV to maximise it's IIP_3.It's contribution to the NF of the LNA is given as:$\frac{4kT\gamma}{g_{m2}}$.Hence, only way to minimise the Noise figure contribution of M_2 , is to increase g_{m2} which means we have to burn more current in CS side of the LNA.A current consumption of up to 6 mA is allowed on the CS side.Therefore, the g_{m2} of M_2 is given as $\frac{6mA}{75mV}$ = 80 mS.The gain on the CG side is fixed to 4 because of limited headroom of just 200 mV to M_1 and channel length modulation effect.So, R_2 is chosen such that equivalent output resistance of M_1 i.e r_{ds2} || R_2 is equal to $\frac{4}{80mS}$ = 50 ohm.Biased at a current density of $12.5uA$/um r_{ds2}=100 ohm, so R_2 is chosen as 100 ohm to have an equivalent output resistance of 50 ohm for M_2.

Contribution of R_2 tot her noise figure of LNA is given as:$\frac{1}{g_{m2}^2R_2R_s}$= $\frac{1}{4*80mS*50}$, which is only 6.25%.

To show the effect of Noise cancellation two plots for Noise figure are shown.

First plot (figure2.7) shows the Noise figure of CG LNA alone, without noise cancellation to be 4.5db with contribution of CG transistor M_1 as 41%.

The second plot(figure2.8) shows the noise figure of LNA with noise cancellation of M_1.The contribution of M_1 to the NF is just less than 10%.The NF is 2.38 db.

The table 2.2following the Noise figure plots shows the noise contribution of each component in LNA before and after noise cancellation.

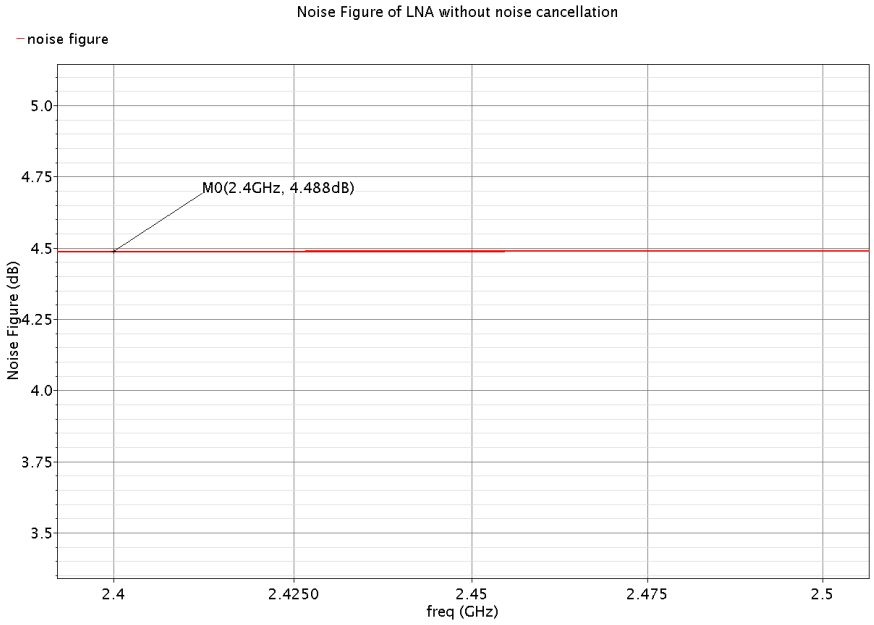

Figure 2.7: Noise figure of LNA without noise cancellation of M_1

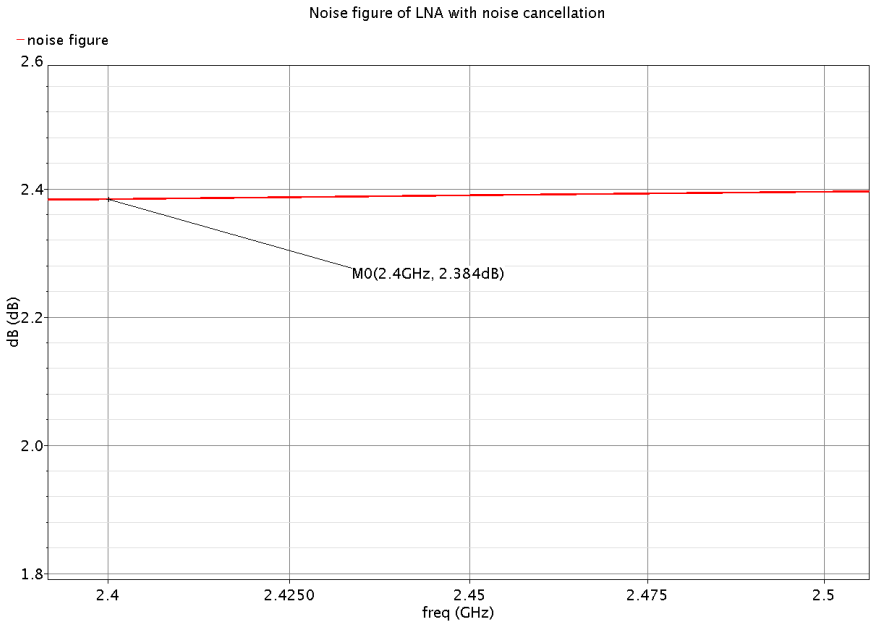

Figure 2.8: Noise figure of LNA with noise cancellation of M_1

M_1	41	9.35
R_1	16.4	12.14
R_0	6.1	9.9
M_2	X	9.15
R_2	X	1.3
$R_s(antenna)$	35	57.76

2.3 Voltage Gain

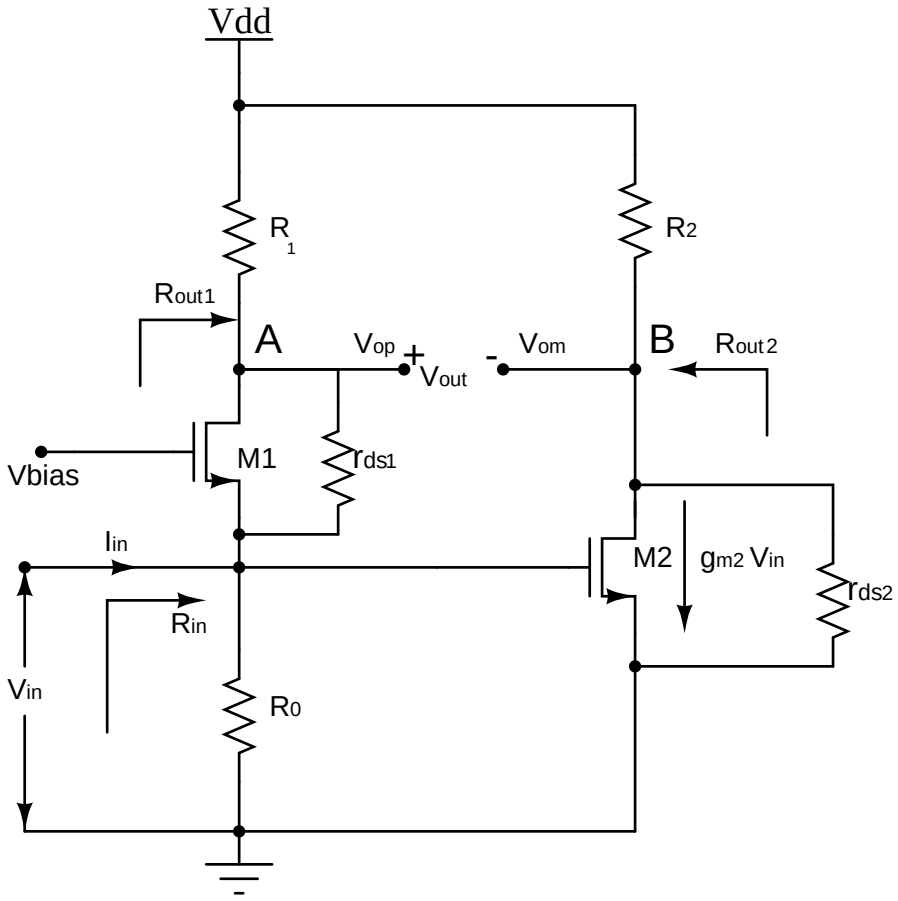

Figure 2.9: Understanding Voltage gain of the LNA

The gain of the LNA defines the overall IIP_3 of the bluetooth receiver.This is because after the transconductor, mixer and TIA does not undergo much input compression as input impedance of both the blocks is very small, approximately 9 ohm for the switch and 0.6 ohm for the TIA.Let IIP_{3LNA} and IIP_{3TCA} be the IIP_3 of the LNA and the transconductor respectively.Let the gain of LNA be A_{LNA} in db.Then the IIP_3 of the LNA referred back to the input of LNA is IIP_{3TCA} - A_{LNA}.So, keeping a low gain

in the LNA is desirable.The LNA is designed for a gain of 12 db.It has a varaible gain step of 6 db, which makes it's gain 6db lower when the input signal power is between -77 dbm and -14 dbm.The discussion on implementation of variable gain is discussed in the last section of the chapter.

Derivation of the Voltage Gain for the Noise Cancellation LNA: In figure 2.9,first neglecting the channel length modulation effect for M_1 and M_2, the gain of the Common Gate side can be written as $\frac{V_{op}}{V_in}$= g_{m1} R_1 and that of the Common source side can be written as $\frac{V_{op}}{V_{in}}$ = g_{m2} R_2.

So,the overall gain of the circuit is $\frac{V_{op}-V_{in}}{V_{in}}$= g_{m1} R_1 + g_{m2} R_2. But as the transistors M_1 and M_2 are short channel transistors, the gain is a major function of channel length modulation.The only advantage the choice of short channel length offers is, sufficient bandwidth is available on the input and output nodes in the circuit.

So, for the short channel case voltage gain is found in the following way: The input impedance of the R_{in} is given as: $R_{in} = \frac{(R_1+r_{ds1})}{(1+g_{m1}r_{ds1})}||R_0$.

The input current I_{in} = $\frac{V_in}{R_{in}}$.The output impedance R_{out1} looking into node A is given as:R_{out1} = (g_{m1} r_{ds1} R_0) + R_0 + r_{ds1} in parallel with R_1.Therefore voltage at node A is given as I_{in} R_{out2} and hence voltage gain for the Common gate section is given as :

$\frac{V_{op}}{V_{in}}$ = $\frac{R_{out1}}{R_{in}}$

In the design: (g_{m1} r_{ds1}) = 4.37, r_{ds1}= 228 ohm , R_1 = 424 ohm , R_0 = 300 ohm.

R_{out1} = 344.5 ohm and R_{in} = 120 ‖ 300 = 85 ohm. Hence, the gain is $\frac{344.5}{85}$ = 4.

The gain of the Common source side is simply written as : g_{m2} *(R_2 ‖ r_{ds2}) = 80 mS * (100 ‖ 100) = 4.

The overall voltage gain $\frac{(V_{op}-V_{om})}{V_{in}}$ for the figure 2.9 is 8, when referred to the antenna input with thevenin resistance of 50 ohm the gain becomes 4 (12 db).

A plot for the voltage gain of LNA (= 12 db) is shown below.

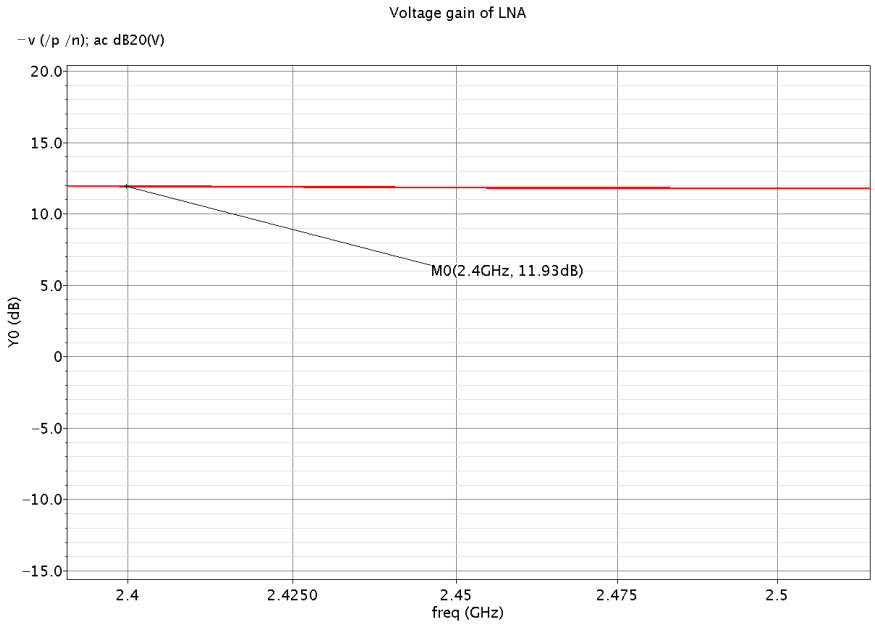

Figure 2.10: Gain for LNA = 12 db

2.4 Third order Input intercept point(IIP_3)

The drain current of a transistor can be approximated as a weak cubic non linearity in the following way:

$i_{ds} = a_1\ v_{gs} + a_2\ v_{gs}^2 + a_3\ v_{gs}^3$

a_1 is the transconductance (g_m) of the transistor.Within the input dynamic range, it is desired that i_d should only be a function of v_{gs} not it's powers.If two interferers at frequencies f_1 and f_2 appear in the frequency band of operation (2.4-2.48 Ghz) in such a way that |2 f_2 - f_1|=f_0, (where f_0 is the frequency of the channel of interest in the band),then with the presence of cubic non linearity these interferes fall on the bluetooth signal of interest at f_0, thus corrupting it.The magnitude of the third order intermodulation components is directly proportional to a_3. Therefore, it is essential that the coefficient a_3 of v_{gs}^3 be minimised at the biasing point of the transistor.

Second order non -linearity arises because of presence of v_{gs}^2 term .Looking at the receiver chain in figure 1.1, we find that if two interferers at f_1 and f_2 undergo second order non - linearity in the LNA and TCA ,second order intermodulation components appear at f_1 +/- f_2.$f_1 - f_2$ is frequency of the order of a few Megahertz and doesn't makes it's way significantly into the baseband after downconversion, because the transconductor is A.C coupled to the mixer and low frequency components are high pass filtered.The

high frequency component is approximately double the frequency of operation and is down converted to around a value of few Gigahertz.Such a high frequency second order intermodulation component is filtered by the channel select low pass filter in the baseband, in this case first order low pass filter shown with the TIA.Hence, less focus is made on minimising the second order intermodulation components.

How to minimise third order intermodulation components and achieve a good IIP_3 for the LNA and transconductor?

The IIP_3 of a source-degenerated Common Gate transistor is given in volts (peak value) as:$3.26V_{dsat}$.Therefore, if we choose a V_{dsat} such that a_1 is maximum at that point and a_3 is minimum then we can ensure, that the magnitude of the $I.M_3$ components will be minimum and the transistor will have the desired linearity between i_d and v_{gs}.

Differentiating the equation w.r.t v_{gs} three times, i_ds = a_1 v_{gs} + a_2 v_{gs}^2 + a_3 v_{gs}^3 , we get a_3 = $1/6$ ($\frac{d^3 i_{ds}}{dx^3}$) or $\frac{1}{6}$ of the second derivative of g_m.

How to find a_3 by simulation?

We first choose a transistor of channel length 60 nm and bias the drain at V_{dd} such that there is no compression at the drain(due to the transistor going into triode region).Choose an arbitrary Width, let's say 10 um.

Sweep the V_{gs} of the transistor from 0 to V_{dd} and plot the g_m of the transistor.Then, take the second derivative of g_m and divide by 6, which gives us a_3.Select the point where a_3 is minimum and g_m (or a_1) is maximum. In the design of LNA and the transconductor,the channel length of the input transistors is set as 60 nm.The optimum valueof V_gs , is selected as 500 mV (giving a V_{dsat} of 75 mV).

The below figure shows the maximum and minimum point of g_m and a_3 respectively.

The blue plot is for a_3 and red plot is for g_m.

The below figure shows the IIP_3 for the LNA.It is +5.43 dbm.

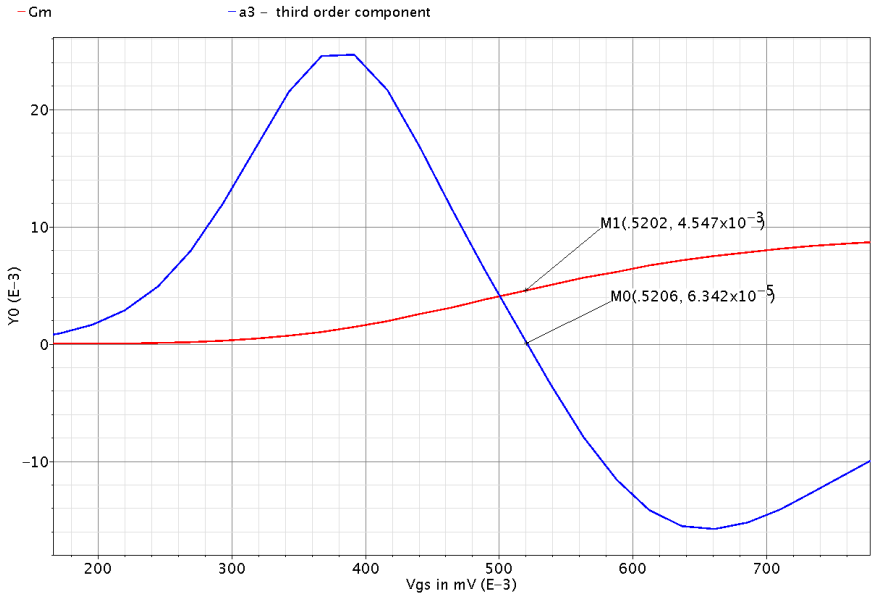

Figure 2.11: Maximising IIP_3 of LNA by careful selection of V_{gs}

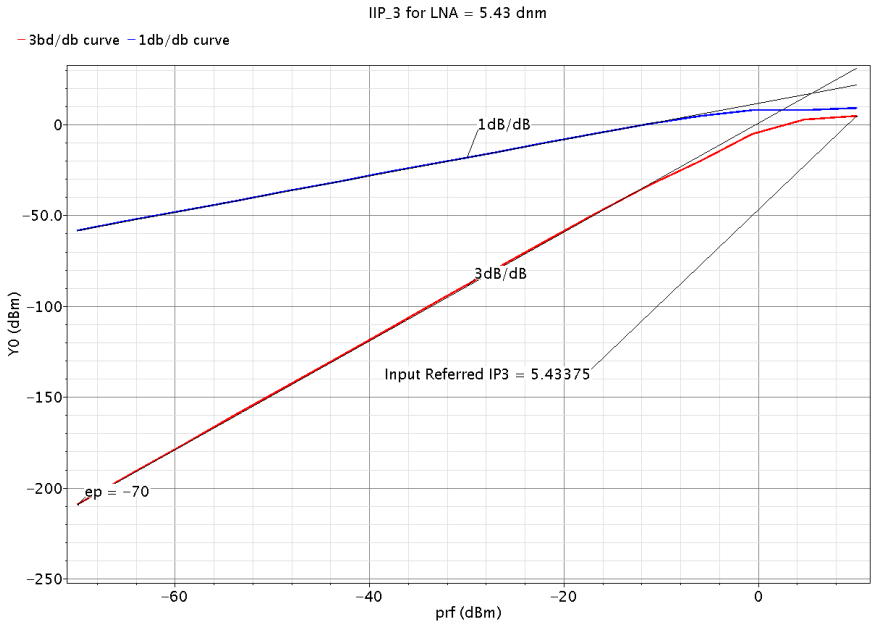

Figure 2.12: IIP_3 for LNA = 5.43 dbm

2.5 Variable gain Architecture of the LNA

Why variable gain LNA? The gain of LNA is reduced by approximately 3b along with the reduction of the transimpedance by 3 db at the same time.This is done to increase the dynamic range of the bluetooth receiver by 6 db.

The gain of the LNA is varied by changing the bias current consumed by the common gate and common source transistors M_1 and M_2 respectively in figure 2.1.This is done with the help of a constant current bias circuit as shown below:

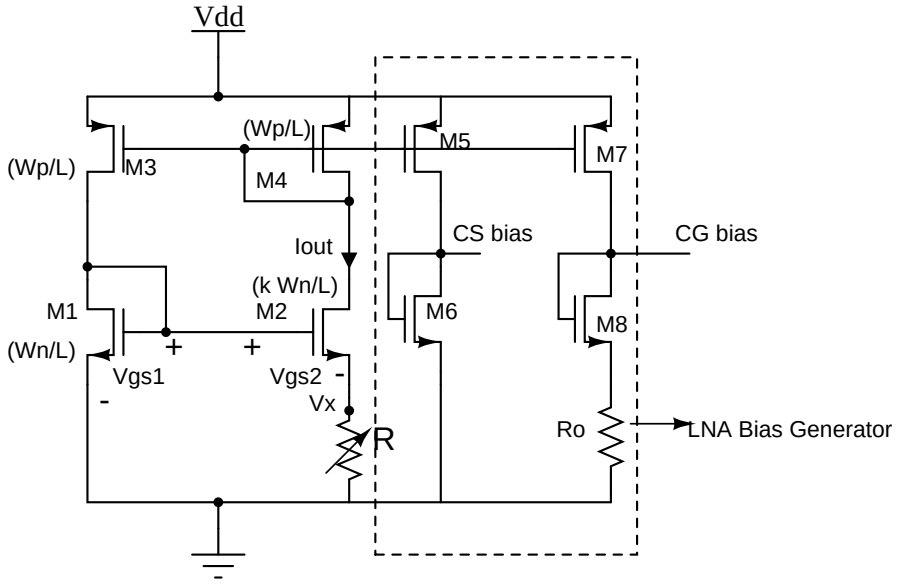

Figure 2.13: Constant current bias circuit for implementing variable gain

An I_{out} = 20 uA current is generated by the constant current bias circuit, when a maximum gain of 12 db is desired in the LNA.

A current density of 2 uA/um in M_1 gives a V_{gs1} of 513 mV.f the size of M_2 is selcted as twice the size of M_1, then it will have a smaller V_{gs} and rest of the voltage appears across the resistor R.By simulations it can be known that for M_2 with double the current density, the V$_g sis 468 mV. The node voltage$V$_x$ remains fixed at 45 mV. Hence, in order to have a output curent I_{out} of 20 uA the value of resistor R is set to $\frac{V_x}{20uA}$= 2.25 Kohm.So,the resistor R is set to about 2.3 Kohm.If the resistor is increased then the output current I_{out} is reduced and so a proportionately reduced current flows in the CG dc bias and CS dc bias path.In this way the resistor R is adjusted to a value of 18.4 K ohm to make the gain of LNA approximately 3 db lesser.A further decline in the gain of the LNA makes the S_{11} of the LNA less than -10 db.Hence only a single 3 db down

step is provided in the voltage gain of the LNA.

CHAPTER 3

Fully differential Transconductor

A simple model of the transconductor highlighting it's G_m and its output impedance at the frequency of operation(2.4 - 2.48 Ghz) is shown below:

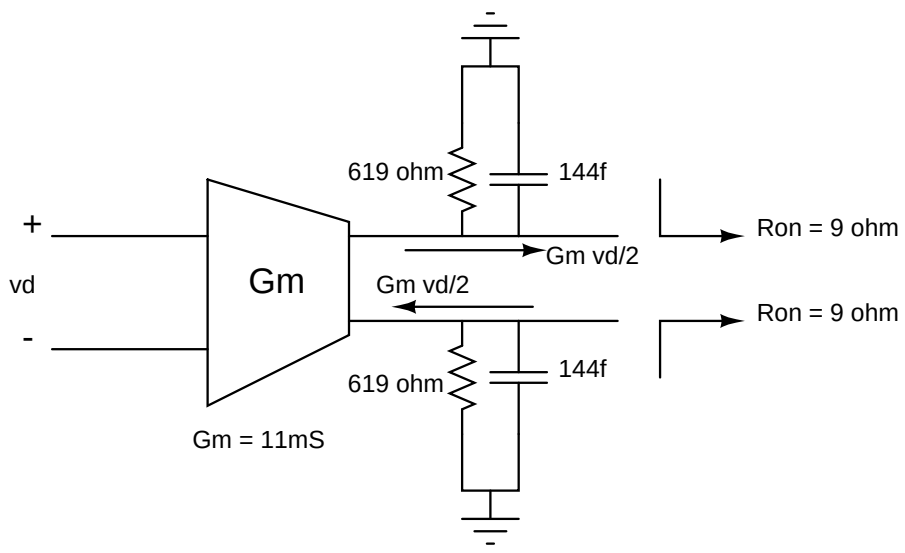

Figure 3.1: Model of a fully differential transconductor

The design aspects of the Transconductor are as follows:

3.1 Noise figure

The figure of the transconductor (figure 3.2)) is shown below:

The input referred voltage squared noise of the transconductor is given as:

$$V_{nTCA}^{2} = \frac{(8kT\gamma_n)}{g_{m1}} + \frac{(8kT\gamma_p g_{m3})}{g_{m1}^2} - - - - - - - - - - - - - - - eqn2.$$

Usually g_{m3} is kept at least 4 times less than g_{m1} and M_3 and M_4 are designed with long channel lengths so that γ_p is usually the minimum, i.e $\frac{2}{3}$.So, the noise due to the M_3 and M_4 can be ignored.

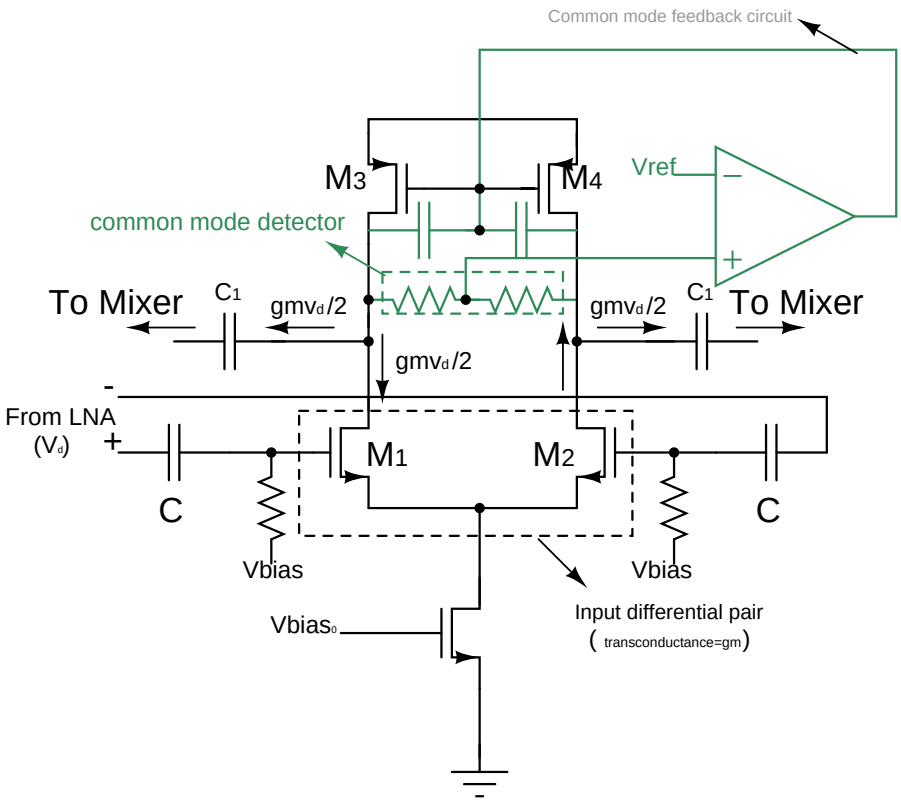

Figure 3.2: Fully Differential transonductor

So, $V_{n\,TCA}^2$ = $\frac{(8kT\gamma_n)}{g_{m1}}$.When referred to the input the LNA of gain 4 , the input referred noise due to TCA becomes $\frac{V_{n\,TCA}^2}{16}$.

k = 1.38 * 10^{23} , T = 300 K , excess drain thermal noise factor γ_n for 60 nm length transistor = 1.2.

We have to assign a noise budget to the transconductor , such that it contributes lesser noise as compared to LNA ,so that the stages ahead of LNA contrbutes less to the NF.

Let $V_{n\,LNA}^2$ be the input referred noise of LNA and let $V_{n\,R_s}^2$ be the input noise due to the antenna's source resistance R_s of 50 ohm.

Below figure shows the total input referred noise of LNA and antenna alone :

From section 2.2 , the contribution of the antenna to the input referred noise as shown in figure 3.3 is 57.76 % of which contribution of antenna is $8 * 10^{-19}\ V^2/Hz$.

Therefore,$V_{n\,LNA}^2$ = $6 * 10^{-19}\ V^2/Hz$. A noise budget of half the input referred noise of LNA is assigned to the transconductor.Therefore, $V_{n\,TCA}^2$ = $\frac{(8kT\gamma_n)}{g_{m1}}$ must be less than $3 * 10^{-19}\ V^2/Hz$ Doing the calculations, we get g_{m1} > 8 mS.For a fixed V_{dsat}

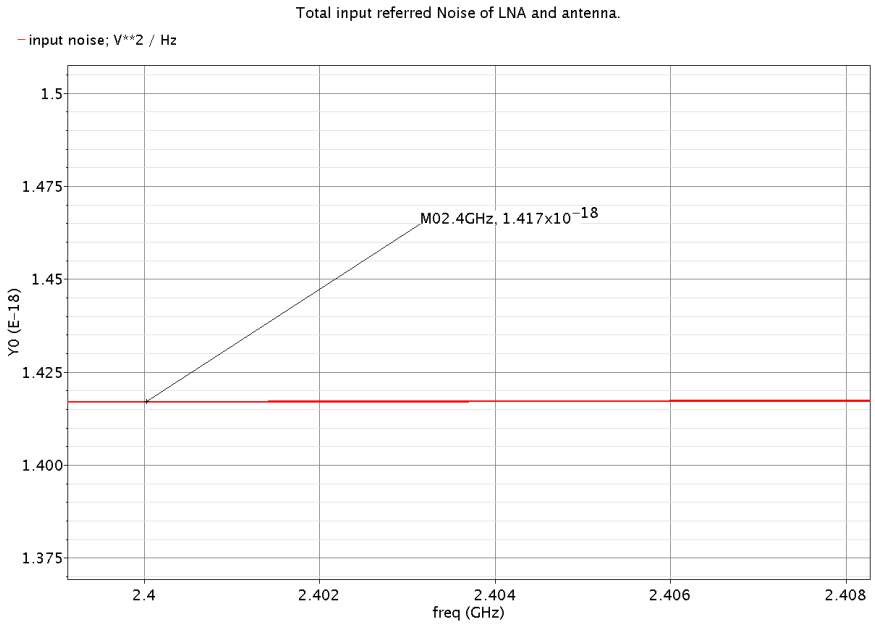

Figure 3.3: Input referred noise voltage PSD of LNA and antenna

of 75 mV to get a good IIP_3 , minimum current consumption of g_{m1} V_{dsat} = 8 mS * 75 mV = 0.6 mA is required in each transistor(M_1 and M_2).So, minimum total current consumption in the transconductor is 1.2 mA.

In our design we have set g_{m1} as 11 mS and g_{m3} as 3.8 mS.From equation 2 the total input referred noise of transconductor to the LNA input input comes out to be $2.5*10^{-19}$ V^2/Hz, which is less than the assigned budget of $3*10^{-19}$ V^2/Hz. $V_{n\,LNA}^2$ = $6*10^{-19}$ V^2/Hz $V_{n\,TCA}^2$ = $2.5*10^{-19}$ V^2/Hz $V_{n\,R_s}^2$ = $8*10^{-19}$ V^2/Hz

The total input referred noise of the LNA-Transconductor-antenna is $16.5*10^{-19}$ V^2/Hz.

The same can be also be seen in the below plot of the total input referred noise of LNA-TCA-antenna.

Now, the total noise factor of LNA-Transconductor cascade is ($V_{n\,LNA}^2$ + $V_{n\,R_s}^2$ + $V_{n\,TCA}^2$) /($V_{n\,R_s}^2$) = 2.06 , which is 3.14 db.

Now we understand that, the mixer and TIA must be designed such that they contribute only 1 db to the NF, so that N = 4 db. The Noise Figure plot of the LNA-Transconductor is shown below:

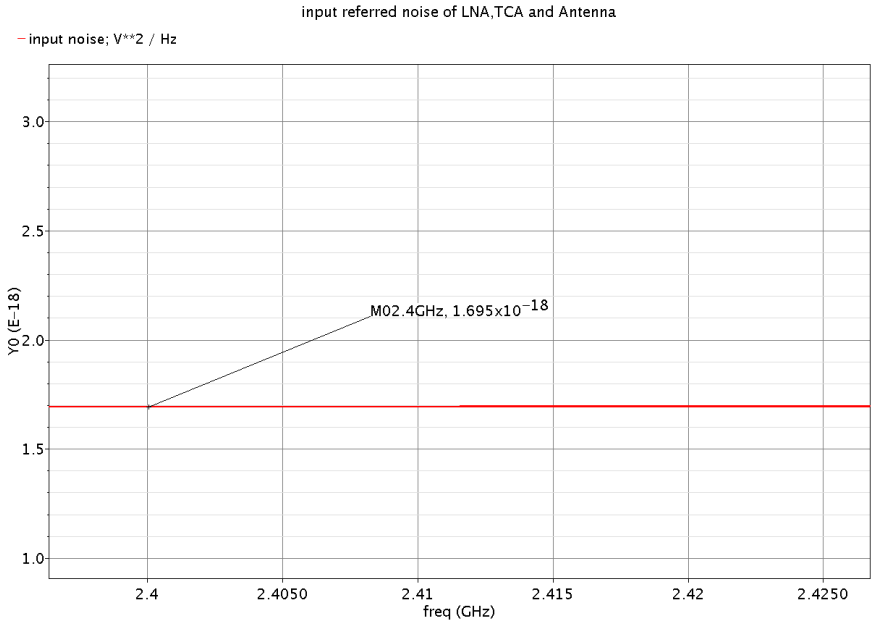

Figure 3.4: Input referred noise voltage PSD of LNA-Transconductor-antenna together

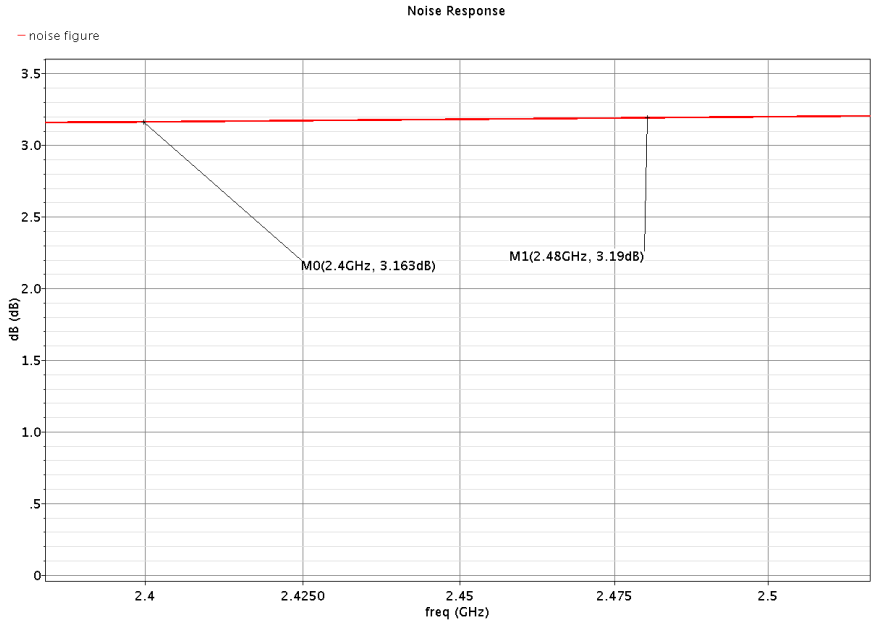

Figure 3.5: Noise figure of LNA-Transconductor cascade

3.2 IIP_3 of Transconductor

As the transconductor is driving the mixer and the TIA, the output impedance of the transonductor is ideally the R_{on} of the switch in the mixer (approximately 10 ohm), the voltage swings at the output of the transconductor are negligible.Therefore, there is no compression faced by the transconductor at it's output.However, there can compression at the input, because it's input is the amplified voltage output of the LNA.Therefore, we have to bother about the maximising the IIP_3 of the TCA.Referring to section 2.4 ,an optimum Gate-source bias voltage is chosen for the input differential pair.The input differential pair is designed with channel length of 60 nm and hence from figure 2.11 ,the optimum point of V_{gs} is at 500 mV, giving a V_{dsat} of 75 mV.

A transconductor is a voltage controlled current source and needs a high output impedance, ideally.So, the output common mode drain voltages of the input differential pair transistors M_1 and M_2 in figure 3.1 is selected as high as possible, such that a minimum headroom of little more than V_{dsat} is maintained for the active PMOS loads.The active PMOS loads are designed with high channel lengths to have a better output resistance.

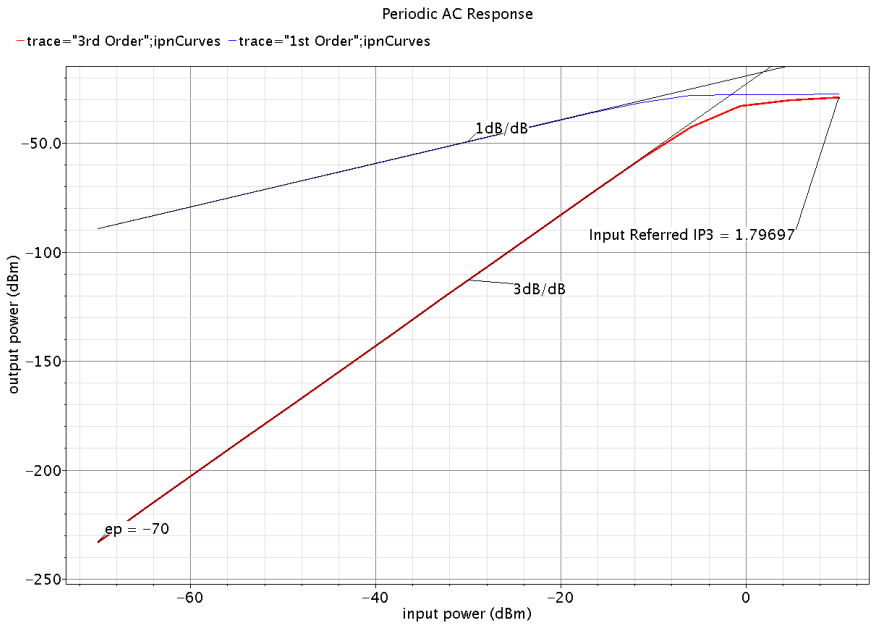

Figure 3.6: IIP_3 of transconductor

In the design the output common drain voltages are set at 800 mv.The output common mode voltages are set using a resistive common mode detector and an op-amp

connected in negative feedback (shown in green colour in figure 3.1). The IIp_3 of the tranconductor is 1.8 dbm and plot for the same is shown below in figure 3.6. The plots for common mode loop gain and phase is shown in figure 3.7 :

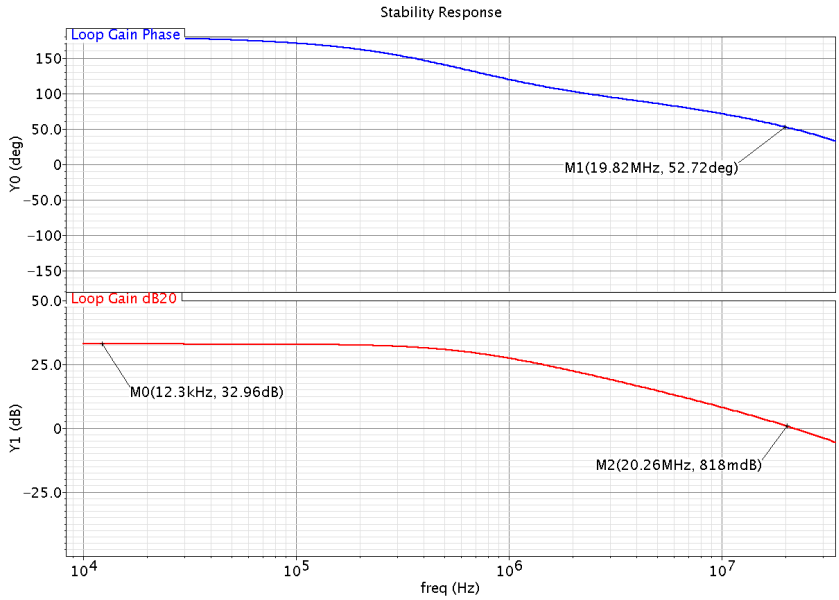

Figure 3.7: Stability of the common mode feedback loop in transconductor

CHAPTER 4

Current mode 25 % duty cycle double balanced passive Mixer

A 25 % duty cycle passive mixer is chosen because of two reasons:

1. To avoid crosstalk between I-path and Q-path.Crosstalk may lead to self corruption of the signal, if it's spectrum is antisymmetric.The crosstalk also leads to an increased noise from the mixer.

2.The Noise figure of a 25 % duty cycle passive mixer is 3db less than the noise figure of a 50 % duty cycle passive mixer.

Both the above points are explained in detail with the help of the diagram below:

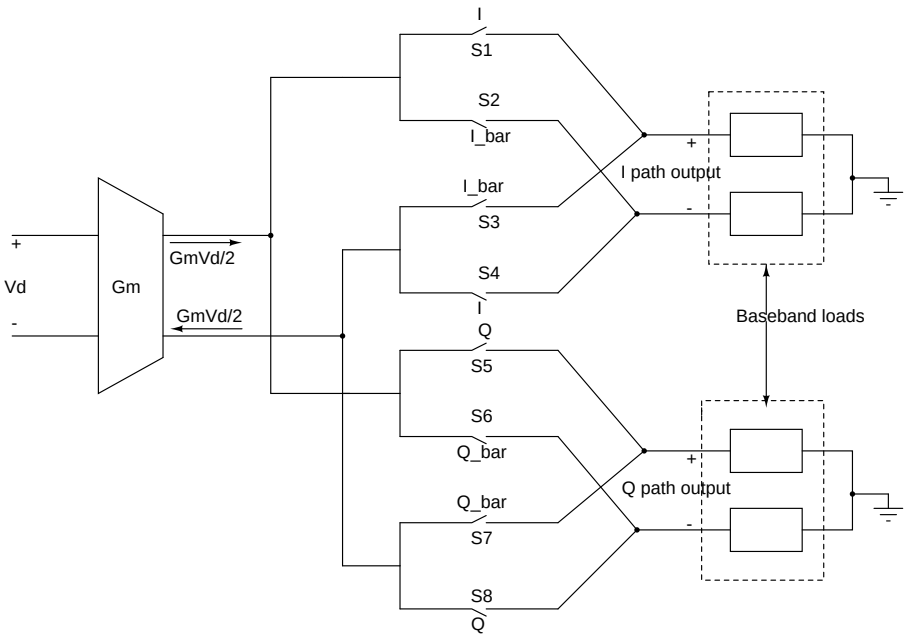

Figure 4.1: A current mode passive mixer

The crosstalk can be identified by knowing which switches are of the I and Q path are simultaneously on during the time period 'T' of the L.O (local oscillator) waveforms.

The figure below shows the in-phase and Quadrature phase waveforms in the case of a 50 % duty cycle passive mixer:

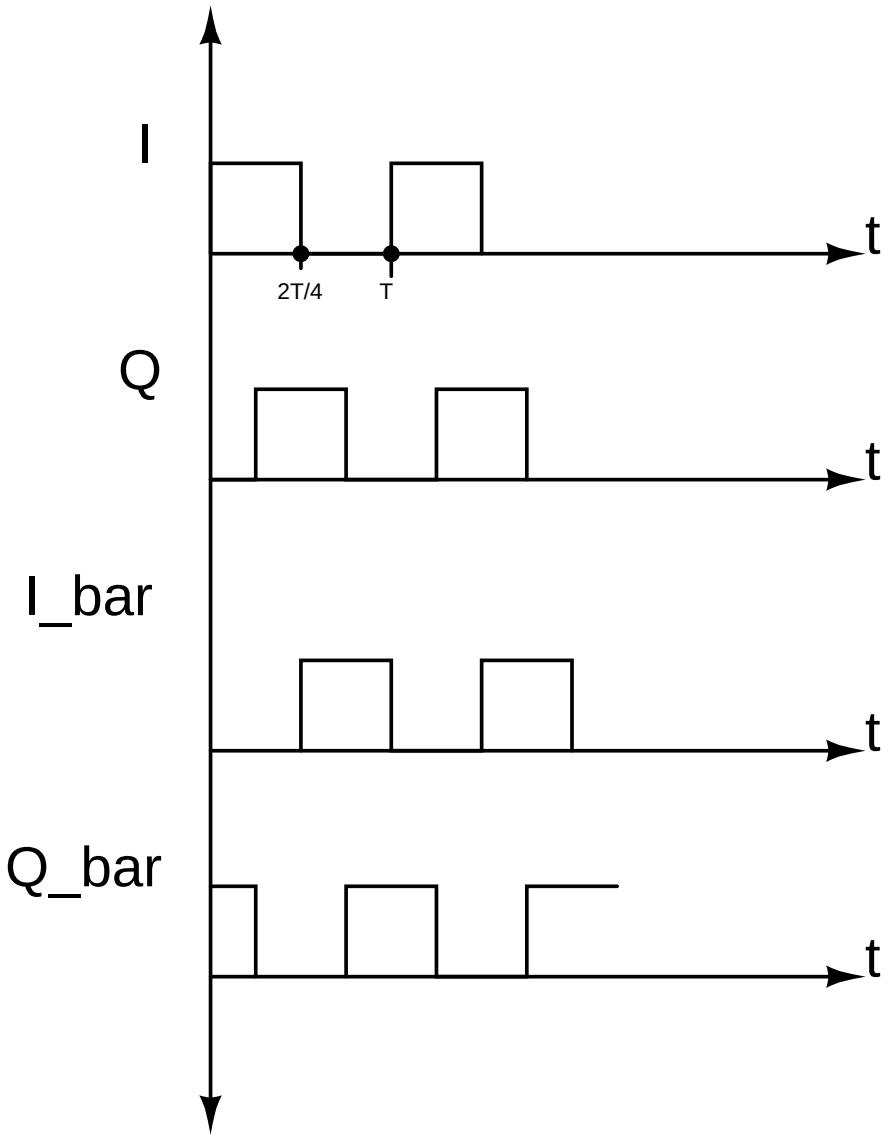

Figure 4.2: 50 % duty cycle I and Q waveforms

During the period 0 < t < T/4 , I and Q_{bar} are on , causing a crosstalk between switches s1,s4 in the I path and s6, s7 in the Q path.During the period T/4 < t < T/2 , I and Q are on , causing a crosstalk between switches s1,s4 in I path and s5, s8 in the Q path.During the period T/2 < t < 3T/4 , I_{bar} and Q are on , causing a crosstalk between switches s2,s3 in I path and s5, s8 in the Q path. Similarly during the period 3T/4 < t < T, I_{bar} and Q_{bar} are on and relevant switches are on.It can be easily observed that in every 1/4 part of the time period 'T' both I and Q paths are ON simultaneously, so the input currents $G_m v_d$/2 and -$G_m v_d$/2 each split equally into I path and Q path 'mixers'

causing only half of the current to be down converted.So, in real only $G_m\ v_d\ /4$ is down converted instead of $G_m v_d/2$ resulting in the half the gain of the mixer in either of the paths i.e $1/\pi$. The above problem of the gain and I-Q crosstalk can be solved if two transconductors are used , one for I path and other for Q path.The drawback here is,the output of the LNA is loaded by double the gate capacitance , reducing nodal bandwidth and hence reducing the gain of the LNA, which increases the noise contributions of all the stages after the LNA. This results in an overall increase in the Noise Figure. The next solution without compromising any increase in the noise figure of the receiver and to avoid I-Q crosstalk is to use a $25\ \%$ duty cycle mixer.The ideal $25\ \%$ duty cycle I,Q waveforms are shown in figure 4.3 As we can see in the waveforms, in $1/4$ of time

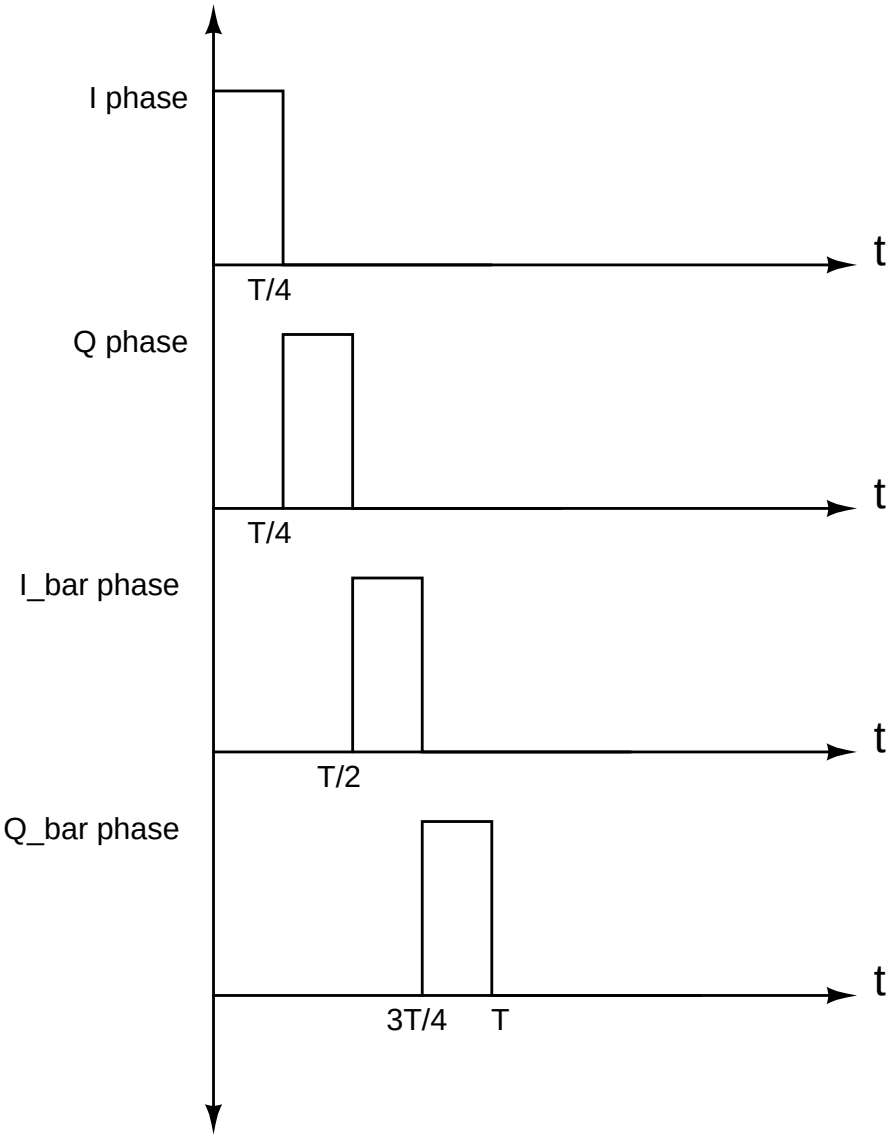

Figure 4.3: $25\ \%$ duty cycle I and Q waveforms

period T, only one of the phase i.e either I or Q or I_{bar} or Q_{bar} is active and hence is

no crosstalk between I and Q paths.Also as either I or Q path is ON in every quarter of a cycle, complete R.F current $G_m\ v_d/2$ is down converted.The current gain of a 25 % duty cycle passive mixer is $\sqrt{2}/\pi$ and it's 3 db higher than the receiver with a 50 % duty cycle passive mixer with a single transconductor.Therefore the stages after the mixer and mixer itself will contribute less to the overall input referred noise at the LNA input.

4.1 Conversion Gain of a 25 % duty cycle passive mixer

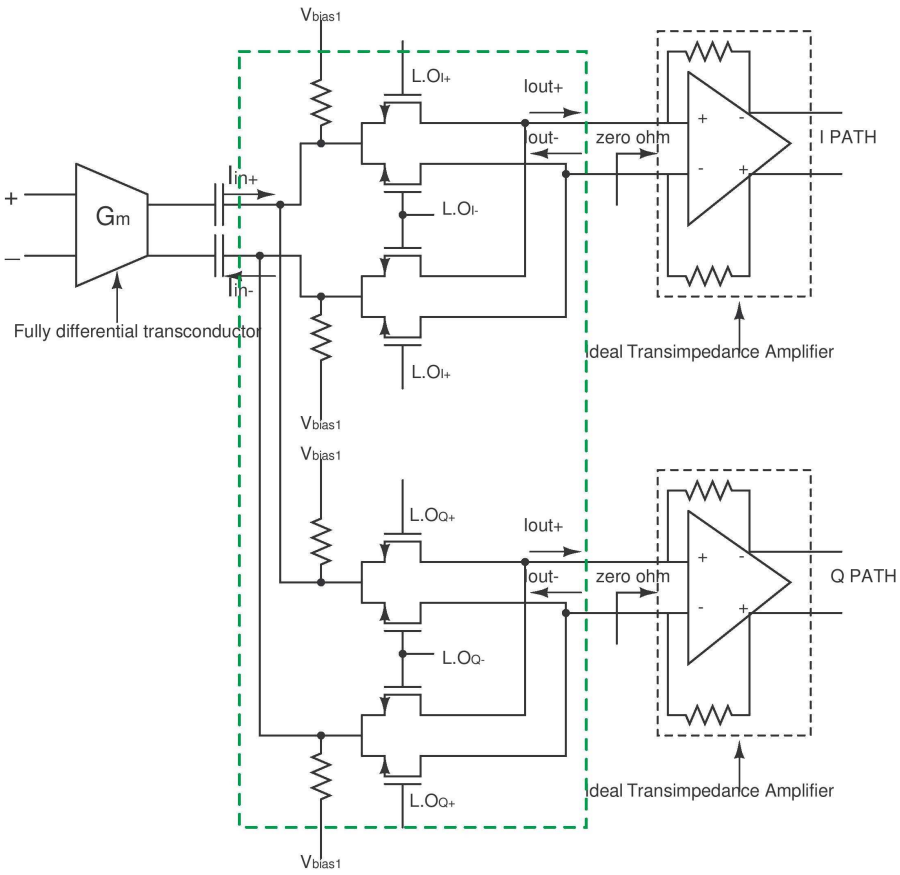

Figure 4.4: Biasing of a passive Mixer

The conversion gain of a double balanced passive mixer is $\sqrt{2}/\pi$,because the magnitude of the fundamental component of a waveform (I - Q) is $2\ \sqrt{2}/\pi$ .On multiplication with an R.F sinusoid the gain becomes $\sqrt{2}/\pi = 0.45$. The figure below (figure 4.4) shows the necessary biasing for a passive mixer.The drain of the mixer is directly coupled to the TIA and hence input common mode voltage of the TIA becomes the drain bias voltage for the switches in the mixer.It is at 600 mV in the design.The source

node of the switches are biased at 600 mV so that it always operates in heavy triode region when ON.As a NMOS switch passes low voltages very easily, the Gates of all the switches are biased above the drain by one Threshold voltage , i.e approximately 600 mV.

Test for the conversion gain of the mixer:

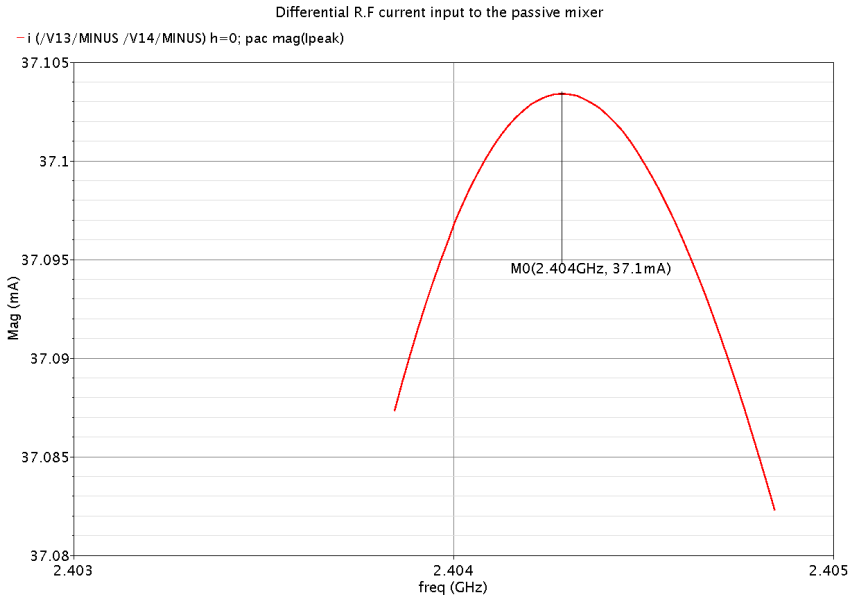

Figure 4.5: Differential R.F current input to the mixer in mA

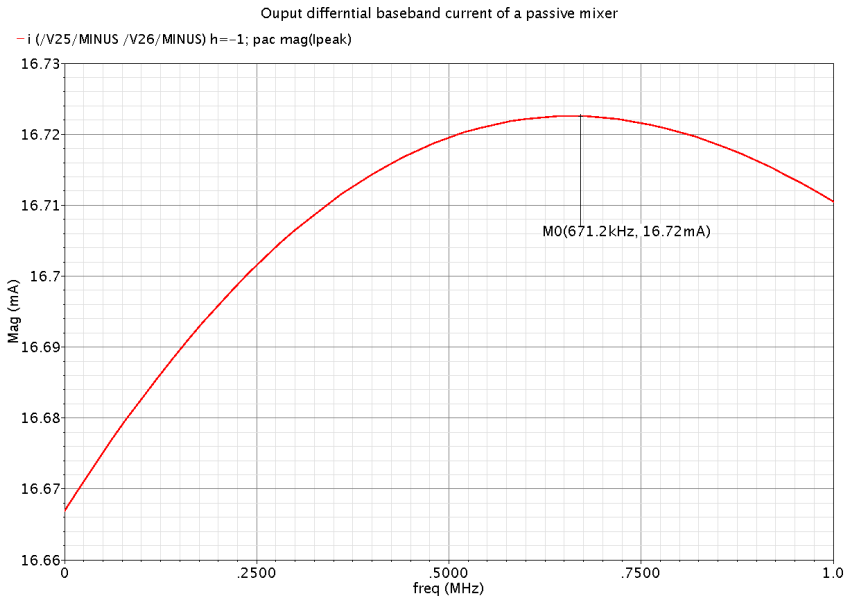

Figure 4.6: Differential Baseband current input to the mixer in mA

To Test the conversion gain of the mixer a 1V input is applied to the LNA, it's output

is 3.55 V(loaded voltage gain of the LNA is 3.55).The differential input R.F current to the mixer is I_{in+}- I_{in-} =1*3.5*11 mS = 38.5 mA.Expected differential output baseband current is I_{out+} - I_{out+}= 0.45 * 38.5 mA = 17.3 mA.The ratio of the currents = 16.72/37.1 = 0.45.The below plots (figure 4.5 and figure 4.6)shows the differential R.F current input to the mixer and output differential baseband current of the mixer

4.2 Noise analysis of a passive mixer by Switched capacitor approach

The noise analysis for a passive mixer is shown with the help of figure 4.7.

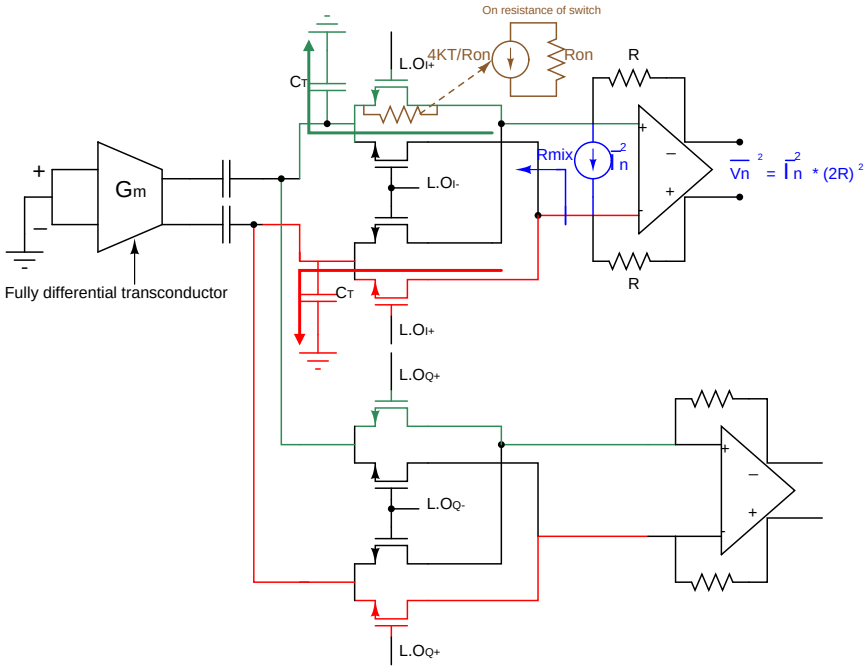

Figure 4.7: Noise analysis in a passive mixer

The thermal noise of a switch with ON resistance of R_{on} is $I_{Ron}{}^2$ =$4kT/\mathrm{R}_{on}$.During the I phase, (switches driven by $L.O_{I+}$ are on)the nodal capacitors C_T are charged with the noise current PSD of the ON resistances of the two switches.The charging process is shown by green and red arrows for the two capacitors C_T.During the Q phase, (switches driven by $L.O_{Q+}$ are on)the capacitors discharge through the ON switches in the Q path into the virtual ground nodes of the TIA.A capacitor C_T charged by an I phase switch and discharged through a Q phase switch gives an equivalent resistance of

$\frac{1}{f_0 C_T}$, according to switched capacitor analysis looking into the single output node of Q path mixer.Since, there are two charge and discharge process going on simultaneously, the equivalent output resistance of the mixer in I or Q path is $\frac{2}{f_0 C_T}$ .This process of charge and discharge of nodal capacitor C_T leads to the noise contribution by the passive mixer.The amount of noise charge deposited on the capacitors is proportional to the R_{on} C_T time constant.So, if C_T is higher then the amount of noise charged sampled by the switches is higher and hence a higher noise contribution from the mixer.

The switched capacitor output resistance(for the I or Q mixer) R_{mix} = $\frac{2}{f_0 C_T}$ is shown in blue colour in figure 4.7.The current noise PSD due to R_{mix} is I_n^2 = 4kT/R_{mix}.Thus, the output voltage squared noise PSD in the I path(or Q path) is V_n^2 = I_n^2 $(2R)^2$.

In our design the noise due the mixer is tracked by hand calculations , with the help of the switched capacitor analysis.

The hand calculation tracking is done as follows:

1. What is the value of C_T? The below figure shows, how to calculate the value of C_T.

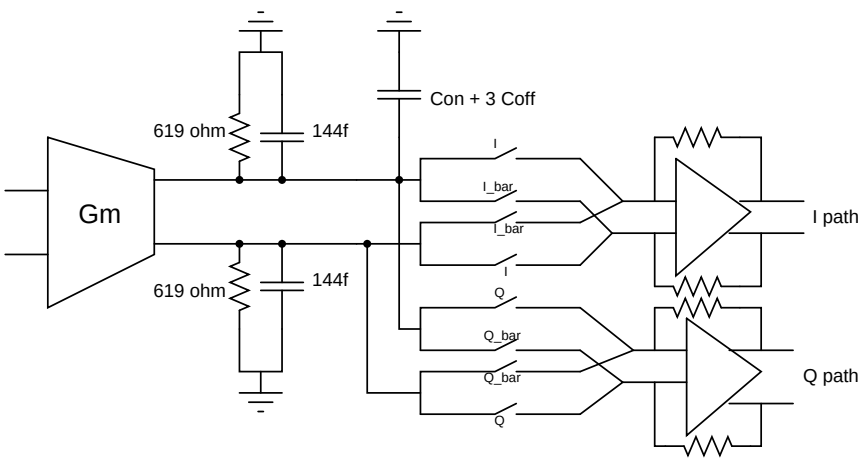

Figure 4.8: Estimating the value of capacitor C_T

The switches are sized such that with a gate swing of 600 mV to 1.8 V(the L.O swing is 1.2 V but the gate is biased at 600 mV), the on resistance of the switch is at 10 ohm.The W/L of a switch is selected as 62.5 u/60 nm.Each output node of the TCA is connected to four switches, and as only one of the switch is ON in a time period of the L.O, the total capacitance contributed by the mixer at each node is given as C_{on} + C_{off}.In the design, C_{on} = 63.5 fF and C_{off} =25.6 fF.A total of 140.3 fF

is contributed by mixer to each output node of the TCA.Thus, C_T = 144 + 140.3 = 284.3 fF. R_{mix} = $\frac{2}{f_0 C_T}$ = 2924 ohm.The current noise PSD of R_{mix} is referred to the LNA as $\frac{4kT/R_{mix}}{(gainofLNA)^2 G_m^2 (gainofmixer)^2}$ which is $\frac{4kT/R_{mix}}{16*11mS^2*0.45^2}$= 1.375 * 10^{-20} V^2/Hz per switch.For four switches, it is 4 times and hence the input referred noise voltage at the input LNA due to the I path is 5.5 * 10^{-20} V^2/Hz.According to the noise summary in the pnoise analysis, the contribution due to the mixer is 6 * 10^{-20} V^2/Hz, which is approximately equal to the hand calculated result.

4.3 25 % duty cycle L.O Generator

An ideal clock of double the required frequency is assumed to available, and a divide by two circuit is used to generate the 2.4 Ghz in phase and quadrature L.O signals.

The circuit used is shown below:

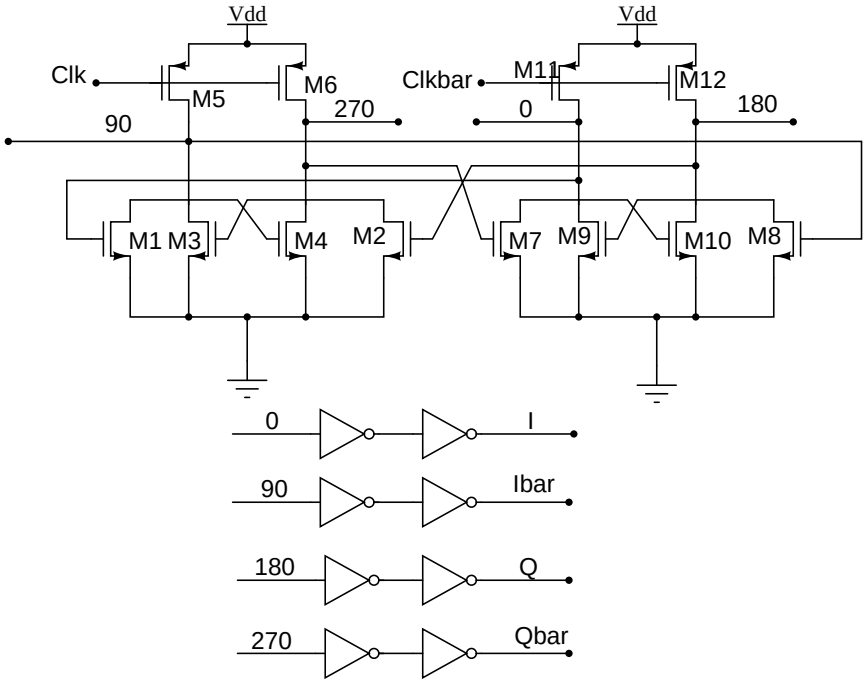

Figure 4.9: Divide by two ciruit

Transistors M1 to M6 constitute the master latch and transistors M7 to M12 constitute the slave latch. Each latch has two sense devices M1 and M2 in the master and M7,M8 in the slave,Regenerative loop (M3,M4 in master and M9,M10 in the slave) and two pull up devices (M5,M6 in the master and M11,M12 in the slave).

The I,Q waveforms generated after smoothing with the help of the buffers are shown below:

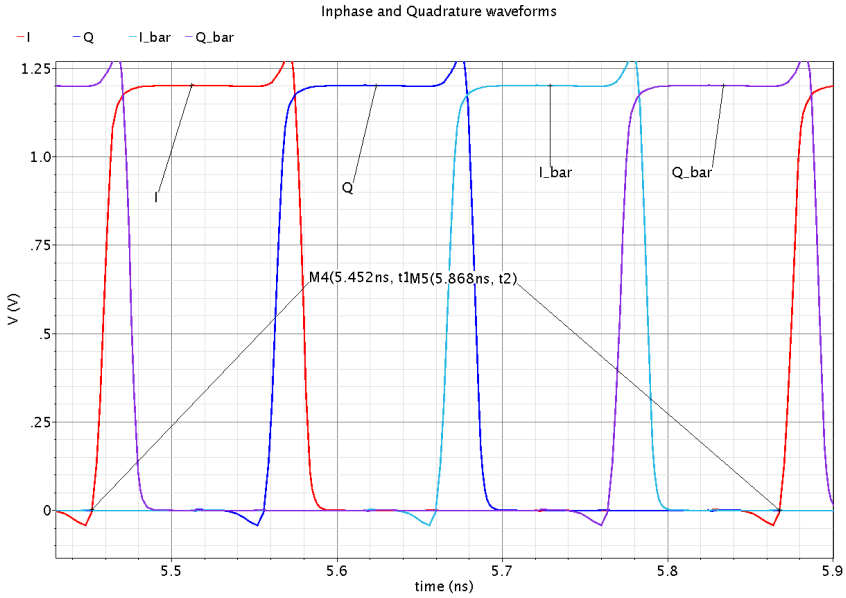

Figure 4.10: 25 % duty cycle I,Q waveforms

CHAPTER 5

Transimpedance amplifier(TIA)

The TIA takes in the downconverted baseband currents and generates baseband voltage.There are two TIA's one each for I , Q phase.A first order low pass filter is implemented with the transresistance of 1 Kohm. TIA is designed using a 2 stage opamp(figure 5.2) Design of the g_m of the input differential pair(figure 5.3): The specification on the g_m is kept by it's input referred noise at the corner frequency.The most important aspect of design of TIA design is flicker noise,as the mixer is dc coupled with the mixer and any flicker noise of the input differential pair is upconverted to R.F frequency range by the mixer and contributes to NF at the LNA input. Specification on the input referred noise of the OPAMP is derived as follows(figure 5.3): $\mathrm{I}_n^2 = \frac{V_n^2}{(R_{mix}/2)^2}$,$\mathrm{R}_{mix}$ = 2924 ohm. I_n^2 when referred to the input of LNA is, $\frac{I_n^2}{(A_lna*g_m*0.45)^2}$< $2.5 * 10^{-19}$, which is the noise budget for the TIA.

By completing the calculatiions we get V_n^2 « $8 * 10^{-17}$. The input referred voltage noise PSD of a differential input pair ignoring the Noise PSD due to active loads, is $\frac{(8kT\gamma)}{g_m}$ which is $2 * V_n^2$ .Accordingly, it is required , that g_m should be more than 138 uS.But, flicker noise corner at this value of g_m is more than 1 Mhz, which will drown out the complete bluetooth signal.With the help of simulationsm it is seen that if the g_m is set to 38 mSThe current density in the input diff pair is selected to have maximum dc gain.Also ,as flicker noise is a concern, the channel length is selected to be 1um.A 1u channel length device gives a maximum dc gain of 100 , when biased at a Vdsat of 70 mV. However, the g_m kept for the input diff pair is kept at 38mS.The unity loop gain frequency of the OPAMP is selected to much larger than the channel bandwidth of 1 Mhz, as the TIA must present an input impedance of ideally 0 ohm for 1 Mhz.

Following are the plots for the OPAMP, its dc gain and stability, and stability of the two common mode feedback loops.

Plot for DC gain(figure 5.4):

Plot for Stability of Common mode feedback loop 1(CMFB1) shown in figure 5.5

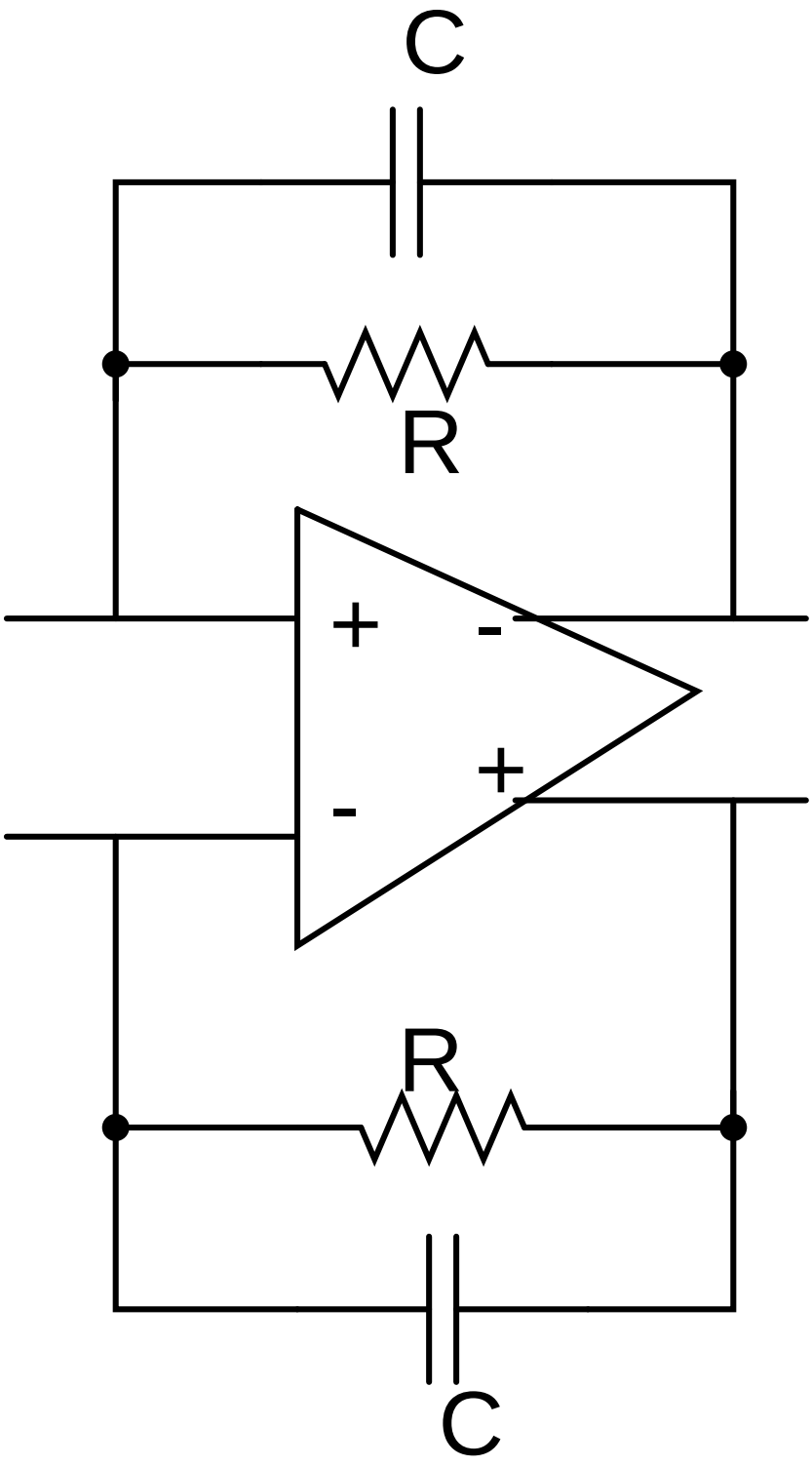

Figure 5.1: TIA:Opamp with a first order low pass filter

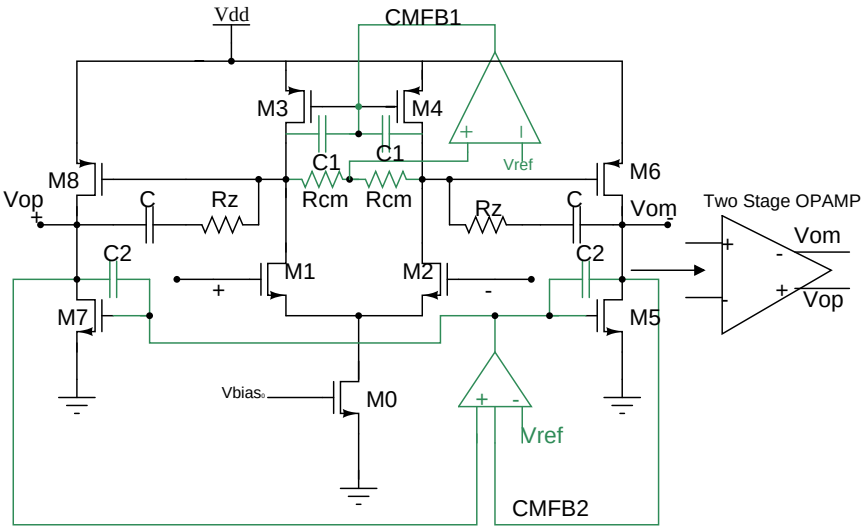

Figure 5.2: Two Stage OPAMP

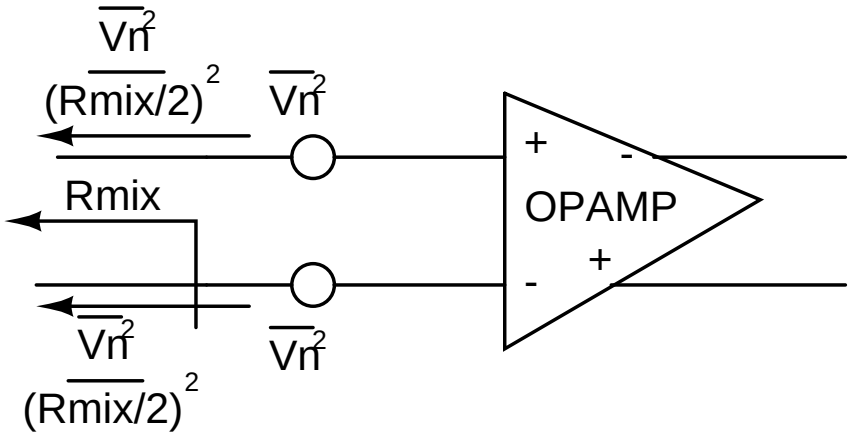

Figure 5.3: Specification on input referred noise of opamp

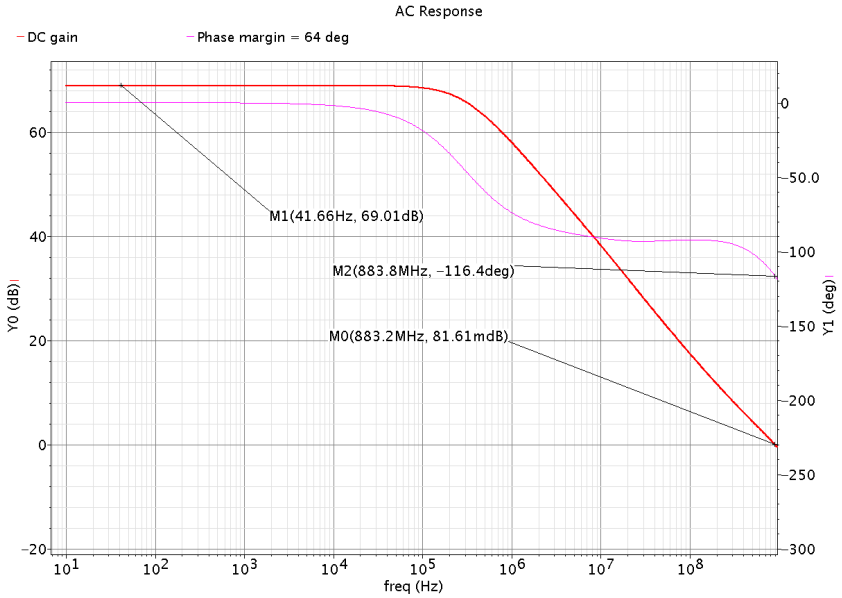

Figure 5.4: DC gain of the opamp

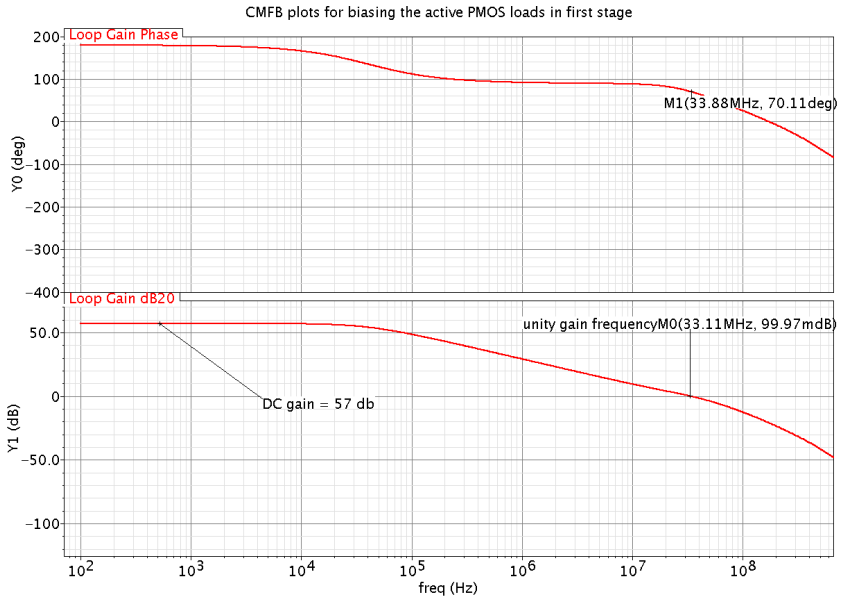

Figure 5.5: Stability of CMFB1

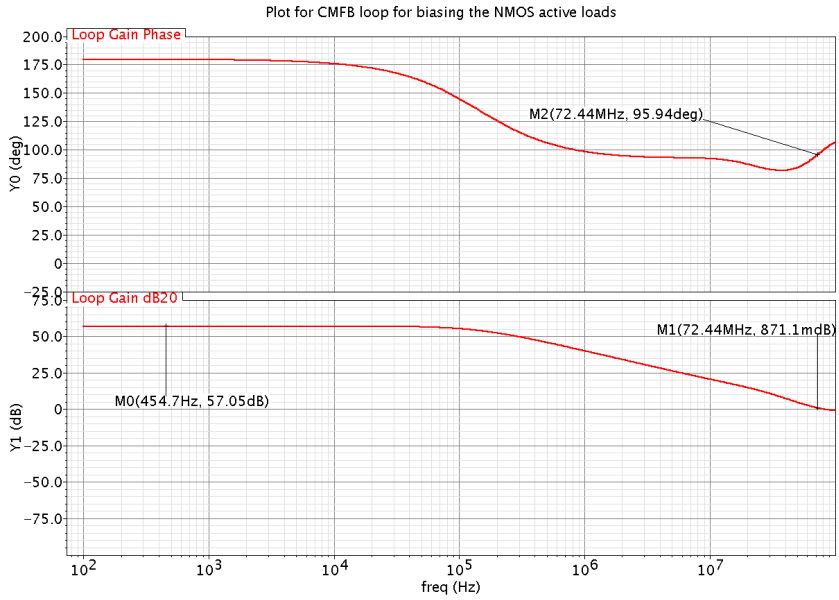

Figure 5.6: Stability of CMFB2

Plot for Stability of Common mode feedback loop 2(CMFB2) shown in figure 5.6

A transresistance of 1Kohm is chosen(not more), as the DC gain is 2800, and the input resistance of the TIA is 1Kohm/2800. The cutoff frequency of the low pass filter can't be selected at 1Mhz, as the droop will be 3db then.Hence , a cutoff of 2.5 Mhz is selected, which demands a parallel capacitor of 63.6 pF.

CHAPTER 6

Results of the complete Receiver Chain

6.1 Voltage Gain,Noise Figure and IIP3

1. Voltage Gain of the Receiver Chain: The voltage Gain of the LNA(loaded by the TCA is 3.55 instead of 4), followed by transconductance g_m = 11mS, followed by a mixer with a current conversion Gain =0.45 and a TIA with transresistance = 1K ohm. So the Voltage Gain is (3.55 * 11mS * 0.45 * 1000 = 17.5 = 24.8 db. The voltage Gain of 24.8 db for the receiver is shown in the figure below:

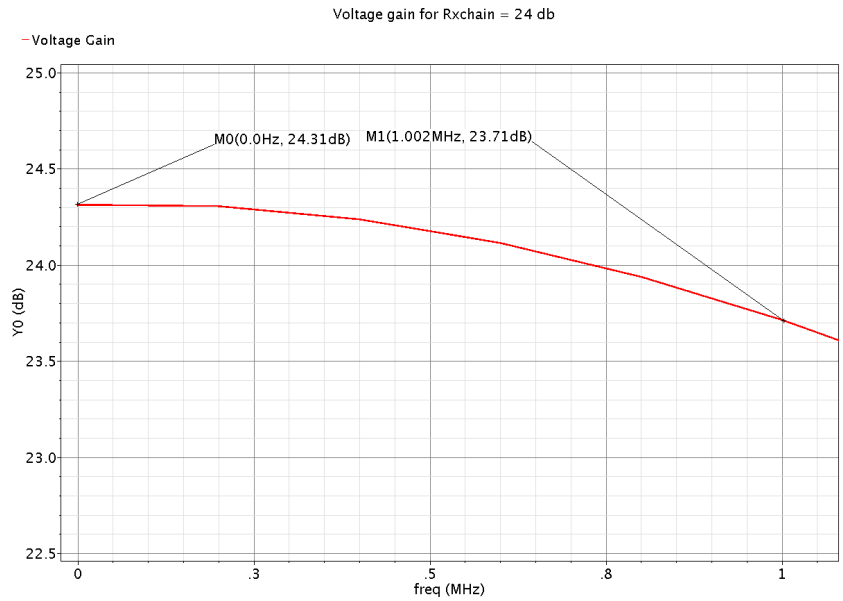

Figure 6.1: Voltage Gain of the receiver

2. Noise Figure of the Receiver : The integrated Noise figure of the receiver from a corner frequency of 10 Khz to 1 Mhz is 4db. Table (6.1)representing noise contributions of different blocks in the receiver is shown below:

The plot for the Noise Figure is shown below:

The IIP_3 of the RX chain is -10.3 db.This result is evident because, the gain of the LNA is 11.5 db(LNA loaded) and the IIP_3 ofthe TCA as shown in chapter on TCA is

Table 6.1: The left coloumn shows the block name and right coloumn shows their percentage contribution to Noise Figure

$Nameoftheblock$	$NFpercentagecontribution$
Antenna	40
Low Noise Amplifier	29
Fully Differential transconductor	14
Mixer	9
Transimpedance Amplifier	5

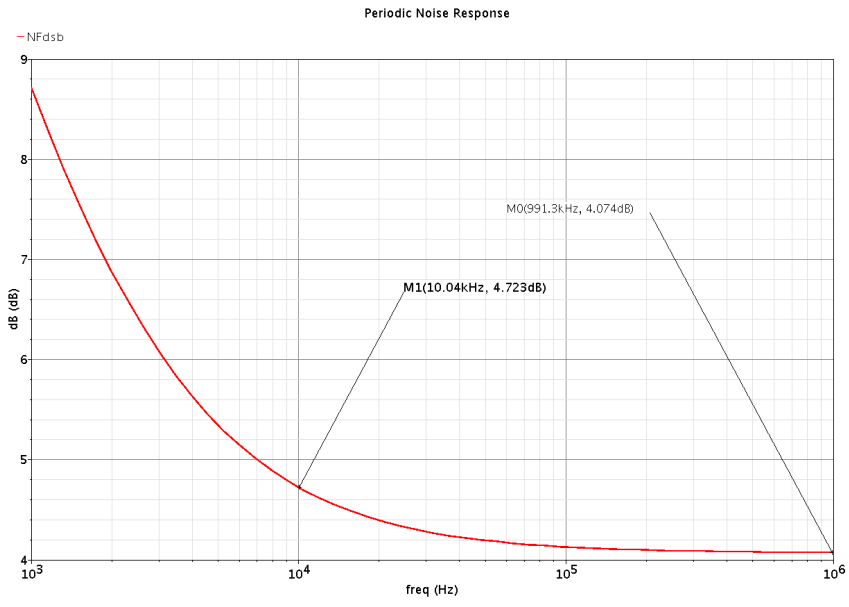

Figure 6.2: Noise Figure of the receiver

approximately $+2$ dbm.So,the overall IIP_3 of the Chain has to be less than $(2-11.5)$ = -9.5 dbm.And the IIP_3 of the chain is -10.3 dbm.The plot for IIP_3 is shown below. Also, an interesting point can be absorbed from this result, i.e the passive mixer and

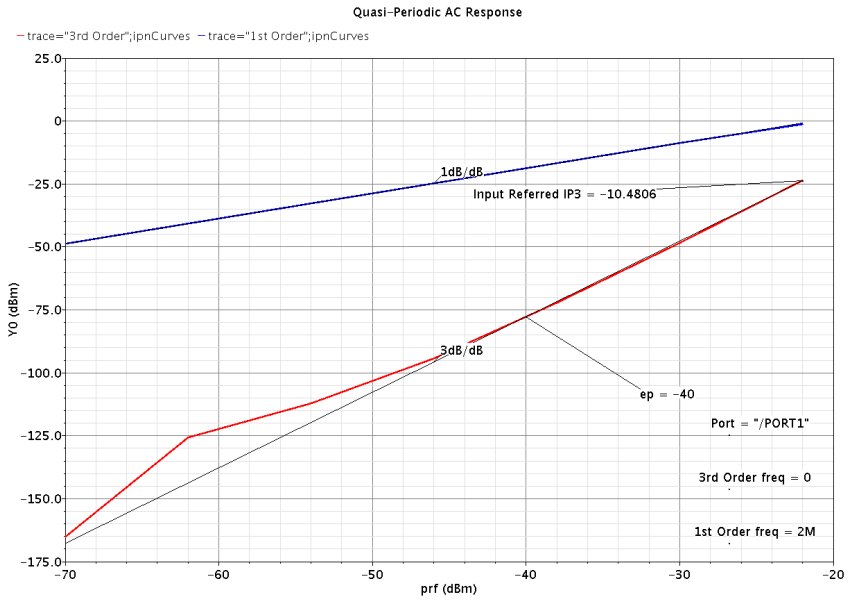

Figure 6.3: IIP_3 of the receiver

the TIA hardly undergo any compression.This shows that a current mode architecture is best suited to obtain good IIP_3 or a good linearity. Also,the 1-db compression point according to the relation between IIP_3 and the 1-db compression point, i.e P1-db = IIP_3 - 9.6 db, is -19.6 dbm.The P1-db , can also be understood intuitively as: The transistors in the 2nd stage in the two stage opamp,are designed to have a V_{dsat} of, 100 mV. The output common mode is set at 600 mV, therefore allowable output signal swing is V_{dd} - V_{dsat} = 600 mV - 100 mV = 500 mV.When referred back to the input of the LNA, corresponding input signal is 500 mV/16 = 31.2 mV = -20 dbm.After -20 dbm of input, there is voltage compression at the output as the transistors in the output stage go from saturation to triode region,so it makes sense to say that P1 db point of the receiver is at -20 dbm.

6.2 Voltage Gain,Noise Figure and IIP_3 across process corners

The plot of Voltage Gain across process corners is shown below in figure 6.4 and 6.5

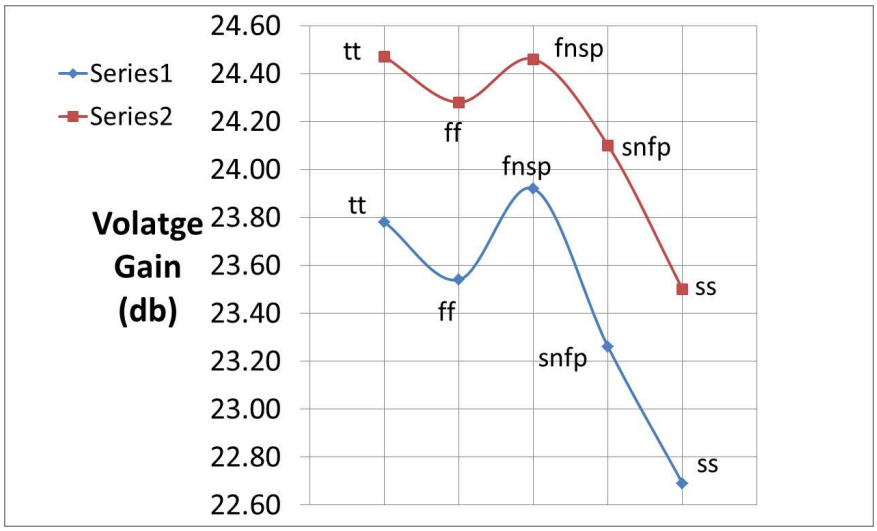

Figure 6.4: Voltage gain across process corners

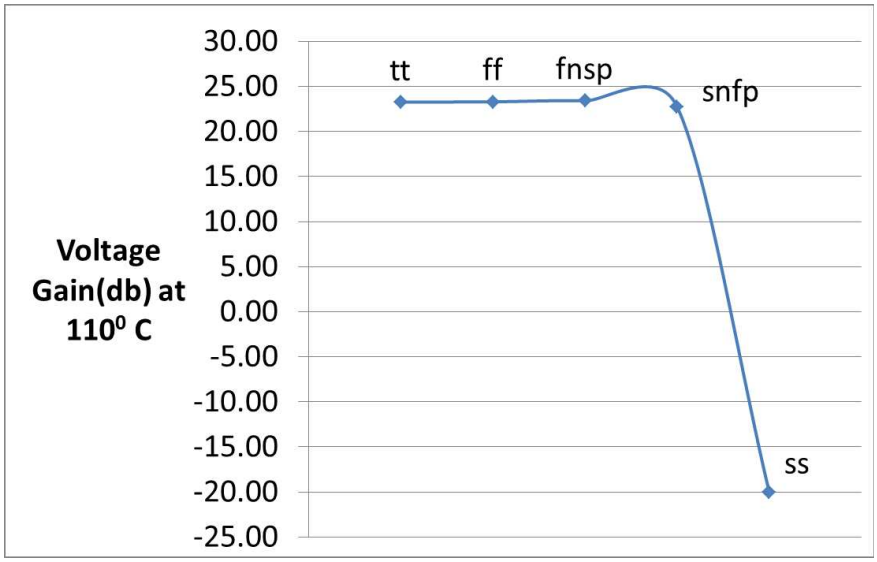

Figure 6.5: Voltage gain across process corners

The plot of Noise figure across process corners is shown below in figure 6.6 and 6.7

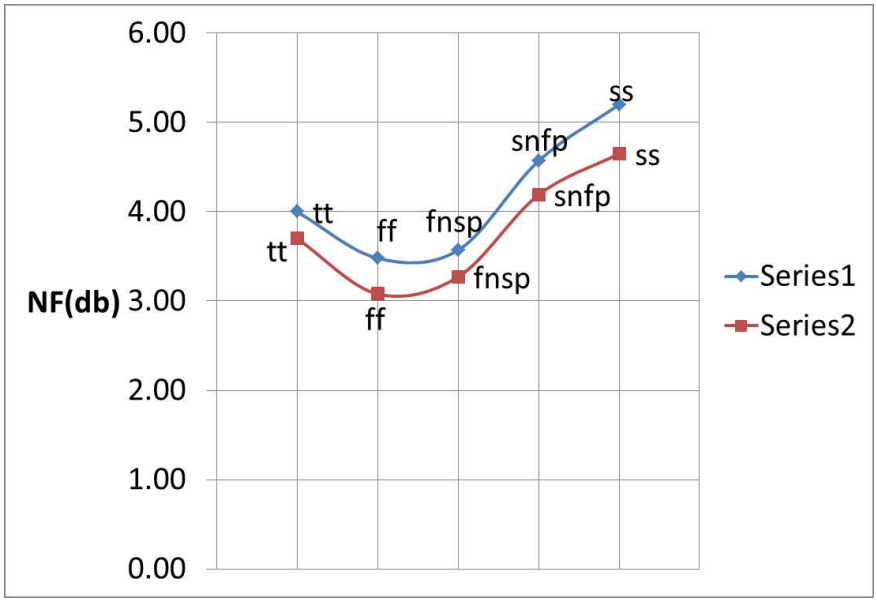

Figure 6.6: NF across process corners

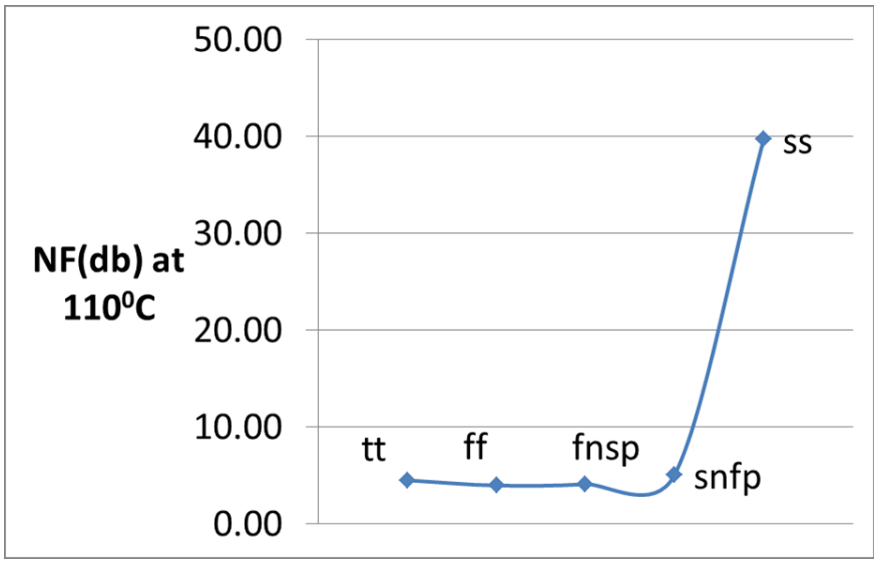

Figure 6.7: NF across process corners

The plot of IIP_3 across process corner is shown below in figure 6.8:

6.3 Results Summary

The results summary is given below for each block in tabular form.

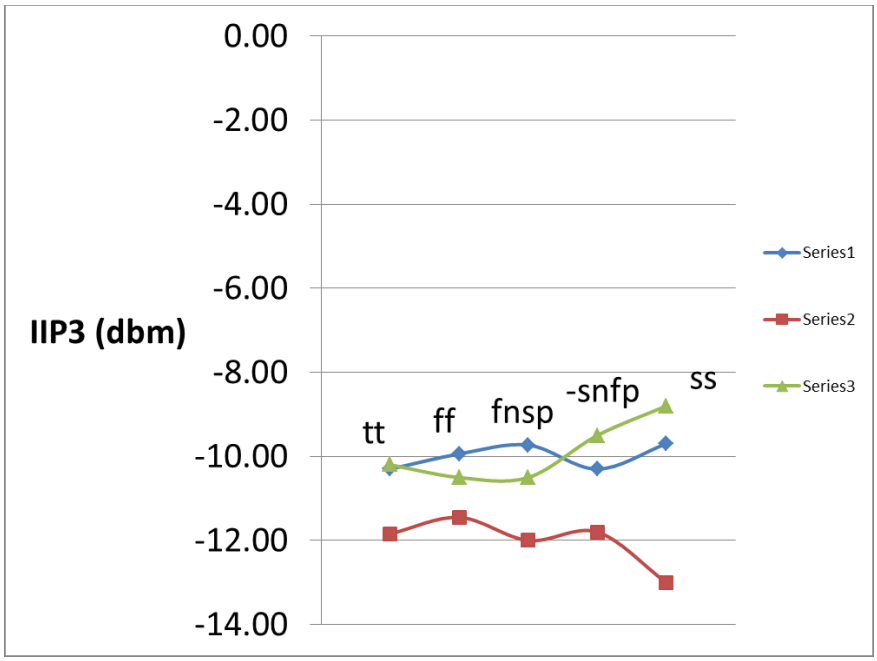

Figure 6.8: IIP_3 across process corners

Table 6.2: Summary of LNA

Characteristic	*Value*
$S11$	-10.74 db
Voltage Gain(unloaded)	12 db
NF	2.4 db
IIP_3	5.4 dbm
Power consumption(V_{dd} =1.2 V)	8.8 mW

Table 6.3: Summary of TCA

Characteristic	*Value*
Transconductance	$11mS$
NF	12 db
Output impedance	619 ohm with a parallel capacitor of 144fF
Power consumption(V_{dd} =1.2 V)	1.92 mW

Table 6.4: Summary of Mixer

Characteristic	*Value*
Conversion Gain	0.45
On resistance of the switch	10 ohm
Contribution to capacitance C_T	140 fF
Power consumption(V_{dd} =1.2 V)	0

Table 6.5: Summary of TIA

$Characteristic$	$Value$
Transimpedance	1 kohm ‖ 66 pF
Unity Gain frequency	400 Mhz
Unity loop Gain frequency	133 Mhz
Power consumption(V_{dd} =1.2 V)	9.6 mW(I+Q)

6.4 Comparison with recent work on Bluetooth

Characteristic	This work	IEEEJSSC[3]	IEEEJSSC[9]	ISSCC[8]
Sensitivity(dbm)	-96	-95.5	-91	-88
Current(mA)	17(high gain)	35	21	29.7
S11(db)	-10.8	-20	-	-
Inductors used in LNA	No	Input Balun used	Yes	Yes
Dynamic range	-96 to -14 dbm	-95.5 to -4 dbm	-	-
IIP_3(dbm)	-10.3	>20	-	-
Technology(nm)	65	110	65	130
V_{dd}(V)	1.2	1.5	1.2	12

Comments on Spec for ADC: Minimum input to ADC = 120 uV.Maximum input to ADC = 420 mV. If the ADC is having 14 bits of resolution or higher then ,it can recognize an input of $(1.2/214)$ = 74 uV.Therefore,need an ADC with D.R of (-96 to -14 dbm)= 82 db.

CHAPTER 7

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