Design of a High Precision Temperature Sensor

A THESIS

submitted by

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THESIS CERTIFICATE

This is to certify that the thesis titled **Design of a High Precision Temperature Sensor** , submitted by **Ajmal V K**, to the Indian Institute of Technology, Madras, for the award of the degree of **Master of Technology** , is a bona fide record of the work done by him under our supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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This thesis is dedicated to my parents, my sisters and to all my loved ones.

ABSTRACT

This thesis presents the design of a high precision temperature sensor. BJT-Core , β- independent bias generator and delta sigma modulator are the important blocks of the system. 16 bit incremental delta sigma modulator is used to convert the temperature variations to digital value. The offset cancellation techniques such as correlated double sampling and chopping are used to achieve the high precision. Dynamic element matching is used to get good matching between the component which results in high accuracy. The spread in the base emitter voltage is trimmed by using a digital delta sigma modulator. The substrate PNP transistor is used to get temperature dependent voltage which is converted to temperature reading.

The design goal is to achieve an accuracy of 0.1^0C from -55^0C to 125^0C.The conversion time is 100ms. The sensor is implemented in UMC 180nm technology.

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ABBREVIATIONS

BJT	Bipolar Junction Transistor
PTAT	Propotional To Absolute Temperature
DEM	Dynamic Element Matching
SNR	Signal to Noise Ratio
DSM	Delta Sigma Modulator
DAC	Digital to Analog Converter
ADC	Analog to Digital Converter
INL	Integral Non Linearity
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
NMOS	N-type Metal-Oxide-Semiconductor
PMOS	P-type Metal-Oxide-Semiconductor
CMOS	Complementary Metal-Oxide-Semiconductor
UMC	United Microelectronics Corporation
OTA	Operational Trans-conductor Amplifier
NTF	Noise Transfer Function
STF	Signal Transfer Function
OBG	Out of Band Gain
UGB	Unity Gain Bandwidth

CHAPTER 1

Introduction

1.1 Motivation

The temperature sensors are widely used in many applications, ranging from instrumentation to household appliances. The low cost of production and high accuracy in sensor output are the typical features demanded by these applications. Compared to conventional temperature sensors, CMOS temperature sensors are smarter and have better cost advantage. The digital output data from CMOS temperature sensors is directly interfaced with a microprocessor. The temperature sensor fabricated in IC technology can be combined with other electronic components on a single chip to build special application systems. Although, it has several distinct features, the limited accuracy in the output is its drawback. These temperature sensors are produced in standard CMOS technology and the temperature errors are typically calibrated and corrected at one temperature to meet the low cost of production. This accounts for the low accuracy of these sensors. The improvements in sensor design and the calibration procedure are implemented to overcome the drawback , maintaining its cost advantage and other features.

CMOS temperature sensors have been a part of academic and industrial research for more than two decades. Several techniques have been introduced to improve the acuracy of the sensor. Thermal management in home and personal appliances had become a major area of concern for the past few years. The equipments with microprocessors need efficient temperature sensing mechanism to track the processor's temperature and regulate it accordingly.

1.2 Design Objective

The main objective of this work is to design a High precision CMOS temperature sensor with accuracy of $+/- 0.1^0C$ over the temperature range of -55^0C to 125^0C.

1.3 Basic design principles

The basic principle of the temperature sensor is to convert the temperature variations into an analog signal of voltage, current or any temperature dependent parameter. This analog signal will be converted into digital representation by an Analog to Digital converter circuitry in the temperature sensor. The digital representation of the temperature requires a reference signal which is used to compare the temperature dependent analog signal. This type of measuring method is known as ratiometric temperature measurement.

Bipolar Junction Transistor (BJT) is a good choice to get temperature dependent voltage signal and temperature independent reference signal. The thermal voltage $\frac{kT}{q}$ and the silicon bandgap voltage V_{g0} can be employed for the ratiometric measurement in temperature sensors. The thermal voltage generates a voltage V_{PTAT} that is proportional to the absolute temperature ($PTAT$) and the bandgap voltage generates the temperature independent reference voltage $VREF$[1]. An Analog to Digital Converter is implemented in the sensor system to convert the ratio of these signals into its digital representation.

The temperature dependent voltage is generated by the difference in the base emitter voltages of two substrate pnp transistors which is biased at different current densities (1:p). As the temperature increases,the base emitter voltage of the transistor decreases at a rate of 2mV/K. The base emitter voltage is equal to the silicon bandgap voltage when extrapolated to 0K. A factor $\alpha\Delta V_{BE}$ is added to the absolute base emitter voltage to compensate for its decrease with temperature

and thus resulting in a temperature independent reference voltage $VREF$.

1.4 Design requirements

The accuracy of the temperature sensor depends on the accuracy of the temperature characteristics of the bipolar transistor. The design should take care of transistor non linearities to not cause significant temperature errors. Essentially, the temperature error resulting from the inaccuracy of V_{BE} alone should be with in $\pm 0.1^0 C$. The design of the CMOS temperature sensor has two important milestones, the first one is the design of a bias current generator circuit for the bipolar transistors which is tuned to operate in a region well suited for accurate temperature sensing and the second one is the design of Analog to digital converter which coverts the voltages to desired temperature reading. Sigma Delta ADC's are used in the design which gives the best results for accurate temperature measurements.

1.5 Thesis organisation

The rest of the thesis is organized as described below.

Chapter 2 discusses the measurement principle of the temperature system and the complete system overview

Chapter 3 discusses the design of BJT core and the principle behind the generation of reference voltage and temperature dependent voltage in detail

Chapter 4 deals with the design of the bias generator circuit for BJT

Chapter 5 deals with the design of Delta Sigma Modulator

Chapter 6 summarizes the integration and layout of different blocks in the sensor

CHAPTER 2

Sensor System and Measurement

2.1 Measurment Principle

The base emitter voltage V_{BE} of a BJT is given by

$$V_{BE} = \frac{kT}{q} \ln(\frac{I_C}{I_S}) \tag{2.1}$$

where k is Boltzmann's constant, q is the electron charge, I_S is the transistor's saturation current, T is the absolute temperature and I_C is collector current of the BJT. The saturation current of the BJT has strong temperature dependency and the temperature coefficient of the base emitter voltage is negative. From equation (2.1) it is evident that, the difference between two BJTs base emitter voltages that carry 1:p current is proportional to temperature and this value is given by

$$\Delta V_{BE} = \frac{kT}{q} \ln(p) \tag{2.2}$$

From equation (2.2), ΔV_{BE} is directly proportional to temperature. ΔV_{BE} can be digitized with respect to a reference voltage to get the temperature measurement. The bandgap reference voltage is a temperature independent voltage. This voltage is generated by adding $\alpha \Delta V_{BE}$ and V_{BE}.

$$V_{REF} = V_{BE} + \alpha \Delta V_{BE} \tag{2.3}$$

α and p are chosen as 12 and 6 respectively to get temperature coefficient of V_{REF} as zero around room temperature. An ADC converts $\alpha \Delta V_{BE}$ to a digital value with reference to V_{REF} which can be used for temperature measurement. The

digital temperature reading D_{out} can be expressed as

$$D_{out} = A.\frac{\alpha \Delta V_{BE}}{V_{REF}} + B \tag{2.4}$$

A and B are constants and D_{out} is in degree Celsius. A and B can be found by minimum meansqaure linear fitting of $\frac{\alpha \Delta V_{BE}}{V_{REF}}$ and temperature measurement. For UMC 180nm technology substrate pnp transistor, A≃ 665.33 and B≃ -277.77.

2.2 System Overview

The block diagram of the temperature sensor system is as shown Figure.2.1. The BJT-Core is giving input to DSM depending on the value of *bs*. The DSM is integrating V_{BE} or ΔV_{BE} and giving the output bit-stream *bs*. The average value of bit-stream is found by low-pass filtering the bitstream using decimation filter. The average value is equal to $\frac{\alpha \Delta V_{BE}}{V_{REF}}$ which is used to get digital temperature output as given by expression(2.4). Biasing of BJT Core is done using special bias circuit.

The incremental ΣΔADC is a good choice for the sensor application. The signal

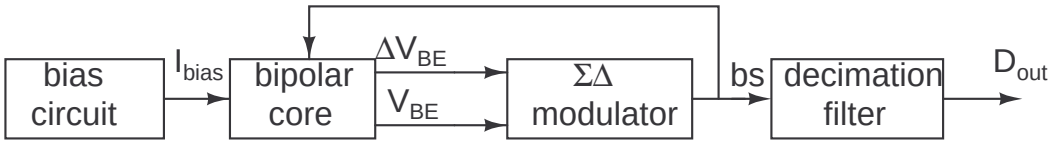


Figure 2.1: Block diagram of the sensor.

in the sensor application is low frequency and the required resolution is high. This makes the incremental ΣΔADC a proper choice for this particular application

2.2.1 Temperature Reading Technique

The output of temperature sensor is in digital format. To get the digital output, we need to convert analog input to digital output using a ADC. The incremental delta

sigma ADC (Charge balancing converter) is well suited in this scenario since it requires very small signal frequency and high ADC resolution. The ADC converts ΔV_{BE} and V_{BE} value to digital temperature reading. The block diagram of an incremental DSM is as shown in Figure.2.2. The loop integrates V_{IN} or $V_{IN} - V_{REF}$

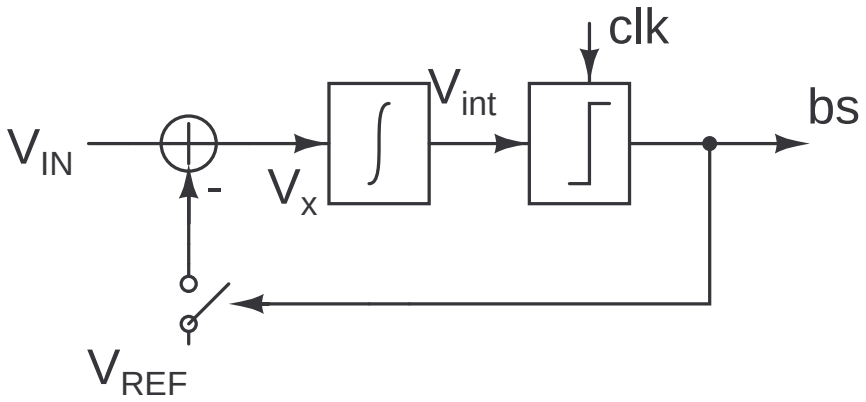


Figure 2.2: Block diagram of incremental DSM.

and if the comparator input is higher than the threshold voltage, it gives output bit as one. If the comparator output is one , the input of the loop filter is $V_{IN} - V_{REF}$ and if it is zero ,then input of the loop filter is equal to V_{IN}. The average value of the output bitstream is equal to $\frac{V_{IN}}{V_{REF}}$. For the temperature measurement , the digital value of $\frac{\alpha \Delta V_{BE}}{V_{REF}}$ is needed. V_{IN} is $\alpha \Delta V_{BE}$ and V_{REF} is the bandgap reference voltage in the case ADC in the temperature sensor. Since V_{REF} is the sum of $\alpha \Delta V_{BE}$ and V_{BE} , this can be implemented as shown in the block Figure. 2.3. From the Figure.2.3 it can be seen that the input to the loop (V_x) is $\alpha.\Delta V_{BE}$

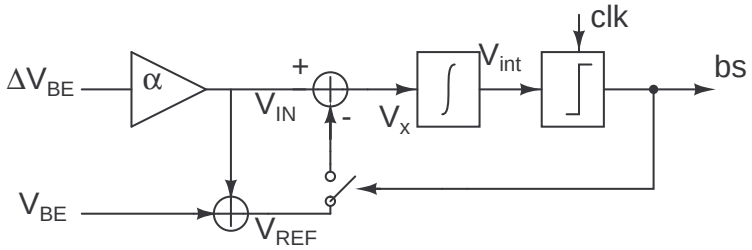


Figure 2.3: $\Delta\Sigma$ modulator in temperature sensor.

if bs=0 and $-V_{BE}$ when bs is one. So the the system can rearrange as shown in Figure.2.4[2]. This is more convenient because only one of the outputs from BJT-

Core , either ΔV_{BE} or V_{BE} is needed at a time. The output of BJT-Core is fed as input to $\Delta\Sigma$ modulator. The BJT-Core is designed in such a way that its output is ΔV_{BE} if bs is zero and V_{BE} if bs is one. Design of BJT core is discussed in chapter 3. This means $V_{IN} - V_{REF}$ is directly taken from BJT-Core. This concept can be exploited in DSM design. Due to negative feedback in the modulator, the

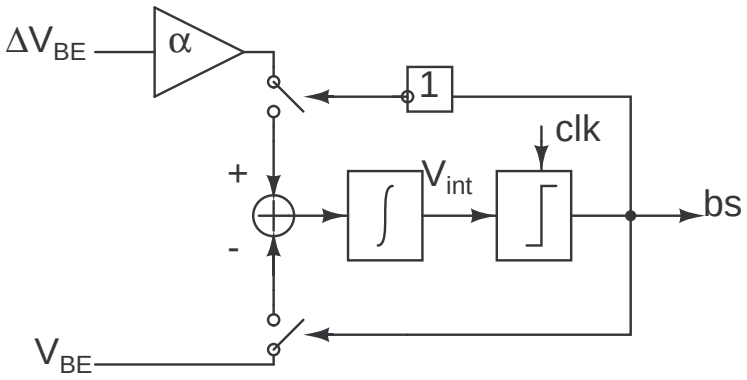


Figure 2.4: $\Delta\Sigma$ modulator in temperature sensor.

charge added at the input of the modulator on an average is zero. The charge added while integrating $\alpha.\Delta V_{BE}$ is removed during the integration of $-V_{BE}$. This charge balancing can be expressed as

$$\begin{aligned}(1-\mu).\alpha.\Delta V_{BE} &= \mu.V_{BE} \\ \mu &= \frac{\alpha.\Delta V_{BE}}{V_{BE}+\alpha.\Delta V_{BE}} \\ &= \frac{\alpha.\Delta V_{BE}}{V_{REF}} \end{aligned} \tag{2.5}$$

where μ is the average value of the bitstream bs. μ is used to calculate the temperature. From equation (2.4) , the digital temperature can be expressed as

$$D_{out} = A.\mu + B \tag{2.6}$$

2.3 Accuracy of reading the value

To get the required accuracy of 0.1^0C , the random error due to mismatch and noise has to be reduced to the level of of 0.01^0C. This accuracy can be expressed as the accuracy requirement in ΔV_{BE} and V_{BE}. The sensitivity of the digital output with respect to ΔV_{BE}, V_{BE} and α is calculated by differentiating it with corresponding variable.

$$\frac{\partial D_{out}}{\partial \Delta V_{BE}} = \frac{A.\alpha V_{BE}}{(V_{BE} + \alpha.\Delta V_{BE})^2} \tag{2.7}$$

$$\frac{\partial D_{out}}{\partial V_{BE}} = -\frac{A.\alpha \Delta V_{BE}}{(V_{BE} + \alpha.\Delta V_{BE})^2} \tag{2.8}$$

$$\frac{\partial D_{out}}{\partial \alpha} = \frac{A.\Delta V_{BE}.V_{BE}}{(V_{BE} + \alpha.\Delta V_{BE})^2} \tag{2.9}$$

$\frac{\partial D_{out}}{\partial \Delta V_{BE}}$, $\frac{\partial D_{out}}{\partial V_{BE}}$ and $\frac{\partial D_{out}}{\partial \alpha}$ are plotted against temperature and the accuracy requirement in V_{BE}, ΔV_{BE} and α are found out. The plots are shown in Figure.2.5, Figure.2.6 and Figure.2.7. It is evident from the plots that, the sensitivity of V_{BE}, $\Delta V_{BE}$and α depend on temperature. The worst case for V_{BE} is at high temperature. For ΔV_{BE}, the worst case is at low temperature and for α, it is at temperature around 50^0C. The error tolerable for V_{BE} is 31μV and for ΔV_{BE}, it is 2.3μV for reducing the temperature error at level of 0.01^0C. Similarly, $6 \times 10^{-3}\%$ accuracy is demanded for α to achieve the same.

2.4 Curvature Correction

The collector current of BJT can be expressed as

$$I_C = I_S \exp\left(\frac{qV_{BE}}{kT}\right) \tag{2.10}$$

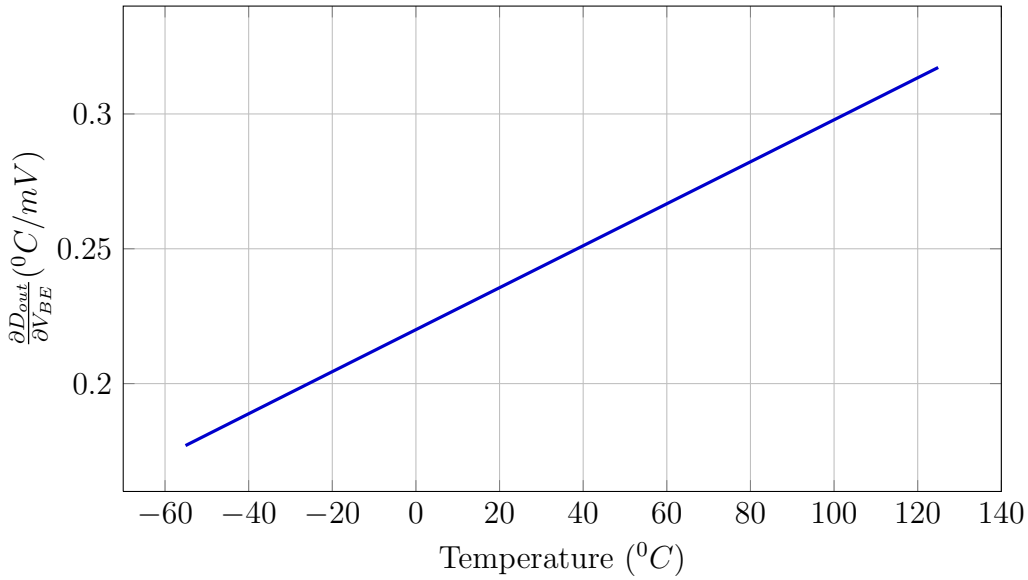


Figure 2.5: Sensitivity of sensor output with respect to V_{BE}.

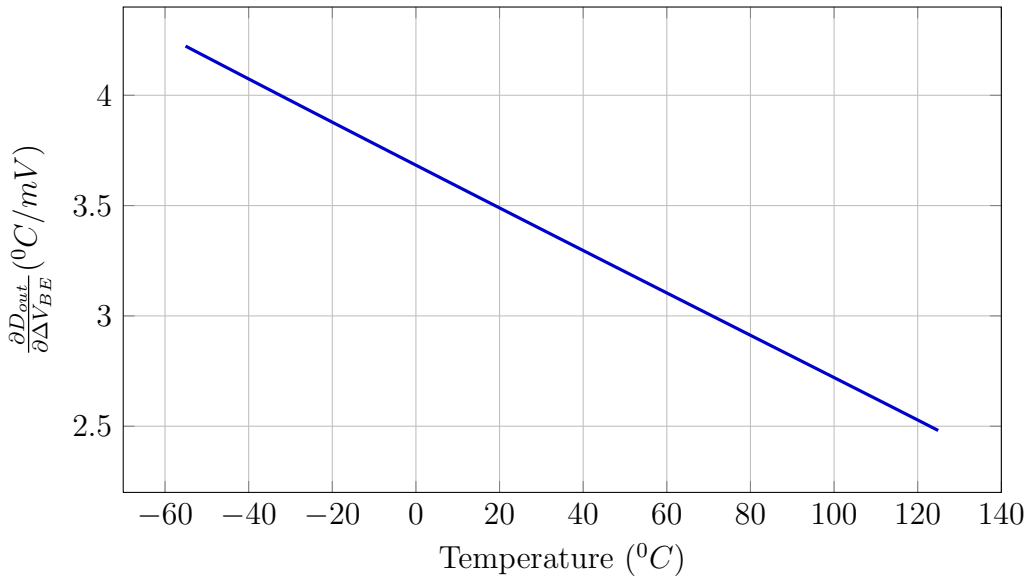


Figure 2.6: Sensitivity of sensor output with respect to ΔV_{BE}.

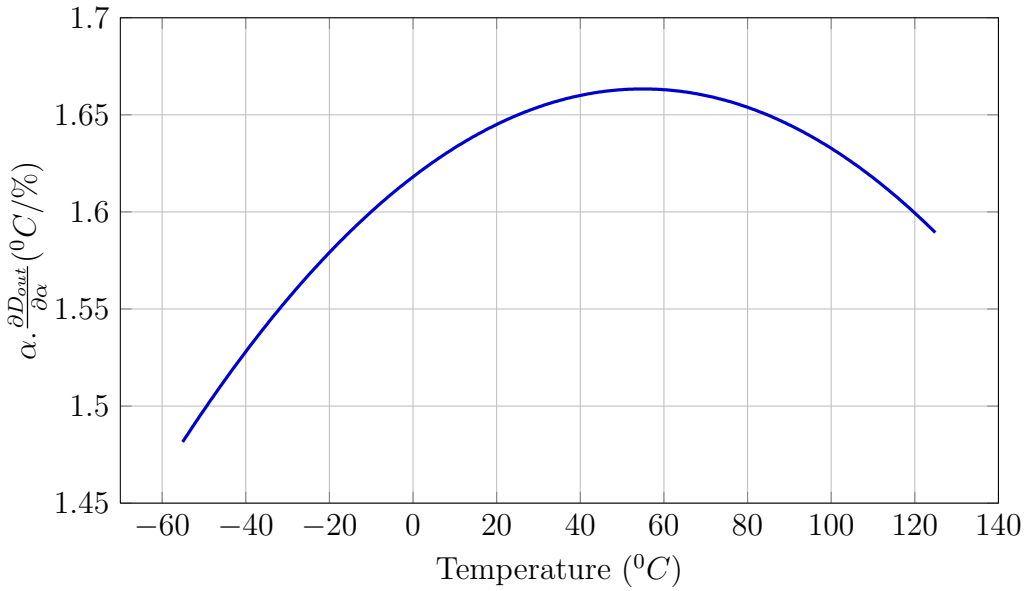


Figure 2.7: Sensitivity of sensor output with respect to α.

The saturation current I_S is dependent on mobility and intrinsic concentration of silicon. The temperature dependency of I_S can be expressed as [3]

$$I_S(T) = CT^{\eta} \exp\left(\frac{-qV_{g0}}{kT}\right) \tag{2.11}$$

where C is a constant, V_{g0} is the extrapolated bandgap reference voltage at 0K temperature and η is modelling parameter which comes from device physics. The value of V_{g0} and η are 1.17 and 2.38 respectively for UMC -180nm $25\mu m^2$ substrate BJT. Substituting equation(2.11) in equation(2.10) , VBE can be expressed as [1]

$$V_{BE}(T) = V_{BE0} - \lambda T + V_{CURV}(T) \tag{2.12}$$

where

$$V_{CURV}(T) = \frac{k}{q}(\eta - 1)(T - T_r - T\ln(\frac{T}{T_r})) \tag{2.13}$$

and T_r is the reference temperature where V_{BE} is linearized. It is evident from expressions 2.12 and 2.13 that the dependency of V_{BE} on temperature is nonlinear. The term V_{CURV} is the indication of non-linearity. Since V_{BE} is nonlinear, the

band-gap reference voltage V_{REF} is also nonlinear. The non linearity in V_{REF} leads to non-linearity in output of the sensor.

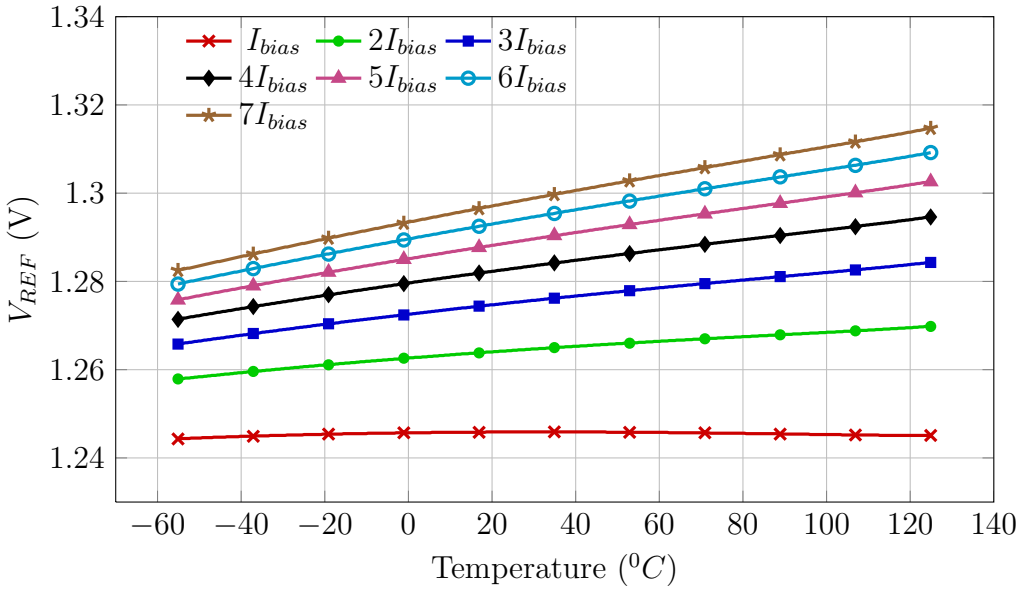


Figure 2.8: Reference voltage for different values of bias current.

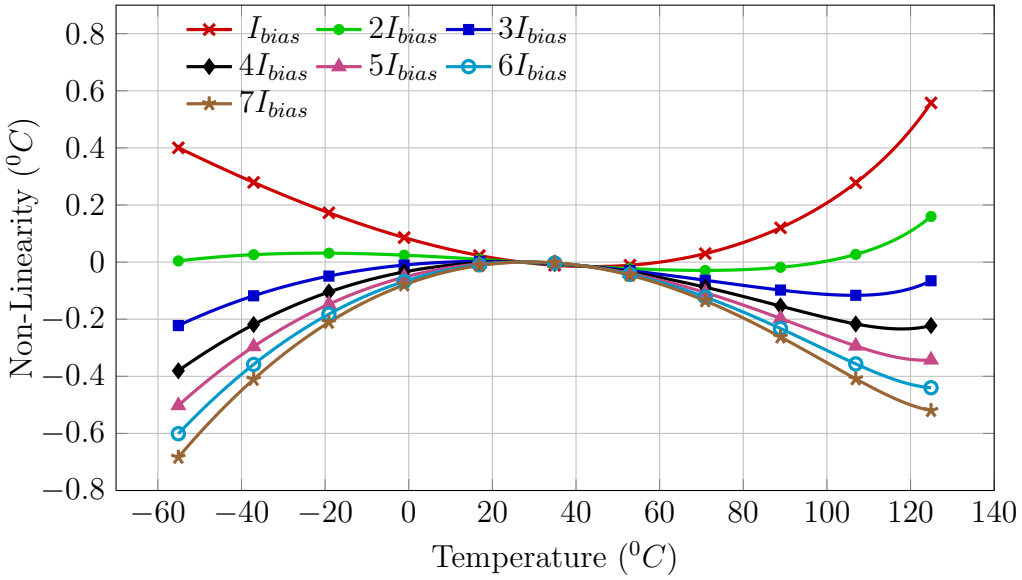


Figure 2.9: Non-linearity of temperature reading (D_{out}). (Output is trimmed at room temperature

The curvature of V_{REF} considering the temperature dependency of resistor in the bandgap reference is as shown in Figure.2.8. The reference voltage V_{REF} shown with bias current I_{bias} is the conventional bandgap reference with zero temperature coefficient around the room temperature. The reference voltage plotted with

different bias currents is as shown in Figure.2.8. From the Figure 2.8, it is clear that as bias current increases the temperature coefficient of V_{REF} becomes more positive. The corresponding non linearity in the output of the temperature sensor is shown in Figure.2.9.

The non linearity can be reduced by the proper choice of temperature coefficient for V_{REF}. The temperature coefficient of V_{REF} can be changed by changing the bias current. It is evident from the Figure.2.9 that the slight positive temperature coefficient for V_{REF} reduces the non linearity at output of the sensor[4]. From Figure.2.9 it can be noted that the emitter current value between $2I_{bias}$ and $3I_{bias}$ gives minimum error with respect to linear fit output. The unit emitter current (I_{bias}) chosen is $1.3\mu A$.

CHAPTER 3

BJT Core

The BJT Core generates voltage V_{BE} or ΔV_{BE}. The Delta Sigma Modulator (DSM) integrates it and creates the bitstream values which is used for temperature measurement. V_{BE} is generated by passing a current through BJT and ΔV_{BE} is generated by passing 1:p current through two different BJTs and taking the difference between their V_{BE} value. Since either V_{BE} or ΔV_{BE} is integrated by the DSM modulator at a time, it is possible to use same BJT for generating V_{BE} and ΔV_{BE}.

3.1 Generating ΔV_{BE}

The difference between the base emitter voltage of two BJTs which carry currents in 1:p ratio will give ΔV_{BE}. The value of p used is 6. The matching between the current sources should be high enough to reduce the random variation in ΔV_{BE} lesser than the required level to keep the temperature error less than 0.01^0C.

3.1.1 Matching requirement between current sources

Current sources with $1 : p$ ratio is used to generate ΔV_{BE}. For this purpose, $p+1$ identical current sources are used. Mismatch between current sources will lead to error in ΔV_{BE}. So to make error within the limit of accuracy, the current sources are to be matched. Let I be the average value of the $p+1$ current sources, then i^{th} current source can be express as I(1+δ_i). If j^{th} current source is a unity current

source,

$$\Delta V_{BE} = \frac{kT}{q} \ln \left(\frac{\sum_{i=1, i\neq j}^{p+1} I_i}{I_j} \right)$$

$$= \frac{kT}{q} \ln(p) + \frac{kT}{q} \ln \left(\frac{1 + \frac{\sum_{i=1, i\neq j}^{p+1} \delta_i}{p}}{1 + \delta_j} \right) \tag{3.1}$$

Since δ_i is small and average value of δ_i is zero , the equation 3.1 can be simplified as

$$\Delta V_{BE} \simeq \frac{kT}{q} \ln(p) - \frac{kT}{q} \frac{p+1}{p} \delta_i \tag{3.2}$$

Knowing the maximum tolerable error in ΔV_{BE} and p=6, the matching in the current sources should be less than $5.72\times\ 10^{-3}\%$ to get the required temperature accuracy for sensor. This order of matching is not achievable. For this reason, Dynamic element matching is used.

3.1.2 Dynamic Element Matching in the current sources

The error due to mismatch can be reduced by dynamically selecting the unit current source from $p + 1$ current sources. This average error due to mismatch can relax the matching requirement between the current sources. If I_k is used as unit current source, V_{BEk} is the corresponding base emitter voltage and assuming

δ_i and average value of δ_i are small

$$\begin{aligned}\Delta V_{BEk} &= \frac{kT}{q}\ln\left(\frac{\sum_{i=1,i\neq k}^{p+1} I_i}{I_k}\right)\\ &= \frac{kT}{q}\ln(p) + \frac{kT}{q}\ln\left(\frac{1+\frac{\sum_{i=1,i\neq k}^{p+1}\delta_i}{p}}{1+\delta_k}\right)\\ &\simeq \frac{kT}{q}\ln(p) - \frac{kT}{q}\frac{p+1}{p}\delta_i + \frac{kT}{2q}\left(\frac{p+1}{p}\delta_i\right)^2 \end{aligned} \tag{3.3}$$

Since the mean value of δ_i is zero, the average value of ΔV_{BE} can be written as

$$\Delta V_{BE,avg} \simeq \frac{kT}{q}\ln(p) + \frac{kT}{2q}\left(\frac{p+1}{p}\delta_i\right)^2 \tag{3.4}$$

Now the required matching between the current sources are 1%. The p+1 dynamic element matched current sources are used to generate ΔV_{BE} as shown in Figure3.1 [5].

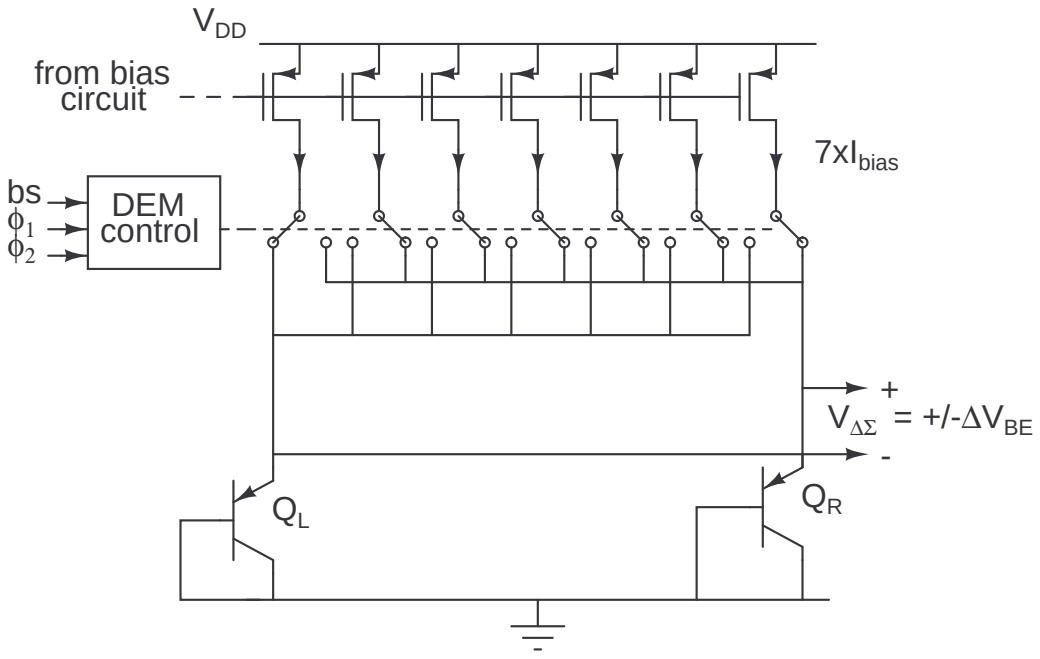


Figure 3.1: Generating ΔV_{BE} with DEM current sources.

By switching the current sources appropriately , each current source can be directed towards Q_L or Q_R. One of the current sources is directed to one BJT and the rest of them are to other BJT to generate ΔV_{BE}. The error due to mismatch can be averaged out by alternating the unit current source in each DSM cycle.

3.2 Generating V_{BE}

V_{BE} is generated by passing current through the BJT. Only the substrate PNP is available in CMOS technology. The collector of the substrate PNP is the p-substrate of the die and it is always connected to the ground. So the way to bias the BJT is by fixing the emitter current I_E. V_{BE} of the BJT can be expressed as

$$V_{BE} = \frac{kT}{q} \ln \left(\frac{I_E}{I_S} \frac{\beta}{\beta + 1} \right) \tag{3.5}$$

Since V_{BE} depends on the absolute value of I_S, β and I_{bias}, the spread of these quantities affect the value of V_{BE}. β-independent biasing scheme is used to make the value of V_{BE} independent of β. This is discussed in chapter 4. The spread in I_S and I_{bias} are corrected by using trimming. There are so many trimming techniques available in the literature. Scaling the emitter, scaling the bias current and adding programmable PTAT voltage are some of them. These techniques require a lot of chip area. In this work, delta sigma digital to analog converter is used to get high trimming resolution. Figure.3.2 shows the V_{BE} generator using bitstream controlled trimmed bias current [6]. I_{trim} is generated from the 1:6 current sources which is used for generating ΔV_{BE}. This can be done because the DSM integrates either ΔV_{BE} or V_{BE} at a time. One of the seven current sources is controlled by the DDSM output and others are controlled by the course tuning input C. The other six current sources can be switched on or off by using input C. Depending on the DDSM output, the current I_{trim} goes back and forth between $C.I_{bias}$ and $(C+1).I_{bias}$. The average value of I_{trim} can be controlled by using the

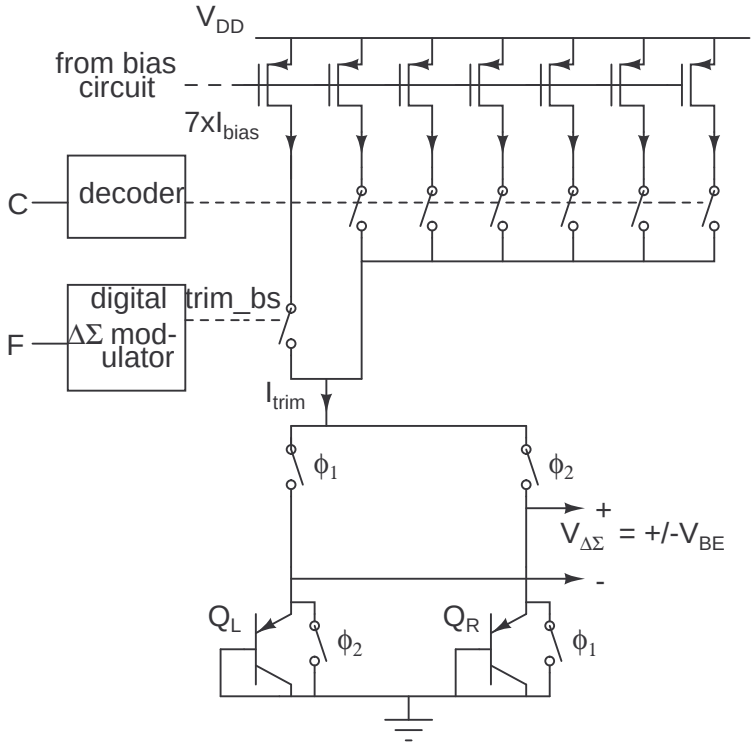


Figure 3.2: Generating V_{BE} using trimmed current sources

digital input F. Total trimming range available in this arrangement is 0 to $7I_{bias}$.

V_{BE} can be written as

$$\begin{aligned} V_{BE} &= \frac{kT}{q} \ln \left(\frac{I_E(1+\varepsilon_{I_E})}{I_S} \frac{\beta}{\beta+1} \right) \\ &= \frac{kT}{q} \ln \left(\frac{I_E}{I_S} \frac{\beta}{\beta+1} \right) + \frac{kT}{q} \ln(1+\varepsilon_{I_E}) \end{aligned} \tag{3.6}$$

ε_{I_E} is the relative error in the emitter current. From the equation (3.6) it can be seen that, to make V_{BE} error due to spread in the emitter bias current less than $31\mu V$, the range of trimming has to be made 10bit. So 10bit trimming range is needed to make the error due to spread in bias current in the order of 0.01^0C at the output of the sensor. This is done using the course tuning using the input C and fine tuning using DDSM. This implies that a trimming resolution of 8nA is needed to achieve the same. This can achieved by 8bit first order DDSM.

3.3 Delta Sigma Digital to Analog Converter

As discussed in the section 3.2, V_{BE} has to be trimmed to avoid the effect of spread of saturation current ε_{I_S} and the spread of emitter bias current ε_{I_E}. Trimming is done by using $\Delta\Sigma$ DAC. The block daigram of conventional $\Delta\Sigma$ DAC is shown in Figure.3.3. For the trimming, it gives a digital input F to the delta sigma. Here

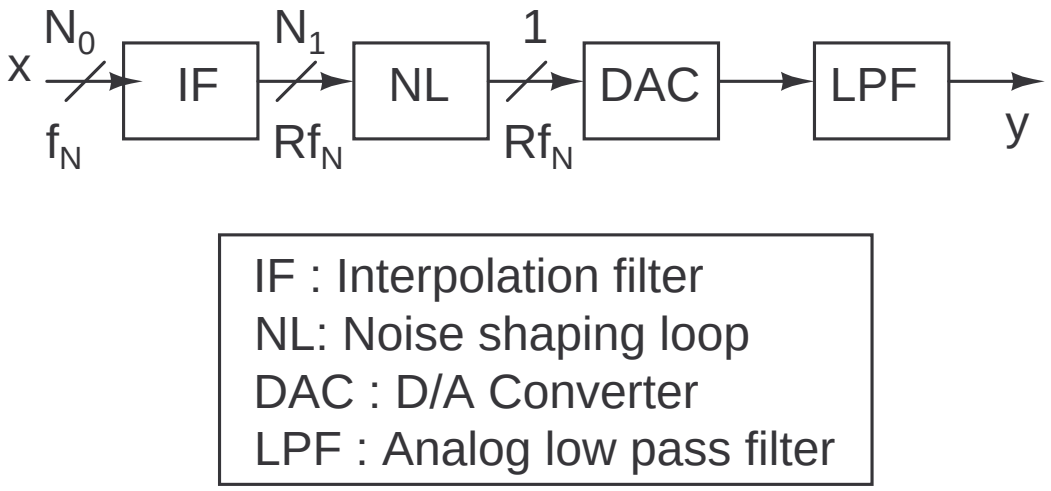


Figure 3.3: Block diagram of a $\Delta\Sigma$ DAC.

this value is same for at least during one reading of the sensor. One reading of the sensor is obtained by averaging 800 $\Delta\Sigma$ cycles. So the digital input is same for the 800 $\Delta\Sigma$ cycles. It means that the digital input is interpolated as the same value for 800 cycles. So the oversampling ratio R is 800. The general structure of the noise shaping is as shown in the Figure.3.4. In the Figure.3.4 x,y and e are input, output of DDSM and truncation error respectively. In the z-domain this can be written as

$$\begin{aligned} E_1(z) &= X(z) - H(z)E(z) \\ E(z) &= Y(z) - E_1(z) \\ Y(z) &= X(z) + (1 - H(z))\, E(z) \end{aligned} \tag{3.7}$$

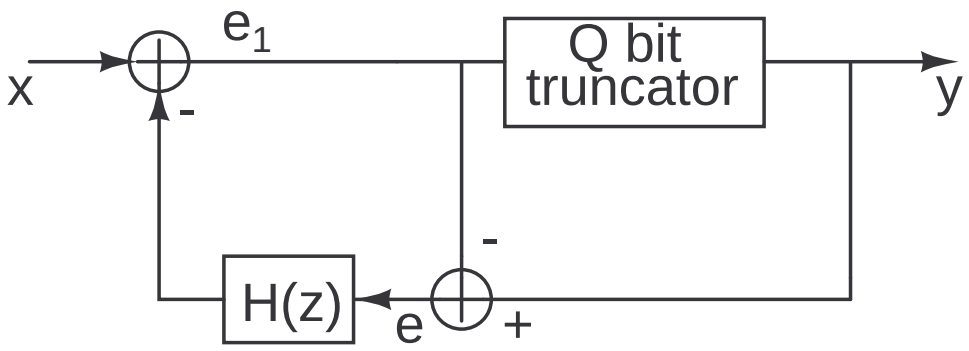


Figure 3.4: Error feedback DDSM.

Comparing equation 3.7 with usual DSM output, it can be shown that

$$STF(z) = 1$$
$$NTF(z) = 1 - H(z) \tag{3.8}$$

The word length and gain of the loop are chosen in such a way that the modulator is stable. For Q bit truncator, maximum OBG of the NTF possible is 2^Q [7]. Since the required accuracy is 8bit , the first order noise shaping is used and $H(z) = 1$ is chosen to get the first order NTF. The first order DDSM is as shown in Figure.3.5. This digital delta sigma is coded in verilog and synthesized using the tool Designvision. The synthesized netlist is placed and rooted by using the tool Encounter.

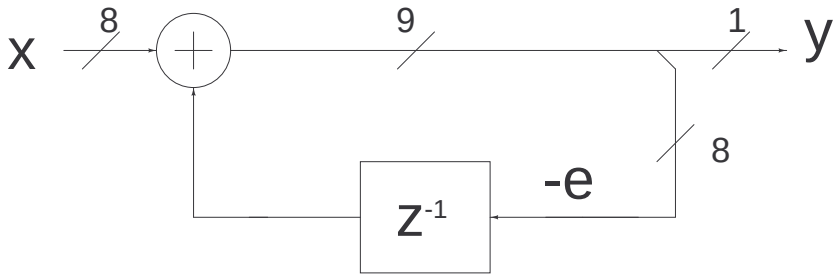


Figure 3.5: First order digital delta sigma modulator.

3.4 Complete funcioning BJT Core

The full schematic of the BJT-Core is as shown in Figure.3.6. If bs=1 and ϕ_1 is

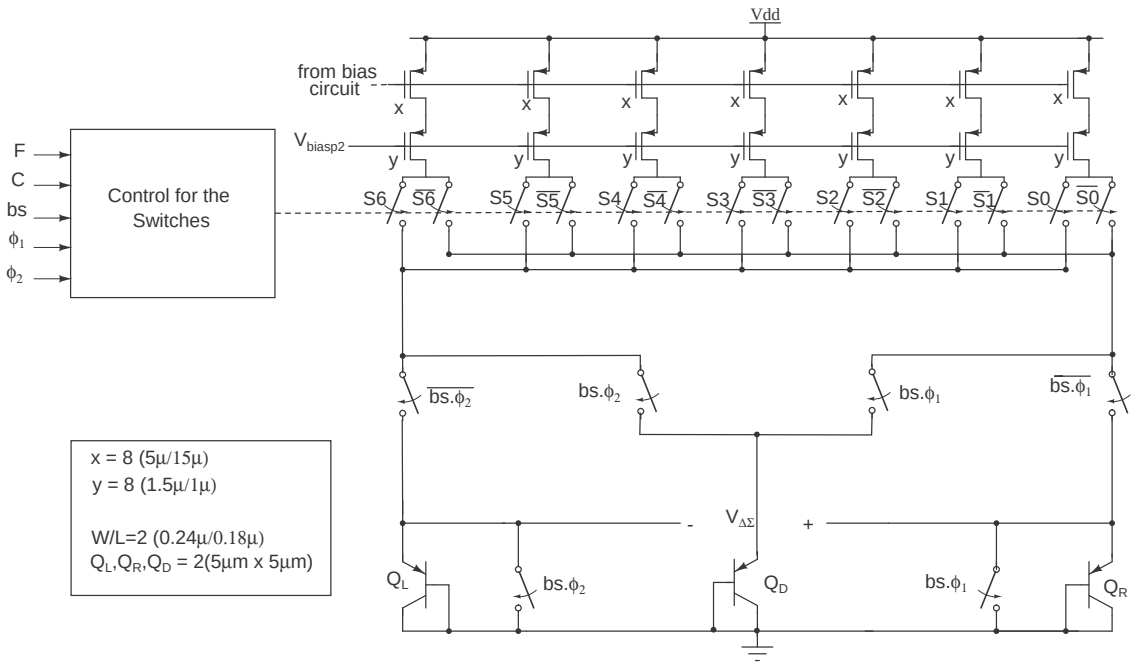


Figure 3.6: The complete BJT-Core.

high , the trimmed bias current flows through Q_L and the remaining current flows through the dummy transistor Q_D which carries the unused current. The emitter of transistor Q_R is shorted to ground and $V_{\Delta\Sigma}$ is equal to $-V_{BEL}$. While the currents between Q_L and Q_R swap, the value of $V_{\Delta\Sigma}$ is equal to $-V_{BER}$. If bs=0 and ϕ_1 is high, $6I_{bias}$ current flows through Q_R and I_{bais} current flows through Q_L and $V_{\Delta\Sigma}$ becomes ΔV_{BE}. During ϕ_2 , the current swaps between Q_R and Q_L and $V_{\Delta\Sigma}$ becomes $-\Delta V_{BE}$. If bs=0, ΔV_{BE} is integrated twice by using six times higher sampling capacitor than in bs=0. So clock ϕ_1 and ϕ_2 reduce the time period when the bs=0. The layout of BJT-Core is done and the functionality is verified using RC-extracted simulation.

The output of BJT-Core with clock is as shown in Figure.3.7. The required matching of current source is 1% and this is verified by the Monte Carlo analysis. The Histogram obtained for 1000 samples is as shown in Figure 3.8.

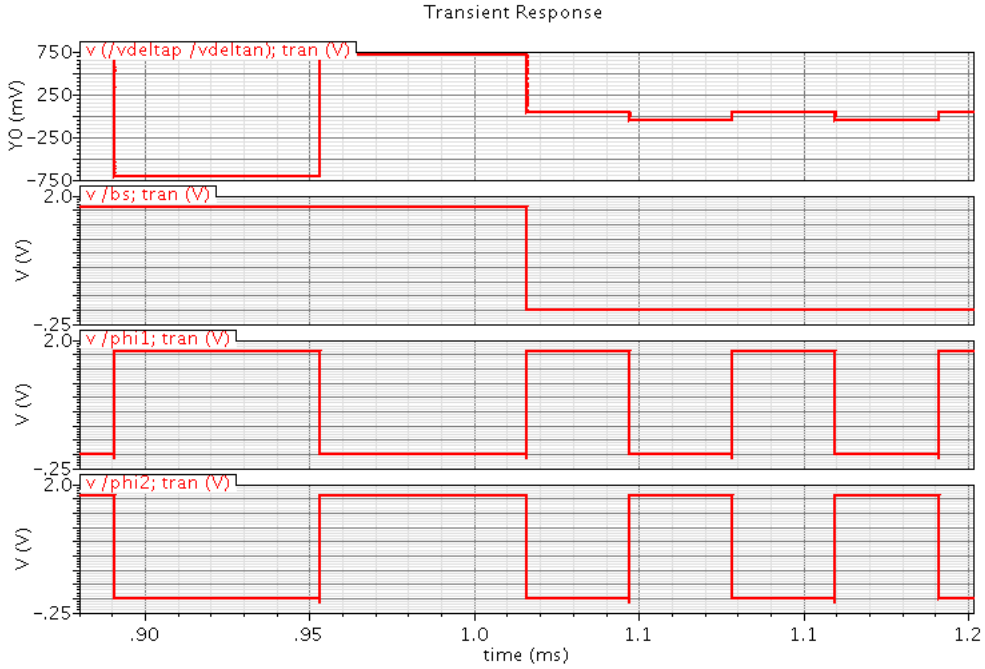


Figure 3.7: The RC extracted simulation result of BJT-Core.

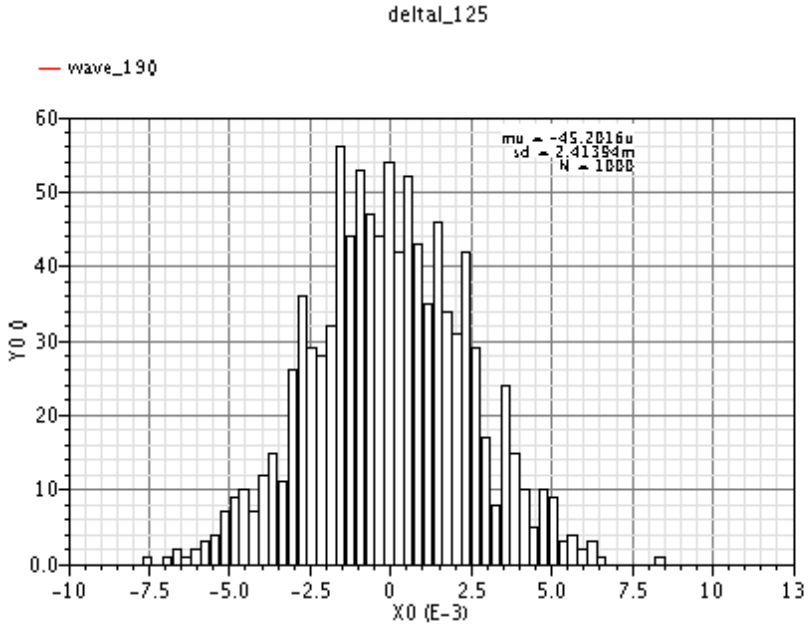


Figure 3.8: Histogram from Monte Carlo Analysis ($\frac{I_2-I1}{average(I2,I1)}$ plotted).

CHAPTER 4

BJT Bias Circuit

4.1 β- independent bias generator

The base emitter voltage of BJT can be written as

$$\begin{aligned} VBE &= \frac{kT}{q}\ln(\frac{I_C}{I_S}) \\ &= \frac{kT}{q}\ln(\frac{\beta I_E}{I_S(\beta+1)}) \end{aligned} \tag{4.1}$$

where k is Boltzmann's constant, T is the temperature in kelvin, q is the electron charge, I_C is the collector current of the BJT, I_E is the emitter current of BJT and β is current gain of BJT. The current gain of BJT (β) depends on temperature

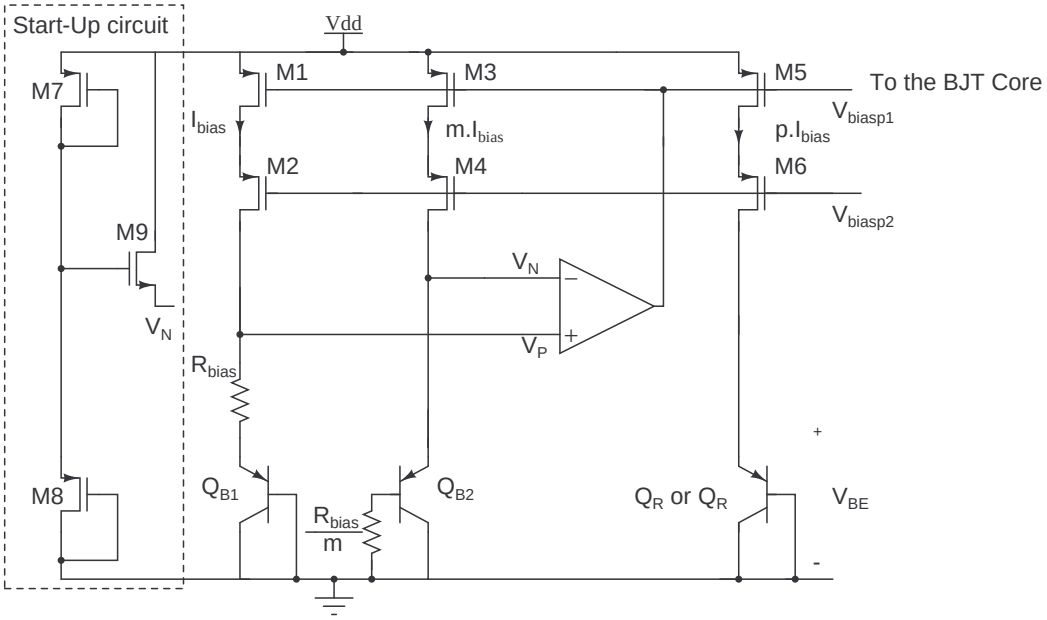


Figure 4.1: β- independent bias generator makes the V_{BE} value independent of current gain of BJT.

significantly. This leads to temperature error which is higher than tolerable range.

Nominal value of β is 1.38 in 0.18μm technology. The circuit to generate V_{BE} value independent of the current gain of the BJT is as shown in Figure 4.1[2]. The difference between base emitter voltages ($\Delta V_{BE,bias}$) of Q1 and Q2 can be written as

$$\begin{aligned} \Delta V_{BE,bias} &= V_{BE2} - V_{BE1} \\ &= \frac{kT}{q}\ln(m) \end{aligned} \tag{4.2}$$

where 1:m is the current ratio in QB1 and QB2. Here m is chosen to be 10. Since the negative feedback ensures that the voltage between two terminals of the op-amp is zero,

$$R_{bias}.I_{bias} - \frac{R_{bias}}{m}\frac{m.I_{bias}}{(\beta+1)} = \Delta V_{BE,bias} \tag{4.3}$$

$$I_{bias} = \frac{(\beta+1)}{\beta}\frac{\Delta V_{BE,bias}}{R_{bias}} \tag{4.4}$$

The currents through Q_L or Q_R are mirrored from M1 and I_E is equal to $p.I_{bias}$. Substituting this in equation (4.1) , V_{BE} is given by

$$VBE = \frac{kT}{q}\ln\left(\frac{p.\Delta V_{BE,bias}}{R_{bias}.I_S}\right) \tag{4.5}$$

It is clear from equation (4.6) that , V_{BE} value is independent of β.

The offset in the β- independent bias generator introduces error in V_{BE}. It is not possible to trim out the spread in the value of V_{BE} completely. The major sources of error in the circuit shown in Figure.4.1 are offset of the op-amp and mismatch between Q_1 and Q_2. Error due to these factors should be less than accuracy requirement while reading ΔV_{BE} and V_{BE}.The BJT core designed is as shown in Figure.4.1. The input referred offset of op-amp V_{OS} directly appears as

an error in $\Delta V_{BE,bias}$ which in turns appear as an error in V_{BE}. V_{BE} with the offset at op-amp is given by[8]

$$VBE = \frac{kT}{q} \ln\left(\frac{p(.\Delta V_{BE,bias} + V_{OS})}{R_{bias}.I_S}\right) \tag{4.6}$$

$$= \frac{kT}{q} \ln\left(\frac{p\Delta V_{BE,bias}}{I_S Rbias}\right) + \frac{kT}{q} \ln\left(1 + \frac{V_{OS}}{\Delta V_{BE,bias}}\right) \tag{4.7}$$

$$\approx \frac{kT}{q} \ln\left(\frac{p\Delta V_{BE,bias}}{I_S Rbias}\right) + \frac{V_{OS}}{\ln(m)} \tag{4.8}$$

The error should be less than the maximum tolerable error in V_{BE} (31μV). This leads to V_{OS} value less than 71μV for m=10. This level of offset is very difficult to achieve. So chopping is used to reduce the offset of op-amp in β- independent bias generator. A finite voltage difference exists between op-amp terminals due to finite open loop gain (A_{OL}). This is approximately equal to $\frac{\Delta V_{BE,bias}}{A_{OL}}$. This causes an error of $\frac{\Delta V_{BE,bias}}{A_{OL}\ln(m)}$ in V_{BE}. To make V_{BE} error within tolerable range, the open loop gain has to be higher than 1100,or 61dB. This can be easily achieved.

The start-up circuit is necessary for this circuit to work as expected. When switching on the supply, there is a possibility that the emitter of Q_{B2} and Q_{B1} are at zero voltage and the current through these are zero. This is also a valid operating point of the circuit. But this operating point is not the desired one. If emitter of Q_{B2} is zero and then switching on M7 makes it nonzero. If loop starts working, the emitter voltage of Q_{B2} is high and M7 is switched off, then the start-up circuit has no effect on the functioning of the circuit.

4.2 Offset cancellation

As found in section 4.1, some offset cancellation technique is needed to achieve the required accuracy. Chopping is used to cancel the offset of the op-amp [2].

The circuit used is as shown in Figure.4.2. The switch position in ϕ_1 is shown in

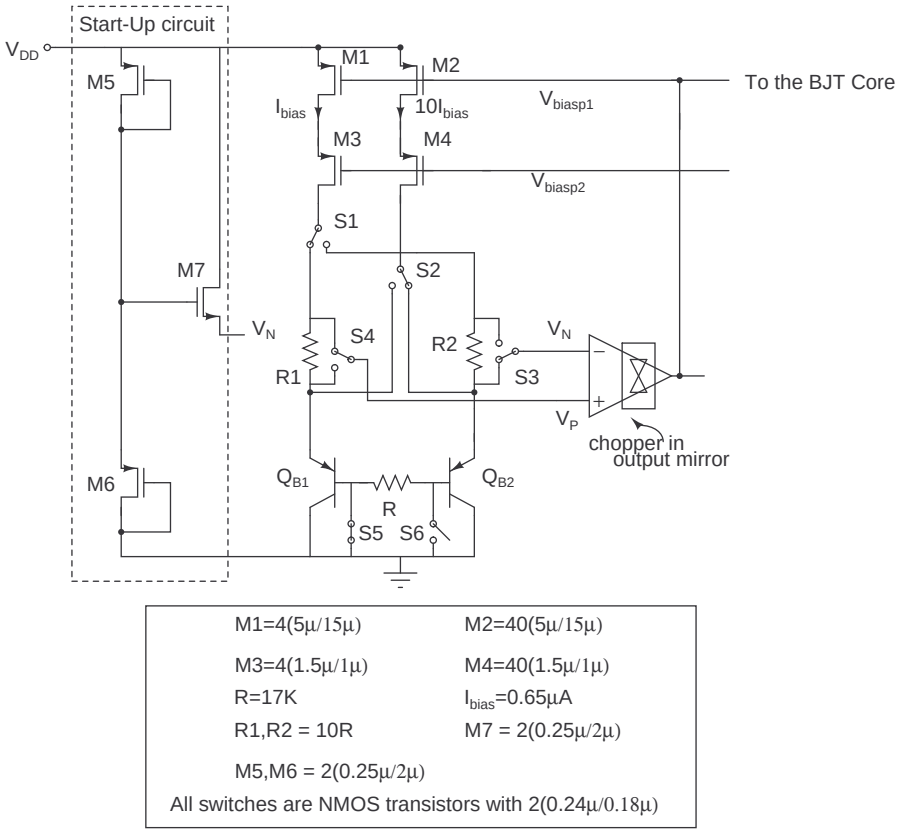


Figure 4.2: Chopped β- independent bias generator.

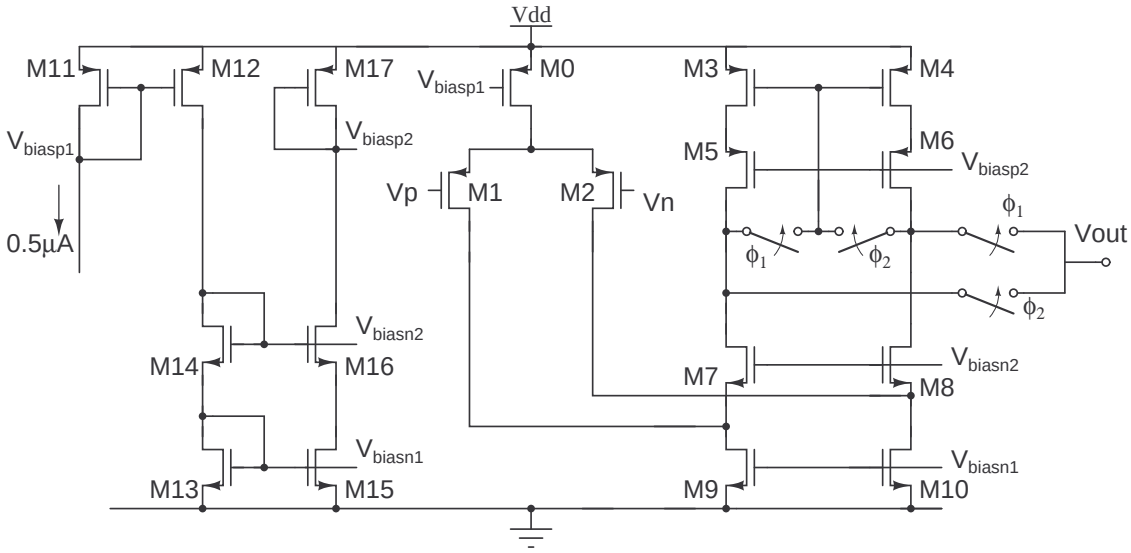
Figure.4.2. During ϕ_1, in BJT-Core , bias current is switched to Q_L and during ϕ_2 bias current is switched to Q_R. If there is any offset present in the bias generator circuit, one BJT (Q_L or Q_R) is biased with positive offset and other with negative offset. Integrator in the DSM is integrating the sum of this V_{BE}. So effectively the offset effect is nullified.There will be residual offset due to exponential nature of BJT characteristic.

$$V_{BEL} + V_{BER} = \frac{kT}{q} \ln\left(\frac{p(.\Delta V_{BE,bias} + V_{OS})}{R_1.I_{SL}}\right) + \frac{kT}{q} \ln\left(\frac{p(.\Delta V_{BE,bias} - V_{OS})}{R_2.I_{SR}}\right)$$
$$\simeq 2\frac{kT}{q} \ln\left(\frac{p.\Delta V_{BE,bias}}{\sqrt{R1.R2}\sqrt{I_{SR}.I_{SL}}}\right) - \frac{kT}{q}\left(\frac{V_{OS}}{\Delta V_{BE,bias}}\right)^2 \quad (4.9)$$

It can be seen that V_{OS} required for the op-amp is less than 2mV. And also there is no matching requirement between Q_L,Q_R and R_1,R_2.

4.3 Op-amp in β- independent bias generator

The folded cascode op-amp is used in chopped β- independent bias generator. The output current mirror is chopped synchronously with the chopper in the β-independent bias generator to keep the negative feedback. The speed of op-amp is chosen in such a way that the voltage V_{biasp1} in Figure.4.2 settles during switching. This op-amp is driving the gate of the current sources present in the BJT-Core. These transistors are large in size to achieve the matching. The tail current is made 6μV to settle V_{biasp1} node voltage in Figure.4.2 and it settles within the clock period of chopping. The op-amp is configured in the unity feedback and the magnitude



M0 = 24(2μ/1μ)	M9,M10 = 20(0.75μ/3μ)
M1,M2 = 16(2μ/1μ)	M11,M12 = 2(2μ/1μ)
M3,M4 = 8(2μ/1μ)	M13,M14 = 2(0.75μ/3μ)
M5,M6 = 8(2μ/1μ)	M15,M16 = 2(0.75μ/3μ)
M7,M8 = 8(0.75μ/3μ)	M17 = (2μ/12μ)

All switches are PMOS with 2(0.24μ/0.18μ)

Figure 4.3: Opamp with output current mirror chopped.

and phase response loop gain is plotted with 2pF load capacitor. The magnitude and the phase response in as shown in Figure.4.4 and 4.5 respectively.

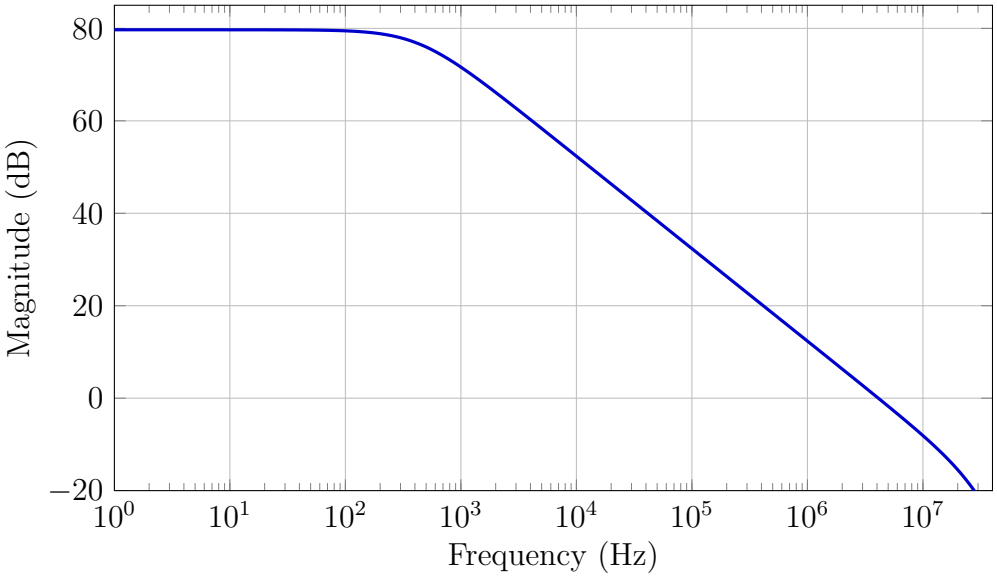


Figure 4.4: Magnitude response of loop gain.

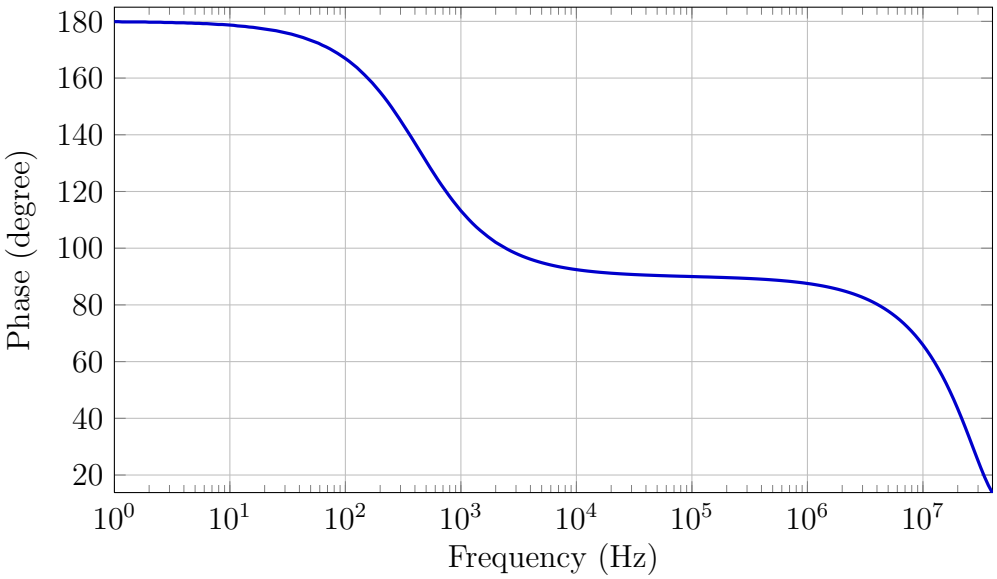


Figure 4.5: Phase response of the loop gain.

Table 4.1: Summary of opamp in the β- independent bias generator

DC loop gain	79dB
Unity gain frequency (C_L=2pF)	4.1MHz
Input referred offset	1.6mV
Power consumed	20.7 μ W

CHAPTER 5

Delta Sigma ADC

The incremental delta sigma ADC is used for the conversion of analog value to a digital value which in turn is used for the temperature reading. As discussed in chapter.2, this can be achieved by using incremental delta sigma ADC (charge balancing converter). But the exact charge balancing does not practically. This is equivalent to quantization noise in the ADC. The error due to this factor has to be in the order of 0.01^0C to get the overall accuracy of 0.1^0C. From equation 2.6 the error in μ can be found. The error that is tolerable in μ is 1.5×10^{-5}. This leads to an accuracy requirement of the ADC equal to 16bits.

5.1 Modulator Loop Design

Delta-sigma modulator with 16 bit accuracy is needed for converting the temperature to digital output. In sensor application , the frequency of the signal is small so that the incremental $\Delta\Sigma$ ADC is used. The shaped quantization noise at the output of ADC is filtered using decimation filter. For the first order delta sigma, simple counter can be used as decimation filter. But 2^{16} $\Delta\Sigma$ cycles are needed to get an accuracy of 16bits. The desired conversion time is 100ms. In order to get this conversion time, sampling frequency of DSM has to be high. This leads to high power dissipation. So the first order modulator is not a good choice. The sampling frequency can be reduced by using second order modulator. For the second order modulator , in band noise is lesser than that in first order so that it is possible achieve the same bit accuracy using less number of delta sigma cycles.

The general CIFB second order delta sigma loop is as shown in Figure.5.1. The coefficients of the loop variable decides the NTF of the system. The second order modulator with single bit quantizer is used to achieve the design goal. The single bit quantizer has to use an OBG which is less than 1.5 for the stability of the loop. The Butterworth and inverse chebyshev are common functions used as NTF

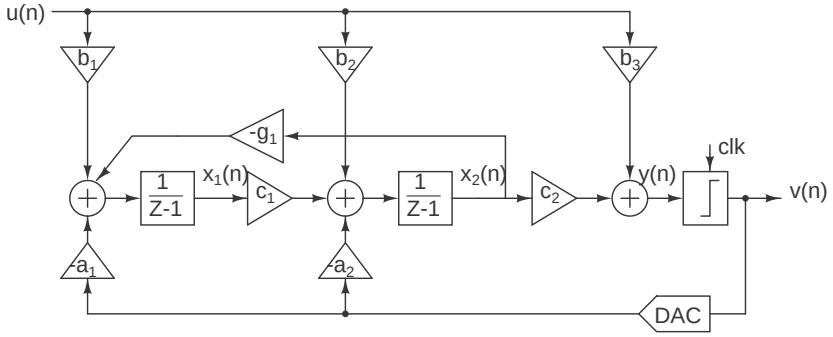


Figure 5.1: Second order Delta Sigma loop with CIFB structure.

functions. In butterworth implementation, g_1 value is zero. For high OSR, g_1 value is very small since second zero is close to $\omega = 0$. Very small coefficients are difficult to be implemented in switched capacitor type DSM. So the Butterwoth NTF function is used to implement the loop filter.

As described in chapter.2 when output of the DSM is zero, $\alpha.\Delta V_{BE}$ is integrated and when output is one, $-V_{BE}$ is integrated. The BJT-Core switches according to the DSM output. This means that the first subtraction is happening inside BJT-Core. The DSM loop includes the BJT-Core also. So the output from the BJT-Core is $V_{IN} - V_{REF}$. So the path containing b_3 has to be avoided from the conventional CIFB structure. The coefficient is calculated using delta sigma toolbox by setting $b_3 = 0$. Since b_3 is not part of the loop, this change will not affect the NTF, but STF is going to change. For second order delta sigma modulator, $a_1 = b_1$ and $a_2 = b_2$ and for butterworth NTF, $g_1 = 0$. Since $a_1 = b_1$ and $a_2 = b_2$, this can be pushed through the summing node and make the block diagram as shown in Figure.5.2. Since the quantizer is one bit, c_2 can be scaled to limit the integrator swing. $k_1 = a_1c_1$, $b = b_2$ and $k_2 = c_2$ in the Figure.5.2. The

NTF function as shown in Figure.5.3. Since in the sensor the ADC is working only at 40% ADC reference OBG slightly higher than 1.5 not an issue. The

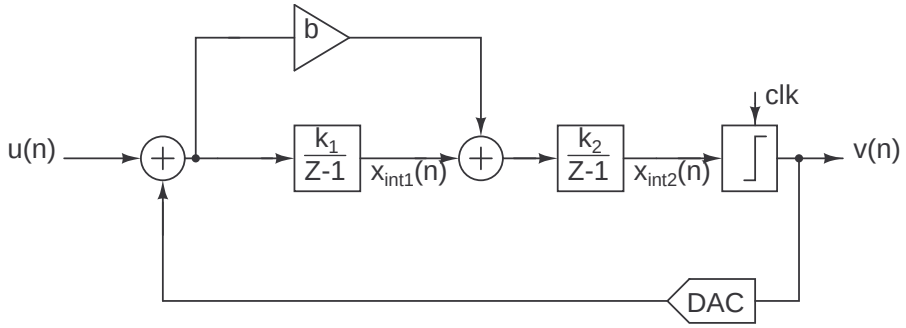


Figure 5.2: Second order Delta Sigma loop with CIFB structure.

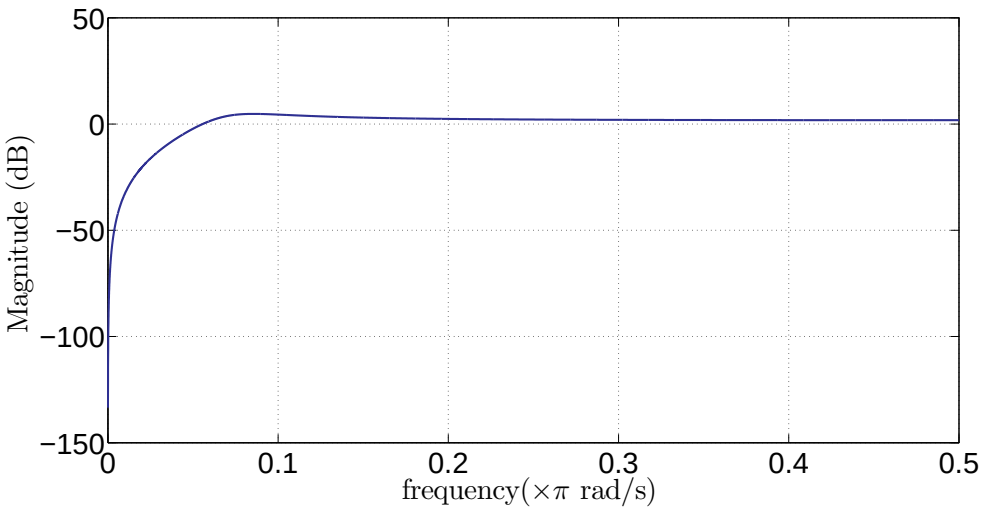


Figure 5.3: NTF of the modulator.

same modulator topology is configured for the incremental operation as shown in Figure.5.4. In incremental operation, the modulator state needs to be reset after every reading. By using the delta-sigma toolbox, the coefficients found and scaled the node and and k_1,b and k_2 are chosen as 0.25 , 2/3 and 0.5 respectively.The DSM noise mainly comes from quantization noise, thermal noise from switch and noise of the first op-amp. The quantization noise is made 10dB lesser than the targeted SNR. The thermal noise from switch and noise of the op-amp are made smaller than the minimum required voltage accuracy of input to read (That is equal to $2.3\mu V$ while reading the ΔV_{BE}). The sampling capacitor C_s is chosen as

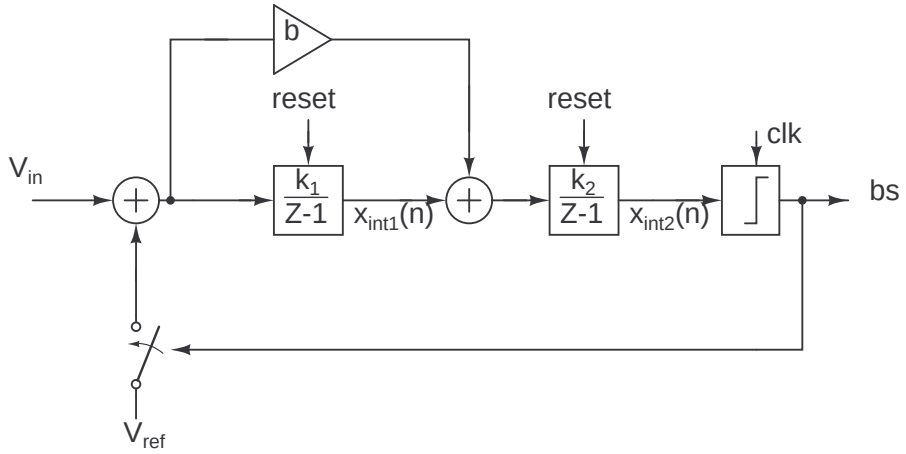


Figure 5.4: Second order Incremental Delta Sigma Modulator.

5pF. While integrating ΔV_{BE}, the sampling capacitor becomes 30pF to achieve six times gain than in V_{BE}. The accuracy of second order incremental DSM is approximately $2\log_2(N) - 1$ [9]. 800 cycles are chosen for one reading.

5.2 Realization of $\alpha\Delta V_{BE}$

The α value is realized by sampling the ΔV_{BE} input twice and each sampling gain of $\frac{\alpha}{2}$ is realized by increasing the number of sampling capacitor from one to $\frac{\alpha}{2}$.

5.2.1 Input sampling capacitor matching requirement

Let C_s be the average value of the $\frac{\alpha}{2}$ capacitors. Then i^{th} capacitor can be expressed as C(1+δ_i). Assuming j^{th} capacitor is used for sampling V_{BE} and $\frac{\alpha}{2}$ capacitor for the sampling of ΔV_{BE},

$$\alpha = 2 \times \left(\frac{\sum_{i=1}^{\frac{\alpha_{ideal}}{2}} C_i}{C_j} \right)$$

$$= \alpha_{ideal} \frac{C}{C(1+\delta_j)}$$

$$\approx \alpha_{ideal}(1 - \delta_j + (\delta_j)^2....) \tag{5.1}$$

To get the percentage accuracy of $6 \times 10^{-3}\%$ in α , the percentage variation in capacitor value needs to be $6 \times 10^{-3}\%$. This level of matching is not achievable. So it is necessary to use some kind of matching mechanism between capacitors.

5.2.2 Dynamic Element Matching

So one of the matching techniques is DEM. The capacitor used for the sampling of V_{BE} is chosen dynamically and the average value of α is made closer to the desired value.

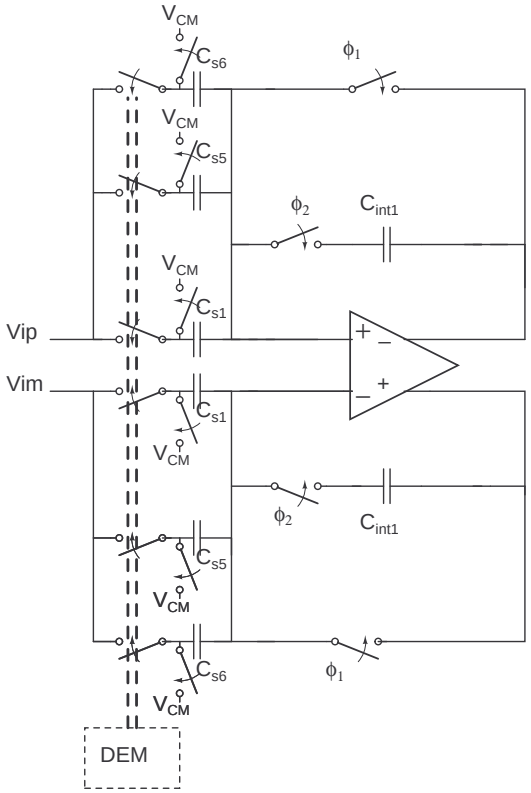


Figure 5.5: DEM on input sampling capacitor.

If the number of cycles during which V_{BE} value is integrated is exactly equal to a multiple of α , the gain error will be completely averaged out. So the gain error

after N Delta Sigma cycles is given by [8]

$$\left|\frac{\alpha - \alpha_{ideal}}{\alpha}\right| = \left|\frac{1}{N}\sum_{i=1}^{N-\lfloor\frac{N}{\alpha}\rfloor\alpha}\delta_i\right| \tag{5.2}$$

δ_i is Gaussian distributed. So the bound of equation (5.2) is

$$\left|\frac{\alpha - \alpha_{ideal}}{\alpha}\right| < \frac{\sqrt{\alpha - 1}}{N}\delta_{max} \tag{5.3}$$

To get the percentage accuracy of $6 \times 10^{-3}\%$ in α, the percentage variation of sampling capacitors should be less than 2%.

5.3 Opamp Design

Considering the above discussed concern, the op-amp needs to be designed. The first op-amp design is more crucial than the second op-amp, since the input referred noise at the input of the modulator is attenuated by the gain of previous block.

5.3.1 First Opamp

The maximum error that can be tolerable while reading V_{BE} and ΔV_{BE} are $31\mu V$ and $2.3\mu V$ respectively. So when the first integrator is integrating its input, the settling error due to finite gain and finite bandwidth of OTA is made less than this value. Settling error due to finite gain is given by

$$Settling\ error\ due\ to\ finite\ gain = \left(1 + \frac{C_S}{C_{int1}}\right)\frac{V_{in}}{A_0} \tag{5.4}$$

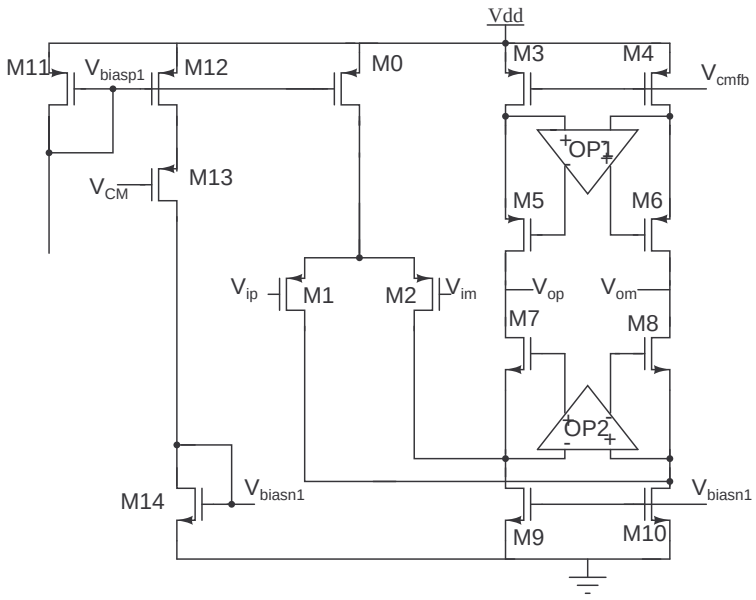
where C_S is the sampling capacitor, C_{int1} is the integrating capacitor and A_0 is the dc-gain of the op-amp. To make settling error less than 31μ for V_{BE} and 2.3μ for ΔV_{BE} at all temperatures , the first op-amp requires a dc gain of above 100dB.

The limiting reading is the ΔV_{BE} reading at high temperature. Similarly there is a settling error due to finite bandwidth of op-amp. The op-amp speed has to be high enough such that the desired settling is happening at some fraction of clock cycles. The settling error due to finite bandwidth is given by

$$Settling\ error\ due\ to\ finite\ bandwidth(in\%) = e^{\frac{-t_{set}}{\tau}} \tag{5.5}$$

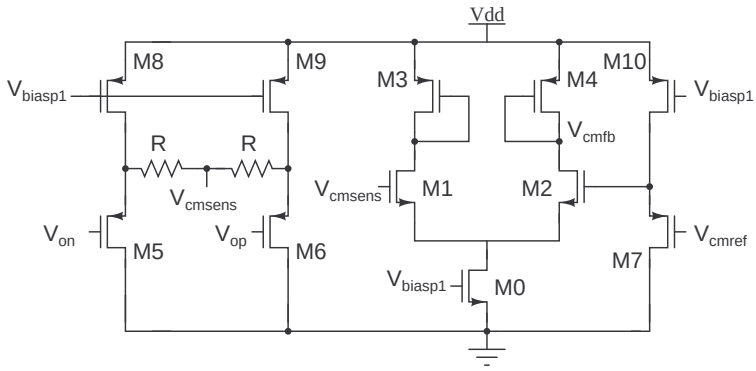
where t_{set} is the time of settling and τ is the time constant associated with dominant pole of the closed loop. To make settling error less than 31μ for V_{BE} and 2.3μ for the ΔV_{BE} at all temperatures, $t_{set} = 11\tau$. Settling time is decided such that one forth of the clock time is required for integration. While integrating ΔV_{BE}, the clock time available is one fourth of $\Delta\Sigma$ clock period. So the bandwidth required is decided by the accuracy requirement in ΔV_{BE}. The required UGB is higher than 0.6MHz.

Since the gain required is higher than 100dB, the gain boosted folded cascode opamp is used. PMOS input pair is used because input common-mode is zero. The schematic of the op-amp is as shown in Figure.5.6. The tail current used is 10μA to reduce the thermal noise floor in the required range. M9 and M10 are made in large size to reduce the flicker noise corner less than half of the sampling frequency. The commom mode feedback used for the op-amp is as shown in Figure.5.7. OP1 is folded cascode op-amp with NMOS input pair and the OP2 is folded cascode op-amp with PMOS input pair. The schematic of OP1 is as shown in Figure.5.8 and OP2 is as shown in Figure.5.9. The common mode feedback circuits of these opamps are shown in Figure.5.10 and Figure.5.11. The open loop magnitude and phase responses of the opamps are shown in Figure.5.12 and Figure.5.13. The common-mode feedback loop magnitude and phase response are as shown in Figure.5.14 and Figure.5.15 respectively. The settling of opamp is tested by configuring the designed opmap as integrator and applying a pulse. The settling of the opamp meets the accuracy requirement.



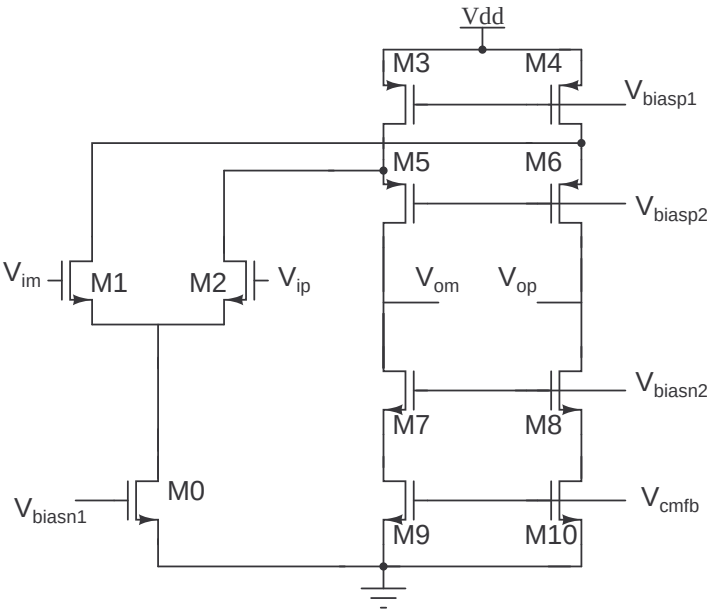
M11,M12 = 2(2μ/1μ)	M3,M4 = 8(2μ/1μ)
M13 = 2(2μ/1μ)	M5,M6 = 8(2μ/1μ)
M14 = 4(2μ/12μ)	M7,M8 = 8(0.75μ/3μ)
M0 = 40(2μ/1μ)	M9,M10 = 56(2μ/12μ)
M1,M2 = 24(1μ/0.5μ)	

Figure 5.6: Schematic of the first op-amp.



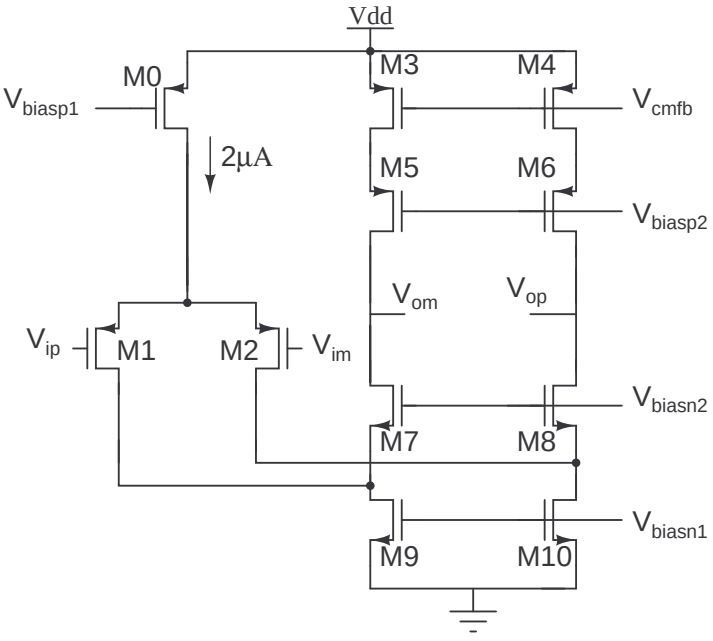
M0 = 16(2μ/12μ)	M5,M6,M7 = 4(2μ/1μ)
M1,M2 = 4(0.24μ/0.18μ)	M8,M9,M10 = 4(2μ/1μ)
M3,M4 = 4(2μ/1μ)	R = 1MΩ

Figure 5.7: Schematic of the common-mode feedback of first op-amp.



M0 = 8(0.75µ/3µ)	M5,M6 = 4(2µ/1µ)
M1,M2 = 4(1µ/0.5µ)	M7,M8 = 4(0.75µ/1µ)
M3,M4 = 8(2µ/1µ)	M9,M10 = 4(0.75µ/3µ)

Figure 5.8: Schematic of the folded cascode op-amp with NMOS input pair.



M0 = 8(2µ/1µ)	M5,M6 = 4(2µ/1µ)
M1,M2 = 8(1µ/0.5µ)	M7,M8 = 4(0.75µ/1µ)
M3,M4 = 4(2µ/1µ)	M9,M10 = 8(0.75µ/3µ)

Figure 5.9: Schematic of the folded cascode op-amp with PMOS input pair.

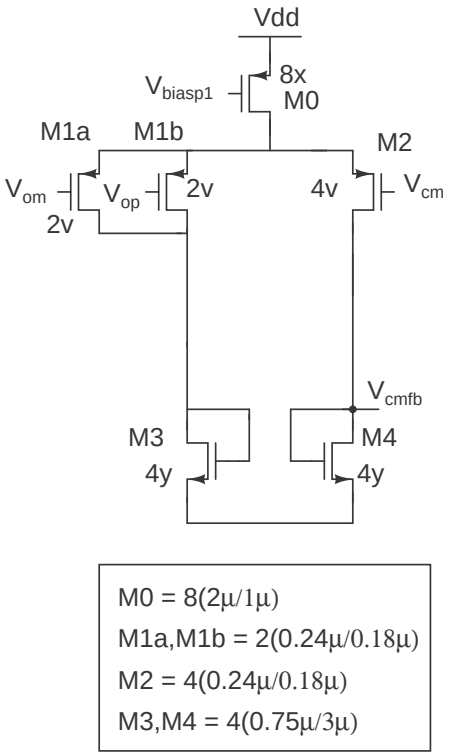


Figure 5.10: Schematic of the common-mode feedback of folded cascode op-amp with NMOS input pair.

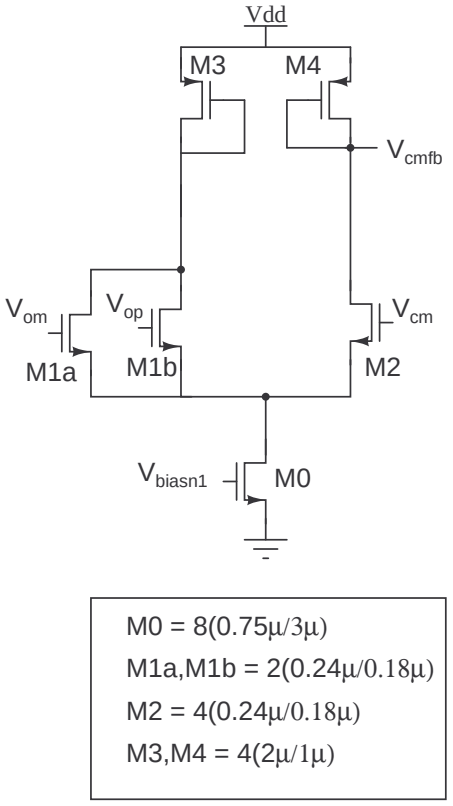


Figure 5.11: Schematic of the common-mode feedback of folded cascode op-amp with PMOS input pair.

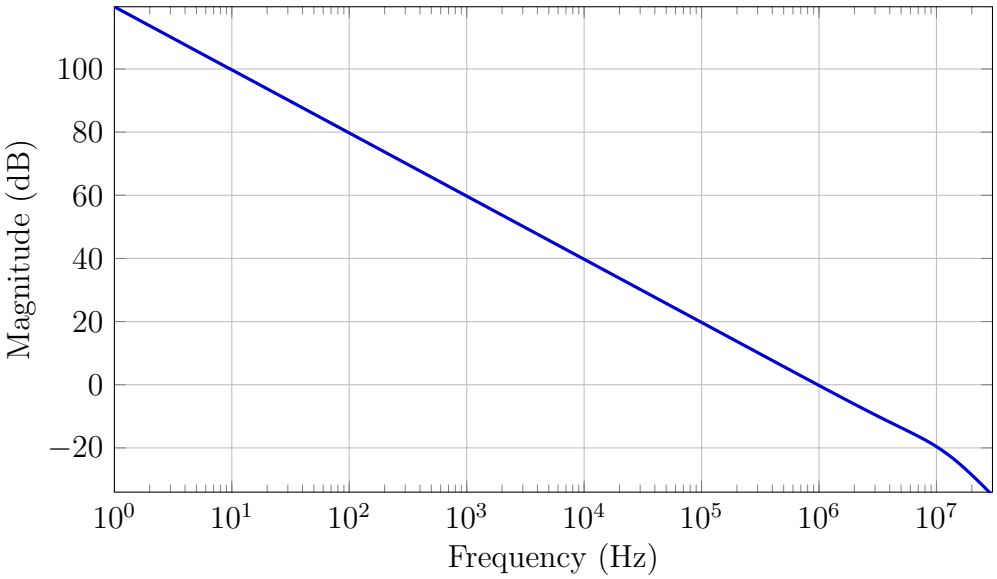


Figure 5.12: Magnitude response of opamp .

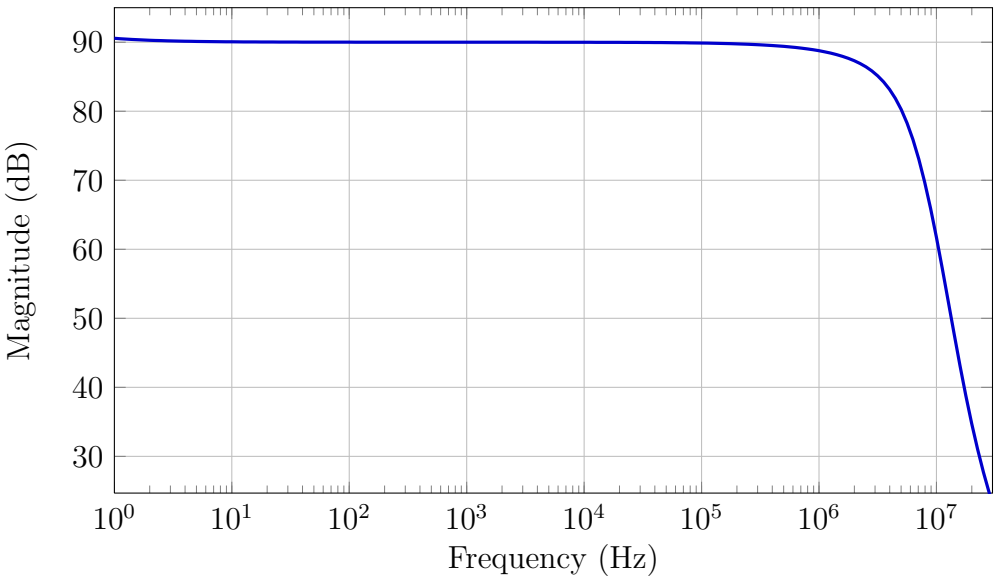


Figure 5.13: Phase response of opamp .

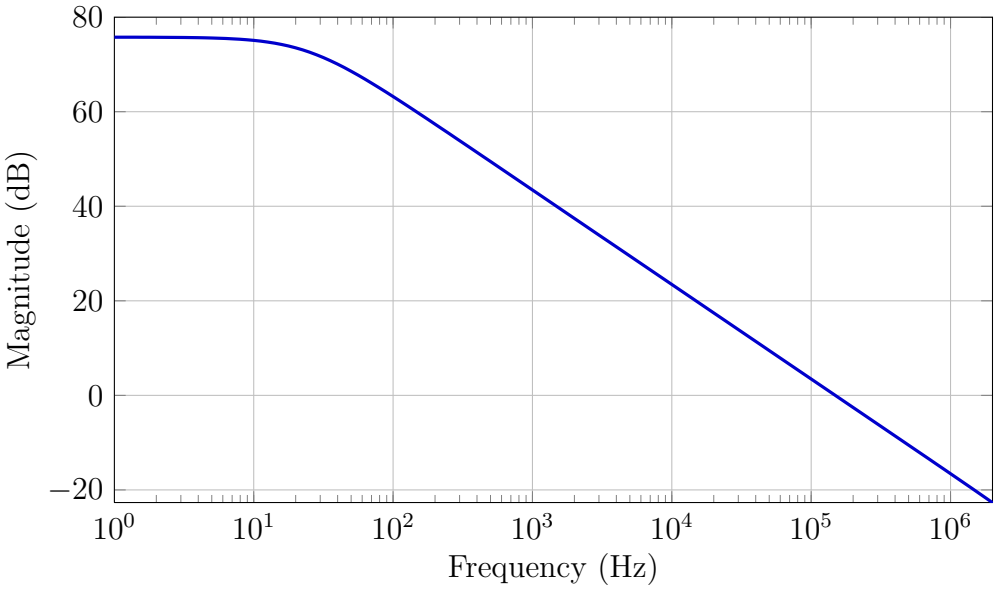


Figure 5.14: Magnitude response of commonmode feedback loop .

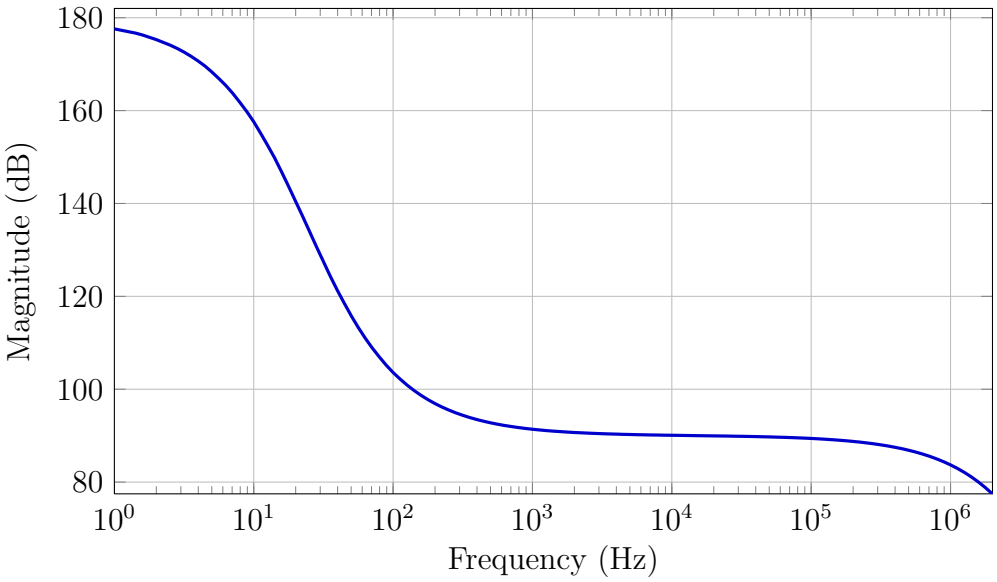
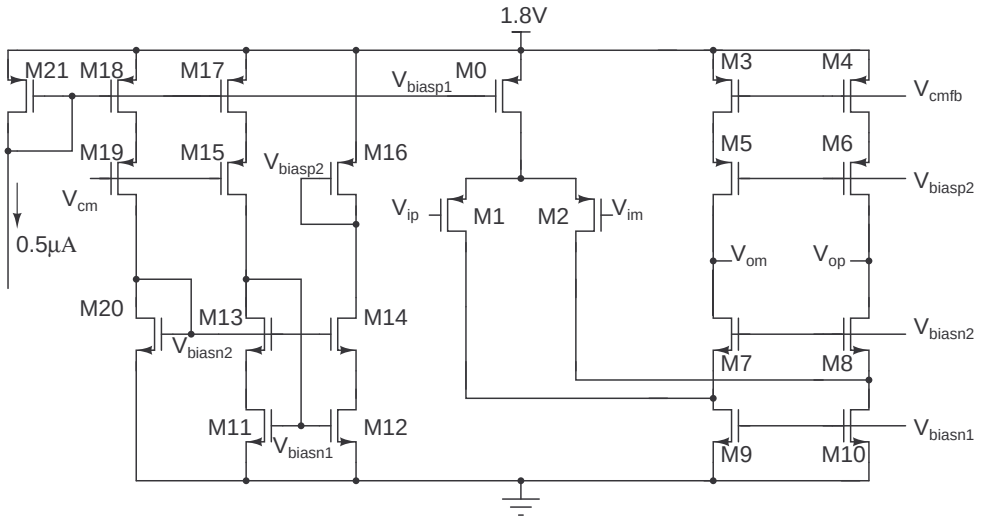


Figure 5.15: Phase response of commonmode feedback loop.

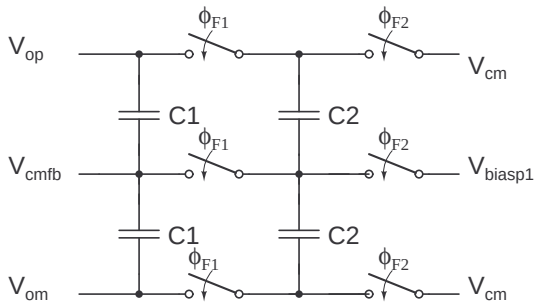
5.3.2 Second Opamp

The noise of the second opamp is attenuated by the first stage of the modulator. So the noise performance is not so critical here. A scaled down version of the folded cascode opamp designed for the first stage is used here. The schematic of the opamp is as shown in the Figure.5.16. The switched capacitor common mode feedback is used for the second opamp. The schematic of the common-mode feedback is as shown in Figure.5.17. The common mode settling is verified by the



M21,M18,M17 = 2(2µ/1µ)	M13,M14 = 2(0.75µ/3µ)	M3,M4 = 8(2µ/1µ)
M19,M15 = 2(2µ/1µ)	M16 = 2(2µ/10µ)	M5,M6 = 8(2µ/1µ)
M20 = 2(0.75µ/27µ)	M0 = 16(2µ/1µ)	M7,M8 = 8(0.75µ/3µ)
M11,M12 = 2(0.75µ/3µ)	M1,M2 = 4(2µ/0.5µ)	M9,M10 = 16(0.75µ/3µ)

Figure 5.16: Schematic of the OTA used in the second integrator .



C1=0.25pF

C2=1pF

All switches are transmission gates with NMOS=2(0.24µ/0.18µ) and PMOS=2(0.24µ/0.18µ)

Figure 5.17: Switched capacitor common mode feedback in the OTA of second integrator.

transient analysis. The gain and phase of the op-amp is plotted by putting the ideal common-mode feedback. (Since switched capacitor common-mode is used, ac analysis is not possible). The gain and phase of the op-amp are as shown in Figure. 5.18 and Figure.5.19 respectively.

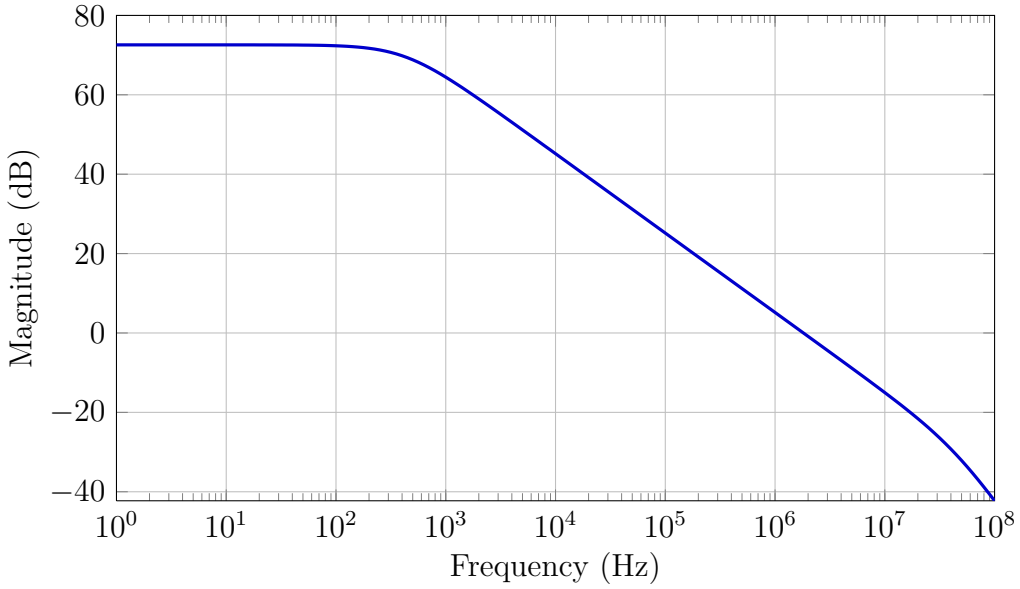


Figure 5.18: Magnitude response of the second op-amp.

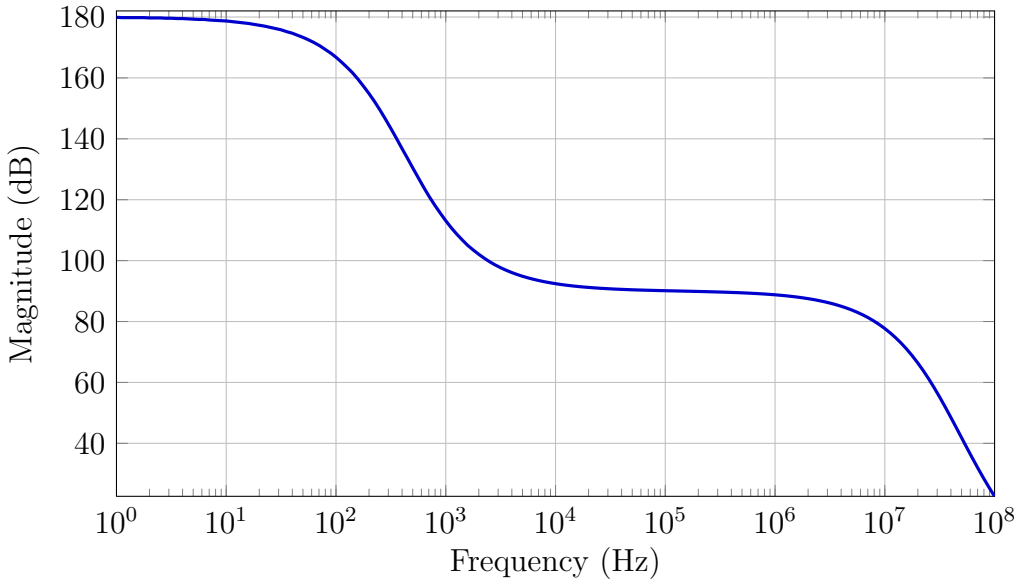
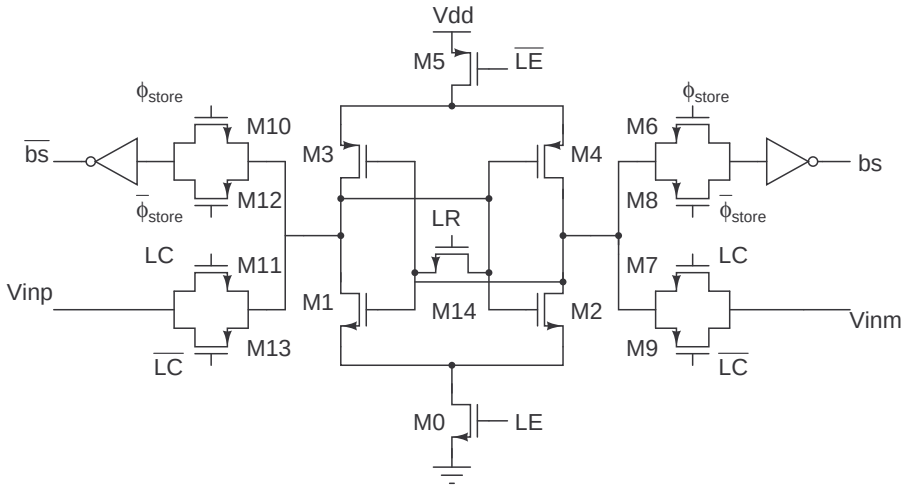


Figure 5.19: Phase response of the second op-amp.

5.4 Quantizer Design

The modualtor uses a single bit quantizer which compares the second integrator output with zero and generates output bitstream (bs). The inverter cross coupled latch is used for this as shown in Figure5.20. When LC is equal to one ,the



M0 = 2(0.24µ/0.18µ)	M6,M7 = 2(0.24µ/0.18µ)
M1,M2 = 2(0.24µ/0.18µ)	M8,M9 = 2(0.24µ/0.18µ)
M3,M4 = 4(0.24µ/0.18µ)	M10,M11 = 2(0.24µ/0.18µ)
M5 = 2(0.24µ/0.18µ)	M12,M13 = 2(0.24µ/0.18µ)
M14 = 2(0.24µ/0.18µ)	

Figure 5.20: Schematic of the quantizer latch

output of second integrator is sampled as the parasitic capacitor of the input of the inverters. LE is one, depending on the relative value betweem V_{inp} and V_{inm}. If V_{inp} is higher than V_{inm}, the value of bs is one , otherwise it is zero. This is called degeneration of latch. When ϕ_{store} is one , the degenerate value goes to buffer and this is the output of DSM. This bit value goes to BJT-Core and decides whether V_{BE} or ΔV_{BE} is to be integrated in the next DSM cycle. This output needs to be routed to clk generator and to DEM logic for the appropriate operation.

5.5 Offset and flicker noise cancellation

Since the low frequency signal is coming as the input, the flicker noise and the offset of the op-amp are concerns. The circuit of first stage integrator is as shown in figure.5.21. Let the offset does not change from ϕ_1 phase to ϕ_2 phase. (Similar

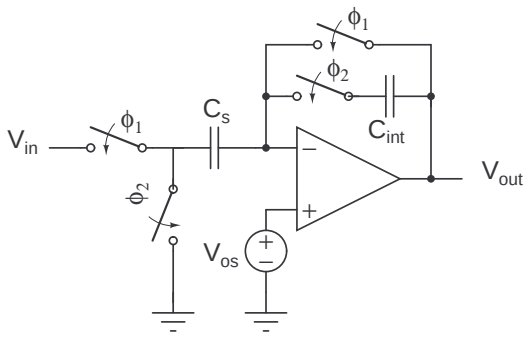


Figure 5.21: Correlated Double Sampling.

case can be applied for 1/f noise, since 1/f noise corner is very much smaller than sampling frequency). At the end of ϕ_1 phase, the charge stored in C_s is $C_s(V_{os} - V_{in}(n))$ and in C_{int} is $C_{int}(V_{os} - V_{out}(n-1))$. During ϕ_2 phase,charge stored in C_s is $C_s(V_{os})$ and in C_{int} is $C_{int}(V_{os} - V_{out}(n))$. Equating the charges in both phases of the clock,

$$C_s(V_{os} - V_{in}) + C_{int}(V_{os} - V_{out}(n-1)) = C_s(V_{os}) + C_{int}(V_{os} - V_{out}(n))$$
$$V_{out}(n) = V_{out}(n-1) + \frac{C_s}{C_{int}} V_{in} \tag{5.6}$$

Ideally the offset and 1/f noise completely cancel each other by this technique. This technique in literature is known as correlated double sampling. The problem with this technique is the folding back of broadband thermal Noise. The folded back component is given by[10]

$$S_{fold,white} \approx \left(\frac{\pi f_c}{f_s} - 1\right) S_0 sinc^2\left(\frac{\pi f}{f_s}\right) \tag{5.7}$$

f_c is -3dB frequency of the system and f_s is sampling frequency. If noise bandwidth of $\frac{\pi}{2} f_c$ is half of the sampling frequency , there is no folding back component. In general f_c is higher than f_s, since the integrator's settling requirement is determining f_c. So for the first op-amp, thermal noise is made smaller to take care the folding back component . It can be seen from the Figure.5.22 and Figure.5.23

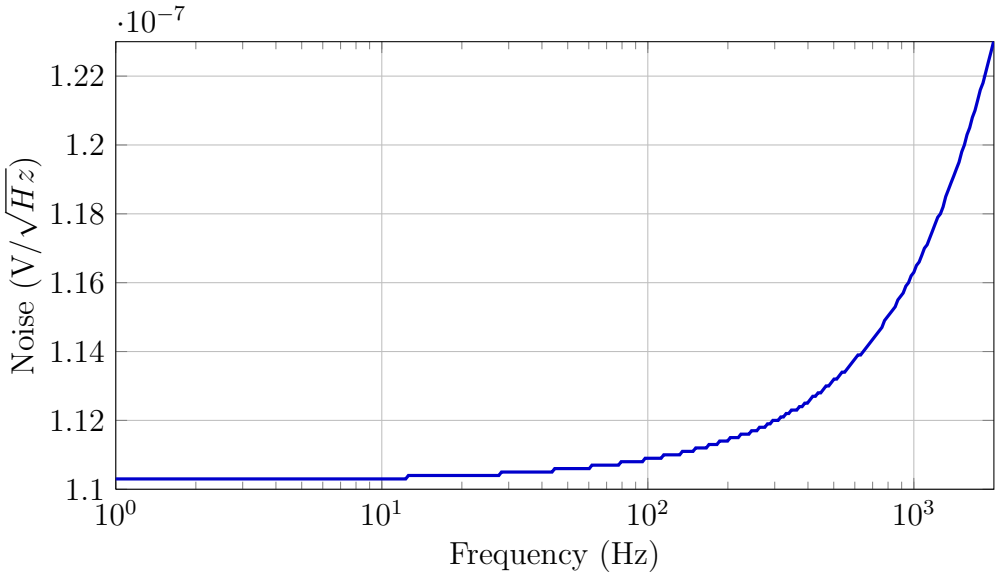


Figure 5.22: Input refred noise of first opamp with CDS.

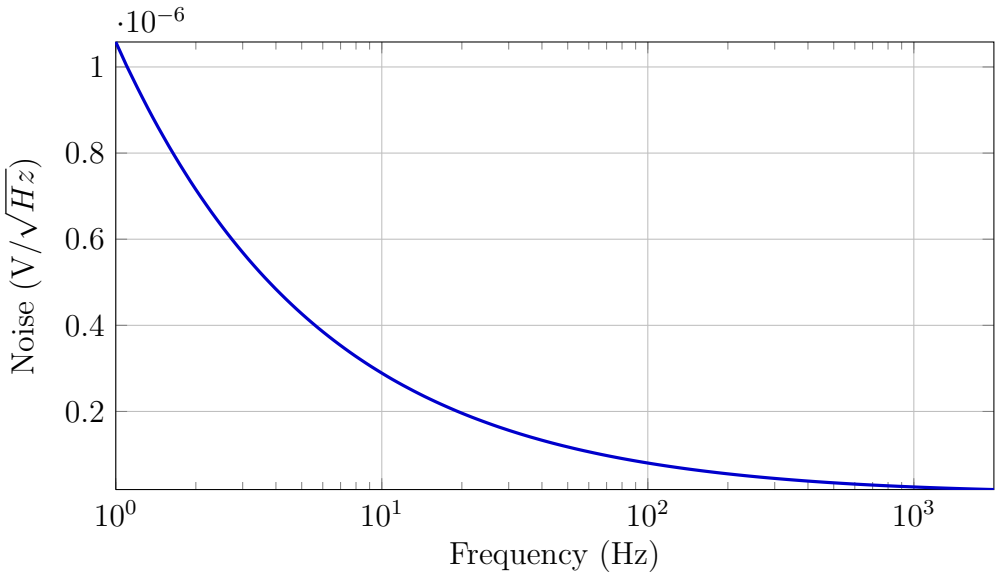


Figure 5.23: Input refred noise first opamp without CDS.

that due to CDS, the noise at the band of interest is reduced considerably as expected.

5.6 System Level Chopping

CDS technique ideally nullifies the effect of offset and 1/f noise. But charge injection from the switches leads to error in reading value. To avoid this, fully differential topology is used . In fully differential topology, the change in voltage across capacitor due to charge injection acts as common-mode signal as long as the switches are well matched. But the mismatch between sampling switches leads to a differential charge injection. For minimum size transistor (W=0.24μm, L=0.18μm), the mismatch threshold voltage is approximately $24mV$ ($A_{VT} \approx 5mV\mu m$). This leads to an amount of $0.01fC$ differential charge injected to the sampling capacitor. This creates a $3\sigma_{offset}$ of $6\mu V$ at the input of first integrator. (Sampling capacitor is $5pF$). The accuracy requirement of ΔV_{BE} is 2.3μV. To reduce the residual error to the level of accuracy required, the system level chopping is used.

From above, it is evident that the residual offset is due to charge injection spike in the switches used for CDS and charge injection is directly proportional to sampling frequency(f_s). Residual offset can be reduced by adding another chopper switches which switch at much lower frequency (f_{chop}) than CDS frequency. This technique is known as system level chopping. The system level chopping periodically flips the polarity of charge injection spike introduced by the CDS switches. Now the residual offset is determined by the charge injection mismatch between the system level chopper switches. Since chopping frequency(f_{chop}) is lower than sampling frequency(f_s), the offset ideally is reduced by a factor of $\frac{f_s}{f_{chop}}$.The circuit that implements system level chopping for delta sigma modulator is as shown in Figure.5.24. System level chopping frequency should be higher than two times the bandwidth of the signal. It is assumed that the bandwidth will be very small , since temperature is a slowly varying signal . The system level chopping frequency is selected as 40Hz: four cycles of chopping in 800 delta sigma cycles. (Hand calculated residual offset= $6\mu V/200 = 30nV$).

5.7 Complete Modulator

The modulator which is implemented contains correlated double sampling and system level chopping to reduce input refered flicker noise and offset. The chopper implementation is as shown in Figure.5.25. At the input of the delta sigma, input is chopped by using a chopper switch. To keep the integrator sign correctly, the capacitor of each integrator is swapped using a pair of chopper switch. The output bit from quantizer is taken according to the value of the chop clock signal. The MUX is used for this purpose. The modulator is tested by the applying the

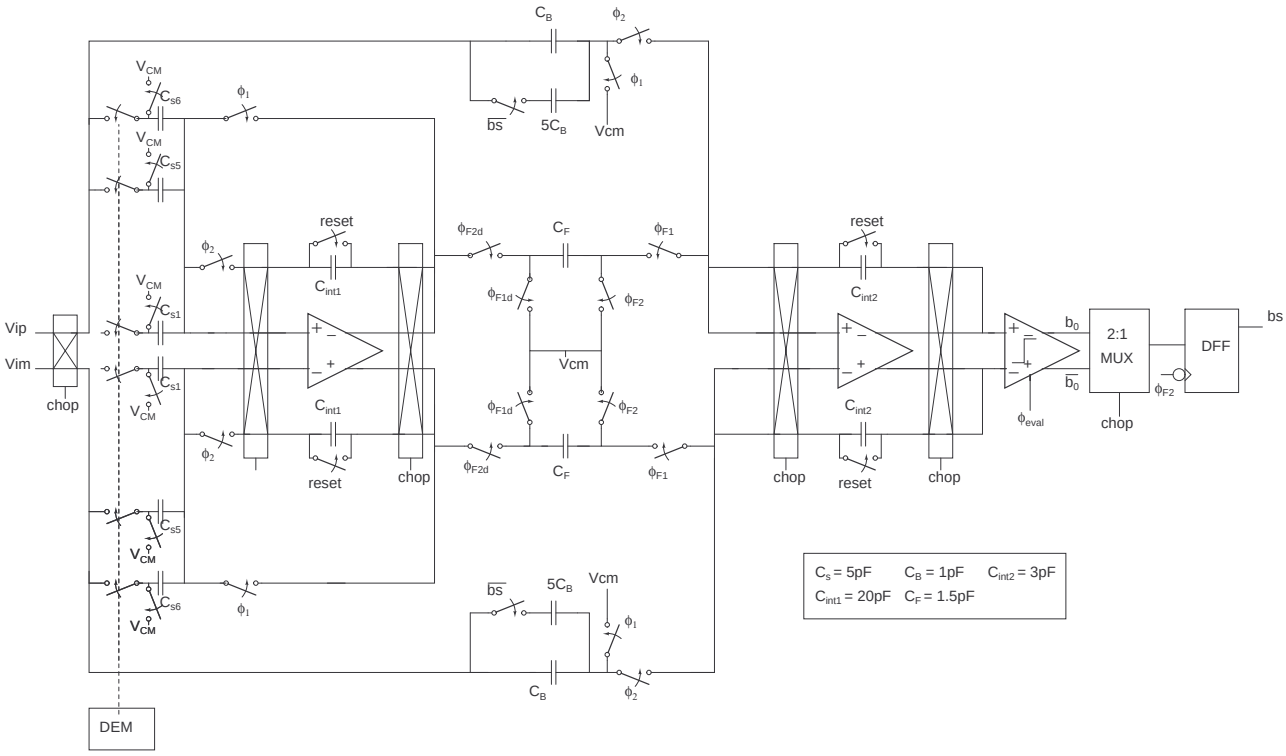


Figure 5.24: Second order delta sigma modulator.

dc value at the input and output bitstream is filtered by using $sinc^2$ decimation filter. The accuracy is measured by linear fitting the output with straight line and by finding the error between input and output. The SQNR obtained is 17.3bits. Four chopping cycles are used in one conversion cycle. So the offset is modulated to second zero of the decimation filter.

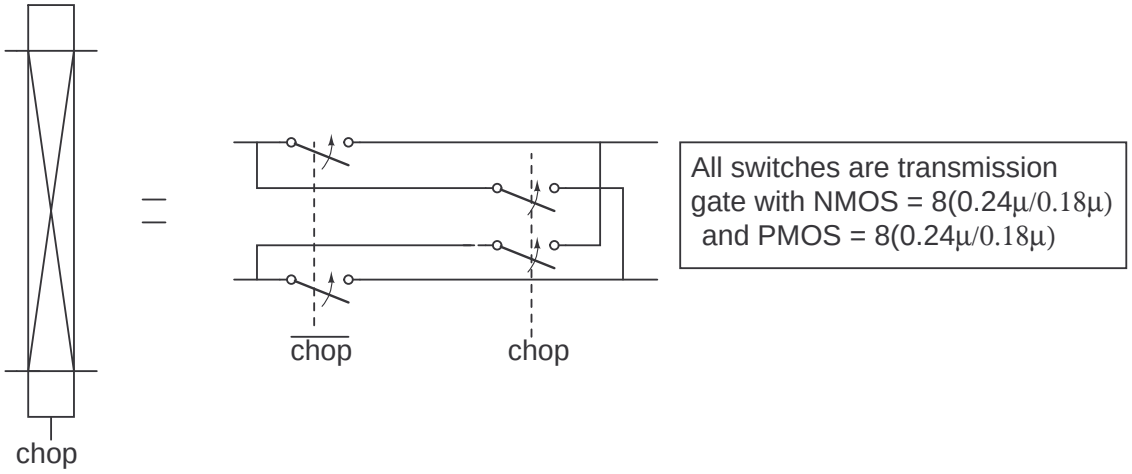


Figure 5.25: Chopper switching used for system level chopping.

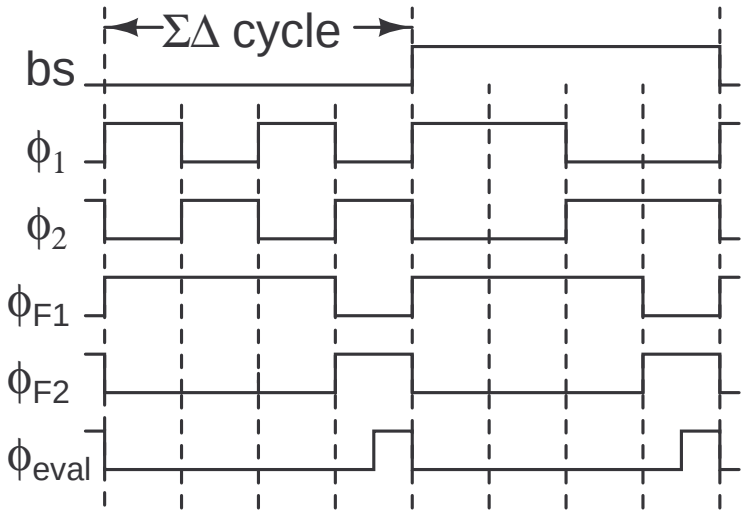


Figure 5.26: Timing of delta-sigma modulator.

CHAPTER 6

Complete system and the layout

The BJT-Core , β-independent bias generator and the delta sigma modulator are combined and formed the high precision CMOS based temperature sensor. The temperature reading is tested by simulating it at few sampling temperatures and confirmed the accuracy of the sensor. There exists non-linearity about 0.2^0C after curvature correction. This is corrected by a look up table. The value of non-linearity is stored in MATLAB and corrected after decimation filter. The output getting from the schematic level simulation is imported to MATLAB. The $sinc^2$ filter is used as decimation filter. The decimation filter is coded in the MATLAB. The bit-stream obtained is low pass filtered and corrected the output using look-up table and obtained the final reading. The layout of the analog blocks of the system is shown in Figure.6.1. All digital blocks are coded in verilog and synthesized using the tool Designvision. The synthesized netlist is placed and rooted by using the tool Encounter.

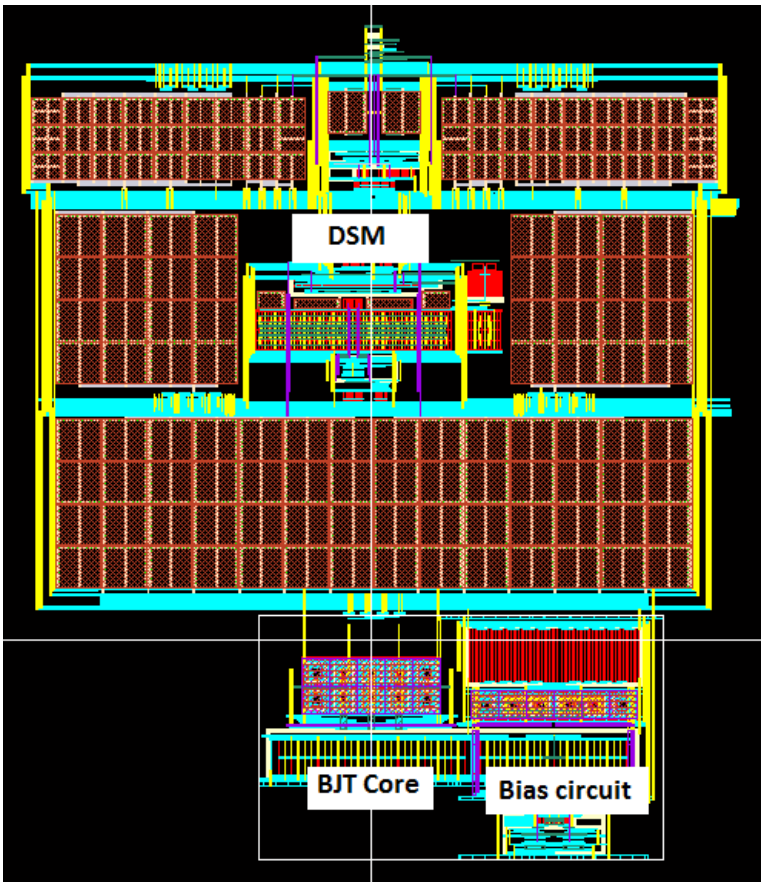


Figure 6.1: Layout of analog block.

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