CONTROL AND OPERATION OF UNIFIED POWER QUALITY CONDITIONER WITH BATTERY-ULTRACAPACITOR ENERGY STORAGE SYSTEM

A Project Report

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THESIS CERTIFICATE

This is to certify that the thesis titled **CONTROL AND OPERATION OF UNIFIED POWER QUALITY CONDITIONER WITH BATTERY-ULTRACAPACITOR ENERGY STORAGE SYSTEM**, submitted by **NAFIH MUHAMMAD I**, to the Indian Institute of Technology, Madras, for the award of the degree of **Master of Technology**, is a bona fide record of the research work done by him under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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ABSTRACT

KEYWORDS: UPQC; Battery-Ultracapacitor Hybrid; DC/DC Converters; Power Quality;

Power Quality (PQ) can be defined as a set of electrical boundaries that makes an equipment to function in its intended manner without significant loss of performance. UPQC has been widely studied by researchers to mitigate the disturbances propagated from source side and load side. It simultaneously mitigates the current disturbance in load side and voltage disturbance in source side. However it cannot compensate the voltage interruption because it has no energy storage devices connected in the DC link.

An ultracapacitor also referred to as supercapacitor stores charge in a double layer formed on a large surface area of micro porous materials such as activated carbon. The rate of discharge of ultracapacitor is faster than battery ranging from 0.3s to 30s. The lead acid rechargeable battery has high specific energy and a lower specific power compared to ultracapacitor. A combination of ultracapacitor and battery can take advantage of each kind of device to yield a power source which has both high power density and high energy density. Research on hybrid power sources shows that the combination of battery and ultracapacitor achieves a higher power capability and a longer run time compared to battery or ultracapacitor alone under a pulsed load condition.

The purpose of this thesis is to research the combined operation of UPQC and battery supercapacitor hybrid. This thesis proposes new configuration of UPQC that consists of battery and ultracapacitor connected to DC link through DC/DC converters for compensating the voltage interruption. The operation of proposed system was verified through simulations with Matlab/Simulink.

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ABBREVIATIONS

UPQC	Unified Power Quality Conditioner
SC	Super Capacitor
IEEE	Institute of Electrical and Electronics Engineers
IEC	International Electrotechnical Commission
PQ	Power Quality
APF	Active Power Filter
PI	Proportional and Integral
DC	Direct Current
PCC	Point of Common Coupling
VSI	Voltage Source Inverter
PWM	Pulse Width Modulation
THD	Total Harmonic Distortion
GTO	Gate Turn Off thyristor
SSCL	Solid State Current Limiter
SSCB	Solid State Circuit Breaker
SSTS	Solid State Transfer Switch
DSTATCOM	Distribution STATic COMpensator
DVR	Dynamic Voltage Restorer
CSI	Current Source Inverter
IGBT	Insulated Gate Bipolar Transistor
VA	Volt Ampere
DG	Distributed Generation
PLL	Phase Locked Loop
OCC	One Cycle Control
SOC	State Of Charge
DER	Distributed Energy Resources

NOTATION

v_α, v_β, v_0	Instantaneous voltages in $\alpha\beta 0$ frame, V
v_d, v_q, v_0	Instantaneous voltages in *dq0* frame, V
v_{ta}, v_{tb}, v_{tc}	Source terminal voltages in phase-a, b and c respectively, V
v_{sa}, v_{sb}, v_{sc}	Source voltages in phase-a, b and c respectively, V
v_{fa}, v_{fb}, v_{fc}	Series inverter voltages in phase-a, b and c respectively, V
v_{la}, v_{lb}, v_{lc}	Three phase load voltages, V
i_{sa}, i_{sb}, i_{sc}	Three phase source current, A
i_{fa}, i_{fb}, i_{fc}	Three phase shunt inverter current, A
i_{fn}	Shunt APF neutral current, A
C_f	Filter capacitance connected at load terminal, mF
i_{la}, i_{lb}, i_{lc}	Current drawn by connected load and C_f in phase-a, b and c respectively, A
$i_{la}^{'}, i_{lb}^{'}, i_{lc}^{'}$	Three phase current drawn by connected load, A
p	Instantaneous active power, W
q	Instantaneous reactive power, var
R_s, L_s	Feeder resistance and inductance, Ω, mH
R_f, L_f	Shunt inverter filter resistance and inductance, Ω, mH
L_{se}, C_{se}	LC filter inductance and capacitance of series APF, mH, μF
V_{dc}	DC link voltage, V
C_{dc}	DC link capacitance, μF
v_{a0}, v_{a1}, v_{a2}	Instantaneous symmetrical components in phase a, V
P_{lavg}	Average load power, W
V_{ta1}^{+}	Fundamental positive sequence component of terminal voltage, V
$-\theta_1$	Phase angle of fundamental positive sequence terminal voltage, rad
SOC_b, SOC_{sc}	SOC of battery and supercapacitor respectively
V_{batt}, V_{sc}	Voltage across battery and supercapacitor respectively, V
I_b, I_{sc}	Discharge current of battery and ultracapacitor respectively, A
L_b, C_b	Battery converter inductance and capacitance respectively, mH, μF
L_{sc}	Supercapacitor converter inductance, mH
Q	Maximum capacity of battery, Ah
V_{exp}, Q_{exp}	Exponential zone voltage and capacity of battery, V, Ah
V_{nom}, Q_{nom}	Nominal voltage and capacity of battery, V, Ah
V_{full}	Fully charged voltage of battery, V
Q_c	supercapacitor charge, C
I_{sd}	Self discharging current of supercapacitor, mA
ΔV	Over-potential, V
D	Duty cycle
V_l	Rated rms load voltage, V
θ	Angle to synchronize load voltage at interruption and source voltage, rad
h	Hysteresis band
ω	Frequency, rad/s

CHAPTER 1

INTRODUCTION

In the current scenario of power industry, both consumers and power suppliers are obliged to comply with different Power Quality (PQ) standards proposed by international bodies such as IEC and IEEE. Power Quality is defined as the concept of powering and grounding electronic equipment in a manner that is suitable to the operation of that equipment and compatible with the premise wiring system and other connected equipment in IEEE standard 1159-1995. IEC defined power quality as set of parameters defining the properties of power quality as delivered to the user in normal operating conditions in terms of continuity of supply and characteristics of voltage (frequency, magnitude, waveform and symmetry). Power quality (PQ) depends not only on the supply system but can be strongly affected by the end users selection of equipments and installation practices.

1.1 Electric Power Quality and Mitigation

There are two major classes of power quality problems namely problems due to low quality of current drawn by the nonlinear loads and voltage fluctuations that caused by faults in the power system. The most significant and critical power quality problems are voltage sags, voltage swells and current harmonics [4]. These problems cause tripping of sensitive electronic equipment with dangerous consequences in industrial plants where tripping of a critical equipment can cause the stoppage of the whole production with high costs associated. As more sensitive loads such as automation equipments, communication equipments and computers have come into wide use, the power quality becomes a very big issue in the utility company and customer. These equipments are sensitive to the source voltage disturbances, the fault or inadequate operation of these loads brings about huge losses [5],[6].

1.1.1 Custom Power Devices

To provide a flexible and active solution for PQ problems, many efforts have done from time to time. Among these PQ solutions lossless passive filters [7],[8] consists of L-C tuned component have been widely used to suppress harmonics. The advantages of passive filters over active filters are its low initial cost and high efficiency. On the other hand, it have various drawbacks such as fixed compensation, resonance with supply system and instability. To overcome these limitations active power filters (APF) [9],[10] have been widely used. APF has different configurations namely shunt, series and hybrid. Shunt APF is usually used for compensating current related distortions while series APF compensates voltage related distortions. Hybrid APF [11],[12] is used for filtering higher order harmonics. However it has a problem is that its rating is sometimes very close to load (up to 80% of load) in typical applications. PQ level cannot be obtained because of this reason.

To increase the reliability of distribution systems and mitigate the PQ problems, advanced power electronic controller devices have launched over last decades. The advent of power electronic devices has given birth to the custom power devices [13],[14]. Custom power devices uses power electronic controllers for power quality improvements on distribution systems. Their performance has been checked and demonstrated for isolated as well as grid connected distribution systems. Custom power devices are classified into network reconfiguring type and compensating type. The network reconfiguring type changes the configuration of the power system networks for PQ enhancement. Network reconfiguring type includes SSCL (Solid State Current Limiter) [15], SSCB (Solid State Circuit Breaker) [16] and SSTS (Solid State Transfer Switch) [17]. A pictorial representation of SSCL and SSTS are shown in Fig. 1.1(a) and Fig. 1.1(b) respectively [18]. SSCL uses a GTO that inserts an inductor in series with a power system network and limits the fault current, the inductor is removed from the circuit when the fault is cleared. SSCB is a protection device and it isolates the faulted circuit from the system. SSTS is used for rapid transfer of the load from a faulted line to an available alternative line to protect a sensitive load. The schematic diagram of SSTS is shown in . All of these are thyristor or GTO based devices.

The compensating type devices are mainly uses for load balancing, filtering, voltage regulation and power factor correction. The compensating devices include DVR

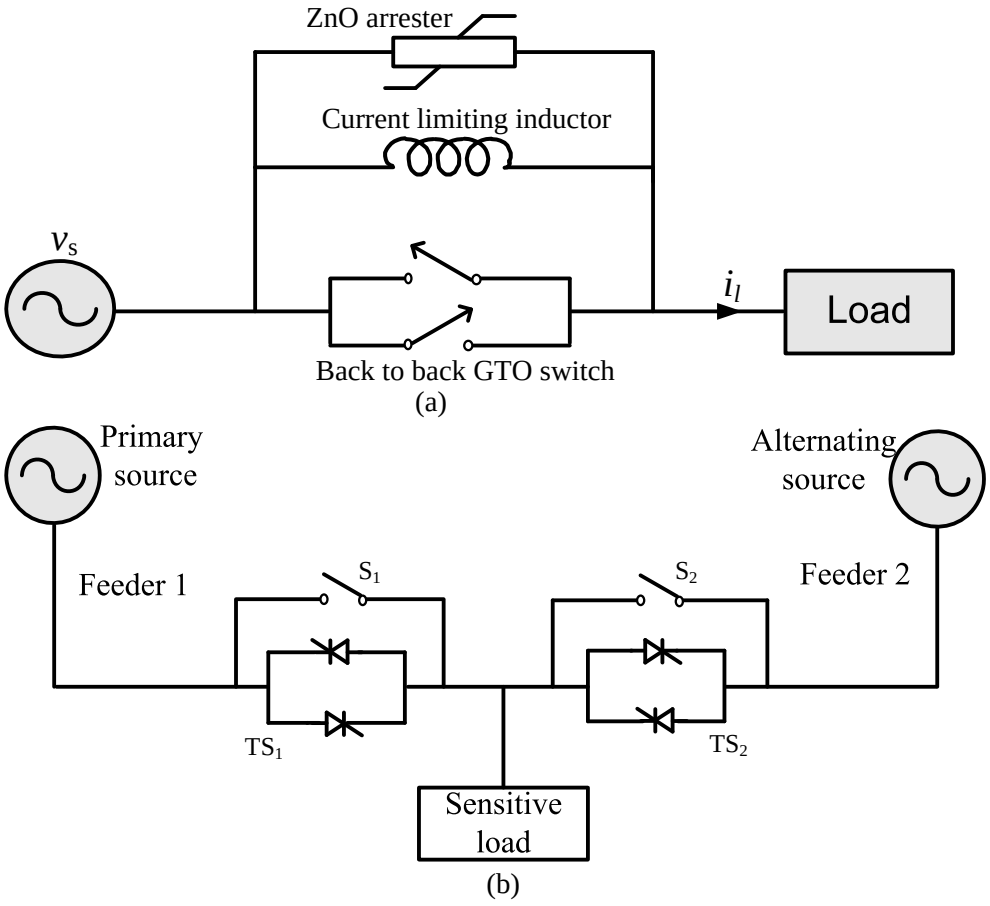

Fig. 1.1 Schematic diagram of : (a) SSCL (b) SSTS [18]

(Dynamic voltage restorer), DSTATCOM (Distribution Static compensator) and Unified power quality conditioner (UPQC). A DSTATCOM [19] configuration consists of a VSI , DC energy storage device (usually a capacitor) and a filter. Fig. 1.2(a) shows the schematic diagram of a DSTATCOM used for PQ problem compensation in a distribution system. In current control mode, DSTATCOM is used for elimination of current harmonics, power factor correction and compensation of reactive power of load. The DVR [20] is commonly used for voltage sag/swell mitigation, unbalanced voltage disturbance mitigation and elimination of voltage harmonics. The DVR uses the same blocks as the DSTATCOM, but in DVR the coupling transformer is connected in series with the ac supply system as shown in Fig. 1.2(b). The main functions of DVR are, compensation of voltage sag/swell, voltage regulation and unbalance voltage compensation. UPQC [21] uses for the mitigation of voltage and current related problems that could affect sensitive electrical loads, it also uses for compensating the load reactive power. It consist of both shunt and series active power filters for simultaneous compensation of current and voltage related PQ problems and load reactive power. The basic structure of UPQC is shown in Fig. 1.2(c).

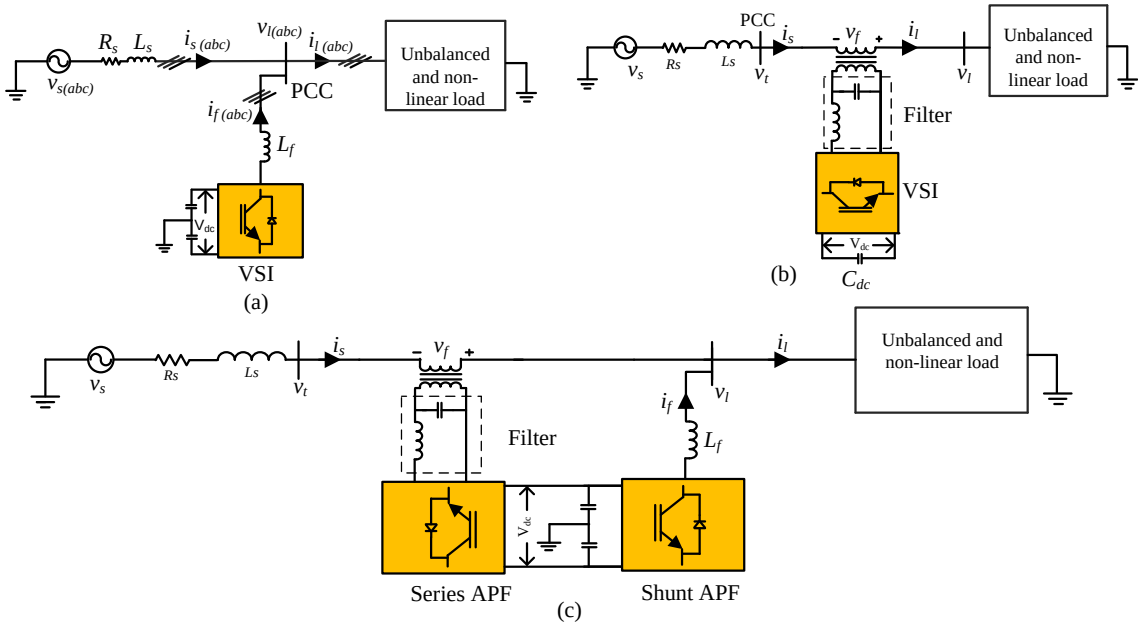

Fig. 1.2 Schematic diagram of compensating type custom power devices:
(a) DSTATCOM (b) DVR (c) UPQC.

1.2 Energy storage Devices

The way energy is stored in devices mainly depends on the source of energy. According to this, the following are the main methods of energy storage.

1.2.1 Chemical Energy Storage

Chemical energy is a form of potential energy, its storage depends on the source of energy. Hydrogen gas has potentials as a source of energy and it is primarily used as an energy storage medium for subsequent use. Examples are underground hydrogen storage which uses in the underground caverns, empty oil and gas fields to store grid energy for intermittent energy resources such as solar and wind energy.

1.2.2 Electrochemical Energy Storage

Electrochemical energy storage uses various devices which convert chemical energy into electrical energy. Examples include fuel cell and battery. Batteries are widely used devices that converts stored chemical energy into electrical energy. Two basic types of batteries are primary batteries or non-rechargeable batteries and secondary batteries or rechargeable batteries. Fuel cell converts chemical energy into electrical energy through

chemical reaction.

1.2.3 Electrical Energy Storage

In these kind of storage system, devices stores energy in its electric field. Examples include ultracapacitor, superconducting magnetic energy storage (SMES) and capacitor. Both ultracapacitor and capacitor are used to store electric charge, as its name reveals, ultracapacitor can store more electric charge than capacitor. Capacitor is used as a short time backup power, while ultracapacitor can also be used to power large systems including electric vehicles. SMES are relatively new technology which stores electric energy from the grid in its magnetic field created by the flow of current in a coil.

1.2.4 Thermal Energy Storage

It is a method that used to store thermal energy in order to use it to heat or cool buildings when the temperature inside is below or above the internal energy in the stored substance. Examples are storage heater, hot water storage tank and steam accumulator. Hot water storage tank are used to store hot water for washing, bathing, space heating etc. Storage heater is an electric heater that stores energy during the night or evening and releases the heat during day when the price of base load electricity is higher. Storage heaters accumulate heat in ceramic like materials. Steam accumulators uses a steel tank that contains steam under high pressure. It is used to balance supply and demand by accepting steam when the demand is less than supply and to release it when load demand exceeds the supply power.

1.2.5 Mechanical Energy Storage

Mechanical energy storage stores energy that is produced by motion including flywheel and hydraulic accumulator. Hydraulic accumulator is a kind of storage reservoir which stores non compressible fluid under pressure. The most widely used hydraulic accumulator is the compressed gas accumulator which store gas under pressure, usually nitrogen. Flywheel energy storage is used to store grid energy and energy generated by wind farms. It also shows potentials in transportation and as an emergency source of

power.

1.3 Problem Definition

UPQC is a device that can simultaneously mitigate source side voltage disturbance and load side current disturbance. UPQC can compensate voltage sag/swell, current harmonics and harmonic voltage, and it can control the reactive power supplied by the source. However, it cannot compensate the voltage interruption because it has no energy storage devices connected to its DC link. The commonly used storage device is lead acid batteries, it possess low power density. The battery charge and discharge are slower and hence, it is not suitable for highly fluctuating load demand. The super capacitors are becoming popular for its high power density compared to battery and it can respond very quickly to high fluctuating power. But, the low energy density of super capacitor makes it not suitable to supply the average load demand for longer time.

A combination of ultracapacitor and battery can take advantage of each kind of energy storage devices to yield a power source having high power density and high energy density. This project proposes a new configuration of UPQC that consists of the DC/DC converters and the battery supercapacitor hybrid for compensating the voltage interruption. The DC/DC converter is used to actively control the power flow between battery, ultracapacitor and the UPQC DC link, thereby enhancing the power capability of the system.

1.4 Objectives and Scope

The project involves the design of UPQC with battery ultracapacitor hybrid, modelling of controllers associated with different components and control strategy to share power between two energy storage devices and UPQC. Thus compensating grid voltage interruptions along with reduced battery stress and extended energy storage devices life are the major considerations. The objectives of this project are listed below.

- To control the charging and discharging of battery and ultracapacitor during normal voltage (0.9 pu to 1.1 pu), voltage sag and voltage swell conditions.

- To study the operation of UPQC with unbalanced non linear load and battery ultracapacitor hybrid during normal voltage,voltage sag and swell.
- To control Battery ultracapacitor hybrid energy storage system during grid voltage interruption and to relieve stress on the battery during load fluctuations for improving battery life.

1.5 Organisation of Thesis

Chapter 2 presents the literature review. Various power quality problems, UPQC topologies and control strategies, battery ultracapacitor hybrid and advantages of using DC/DC converter for battery ultracapacitor hybrid are discussed in detail.

Chapter 3 describes design, modelling and control of UPQC. The series APF and shunt APF are controlled in voltage control and current control mode respectively.

In **Chapter 4**, the design and modelling of battery and ultracapacitor are explained in detail. The Matlab/Simulink library model of battery and ultracapacitor are used for the simulation study. This chapter discussed the various parameters considered for modelling of battery and ultracapacitor.

Chapter 5 proposes a UPQC configuration with battery ultracapacitor hybrid energy storage system. The control of UPQC, battery and ultracapacitor during different voltage disturbances are explained. The operation of UPQC in grid connected mode and voltage interruption condition are explained in detail.

Chapter 6 discusses simulation results. The performance of UPQC and battery ultracapacitor hybrid energy storage system are verified with the help of simulation results.

Chapter 7 discusses the conclusions and future scope of work.

CHAPTER 2

LITERATURE REVIEW

Power quality (PQ) has significant influence on high technology equipments related to automation, communication, precise manufacturing technique, online services and advanced control. Majority of the distributed generations (DG) from renewable energy sources are connected to the grid through power electronic devices, which introduce additional harmonics especially switching harmonics in the distribution systems. Research is being carried out to integrate active filtering devices especially the combination of shunt and series devices to mitigate a variety of PQ problems by using a single device.

For a generalized solution, UPQC could be the most effective PQ protecting device for sensitive non linear loads, which draws harmonic current and require quality input supply. Also, harmonics in the load current should be isolated to ensure the quality of the supply current. Battery and ultracapacitor are the two effective energy storage devices that can be used with UPQC, for enabling UPQC to work under voltage interruptions. Ultracapacitor reduces the stress on the battery, thus improving the life of battery. Different power quality terms, UPQC configurations and control methods, the idea of combining two different storage elements, the choice of devices and the previous attempts made towards it are briefly described in this chapter.

2.1 Introduction to Power Quality

Most of the power apparatus made over a decade back could operate normally with wide variations of voltage, frequency and current. However, equipment developed in recent years is generally not that tolerant to these variations because of the increased use of power electronic switches and electronic controllers. Hence, power system disturbances, which were tolerated earlier, may now cause disturbances to industrial power system with a huge loss of production and this could be substantial with greater stress

on quality and productivity of products. In a developing country like India, PQ is of prime importance considering the need for energy conservation.

2.1.1 Power Quality Problems

The power quality problems can be put under the following main categories.

- Voltage dip or sag
- Voltage swell
- Voltage fluctuations and flicker
- Voltage interruptions
- Harmonics
- Unbalances
- Transients
- Commutation notches
- Electric noise

PQ parameter variations fall into three main categories namely transient disturbances, momentary disturbances and steady state disturbances. Transient disturbances include oscillatory transients, localized faults, unipolar transients and other events typically lasting less than 10 ms. Momentary disturbances, on the other hand are voltage swell/sag lasting more than 3 ms but less than 3 sec. Steady state disturbances are deviations lasting more than 3 sec.

2.1.2 Power Quality Terminology

More commonly used power quality terms [22] are defined and explained below.

2.1.2.1 *Flicker*

Flicker can be expressed as the change in voltage over nominal voltage expressed as a percent. Any load that has significant time variations, especially in the reactive power, can cause voltage fluctuations. The term flicker is derived from the impact of the voltage

fluctuation on lighting intensity. Voltage fluctuation is an electromagnetic phenomenon and flicker is an undesirable effect of that phenomenon.

2.1.2.2 *Power frequency*

Frequency variation is extremely rare in power grids. Frequency variations occur systems with standby diesel generators. Modern SMPS is frequency tolerant, and are generally not affected by small frequency shifts. Frequency variations are very dangerous in systems with motors, because it changes the angular speed of motor and other parameters like torques and power. The magnitude of the frequency shift and its duration mainly depends on the system load characteristics and the response of the power generation system to load changes.

By standard EN 50160, frequency in the systems with synchronous connection to an interconnected system has to be in range as given below.
$\pm 1\%\,(49.5 - 50.5\,\text{Hz})$ for 99.5% of a year
$-6\%/+4\%\,(47 - 52\,\text{Hz})$ for 100% of the time
In the systems with no synchronous connection to an interconnected system frequency has to be in range as given below.
$\pm 2\%\,(49 - 51\,\text{Hz})$ for 99.5% of a year
$\pm 15\%\,(42.5 - 57.5\,\text{Hz})$ for 100% of the time.

2.1.2.3 *Voltage sag*

Sag is a decrease in rms voltage or current at the power frequency for durations from 0.5 cycles to 1 minute [22]. Voltage sags are usually associated with system faults, starting of heavy motors and switching of large loads. Fault on a parallel feeder circuit results in a drop in the bus voltage which affects all the nearby healthy feeders until the fault is cleared. In PQ problems, the term sag is using to describe a short duration voltage decrease. The IEC definition for this phenomenon is dip. Sag duration is subdivided into three categories, namely, instantaneous, temporary and momentary, which coincide with the three categories of swell and interruption.

2.1.2.4 *Voltage swell*

Swell is an increase in rms voltage or current at the power frequency for durations from 0.5 cycles to 1 min [22]. Typical values are $1.1 - 1.8$ pu. Voltage swells are associated with system faults but they are much less common than voltage sags. The main causes of voltage swells are a single line to ground fault, a large load switching OFF and a large capacitor bank switching ON.

2.1.2.5 *Momentary interruption*

Momentary interruption is the complete loss of voltage (<0.1 pu) on one or more phase conductors for a time period between 0.5 cycles and 3 sec [22]. Momentary interruptions on power utility systems occur due to automatic circuit reclosings which are used to clear temporary faults on the system, mechanical transfer switches, poor intermittent connections used and faults adjacent to the load which dip the voltage to zero volts.

2.1.2.6 *Sustained interruption*

When decrease in source voltages occur (<0.1 pu) for more than 1 minute, it is considered as a sustained interruption. A sustained interruption is in the category of a long duration voltage disturbances. Sustained interruptions are specific power system phenomena and have no relation to the term outage. Outage does not refer to a specific phenomena, but rather to the state of a component in a system that has failed to function as expected [22]. A loss of service means that no source voltage is present where as interruption implies that a small but inconsequential (< 0.1 pu) of voltage may remain on the incoming transmission lines.

2.1.2.7 *Temporary interruption*

The complete loss of voltage (<0.1 pu) on one or more phase conductors for a time period between 3 s to 1 minute is considered as a temporary interruption. Fig. 2.1 shows the different voltage variations, distributed based on the duration of voltage variations.

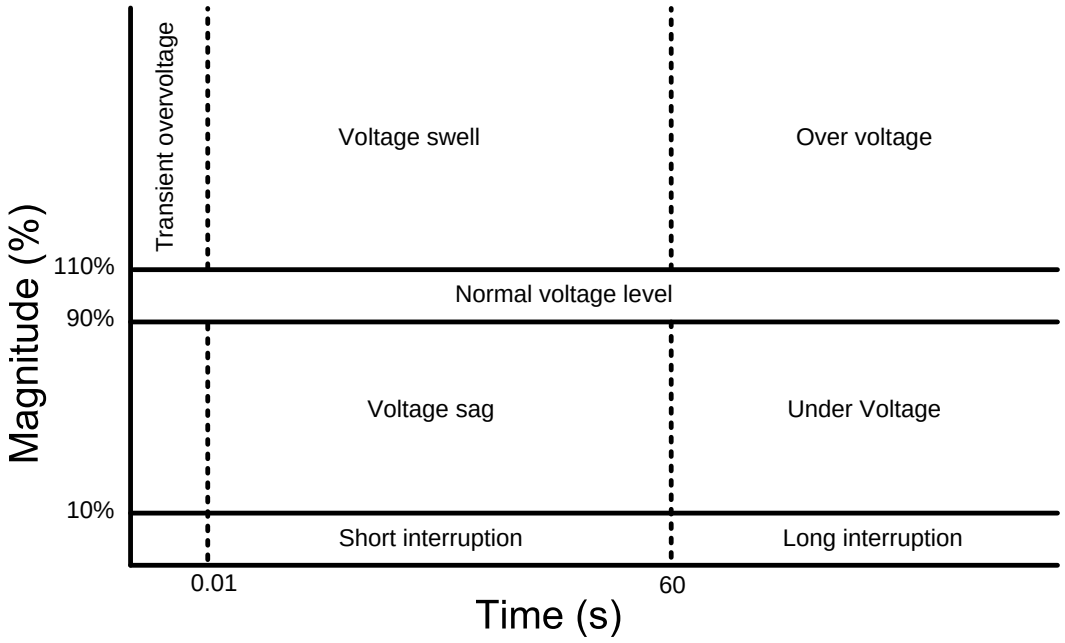

Fig. 2.1 Distribution of voltage problems.

2.1.2.8 *Voltage unbalance*

Voltage unbalance (or imbalance) is defined as the ratio of the negative or zero sequence component to the positive sequence component [22]. The negative or zero sequence voltages in a power system generally result from unbalanced loads, faults in one or two lines and capacitor bank irregularities.

2.1.2.9 *Harmonics*

Harmonics are sinusoidal currents or voltages having frequency components that are integer multiples of the frequency at which the system is designed to operate (termed the fundamental component, in India it is 50 Hz). Harmonics combine with the fundamental current or voltage produces waveform distortion. Harmonics exists due to the nonlinear characteristics of devices and loads used in the power system. Voltage distortion results due to nonlinear voltage drops across the feeder impedances by harmonic currents. Harmonic distortion is a growing concern for many customers and utilities due to increasing application of power electronics equipment.

2.1.2.10 *DC offset*

DC offset is the presence of a DC current or voltage in an ac power system. Direct current in alternating current networks affects the system adversely due to an increase in transformer saturation and additional stress on insulation.

2.1.2.11 *Interharmonics*

Interharmonics are currents or voltages having frequency components that are not integer multiples of fundamental frequency. The main sources of interharmonic distortion are cyclo-converters, static frequency converters, arcing devices and induction motors. The IEC places background noise phenomenon in the interharmonic category.

2.1.2.12 *Transient*

Transient is designating a quantity or a phenomenon which varies rapidly between two consecutive steady states for short time interval. A transient can be a unidirectional impulse of either polarity or a damped oscillatory wave with the first peak occurring in either polarity. Transients can be classified into two main categories, impulsive and oscillatory. An impulsive transient is a sudden non power frequency change in the steady state condition of current, voltage or both, that is unidirectional in polarity. The most common cause of impulsive transients is lightning. An oscillatory transient is similar to impulsive transient except that the former has both positive and negative polarities.

2.1.2.13 *Notching*

Notch is mainly a switching disturbance of the normal power system voltage waveform lasting less than 0.5 cycles which is initially of opposite polarity than the waveform and is thus subtracted from the normal waveform in terms of the peak value of the disturbance voltage [22]. Notching can occur due to current commutation from one phase to another, three phase converters that produce continuous DC currents may cause voltage notching. Voltage notching represents a special case that falls between transients and harmonic distortion.

2.1.2.14 *Noise*

Noise is defined as an unwanted electrical signals with broadband spectral content lower than 200 kHz superimposed upon the power system current or voltage in phase conductors, or found on neutral conductors or signal lines. Arcing equipment, power electronic devices, control circuits and switching power supplies can cause noise in the power system. Noise consists of any unwanted distortion of voltage or current that cannot be classified as harmonic distortion or transients.

2.2 Unified Power Quality Conditioner (UPQC)

PQ issues are becoming more and more significant in these days because of the large number of power electronic devices and switches that behave as nonlinear loads. Many solutions to PQ problems are available for both the operator and the end user. The shunt APF is usually connected across the loads to compensate for all current related problems such as the reactive power compensation, power factor correction, load unbalance compensation and current harmonic compensation. The series APF is connected in series with the line through series injection transformer. It acts as controlled source of voltage and can compensate all voltage related problems such as voltage sag, voltage harmonics, flicker and voltage swell. UPQC is a custom power device that consists of both series APF and shunt APF. UPQC system can be divided into two sections, namely the control unit and the power circuit. Control unit includes voltage and current disturbance detection, reference signal generation, gate pulse generation and voltage/current measurements. Power circuit consists of two VSI, standby and system protection systems, injection transformers and harmonic filters.

The findings of the comprehensive literature survey summarize the available studies related to power circuit and control unit of UPQC.

2.2.1 Power Circuit Topologies of UPQC

UPQC is relatively a new member of the custom power devices family. It is a combination of series and shunt compensator. UPQC can be used for compensating supply

voltage flicker, voltage sag, swell, load reactive power, voltage and current unbalance and harmonics in voltage and current. In other words, UPQC has the capability of correcting the current and voltage related problems at the point of installation on power systems . The UPQC therefore is expected to be one of the most powerful equipment to mitigate all the power quality issues.

Fig. 2.2 shows the power circuit of the neutral clamped VSI topology based UPQC which uses split capacitor as DC link. In this figure, v_{sa}, v_{sb}, v_{sc} are the source voltage of phase a, b and c respectively. Similarly, v_{ta}, v_{tb} and v_{tc} are the terminal voltages (supply voltage after voltage drop in the feeder impedance), v_{fa}, v_{fb} and v_{fc} are the voltage injected by the series APF. v_{la}, v_{lb} and v_{lc} are the three phase load voltages. The three phase source currents are represented by i_{sa}, i_{sb} and i_{sc}, load currents are i_{la}, i_{lb} and i_{lc}. The shunt APF currents are denoted by i_{fa}, i_{fb} and i_{fc} and i_{ln} is the current in the load neutral wire. L_s and R_s represent the feeder inductance and resistance respectively. C_{sh} is the shunt filter capacitor, L_f and R_f are shunt APF filter inductance and resistance respectively. The filter inductance and capacitance of the series APF are represented by L_{se} and C_{se} respectively. The load includes both linear and nonlinear loads. The DC link capacitance and voltages across them are represented by $C_{dc1} = C_{dc2} = C_{dc}$ and $V_{dc1} = V_{dc2} = V_{dc}$ respectively.

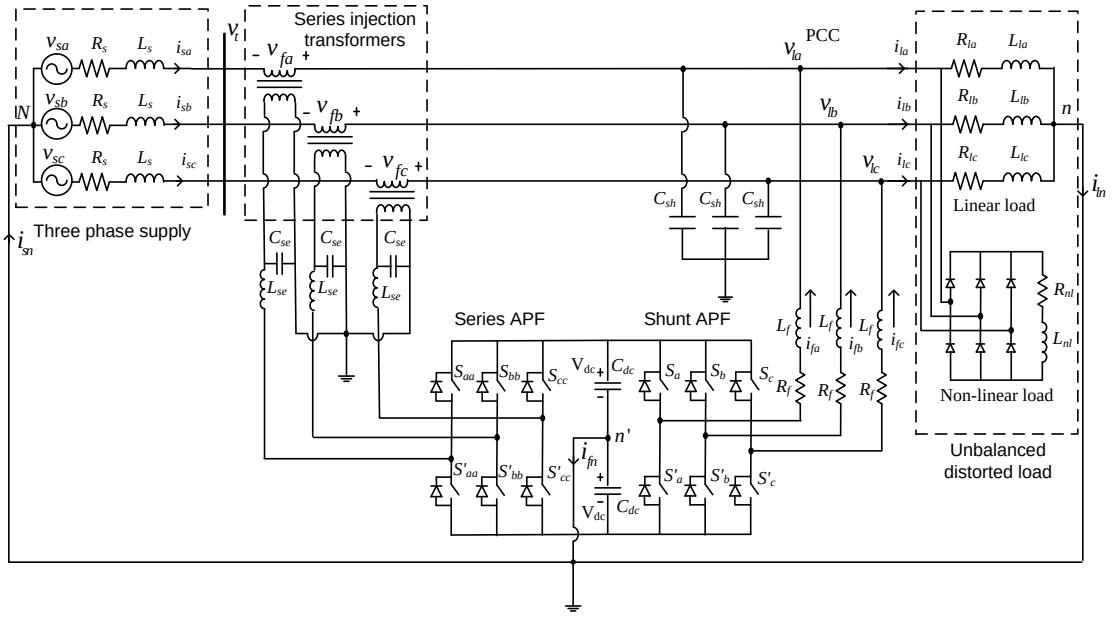

Fig. 2.2 Power circuit of three phase UPQC.

The UPQC consists of two voltage source inverters, which are connected back to back with a common DC energy storage capacitor. One of these two VSIs is con-

nected in series with the feeder called series APF and the other is connected in parallel (shunt APF) to the same feeder. The shunt APF tackles the current related problems, whereas, the series APF is the most suitable to mitigate the voltage related problems. Since the modern distribution system demands a better power quality, installation of these APFs has greater scope in distribution systems. However, installing two separate APFs to compensate current and voltage related PQ problems independently may not be a cost effective solution. The back to back inverter system configuration came into attention when Fujita and Akagi [23] proved the practical application of UPQC topology with experimental results. They named this device as unified power quality conditioner (UPQC) and since then the name UPQC has been popularly used by majority of the researchers. The back to back converter topology has been also addressed as series-parallel converter [24], unified active power filter (UAPF) [25], universal active power line conditioner [26], universal power quality conditioning system (UPQS) [27], universal active filter [28], and so forth.

UPQC is similar to a unified power flow controller (UPFC) [29] in construction. A UPFC is employed in power transmission system whereas UPQC is employed in a power distribution system and it perform shunt and series compensation simultaneously. However, a UPFC only needs to provide balance series and/or shunt compensation. Since the transmission network generally operates under a balanced and distortion free environment. On the other hand, a power system distribution network may contain distortion, DC components, and unbalance both in voltages and currents. Therefore, a UPQC should operate under this environment while performing series and/or shunt compensation. The main components of UPQC are as follows.

- A VSI which is connected across the load (at the PCC) and acts as a shunt APF and another VSI in series with the line (through an injection transformer) which acts as a series APF.
- Shunt coupling inductor L_f is used to interface the shunt inverter to the network. It also helps in smoothing the inverter current. Some configurations uses an isolation transformer to electrically isolate the shunt inverter from the network.
- A common DC link (L_{dc} or C_{dc}) that is formed by using an inductor or a capacitor (usually capacitor is used). In Fig. 2.2, the DC link is realized using a capacitor which interconnects the two inverters and also maintains a constant DC bus voltage across it.
- A LC low pass filter (LPF) is connected to the output of series APF to eliminate switching harmonics from the inverter output voltage. A small resistor can be used in series with inductor to provide sufficient damping to voltage oscillations.

- A Series injection transformer with suitable turns ratio is used to connect the series APF in the network.

In principle UPQC is an integration of series and shunt APF with a common DC bus. The shunt APF of UPQC is controlled in current control mode such that it delivers a current (I_f) which follows the current reference given by the UPQC control algorithm. Usually the shunt inverter is used to maintain DC link voltage at the reference value. In order to cancel out the harmonics generated by nonlinear load, the shunt APF reference current can be calculated as,

$$i_f^* = i_l - i_s^*$$

where i_f^*, i_s^* and i_l represent the shunt inverter reference current, reference source current and load current respectively.

Similarly, the series inverter of UPQC is controlled in voltage control mode such that it injects a voltage in series with the terminal voltage to achieve a sinusoidal, distortion free voltage with desired magnitude (rms) at the load terminal. The operation of series APF can be represented by the following equation.

$$v_f^* = v_l^* - v_t$$

where v_f^*, v_l^* and v_t represent the series inverter reference voltage, reference load voltage, and actual source terminal voltage respectively.

Fig. 2.3 shows a pictorial view for the classification of UPQC [30]. The UPQC classification can be based on the physical structure and voltage sag compensation approach used.

2.2.1.1 *Classification based on the converter topology*

Generally the shunt inverter is responsible to regulate the DC link at reference value. The UPQC can be developed using a current source inverter (CSI) [31] that shares a common energy storage inductor L_{dc} to form the DC link. Fig. 2.4 shows single line representation of a CSI based UPQC system configuration.

VSI based configuration is the most common and popular converter topology for

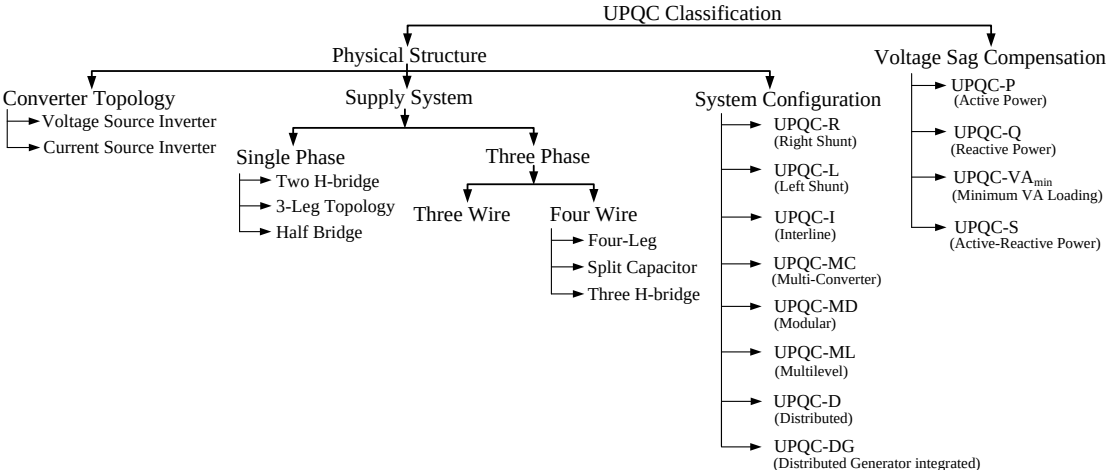

Fig. 2.3 Classification of UPQC.

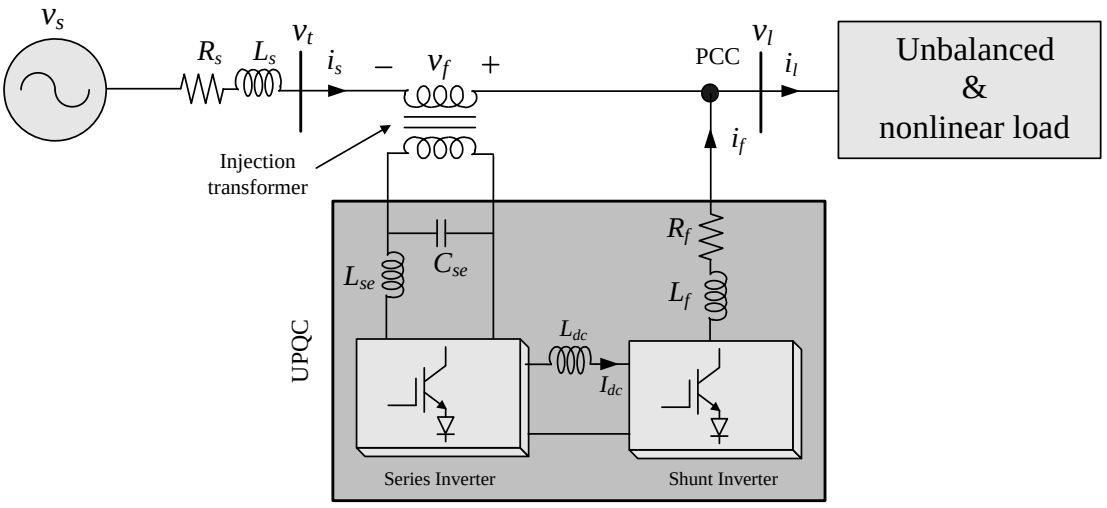

Fig. 2.4 CSI based UPQC system configuration.

UPQC that shares a common energy storage capacitor C_{dc}. Single line representation of a VSI based UPQC system configuration is shown in Fig. 2.5. The VSI based topology is dominantly used in almost all the reported work on the UPQC. Some of the advantages offered by voltage source inverter topology over current source inverter includes cheaper, lighter in weight, no need of blocking diodes, flexible overall control and capability of multilevel operation.

2.2.1.2 *Classification based on the supply system*

Both 1-ϕ and 3-ϕ systems has similar kind of voltage related PQ problems except an additional voltage unbalance compensation needed in the case of a 3-ϕ system. The current harmonics and the load reactive current are the major issues in 1-ϕ system. In the case of 3-ϕ three wire (3ϕ3W) system, current unbalance are also comes into picture.

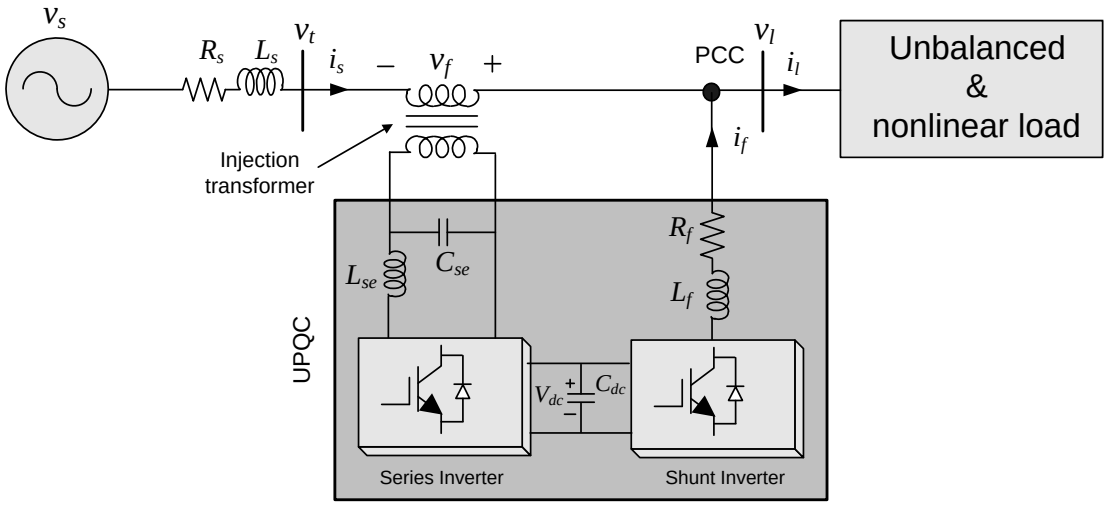

Fig. 2.5 VSI based UPQC system configuration.

The 3-ϕ four wire (3ϕ4W) system requires an additional neutral current compensation control. Fig.2.6(a) shows the most popular UPQC system configuration to compensate the PQ problems in 1-ϕ two wire (1ϕ2W) supply system consisting of two H-bridge inverters [32]. Nasiri and Emadi introduced two configurations for 1-ϕ UPQC [33],

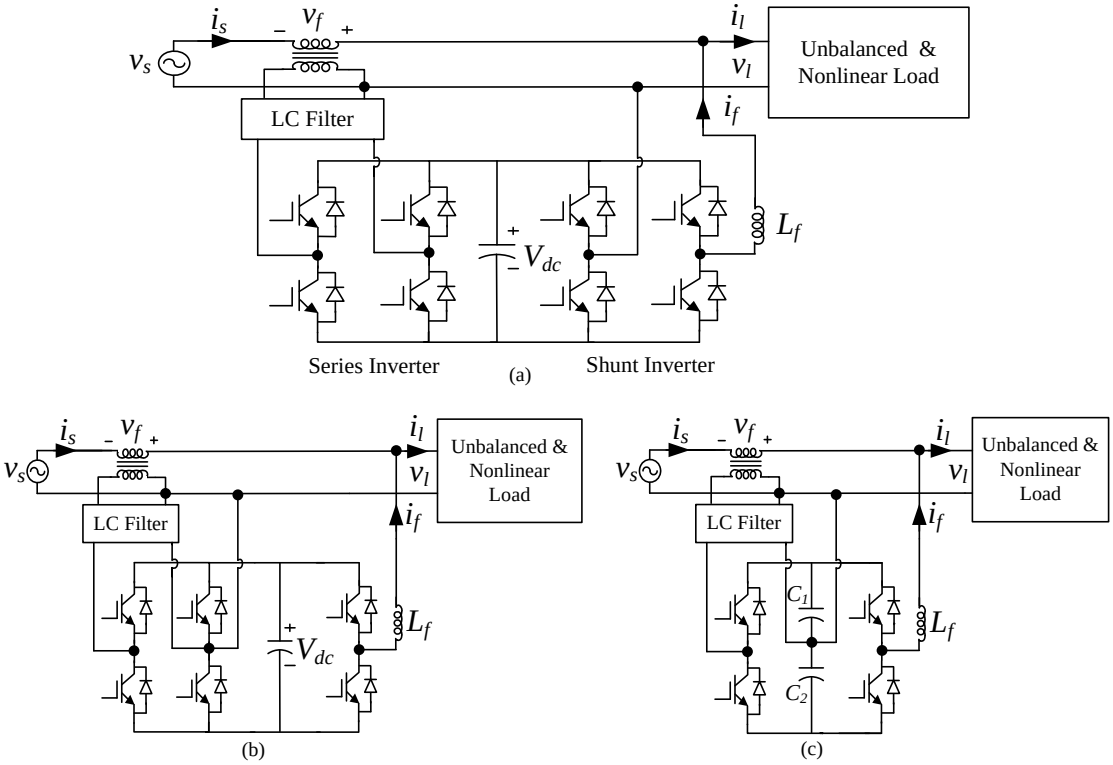

Fig. 2.6 1ϕ2W UPQC: (a) Two H-bridge configuration (b) Three leg configuration (c) Half bridge configuration.

namely, three leg 1-ϕ UPQC shown in Fig. 2.6(b) and half bridge 1-ϕ UPQC shown in Fig. 2.6(c). These topologies are useful for low cost low power applications.

Several nonlinear loads such as, current regulator, adjustable speed drives fed from 3ϕ3W, arc welding machines, frequency converters, and arc furnaces impose combinations of PQ problems. A 3ϕ3W VSI based UPQC is shown in Fig. 2.7. Apart from the 3-ϕ loads many industrial plants often consist of combined loads such as, 1-ϕ loads and a variety of 1-ϕ loads supplied by 3ϕ4W sources. The neutral conductor demands an additional compensation requirement under unbalanced currents. To mitigate the neutral current problems in 3ϕ4W system, various shunt inverter configurations have been proposed by researchers such as, four leg, two split capacitor and three H-bridge topologies. Fig. 2.2 shows the 3ϕ4W UPQC based on split capacitor topology. Fig. 2.8

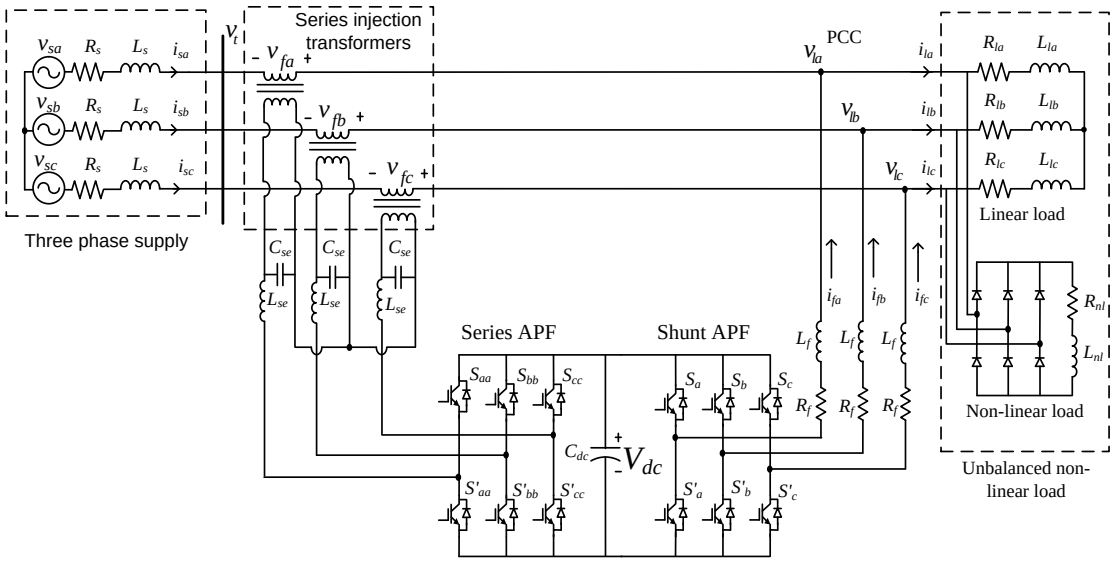

Fig. 2.7 Power circuit of 3ϕ3W UPQC.

shows the 3ϕ4W UPQC based on four leg shunt inverter and Fig. 2.9 shows H-bridge based 3ϕ4W UPQC.

In split capacitor topology, the voltages across both the capacitor should be equal to avoid the flow of circulating current. This requires an additional control algorithm for DC link capacitor voltage regulation. In four leg topology, the load neutral current is compensated by using an additional leg (two semiconductor switches). The four leg topology may offer better control over neutral current compared to other topologies due to the dedicated fourth leg. The three H-bridge topology consists of three units of 1-ϕ H-bridge inverters connected to the same DC link of the UPQC. These three H-bridges can use for shunt inverter or series inverter.

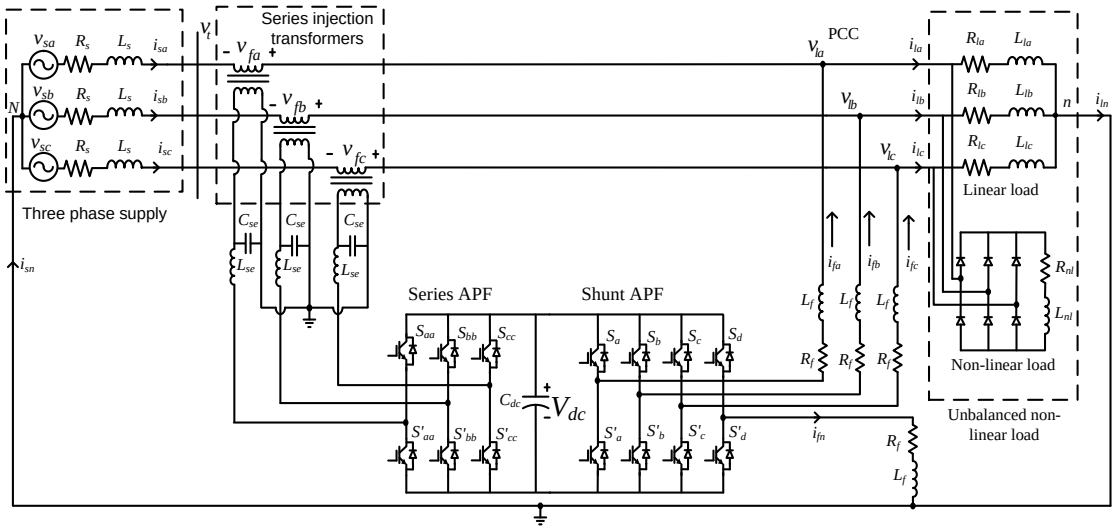

Fig. 2.8 3ϕ4W UPQC based on four leg shunt inverter topology.

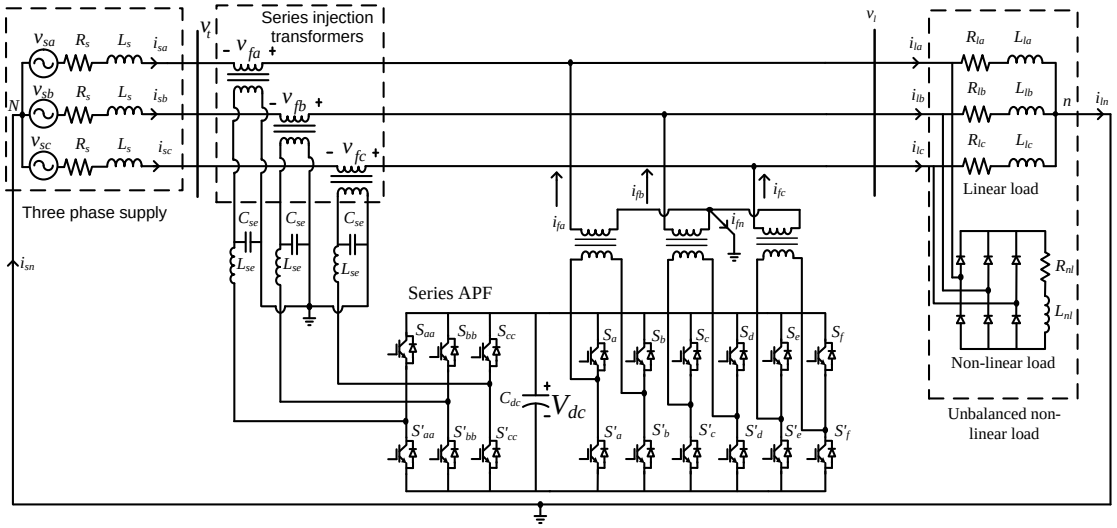

Fig. 2.9 3ϕ4W UPQC based on H-bridge shunt inverter topology.

2.2.1.3 *Classification based on the UPQC configuration*

Based on the shunt inverter location (right or left) with respect to series inverter, UPQC can be classified as UPQC-R and UPQC-L [34]. Figs. 2.5 shows UPQC-R system configuration, while Fig. 2.10 shows UPQC-L configuration. Among two configurations, the UPQC-R is most commonly used by the researchers.

In Interline UPQC (UPQC-I) [35], two converters of the UPQC are connected between two distribution feeders. One of the converter is connected in series with one of the feeders while the other converter in shunt with second feeder as shown in Fig. 2.11(a). With such a configuration, both the feeder voltages can be simultaneously regulated. Furthermore, the UPQC-I can manage and control the flow of real power between

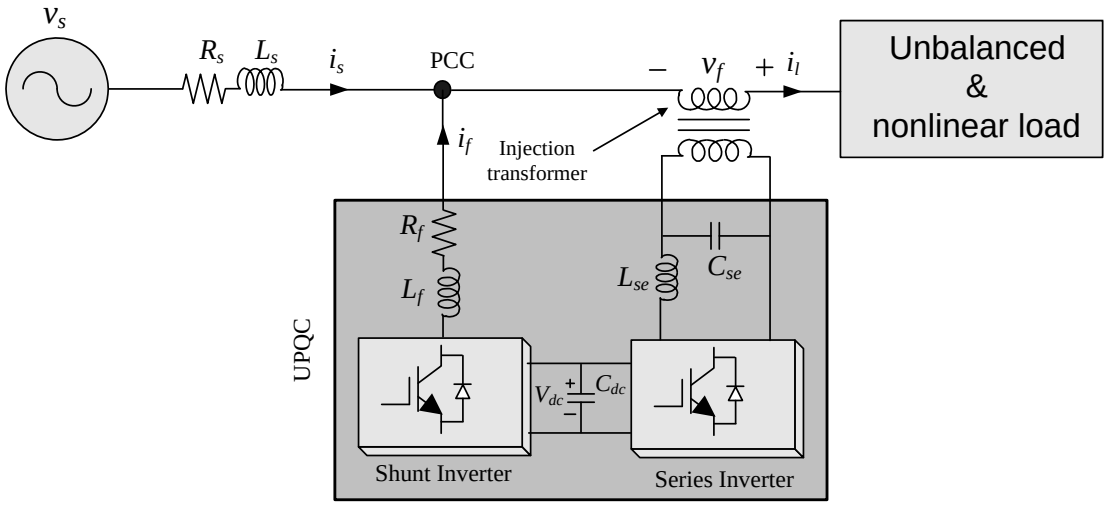

Fig. 2.10 Schematic diagram of left shunt UPQC.

the two feeders. The current related problems (such as unbalance and harmonics) could be effectively compensated only on the shunt inverter connected feeder. Alternatively, the harmonics in the voltages can only be mitigated in the feeder in which the series inverter is connected. Researchers have explored the possibilities for improving the

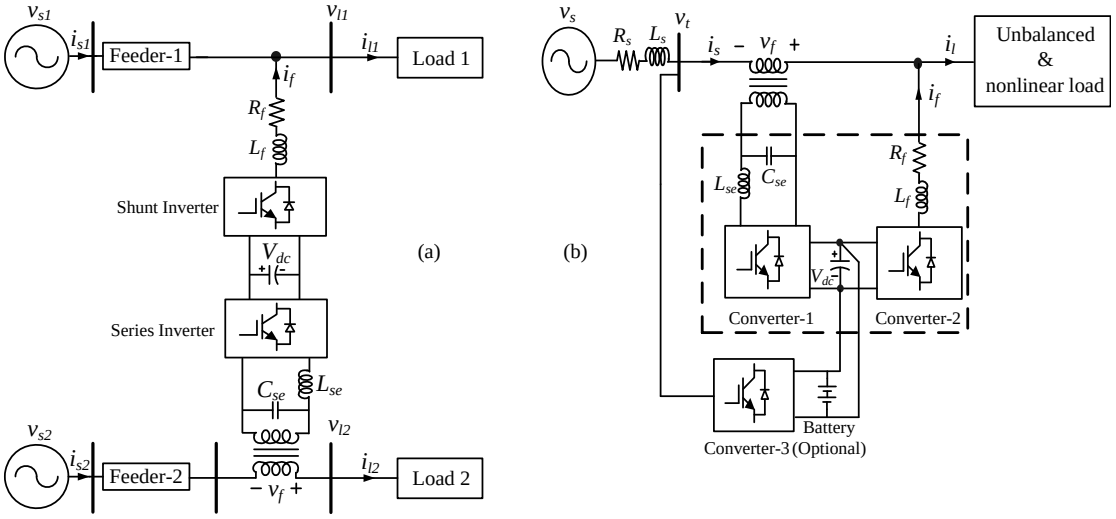

Fig. 2.11 UPQC configurations: (a) Interline UPQC (b) Multi-converter UPQC.

power system performance by considering a third inverter unit to support the DC link. To further enhance the system performance, the use of an ultracapacitor or storage battery can be used. The third converter can be connected in many ways, for example, in parallel with the same feeder [36] or in series/parallel with the adjacent feeder [37] and is named as multi-converter UPQC (UPQC-MC). In MC-UPQC, the third converter is connected in series with the adjacent feeder. Similar to UPQC-I, the UPQC-MC can be connected between two different feeders. Fig. 2.11(b) shows a multi converter UPQC

configuration in which three inverters are utilized to realize the UPQC system.

In [38] a modular UPQC (UPQC-MD) configuration is realized by using several H-bridge modules similar as connecting several 1-ϕ UPQCs in cascade in each phase. As the number of modules increase, the voltage across each module decreases, thus it can be useful in the medium voltage application to achieve higher power levels. A multilevel UPQC (UPQC-ML) [39] uses multilevel converters, a three level topology requires double semiconductor devices as that of a two level UPQC system. A 3ϕ4W distribution system is generally realized by utilizing a $\Delta - Y$ transformer at the distribution level or by providing a neutral conductor along with the three power lines from substation. A new topology for 3P4W UPQC based distribution system is proposed in [40], in that it is possible to extend the UPQC based 3P3W system to a 3P4W system referred as 3P3W to 3P4W distribution UPQC (UPQC-D). The neutral of injection transformer, used in the series APF part of UPQC is considered as a neutral for 3P4W system. Thus, even if the power supplied by the grid is 3P3W, an easy expansion to 3P4W system can be achieved with this configuration. A fourth leg is added to the shunt APF of 3P3W UPQC to compensate the transformer neutral current and it can ensure zero current flow toward the neutral point. Thus, it is possible to maintain transformer neutral point at virtual zero potential.

Wind and solar energies are emerging as alternate sources of electricity. The UPQC can be integrated with one or many distributed generation (DG) systems. The system configurations thus, achieved is referred as UPQC-DG and is shown in Fig. 2.12. The DG power can be regulated and managed through UPQC to supply to the electrical loads connected to the PCC in addition to the current and voltage PQ problem compensation. Additionally, a battery can be connected to the DC link for energy storage, such that the excess DG generated power can be stored and used as backup. In the event of voltage interruption, the UPQC-DG system can act as a backup power source.

2.2.1.4 *Classification based on the voltage sag compensation approach*

The voltage sag on power system is considered as one of the most important and frequent PQ problem. The existing literature suggests four important methods to compensate the voltage sag in UPQC applications.

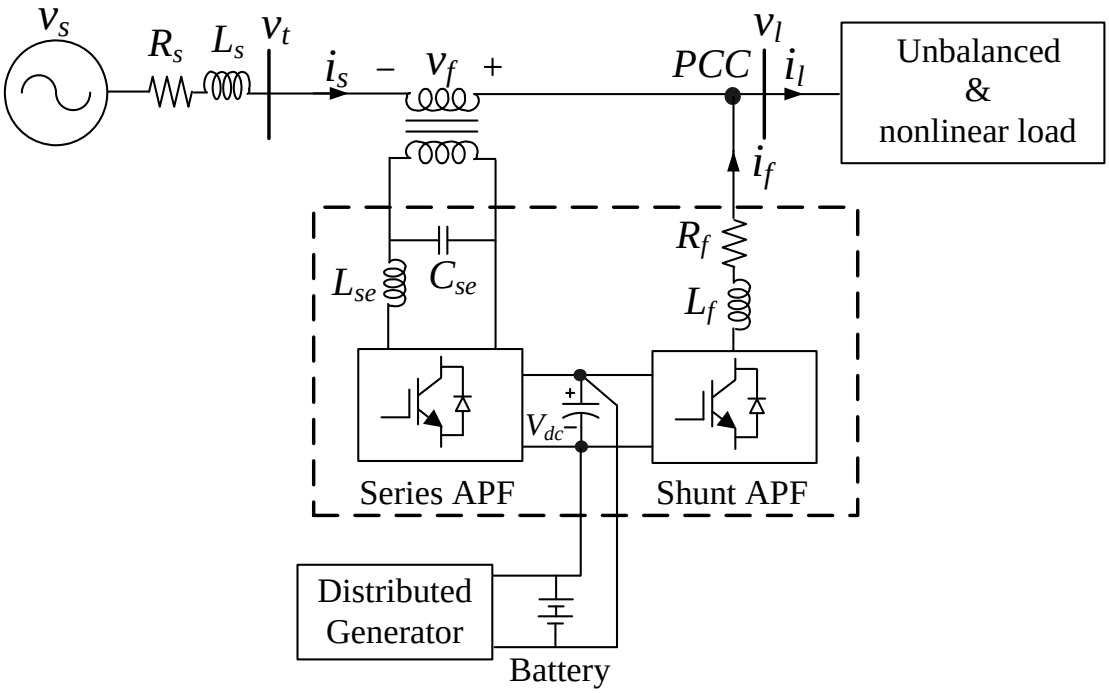

Fig. 2.12 UPQC-DG system configuration.

UPQCs mitigating voltage sag using active power are called UPQC-P. In principle to compensate the voltage sag, an in phase voltage component is injected in the series with grid voltage by series APF through an injection transformer [41]. The voltage sag can also be mitigated by reactive power injection through series APF of UPQC [42]. In that case, it is called as UPQC-Q (Q stands for reactive power). The concept is to inject a quadrature voltage by the series APF such that the vector sum of terminal voltage and the injected filter voltage equals the required rated load voltage. The shunt inverter of UPQC maintains a upf operation at the PCC. Therefore, by injecting a voltage in quadrature with the terminal voltage, the need of active power to mitigate voltage sag is eliminated. However, the load voltage achieved has phase shift with respect to the source terminal voltage. To compensate an equal percentage of voltage sag, the UPQC-Q requires larger magnitude of injection voltage compared to UPQC-P. In [43] a UPQC control is used to minimize the UPQC volt-ampere (VI) rating during voltage sag compensation. In this method, the voltage is injected to the line at certain optimal angle with respect to the source current. This method of compensating voltage sag using UPQC is abbreviated as UPQC-VA$_{min}$. In UPQC-S [44] (S stands for apparent power), series APF delivers both reactive and active power during voltage sag.

In general, the UPQC-MC, UPQC-I, UPQC-ML, UPQC-MD, UPQC-DG and UPQC-D can be based on CSI or VSI converter topology. Moreover, these topologies can be

configured as UPQC-L or UPQC-R. Expect UPQC-D all other configuration can be realized for 3ϕ3W, 3ϕ4W and 1ϕ2W systems. Additionally, the UPQC sag/swell compensation controllers can be based on UPQC-Q, UPQC-P, UPQC-VA$_{min}$ and UPQC-S approaches.

2.2.2 Control Techniques For UPQC

Control strategy decides the desired operation and behavior of UPQC. The UPQC control strategy determines the reference signals (current for shunt and voltage for series APF) and decides the switching methods for inverter switches, such that the desired performance can be achieved. There are several control techniques available in the existing literature, those have successfully applied to UPQC systems. Frequency domain methods such as, based on the fast Fourier transform (FFT) method, are not much popular due to its delay in calculating the FFT and large computation time. UPQC control methods in the time domain are based on instantaneous derivation of compensating references in the form of current or voltage signals. There are many control methods in the time domain, few are briefly discussed here. Three most widely used time domain control techniques for UPQC are the instantaneous active and reactive power theory or 3-ϕ pq theory [45], synchronous reference frame method or 3-ϕ dq theory [46] and instantaneous symmetrical components theory [47].

2.2.2.1 *Instantaneous reactive power theory*

The main aim of instantaneous reactive power theory is to develop a mathematical formulation for the instantaneous reactive power so that the reactive power can be easily calculated and compensated. Shunt APF needs to compensate for load reactive power and load current harmonics. Hence this theory is mostly applied to calculate the reference current of the shunt active filter. It uses the instantaneous values of currents and voltages to formulate the compensating quantities. The *abc* phase voltages and currents are transformed to the stationary α-β axes using the Clarke transformation as given below and are illustrated in Fig. 2.13. For a balanced source voltage the v_0 component

will be zero.

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix}$$
$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{2.1}$$

The instantaneous power on both reference frames are equal. For a balanced 3-ϕ system,

$$\begin{aligned} v_a i_a + v_b i_a + v_c i_c &= v_\alpha i_\alpha + v_\beta i_\beta \\ p &= v_\alpha i_\alpha + v_\beta i_\beta \end{aligned} \tag{2.2}$$

(where v and i are voltage and current respectively)

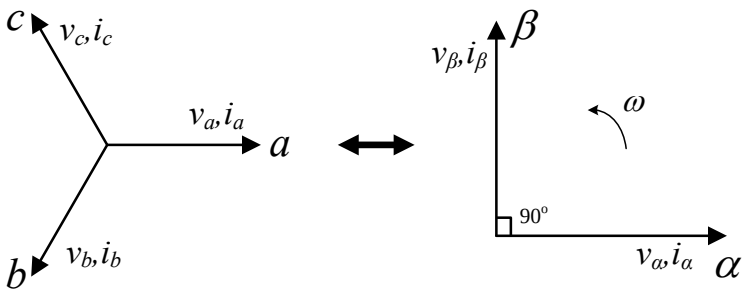

Fig. 2.13 *abc* to $\alpha\beta$ reference frame

The instantaneous reactive power is defined by using cross product of the instantaneous voltage in one axis and the instantaneous current in the other axis.

$$q = \overrightarrow{v_\alpha} \times \overrightarrow{i_\beta} + \overrightarrow{v_\beta} \times \overrightarrow{i_\alpha} \tag{2.3}$$
$$q = v_\alpha i_\beta + v_\beta i_\alpha \tag{2.4}$$

Using (2.1) and (2.3), the reactive can be expressed in *abc* coordinates as given below.

$$q = -\frac{1}{\sqrt{3}} \times [(v_a - v_b)i_c + (v_b - v_c)i_a + (v_c - v_a)i_b] \tag{2.5}$$

$$q = -\frac{1}{\sqrt{3}} \times [v_{ab}i_c + v_{bc}i_a + v_{ca}i_b] \tag{2.6}$$

From (2.2) and (2.4), the instantaneous active and reactive power in $\alpha\beta$ coordinates can be expressed in matrix form as,

$$\begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} v_\alpha & v_\beta \\ -v_\beta & v_\alpha \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \tag{2.7}$$

It can be rearranged in the following form.

$$\begin{aligned} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} &= \begin{bmatrix} v_\alpha & v_\beta \\ -v_\beta & v_\alpha \end{bmatrix}^{-1} \begin{bmatrix} p \\ q \end{bmatrix} \\ &= \frac{1}{v_\alpha^2 + v_\beta^2} \begin{bmatrix} v_\alpha & -v_\beta \\ v_\beta & v_\alpha \end{bmatrix} \begin{bmatrix} p \\ q \end{bmatrix} \\ &= \begin{bmatrix} i_{\alpha p} \\ i_{\beta p} \end{bmatrix} + \begin{bmatrix} i_{\alpha q} \\ i_{\beta q} \end{bmatrix} \end{aligned} \tag{2.8}$$

The various terms in the above equation are defined as follows.

α- axis instantaneous active current $i_{\alpha p} = v_\alpha p/(v_\alpha^2 + v_\beta^2)$

α- axis instantaneous reactive current $i_{\alpha q} = -v_\beta q/(v_\alpha^2 + v_\beta^2)$

β- axis instantaneous active current $i_{\beta p} = v_\beta p/(v_\alpha^2 + v_\beta^2)$

β- axis instantaneous reactive current $i_{\beta q} = v_\alpha q/(v_\alpha^2 + v_\beta^2)$

Using above definitions of various components of currents, the instantaneous power for a balanced 3-ϕ system can be expressed as,

$$\begin{aligned} p &= v_\alpha i_\alpha + v_\beta i_\beta \\ &= v_\alpha(i_{\alpha p} + i_{\alpha q}) + v_\beta(i_{\beta p} + i_{\beta q}) \\ &= v_\alpha i_{\alpha p} + v_\alpha i_{\alpha q} + v_\beta i_{\beta p} + v_\beta i_{\beta q} \\ &= p_{\alpha p} + p_{\alpha q} + p_{\beta p} + p_{\beta q} \\ &= v_\alpha \frac{v_\alpha p}{v_\alpha^2 + v_\beta^2} + v_\alpha \frac{-v_\beta q}{v_\alpha^2 + v_\beta^2} + v_\beta \frac{v_\beta p}{v_\alpha^2 + v_\beta^2} + v_\beta \frac{v_\alpha q}{v_\alpha^2 + v_\beta^2} \\ &= p_{\alpha p} + p_{\beta p} \end{aligned} \tag{2.9}$$

where,

α- axis instantaneous active power, $p_{\alpha p} = v_\alpha^2 p/(v_\alpha^2 + v_\beta^2)$

α- axis instantaneous reactive power, $p_{\alpha q} = -v_\alpha v_\beta q/(v_\alpha^2 + v_\beta^2)$

β- axis instantaneous active power, $p_{\beta p} = v_\beta^2 p/(v_\alpha^2 + v_\beta^2)$

β- axis instantaneous reactive power, $p_{\beta q} = v_\alpha v_\beta q/(v_\alpha^2 + v_\beta^2)$

Using (2.7), the filter current components along $\alpha - \beta$ axes in terms of its powers and voltages can be expressed as,

$$\begin{bmatrix} i_{f\alpha} \\ i_{f\beta} \end{bmatrix} = \begin{bmatrix} v_\alpha & v_\beta \\ -v_\beta & v_\alpha \end{bmatrix}^{-1} \begin{bmatrix} p_f \\ q_f \end{bmatrix} \tag{2.10}$$

where $i_{f\alpha}$ and $i_{f\beta}$ are the reference filter current along α and β axis respectively, p_f and q_f are the powers to be compensated by the filter, v_α and v_β are the $\alpha\beta$ components of voltage across the filter.The instantaneous active and reactive power can be divided in the following way.

$p = \bar{p} + \tilde{p}$ and $q = \bar{q} + \tilde{q}$, where $\bar{p}$ and $\tilde{p}$ are the average and oscillatory components of instantaneous active power and $\bar{q}$ and $\tilde{q}$ are the average and oscillatory components of instantaneous reactive power respectively. For compensating instantaneous harmonic active power, instantaneous harmonic and fundamental reactive power select the filter reference as, $p_f = \tilde{p}$ and $q_f = \bar{q} + \tilde{q}$. $\bar{p}$ includes fundamental and harmonic average power, but if the harmonic voltage is zero, then the harmonic average power will be zero. For a shunt active power filter by choosing $p_f = \tilde{p}$ and $q_f = \bar{q} + \tilde{q}$, it is possible to eliminate harmonic and reactive component of current from source current.

2.2.2.2 *Synchronous reference frame theory*

The synchronous reference frame theory or *dq* theory uses time domain reference signal estimation techniques. The basic structure of synchronous reference frame (SRF) controller consists of direct *dq* and inverse *dq* transformations (Park transformation). The main difference between $\alpha\beta 0$ reference frame and *dq0* reference frame is that the former is a stationary reference frame while the latter is a rotating reference frame. The *dq0* rotating reference frame to *abc* stationary reference frame transformation is given below and is shown in Fig.2.14

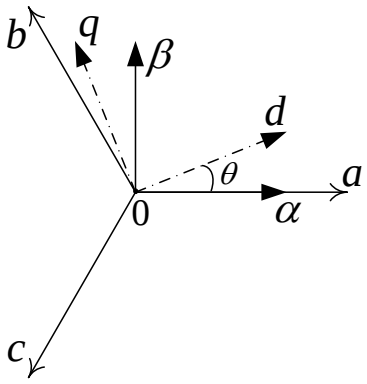

Fig. 2.14 *dq0* reference frame.

$$\begin{bmatrix} v_d \\ v_q \\ v_0 \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos\theta & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ -\sin\theta & -\sin(\theta - \frac{2\pi}{3}) & -\sin(\theta + \frac{2\pi}{3}) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{2.11}$$

Choosing θ as $(\omega t - \frac{\pi}{2})$ gives DC quantities along d and q axis in these reference frames. The final transformation matrix can be obtained by substituting $\theta = \omega t - \frac{\pi}{2}$ in (2.11) and it is shown in (2.12).

$$\begin{bmatrix} v_d \\ v_q \\ v_0 \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \sin\omega t & \sin\left(\omega t - \frac{2\pi}{3}\right) & \sin\left(\omega t + \frac{2\pi}{3}\right) \\ \cos\omega t & \cos\left(\omega t - \frac{2\pi}{3}\right) & \cos\left(\omega t + \frac{2\pi}{3}\right) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{2.12}$$

For *dq* transformation the angle θ is required, which can be obtained by using a phase locked loop (PLL). In *dq* transformation, the output depends on the performance of the PLL. The PLL circuit provides the angular speed (rad/sec) of the rotating reference frame, where ωt is set as fundamental frequency component. Depending on the fundamental, harmonics and negative sequence components in voltages and currents, the *dq* components can have different frequencies. The analysis of the *dq* components and use of appropriate filtering technique can support the generation of the voltage and current references as required by the control. The load current can transform from *abc* to *dq0* reference frame by using (2.12).The *dq* components consists of AC and DC components as given below.

$$i_{ld} = \bar{i}_{ld} + \tilde{i}_{ld} \tag{2.13}$$

$$i_{lq} = \bar{i}_{lq} + \tilde{i}_{lq} \tag{2.14}$$

By setting ωt as fundamental frequency component, the DC components $\bar{i}_{ld}$ and $\bar{i}_{lq}$ corresponds to the fundamental positive sequence load currents and the AC components $\tilde{i}_{ld}$ and $\tilde{i}_{ld}$ corresponds to the harmonic and unbalanced load current. Component $\bar{i}_{lq}$ represents the fundamental positive sequence reactive power component of load current and $\bar{i}_{ld}$ represents the fundamental positive sequence active power component of the load current. For compensating harmonics, unbalance and reactive power in the load current, the reference for the compensator can be as follows.

$$i^*_{fd} = -\tilde{i}_{ld} \tag{2.15}$$

$$i^*_{fq} = -\bar{i}_{lq} - \tilde{i}_{lq} \tag{2.16}$$

$$i^*_{f0} = -i_{l0} \tag{2.17}$$

The shunt active filter references in *abc* reference frame are obtained as follows.

$$\begin{bmatrix} i^*_{fa} \\ i^*_{fb} \\ i^*_{fc} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \sin\omega t & \cos\omega t & \frac{1}{\sqrt{2}} \\ \sin\left(\omega t - \frac{2\pi}{3}\right) & \cos\left(\omega t - \frac{2\pi}{3}\right) & \frac{1}{\sqrt{2}} \\ \sin\left(\omega t + \frac{2\pi}{3}\right) & \cos\left(\omega t + \frac{2\pi}{3}\right) & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} i^*_{fd} \\ i^*_{fq} \\ i^*_{f0} \end{bmatrix} \tag{2.18}$$

The calculation of reference currents using this approach is not affected by voltage distortion and/or unbalance. However, to obtain the transformation angle (ωt) from the supply voltage a PLL is used. Hence this affects the performance of the system when the supply voltages are unbalanced and/or distorted. The fundamental positive sequence component in distorted voltage or current are DC quantities. These quantities can easily be extracted using a low pass filter (LPF).

2.2.2.3 *Instantaneous symmetrical components theory*

The theory of instantaneous symmetrical components can be used for load balancing, harmonic suppression and power factor correction [47]. The control strategy based on the instantaneous symmetrical component theory can partially or fully compensate any kind of harmonic and unbalance in the load current with high bandwidth current sources to track the reference filter currents. This control algorithm has been derived and explained in Chapter-3. Using symmetrical component theory it is possible to derive an expression for source current reference. From this reference current the filter current

reference can be calculated. By injecting this filter current it is possible to maintain fundamental positive sequence and upf current at the source. It is very easy to maintain the DC link voltage through this method because the equation contains a variable P_{loss} which will include the losses in the converter. This will control the DC link voltage by drawing the small amount of real power from the source by the shunt inverter.

$$\begin{aligned} i^*_{sa} &= \left[\frac{(v_{la}-v_{l0})+\beta(v_{lb}-v_{lc})}{\sum_{j=a,b,c} v^2_{lj}-3v^2_{l0}}\right](P_{lavg}+P_{loss}) \\ i^*_{sb} &= \left[\frac{(v_{lb}-v_{l0})+\beta(v_{lc}-v_{la})}{\sum_{j=a,b,c} v^2_{lj}-3v^2_{l0}}\right](P_{lavg}+P_{loss}) \\ i^*_{sc} &= \left[\frac{(v_{lc}-v_{l0})+\beta(v_{la}-v_{lb})}{\sum_{j=a,b,c} v^2_{lj}-3v^2_{l0}}\right](P_{lavg}+P_{loss}) \end{aligned} \tag{2.19}$$

$$\begin{aligned} i^*_{fa} &= i_{la}-i^*_{sa} \\ i^*_{fa} &= i_{la}-i^*_{sa} \\ i^*_{fa} &= i_{la}-i^*_{sa} \end{aligned} \tag{2.20}$$

where,

i^*_{sa}, i^*_{sb} and i^*_{sc} are source current reference, v_{la}, v_{lb} and v_{lc} are PCC voltages, v_{l0} is the instantaneous zero sequence component of the PCC voltage, $\beta = \tan\phi/\sqrt{3}$, ϕ is *pf* angle, P_{lavg} is the average load power and P_{loss} is the power loss in the converter.
The source reference current equation is shown in (2.19) and the filter reference current equation is shown in (2.20). When the source voltages used for generating the shunt filter current references are distorted and unbalanced, this algorithm results in erroneous compensation. To eliminate this limitation, fundamental positive sequence component of the PCC voltages should use in the algorithm.

A simple controller scheme for UPQC, called as unit vector template generation (UVTG), is given in [48]. The method uses a PLL to produce unit vector templates for three or single phase system. In [49] a method called one cycle control (OCC) of switching converters is developed for the UPQC. The OCC controller uses an integrator which has a reset feature to force the controlled parameters to meet the control goal in each switching cycle. A model predictive control scheme is proposed for UPQC in

[50]. The model predictive controller has simple online computations and can handle multi variable control problems. Kamran and Habetler [24] have proposed a technique based on deadbeat control in which the UPQC converter combination is treated as a single unit. The overall system can be modeled as a single multi-input multi-output system. This results in reduced inter-converter energy storage and an improved control performance over the separately controlled converters. The frequency domain and time domain techniques have certain limitations. To overcome this problems a wavelet analysis technique is proposed by certain researchers. The wavelet transform is used to represent a time varying signal in terms of frequency component [51].

2.2.3 UPQC for Compensating Voltage Interruption

UPQC has been widely studied to mitigate or eliminate the disturbances propagated from the load side and source side. UPQC can simultaneously mitigate the current disturbance in load side and the voltage disturbance in source side. UPQC can compensate voltage sag/swell, harmonic voltage, harmonic current and control the active and reactive power flow. However, UPQC cannot compensate the voltage interruptions because it has no energy storage devices connected to its DC bus. A new configuration of UPQC that consists of DC/DC converters and the supercapacitor for compensating the voltage interruption is proposed in [52] and [53]. Fig. 2.15 shows the configuration of UPQC, which additionally has a DC/DC converter and supercapacitor for compensating the voltage interruption. The energy in the DC link charges the supercapacitors through the DC/DC converter when the system is in normal operation. The energy in the supercapacitor is released to the DC link through the DC/DC converter when a voltage interruption occur. The system uses a positive sequence detector which calculates the supply voltage positive sequence component and the system works in normal mode when the supply voltage level is maintained as 1 pu. It works in sag or swell mode when the level is between 0.5 and 1.0 pu or higher than 1.0 pu respectively. It works in interruption mode when the supply voltage level is lower than 0.5 pu.

In normal mode, the series inverter do not injects any voltage to the line, and the shunt inverter absorbs the current harmonics generated by the load to maintain fundamental source current. The DC/DC converter works in standby mode or charge mode depending on the voltage level of the supercapacitor. Switch S_3 is closed, S_1 and S_2 are

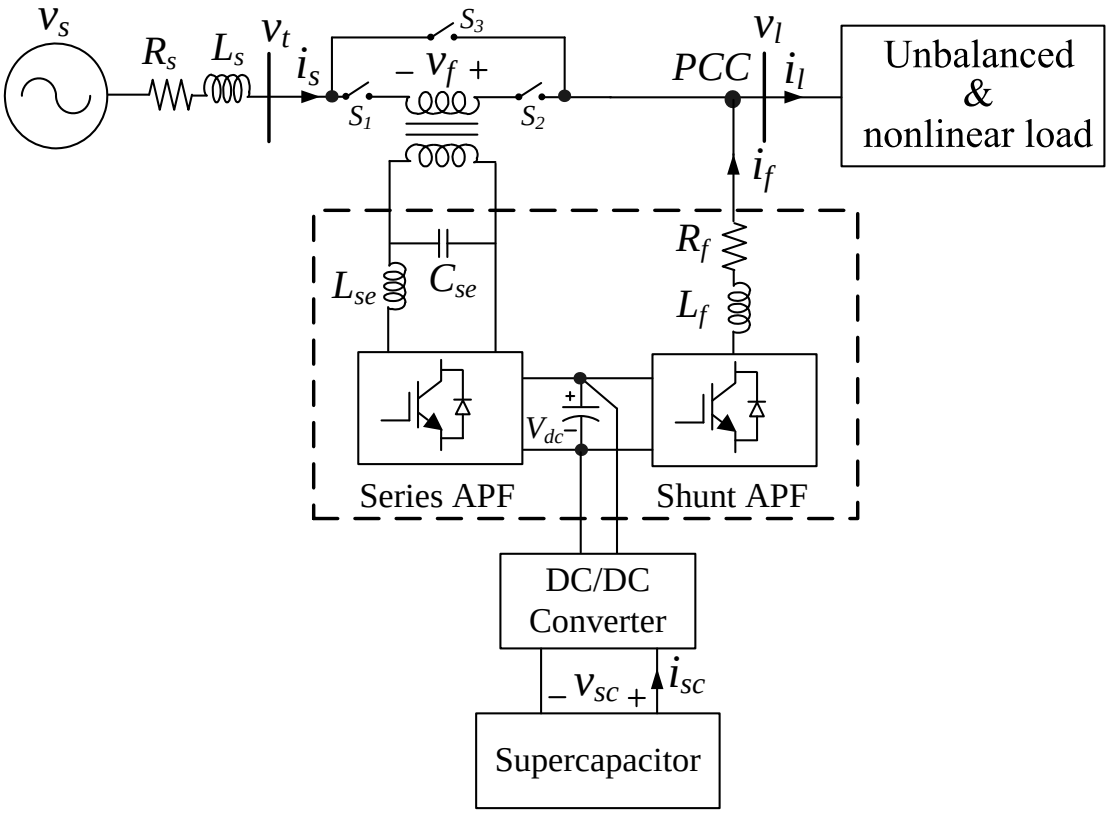

Fig. 2.15 UPQC system interconnected with energy storage.

open during normal mode operation. In voltage sag or swell mode, the series inverter injects the compensating voltage to maintain the load voltage constant. The shunt inverter absorbs the current harmonics generated by the load and the DC/DC converter works in standby mode. During this mode of operation the switches S_1 and S_2 are closed, S_3 is open. In voltage interruption mode, the series inverter is disconnected from the line (all the three switches S_1, S_2 and S_3 are open). The shunt inverter starts to work as an AC voltage source. The DC/DC converter works in discharge mode to supply the energy stored in the supercapacitor to the load.

The supercapacitor has less energy density compared to battery. So it cannot deliver energy for a long time, because of this the backup time of this configuration is less. Also during voltage sag and swell supercapacitor is in standby mode, hence all the dc link voltage fluctuation is mitigated by shunt inverter. By using battery-supercapacitor hybrid energy storage this limitations can be eliminated. Battery ultracapacitor will increase the backup time during voltage interruption and the ultracapacitor can effectively utilize for delivering energy during sag and swell. Also the stress on the battery can reduce by diverting the load fluctuations to the supercapacitor.

2.3 Parameters Influencing Battery Performance

Battery can be used as an energy storage device in UPQC for compensating voltage interruption. Hence, this section focuses on the parameters influencing the performance of the battery. For lead acid batteries, the electrodes are PbO_2 and Pb and the electrolyte is H_2SO_4 [54]. The battery charging and discharging occur as a result of chemical reaction between the electrolyte and electrode plates. The rate of chemical reaction is influenced by state of charge (SOC), rate of charge/discharge, battery storage capacity, age/shelf life and environmental temperature. Batteries are characterized in terms of energy density, power density and life cycle. Life cycle is highly dependent on depth of discharge (DOD).

2.3.1 Capacity of Battery

Capacity of battery means the energy that is stored or released from a battery. The battery voltage variation is not very serious during normal discharge condition, the capacity of battery can be roughly calculated by discharging current and time. Since the units used are ampere and hour, ampere-hour (*Ah*) is used as capacity unit. The capacity (Ah)that can be drawn from a lead acid battery is not constant, it is related to many factors. The most dominant factor is discharging current.

Peukert proposed an equation to describe the relation between the discharging time and discharging current [55].

$$\begin{aligned} I^n \times T &= C \\ N &= \frac{C}{I^{n-1}} \end{aligned} \tag{2.21}$$

where, I is discharging current, T is discharging time, C is a constant, N is battery nominal capacity (*Ah*) and n is an exponential parameter which varies with different batteries between the range of 1.05 and 2. If n equals 1, that means the battery capacity can be extracted is not related to the magnitude of discharging current. This equation cannot describe the relation precisely, it can only be used as a rough estimation.

State of charge (SOC) can be used as a state variable to indicate the residue capacity of a battery, instead of practical ampere hour capacity. For lead acid battery SOC is

proportional to the concentration of the sulfuric acid in the electrolyte. From (2.21) it is understood that the actual battery storage capacity reduces with increase in discharge current and it results in poor utilization of the battery. Hence, the higher load demands should not be supplied by battery for efficient operation.

2.3.2 Battery Life

The charge discharge cycle life of a battery is usually defined according to its maximum capacity. To expand a battery's life means to maintain a battery to reserve a better capacity (Ah) of stored energy. When high current is drawn from the battery (at high charge/discharge rate), the chemical reaction could not respond very faster and results in oxygen and hydrogen gas formation. This gas formation reduce the effectiveness and performance of the battery. Other problems that affects the battery performance includes sulphation, electrode corrosion and degradation. These problems becomes dominant when high discharge current is drawn from battery. The most important factors influencing battery life include depth of discharge (DOD), temperature and acid density. The lower DOD increases battery life. The acid density decreases the battery life. Very high temperature reduces the battery capacity. High discharge rate results in high DOD, it adds more stress on the battery and decreases the cycle life of battery. Hence it is necessary to not discharge battery completely. Maintaining a minimum 50% SOC improves the battery lifetime.

2.3.3 Power Density and Energy Density

The specific energy is the energy per unit weight (Kg) of the energy storage devices, which decides the capacity of energy storage devices. A supercapacitor stores electric charge in a double layer formed on a large surface area of micro porous material such as activated carbon. In Fig. 2.16 , it is seen that supercapacitors occupy a region between conventional capacitors and batteries. Despite greater capacitances than conventional capacitors, supercapacitors have yet to match the energy densities of mid to high end batteries. With higher energy density, it is possible for the energy storage devices to supply energy for a longer time. A comparison of different energy storage devices with respect to energy and power density as shown in Fig. 2.16 [1]. The

specific power decides the speed of energy storage devices at which the energy can be absorbed or supplied. The supercapacitor stores energy by means of static charge and hence, the charging and discharging is faster. Because of the high power density of supercapacitors, it can supply high load demand instantaneously. During sag and

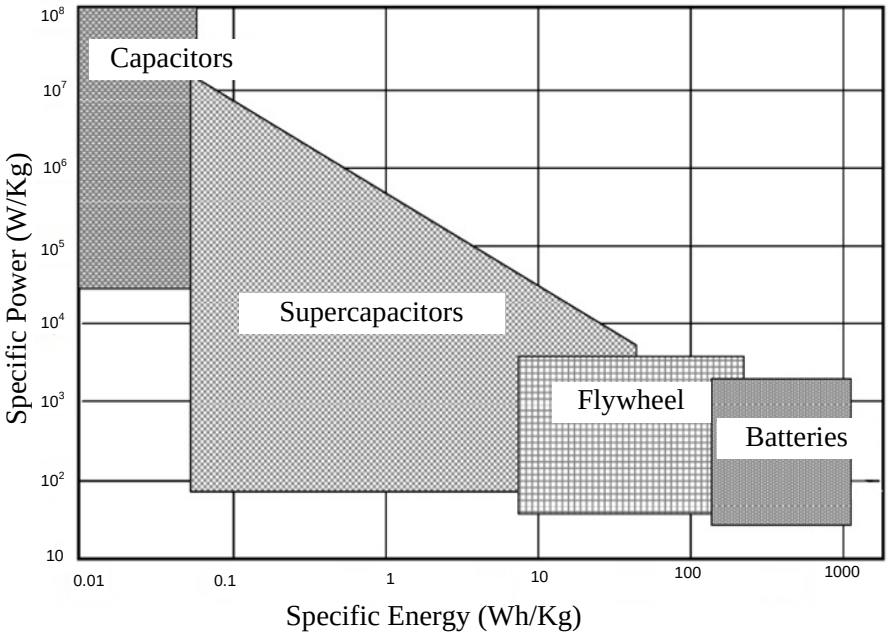

Fig. 2.16 Specific power Vs specific energy ranges for different storage elements [1].

swell the supercapacitor can instantaneously discharge and charge so that the DC link voltage fluctuations can reduce. Moreover, it is possible to mitigate a sag as high as 0.5 pu without much difficulty with the support of supercapacitor. The battery lifetime can be extended by using supercapacitor because it will reduce the stress and depth of discharge of battery.

2.4 Battery Supercapacitor Hybrid

In the previous section, it is seen that supercapacitor has high power density compared to battery and it can deliver power quickly. In fluctuating load or UPQC-DG applications, it is advantageous to use battery-supercapacitor hybrid [56] instead of battery or supercapacitor alone, because it can advantage of each storage devices to yield a source having both high energy density and high power density. Battery delivers power to the load for a long time and supercapacitor mitigates all the sudden DC link voltage fluctuations of UPQC. Thus battery lifetime increases. The comparison of battery and super

capacitor on different parameters are given in the Table 2.1.

Supercapacitors can be divided into three main categories, namely, pseudo capacitors, electrochemical double layer capacitors and hybrid supercapacitors. Each category is characterized by its unique mechanism for storing electric charge. These are, respectively, faradaic, non faradaic and a combination of the two. Faradaic mechanism, such as oxidation reduction reactions, involve the transfer of electric charge between electrolyte and electrode. A non faradaic process does not use a chemical reaction, rather, charges are distributed on surfaces of interface by physical processes that do not involve the breaking and making of chemical bonds. In this project electrochemical double layer capacitor is considered.

Table 2.1 Battery and Supercapacitor Comparison.

Parameters	Lead Acid Battery	Supercapacitor
Specific Energy (Wh/Kg)	$10 - 100$	$1 - 10$
Specific Power (W/Kg)	< 1000	$< 10,000$
Cycle Life	1000	$500,000$
Charge/Discharge Efficiency	$70 - 80\%$	$85 - 98$
Charging Time	$1 - 5$ hr	$0.3 - 30$ s
Discharging Time	$0.3 - 3$ hr	$0.3 - 3$ s

In the direct connection (without DC/DC converter) of the battery and ultracapacitor in parallel to DC link of UPQC, the power sharing between the battery and the ultracapacitor is determined by their respective resistances. The terminal voltage of such a power source is not regulated instead follows the battery discharge curve and can vary considerably between fully charged and fully depleted. This kind of connection is not recommended in UPQC application because of the limited control over battery and supercapacitor and large fluctuations in the DC link voltage which will affect the performance of UPQC. The battery ultracapacitor hybrid that uses DC/DC converters for both the energy storage devices (active hybrid) is used to actively control the power flow between battery, ultracapacitor UPQC DC link and the load, thereby enhancing the power capability.

Adding DC/DC converter between battery-ultracapacitor and UPQC DC link has several advantages such as, the ultracapacitor voltage can be different from the battery voltage and DC link voltage which offers flexibility with respect to the design of the battery and ultracapacitor arrays, the power capacity of the hybrid system can be much higher than that of the passive hybrid without exceeding the safety limit of the battery

current, the DC/DC converter can also serve as the battery charging controller while a passive hybrid power source would require a separate battery charger, the DC bus voltage of UPQC can be kept relatively constant with a smaller variation than that of the passive connection even as the battery is depleted. The active hybrid offers advantages of a better voltage regulation, broader voltage range, a smaller battery and supercapacitor current ripple and less weight and volume of the system.

2.5 Summary

In this chapter, various power quality problems, UPQC topologies and control strategies, battery ultracapacitor hybrid and advantages of using DC/DC converter for battery ultracapacitor hybrid were explained in detail. The voltage sag is the common power quality problem that affect the system adversely. Out of various control methods for UPQC, the instantaneous symmetrical component theory with fundamental positive sequence component extraction is simple in formulation and because of its flexibility and simplicity to work under all source voltage and load current circumstances, in this work, this theory has been used for reference current generation for shunt APF of UPQC during grid connected mode. Various voltage source inverter topologies for UPQC applications are detailed in this chapter. The four leg shunt inverter topology is suitable for the UPQC with battery-ultracapacitor applications because it uses a single capacitor as DC link and hence the control of DC link voltage is simple. Using battery-ultracapacitor instead of battery or ultracapacitor alone is advantageous in fluctuating load and UPQC-DG applications. The next Chapter explains the design and control of UPQC.

CHAPTER 3

DESIGN AND CONTROL OF UPQC

Series inverter, shunt inverter, filters and DC link are the various components of UPQC. The series inverter reference voltage generation, shunt inverter reference current generation, switching pulse generation for series and shunt inverter, design of DC link, shunt interface inductor design and series inverter filter design are explained in this chapter.

3.1 Design of DC Link Capacitor

Fig. 3.1 shows the power circuit of three phase UPQC used in this work. The compensation performance of series and shunt APF depends on the voltage rating of DC link capacitor. The primary condition for reactive power compensation is that the DC link voltage should be higher than the peak voltage at the point of common coupling (PCC). The DC link voltage for the shunt active filter must have a higher value than the peak value of the line-to-neutral voltage. For proper operation of the UPQC inverters, at any instant the voltage of the DC link capacitor should be greater than $\sqrt{6}$ times the phase voltage of the system [57]. When the DC link voltage is less than this limit, there is insufficient voltage for shunt APF to drive the currents through the inductances for tracking the reference currents. A DC link voltage equal to the peak of the line-to-line voltage of the system is sufficient for series APF compensation. The DC link voltage requirement for the shunt and series active filters is not the same. The shunt active filter requires higher DC bus voltage when compared to the series active filter for proper compensation. The PCC phase rms voltage is 230 V and the DC link voltage (V_{dc}) chosen for simulation is 700 V.

The determination of the value of DC link capacitor is either based on instantaneous power flow on the DC and AC side of the converter, or the mitigation of DC link voltage oscillations imposed by the lower order harmonics or unbalance in linear and non linear loads [58]. Increasing the capacitor value suppress the voltage ripple. For maintaining a constant voltage across the capacitor a PI controller is used as shown in the Fig. 3.2.

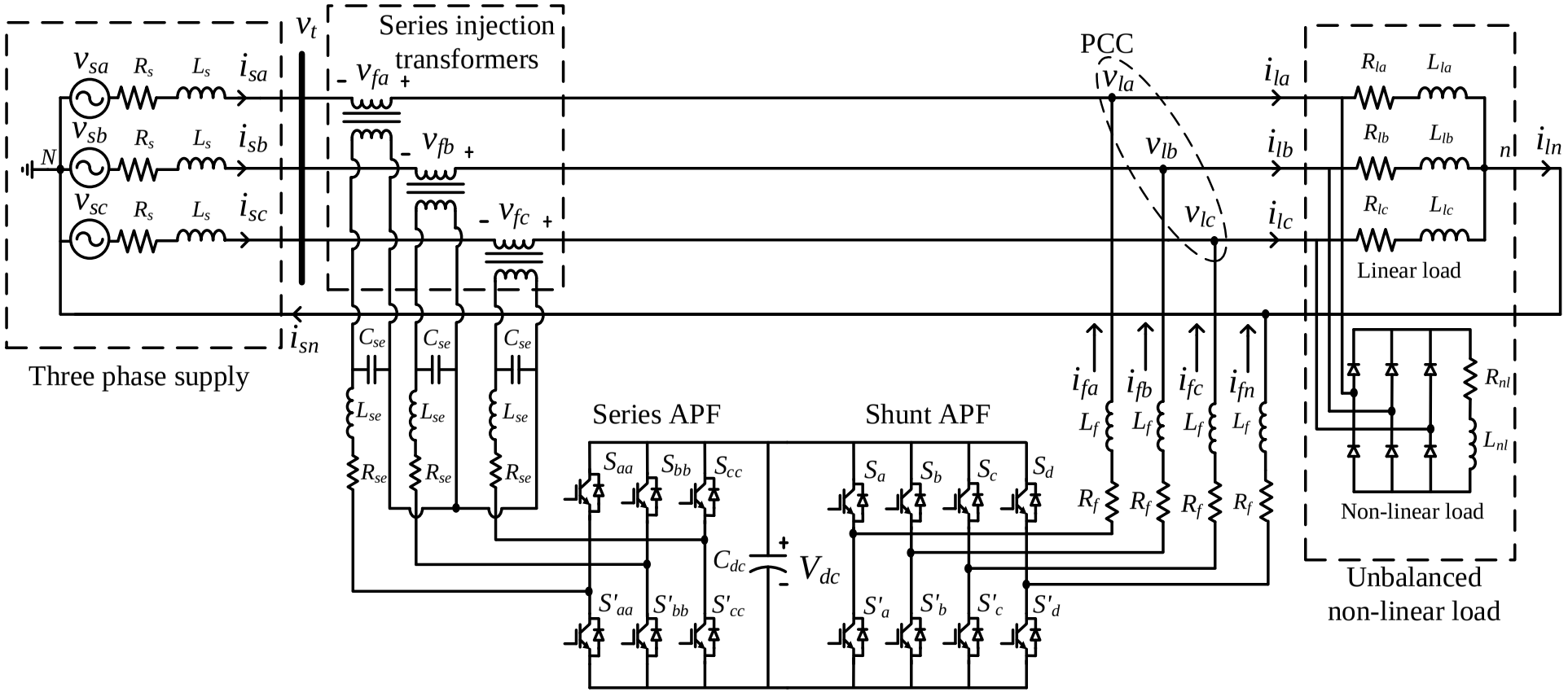

Fig. 3.1 Power circuit of three phase UPQC.

The proper selection of the parameters of the PI controller reduces the voltage ripple across DC link capacitor. Higher value of DC link capacitor increases the rise time of the PI controller and thus it reduces the speed of the controller. Hence the capacitor value should not be high enough to increase the rise time of PI controller to unexpected level and should not be low enough to cause high voltage ripple.

3.2 Design and Control of Shunt APF

The shunt inverter of UPQC is used for current related power quality mitigation. This inverter works in current control mode. The load reactive power, load current harmonics and load current unbalance are mitigated by shunt APF. During voltage interruption, series APF is isolated from the system, the battery and ultracapacitor deliver power through the shunt inverter. Therefore, when selecting the rating of shunt inverter, one should keep in mind that the shunt inverter has to carry the load current during voltage interruption. Shunt inverter is connected in parallel with the AC load and it inject a current into the PCC, this makes the source current balanced, sinusoidal and upf. The primary step towards designing shunt APF is the generation of the filter current reference.

3.2.1 Reference Current Generation

Theory of instantaneous symmetrical components is used for generating source current reference and there by filter current reference.

3.2.1.1 *Instantaneous symmetrical component theory*

The theory of instantaneous symmetrical components can be used for the purpose of load balancing, harmonic suppression, and power factor correction [47][59]. Theoretically, the control algorithms based on instantaneous symmetrical component theory can compensate any kind of unbalance and harmonics in the load. For any set of 3-ϕ instantaneous currents or voltages, the instantaneous symmetrical components are defined

by,

$$\begin{bmatrix} \overline{v}_{a0} \\ \overline{v}_{a1} \\ \overline{v}_{a2} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \begin{bmatrix} v_{la} \\ v_{lb} \\ v_{lc} \end{bmatrix} \tag{3.1}$$

$$\begin{bmatrix} \overline{i}_{a0} \\ \overline{i}_{a1} \\ \overline{i}_{a2} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \begin{bmatrix} i_{sa} \\ i_{sb} \\ i_{sc} \end{bmatrix} \tag{3.2}$$

where, a is a complex operator and it is given by $a = e^{j2\pi/3}$.

Here, the shunt inverter is connected in parallel with the load, the common point where load and shunt APF are connected is called the point of common coupling (PCC). The PCC voltage is the load voltage which is represented as v_{la}, v_{lb} and v_{lc}. Instantaneous symmetrical component theory for load compensation is derived out of three conditions they are,

1. The source neutral current must be zero. Therefore,

$$i_{sa} + i_{sb} + i_{sc} = 0 \tag{3.3}$$

2. To have a predefined power factor at the PCC, the relationship between fundamental positive sequence load voltage and source current is given below.

$$\angle v_{la1} = \angle i_{sa1} + \phi \tag{3.4}$$

   where, ϕ is the phase angle between v_{la1} and i_{sa1}.

3. The average real power demand by the load should be met by the utility grid . This gives the following equation,

$$v_{la}i_{sa} + v_{lb}i_{sb} + v_{lc}i_{sc} = P_{lavg} = \frac{1}{T}\int_{t_1}^{t_1+T} (v_{la}i_{la} + v_{lb}i_{lb} + v_{lc}i_{lc})dt \tag{3.5}$$

Now we have to get an expression for source current reference which is in phase with the PCC voltage (load voltage). The source current reference is represented by, $i^*_{sa}, i^*_{sb}, i^*_{sc}$ and shunt APF injected reference current is $i^*_{fa}, i^*_{fb}, i^*_{fc}$. Then we can formu-

late as,

$$\begin{aligned} i^*_{sa} &= i_{la} - i^*_{fa} \\ i^*_{sb} &= i_{lb} - i^*_{fb} \\ i^*_{sb} &= i_{lc} - i^*_{fc} \end{aligned} \tag{3.6}$$

From (3.1),(3.2) and (3.4) we can write as,

$$\angle\frac{1}{3}(v_{la} + av_{lb} + a^2v_{lc}) = \angle\frac{1}{3}(i_{sa} + ai_{sb} + a^2i_{sc}) + \phi \tag{3.7}$$

Substituting the value of a and rearranging,

$$\angle\frac{1}{3}\left(v_{la} - \frac{v_{lb}}{2} - \frac{v_{lc}}{2} + \frac{j\sqrt{3}}{2}(v_{lb} - v_{lc})\right) = \angle\frac{1}{3}\left(i_{sa} - \frac{i_{sb}}{2} - \frac{i_{sc}}{2} + \frac{j\sqrt{3}}{2}(i_{sb} - i_{sc})\right) + \phi$$

Taking tan of the equation on both sides and rearranging we get,

$$\begin{aligned} &\frac{\sqrt{3}}{2}(v_{lb} - v_{lc}) + \frac{\tan\phi}{2}[v_{lb} + v_{lc} - 2v_{la}]i_{sa} + \\ &\frac{\sqrt{3}}{2}(v_{lc} - v_{la}) + \frac{\tan\phi}{2}[v_{la} + v_{lc} - 2v_{lb}]i_{sb} + \\ &\frac{\sqrt{3}}{2}(v_{la} - v_{lb}) + \frac{\tan\phi}{2}[v_{la} + v_{lb} - 2v_{lc}]i_{sc} = 0 \end{aligned} \tag{3.8}$$

On substituting $\frac{tan\phi}{\sqrt{3}} = \beta$ we obtain,

$$\begin{aligned} &[(v_{lb} - v_{lc}) + \beta(v_{lb} + v_{lc} - 2v_{la})]\, i_{sa} + \\ &[(v_{lc} - v_{la}) + \beta(v_{la} + v_{lc} - 2v_{lb})]\, i_{sb} + \\ &[(v_{la} - v_{lb}) + \beta(v_{la} + v_{lb} - 2v_{lc})]\, i_{sc} = 0 \end{aligned} \tag{3.9}$$

Using the equation $v_{la} + v_{lb} + v_{lc} = 3v_{l0}$, where v_{l0} is the zero sequence component of the PCC voltage. The above equation becomes,

$$\begin{aligned} &[(v_{lb} - v_{lc}) + \beta(3v_{l0} - 3v_{la})]\, i_{sa} + \\ &[(v_{lc} - v_{la}) + \beta(3v_{l0} - 3v_{lb})]\, i_{sb} + \\ &[(v_{la} - v_{lb}) + \beta(3v_{l0} - 3v_{lc})]\, i_{sc} = 0 \end{aligned} \tag{3.10}$$

Now the three conditions can be rewritten in the form of equations as following,

$$i^*_{sa} + i^*_{sb} + i^*_{sc} = 0 \tag{3.11}$$

$$\begin{aligned} &[(v_{lb} - v_{lc}) + \beta(3v_{l0} - 3v_{la})]\, i^*_{sa} + \\ &[(v_{lc} - v_{la}) + \beta(3v_{l0} - 3v_{lb})]\, i^*_{sb} + \\ &[(v_{la} - v_{lb}) + \beta(3v_{l0} - 3v_{lc})]\, i^*_{sc} = 0 \end{aligned} \tag{3.12}$$

$$v_{la} i^*_{sa} + v_{lb} i^*_{sb} + v_{lc} i^*_{sc} = P_{lavg} \tag{3.13}$$

Solving the above three equations the desired source current can be obtained as,

$$\begin{aligned} i^*_{sa} &= \left[\frac{(v_{la} - v_{l0}) + \beta(v_{lb} - v_{lc})}{\sum_{j=a,b,c} v^2_{lj} - 3v^2_{l0}} \right] P_{lavg} \\ i^*_{sb} &= \left[\frac{(v_{lb} - v_{l0}) + \beta(v_{lc} - v_{la})}{\sum_{j=a,b,c} v^2_{lj} - 3v^2_{l0}} \right] P_{lavg} \\ i^*_{sc} &= \left[\frac{(v_{lc} - v_{l0}) + \beta(v_{la} - v_{lb})}{\sum_{j=a,b,c} v^2_{lj} - 3v^2_{l0}} \right] P_{lavg} \end{aligned} \tag{3.14}$$

When load voltage are balanced, the above equation is satisfied for balanced source currents. However if load voltage are unbalanced and distorted, above equation gives set of currents which are also not balanced and sinusoidal in order to supply constant load power. The series inverter try to maintain a balanced fundamental voltage at the PCC. Hence the load voltage is always balanced and sinusoidal, thus $v_{s0} = 0$. The entire load reactive power should be given by the shunt inverter so that only real power is drawn from the grid. For this the load voltage and source current should be in phase, therefore $\phi = 0$. The series inverter maintain the load voltage such that the load voltage and source voltage are in phase. Hence the source voltage and source current are in phase.

$$\beta = tan\phi/\sqrt{3}$$

$$\phi = 0$$

$$\beta = 0 \tag{3.15}$$

$$v_{l0} = 0 \tag{3.16}$$

By substituting (3.15) and (3.16) in (3.14), we get (3.17)

$$\begin{aligned} i_{sa}^{*} &= \left(\frac{v_{la}}{\sum_{j=a,b,c} v_{lj}^{2}}\right) P_{lavg} \\ i_{sb}^{*} &= \left(\frac{v_{lb}}{\sum_{j=a,b,c} v_{lj}^{2}}\right) P_{lavg} \\ i_{sc}^{*} &= \left(\frac{v_{lc}}{\sum_{j=a,b,c} v_{lj}^{2}}\right) P_{lavg} \end{aligned} \tag{3.17}$$

where, P_{lavg} is average load active power. During sag and swell series inverter injects a voltage through series injection transformer which is added to the source voltage and gives a constant rms voltage at the load. During voltage sag the DC link voltage decreases and during voltage swell it increase, for proper operation of UPQC it is necessary to maintain a constant voltage at the DC link capacitor. For this UPQC consume some active power from the grid. We have to modify equation (3.17) for including all the losses in the UPQC converters. A variable P_{loss} is included in the equation, this term includes converter switching losses and helps to maintain a constant voltage at the DC link capacitor during sag and swell. Equation (3.17) can be modified as,

$$\begin{aligned} i_{sa}^{*} &= \left(\frac{v_{la}}{\sum_{j=a,b,c} v_{lj}^{2}}\right) (P_{lavg} + P_{loss}) \\ i_{sb}^{*} &= \left(\frac{v_{lb}}{\sum_{j=a,b,c} v_{lj}^{2}}\right) (P_{lavg} + P_{loss}) \\ i_{sc}^{*} &= \left(\frac{v_{lc}}{\sum_{j=a,b,c} v_{lj}^{2}}\right) (P_{lavg} + P_{loss}) \end{aligned} \tag{3.18}$$

The term P_{lavg} is obtained using simple moving average filter over a half cycle as the oscillating part of the real power has frequency which is double the system frequency. A PI controller is used for getting P_{loss}. Fig. 3.2 shows the block diagram for obtaining P_{loss} using PI controller. The error between DC voltage reference and actual DC voltage are processed through PI controller to obtain P_{loss}. Applying Kirchoff's current law at the point of common coupling (PCC),

$$\begin{aligned} i_{fa}^{*} &= i_{la} - i_{sa}^{*} \\ i_{fb}^{*} &= i_{lb} - i_{sb}^{*} \\ i_{fc}^{*} &= i_{lc} - i_{sc}^{*} \end{aligned} \tag{3.19}$$

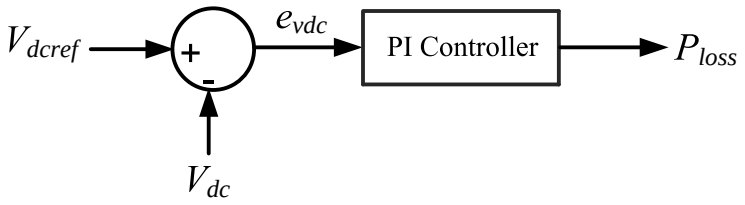

Fig. 3.2 PI controller for maintaining constant DC link voltage.

where, i^*_{fa}, i^*_{fb} and i^*_{fc} are the shunt inverter reference current. The fourth leg of the shunt inverter is for source neutral current compensation. Source neutral current must be zero for balanced current. Calculation of i^*_{fn} is given below,

$$\begin{aligned} i_{ln} &= i_{la} + i_{lb} + i_{lc} \\ i^*_{sn} &= i^*_{fn} + i_{ln} \\ i^*_{sn} &= 0 \\ i^*_{fn} &= -(i_{la} + i_{lb} + i_{lc}) \end{aligned} \tag{3.20}$$

By substituting (3.18) in (3.19), we get,

$$\begin{aligned} i^*_{fa} &= i_{la} - \left(\frac{v_{la}}{\sum_{j=a,b,c} v^2_{lj}} \right) (P_{lavg} + P_{loss}) \\ i^*_{fb} &= i_{lb} - \left(\frac{v_{lb}}{\sum_{j=a,b,c} v^2_{lj}} \right) (P_{lavg} + P_{loss}) \\ i^*_{fc} &= i_{lc} - \left(\frac{v_{lc}}{\sum_{j=a,b,c} v^2_{lj}} \right) (P_{lavg} + P_{loss}) \end{aligned} \tag{3.21}$$

Now we have to generate switching pulses for shunt inverter such that inverter current follows the current reference shown in the equations (3.21) and (3.20). Hysteresis current controller is used for generating switching pulses for shunt inverter during normal voltage, voltage sag and swell.

3.2.2 Hysteresis Based PWM Controller

The hysteresis band control is used to generate the switching pulses of the shunt inverter. Hysteresis controller is chosen ahead of various other controllers because of its fast dynamics, robust control and ease of implementation. Hysteresis based PWM control is the simplest control method for generating switching pulses for shunt APF

while sinusoidal PWM (SPWM) is suitable for generating switching pulses for series APF [60]. The operation of hysteresis current controller can be understood by observing Fig. 3.3. An upper band and lower band ($+h$ and $-h$) are defined around the shunt

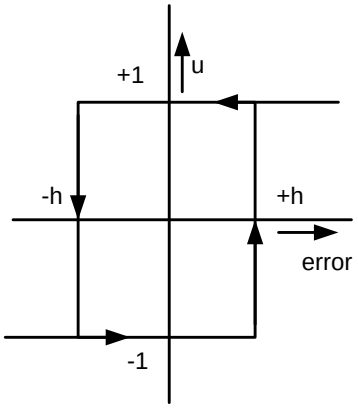

Fig. 3.3 Two-level hysteresis scheme.

inverter reference current. The error is the difference between reference current and actual current. Consider the a phase leg of the four-leg shunt inverter, it has an upper switch S_a and lower switch $S_a^{'}$. Whenever the error goes above $+h$ the upper switch S_a should be turned ON and $S_a^{'}$ should turned OFF. Whenever the error goes below $-h$, complement to the previous operation should take place.

If $error \geq h$ then $u = 1$

If $error \leq h$ then $u = -1$

$$\left.\begin{array}{ll} S_a & ON \\ S_a^{'} & OFF \end{array}\right\} \quad u = 1$$

$$\left.\begin{array}{ll} S_a & OFF \\ S_a^{'} & ON \end{array}\right\} \quad u = -1$$

When $u = 1$ the actual current injected by shunt APF increases and when $u = -1$ the current injected by shunt APF decrease.

3.2.3 Shunt Interface Inductor

The shunt APF filter inductance should be low enough to allow a high rate of change of current to all harmonic components of interest. At the same time it should be high enough to limit higher frequency switching components. Therefore by considering the

highest frequency component that should be injected and the switching frequency that should be filtered, a compromise value of the shunt inductor is chosen. Hysteresis controller has a variable switching frequency and is proportional to DC link voltage (V_{dc}) and inversely proportional to both hysteresis band (h) and inductance (L_f). The hysteresis band chosen for simulation study is, $h = 0.1$. The inductance value can be found out by considering the constraint on the maximum ripple current [58] and it is given below.

$$L_f = \frac{V_{dc}}{6 f_s \Delta I_{(p-p)max}} \tag{3.22}$$

where, $V_{dc} = 700$ V, f_s is the average switching frequency (20 kHz) and $\Delta I_{(p-p)max}$ is the maximum ripple in the inverter current and is chosen to be 0.3 A. Substituting this values to (3.22), we get, $L_f = 19.4$ mH. In the simulation study 20 mH inductor is used as shunt interfacing inductor.

3.2.4 Control of Shunt Inverter

During normal voltage, voltage sag and swell the shunt inverter works in current control mode. Hysteresis current controller is used for generating the switching pulses during these conditions so that the current generated by the shunt APF follows the reference current. During voltage interruption the shunt inverter work in voltage control mode.

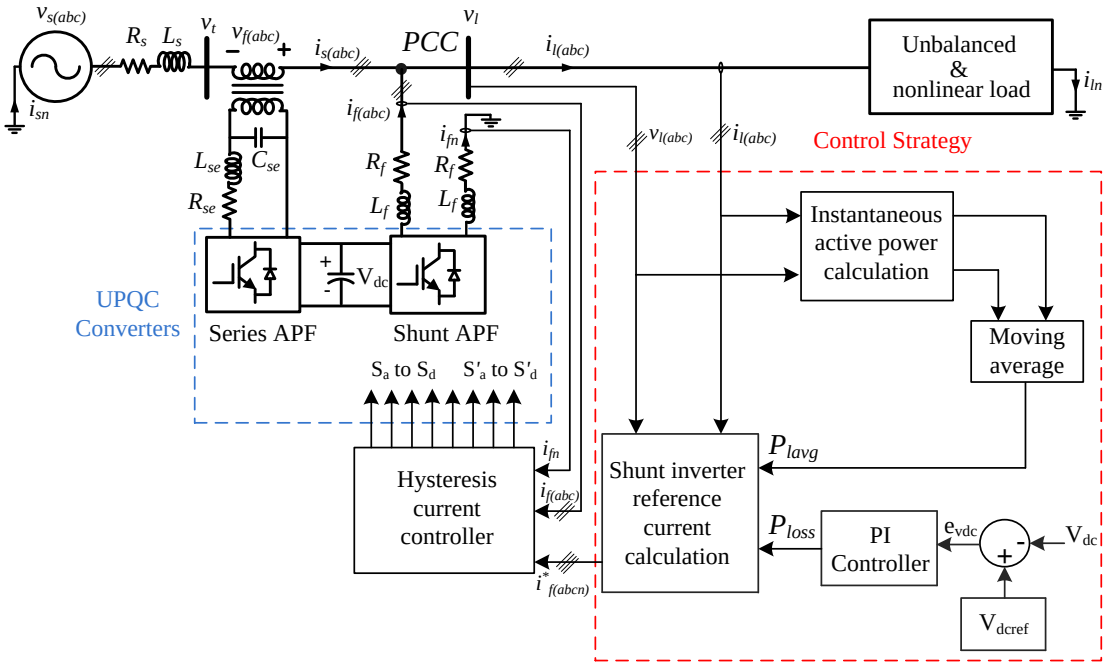

Fig. 3.4 Control strategy of shunt APF.

SPWM control is used for generating switching pulses so that it maintain a constant rms voltage at the load terminal. The control of shunt inverter during voltage interruption is explained in Chapter-5.

Fig. 3.4 shows the control strategy of shunt inverter during normal voltage ($0.9-1.1$ pu), voltage sag and voltage swell. The shunt interfacing inductor L_f is used to filter out the switching frequency components produced by the hysteresis controller.

3.3 Design and Control of Series APF

Series APF is used for compensating voltage sag and voltage swell. The control system of series APF performs sag/swell detection, reference voltage generation and gate signal generation. During normal voltage conditions the injection transformer is bypassed by the bypassing switches so that unwanted voltage drop is avoided. The inclusion of series APF injection transformer and the injection of voltage in series with the supply is controlled by the voltage sag/swell detection. The reference voltage generator produces a reference load voltage which has to be maintained at the load terminals all the time.

3.3.1 Reference Voltage Generation

The supply voltage may contain harmonics and unbalance. Irrespective of the supply harmonics and unbalance the load voltage should always be balanced and fundamental. Also it is synchronize with the supply voltage phase angle so that supply voltage and load voltage are in-phase. We need to extract the fundamental positive sequence component of the supply voltage. The instantaneous symmetrical component theory is used for the extraction of symmetrical components of voltages and the complex Fourier coefficients [61] are used for the extraction of fundamental component of voltages.

$$\begin{bmatrix} \overline{v}_{ta}^{0} \\ \overline{v}_{ta}^{+} \\ \overline{v}_{ta}^{-} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \begin{bmatrix} v_{ta} \\ v_{tb} \\ v_{tc} \end{bmatrix} \tag{3.23}$$

Where, v_{ta}, v_{tb} and v_{tc} are the instantaneous source voltage after the feeder voltage drop, $\overline{v}_{ta}^{0}, \overline{v}_{ta}^{+}$ and $\overline{v}_{ta}^{-}$ are the zero, positive and negative sequence components of a phase

voltage and are complex time varying quantities. If the source voltage has harmonic components, then the symmetrical components also have harmonics. The extraction of fundamental component can be written as,

$$\begin{bmatrix} \overline{v}^0_{ta1} \\ \overline{v}^+_{ta1} \\ \overline{v}^-_{ta1} \end{bmatrix} = \frac{\sqrt{2}}{T}\int_{t_1}^{t_1+T} \begin{bmatrix} \overline{v}^0_{ta} \\ \overline{v}^+_{ta} \\ \overline{v}^-_{ta} \end{bmatrix} e^{-j(\omega t-\pi/2)}dt \tag{3.24}$$

The factor $\sqrt{2}$ is used to change from power invariant description to the magnitude invariant description. Furthermore, time interval is chosen as half a cycle for a low-delay rejection of harmonics and negative phase-sequence effects. This averaging can be between any two points and need not be synchronized with the zero crossing of the current. A moving average filter for a window of half cycle can be used for calculation of fundamental component. ω should be fundamental angular frequency for extracting fundamental component of voltage. Equation (3.24) can be used for extracting fundamental positive sequence phase and magnitude which can be used for sag/swell detection. Let the supply voltage is of the form,

$$\begin{aligned} v_{ta} &= \sqrt{2}V_{ta1}\sin(\omega t-\theta_{a1})+v_{tah} \\ v_{tb} &= \sqrt{2}V_{tb1}\sin(\omega t-2\pi/3-\theta_{b1})+v_{tbh} \\ v_{tc} &= \sqrt{2}V_{tc1}\sin(\omega t+2\pi/3-\theta_{c1})+v_{tch} \end{aligned} \tag{3.25}$$

where, V_{ta1}, V_{tb1} and V_{tc1} are the fundamental rms value of terminal voltages (source voltage after the feeder impedance drop), θ_{a1}, θ_{b1} and θ_{c1} are the phase angle of fundamental voltages with respect to a reference, v_{tah}, v_{tbh} and v_{tch} are the instantaneous harmonic component of terminal voltages and ω is the fundamental angular frequency. Fundamental positive sequence component of a-phase terminal voltage can be written as,

$$\overline{V}^+_{ta1} = \frac{\sqrt{2}}{T}\int_0^T \bar{v}^+_a e^{-j(\omega t-\pi/2)}dt \tag{3.26}$$

$$= \frac{\sqrt{2}}{T}\int_0^T \frac{v_{ta}+av_{tb}+a^2v_{tc}}{3}(\sin\omega t+j\cos\omega t)dt \tag{3.27}$$

substituting (3.25) in (3.27) and simplifying, we get equation (3.28).

$$\overline{V}^{+}_{ta1} = \frac{V_{ta1}\angle -\theta_{a1} + V_{tb1}\angle -\theta_{b1} + V_{tc1}\angle -\theta_{c1}}{3} \tag{3.28}$$

Equation (3.28) shows that $\overline{V}^{+}_{ta1}$ is a complex quantity, its magnitude represents rms value of fundamental positive sequence terminal voltage and argument represents the phase angle of fundamental positive sequence a-phase terminal voltage. If the terminal voltage is balanced, that is, $V_{ta1} = V_{tb1} = V_{tc1} = V_{t1}$ and $\theta_{a1} = \theta_{b1} = \theta_{c1} = \theta_1$, then the equation (3.28) can be modified as,

$$\overline{V}^{+}_{ta1} = V_{t1}\angle -\theta_1 \tag{3.29}$$

where, V_{t1} is rms value fundamental positive sequence terminal voltage and $-\theta_1$ is the phase angle of fundamental positive sequence terminal voltage. The load voltage reference can be written as,

$$\begin{aligned} v^{*}_{la} &= \sqrt{2}V_l \sin(\omega t - \theta_1) \\ v^{*}_{lb} &= \sqrt{2}V_l \sin(\omega t - 2\pi/3 - \theta_1) \\ v^{*}_{lc} &= \sqrt{2}V_l \sin(\omega t + 2\pi/3 - \theta_1) \end{aligned} \tag{3.30}$$

where, V_l is the required rms value of load voltage which has to be maintained by the series inverter during voltage sag and swell, θ_1 is obtained from (3.29). Equation (3.30) shows that load voltage is in-phase with the fundamental positive sequence component of terminal voltage, during sag/swell series inverter injects a fundamental positive sequence voltage in-phase/anti-phase with terminal voltage such that load rms voltage is maintained constant all the time. The source voltage harmonics has to be compensated by the series inverter. Series inverter reference voltage can be written as,

$$\begin{aligned} v^{*}_{fa} &= v^{*}_{la} - v_{ta} \\ v^{*}_{fb} &= v^{*}_{lb} - v_{tb} \\ v^{*}_{fc} &= v^{*}_{lc} - v_{tc} \end{aligned} \tag{3.31}$$

substituting (3.30) in (3.31), we get (3.32),

$$\begin{aligned} v^*_{fa} &= \sqrt{2}V_l \sin(\omega t - \theta_1) - v_{ta} \\ v^*_{fb} &= \sqrt{2}V_l \sin(\omega t - 2\pi/3 - \theta_1) - v_{tb} \\ v^*_{fc} &= \sqrt{2}V_l \sin(\omega t + 2\pi/3 - \theta_1) - v_{tc} \end{aligned} \tag{3.32}$$

Sinusoidal pwm (SPWM) controller is used for generating switching pulses for series inverter.

3.3.2 Sag/Swell Detection

An essential part of the control of a series APF is the detection circuit. A voltage sag/swell must be detected fast and corrected with a minimum of false operations. The detection circuit operates the series APF from standby to active mode and vice versa. Equation (3.24) gives fundamental zero, positive and negative sequence components of terminal voltages, which can be used for detection of both balanced and unbalanced voltage disturbances. $\overline{v}^0_{a1}, \overline{v}^+_{a1}$ and $\overline{v_{a1}}$ are complex quantities and its magnitudes are the rms value of fundamental component of zero, positive and negative sequence terminal voltages respectively. Balanced voltage sag and swell are considered for the simulation study. The logical steps of operation of detection circuit is given below.

1. Equation (3.27) gives fundamental positive sequence magnitude and phase angle of terminal voltage. A moving average filter with window size of half cycle is used for calculating equation (3.27). This moving average filter introduces a maximum of half cycle delay in the detection algorithm.
2. The magnitude given by moving average filter is compared with the set values to detect normal voltage, voltage sag, voltage swell and voltage interruption.
3. When the condition 0.9 pu $\leq |\overline{V}^+_{ta1}| \leq 1.1$ pu is satisfied, the system operates in normal voltage condition.
4. When 0.5 pu $\leq |\overline{V}^+_{ta1}| < 0.9$ pu is satisfied, the system operates in voltage sag condition.
5. When 1.1 pu $< |\overline{V}^+_{ta1}| \leq 1.5$ pu is satisfied, the system operates in voltage swell condition.
6. When $|\overline{V}^+_{ta1}| < 0.5$ pu or $|\overline{V}^+_{ta1}| > 1.5$ pu, the system operates in voltage interruption condition.

3.3.3 PWM Gate Signal Generation

Equation (3.32) represents the reference voltage of series APF. Sinusoidal PWM controller is used for generating series APF voltage which follows the reference voltage. The reference voltage is taken as the modulating signal and the carrier signal is a triangular wave with frequency 5 kHz. The output voltage have switching frequency harmonics which is filtered by a LC low-pass filter. The triangular wave peak value should be greater than that of inverter reference voltage. The triangular signal and series inverter reference voltages are given to comparators and its operation is given below.

If $v_{fa}^{*} \geq v_{tr}$, $S_{aa}-$ON and $S_{aa}^{'}-$OFF

If $v_{fa}^{*} < v_{tr}$, $S_{aa}-$OFF and $S_{aa}^{'}-$ON

If $v_{fb}^{*} \geq v_{tr}$, $S_{bb}-$ON and $S_{bb}^{'}-$OFF

If $v_{fb}^{*} < v_{tr}$, $S_{bb}-$OFF and $S_{bb}^{'}-$ON

If $v_{fc}^{*} \geq v_{tr}$, $S_{cc}-$ON and $S_{cc}^{'}-$OFF

If $v_{fc}^{*} < v_{tr}$, $S_{cc}-$OFF and $S_{cc}^{'}-$ON

Where, v_{tr} is the triangular signal, S_{aa}, S_{bb}, S_{cc} are series inverter upper switches and $S_{aa}^{'}, S_{bb}^{'}, S_{cc}^{'}$ are series inverter lower switches.

3.3.4 LC Low Pass Filter

The sinusoidal PWM switching frequency used in the simulation study is 5 kHz. The output voltage of the series inverter includes switching frequency components, the harmonic components in the output voltages are around switching frequency and multiple of switching frequency. The LC low pass filter eliminates all the switching frequency harmonics from the series inverter output voltage so that the load voltage is distortion free. Fig. 3.5 shows the circuit diagram of filter used. The transfer function of the

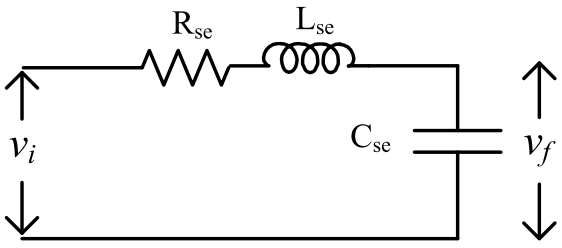

Fig. 3.5 LC low pass filter.

circuit is,

$$\frac{V_f(s)}{V_i(s)} = \frac{\frac{1}{LC}}{s^2 + \frac{R}{L}s + \frac{1}{LC}} \tag{3.33}$$

From transfer function, the natural frequency and damping factor can be written as,

$$\omega_n = \frac{1}{\sqrt{LC}}$$

$$f_n = \frac{1}{2\pi\sqrt{LC}} \tag{3.34}$$

$$\delta = \frac{R}{2}\sqrt{\frac{C}{L}} \tag{3.35}$$

where, f_n is the natural frequency of the low pass filter and δ is the damping factor. If the source voltage has harmonics, it has to be compensated by the series inverter. The LC filter cutoff frequency (f_n) should be greater than the harmonics components which needs to be compensated. L and C values are chosen to provide a particular cutoff frequency which passes the fundamental and necessary harmonic components. Higher value of C reduce the voltage ripple in the filter voltage. R is chosen such that it provides proper damping to the filter output oscillations. The voltage oscillations at the instant of series inverter activation/deactivation is reduced by higher value of resistance. But increasing the value of resistance cause more voltage drop across it and thus it reduces the rms value of load voltage.

3.3.5 Control of Series Inverter

Control section of series inverter includes, reference voltage generation, sag/swell detection and switching pulse generation as shown in Fig. 3.6. Sag/swell detector sends a control signal to the SPWM controller to enable it according to the occurrence of sag or swell. The series APF injects a voltage in series with the source voltage to maintain the load voltage sinusoidal and balanced. The power consumption of the series inverter to inject voltage causes DC link voltage fluctuation, the shunt APF draws power from the source to maintain the DC link voltage. The switching frequency components from the series inverter out put is filtered by the LC low pass filter.

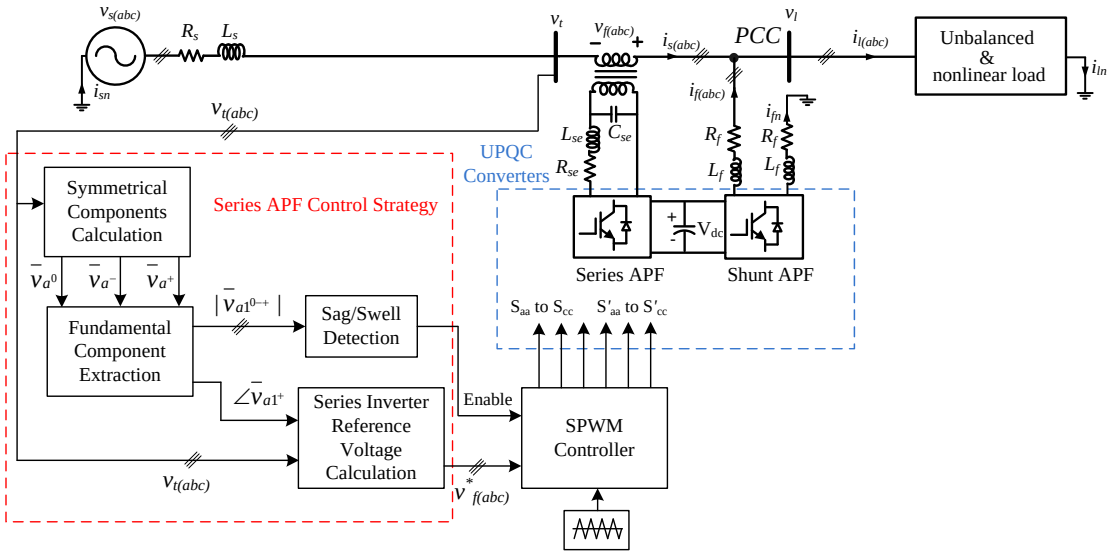

Fig. 3.6 Control strategy of series APF.

3.4 Summary

The series inverter mitigates the voltage related power quality problems while shunt inverter mitigates current related power quality problems. The DC link voltage is maintained constant by shunt inverter control. Fig. 3.7 shows the complete control of UPQC. The series inverter controller sense the sag and swell and inject the voltage in series with the supply to maintain load voltage. A faster sag/swell detection is required for better operation of UPQC. The algorithm used in this study has a maximum of half cycle delay which is introduced by the moving average filter. The hysteresis controller has variable switching frequency, the proper selection of filter inductance eliminate the switching frequency components from the shunt inverter current and hence from the source current. The SPWM introduce harmonics to the voltage which depends on the switching frequency used. Higher switching frequency reduces the THD in the series inverter voltage, but it cause more switching losses. The UPQC cannot compensate voltage interruption because it doesn't have any energy storage devices like battery or ultracapacitor. When voltage interruption occur, the DC link voltage quickly falls to zero. The energy storage devices maintain the DC link voltage at the time of interruption and one of the UPQC inverter is operational to maintain the load voltage. The modelling of battery, ultracapacitor and the design of DC/DC converters are explained in the next chapter.

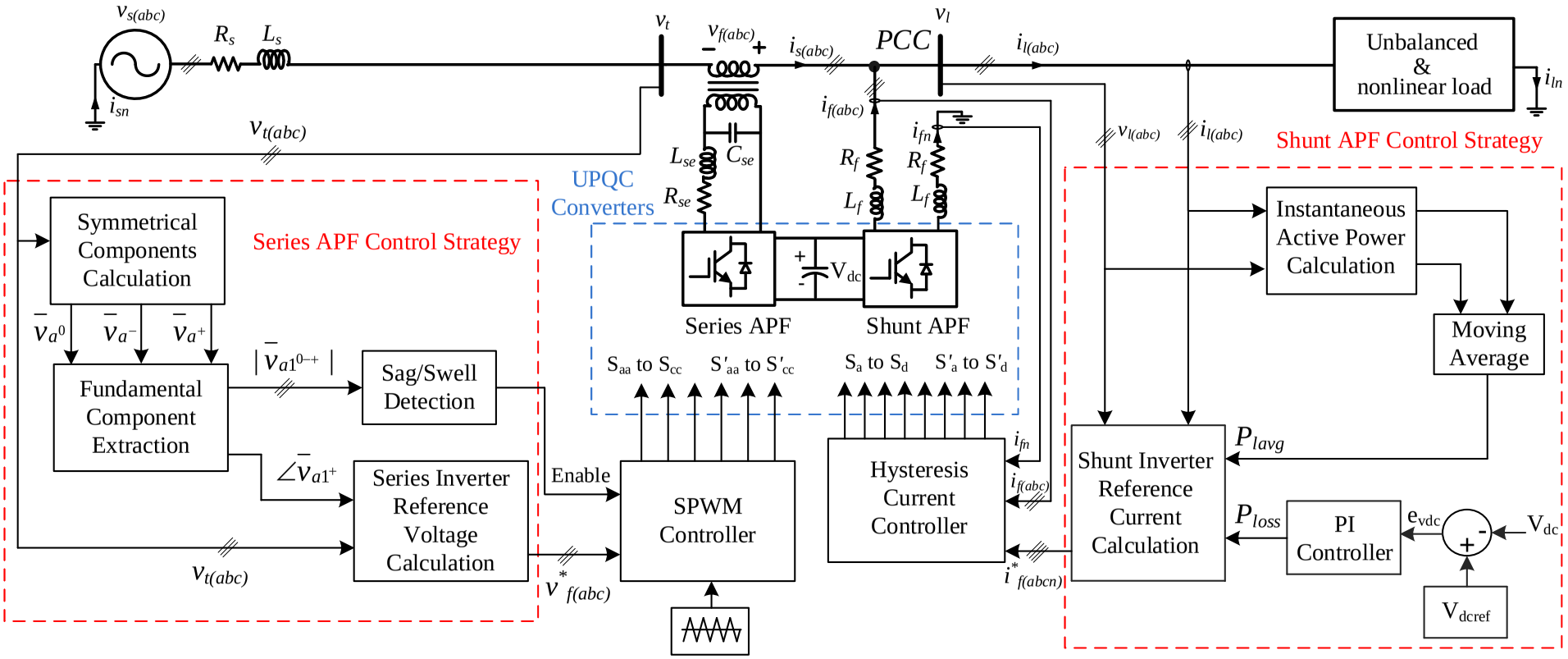

Fig. 3.7 Control strategy of UPQC.

CHAPTER 4

MODELLING OF BATTERY AND SUPERCAPACITOR

The battery and ultracapacitor are modelled with parameters to suit their charge/discharge characteristics. The Matlab/Simulink simpowersystems library model is used for battery and ultracapacitor models [3]. Battery is the primary energy storage device in this study, it has higher energy density compared to ultracapacitor. The capacity of battery is chosen such that the battery SOC is changed considerably during simulation. Ultracapacitor has high power density and can deliver power quickly. The DC link fluctuations can be diverted to supercapacitor so that the sudden battery current fluctuations are avoided.

4.1 Battery Modelling

The lead-acid battery model is used for simulation study. Its advantages include inexpensive and low maintenance requirements, low self discharge rate. It is best suitable for UPS applications. The Matlab/Simulink library model of battery is used for the simulation study.

4.1.1 The Charge Model

When the lead-acid battery reaches the full charge, its voltage increases rapidly. This phenomenon can be modelled by the term polarization resistance. The polarization resistance of battery increases in the charge mode operation until the it is almost fully charged. The polarization resistance increases abruptly above the fully charge point [62]. The polarization resistance is given by the equation,

$$R_p = K_1 \frac{Q}{it} \tag{4.1}$$

where, K_1 is the polarization constant (Ω), Q is battery capacity (Ah) and $it = \int idt$ is the actual battery charge (Ah). Theoretically, the polarization resistance (R_p) is infinite when $it = 0$ (fully charged). About 10% of the battery capacity is contributed by R_p. Equation (4.1) can be re-written to,

$$R_p = K_1 \frac{Q}{(it + 0.1Q)} \tag{4.2}$$

Lead acid battery has a hysteresis phenomenon between discharge and charge operation which do not depends on battery SOC. Hysteresis phenomenon occurs only in the battery exponential area. A nonlinear dynamic system defined by the equation (4.3) is used for expressing this behaviour .

$$\dot{v}_{exp}(t) = B|i(t)|(-v_{exp}(t) + Am(t)) \tag{4.3}$$

Where, $v_{exp}(t)$ is the exponential zone voltage, $i(t)$ is the battery current, $m(t)$ is the charge or discharge mode and A & B are exponential zone constants. The exponential zone voltage depends on the initial voltage $v_{exp}(t_0)$ and charge ($m(t) = 1$) or discharge mode ($m(t) = 0$). The lead acid battery charging can be expressed by equation (4.4) [62].

$$V_{batt} = E_0 - iR - K_1 \frac{Q}{(it + 0.1Q)} i^* - K_2 \frac{Q}{(Q - it)} it + v_{exp} \tag{4.4}$$

Where, V_{batt} is the battery terminal voltage (V), E_0 is the battery constant voltage (V), K_1 & K_2 are polarization constants, Q is battery maximum capacity, R is the battery internal resistance (Ω), i is the battery discharge current (A), i^* is the filtered battery current (A), it is the time integral of battery current which represents the amount of charge discharged from the battery, v_{exp} is the exponential zone voltage which will get by solving equation (4.3) in which $m(t) = 1$. The term $(K_2 Qit)/(Q - it)$ in (4.4) represents the polarization voltage, this shows the nonlinear relationship between battery SOC and open circuit voltage.

4.1.2 The Discharge Model

When battery is discharging, the polarization resistance increases. During discharging, $m(t) = 0$ in (4.3). Fig. 4.1 shows the typical discharge curve of lead acid battery. The

complete equation representing battery discharge [62] can be expressed as,

$$V_{batt} = E_0 - iR - K_1\frac{Q}{(Q-it)}i^* - K_2\frac{Q}{(Q-it)}it + v_{exp} \tag{4.5}$$

For battery discharge, equation (4.3) can be modified as,

$$\begin{aligned} \dot{v}_{exp}(t) &= -B|i(t)|v_{exp}(t) \\ v_{exp}(t) &= v_{exp}(t_0)e^{-B|i(t)|t} \end{aligned} \tag{4.6}$$

where, $v_{exp}(t_0)$ is the initial exponential zone voltage. When the battery discharge

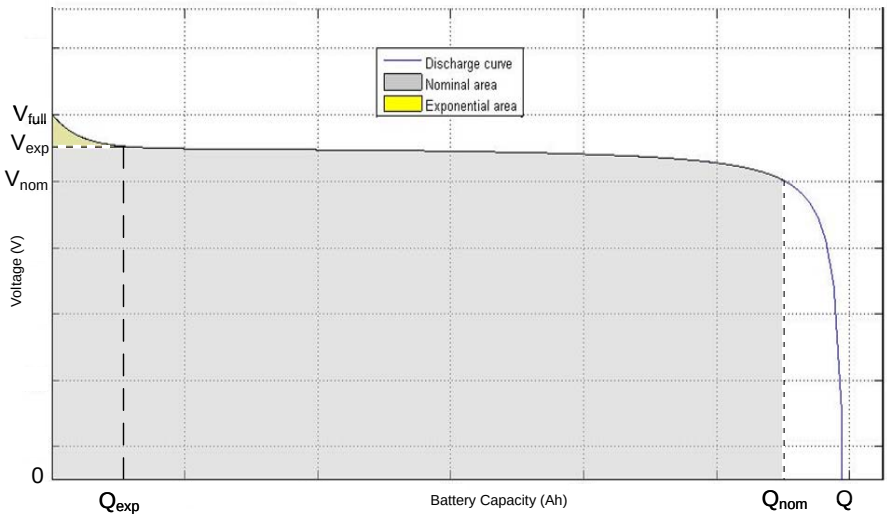

Fig. 4.1 Typical discharge curve of lead-acid battery.

occur, the exponential voltage decreases immediately. The state of charge (SOC) for a fully charge lead acid battery is 100% and for an empty battery is 0%. The SOC is calculated as,

$$SOC = 100\left(1 - \frac{1}{Q}\int_0^t i(t)dt\right) \tag{4.7}$$

where, $i(t)$ is the battery discharge current. Fig. 4.2 shows the complete charge/discharge model of battery [2]. m is the battery charge or discharge mode selection, $m = 1$ for charging and $m = 0$ for discharging. Equation (4.6) gives the expression for v_{exp} during battery discharging. Solving (4.3) with $m(t) = 1$ will give the expression for v_{exp} during battery charging. The expression for E_{batt} during charging and discharging is,

$$E_{batt} = \begin{cases} E_{discharge} & : i^* > 0 \\ E_{charge} & : i^* < 0 \end{cases}$$

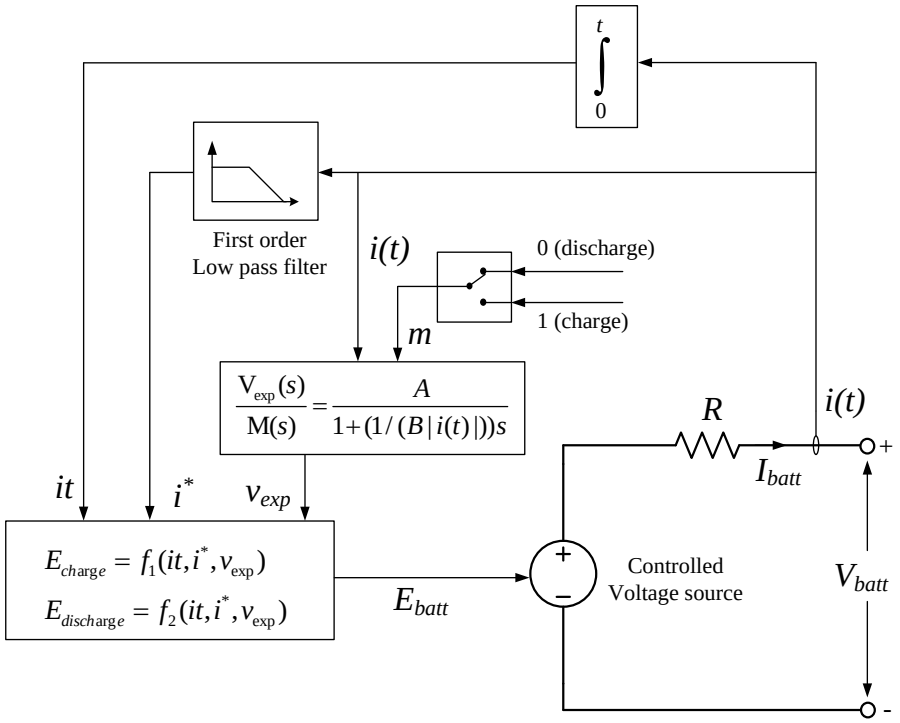

Fig. 4.2 Battery model [2].

When battery is in standby mode $i^* = 0$, during battery charging $i^* < 0$ and $i^* > 0$ for battery discharging. The expression for E_{charge} and $E_{discharge}$ can be written as,

$$E_{charge} = E_0 - K_1 \frac{Q}{(it + 0.1Q)} i^* - K_2 \frac{Q}{(Q - it)} it + \mathscr{L}^{-1}\left(\frac{V_{exp}(s)}{M(s)} \frac{1}{s}\right) \tag{4.8}$$

$$E_{discharge} = E_0 - K_1 \frac{Q}{(Q - it)} i^* - K_2 \frac{Q}{(Q - it)} it + v_{exp}(t_0) e^{-B|i(t)|t} \tag{4.9}$$

The symbol $\mathscr{L}^{-1}$ represents inverse Laplace transform. During battery charging, the battery terminal voltage (V_{batt}) can be written as,

$$\begin{aligned} V_{batt} &= E_{batt} - iR \\ &= E_{charge} - iR \end{aligned} \tag{4.10}$$

During battery discharging, V_{batt} can be written as,

$$V_{batt} = E_{discharge} - iR \tag{4.11}$$

4.1.3 Model Assumptions and Limitations

The Matlab/Simulink online documentation gives the battery model assumptions used, which are :

- During the charge and discharge of battery, the internal resistance is taken constant and it does not vary with the amplitude of battery current.
- The battery discharge characteristics is used for extracting model parameters and assumed to be same during battery charging.
- The Peukert effect is not taken into consideration in this model.
- The model does not consider the temperature effect.
- The battery self discharge is not taken into consideration.

The battery model limitations are :

- The minimum value of battery voltage at no load is 0 V and the maximum voltage of battery possible by this model is $2E_0$.
- The battery minimum capacity is 0 Ah and Q is the maximum possible battery capacity. The maximum state of charge of battery cannot be greater than 100% even if the battery is overcharged.

4.1.4 Battery Model Parameters

Battery model parameters are chosen to best fit the battery discharge curve. The model requires three parameters from the discharge curve for complete modelling of battery. These are the fully charged voltage (V_{full}), the end of the exponential zone (Q_{exp}, V_{exp}) and the end of nominal zone (Q_{nom}, V_{nom}). Also the model requires the maximum capacity (Q) and internal resistance (R). The factor B is approximated to $3/Q_{exp}$ in the exponential zone, since after three time constants the energy of the battery exponential term is almost 0.

$$B = \frac{3}{Q_{exp}} \tag{4.12}$$

In steady state, the filtered current (i^*) is equal to discharge current (i). The polarization constants K_1 and K_2 are equal in magnitude ($K_1 = K_2 = K$). Equation (4.5) can be modified as,

$$V_{exp} = E_0 - iR - K\frac{Q}{(Q - Q_{exp})}(Q_{exp} + i) + Ae^{(\frac{-3}{Q_{exp}}Q_{exp})} \tag{4.13}$$

The nominal zone voltage is given by,

$$V_{nom} = E_0 - iR - K\frac{Q}{(Q - Q_{nom})}(Q_{nom} + i) + Ae^{(\frac{-3}{Q_{exp}}Q_{nom})} \tag{4.14}$$

The amount of charge discharged is zero ($it = 0$) for a fully charged battery voltage and the filter output current (i^*) is zero because the step current is just started. Then fully charged voltage can be expressed as,

$$V_{full} = E_0 - iR + A \tag{4.15}$$

Battery parameters E_0, K, A and B are calculated by solving equations (4.12),(4.13),(4.14) and (4.15). The parameters considered for obtaining the battery characteristics are given in the Table 4.1. The discharge curve of lead-acid battery used for simulation study is shown Fig. 4.3 [3].

Table 4.1 Parameters Considered for Battery Characteristics.

Parameters	**Value**
Nominal voltage (V_{nom})	300 V
Rated capacity	20 mAh
Nominal capacity (Q_{nom})	15 mAh
Fully charged voltage (V_{full})	320.65 V
Exponential zone capacity (Q_{exp})	2 mAh
Exponential zone voltage (V_{exp})	312 V
Initial state of charge	50% while charging 100% while discharging
Internal resistance	0.06 Ω

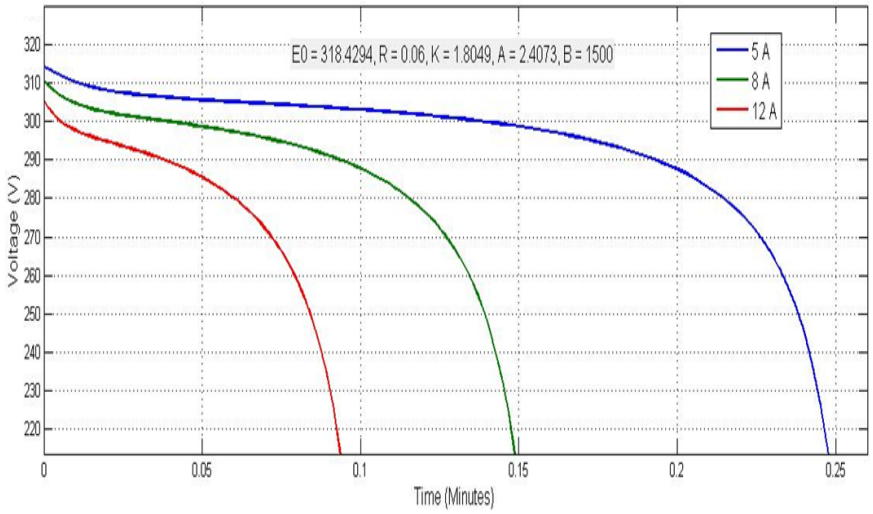

Fig. 4.3 Discharge curve of lead acid battery [3].

4.2 Supercapacitor Modelling

Ultracapacitors close the gap between rechargeable batteries and capacitors. A double layer supercapacitor with metal-electrolyte interface is modelled in this section. When a metal electrode is immersed in an electrolyte solution, metal-electrolyte interface forms an electric double layer. The metal surface has a layer of charge and an equal and opposite charge is formed inside the electrolytic solution. An electric double layer can be described using the Gouy-Chapman-Stern model [63],[64], which distinguishes three layers, namely, a porous carbon which has the electrical charge in the carbon structure, the electrical charge in the carbon structure is compensated by the ions called the diffuse layer, the third layer exist in between the carbon structure and the diffuse layer called the Stern layer. Stern layer is electrically neutral and having a width of atomic dimension. The Gouy-Chapman-Stern model treats each cation and anion as a hard sphere, each have the same radius r, with its charge located at the geometric centre of the sphere.

Let q is the charge density (charge/area) on the metal surface, then $-q$ is the total charge density on the diffuse layer. The ratio of potential difference between the metal surface and the bulk of the electrolyte to the charge density on the metal electrode surface [63] can be expressed as,

$$\frac{V}{q} = \frac{r}{\epsilon} + \frac{2RT}{Fq} \operatorname{arsinh}\left(\frac{q}{\sqrt{8RT\epsilon c}}\right) \tag{4.16}$$

where, V is the potential difference between the metal surface and electrolyte, r is the molecular radius, ϵ is the permittivity of the material, R is the ideal gas constant equal to 8.314472 J/mol/K, T is temperature in Kelvin, F is Faraday constant equal to 96485.3383 sA/mol, c is molar concentration. Equation (4.16) is of the form expected for series connected capacitors, thus the reciprocal of the overall capacitance can be written as the sum of reciprocal of two capacitors, each representing one of the elements of which the double layer is formed.

$$\frac{1}{C} = \frac{1}{C_{inner}} + \frac{1}{C_{outer}} \tag{4.17}$$

$$\frac{1}{C_{inner}} = \frac{r}{\epsilon} \tag{4.18}$$

$$\frac{1}{C_{outer}} = \frac{2RT}{Fq} \operatorname{arsinh}\left(\frac{q}{\sqrt{8RT\epsilon c}}\right) \tag{4.19}$$

The inner layer (Helmholtz layer) has a width equal to molecular radius (r) and the outer layer is diffuse layer. These two layers constitute the double layer of supercapacitor. Let there is N layers in the electrode, N_s supercapacitor units connected in series and N_p units connected in parallel. Then the equation (4.16) can be modified for voltage as,

$$V = \frac{N_s Q_c r}{N_p N \epsilon \epsilon_0 A} + \frac{N N_s 2RT}{F} \operatorname{arsinh}\left(\frac{Q_c}{N_p N^2 A \sqrt{8RT\epsilon\epsilon_0 c}}\right) \tag{4.20}$$

where, Q_c is the total charge on the metal electrode and V is the supercapacitor voltage including drop across equivalent series resistance. Equation (4.20) (Stern equation) is used for calculating voltage across supercapacitor during charging and discharging. The voltage drop across the equivalent DC series resistance (R_{sc}) is subtracted from the voltage from equation (4.20) to get terminal voltage of supercapacitor. Molar concentration c (mol/m^3) is calculated by using equation (4.21).

$$c = \frac{0.86}{8 N_A r^3} \tag{4.21}$$

Where, N_A is Avogadro constant equal to 6.0221×10^{23} mol^{-1}.

4.2.1 Self Discharge of Supercapacitor

Ultracapacitor's charge separation distance is in the range of molecular radius. Many irregularities can occur in this short distance, which leads to a small exchange of charge carriers between the electrode and electrolyte and a gradual discharge. This is called self discharge or leakage current. Leakage current mainly depends on voltage, capacitance, chemical stability and temperature of the electrode and electrolyte. In standby mode operation, supercapacitor voltage decreases due to self discharge. The over potential (deviation from equilibrium voltage) and rate of electrochemical reaction are related

by Tafel equation. Over potential is the deviation of metal electrolyte interface voltage from voltage at equilibrium (reversible potential). On a single electrode structure the Tafel equation can be stated as,

$$\Delta V = M \ln\left(\frac{i}{i_0}\right) \tag{4.22}$$

where, ΔV is the overpotential, M is Tafel slope, i is the current density and i_0 is the exchange current density. Exchange current density is the current density at equilibrium condition. For a supercapacitor, standby condition can be considered as an equilibrium condition because there is no net charging or discharging occur at this condition. The current during standby mode is the leakage current. Hence exchange current can be replaced by leakage current. The self discharging current depends on the overpotential, maximum voltage in the supercapacitor and the voltage across the supercapacitor. Then the Tafel equation [65] can be modified to represent the self discharging current of supercapacitor as,

$$I_{sd} = Ai_0 N \exp\left[\frac{\alpha F\left(\frac{V}{N_s} - \frac{V_{max}}{N_s} - \Delta V\right)}{RT}\right] \tag{4.23}$$

where, I_{sd} is the self discharging current, A is the interfacial area between electrodes and electrolyte, i_0 is the exchange current density, α is the charge transfer coefficient ($0 < \alpha < 1$), V_{max} is the maximum voltage and ΔV is the overpotential. Exchange current (Ai_0) equals to the leakage current of ultracapacitor. Self discharge occur in the standby mode, that is the charge or discharge current equal to zero. During charging and discharging of ultracapacitor self discharge current is taken as zero and during standby condition it is calculated using (4.23). There should be some minimum charge (Q_{min}) in the supercapacitor for self discharging to happen. The self discharging current of ultracapacitor is modelled using the variable I_{sdt} which is defined as,

$$I_{sdt} = \begin{cases} I_{sd} & : i = 0 \text{ and } Q_c > Q_{min} \\ 0 & : otherwise \end{cases}$$

i is the supercapacitor discharging current (A).

4.2.2 Complete Super Capacitor Model

The complete supercapacitor modelling include the calculation of SOC, charge/discharge voltage and the self discharging current. Fig. 4.4 shows the complete supercapacitor model. For the calculation of total charge in the supercapacitor, initial charge (Q_{int}) is

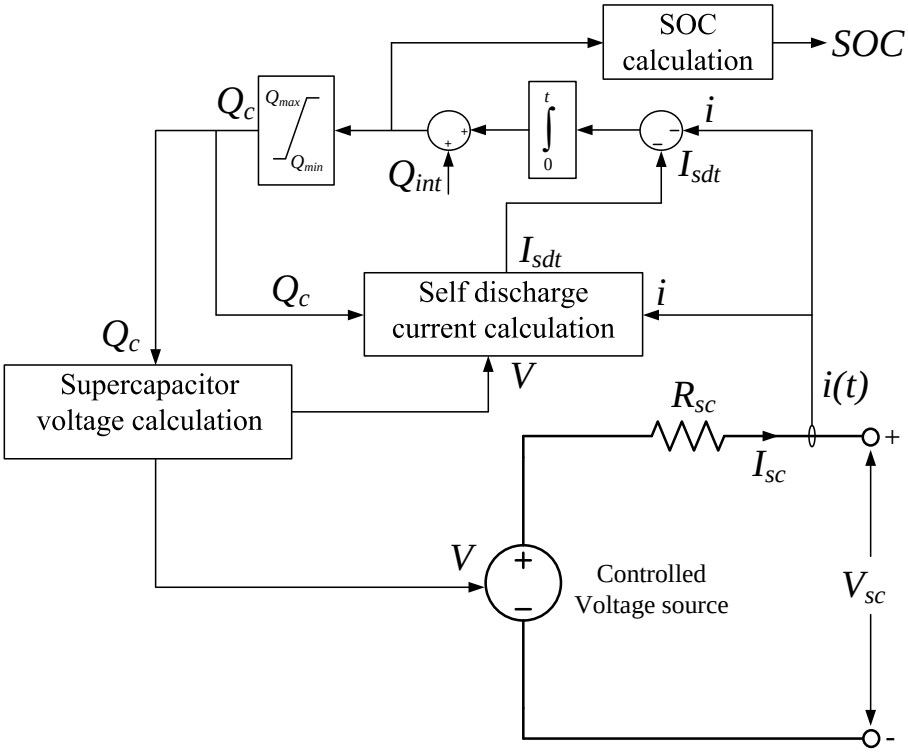

Fig. 4.4 Supercapacitor model.

required which can calculate using the initial voltage in the supercapacitor. The total charge can be expressed as,

$$\begin{aligned} Q_c &= Q_{charge} - Q_{sd} + Q_{int} \\ &= \int_0^t (-i)dt - \int_0^t I_{sd}dt + Q_{int} \end{aligned} \tag{4.24}$$

where, Q_{sd} is the charge lost due to self discharging and i is the supercapacitor discharging current. Maximum charge in the supercapacitor is $Q_{max} = CV_{max}$. The SOC for a fully charged supercapacitor is 100% and for an empty supercapacitor is 0%. The SOC is calculated as,

$$SOC = \frac{Q_c}{Q_{rate}} 100 \tag{4.25}$$

where, Q_c is the charge in the supercapacitor and Q_{rate} is the rated charge of the ultracapacitor. Q_{rate} is the product of rated voltage and the capacitance of supercapacitor.

The stored energy in the supercapacitor can be calculated as,

$$E_{sc} = 0.5 C_{sc} V_{sc}^2 \tag{4.26}$$

The maximum voltage drop in the supercapacitor is limited to 80% of the rated voltage. The maximum exchanged energy of supercapacitor can be calculated as,

$$E_{scex} = \frac{1}{2} C_{sc} (V_{sc}^2 - V_{scmin}^2) \tag{4.27}$$

where, E_{scex} is the maximum energy drawn from supercapacitor and V_{scmin} is the minimum voltage across supercapacitor. Relating energy to the power,

$$S_{sc} \times t = \frac{1}{2} C_{sc} (V_{sc}^2 - V_{scmin}^2) \tag{4.28}$$

The connected load to the UPQC is 5 kVA. Maximum energy is drawn from the supercapacitor at 50% voltage sag for maintaining DC link voltage. For a sag duraion of 10 s, supercapacitor deliver maximum power of 20% of the connected load ($S_{sc} = 0.2 \times 5$ kVA). Then using (4.28), the capacitance of supercapacitor can be found as $C_{sc} = 0.331$ F. During voltage interruption, the fluctuating load power are delivered by the supercapacitor. Average load power is delivered by the battery and thus the supercapacitor capacitance mainly depends on the required performance during worst case voltage sag. The parameters of supercapacitor considered for the simulation study is given in Table 4.2. The voltage and current variation of supercapacitor with time is shown in Fig. 4.5 [3]. Initially ultracapacitor is charging with a constant current of 8A and after reaching

Table 4.2 Parameters Considered for Supercapacitor Characteristics.

Parameters	**Value**
Rated capacitance	0.35 F
Equivalent DC series resistance	$0.205\ \Omega$
Rated voltage	251 V
Surge voltage	265 V
Leakage current	0.5 mA
Operating temperature	25^o C

the rated voltage it stops charging. The voltage during standby condition is slightly decreasing due to self discharge.

The battery-supercapacitor hybrids can be classified based on whether the DC/DC

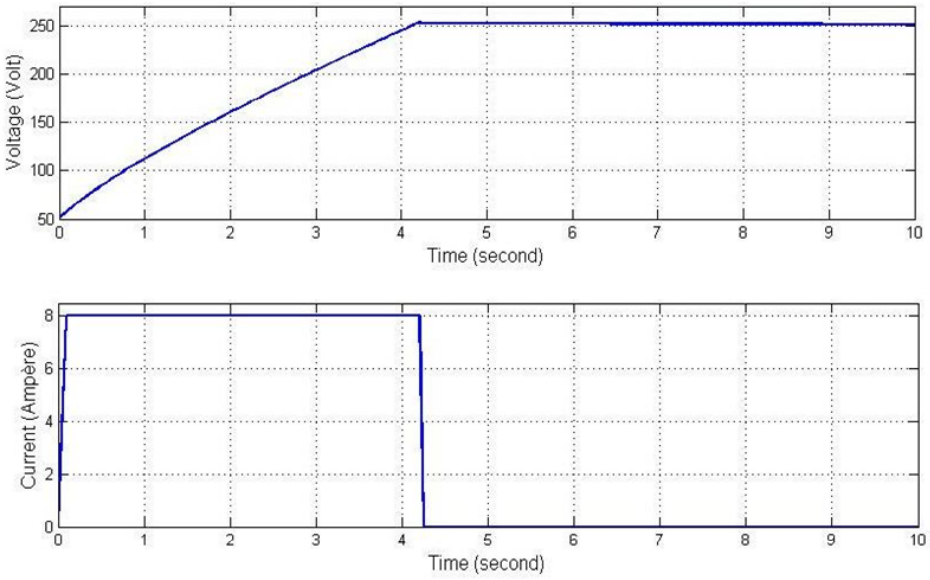

Fig. 4.5 Supercapacitor voltage and current as a function of time [3].

converters used or not, that are, passive, semi-active, and fully active topologies. In the passive structure, the battery and supercapacitor banks are connected in parallel and directly coupled to the UPQC DC link, the semi-active topology uses a DC/DC converter which enhances the performance of the passive hybrid but this topology impose additional cost because of the DC/DC converter and control circuitry used. The fully active hybrid uses two DC/DC converters for battery and supercapacitor, and as a result, the performance of the system is improved. But this increases the control complexity. Passive and semi active topologies are not suitable for UPQC applications. The battery and ultracapacitor are connected to the DC link through DC/DC converters so that each energy storage element is individually controlled.

4.3 Parameter Selection of Bidirectional Converter

The bidirectional buck-boost converter circuit is shown in the Fig. 4.3. The inductor and capacitor values determines the correct operation of the converter. For the battery DC-DC converter, during buck operation,

$$(V_{dc} - V_{batt})T_{on} = V_{batt}(T - T_{on}) \tag{4.29}$$

$$\frac{V_{batt}}{V_{dc}} = D_1 \tag{4.30}$$

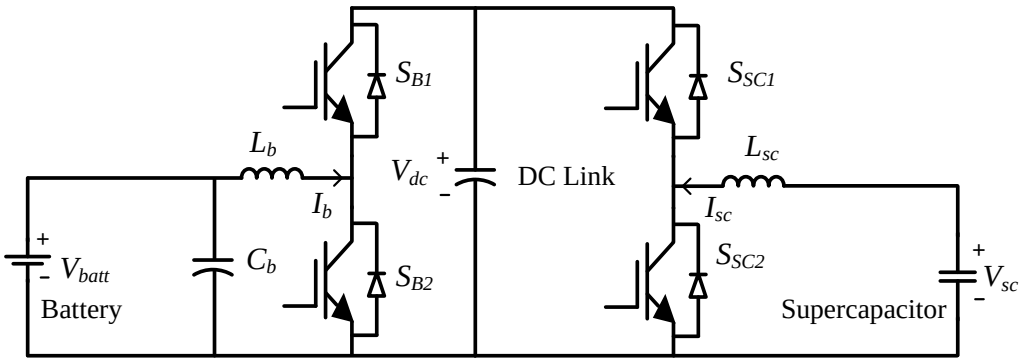

Fig. 4.6 Bidirectional buck-boost converter for battery-supercapacitor hybrid.

where, D_1 is the duty ratio for buck-boost converter and is equal to,

$$D_1 = \frac{T_{on}}{T} \tag{4.31}$$

where, T is the switching time period and T_{on} is the ON time of S_{B1}. The value of L_b [66] can be found as,

$$L_b = \frac{(V_{dc} - V_{batt})D_1}{\Delta I_b f} \tag{4.32}$$

The expression for C_b is,

$$C_b = \frac{\Delta I_b}{8\Delta V_{batt} f} \tag{4.33}$$

Similarly for supercapacitor, the value of L_{sc} can be found by,

$$L_{sc} = \frac{(V_{dc} - V_{sc})D_2}{\Delta I_{sc} f} \tag{4.34}$$

For the battery DC-DC converter, during boost operation the value of inductance and capacitance [66] are,

$$L_b = \frac{V_{batt} D_3}{\Delta I_b f} \tag{4.35}$$

$$C_b = \frac{I_b D_3}{\Delta V_{batt} f} \tag{4.36}$$

The value of L_{sc} during boost operation is,

$$L_{sc} = \frac{V_{sc} D_4}{\Delta I_{sc} f} \tag{4.37}$$

The voltage and current ripple are limited to 5%. The maximum load power during voltage interruption is $P_0 = 3.5$KVA. Battery nominal voltage is 300V. Then I_b can

found as,

$$I_b = \frac{P_0}{V_{batt}} \tag{4.38}$$

The battery and supercapacitor DC/DC converters inductance value is calculated for minimizing converter current ripple using (4.32), (4.35) and (4.34), (4.37) respectively and the maximum value of inductance is chosen. The switching frequency used for simulation is 20KHz and the maximum duty cycle is 1. The battery DC/DC converter capacitance value is calculated for minimizing voltage ripple using (4.33) and (4.36) and the maximum value of capacitance is chosen. The L and C values for minimum current and voltage ripple are shown in Table. 4.3.

Table 4.3 L and C values of DC/DC converters.

Parameters	**Value**
Battery converter inductance (L_b)	35 mH
Battery converter capacitance (C_b)	60 μF
Supercapacitor converter inductance (L_{sc})	30 mH

4.4 Summary

The Matlab/Simulink simpowersystems library model is used for battery and ultracapacitor models. Battery battery charge and discharge model uses the parameters extracted from the battery discharge curve. The temperature effect on the battery is not considered in this model. Super capacitor terminal voltage is modelled using Stern equation and internal resistance. The ultracapacitor self discharge is modelled using Tafel equation. For controlling terminal voltage of battery and ultracapacitor individually, two DC/DC converter is needed. The proper selection of inductance reduce the current ripple while the capacitance reduce the voltage ripple. The battery-supercapacitor charge and discharge can be controlled using DC/DC converter.

CHAPTER 5

PROPOSED UPQC WITH BATTERY-ULTRACAPACITOR HYBRID STORAGE

Conventional UPQC does not have the capability to mitigate voltage interruption because it has no energy storage devices like battery and ultracapacitor connected to its DC link. In the proposed system a battery and ultracapacitor is connected to the DC link as energy storage devices. Ultracapacitor is faster than battery and it can deliver power quickly. Battery can deliver power for long time. Sudden variations in the load and other disturbances may cause deep discharging of battery. This reduces the battery life time. Diverting all the DC link disturbances to the supercapacitor improves the battery life time and it reduces the stress on the battery. Moreover supercapacitor can deliver power during voltage sag and maintain DC link voltage constant there by reducing the burden on shunt APF.

The UPQC with battery ultracapacitor energy storage system has two mode of operation namely grid connected and voltage interruption mode. In grid connected mode battery charges from the DC link through the DC/DC converter. DC/DC converter controls the charging of battery and disconnect battery from the DC link when it is fully charged. Ultracapacitor on the other hand charges or discharges according to the system condition. During normal voltage level and voltage swell supercapacitor charges and during voltage sag it discharges. In all these conditions the DC link voltage is maintained constant. In voltage interruption mode the battery discharges to maintain a constant DC link voltage. Ultracapacitor takes all the DC link fluctuations due to sudden load change there by increasing battery life. In grid connected mode the shunt APF works in current control mode and series APF works in voltage control mode. During voltage interruption shunt APF works in voltage control mode to maintain a constant rms voltage at the load terminal and series APF is removed from the system. The combined control of battery-ultracapacitor DC/DC converters and UPQC is explained in this Chapter.

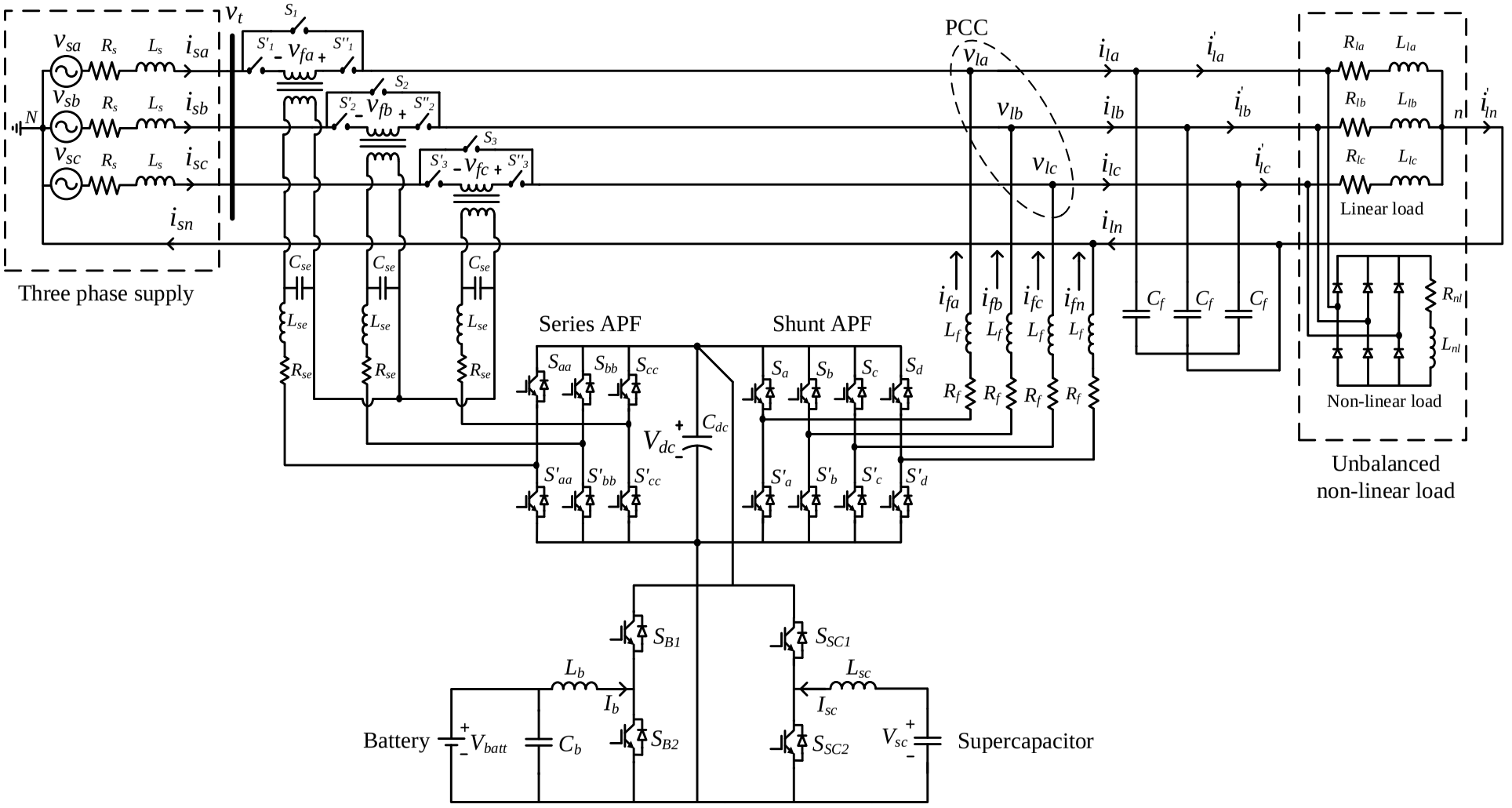

Fig. 5.1 Power circuit of UPQC with battery ultracapacitor hybrid.

5.1 Methodology of UPQC Operation with Battery Ultracapacitor Energy Storage

Fig. 5.1 shows the proposed configuration of UPQC that consists of DC/DC converters and battery-ultracapacitor energy storage. The purpose of battery in UPQC application is to enable UPQC to mitigate voltage interruption. Supercapacitor reduces the stress on the battery and deliver or absorbs power during sag/swell conditions. The algorithm of battery, ultracapacitor and UPQC operation can be arrived as given in Fig. 5.2. When there is no voltage sag, swell and interruption (normal voltage condition), the series inverter injects no voltage and shunt inverter injects required current to mitigate load current power quality problems. Apart from that, the shunt APF maintain the DC link voltage with the help of a PI controller. Shunt APF draws power from the grid to maintain DC link voltage, this power includes the power drawn by battery and ultracapacitor for charging and the converter losses. The battery charges in normal voltage condition. Supercapacitor charging system checks the DC link voltage so that in any condition the DC link voltage do not go below a set minimum voltage. When the grid voltage is normal ($0.9\,pu \leq |V_{ta1}^{+}|_{pu} \leq 1.1\,pu$) and DC link voltage is greater than the minimum voltage limit (in simulation, it is chosen 99% of rated DC link voltage), supercapacitor starts charging from DC link through DC/DC converter until it reaches maximum SOC. The control of DC link voltage by shunt inverter is a slow process compared to supercapacitor response time. Hence in grid connected mode, whenever the DC link voltage goes below 99% of rated voltage, supercapacitor discharges to support shunt inverter for maintaining DC link voltage. When the DC link voltage goes below the set lower limit, battery goes to stand by mode to reduce the stress on the shunt inverter.

When voltage sag occur, battery goes into standby mode. The main role of supercapacitor in grid connected mode is to support shunt inverter to reduce the DC link voltage fluctuations. The faster charge/discharge capability of supercapacitor can be effectively utilize in the sag/swell condition. Supercapacitor discharge or goes standby mode (neither charges nor discharges) according to the DC link voltage. If the shunt inverter itself maintain DC link voltage, super capacitor goes to stand by mode. Other wise supercapacitor discharges to support shunt inverter for maintaining DC link voltage. When

voltage sag occur, the series inverter inject voltages in series with the source voltage to maintain load voltage at the required level and the shunt inverter injects current such that source current is sinusoidal balanced and upf. When voltage swell occur, the DC link voltage increases and this extra power is used to charge the battery. The series APF injects voltage to maintain load voltage and shunt inverter injects current to mitigate load current power quality problems. Additionally, the shunt inverter maintains the DC link voltage constant. The operation of supercapacitor during voltage swell is similar to that during voltage sag except that it charges when there is rated DC link voltage. The charging and discharging of battery and ultracapacitor is controlled in such a way that, it does not over charge in any condition. When voltage interruption ($0.5\,pu > |V^{+}_{ta1}|_{pu}$ or $|V^{+}_{ta1}|_{pu} > 1.5\,pu$, where $|V^{+}_{ta1}|_{pu}$ is rms value of fundamental positive sequence source voltage in per unit) occur, battery must discharge to maintain the DC link voltage constant. The average load power is supplied by the battery while load fluctuations are managed by the supercapacitor. During voltage interruption, the series inverter is isolated from the system and shunt inverter operates in voltage control mode to maintain the load voltage.

5.2 Grid Connected Mode of UPQC with Battery Ultracapacitor Energy Storage

Grid connected mode has three voltage conditions, normal voltage ($0.9pu \leq |V^{+}_{ta1}|_{pu} \leq 1.1pu$), balanced voltage sag ($0.5pu \leq |V^{+}_{ta1}|_{pu} < 0.9\,pu$) and balanced voltage swell ($1.1\,pu < |V^{+}_{ta1}|_{pu} \leq 1.5\,pu$). The fundamental positive sequence voltage extraction, reference voltage generation of series inverter, reference current generation of shunt inverter, sag/swell detection algorithm and UQPC control method were explained in Chapter-3. This section deals with the combined operation and control of battery-supercapacitor hybrid storage and UPQC.

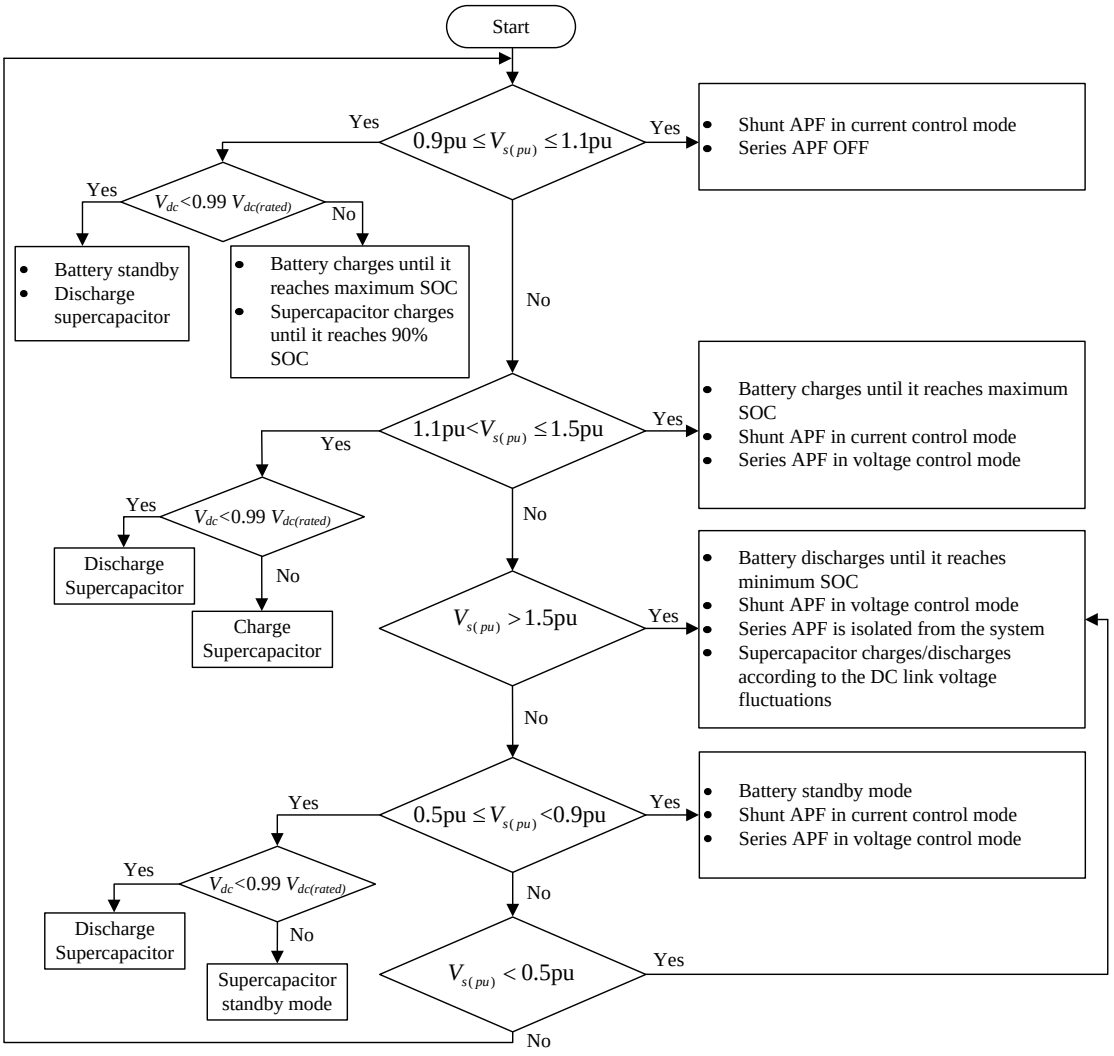

Fig. 5.2 Methodology of UPQC operation with battery supercapacitor energy storage.

5.2.1 Control of Battery and Ultracapacitor During Normal Voltage Condition

The series inverter is OFF (S_1, S_2, S_3 are ON and $S_1^{'}, S_1^{''}, S_2^{'}, S_2^{''}, S_3^{'}, S_3^{''}$ are OFF) in this condition because there is no need of injecting voltage in series with the source. Connecting series inverter injection transformer in series with the source will cause additional voltage drop across it. The control of shunt inverter is explained in Chapter-3. Fig. 3.4 explains the control of shunt inverter. Now the PI controller parameters is adjusted such that the P_{loss} term includes the power drawn by the battery and supercapacitor from the DC link. The battery charges in this condition until it reaches the maximum SOC. Ultracapacitor charges or discharges according to DC link voltage. The charging and discharging of battery and ultracapacitor is controlled through DC/DC converter.

5.2.1.1 *Control of battery charging*

Battery DC/DC converter operates in buck mode during battery charging. Fig. 5.1 shows the battery and DC/DC converter connected to DC link of UPQC. Switch S_{B1} is controlled by the PWM controller and switch S_{B2} is OFF. Battery charging current has a maximum limit, if the current goes above that, the battery will damage. The saturation block limits the battery charging current and duty cycle. Duty cycle (D_1) should be in the range of 0 to 1. The battery charging control method is shown in Fig. 5.3. SOC is calculated using (4.7) and $SOC = 100\%$ for fully charged condition. When the battery is fully charged both the DC/DC converter switches turned OFF and the battery goes to standby mode.

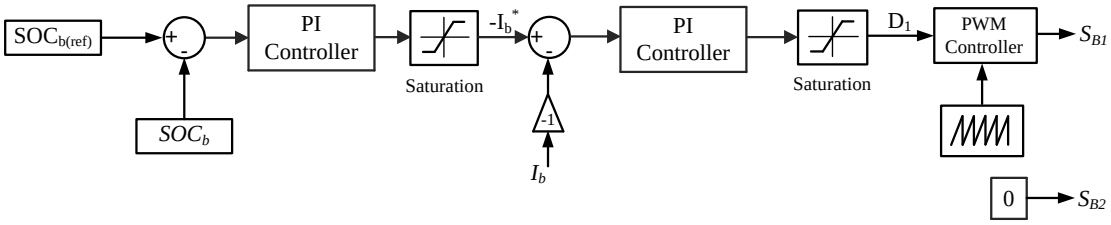

Fig. 5.3 Control of battery charging.

The PWM controller compare the duty cycle (D_1) with a sawtooth signal having negative peak 0 and positive peak 1. The output of the comparator is the switching pulse for switch S_{B1}.

$S_{B1} = 1$ when $D_1 \geq v_{saw}$, and

$S_{B1} = 0$ when $D_1 < v_{saw}$.

Where, v_{saw} is the sawtooth signal's instantaneous magnitude.

5.2.1.2 *Control of supercapacitor DC/DC converter*

Supercapacitor charges when DC link voltage has more voltage than the set minimum voltage limit. Due to sudden changes in load and other disturbances the DC link voltage may suddenly decrease. The PI controller takes some cycles to regain the DC link voltage. During this time supercapacitor has to deliver power and maintain the DC link voltage. The charging and discharging control of supercapacitor during normal source voltage level is shown in Fig 5.4(a) and (b) respectively. When supercapacitor charging from very low voltage, it draws very large current. This may damage the

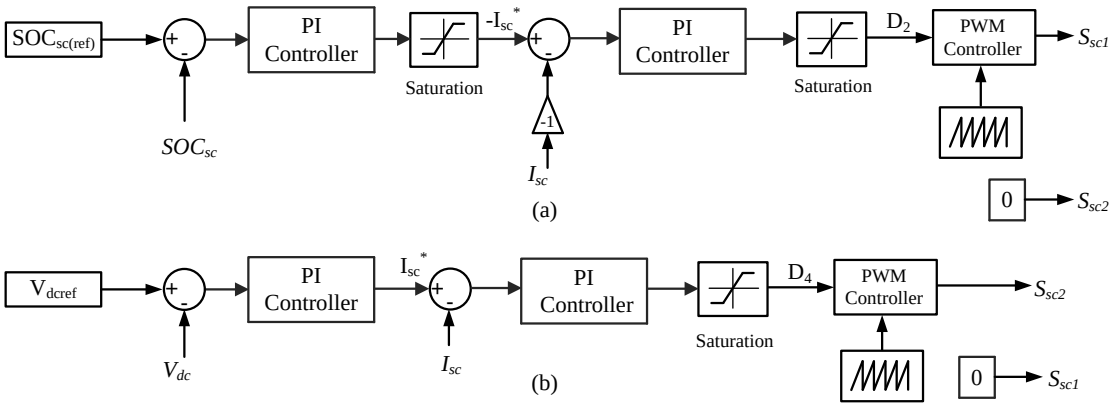

Fig. 5.4 Control of supercapacitor DC/DC converter for: (a) supercapacitor charging (b) supercapacitor discharging.

supercapacitor. To avoid this a current limiter is used in the supercapacitor charging controller. Supercapacitor charges until it reaches 90% SOC due safety considerations. Other wise it may overcharge during voltage swell and other sudden DC link voltage increasing cases.

5.2.2 Control of Battery and Ultracapacitor During Voltage Sag

The UPQC series converter injects voltage in series with the grid voltage to maintain rms value of load voltage constant. The detection of sag and swell and control of series and shunt APF are explained in Chapter-3. Fig. 3.7 shows the control strategy of UPQC. During voltage sag ($0.5\,pu \leq |V_{ta1}^{+}|_{pu} < 0.9\,pu$) the DC link voltage starts decreasing because series inverter draw power from it to inject voltage. Shunt inverter tries to maintain the DC link voltage constant by drawing power from the grid. The proposed topology can mitigate up to 50% voltage sag. During high voltage sag, the DC link voltage is reduced much and the inverter operation becomes disturbed. To avoid this whenever the DC link voltage goes below 99% of its rated value, the ultracapacitor discharges to maintain the DC link voltage. Battery charging in voltage sag condition introduces more stress on the shunt inverter. Hence both the DC/DC converter switches S_{B1} and S_{B2} are OFF at this condition. Battery will neither charge nor discharge during voltage sag. The control strategy for supercapacitor discharging is shown in Fig. 5.4(b). Both the supercapacitor DC/DC converter switches S_{SC1} and S_{SC2} are OFF for supercapacitor stand by mode.

5.2.3 Control of Battery and Ultracapacitor During Voltage Swell

The shunt inverter injects a current to the PCC to supply load reactive power and to eliminate harmonics from the source current. The high grid voltage increases the DC link voltage above rated value. The extra power from the grid can use to charge the battery while shunt inverter tries to maintain the DC link voltage. The battery charging control is shown in Fig. 5.3. Most of the time DC link voltage has voltage greater than 99% of its rated value, in that case supercapacitor charges from the DC link and the control strategy is shown in Fig. 5.4(a). The series inverter injects voltage in series with the grid voltage to maintain the load voltage rms value constant. The voltage swell ($1.1\,pu < |V_{ta1}^{+}|_{pu} \leq 1.5\,pu$) is less frequent when compared to voltage sag.

5.2.4 Complete Control Strategy in Grid Connected Mode

The battery converter, ultracapacitor converter, series APF and shunt APF control strategy in grid connected mode is shown in Fig. 5.5. In grid connected mode battery is either charging or standby mode. Super capacitor charging and discharging is determined by the sag, swell, DC link voltage drop below a reference value and SOC. In battery alone system, battery has to discharge for supporting DC link during large voltage fluctuations. Deep battery discharge will reduce the battery life time. When supercapacitor added to the system, DC link is supported by supercapacitor during high DC link voltage fluctuations. Thus frequent battery discharge is avoided.

5.3 Operation of UPQC with Battery-Ultracapacitor Storage in Voltage Interruption Condition

When voltage interruption occur, the load power is delivered by the battery-ultracapacitor hybrid energy storage system. This happens when the supply voltage goes below 0.5 pu or above 1.5 pu. The series inverter can mitigate up to 50% source voltage variations (for high sag compensation, series invcerter rating should be high). Compensating higher voltage disturbances need high rating series inverter. Also the cost of transformer and filter unit increases. Hence the compensation capability of series inverter is limited

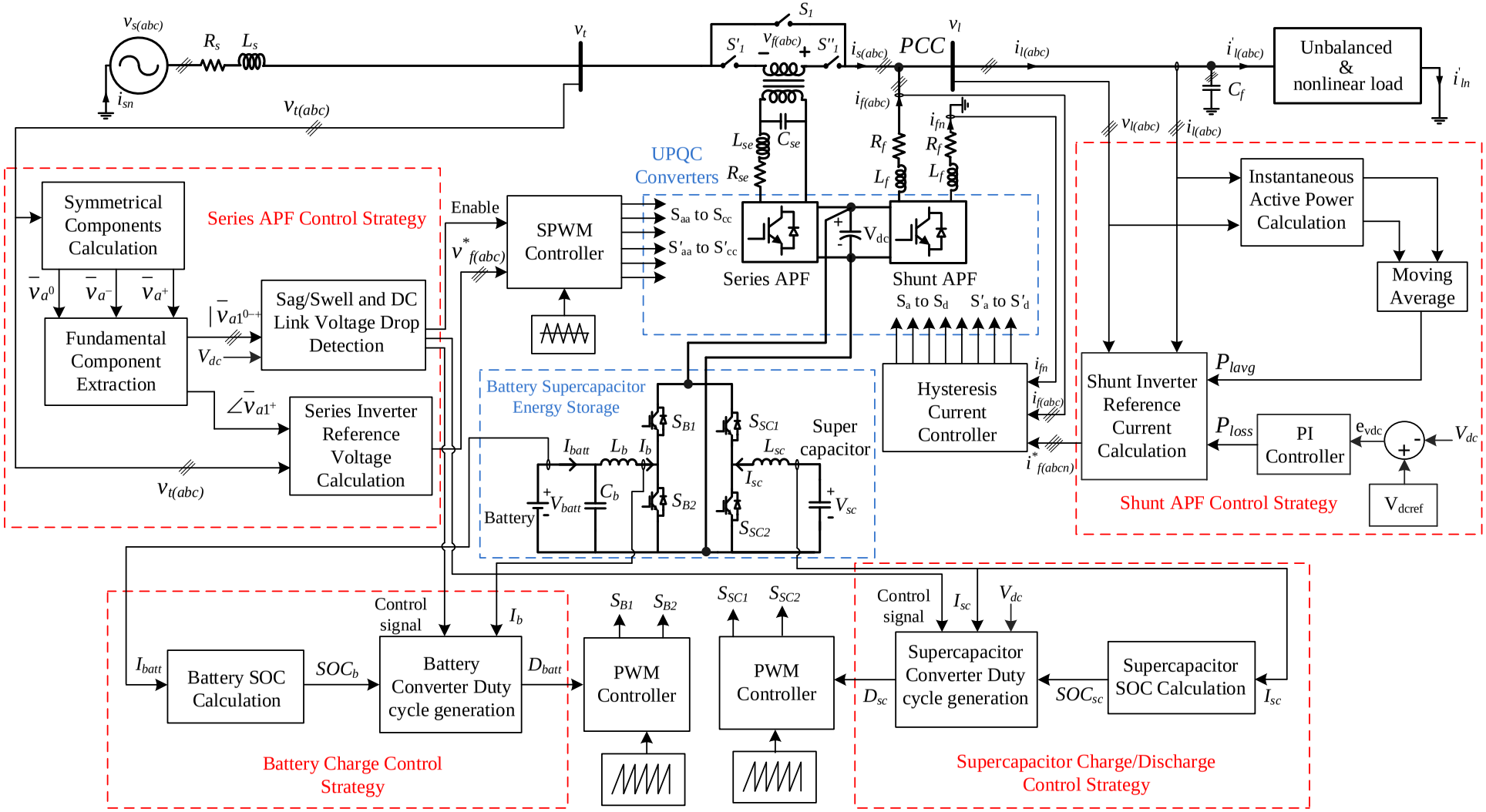

Fig. 5.5 Complete control of battery, ultracapacitor and UPQC in grid connected mode.

to 50% sag and swell. When voltages violate this limit the energy stored in the battery and ultracapacitor is used to deliver power to load. One of the UPQC converter (series or shunt) is used as inverter to maintain sinusoidal balanced load voltage. Using shunt inverter for this purpose is the simplest methode. The power circuit of the whole system during voltage interruption ($|V_{ta1}^{+}|_{pu} < 0.5$ pu or $|V_{ta1}^{+}|_{pu} > 1.5$ pu) is shown in Fig. 5.6. Whenever the source voltage fundamental rms value goes below 0.5pu or above 1.5pu,

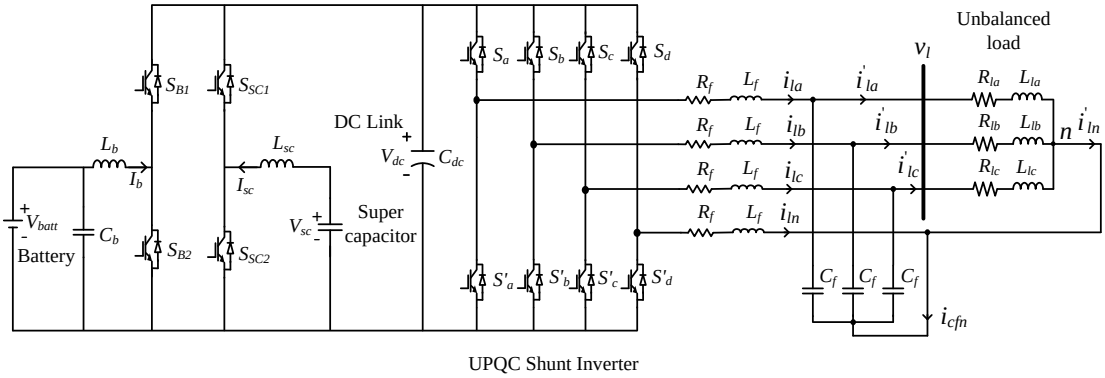

Fig. 5.6 Power circuit of whole system during voltage interruption.

the series inverter and source terminals are isolated from the system by switching OFF series and bypass switches ($S_1, S_2, S_3, S_1', S_2', S_3', S_1'', S_2'', S_3''$). The shunt inverter abc phase legs works in voltage control mode and the neutral leg works in current control mode to provide a balanced load voltage.

5.3.1 Shunt Inverter Control During Voltage Interruption

Shunt inverter works in current control mode in grid connected mode of operation. It injects current to mitigate load current power quality problems. But during voltage interruption the load voltage should maintain, for that shunt inverter must operate in voltage control mode. An LC filter is used to filter switching harmonics from the output voltage. The inductor L_f is used for current harmonics filtering in current control mode. The same inductor can use in LC filter for voltage switching harmonics filtering. The resister R_f provides necessary damping to the oscillations at the time of switching from grid connected mode to voltage interruption condition and vice versa. The capacitor C_f is needed for filtering switching harmonics in voltages. It can be used either permanently connected at the load terminal or connecting only at the time of voltage interruption. But capacitor switching at the time of voltage interruption causes voltage

transients and it should be avoided. Hence the capacitor C_f is permanently connected to the load terminal. The shunt inverter treat capacitor (C_f) as a part of load in grid connected mode. Most of the load connected are inductive in nature and it draw reactive power from the shunt inverter. The capacitor deliver reactive power to the load and reduces the burden on the shunt inverter.

The load voltage after voltage interruption should synchronize with the voltage before interruption. Otherwise phase jump will occur in the load voltage. The phase angle of load voltage at the time of voltage interruption is extracted and used for generating load voltage reference. The load voltage reference during voltage interruption can be written as,

$$\begin{aligned} v_{la}^{*} &= \sqrt{2}V_l \sin(\omega t^{'} + \theta) \\ v_{lb}^{*} &= \sqrt{2}V_l \sin(\omega t^{'} - 2\pi/3 + \theta) \\ v_{lc}^{*} &= \sqrt{2}V_l \sin(\omega t^{'} + 2\pi/3 + \theta) \end{aligned} \tag{5.1}$$

Time $t^{'} = 0$ at the instant of supply voltage interruption. Angle θ is calculated from the instantaneous value of load voltage at the instant of supply voltage interruption. From equation (3.30), θ can be calculated as,

$$\theta = \omega\, t_{int} - \theta_1 \tag{5.2}$$

where, $-\theta_1$ is the phase angle of fundamental positive sequence terminal voltage (also equal to the phase angle of load voltage) and t_{int} is the time at which the voltage interruption occur. The exact time of voltage interruption can be detected by checking the voltage magnitude generated from (3.29). SPWM controller is used for producing switching pulses for the abc leg of shunt inverter. The control is similar to the control of series APF in voltage control mode. The load voltage should be balanced, for that the current through the filter capacitor (C_f) should be balanced. That is i_{cfn} should be zero. This can be written as,

$$i_{ln}^{*} = i_{cfn} - i_{ln}^{'} \tag{5.3}$$

$$i_{cfn} = 0 \tag{5.4}$$

where, i_{ln}^{*} is the inverter neutral leg current reference and $i_{ln}^{'}$ is the load neutral cur-

rent. From (5.3) and (5.4), reference current for neutral leg (switches $S_d, S_d^{'}$) can be calculated as,

$$i_{ln}^{*} = -i_{ln}^{'} \tag{5.5}$$

The neutral leg of inverter operates in current control mode and hysteresis current controller is used for generating switching pulses for this leg. The complete control of shunt inverter during voltage interruption is shown in Fig. 5.7.

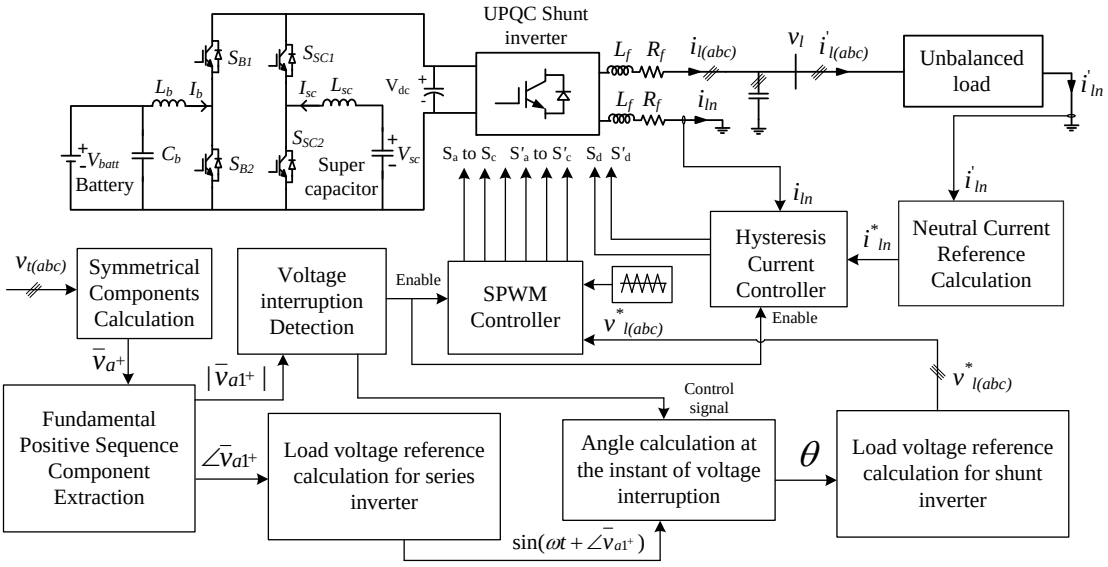

Fig. 5.7 Complete shunt inverter control during voltage interruption.

5.3.2 Control of Battery Ultracapacitor Hybrid During Voltage Interruption

Life cycle (total number of charge-discharge cycle) of battery highly dependent on the depth of discharge. When a sudden load increase occur battery discharge current increases quickly. Frequent load fluctuations cause battery deep discharge. Frequent charging and discharging increases the stress on battery and it may have detrimental effect on the lifetime and performance of the battery. Ultracapacitor has high power density. The charge/discharge efficiency of an ultracapacitor is much higher than that of any battery, resulting in reduced system losses, which contributes to higher efficiency and prolonged power system life as a result of lower operating temperature and smaller heat sink. Also ultracapacitor has higher number of charge-discharge cycles compared to battery and its charge and discharge is faster than that of battery. Since superca-

pacitor can react faster to quick fluctuations, the stress on the battery can be reduced. Thus ultracapacitor manages high load fluctuations while battery deliver average load power. By diverting high fluctuating power from battery, battery depth of discharge is reduced. Thus the control scheme increases the battery life by preventing deep battery discharge. The DC/DC converter control scheme for battery and ultracapacitor during voltage interruption is shown in Fig. 5.8.

Battery minimum SOC is limited to 50% to avoid battery full discharge. If there is no grid voltage and the battery discharges to 50% SOC, then the complete system will shutdown. The ultracapacitor alone cannot supply the load for long time because it discharges faster than battery. The controller is enabled by the voltage interruption

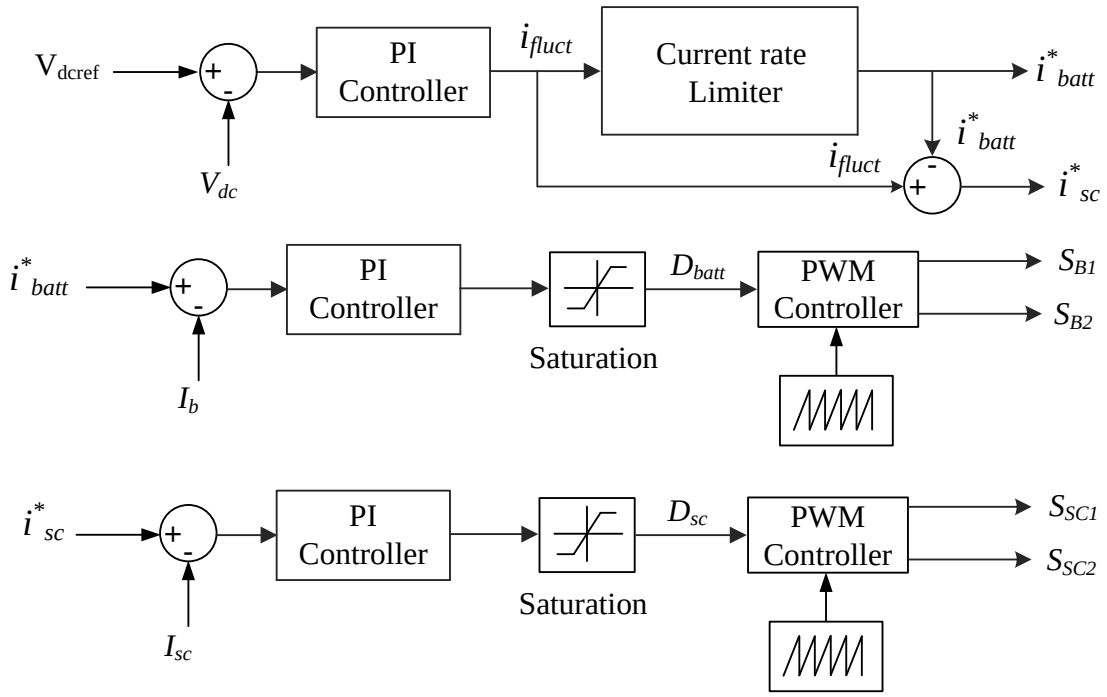

Fig. 5.8 Control of battery-ultracapacitor DC/DC converters during voltage interruption.

detector. The difference between the actual DC link voltage and the reference voltage is generated. This difference upon passing through PI controller results in reference current for energy storage. This is the current injected or absorbed by the energy storage devices to maintain DC link voltage constant. The reference current upon passing through rate limiter gives battery current reference. The rate limiter block limits rate of change of battery current. In practical applications, a low pass filter can use instead of rate limiter. The high discharge rate of battery is avoided by using rate limiter which in turn increases the battery cycle life. The difference between the total reference current

and battery reference current is the high frequency fluctuating component. This current is given as the reference current for supercapacitor.

The discharge current of battery and reference current are compared and the difference is given to a PI controller. PI controller generates the duty cycle of the battery converter which is given to a PWM controller to generate the switching pulses. The duty cycle ranges from 0 to 1. Hence a saturation block is used to limit the duty cycle value. The same control is adopted for supercapacitor as well. By proper tuning of PI controller the error can be reduced to zero. By this control scheme the average load power is supplied by the battery while the load fluctuations are managed by supercapacitor.

5.4 Summary

Conventional UPQC cannot compensate voltage interruption because it has no energy storage devices connected to DC link. Battery and ultracapacitor are the best energy storage devices for UPQC applications. A combination of battery and ultracapacitor can take advantage of each kind of device to yield a power source of both high power density and high energy density. In grid connected mode series inverter mitigate voltage related power quality problems while shunt inverter mitigates current related power quality problems. Battery and ultracapacitor charging and discharging is controlled by DC/DC converters. The DC link voltage variations during sag and swell can effectively reduce by controlling ultracapacitor DC/DC converter. Ultracapacitor can be used to support the shunt APF to maintain a constant DC link voltage. During voltage interruption, the series inverter is isolated from the system and the shunt inverter deliver power to the load from battery-ultracapacitor energy storage system. The highly fluctuating load power is delivered by the supercapacitor and the average load power is delivered by the battery. The full discharging of battery reduces its life time. Battery DC/DC converter is controlled such a way that battery do not discharge below 50% SOC. By connecting supercapacitor the stress on the battery is reduced, thereby the battery life time is improved.

CHAPTER 6

SIMULATION RESULTS

For the complete UPQC compensated system shown in Fig. 5.1, a simulation study is conducted to verify its operation under different operating conditions. UPQC and battery-ultracapacitor system has two mode of operation namely grid connected mode and voltage interruption condition. This chapter gives the simulation analysis carried out on the system.

6.1 Grid Connected UPQC and Battery-Ultracapacitor Operation

As explained in the previous chapter, grid connected mode of operation includes normal voltage, voltage sag and voltage swell conditions. Parameter values of the system shown in Fig. 5.1 is given in Table 6.1. The same is used for simulation study. The battery-ultracapacitor charge/discharge depends on the supply voltage and DC link voltage level. This section gives the simulation results of UPQC and battery ultracapacitor energy storage system during grid connected mode of operation.

6.1.1 Normal Voltage Operation

During normal voltage, series APF injects no voltage to the line as shown in Fig. 6.1(b) because the source voltage has enough magnitude to deliver power to the load. The source terminal voltage and load voltage are shown in Fig. 6.1(a) and Fig. 6.1(c)respectively. The load draws an unbalanced non linear current from the PCC. To maintain a balanced unity power factor fundamental current at the source terminal, shunt inverter injects a current to the PCC which is shown in Fig. 6.2(b). Shunt APF deliver the load reactive power to maintain unity power factor at the PCC terminal. The shunt inverter injected current eliminates the unbalance and harmonics from source current. The source current and load current are shown in Fig. 6.2(a) and Fig. 6.2(c) respectively.

Table 6.1 Parameter values for simulation study

Parameter	Value
UPQC DC link voltage, capacitance (V_{dc}, C_{dc})	700 V, 2000 μF
Utility grid voltage ($V_{s(L-L)}$)	400 V
Fundamental frequency	50 Hz
Feeder resistance, inductance	0.05 Ω, 0.01 mH
Shunt APF L_f, R_f, C_f	20 mH, 4 Ω, 80 μF
Series APF L_{se}, R_{se}, C_{se}	1.1 mH, 1.6 Ω, 200 μF
K_p, K_i for DC link PI controller	140, 20
Hysteresis band ($\pm h$)	0.1 A
SPWM switching frequency for series APF	7 kHz
Battery nominal voltage	300 V
Battery rated capacity	20 mAh
Battery converter L_b, C_b	35 mH, 60 μF
Supercapacitor rated capacitance	0.35 F
Supercapacitor rated voltage	251 V
Supercapacitor converter inductance (L_{sc})	30 mH
K_p and K_i for supercapacitor charge controller	0.8 and 0.3 for voltage PI controller 0.6 and 0.3 for current PI controller
K_p and K_i for supercapacitor discharge controller	0.5 and 0.2 for voltage and current PI controller
K_p and K_i for battery charge controller	0.7 and 0.5 for voltage PI controller 1 and 0.5 for current PI controller
DC/DC converter switching frequency	20 kHz
Unbalanced nonlinear load	Z_a= 100+j 20 Ω Z_b= 75+j 47 Ω Z_c= 55+j 24 Ω 3-ϕ full bridge diode rectifier supplying an R-L (100 Ω - 1 H) load

During normal voltage level the battery and ultracapacitor charges. Battery charges to 100% SOC while supercapacitor charges until it reaches 90% SOC. A 10% SOC margin is provided to avoid supercapacitor overcharging under transient conditions. When the supercapacitor converter switched ON at 0.05 s, it suddenly discharges (if it is initially charged) to maintan the DC link voltage at reference value. This current variaion is shown in Fig .6.3(h). After DC link voltage attains steady state value (700 V), battery and ultracapacitor started charging. Battery charges with a constant current which is shown in Fig. 6.3(d). The DC link voltage variation, average power extracted by a moving average filter, change in battery SOC, battery discharge current (negative for charging current) , battery voltage variaton, change in supercapacitor SOC, supercapacitor terminal voltage change and supercapacitor discharge current during normal voltage operation are shown in Fig. 6.3(a-h). When battery and ultracapacitor charges,

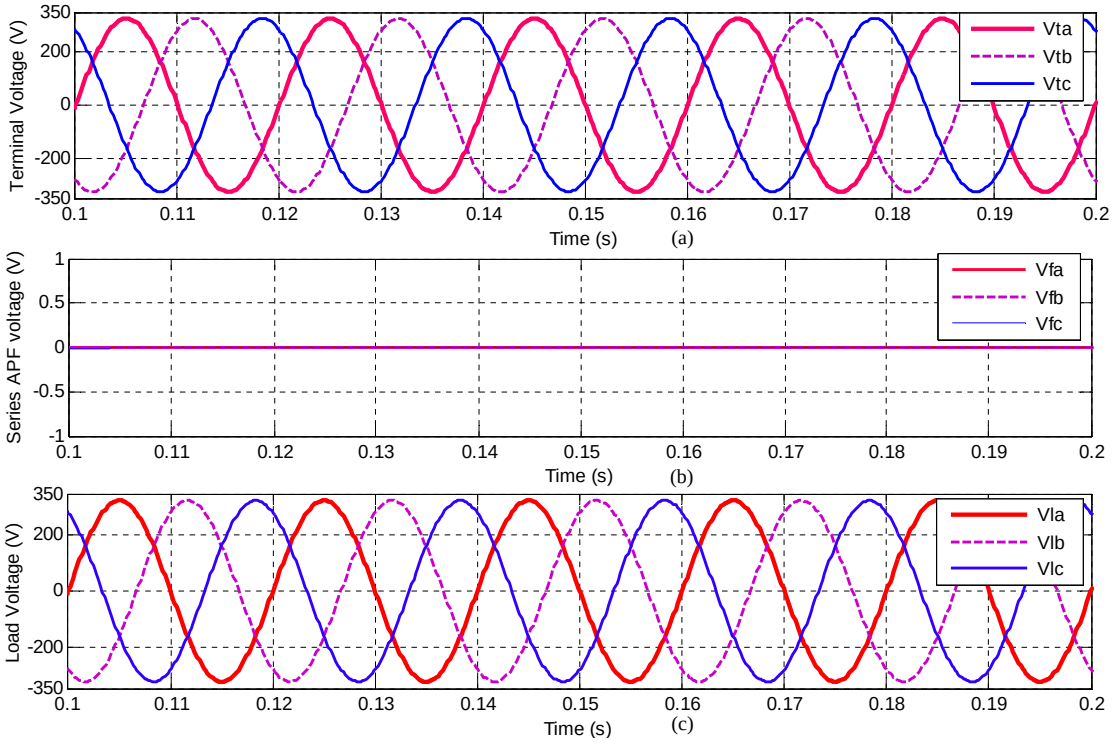

Fig. 6.1 (a) Source terminal voltage (b) Series inverter injected voltage (c) Load voltage.

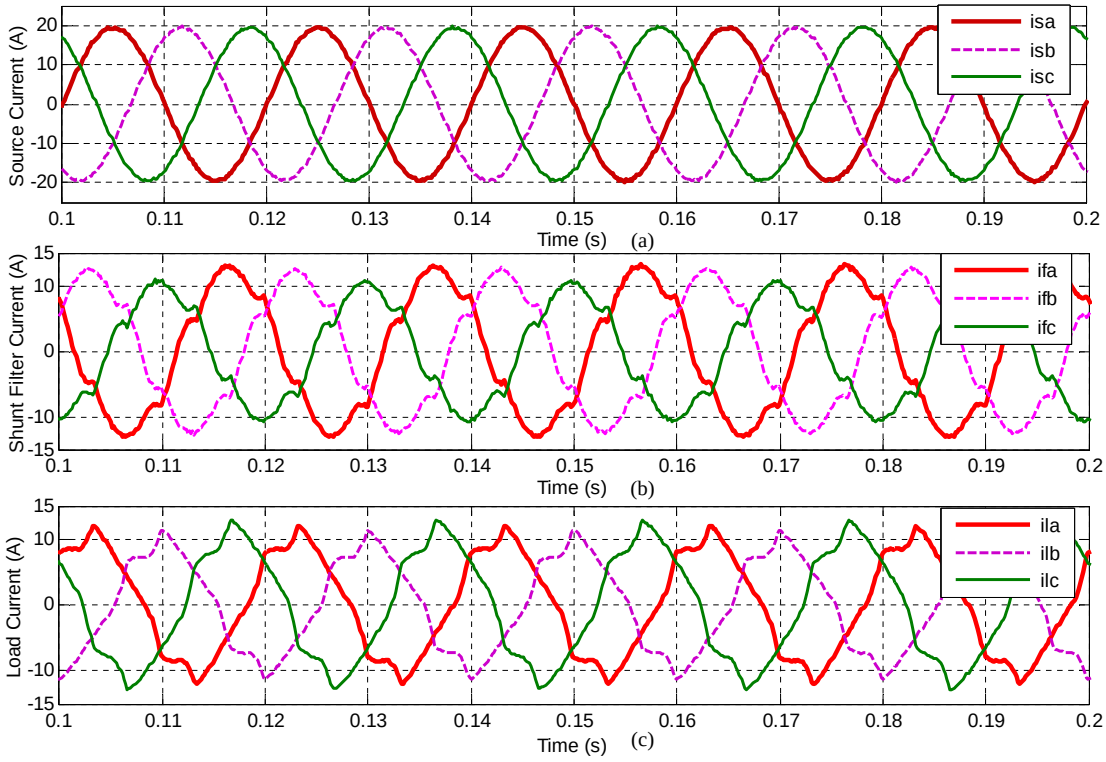

Fig. 6.2 (a) Source current (b) Shunt inverter injected current (c) Load current.

shunt APF maintain the DC link voltage by drawing power from the grid. This power includes the power drawn by the battery and ultracapacior for its charging and the losses in the converter. Whenever the DC link voltage goes below 99% of rated value due to

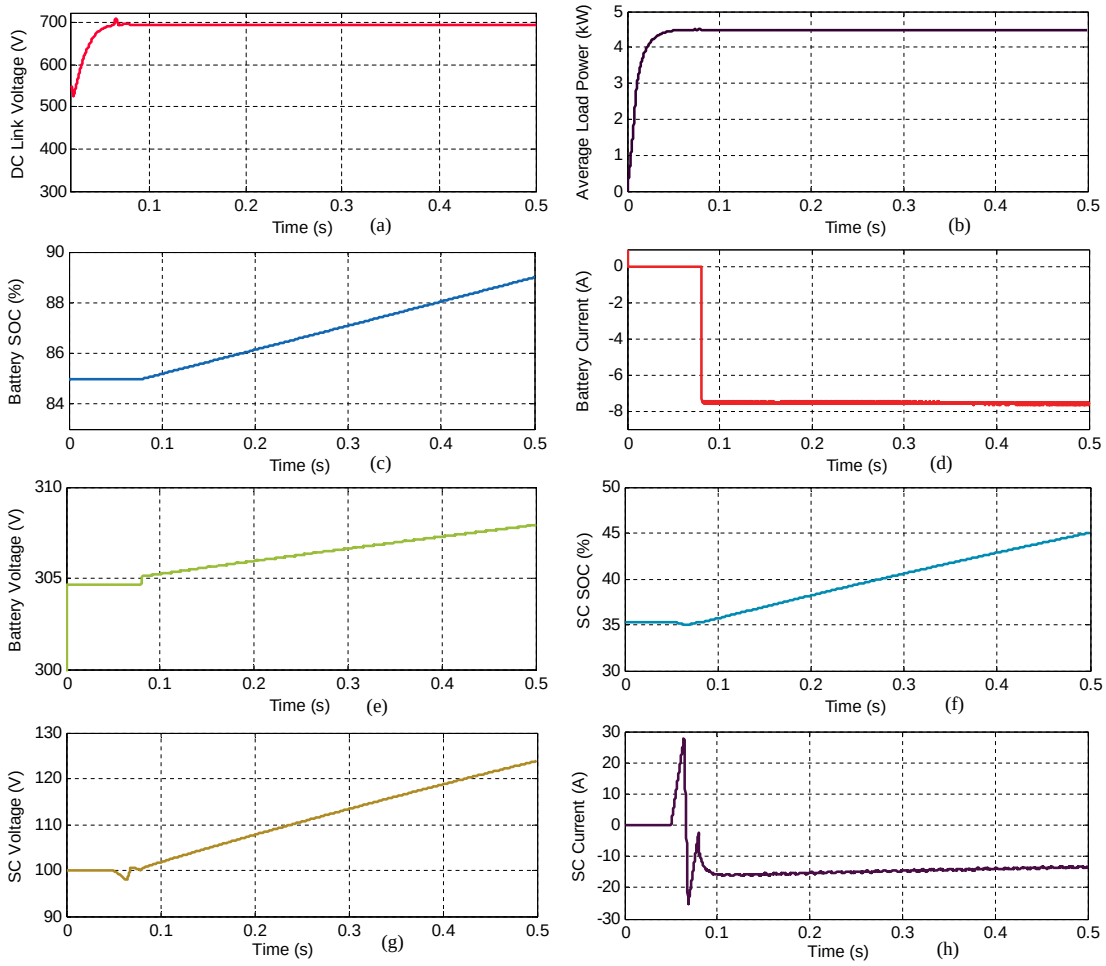

Fig. 6.3 Normal voltage operation: (a) DC link voltage (b) Average load power (c) Battery SOC (d) Battery current (e) Battery terminal voltage(f) Supercapacitor SOC (g) Supercapacitor terminal voltage (h) Supercapacitor discharge current.

some transients, the battery goes to standby mode. During this time ultracapacitor and shunt active power filter tries to maintain the DC link voltage at the rated value.

6.1.2 Operation During Voltage Sag

The simulation was done for a 50% voltage sag. The change in source phase rms voltage (pu) is shown in Fig. 6.6(b). Voltage sag occur at 0.14 s and the duration of sag is 7 cycles. During voltage sag series inverter injects voltages into the line to maintain load voltage undisturbed. The voltage injected by series APF is shown in Fig. 6.4(b). Fig 6.4(c) shows that the series inverter maintain load voltage during voltage sag. The DC link voltage is mainly maintained by the shunt APF by drawing more current from the grid. Whenever the DC link voltage goes below 99% of rated value, ultracapacitor discharges and maintain the DC link voltage at the rated voltage. Shunt APF injects current

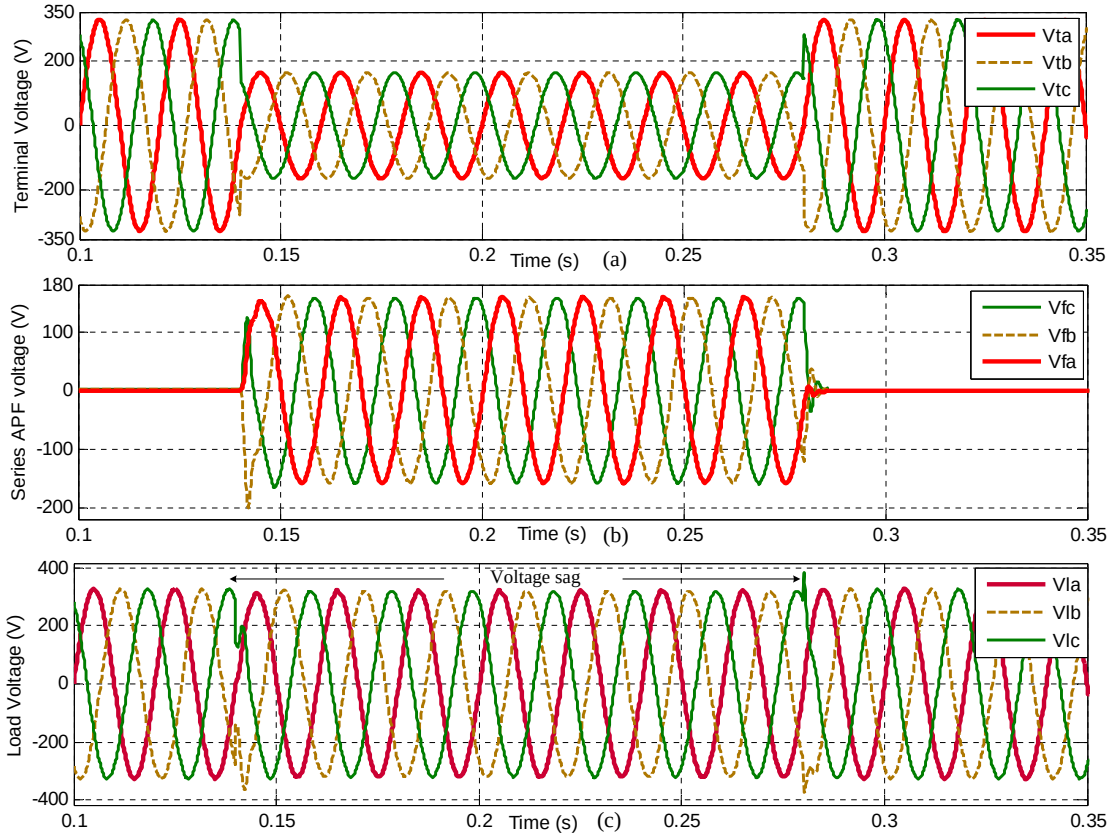

Fig. 6.4 Voltages during sag: (a) Source terminal voltage (b) Series inverter injected voltage (c) Load voltage.

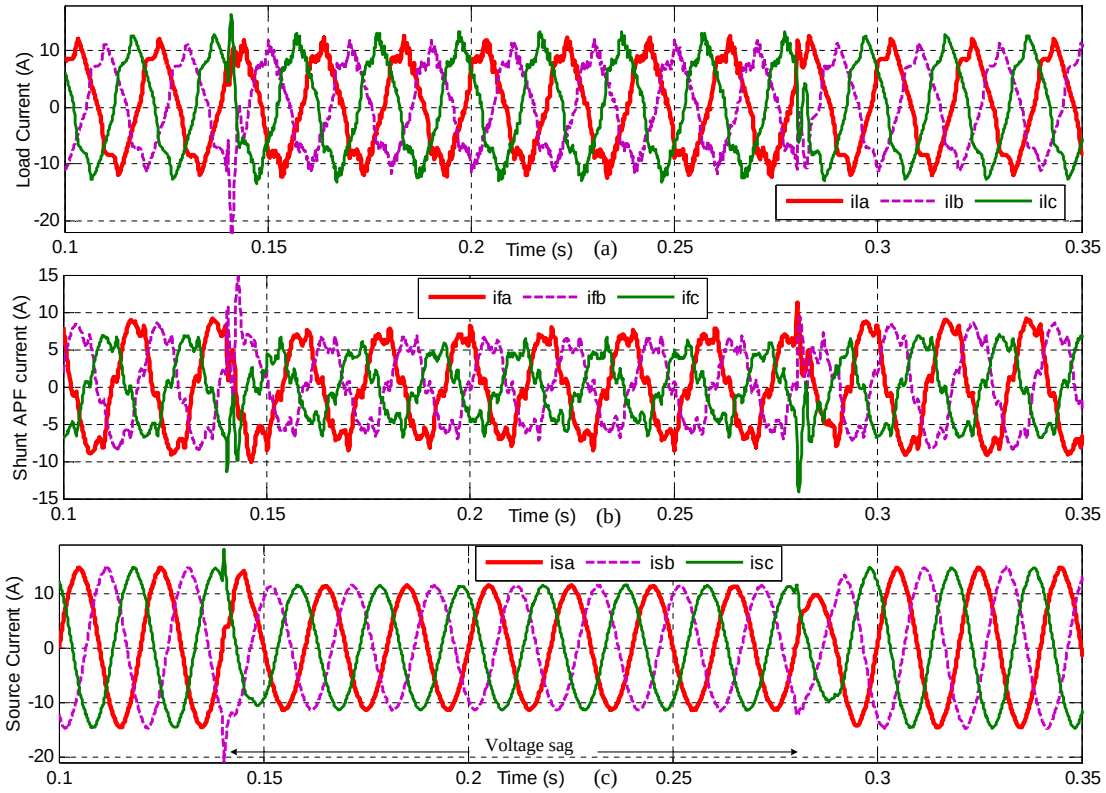

Fig. 6.5 Currents during sag: (a) Load current (b) Shunt inverter current (c) Source current.

into the PCC as shown in the Fig. 6.5(b). This current compensate for load harmonics, unbalance and reactive power. Unbalanced and non linear load current is shown in Fig. 6.5(a). The sinusoidal, balanced and upf source current is shown in Fig. 6.5(c). The DC link voltage is shown in Fig. 6.6(a) which is maintained at the reference voltage. The battery charges in normal voltage condition and it stops charging when voltage sag occur as shown in Fig. 6.6(c). Supercapacitor discharges whenever a sudden DC link voltage fluctuation occur. Fig. 6.6(h) shows the supercapacitor discharge current. Supercapacitor, battery terminal voltage and SOC variation during sag condition is shown in Fig. 6.6. From this figure it is evident that supercapacitor discharges suddenly at the sag occurrence point. This happened because when sag occur series inverter injects voltage and the DC link voltage reduces. The PI controller takes time to maintain the DC link voltage. The shunt APF alone cannot maintain the DC link voltage at 50% sag, that is why the supercapacitor discharges continuously during sag condition.

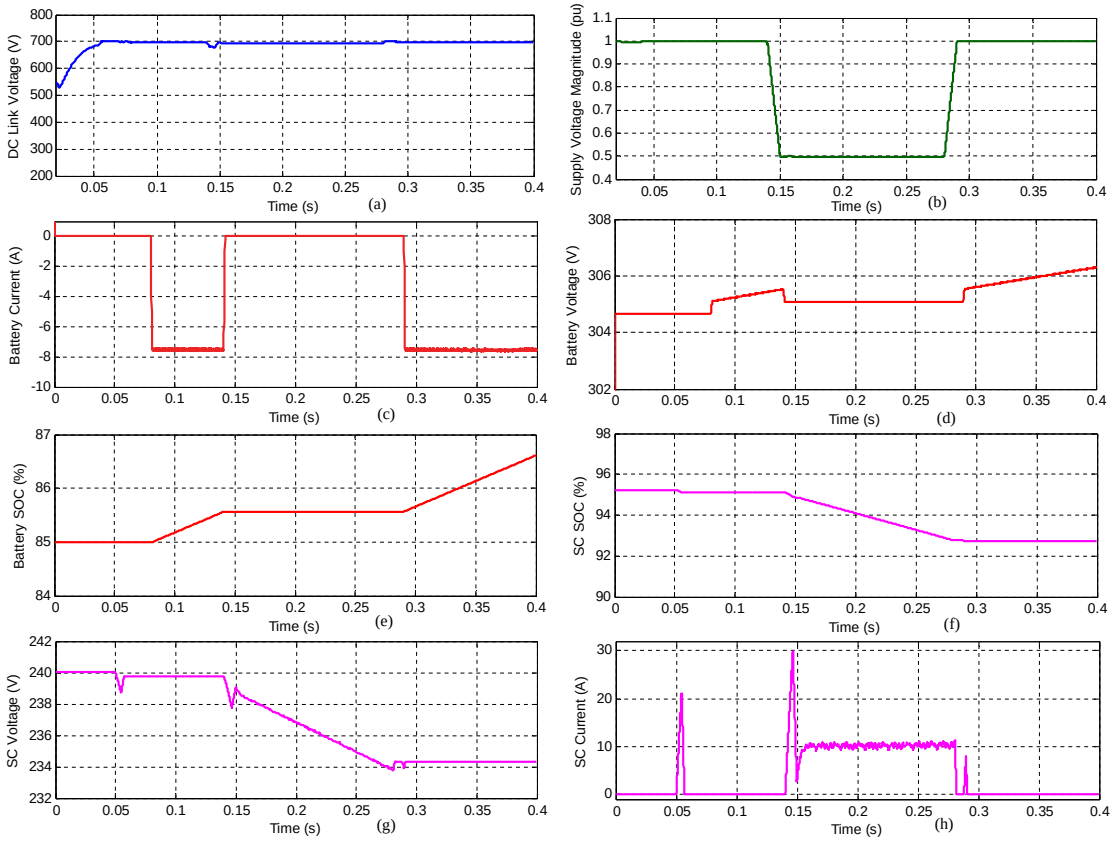

Fig. 6.6 Operation during sag : (a) DC link voltage (b) Source voltage magnitude variation (c) Battery current (d) Battery terminal voltage (e) Battery SOC (f) Supercapacitor SOC (g) Supercapacitor terminal voltage (h) Supercapacitor discharge current.

6.1.3 Operation During Voltage Swell

The proposed system was simulated for a 45% voltage swell and the results are explained in this section. The source voltage rms variation is shown in Fig. 6.9(b). Source terminal voltages, series inverter voltages and load voltages are shown in Fig. 6.7. The

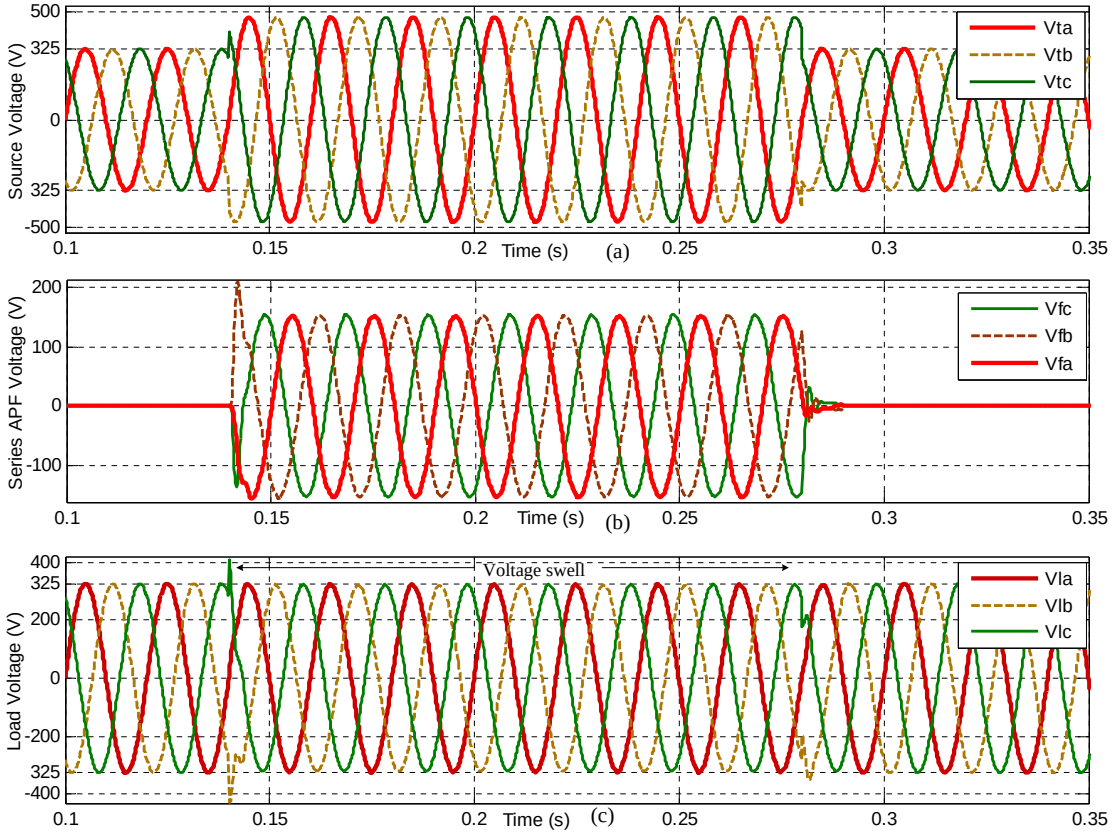

Fig. 6.7 Voltages during swell: (a) Source terminal voltage (b) Series inverter injected voltage (c) Load voltage.

series inverter maintains load voltage undisturbed by compensating the source voltage swell. Shunt inverter helps in maintaining DC link voltage, also it mitigates the load current power quality problems. Load current, shunt inverter current and source current are shown in Fig. 6.8. During voltage swell the DC link voltage increases above reference value. Battery can continue its charging in the voltage swell operation. Battery SOC, terminal voltage and discharge current variations in voltage swell condition are shown in Fig. 6.9. DC link voltage suddenly goes below 693 V when the source voltage restores normal voltage at 0.28 s. At this time interval battery goes to standby mode which is shown in Fig. 6.9(d). The supercapacitor DC/DC converter is switched ON at 0.05 s and it discharged at that instant to increase the DC link voltage. The supercapacitor SOC is greater than 90% and hence it stays in standby mode during normal

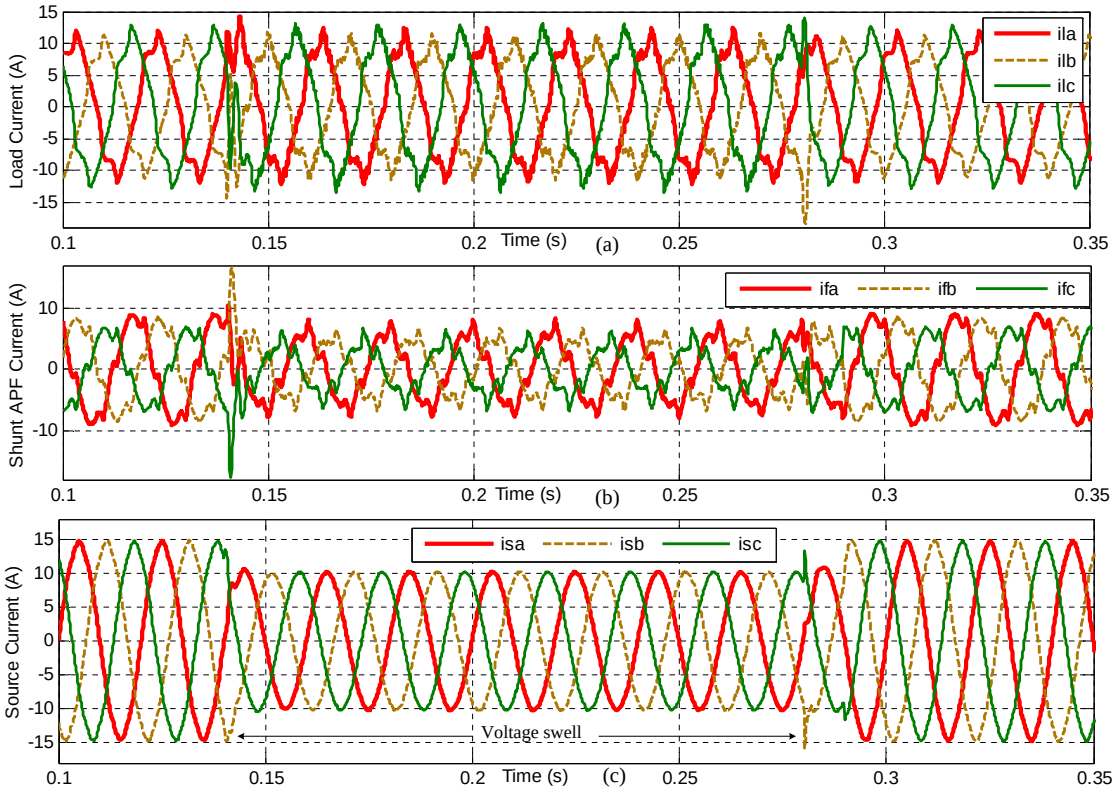

Fig. 6.8 Currents during swell: (a) Load current (b) Shunt inverter current (c) Source current.

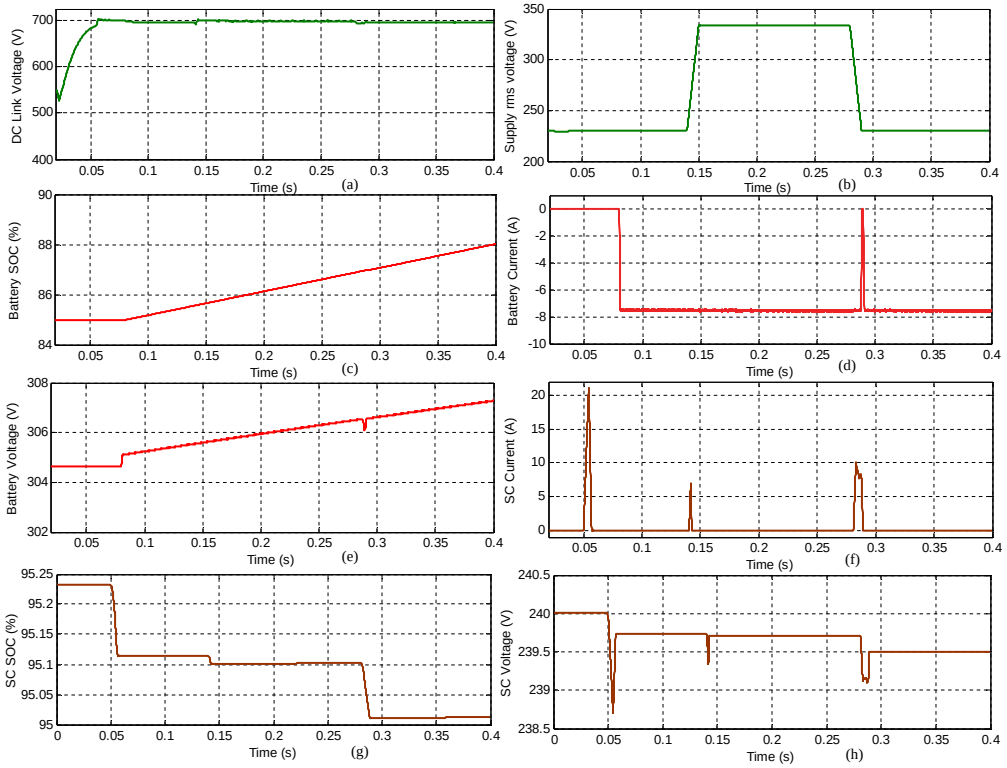

Fig. 6.9 Operation during swell : (a) DC link voltage (b) Source phase voltage variation (c) Battery SOC (d) Battery current (e) Battery terminal voltage (f) Supercapacitor discharge current (g) Supercapacitor SOC (h) Supercapacitor terminal voltage.

voltage. At 0.14 s (swell occur) and 0.28 s (source voltage restore) the DC link voltage dropped below 693 V and because of that supercapacitor discharged at those points. This is shown in Fig. 6.9(f). Supercapacitor SOC and voltage variations in voltage swell condition are shown in Fig. 6.9(g) and 6.9(h) respectively.

6.2 UPQC and Battery-Ultracapacitor Operation in Voltage Interruption

Whenever the grid fundamental positive sequence rms voltage goes below 0.5 pu or above 1.5 pu, the system is said to be in voltage interruption condition. In this mode of operation, the series inverter is isolated from the system, shunt inverter operates in voltage control mode, sensitive loads are switched OFF (in simulation non linear load was switched OFF), battery supply the average load power and supercapacitor supply the sudden load fluctuations. Simulation was done for both sudden increase in load and constant load. Table 6.2 gives the K_p, K_i values for DC/DC converter controller. Other parameters for simulation study are given in Table 6.1.

Table 6.2 K_p and K_i values for simulation study

K_p, K_i values for DC link voltage PI controller	1, 0.5
K_p, K_i values for battery PI controller	5, 2
K_p, K_i values for supercapacitor PI controller	7, 2

6.2.1 Simulation with Constant Load

The average load power variation is shown in Fig. 6.12(a) which has a constant power during voltage interruption. Fig. 6.10(b) shows that the load voltage is maintained at the required value during voltage interruption by shunt APF. The source voltage variation is shown in Fig. 6.10(a). Load voltage transient at the voltage interruption instant can be reduced by choosing appropriate value of resistance (R_f), but higher value of resistance increases the voltage drop across it and thus reduces the load voltage. The source current variation is shown in Fig. 6.11(a). The sensitive non linear load is switched OFF at voltage interruption. The load current variation is shown in Fig. 6.11(b). When voltage interruption occur the DC link voltage has high fluctuations. This fluctuations are

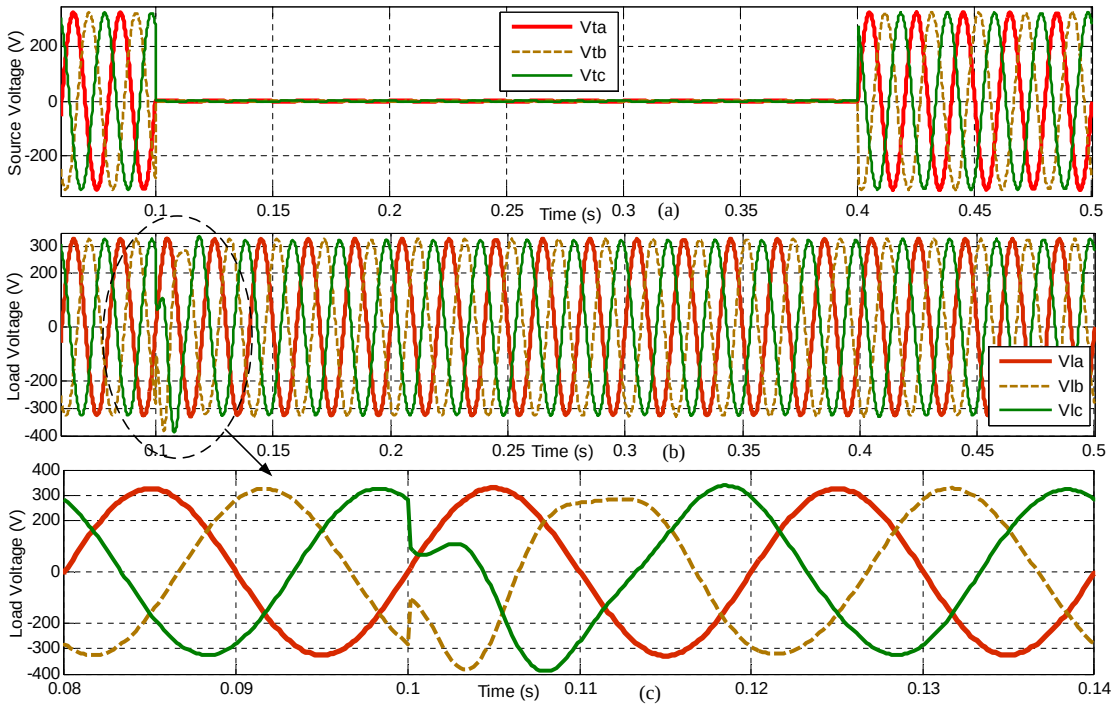

Fig. 6.10 Voltages during supply interruption: (a) Source terminal voltage (b) Load voltage (c) Load voltage variation from 0.08 s to 0.14 s.

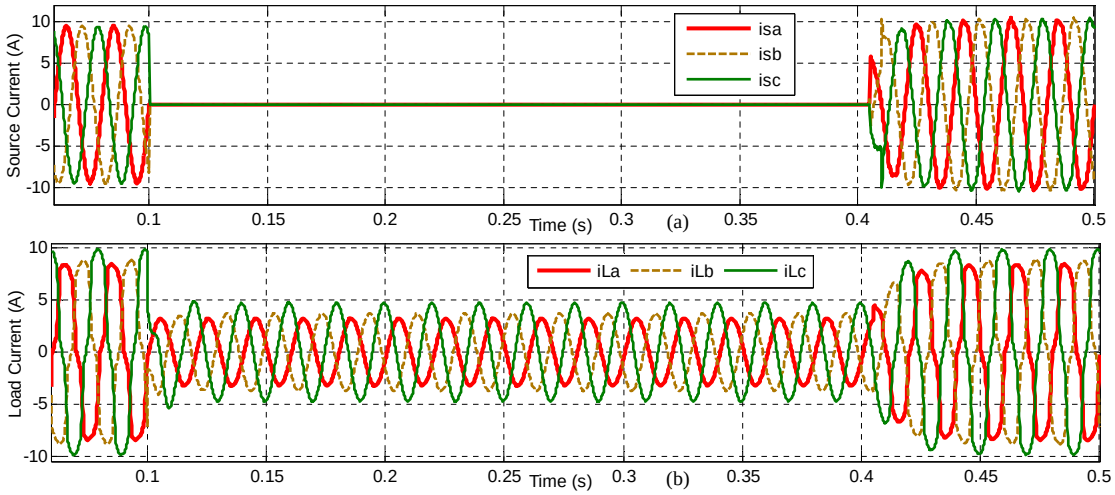

Fig. 6.11 Currents during supply interruption: (a) Source current (b) Load current.

reduced by discharging ultracapacitor. The ultracapacitor discharge current is shown in Fig. 6.12(e). Voltage interruption occur at 0.1 s, at that instant supercapacitor discharge more to reduce the DC link fluctuations. As the DC link fluctuation decreases, the supercapacitor discharge current reduces and finally supercapacitor goes to standby mode. Battery deliver the average load power. From Fig. 6.12(g), it is evident that the battery discharges with a constant current. The battery current fluctuations are reduced by supercapacitor because it takes all the DC link fluctuations. SOC and voltage variations of ultracapacitor and battery are shown in Fig. 6.12. At 0.4 s the source voltage

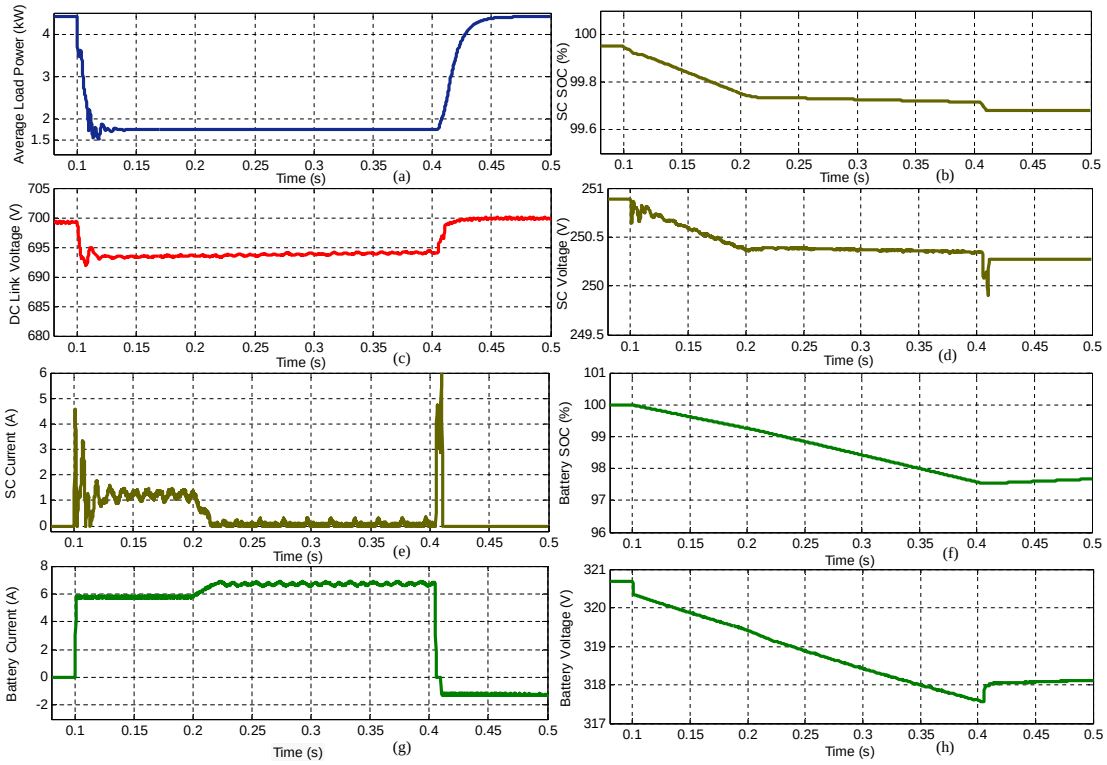

Fig. 6.12 Operation during voltage interruption : (a) Average load power variation (b) Supercapacitor SOC (c) DC link voltage (d) Supercapacitor terminal voltage (e) Supercapacitor discharge current (f) Battery SOC (g) Battery discharge current (h) Battery terminal voltage.

restores its rated voltage and the UPQC goes to grid connected mode operation. Fig. 6.12(e) shows that for maintaining DC link voltage ultracapacitor discharges at 0.4 s.

6.2.2 Simulation with Load Change

The loads used for simulation study is given in Table 6.3. The voltage interruption occur from 0.1 s to 0.9 s. The sensitive nonlinear load is disconnected from the system during this interval. At 0.5 s a balanced linear load is switched ON. The load average power variation is shown in Fig. 6.16(a). The load voltage variation during source voltage

Table 6.3 Loads for simulation study

Linear unbalanced load	Z_a= 100+j 20 Ω Z_b= 75+j 47 Ω Z_c= 55+j 24 Ω (connected all the time)
Nonlinear load	3-ϕ full bridge diode rectifier supplying an R-L (100 Ω - 1 H) load (disconnected during voltage interruption)
Linear balanced load	Z= 150+j 30 Ω (connected from 0.5 s to 0.9 s)

interruption is shown in Fig. 6.13. The load current variation is shown in Fig. 6.14. The load current increases at 0.5 s which causes more voltage drop across the filter

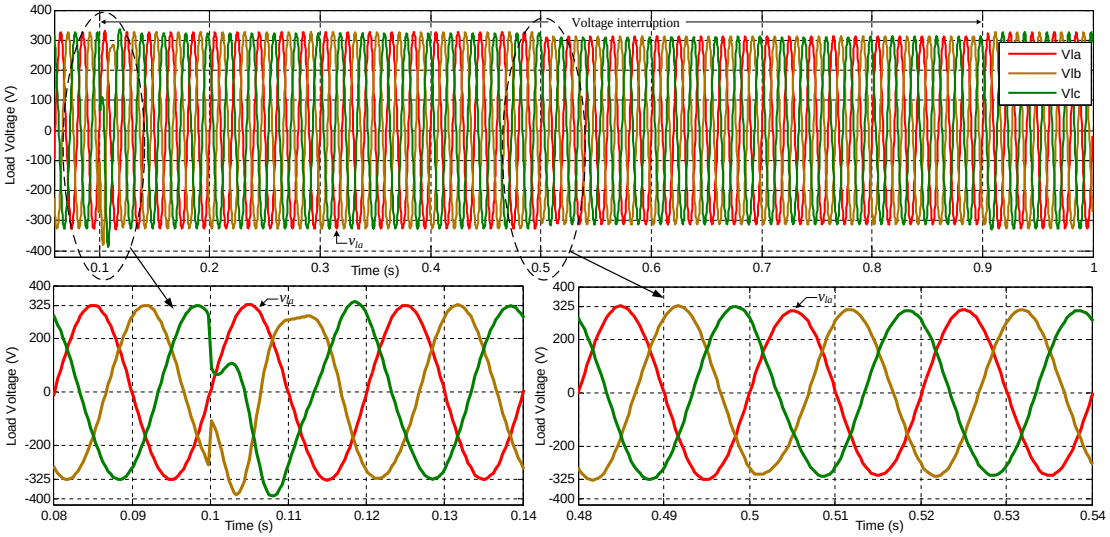

Fig. 6.13 Load voltage variation during source voltage interruption.

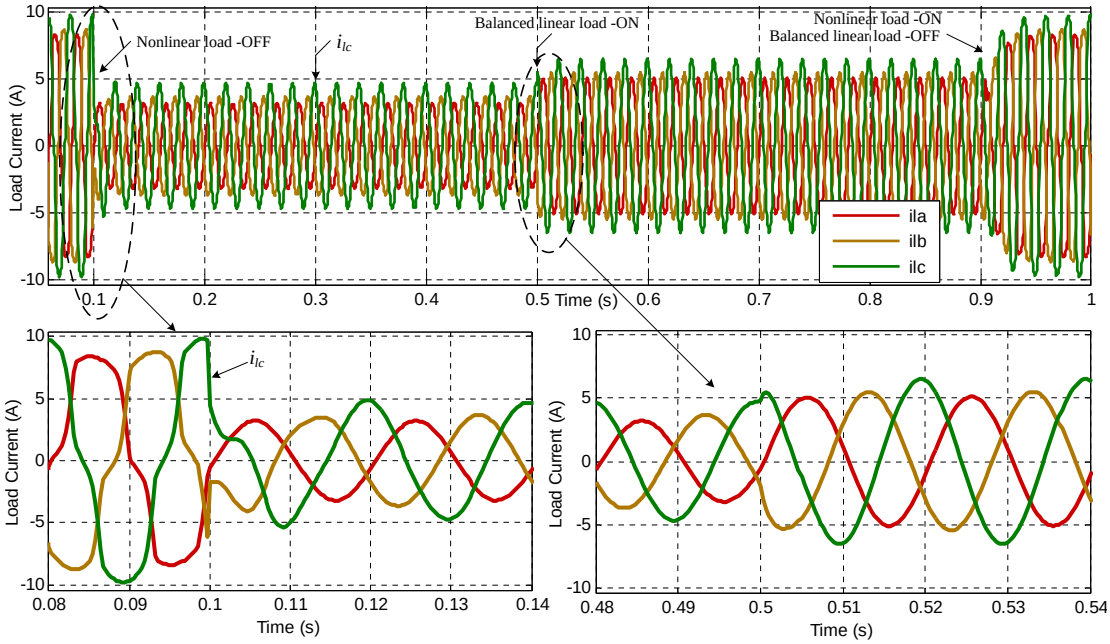

Fig. 6.14 Load current variation during source voltage interruption.

resistance (R_f). Because of this the load voltage slightly decreases as shown in Fig. 6.13. The DC link voltage variation is shown in Fig. 6.16(e). Fig. 6.16(d) shows the variation of source terminal rms voltage. The SOC and voltage variation of battery and ultracapacitor is shown in Fig. 6.15. When the load increases at 0.5 s, battery discharge current slowly increases until it reaches a new steady state value which is shown in Fig. 6.16(b). During this interval supercapacitor current increases sharply which is shown in Fig. 6.16(c). From Fig. 6.16(b) and Fig. 6.16(c), it is evident that battery supply DC

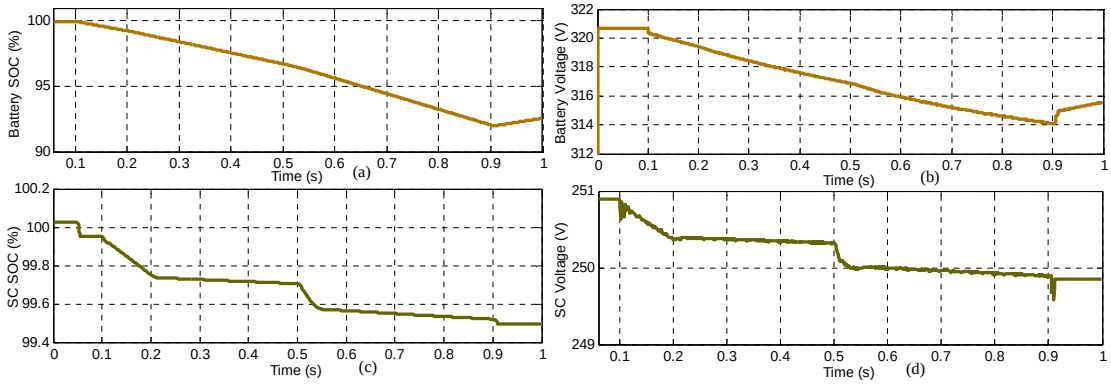

Fig. 6.15 (a) Battery SOC variation (b) Battery terminal voltage (c) Supercapacitor SOC variation (d) Supercapacitor voltage.

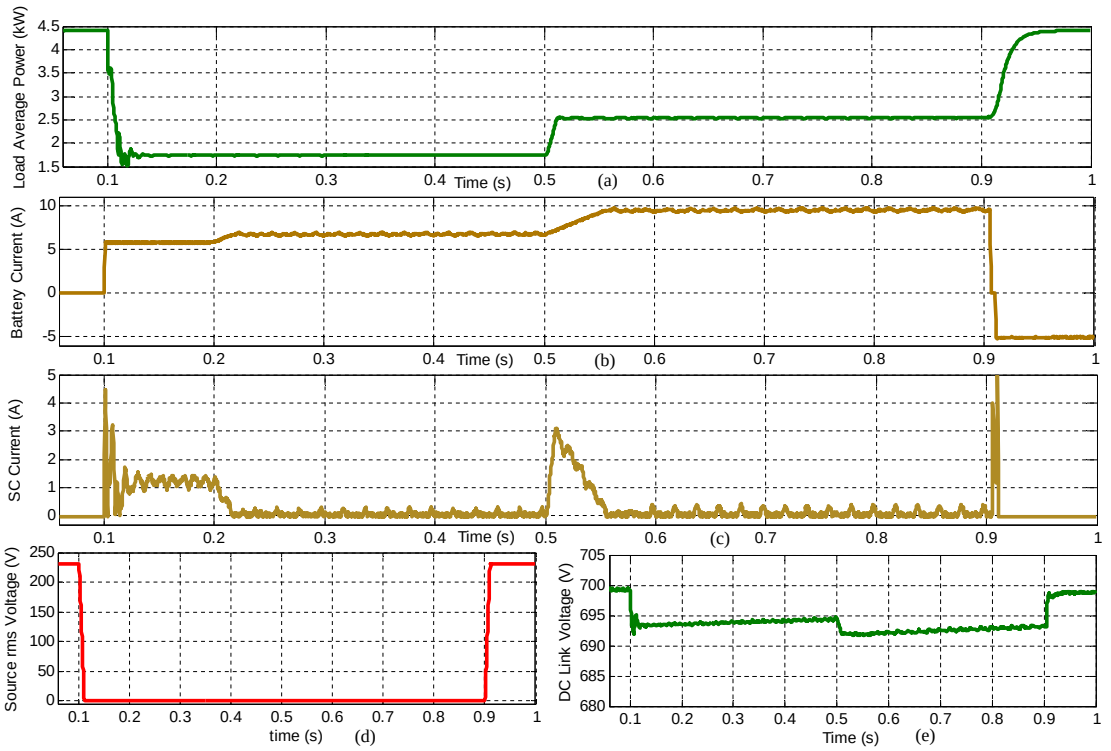

Fig. 6.16 (a) Average load power variation (b) Battery discharge current (c) Supercapacitor discharge current (d) Source rms voltage variation (e) DC link voltage.

link average variation while supercapacitor supply DC link high frequency fluctuations. Thus the stress on the battery is reduced by supercapacitor. This may increase the battery life time. When battery battery discharge rate is high, the chemical reaction rate becomes slower than current discharge rate. This causes unwanted chemical reactions and higher depth of discharge. Higher DOD reduces battery life. By reducing the battery stress and DOD, ultracapacitor increases the cycle life of battery.

CHAPTER 7

CONCLUSION AND FUTURE SCOPE

7.1 Conclusion

Conventional UPQC cannot compensate voltage interruptions. Battery and ultracapacitor are suitable energy storage devices in UPQC applications for compensating voltage interruptions. The combination of two energy storage systems can take advantage of each kind of devices. To effectively work in grid connected and voltage interruption condition, control algorithms for proposed UPQC with battery-ultracapacitor system was developed.

A detailed simulation study was conducted to analyse the combined operation of UPQC and battery-ultracapacitor hybrid in grid connected and voltage interruption condition. From simulations, it was found that the system were giving desired results in all the cases. The performance of UPQC during sag and swell was improved by managing ultracapacitor effectively. The proposed system compensates 50% sag and swell without much disturbances in the DC link voltage.

The Shunt APF was used as inverter for delivering power form energy storage devices during voltage interruptions, thereby avoided the use of extra inverter. During voltage interruption, the battery and ultracapacitor was controlled in such a way that the supercapacitor took all the DC link fluctuations while battery deliver average power. Adding supercapacitor reduced the DOD and stress on the battery. This improves the battery cycle life. The proposed UPQC with battery ultracapacitor hybrid energy storage system has the capability to mitigate source voltage sag, swell, interruption, load current harmonics, load current reactive power and load current unbalance. The UPQC effectively utilized the battery and ultracapacitor energy storage system in all operating conditions. From simulation studies, it is found that the proposed system is suitable for providing backup power to fluctuating loads.

7.2 Future Scope

In this study, the distributed energy sources are not considered. The distributed energy resources (DER) can be connected to the system and battery-ultracapacitor hybrid energy storage system can work to manage power from DER and grid. The controlling and operation of UPQC, DER and battery-ultracapacitor hybrid can be subjected to future studies. Only simulation analysis was done on the proposed system. The validation of the system through hardware is required for practical implementation. Therefore verifying proposed system through hardware is another future prospect. Non isolated DC/DC converters was used in this study. The battery and ultracapacitor voltage level can reduce further by using isolated DC/DC converters. The analysis of UPQC with reduced voltage battery and ultracapacitor by incorporating isolated DC/DC converter can be a future work.

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