SINGLE PHASE POWER FACTOR CORRECTION USING FRONT END CONVERTER

A Project Report

submitted by

T V SAIKUMAR

in partial fulfilment of the requirements

for the award of the degree of

MASTER OF TECHNOLOGY

DEPARTMENT OF ELECTRICAL ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY MADRAS.

MAY 2014

THESIS CERTIFICATE

This is to certify that the thesis titled **SINGLE PHASE POWER FACTOR CORRECTION USING FRONT END CONVERTER**, submitted by **T V SAIKUMAR**, to the Indian Institute of Technology, Madras, for the award of the degree of **Master of Technology**, is a bona fide record of the research work done by him under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

Dr. LAKSHMI NARASAMMA
(Project Guide)
Professor
Dept. of Electrical Engineering
IIT-Madras, 600 036

Place: Chennai

Date: 10th May 2014

ACKNOWLEDGEMENTS

It gives me great pleasure in expressing my sincere and heartfelt gratitude to my project guide Prof. LAKSHMI NARASAMMA for her excellent guidance, motivation and constant support throughout my project . I consider myself extremely fortunate to have had a chance to work under her supervision. In spite of her hectic schedule she was always approachable and took her time off to discuss problems and give her advice and encouragement. It has been a very learning and enjoyable experience to work under her.

I am also grateful for the laboratory facilities provided by her in the Lab, ESB 105, Department of Electrical Engineering, which facilitated my simulation work and to develop hardware setup. I express my gratitude to Dr.Krishna Vasudevan, Dr.Srirama Srinivas, Dr.Kamalesh Hatua and Technical staffs in our department.

My appreciation to my fellow research scholars in the Lab, especially Sandeep for spending his invaluable time with me, in discussing about the project and answering my queries, goes well beyond words. I would also extend my thanks to Dinesh, Krishna Teja, Lokesh for their support during my work.

This work could not have come to this stage without the support and encouragement from my family. My heartfelt thanks to all of them.

ABSTRACT

KEYWORDS: Power Factor Correction(PFC); AC−DC power conversion; Boost converter

In present situation, the increase in the utilization of computers, laptops, uninterruptable power supplies, telecoms and bio-medical equipments has become uncontrollable as its growth is rising exponentially. Whenever switching loads such as DC-DC converter are connected to the rectifier, switching harmonics are injected into the supply current. This makes supply current to be out of phase with supply voltage making supply power factor very poor. As the rectifier other end is connected to grid side, the main grid will get affected with these converters. A front end converter is placed between rectifier and DC-DC converter. This front end converter will make sure that the supply current is sinusoidal and in phase with supply voltage and it also regulates the output voltage. The front end converter can be Boost converter,Fly-back converter,interleaved Boost converter. Here Boost topology is presented as Power Factor Correction(PFC) interface.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

ABBREVIATIONS

PFC	Power Factor Correction
PI	Proportional and Integral
DC	Direct Current
AC	Alternating Current
PCC	Point of Common Coupling
PWM	Pulse Width Modulation
THD	Total Harmonic Distortion
PF	Power Factor
RMS	Root Mean Square

NOTATION

V_g	Rectified Voltage, V
V_{ref}	Reference Voltage, V
V_{fb}	Feedback Voltage, V
I_{ref}	Reference Current, A
I_g	Rectified Current, A
I_Q	Switch Current, A
i_{sense}	Sense current A
R_e	Emulated resistance Ω
$d(t)$	Duty cycle
L	Inductance , mH
C	Filter Output Capacitance,
V_o	DC bus voltage, V
P	Load Active Power, W
ω	Frequency, rad/s

CHAPTER 1

INTRODUCTION

Power electronics is a field in electrical engineering that deals with converting an available form of energy from a power source to the form required by a load. A power converter uses semiconductor devices such as diodes, MOSFETs and IGBTs to achieve this power conversion. Diodes are uncontrolled switches that turn on and conduct current when they are forward-biased and turn off when they are reverse-biased; MOSFETs and IGBTs are controlled switches that can be turned on or off by a switching signal at their gate (i.e. a high gating pulse is the turn-on command and a low or zero gating pulse is the turn-off command). A power converter can be an AC/DC converter, DC/DC converter, DC/AC inverter or AC/AC converter depending on the application. Many types of power sources can be used for these converters, such as AC single phase, AC three-phase, DC source, battery, solar panel, or an electric generator. This thesis will focus on low power (< 100 W) single-phase, AC/DC converters.

Some sort of control method is needed to ensure that the output voltage of an AC/DC converter is regulated to the desired DC voltage. In a closed-loop power converter, a sensing circuit is responsible to send output voltage values (samples) to a controller circuit so that adjustments can be made to the power converter, typically this means changing the converter duty-cycle. The term duty-cycle (D) refers to the proportion of on-time to the period T of the switch and is expressed in percent, with 100% as being fully on. It is by controlling the width of the on-time gating pulse relative to the switching cycle that allows the output voltage to be regulated. Such a control method is generally referred to as Pulse-Width Modulation (PWM) in the power electronics literature.

1.1 Power Factor and Harmonic Distortion

The input power factor of an AC/DC power converter is an important consideration as it is a measure of how effectively the converter utilizes AC input power. Power factor is

defined as the ratio of the real power flowing to the load to the apparent power can be expressed as.

$$P.F = \frac{realpower}{apparentpower}. \tag{1.1}$$

$$= \frac{\sum I_{snrms} V_{snrms} \cos\theta_n}{I_{srms} V_{srms}} \tag{1.2}$$

where I_{snrms} and V_{snrms} are rms values of the nth harmonic of input current and input voltage, respectively and θ_n is the phase shift between them. Since the input AC voltage can be assumed to be a pure sinusoid, the product of voltage harmonic terms and current harmonic terms are zero with the exception of the product of fundamental voltage and current harmonics so that eq. (1.2) can be simplified to be.

$$P.F = \frac{I_{s1rms}}{I_{srms}} \cos\theta. \tag{1.3}$$

where I_{snrms} is the rms value of primary component of the input current. As can be seen from eq. (1.3), if the input current is a pure sine wave, then power factor can be defined as cosine of the phase angle between input voltage and current waveforms. Power factor can range from zero to one, with a power factor of one indicating that the input current is a purely sinusoidal waveform that is in phase with the input AC voltage. Another term that is used for measuring the power quality of electrical power systems is Total Harmonic Distortion (THD). THD is defined as the ratio of the square root of the summation of the square of all non-fundamental harmonics of a waveform to fundamental component of the same waveform. For a current waveform, particularly the input current of a power electronic converter, it can be expressed as

$$THD_i = \frac{\sqrt{I_{2rms}^2 + I_{3rms}^2 \cdots}}{I_{1rms}} \tag{1.4}$$

where I_{nrms} is the rms value of the nth harmonic of the input current.

1.2 Power Factor Correction

With the exception of low power converters (< 75 W), most AC/DC converters in commercial products that are powered by the AC utility grid now have some sort of input Power Factor Correction (PFC). Input PFC techniques are needed to shape the input currents of AC/DC converters so that they have acceptable harmonic contents with their fundamental harmonic component in phase with the input AC voltage.

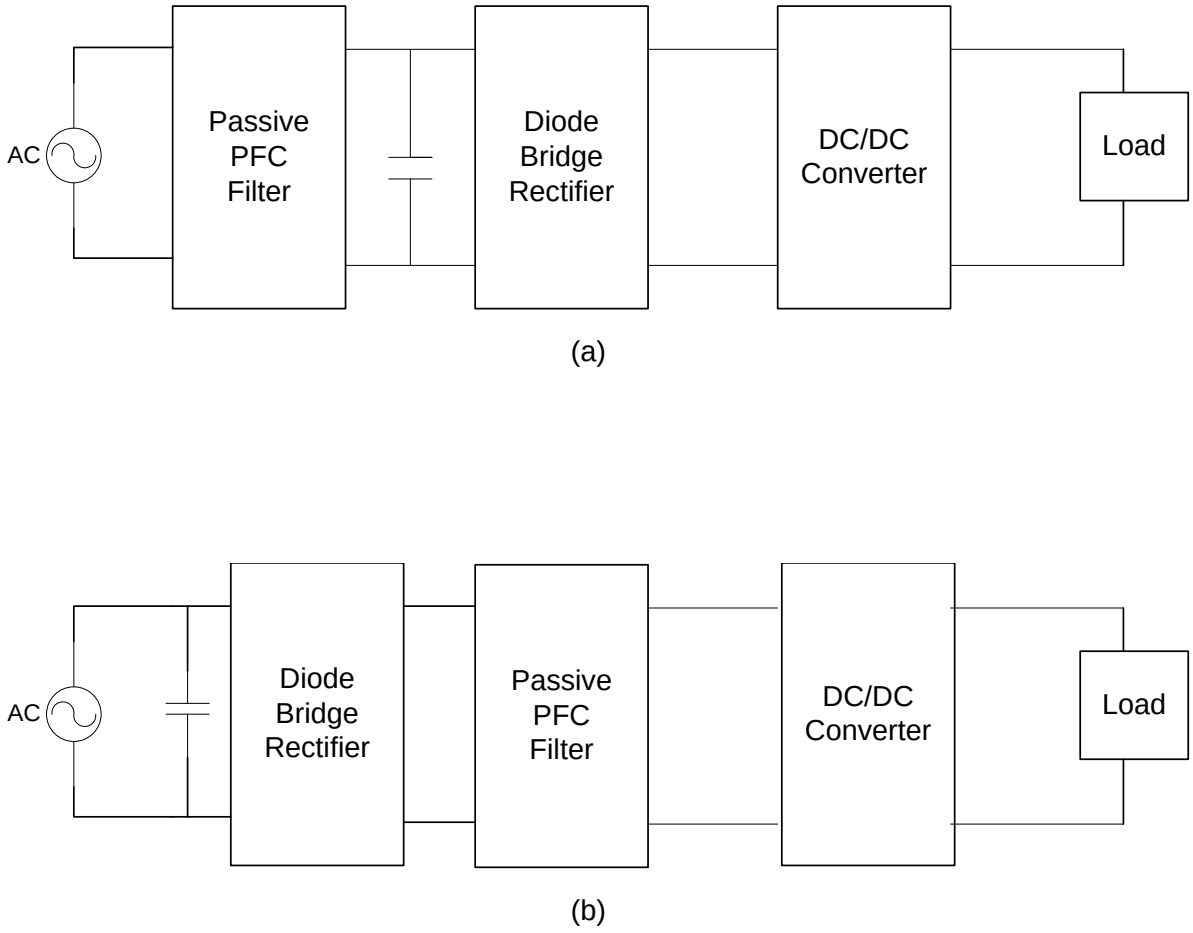

Fig. 1.1 Passive PFC with the filter on (a) the AC side, (b) the DC side of the diode bridge.

PFC techniques can either be passive or active. Passive techniques use passive elements such as inductors and capacitors in a low-pass or band-pass filter structure to filter low frequency harmonics. These passive filters can either be placed at the converterŠs input AC side, as shown in Fig. 1.1(a) or in the intermediate DC link, as shown in Fig.

1.1(b). Although passive PFC techniques are simple and inexpensive, they have one significant disadvantage, which is their need for bulky capacitors and inductors. The size of these elements makes passive PFC techniques unsuitable for most applications except for low-power applications with narrow line voltage range.

1.3 Active Approaches for Power Factor Correction

Active PFC techniques are much more popular than passive PFC techniques. It is a generally accepted standard practice to implement a second active converter at the front-end of an AC/DC converter to perform input power factor correction as shown in Fig. 1.2. In other words, most AC/DC converters are two-stage converters than consist of an AC/DC front-end converter that performs PFC followed by a DC/DC converter that converts the output of the front-end converter into the desired output DC voltage.

The front-end AC/DC converter has a filter capacitor Cstorage to smooth its output

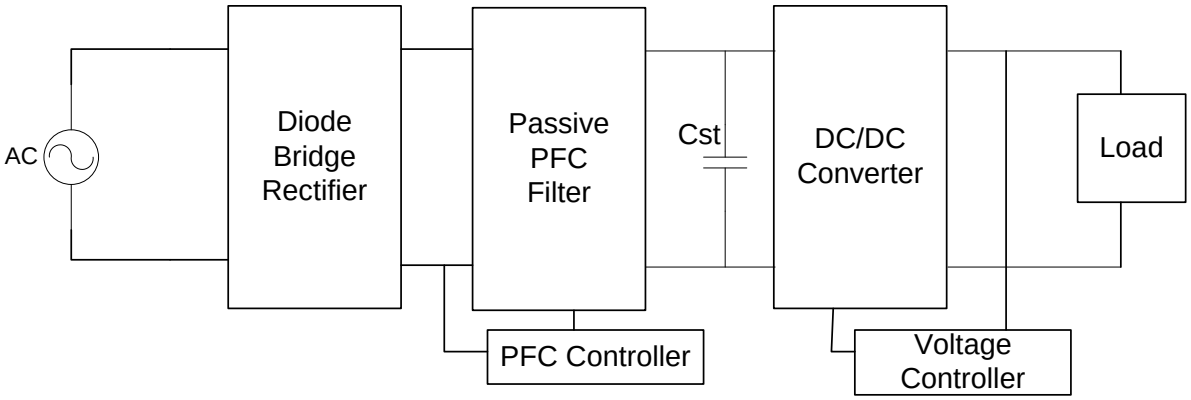

Fig. 1.2 Two-stage AC/DC PFC converter.

voltage and make it DC so that it can be fed to the input of the DC/DC converter. AC/DC boost (step-up) converters are typically used as front-end converters because of their relative simplicity and their effectiveness in shaping input currents. Flyback and forward converter topologies are typically used as DC/DC converter in applications that are < 200 W, which is the focus of this thesis. The main drawback of two-stage converters is the cost and complexity that is associated with operating two separate and independent switch-mode power converters. As a result, power electronic researchers have been motivated to find alternative approaches to conventional twostage AC/DC

converters.

1.4 Organisation of thesis

- **Chapter2** : Modeling and Analysis of PFC Converter which deals with the modeling of the PFC boost circuit and with that calculating the controller design parameters.A control strategy for the PFC converter is proposed in this chapter.In this chapter, the conventional average current mode control approach that is generally used for single-stage PFC converters is discussed and its drawbacks are reviewed.It also presents the losses evaluation in the PFC circuit.

- **Chapter3** : In this chapter, experimental results obtained from a prototype of the PFC Boost converter, implemented with the proposed control scheme described in Chapter 2 are presented. The simulation and hardware setup results are presented.

- **Chapter4** : In this chapter, the contents and results of the thesis work are summarized, the conclusions that have been reached as a result of this research work are presented. are stated.

CHAPTER 2

MODELING AND ANALYSIS OF PFC BOOST CONVERTER

2.1 Introduction

Most of the power conversion applications consists of AC-DC conversion stage immediately following the AC source. The DC output obtained after the rectification is subsequently used for the further stages.Current pulses with high peak amplitude are drawn from the a rectified voltage source with sine wave input and capacitive filtering. The current drawn is discontinuous and of short duration irrespective of the load connected to the system.Since many applications demands DC voltage source,a rectifier with a capacitive filtering is necessary. However this results in discontinuous and short duration current spikes.When this type of current is drawn from the mains supply, the resulting network losses,the total harmonic content, and the radiated emissions become significantly higher.At power levels of more than 500 watts these problems become more pronounced.

Power factor is a parameter that gives the amount of working power used by any system in terms of the total apparent power.Power factor becomes an important measurable quantity because it often results in significant economic savings.Typical waveforms of current with and without power factor is shown in Fig.2.1. These waveforms illustrate that PFC can improve the input current drawn from the mains supply and reduce the DC bus voltage ripple.

This chapter deals with dynamic modeling of PFC boost converter. It also presents the complete analysis of converter and the design parameters to control the duty of the mosfet. The design specification of various components are explained and the losses in the converter is evaluated to calculate the efficiency of the converter.

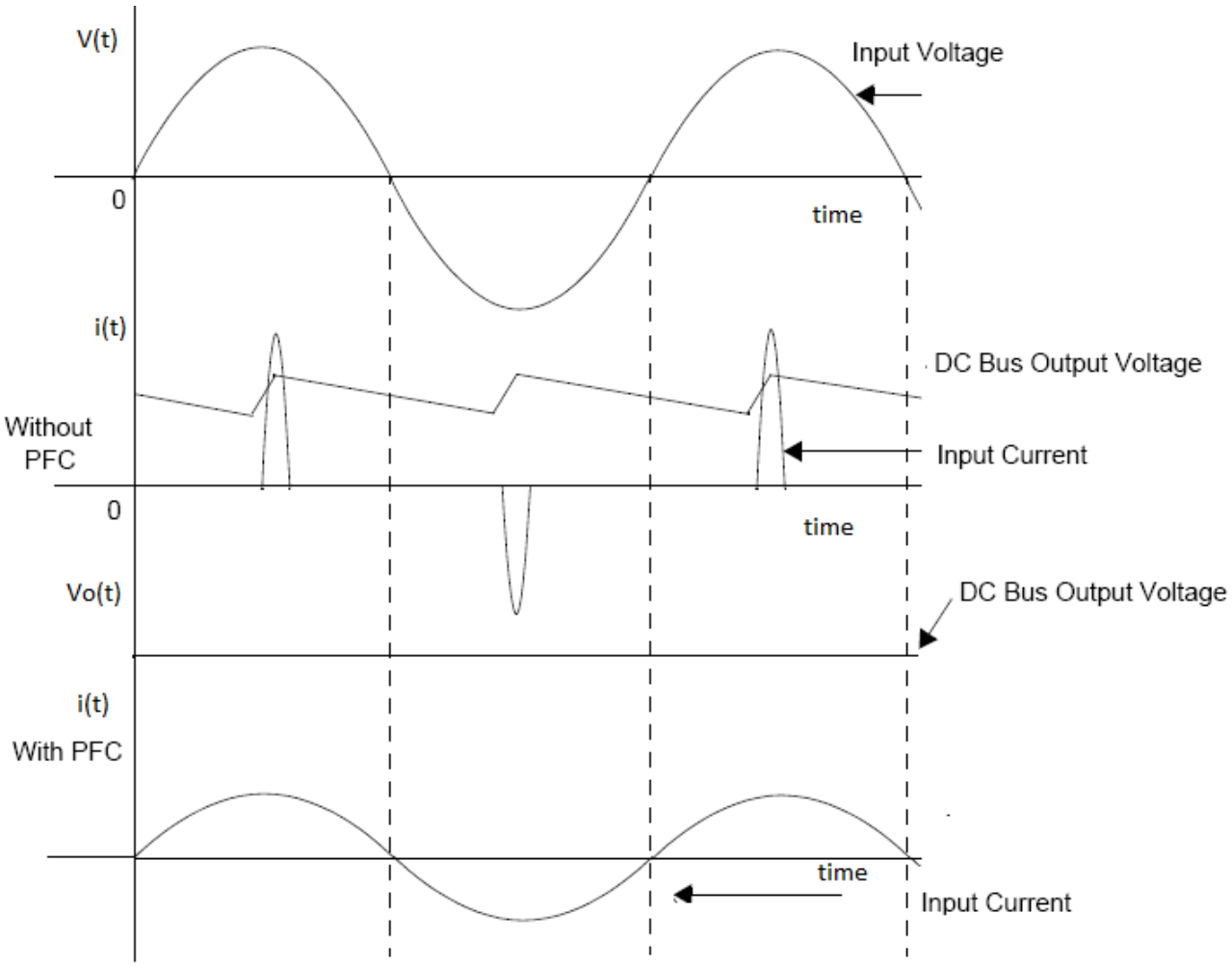

Fig. 2.1 Current waveform with and without PFC circuit

2.2 BOOST CONVERTER

A boost converter is a non-linear load device.Therefore it has a poor power factor due to the nonlinear load.Because of any variations in input impedance as a function of the input voltage will cause distortion of the input current and hence leads to poor power factor.Distortion increases the rms value of current, without giving rise to total power being drawn from supply. Two techniques are used to regulate PF of a boost converter[5].

1. Passive power factor correction.
2. Active power factor correction.

2.2.1 Boost Converter with Active PFC

An active power factor corrector is a power electronics system that controls the amount of power drawn by a load in order to obtain a power factor as close as possible to unity.In most applications, the active PFC controls the input current of the load in such a way that current waveform is proportional to the mains voltage waveform (sine waveform). The aim of active PFC is to make the input to the power supply look like a resistor. It controls all this by programming the input current in response to the input voltage.

Fig.2.2.shows basic control circuit of an power factor corrector. The output of the multiplier is the current programming signal. Multiplier input is from rectified line voltage and the output of voltage error amplifier is divided by the square of the average input voltage before it is multiplied by the rectified input voltage signal. This extra circuitry keeps the gain of the voltage loop constant, without this the gain of voltage loop would change as the square of the input voltage. Feed forward voltage Vff, provides an open loop correction that is fed forward into the voltage loop, where its squared and then divided by output of voltage error amplifier output voltage.

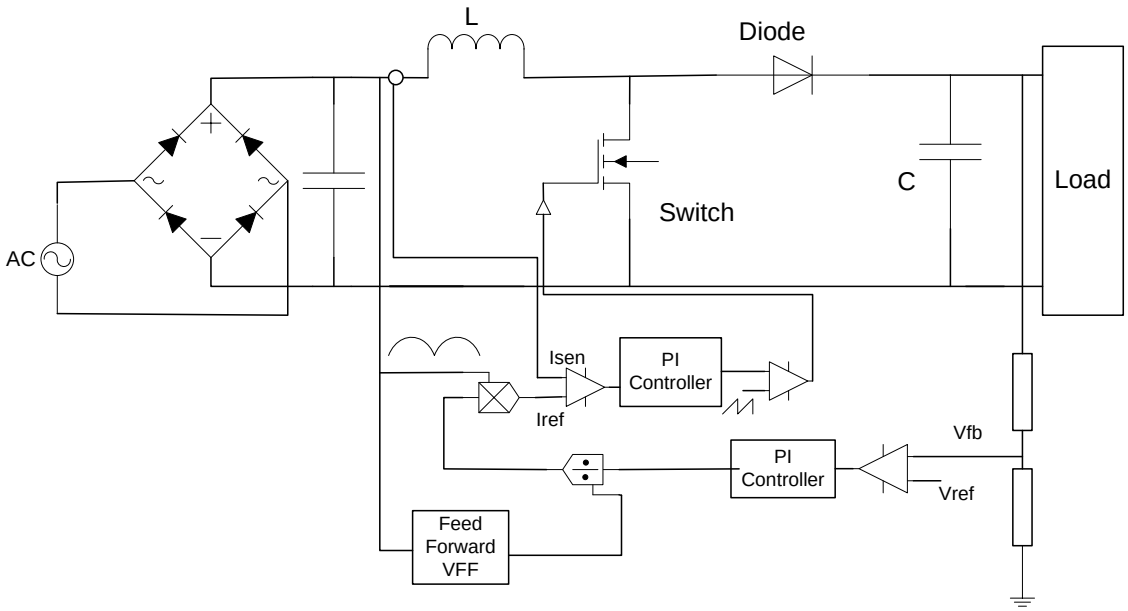

Fig. 2.2 Basic PFC Boost converter

The power circuit of a boost power factor corrector is the same as that of a DC to DC boost converter. There is a diode bridge ahead of the inductor to rectify the AC input voltage but the large input capacitor which would normally be associated with the

AC to DC conversion function has been moved to the output of the boost converter. If a capacitor follows the input diode bridge it is a small one used only for noise control.The output of the boost regulator is a constant voltage but the input current is programmed by the input voltage to be a half sine wave. The power flow into the output capacitor is not constant but is a sine wave at twice the line frequency since power is the instantaneous product of voltage an current. The flow of energy into and out of the capacitor results in ripple voltage at the second harmonic.Note that the voltage ripple is displaced by 90 degrees relative to the current since this is reactive energy storage. The output capacitor must be rated to handle the second harmonic ripple current as well as the high frequency ripple current from the boost converter switch which modulates it.

An active power factor corrector must control both the input current and the output voltage. The current loop is programmed by the rectified line voltage so that the input to the converter will appear to be resistive. The output voltage is controlled by changing the average amplitude of the current programming signal. An analog multiplier creates the current programming signal by multiplying the rectified line voltage with the output of the voltage error so that the current programming signal has the shape of the input voltage and an average amplitude which controls the output voltage. Fig.2.3. is a block diagram which shows the control circuit arrangement necessary for an active power factor corrector. The output of the multiplier is the current programming signal and is called I_{ref} for multiplier output current.

Fig.2.3. shows a squarer and a divider as well as a multiplier in the voltage loop. The output of the voltage error amplifier is divided by the square of the average input voltage before it is multiplied by the rectified input voltage signal. This extra circuitry keeps the gain of the voltage loop constant, without it the gain of the voltage loop would change as the square of the average input voltage. The average value of the input voltage is called the feed forward voltage or Vff since it provides an open loop correction which is fed forward into the voltage loop. It is squared and then divided into the voltage error amplifier output voltage.

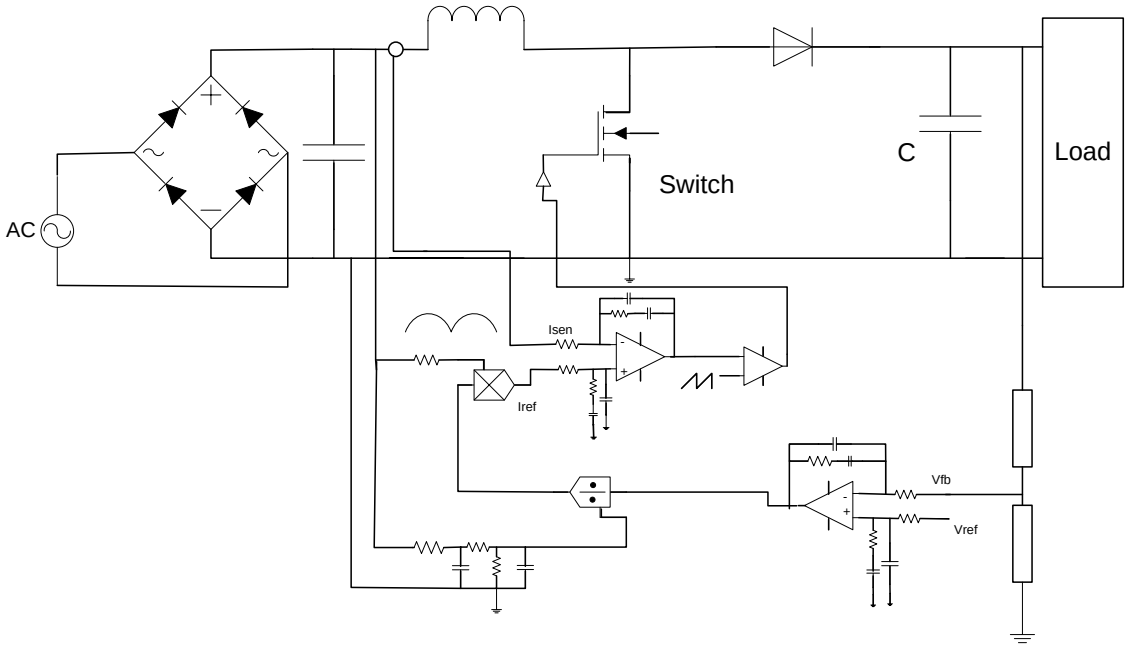

Fig. 2.3 Block diagram for PFC Boost converter

2.3 Expression for Controller Duty Cycle $d(t)$

The controller varies the duty cycle $d(t)$ making current to follow the voltage. By solving the input side loop of Fig.2.4., we obtain

$$i_g(t)d(t)R_{on} = V_g(t) - d'(t)v \tag{2.1}$$

$$\frac{v_g(t)}{R_e}d(t)R_{on} = V_g(t) - d'(t)v \tag{2.2}$$

$$\tag{2.3}$$

where R_e is the an equivalent resistance for the ac port of an ideal rectifier also called as emulated resistance. with $v_g(t) = V_M|sinwt|$ and solving the expression is given by

$$d(t) = \frac{v - v_g(t)}{v - v_g(t)\frac{R_{on}}{R_e}} \tag{2.4}$$

The expression neglects the converter dynamics, an assumption that is justified when these dynamics are sufficiently faster than the ac line voltage variation. The expression also neglects operation in the discontinuous conduction mode near the zero crossing of the ac line voltage waveform[2].

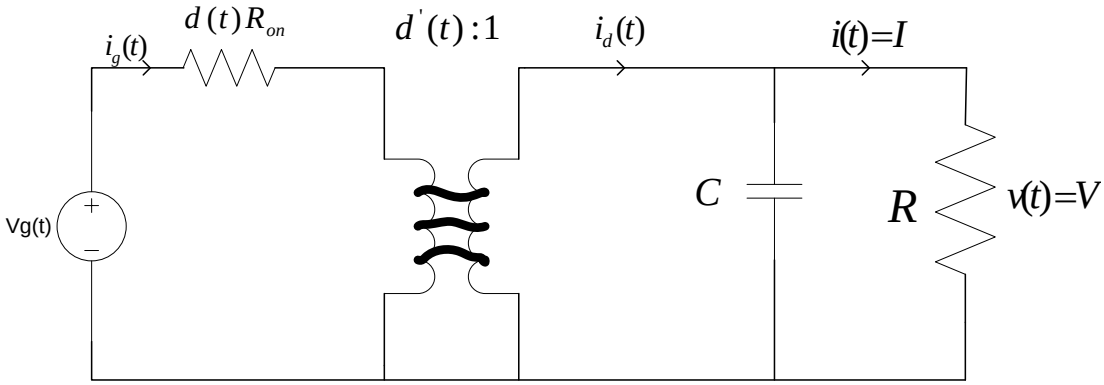

Fig. 2.4 Simplified boost power stage low frequency equivalent circuit on in the discontinuous

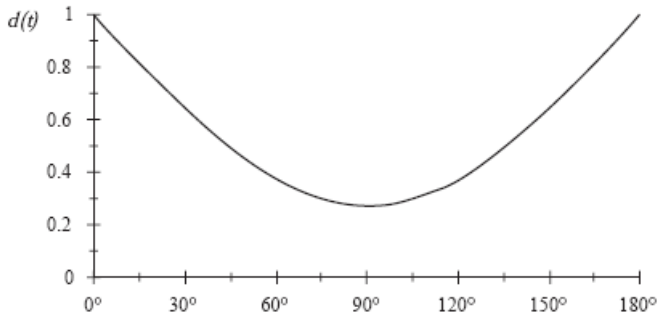

Fig. 2.5 Variation of duty over a period of time

2.4 Dynamic Modeling of front end converter

PFC boost converter consists of inductor as shown in Fig.2.4.and the average current are controlled current loops, whereas load voltage is regulated using outer voltage loop. Current reference to the inner current loops is fed by outer voltage loop. The steps involved in mathematical modeling of average current mode controlled PFC boost converter are explained in this section. State space averaging method is used to obtain small signal model of the converter. The model is derived under the assumption that all the converter elements are ideal[4].

2.4.1 Plant transfer function

By introducing sinusoidal disturbance in duty $\hat{d}$, individual duty to inductor current transfer function is obtained as:

$$G_{id} = \frac{\hat{i}_l}{\hat{d}} = \frac{\frac{\hat{V}_o}{L}(s + \frac{2}{RC})}{s^2 + \frac{s}{RC} + \frac{(1-D)^2}{LC}} \tag{2.5}$$

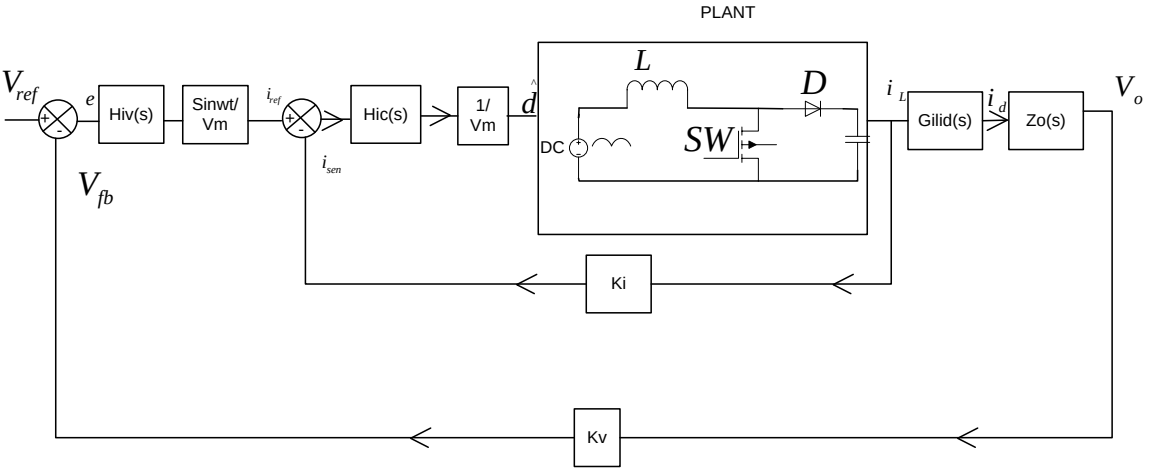

Fig. 2.6 Block diagram representation of PFC Boost converter

The obtained transfer function is similar to duty to inductor current transfer function of conventional boost converter.The derived transfer functions are exploited to design the inner current loop controller. The controller design aspects are explained subsequently.The switching frequency is very high compared to time constant of the inner loop bandwidth.

2.4.2 Current loop transfer functions

The PFC boost converter with closed current loop is modeled as $\hat{i_{ref}}$ to $\hat{i}_l$.

$$\frac{\hat{i}_l}{\hat{i_{ref}}} = \frac{G_{id}(s)H_{ic}(s)\frac{1}{V_m}}{1+G_{id}(s)H_{ic}(s)K_i\frac{1}{V_m}} \tag{2.6}$$

$$G_c = \frac{T_{iL}(s)}{1+T_{iL}(s)}. \tag{2.7}$$

where,

$T_{iL}(s) = G_{id}(s)H_{ic}(s)\frac{1}{V_m}$ for $K_{il} = unity$ is individual current loop gain.At low frequencies the controller is designed such that the individual loop gain is high $T_{iL}(s) >> 1$.Once the current loop is closed the system transfer function will be $\hat{V_o}/\hat{i_{ref}}$ and this can be derived as:

$$\frac{\hat{V}_o(s)}{\hat{i_{ref}}(s)} = \frac{\hat{V}_o(s)}{\hat{i_d}(s)}\frac{\hat{i_d}(s)}{\hat{i_L}(s)}\frac{\hat{i_L}(s)}{\hat{i_{ref}}(s)} \tag{2.8}$$

$$\frac{\hat{V}_o(s)}{\hat{i_{ref}}(s)} = G_{iLid}(s)G_cZ_o(s) \tag{2.9}$$

G_{iLid} is the transfer function of $\hat{i_d(s)}$ to $\hat{i_L(s)}$ and it is derived from the average diode current which is same as load current.

$$i_d = (1-d)i_L \tag{2.10}$$

$$(I_d + \hat{i_d}) = (I_L + \hat{i_L}) - (D + \hat{d})(I_L + \hat{i_L}) \tag{2.11}$$

Taking Laplace and neglecting small signal terms.

$$\hat{i_d(s)} = \hat{i_L(s)} - D\hat{i_L(s)} - I_L\hat{d(s)} \tag{2.12}$$

$$\frac{\hat{i_d(s)}}{\hat{i_L(s)}} = (1-D) - \frac{I_L}{\frac{\hat{i_L(s)}}{\hat{d(s)}}} \tag{2.13}$$

Now the expression for $\hat{V_o}/\hat{i_{ref}}$ is given by

$$\frac{\hat{V_o}(s)}{\hat{i_{ref}}(s)} = G_c((1-D) - \frac{I_L}{\frac{\hat{i_L(s)}}{\hat{d}(s)}})Z_o(s) \tag{2.14}$$

where, $Z_o(s) = \frac{R}{1+SRC}$

The G_{iLid} transfer function features the occurrence of right half plane zero. This implies, if there is a step increment in I_L, I_d fails to follow initially as it droops and then start increasing Thereby, this inherent delay in response can be seen as effect of right half plane zero.

The reference current is a function of input voltage,output voltage and control voltage voltage PI controller. So, an equivalent expression is required comparing all the three signals i.e, reference current (i_{ref}) Input voltage (V_g) control voltage (V_c) output voltage(V_o).

$$i_{ref} = K\frac{V_g V_c}{V_o^2} \tag{2.15}$$

$$(I_{ref} + \hat{i_{ref}}) = K\frac{(V_g + \hat{v_g})(V_c + \hat{v_c})}{((V_o + \hat{v_o})^2)} \tag{2.16}$$

$$(I_{ref} + \hat{i_{ref}})((V_o + \hat{v_o})^2) = K(V_g + \hat{v_g})(V_c + \hat{v_c}) \tag{2.17}$$

$$\tag{2.18}$$

By the small signal approximation.

$$\hat{i_{ref}} = K\frac{V_c}{V_o^2}\hat{V_g} + K\frac{V_g}{V_o^2}\hat{V_c} - 2\frac{I_{ref}}{V_o}\hat{V_o} \quad (2.19)$$

$$\hat{i_{ref}} = G_g\hat{V_g} + G_c\hat{V_c} - \frac{1}{r_2}\hat{V_o} \quad (2.20)$$

Neglecting the load disturbance the fraction with r_2 term will be zero. The modified block diagram representation is shown in Fig.2.5

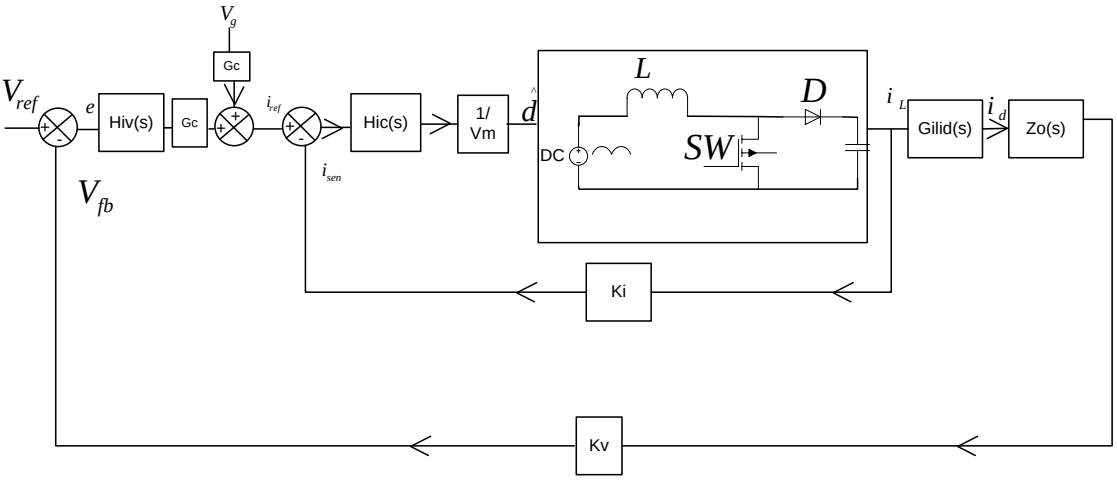

Fig. 2.7 Modified Block diagram of PFC Boost converter

2.4.3 Voltage loop transfer functions

Finally, the total system transfer function $\hat{V_o}/\hat{V_{ref}}$ with both current loop and voltage loop been closed can be obtained as:

$$\frac{\hat{V_o}(s)}{\hat{V_{ref}}(s)} = \frac{G_{VoVc}H_{iv}(s)}{1 + G_{VoVc}H_{iv}(s)} \quad (2.21)$$

$$G_{VoVc} = \frac{\hat{V_o}(s)}{\hat{V_c}(s)} \quad (2.22)$$

$$= \frac{\hat{V_o}(s)}{\hat{i_L}(s)}\frac{\hat{i_L}(s)}{\hat{i_{ref}}(s)}\frac{\hat{i_r ef}(s)}{\hat{V_c}(s)} \quad (2.23)$$

$$= \frac{T_v(s)}{1 + T_v(s)} \quad (2.24)$$

2.5 Frequency response characteristics

The bandwidth of the voltage control loop is determined by the amount of input distortion to be contributed by the output ripple voltage. If the output capacitor is small and the distortion must be low then the bandwidth of the loop will be low so that the ripple voltage will be sufficiently attenuated by the error amplifier. Transient response is a function of the loop bandwidth and the lower the bandwidth the slower the transient response and the greater the overshoot. The output capacitor may need to be large to have both fast output transient response and low input current distortion. Generally the bandwidth of the current loop will be 1/10th of the plant band width. So the current loop bandwidth is chosen to be 7kHz and a low voltage loop bandwidth of 21Hz.

The technique used to design the loop compensation is to find the amount of attenuation of the output ripple voltage required in the error amplifier and then work back into the unity gain frequency. The loop will have the maximum bandwidth when the phase margin is the smallest. A 45 degree phase margin is a good compromise which will give good loop stability and fast transient response and which is easy to design. The voltage error amplifier response which results will have flat gain up to the loop unity gain frequency and will have a single pole roll off above that frequency. This gives the maximum amount of attenuation at the second harmonic of the line frequency from a simple circuit, gives the greatest bandwidth and provides a 45 degree phase margin[1].

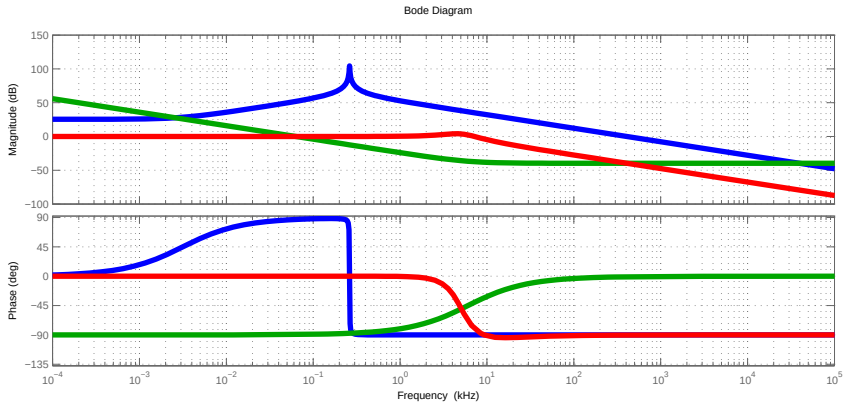

Fig. 2.8 Frequency response of current loop

The compensation of the current error amplifier provides flat gain near the switching frequency and uses the natural roll off of the boost power stage to give the correct

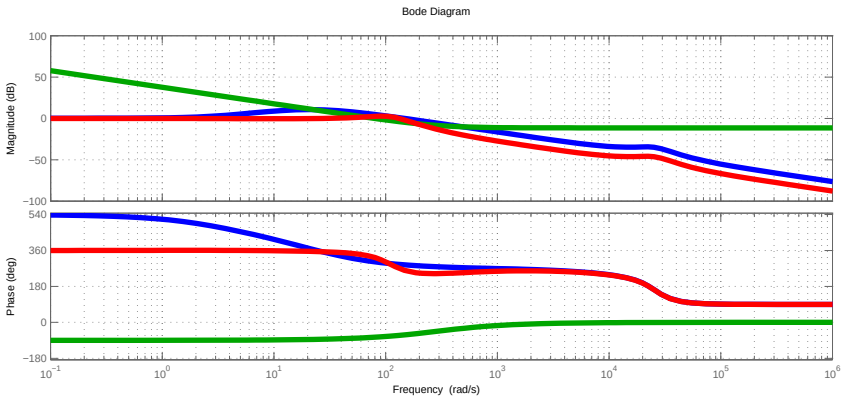

Fig. 2.9 Frequency response of voltage loop

compensation for the total loop. A zero at low frequency in the amplifier response gives the high gain which makes average current mode control work. The gain of the error amplifier near the switching frequency is determined by matching the down slope of the inductor current when the switch is off with the slope of the ramp generated by the oscillator.

2.6 Design of PFC boost converter Power board

2.6.1 Specifications

The design process starts with the specifications for the converter performance. The minimum and maximum line voltage, the maximum output power, and the input line frequency range must be specified.

Maximum power output: 250W

Input voltage range: 80-230Vac

Line frequency range: 50Hz

The output voltage of a boost regulator must be greater than the peak of the maximum input voltage and a value 5%to 10% higher than the maximum input voltage is recommended so the output voltage is chosen to be 400Vdc.

2.6.2 Switching Frequency

The choice of switching frequency is generally somewhat arbitrary. The switching frequency must be high enough to make the power circuits small and minimize the distortion and must be low enough to keep the efficiency high. In most applications a switching frequency in the range of 20kHz to 300kHz proves to be an acceptable compromise. The converter uses a switching frequency of 60kHz as a compromise between size and efficiency. The value of the inductor will be reasonably small and cusp distortion will be minimized, the inductor will be physically small and the loss due to the output diode will not be excessive. Converters operating at higher power levels may find that a lower switching frequency is desirable to minimize the power losses. Turn-on snubbers for the switch will reduce the switching losses and can be very effective in allowing a converter to operate at high switching frequency with very high efficiency.

2.6.3 Inductor Selection

The inductor determines the amount of high frequency ripple current in the input and its value is chosen to give some specific value of ripple current.Inductor value selection begins with the peak current of the input sinusoid[3]. The maximum peak current occurs at the peak of the minimum line voltage and is given by:

$$I_{line} = \frac{\sqrt{2}P}{Vin_{min}} \tag{2.25}$$

For the given specifications the maximum peak line current is 4.42 amps at a Vin of 80Vac.

The maximum ripple current in a boost converter occurs when the duty factor is 50% which is also when the boost ratio M=Vo/Vin=2. The peak value of inductor current generally does not occur at this point since the peak value is determined by the peak value of the programmed sinusoid. The peak value of inductor ripple current is important for calculating the required attenuation of the input filter.

The peak-to-peak ripple current in the inductor is normally chosen to be about 20% of the maximum peak line current. This is a somewhat arbitrary decision since this is

usually not the maximum value of the high frequency ripple current. A larger value of ripple current will put the converter into the discontinuous conduction mode for a larger portion of the rectified line current cycle and means that the input filter must be larger to attenuate more high frequency ripple current.The value of the inductor is selected from the peak current at the top of the half sine wave at low input voltage, the duty factor D at that input voltage and the switching frequency. The two equations necessary are given below:

$$D = \frac{V_o - V_{in}}{V_o} \tag{2.26}$$

$$L = \frac{V_{in} * D}{f_s * \delta I} \tag{2.27}$$

Where δI is the peak-to-peak ripple current.For the specification D=0.71 δI=0.9 A and L=306μH

The high frequency ripple current is added to the line current peak so the peak inductor current is the sum of peak line current and half of the peak to peak high frequency ripple current.The inductor must be designed to handle this current level. The peak inductor current is 5.0 amps. The peak current limit will be set about 10% higher at 5.5 amps.

2.6.4 Output Capacitor

The factors involved in the selection of the output capacitor are the switching frequency ripple current,the second harmonic ripple current, the DC output voltage, the output ripple voltage and the hold-up time. The total current through the output capacitor is the RMS value of the switching frequency ripple current and the second harmonic of the line current.The large electrolytic capacitors which are normally chosen for the output capacitor have an equivalent series resistance which changes with frequency and is generally high at low frequencies.The amount of current which the capacitor can handle is generally determined by the temperature rise. It is usually not necessary to calculate an exact value for the temperature rise. It is usually adequate to calculate the temperature rise due to the high frequency ripple current and the low frequency ripple current and add them together. The capacitor data sheet will provide the necessary ESR and temperature rise information.

The hold-up time of the output often dominates any other consideration in output

capacitor selection. Hold-up is the length of time that the output voltage remains within a specified range after input power has been turned off Hold-up times of 15 to 50 milliseconds are typical. In off-line power supplies with a 400Vdc output the hold-up requirement generally works out to between 1 and 2pF per watt of output.If hold-up is not required the capacitor will be much smaller, perhaps 0.2pF per watt, and then ripple current and ripple voltage are the major concern.Hold-up time is a function of the amount of energy stored in the output capacitor, the load power, output voltage and the minimum voltage the load will operate at. This can be expressed in an equation to define the capacitance value in terms of the holdup time.

$$C_o = \frac{2 * P * \delta t}{V_o^2 - V_{omin}^2} \tag{2.28}$$

Where Co is the output capacitor, Pout is the load power, At is the hold-up time, Vo is the output voltage and Vo(min) is the minimum voltage the load will operate at. By substituting it will be around 120μF

2.6.5 Switch and Diode

The switch and diode must have ratings which are sufficient to insure reliable operation.The switch must have a current rating at least equal to the maximum peak current in the inductor and a voltage rating at least equal to the output voltage. The same is true for the output diode. The output diode must also be very fast to reduce the switch turn-on power dissipation and to keep its own losses low. The switch and diode must have some level of derating and this will vary depending on the application.

For the circuit the diode is a high speed, high voltage type with 35ns reverse recovery, 600Vdc breakdown, and 8A forward current ratings. The power MOSFET in the example circuit has a 650Vdc breakdown and 22Adc current rating. A major portion of the losses in the switch are due to the turn-off current in the diode. The peak power dissipation in the switch is high since it must carry full load current plus the diode reverse recovery current at full output voltage from the time it turns on until the diode turns off. The diode in the converter was chosen for its fast turn off and the switch was over sized to handle the high peak power dissipation.

2.7 Evaluation of losses in low line full load condition

2.7.1 RMS Values of Rectifier Waveforms

A typical waveform such as the transistor current of the boost converter is pulse width modulated, with both the duty cycle and the peak amplitude varying with the ac input voltage. When the switching frequency is much larger than the ac line frequency, then the rms value can be well-approximated as a double integral. The square of the current is integrated first to find its average over a switching period, and the result is then integrated to find the average over the ac line period. The transistor current in the boost rectifier is found to be quite low.The RMS value of the transistor current is defined as

$$I_{Qrms} = \sqrt{\frac{1}{T_{ac}} \int_0^{T_{ac}} i_Q^2(t)} \tag{2.29}$$

where Tac is the period of the ac line waveform. The integral can be expressed as sum of integrals over all of the switching periods contained in one ac line period:

$$I_{Qrms} = \sqrt{\frac{1}{T_{ac}} T_s \sum_{n=1}^{\frac{T_{ac}}{T_s}} (\frac{1}{T_s} \int_{(n-1)T_s}^{nT_s} i_Q^2(t))} \tag{2.30}$$

where Ts is the switching period. The quantity inside the parenthesis is the value of

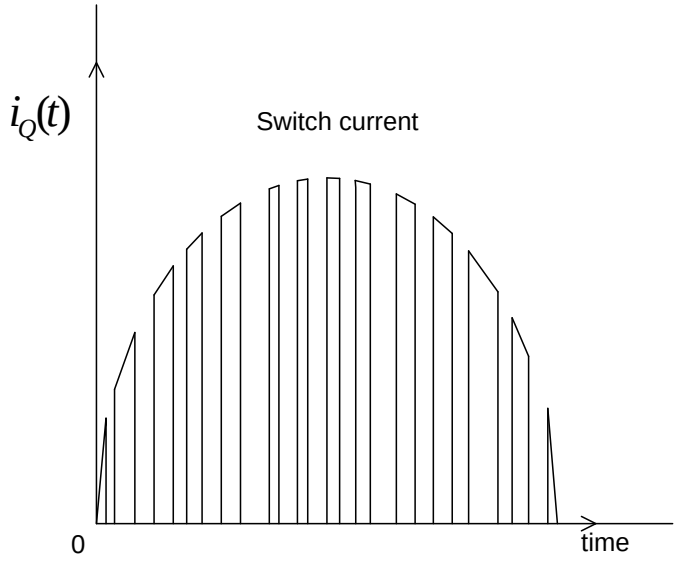

Fig. 2.10 Switch Current waveform

i_Q^2 averaged over the nth switching period. The summation can be approximated by an integral in the case when Ts is much less than Tac. This approximation corresponds to taking the limit as Ts tends to zero, as follows:

$$I_{Qrms} = \sqrt{\frac{1}{T_{ac}} \lim_{T_s \to} (T_s \sum_{n=1}^{\frac{T_{ac}}{T_s}} (\frac{1}{T_s} \int_{(n-1)T_s}^{nT_s} i_Q^2(\tau) d(\tau)} \quad (2.31)$$

$$= \sqrt{\frac{1}{T_{ac}} \int_0^{T_{ac}} \frac{1}{T_{ac}} \int_t^{t+T_s} i_Q^2(\tau) d(\tau)} \quad (2.32)$$

$$= \sqrt{<< i_Q^2(t) >_{T\ s} >_{T\ ac}} \quad (2.33)$$

So $i_Q^2(t)$ is first averaged over one switching period. The result is then averaged over the ac line period, and the square root is taken of the result.

2.7.2 RMS Values of Boost Rectifier Waveforms

For the boost rectifier, the transistor current $i_Q(t)$ is equal to the input current when the transistor conducts, and is zero when the transistor is of. Therefore, the average of $i_Q^2(t)$ over one switching period is

$$< i_Q^2(t) >_{T\ s} = \frac{1}{T_{ac}} \int_t^{t+T_s} i_Q^2(t) \quad (2.34)$$

$$= d(t) i_{ac}^2(t) \quad (2.35)$$

If the input voltage is given by

$$v_{ac} = V_M sinwt \quad (2.36)$$

then the input current will be

$$i_{ac}(t) = \frac{V_M}{R_e} sinwt \quad (2.37)$$

where Re is the emulated resistance. With a constant output voltage V, the transistor duty cycle must obey the relationship

$$\frac{V}{v_{ac}(t)} = \frac{1}{(1 - d(t))} \quad (2.38)$$

This assumes that the converter dynamics are fast compared to the ac line frequency. So d(t) can be written as

$$d(t) = 1 - \frac{V_M}{V} sinwt \tag{2.39}$$

So the average of $i_Q^2(t)$ over one switching period becomes

$$< i_Q^2(t) >_{T_s} = \frac{V_M^2}{R_e^2}(1 - \frac{V_M}{V} sinwt) sin^2 wt \tag{2.40}$$

Then plug in this expression into I_{Qrms} Equation

$$I_{Qrms} = \sqrt{\frac{1}{T_{ac}} \int_0^{T_{ac}} < i_Q^2(t) >_{T\ ac}} \tag{2.41}$$

$$= \sqrt{\frac{1}{T_{ac}} \int_0^{T_{ac}} \frac{V_M^2}{R_e^2}(1 - \frac{V_M}{V} sinwt) sin^2 wt d(t)} \tag{2.42}$$

which can be further simplified to

$$I_{Qrms} = \sqrt{\frac{2}{T_{ac}} \frac{V_M^2}{R_e^2} \int_0^{T_{ac}/2} (sin^2 wt - \frac{V_M}{V} sin^3 wt) d(t)} \tag{2.43}$$

This involves integration of powers of sin(wt) over a complete half-cycle. The integral can be evaluated with the help of the following formula:

$$\frac{1}{\pi} \int_0^{\pi} sin(\theta d(\theta) = \begin{cases} \frac{2}{\pi} \frac{2.4.6....(n-1)}{1.3.5....n} \, if \, n \, is \, odd \end{cases} \tag{2.44}$$

$$= \begin{cases} \frac{1.3.5....(n-1)}{2.4.6..n} \, if \, n \, is even \end{cases} \tag{2.45}$$

This type of integral commonly arises in rms calculations involving PWM rectifiers. Evaluation of the integral in the above equations leads to the following result:

$$I_{Qrms} = I_{acrms} \sqrt{1 - \frac{8}{3\pi} \frac{V_M}{V}} \tag{2.46}$$

It can be seen that the rms transistor current is minimized by choosing the output voltage V to be as small as possible. Larger value of V leads to larger rms transistor current.

A similar analysis for the rms diode current leads to the following expression.

$$I_{Drms} = I_{acrms}\sqrt{\frac{8}{3\pi}\frac{V_M}{V}} \tag{2.47}$$

From the above switch current and the diode current expression various losses are calculated for the low line full load conditions $V_{ac} = 90V$ and the full load which is 250W.

Switch RMS current

$$\begin{aligned} I_{Qrms} &= I_{acrms}\sqrt{1-\frac{8}{3\pi}\frac{V_M}{V}} && (2.48)\\ &= 2.77\sqrt{1-\frac{8}{3\pi}\frac{90\sqrt{2}}{400}} && (2.49)\\ &= 2.36A && (2.50) \end{aligned}$$

Diode RMS current

$$\begin{aligned} I_{Drms} &= I_{acrms}\sqrt{\frac{8}{3\pi}\frac{V_M}{V}} && (2.51)\\ &= 2.77\sqrt{\frac{8}{3\pi}\frac{90\sqrt{2}}{400}} && (2.52)\\ &= 1.43A && (2.53) \end{aligned}$$

Load current

The load current or output current depends on the load power. It is the ratio of load power to the output voltage and the expression is given as

$$\begin{aligned} I_{orms} &= \frac{P}{V} && (2.54)\\ &= \frac{250}{400} && (2.55)\\ &= 0.625A && (2.56) \end{aligned}$$

Capacitor RMS current

$$\begin{aligned} I_{crms} &= \sqrt{I_{Drms}^2 - I_{orms}^2} && (2.57)\\ &= \sqrt{1.43^2 - 0.625^2} && (2.58)\\ &= 1.286A && (2.59) \end{aligned}$$

So the power Loss associated with the Ripple current that is output capacitor loss can be calculated as given below.Each capacitor having $173m\Omega$ ESR. Here totally 2 capacitors are in series. So total ESR is $346m\Omega$.

$$\begin{aligned} P_{caploss} &= I_{crms}^2 * R_{esr} && (2.60)\\ &= (1.286^2)(0.346) && (2.61)\\ &= 0.577W && (2.62)\\ & && (2.63) \end{aligned}$$

2.7.3 Losses in Diode Bridge Rectifier

The rectifier bridge power dissipation can be calculated by finding the input RMS current and the input average current through the bridge diodes.

$$\begin{aligned} I_{brms} &= \frac{\sqrt{2}I_{acrms}}{2} && (2.64)\\ &= \frac{\sqrt{2} * 2.77}{2} && (2.65)\\ &= 1.95A && (2.66) \end{aligned}$$

$$\begin{aligned} I_{bavg} &= \frac{\sqrt{2}I_{acrms}}{\pi} && (2.67)\\ &= \frac{\sqrt{2} * 2.77}{\pi} && (2.68)\\ &= 1.24A && (2.69) \end{aligned}$$

The power dissipated in diode bridge rectifier can be calculated with threshold voltage(V_{th}) and dynamic resistance(R_{diode}) of a single diode of the bridge which will be given in the data sheet.

$$\begin{aligned} P_{bloss} &= 4 * R_{diode} * I_{brms}^2 + 4 * V_{th} * I_{bavg} && (2.70)\\ &= 4 * 0.05 * 1.95^2 + 4 * 0.7 * 1.24 && (2.71)\\ &= 2.21W && (2.72) \end{aligned}$$

2.7.4 Losses in Power MOSFET

The power Losses of the MOSFET are mainly the sum of the conduction, switching and capacitive losses.
MOSFET Power Loss = Conduction Loss + Switching Loss + Capacitive Loss

Conduction Losses

At low line full load condition the conduction losses can be calculated as given.

$$P_{cond} = R_{DSon} * I_{Qrms}^2 \tag{2.73}$$

In order to properly calculate the conduction losses at 100řC that is typical MOSFET junction temperature, a factor K_{TEMP} between 1.5 to 2, which can be given in the data sheet,should be taken into account.
In IPW60R045CS data sheet looking at the normalized On resistance(R_{DSon}) Vs temperature(Tj) graph, a factor 0.175 should be considered at 100řC. So K_{TEMP} =0.175 and R_{DSon}= 0.045Ω at 25°C.
R_{DSon}at 100°C.

$$R_{DSon} = \frac{R_{DSon}}{No\,of\,parallel\,mosfet's} * K_{TEMP} \tag{2.74}$$
$$= 0.045 * 0.175 \tag{2.75}$$
$$= 7.85 * 10^{-3}\Omega \tag{2.76}$$

Therefore the conduction loss is given as

$$P_{cond} = R_{DSon} * I_{Qrms}^2 \tag{2.77}$$
$$= (0.00787) * (2.36^2) \tag{2.78}$$
$$= 0.044W \tag{2.79}$$

Switching Losses

The switching losses depend on the particular switching waveform, determined by many factors like driving current, gate resistors, MOSFET gate internal resistance,V_{th}, gate charge, total capacitance on the drain node including parasitic capacitances etc.

$$P_{sw} = \frac{1}{2} * V_{ds} * I_d * (t_{rise} + t_{fall}) f_{sw} \tag{2.80}$$

where,

$V_{ds} \rightarrow$ Drain to source voltage

$I_d \rightarrow$ Drain current

$t_{rise}\, t_{fall} \rightarrow$ Rise time and fall time

To estimate the rising and falling times of the drain voltage, data sheet values of the switching performances of the MOSFET can be used.

Average Rise time:

The average rise time of the drain voltage can be calculated considering the total drain node capacitance and the average value of the peak current flowing through the inductor. The exact value of the MOSFET C_{oss} is indicated in the data sheet of IPW60R045CS. From Coss vs VDS graph at VDS equal to 400V, $C_{oss}$is 320 pF. So the drain node capacitance C_D can be taken as above capacitance value.The average rising time of the drain voltage is

$$t_{rise} = \frac{C_D * V_{DS}}{I_{Davg}} \tag{2.81}$$

$$= \frac{C_D * V_{DS}}{\frac{1}{\pi}\int_0^{\pi} sin(\theta) d\theta} \tag{2.82}$$

$$= \frac{320 * 10^{-}12 * 400}{33.14} \tag{2.83}$$

$$= 3.74ns \tag{2.84}$$

Average Falling time:

However, the average falling time depends on the driving current I_G which is limited by the resistor placed on the gate, the MOSFET total gate charge Q_G and the driving voltage V_{dr} which is equal to Vcc (15V). In the resistor calculation the intrinsic gate resistance should also be considered. In the case of the IPW60R045CS, R_G is 1.6Ω

which has to be added to the externally placed resistor $R_{Gext} = 3.3\Omega$.

$$t_{fall} = \frac{Q_G}{I_G} \tag{2.85}$$
$$= \frac{Q_G}{\frac{V_{dr}}{R_{ext}+R_G}} \tag{2.86}$$
$$= 38.87ns \tag{2.87}$$

The total gate charge Q_G is given in the data sheet. Finally the MOSFET switching losses can be estimated as given below.

$$P_{sw} = \frac{1}{2} * V_{ds} * I_d * (t_{rise} + t_{fall}) f_{sw} \tag{2.88}$$
$$= \frac{1}{2} * 400 * 2.67 * (3.87 + 38.87) 60000 \tag{2.89}$$
$$= 1.36W \tag{2.90}$$

To estimate the capacitive losses, that is the losses due to the discharge of the total drain capacitance through the MOSFET at turn-on, this expression can be considered.

$$P_{cap} = \frac{1}{2} * C_D * V_{DS}^2 * f_{sw} \tag{2.91}$$
$$= \frac{1}{2} * 320 * 10^{-}12 * 400^2 * 60000 \tag{2.92}$$
$$= 1.488W \tag{2.93}$$

So in MOSFET the total losses are calculated below

$$P_{loss} = P_{cond} + P_{sw} + P_{cap} \tag{2.94}$$
$$= 0.044 + 1.36 + 1.488 \tag{2.95}$$
$$= 2.892W \tag{2.96}$$

2.7.5 Losses in Power Diode

Conduction Loss

The diode Average and RMS current values, the diode threshold voltage(V_{th}) and dynamic resistance(R_d) which are given in the data sheet allow calculating losses. From

the RURG8060 data sheet, the values ofV_{th} at junction temperature of 25°C is 0.94V and R_d is 53.05 m$\Omega$are given.
So the conduction losses in diode is given below.

$$P_{Diode.cond} = V_{th} * I_o + R_D * I^2_{Drms} \quad (2.97)$$
$$= (0.94) * (0.625) + (0.053)(1.43^2) \quad (2.98)$$
$$= 0.695W \quad (2.99)$$

2.7.6 Loss due to ESR of inductance

Every inductor has equivalent series resistance in it. The Loss due to this is

$$I^2_{Lrms} * R_{esr} = 2.77^2 * 31.2m\Omega = 0.239W \quad (2.100)$$

Reverse Recovery Loss

The energy losses due to the reverse recovery effect of the diode is

$$E_{rr} = V_R * Q_{rr} \quad (2.101)$$

where,
$V_R \rightarrow$Reverse voltage across the output diode, when it stops conducting that is 400V.
$Q_{rr} \rightarrow$Reverse recovery charges(Charge must be dissipated through MOSFET)
The Diode RURG8060 is Silicon Carbide Schottky Diode. It has zero reverse recovery current. So if we considered reverse recovery charge Q_{rr}=50nC. So the energy losses due to the reverse recovery effect of the diode is

$$E_{rr} = 400 * 50nC \quad (2.102)$$
$$= 20\mu J \quad (2.103)$$

So the reverse Recovery losses can be calculated as given below.

$$P_{rr} = E_{rr}F_{sw} \quad (2.104)$$

$$= 20\mu * 60000 \quad (2.105)$$

$$= 1.2W \quad (2.106)$$

2.7.7 Total Losses

The total losses in a PFC boost converter is evaluated and theoretical efficiency is calculated. Table.2.1 shows the complete losses in converter. The sum of all losses gives

S.No	Parameter	Losses
1	Diode Bridge rectifier Losses	2.21 W
2	Mosfet Losses	2.892 W
3	Diode Conduction Losses	0.695 W
4	Inductor ESR Loss	0.239 W
5	Capacitor ESR Loss	0.577 W
6	Reverse recovery loss	1.2 W

Table 2.1 Total losses in PFC boost converter

about 7.813 W. Therefore the theoretical efficiency can be calculated

$$\eta = \frac{P_o}{P_o + Losses} \quad (2.107)$$

$$= 96.8\% \quad (2.108)$$

CHAPTER 3

SIMULATION AND HARDWARE TEST RESULT OF FRONT END CONVERTER

3.1 Introduction

In this chapter a 250 W power level PFC boost converter Simulation is proposed. The various waveforms such as Input voltage,Output voltage inductor current, output current are listed in following section. The same power level hardware prototype is developed and different test are carried on it.

3.2 Simulation of 250W PFC Boost converter

Simulation of a single phase PFC for AC to DC boost converter is done by use of MATLAB software package. Fig.3.1-Fig.3.7 shows waveforms of various quantities associated with the boost converter under voltage range specified (80-230V). Simulation is carried by Varying the supply voltage at 80V to 230V and full load of 250W. Then a huge current is drawn by the inductor. Inductor is so chosen to with stand the current.The feed forward voltage causes the power input to remain constant at given control voltage. The output of the voltage error amplifier actually controls the power delivered to the load.If the output of the voltage error amplifier is constant and the input voltage is doubled the programming signal will double but it will be divided by the square of the feed forward voltage, or four times the input, which will result in the input current being reduced to half its original value. Twice the input voltage times half the input current results in the same input power as before. The output of the voltage error amplifier, then, controls the input power level of the power factor corrector.

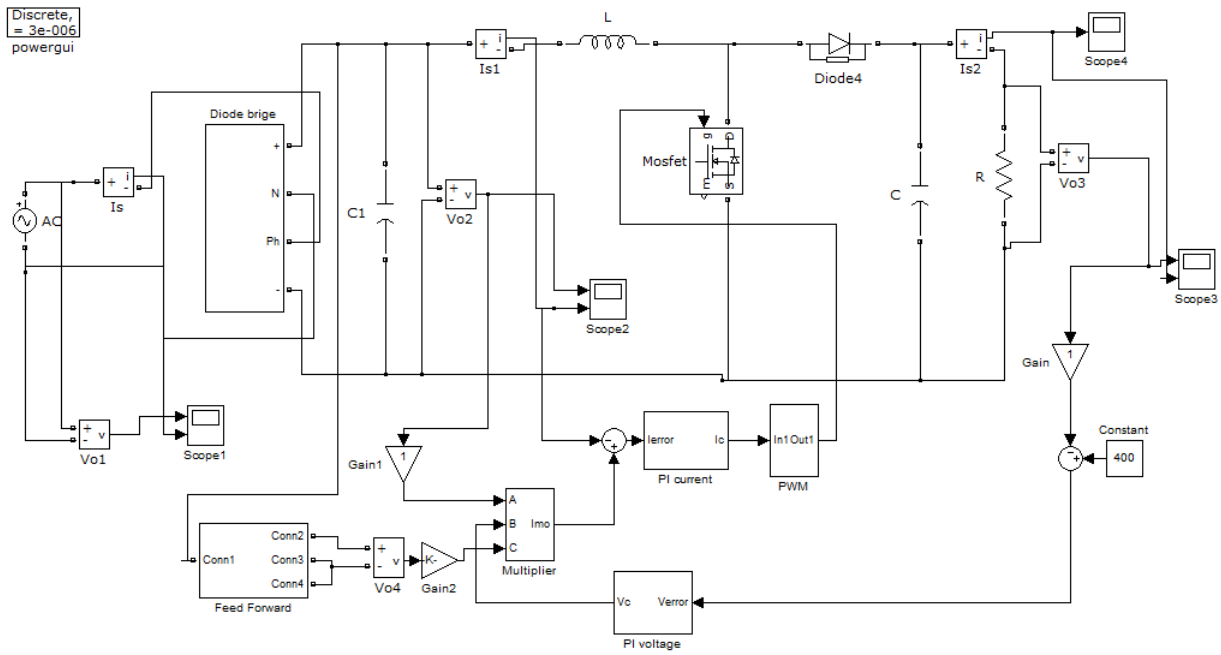

Fig. 3.1 Simulation of 250W PFC Boost Converter

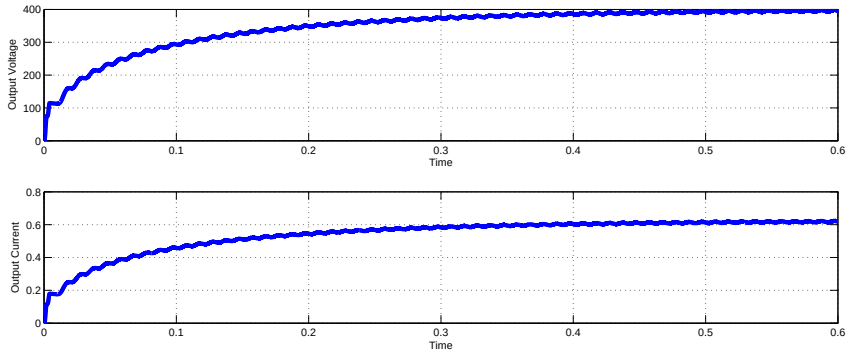

Fig. 3.2 Output Voltage and Output current for low line of 80V

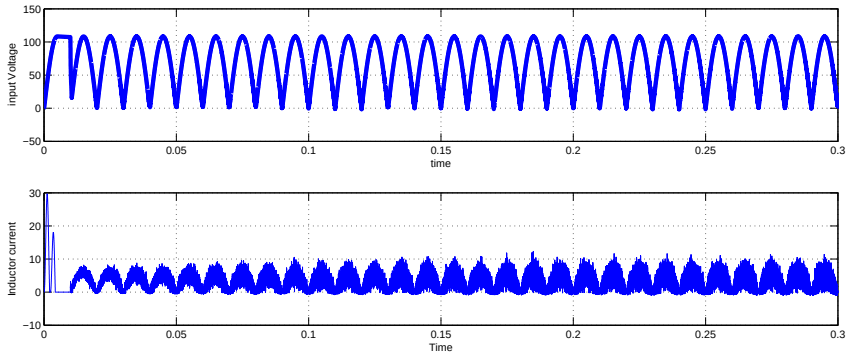

Fig. 3.3 Input voltage and Inductor current for low line of 80V

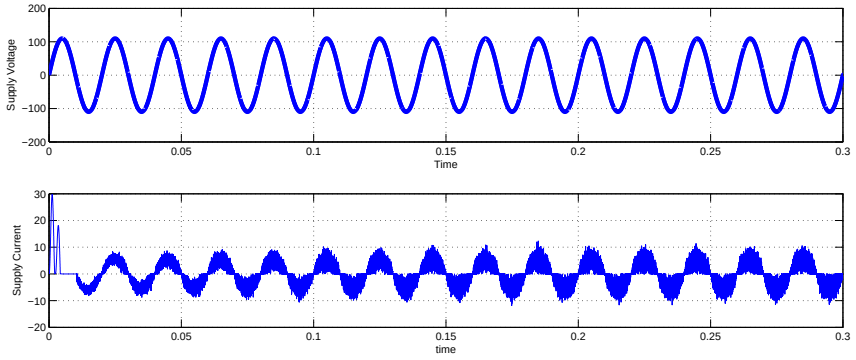

Fig. 3.4 Supply Voltage and Current for low line of 80V

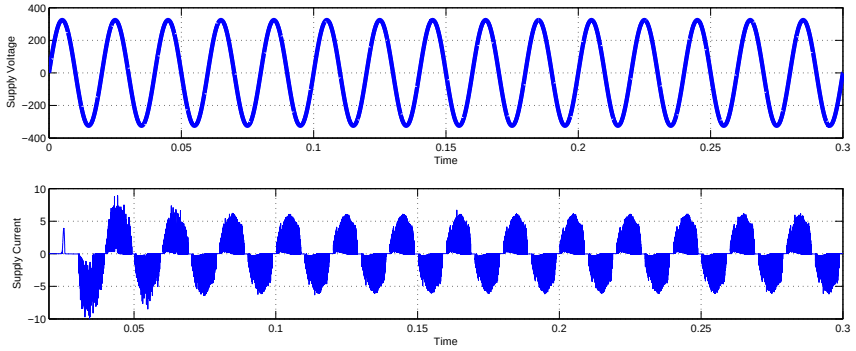

Fig. 3.5 Supply Voltage and Current for full line of 230V

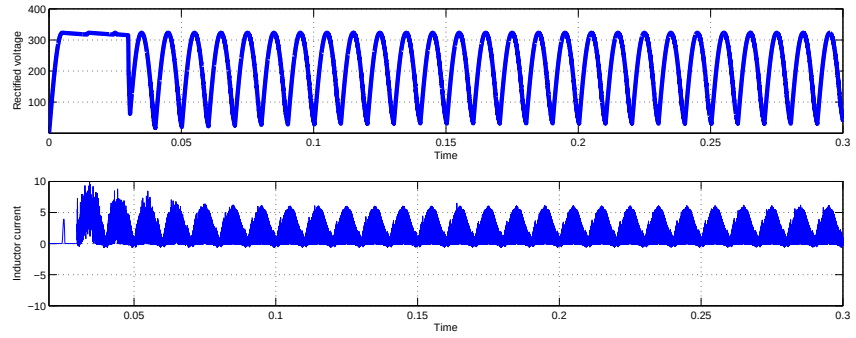

Fig. 3.6 Input voltage and Inductor current for full line of 230V

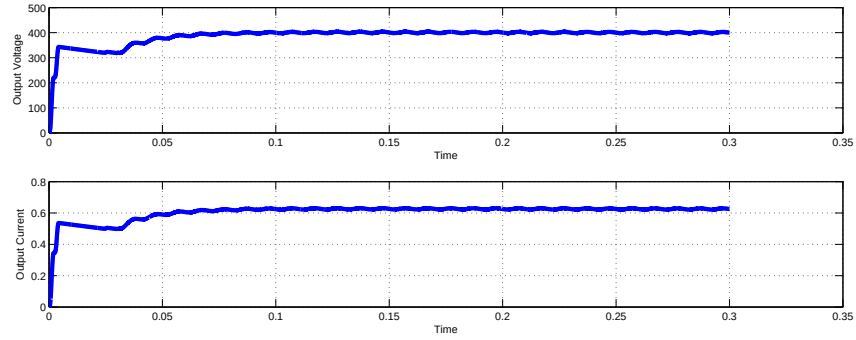

Fig. 3.7 Output Voltage and Output current for full line of 230V

3.3 Experimental Result

Different test are conducted on the hardware setup of PFC Boost converter. The various test are:

- DC Test
- Open loop Test
- Current loop closed converter
- Voltage loop closed converter

3.3.1 DC Test

The power board of PFC boost converter is fed with DC voltage of 15V supply. Here sine pulse width modulation technique is used. Pulses are generated with IC TL494CN with desired duty of 65% and given to the gate to source voltage of the mosfet. In the second case the duty cycle is changed to changed to 30%. With the reduction in duty, the time taken by the inductor to charge is reduced. The input voltage is varied from 15V to 30V and the respective output voltage is noted.

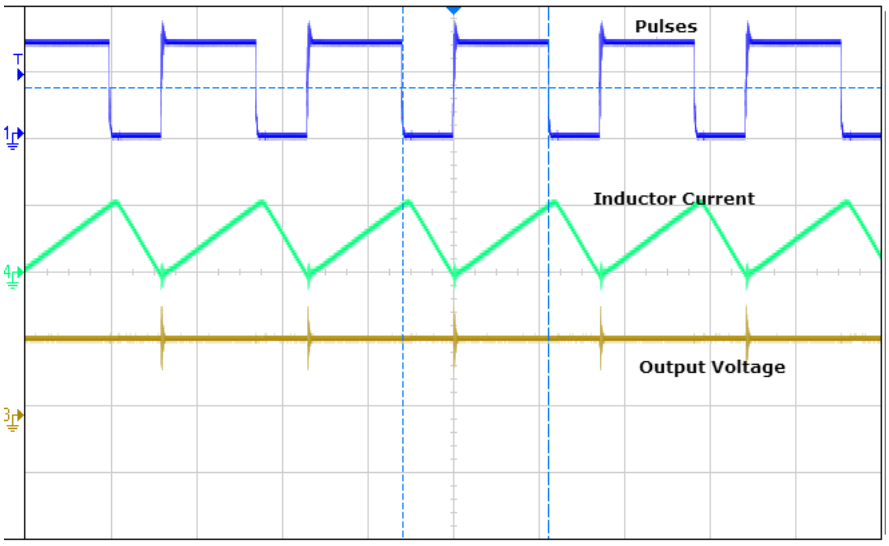

Fig. 3.8 Inductor current with Duty of 65%
Ch1:10V/div,Ch2:500mA/div,Ch3:40V/div.

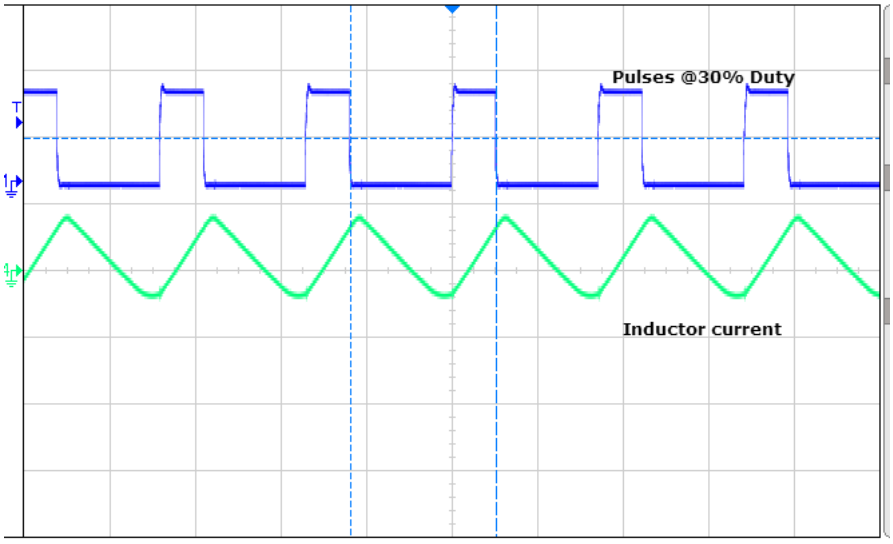

Fig. 3.9 Inductor current with Duty of 30%
Ch1:10V/div,Ch2:500mA/div.

Input voltage	Output Voltage
15	45
20	61
30	91

Table 3.1 DC test with a duty of 65%

Input voltage	Output Voltage
15	23
20	30
30	48

Table 3.2 DC test with a duty of 30%

3.3.2 Open loop Test

In this the input voltage to the PFC boost converter is fed from output of the rectifier.Pulses are generated with IC TL494CN with fixed duty and given to the gate to source voltage of the mosfet. The duty is fixed here,it does not change with the input voltage. In the sine pulse width modulation, as the reference signal to TL494CN is constant the pulses generated from the IC has a fixed duty of 75%.

Input voltage	Output voltage	Input current
10	33	0.187A
50	206	1.46A
98	399	2.87A

Table 3.3 Open loop with a given duty of 65%

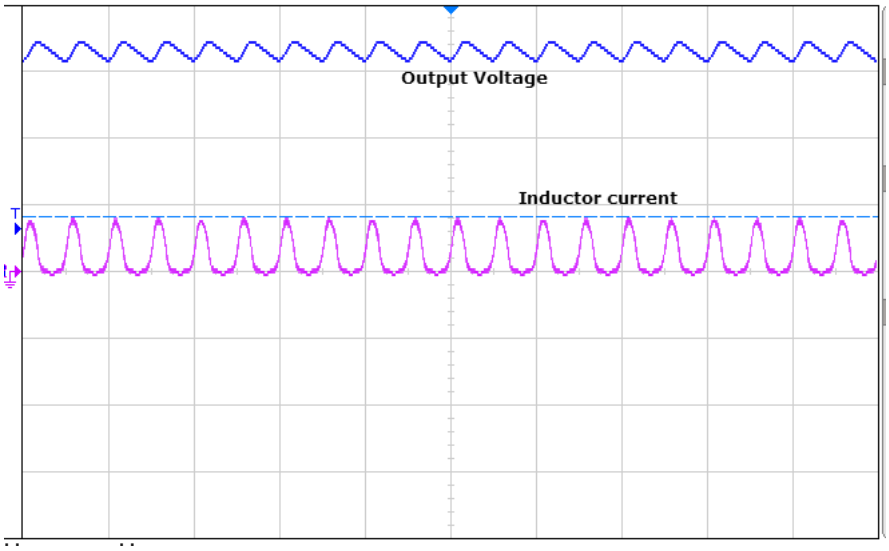

Fig. 3.10 For a very low input voltage
Ch1:10V/div,Ch2:500mA/div.

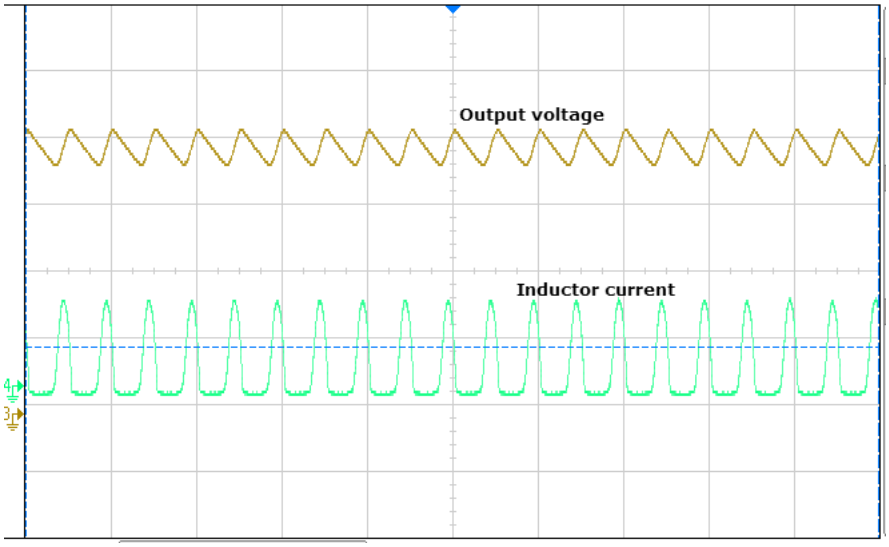

Fig. 3.11 For a full line input voltage
Ch1:10V/div,Ch2:500mA/div.

3.3.3 Current loop closed converter

The voltage loop is removed and in the place of the control voltage a fixed dc voltage of 3V is given to the B point. with feed forward and the control signal reference current is generated. This is compared with the sensed current from the LEM sensor. The PI controller takes necessary action making the current to track the supply voltage. Fig.3.12. shows a Input volatge of 75V a inductor draws a current of 2.45A. As the

Input voltage	Input current
75	2.45A
100	1.44A
140	1.3A
180	1.37A

Table 3.4 Current closed loop with a given duty of 75%

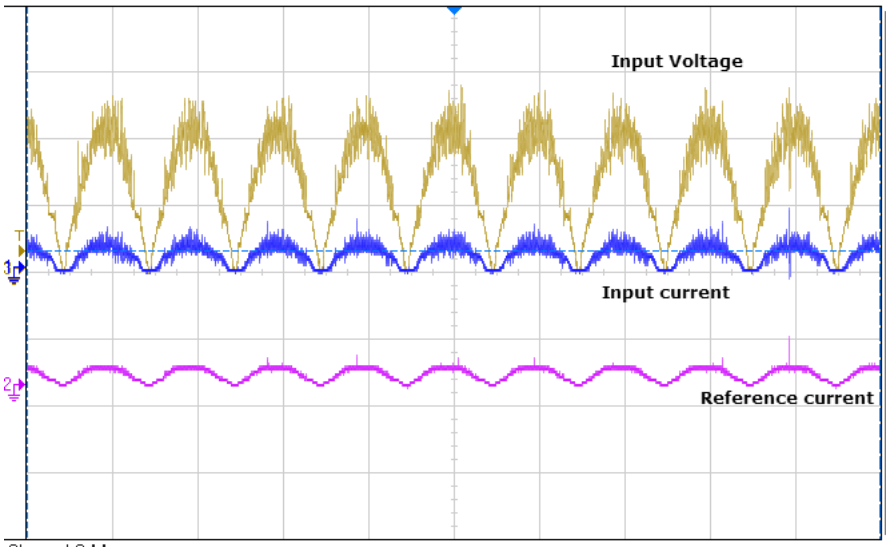

Fig. 3.12 For a low line input voltage
Ch1:10V/div,Ch2:5V/div,Ch3:50V/div.

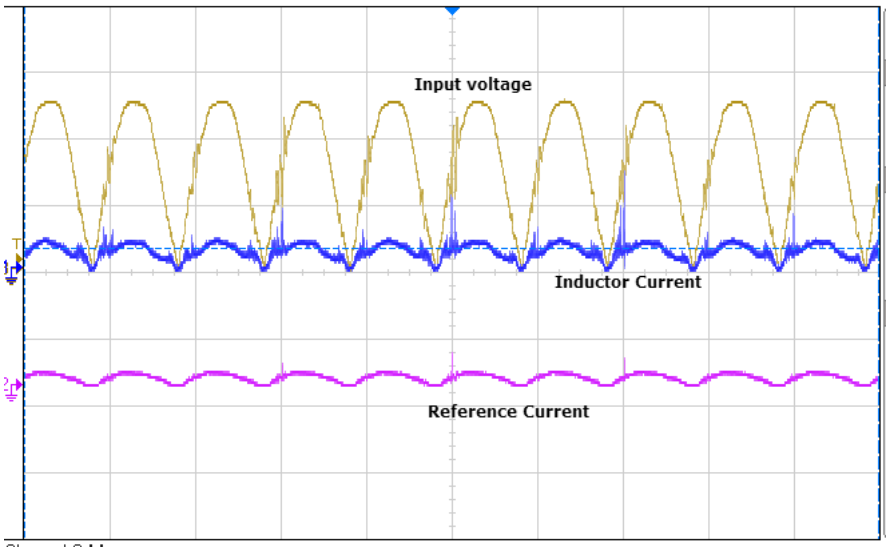

Fig. 3.13 For a full line input voltage
Ch1:10V/div,Ch2:5V/div,Ch3:50V/div.

loop gain is constant for a constant power load with the increase in voltage there should be decrease in current. The tabular column reflects the same.

3.3.4 Voltage loop closed converter

The control voltage which is given as dc in previous current loop is now removed and the voltage loop is closed with PI controller. The output dc voltage of is stepped down to a low value of 6.1V. This volatge is compared with a reference voltage of 6.1V and the error is given to the input of the PI controller. The output of the PI Controller i.e, the control voltage is divided with the feed forward term and given as reference to the current. Whatever change in the output voltage will have a change in voltage loop PI controller and control voltage either increases or decreases to regulate the output voltage.

Input voltage	Output voltage	Input current
100	340	2.21A
140	398	1.63A
157	392	1.45A
170	402	1.34A
204	408	1.2A

Table 3.5 Output voltage regulation

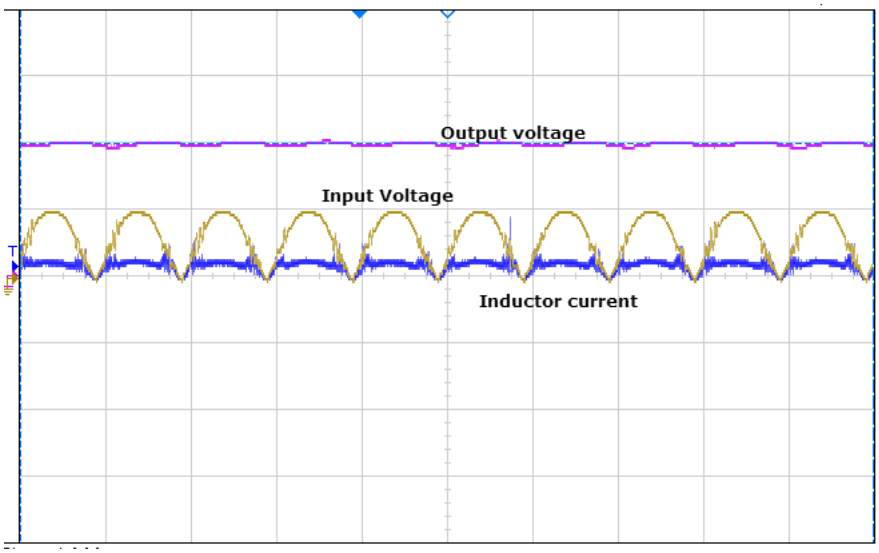

Fig. 3.14 For a voltage of 140V and full load
Ch1:10V/div,Ch2:200V/div,Ch3:200V/div.

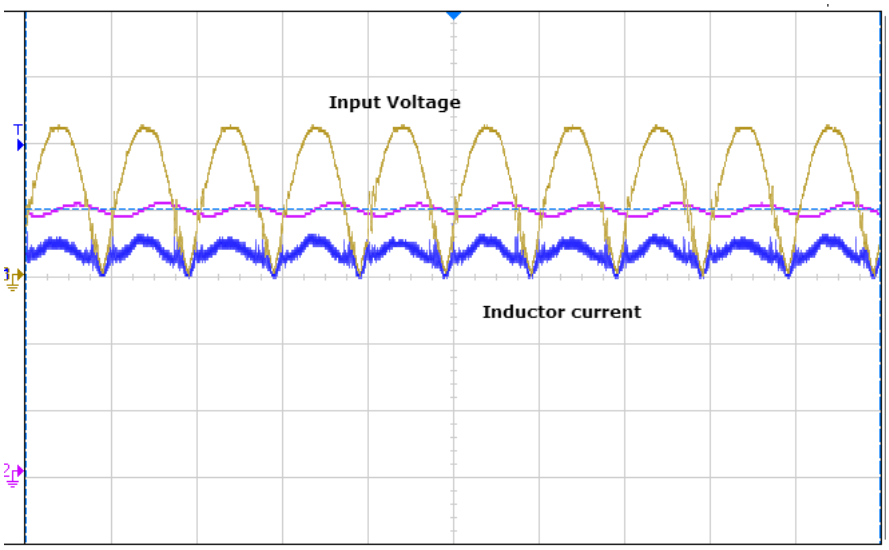

Fig. 3.15 For a voltage of 157V and full load
Ch1:5V/div,Ch2:100V/div,Ch3:100V/div.

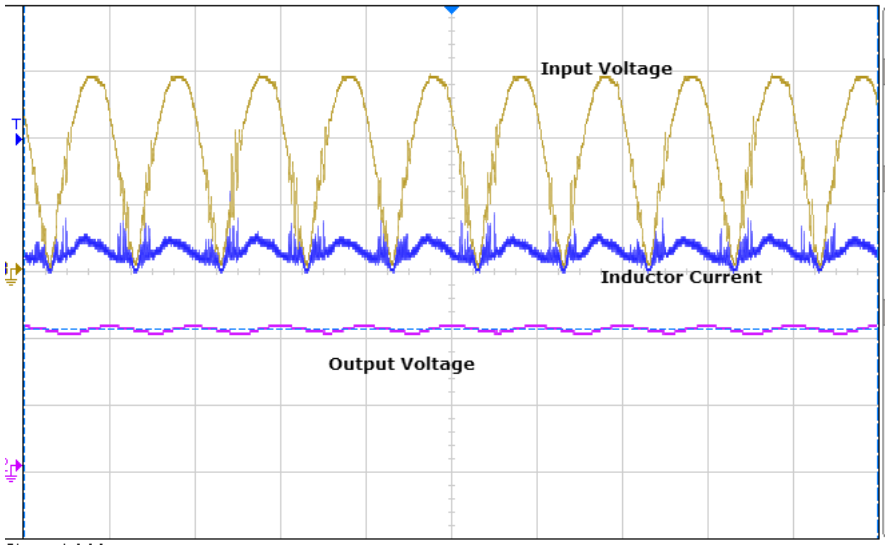

Fig. 3.16 For input voltage 204V and 250W
Ch1:5V/div,Ch2:200V/div,Ch3:100V/div.

CHAPTER 4

CONCLUSION

The need for power factor correction of off line power converters with capacitive input filter has been established. PFC is necessary to increase the utilization efficiency of the AC power and to minimize harmonic pollution of the AC lines. For PFC stage, conventional single switch PFC boost converter is most suitable topology because of its inherent advantages. However, to meet EMI standards, as well as small filter size, switching frequency of PFC boost converter circuit is usually chosen below 150 kHz. The conventional PFC boost converter sacrifices the dynamic response of output voltage during load or line voltage change, owing to the fact of low bandwidth filter in the voltage feedback loop. This sluggish transient response problem is further compounded by large voltage overshoots and voltage drops enforcing additional stress on the PFC boost components, as well as on its downstream switch mode power supply load. Active power factor corrector controls input current of load in such a way that current wave-form is proportional to mains voltage waveform. Hence, the power factor of boost converter will become nearer to unity, which can be clearly seen from the simulation results. Boost converter provides fixed DC voltage, even if input voltage is under certain variations. Thus it is an optimal converter in terms of performance, efficiency and provides unidirectional (DC) power flow in application such as power supplies, electronic ballast and low power drive applications.

REFERENCES

[1] C.Silva, "Power Factor Correction with the UC3854," Application Note Unitrode IC.

[2] Robert W. Erickson, "Fundamentals of Power Electronics," 2nd Edition, Kluwer Aca- demic Publishers

[3] V. Ramanarayanan, "Class notes on Switched Mode Power Conversion"

[4] C.Zhou, "Design and Analysis of an Active Power Factor Correction Circuit", M. S. Thesis, Virginia Polytechnic Institute and State University, Sept.1989.

[5] S. Davis, "Basics of power factor correction design," ED Online 9507, February 3, 2005