DESIGN AND DEVELOPMENT OF DSP AND FPGA BASED DIGITAL CONTROLLERS FOR HIGH POWER DRIVES APPLICATION

A Project Report

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THESIS CERTIFICATE

This is to certify that the thesis titled **DESIGN AND DEVELOPMENT OF DSP AND FPGA BASED DIGITAL CONTROLLERS FOR HIGH POWER DRIVES APPLICATION** , submitted by **K JAYENDRA TEJA**, to the Indian Institute of Technology, Madras, for the award of the degree of **Master of Technology**, is a bona fide record of the research work done by him under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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ABSTRACT

KEYWORDS: Digital Motor Control;Digital Platform;DSC;ADC;Scalar Control of Induction machine;FPGA;

In earlier days, the control of speed and torque of electrical motors was performed using purely analog controllers. With the microcontroller revolution, digital control has become widely popular. This helps in implementing complex control algorithms by which better control of electric motors is possible . Texas Instruments TMS320F28335 digital signal controller, the state of the art in power procesessing applications, based control platform is designed and developed. It is tested by performing scalar control (V/f) of induction motor. Also Altera Cyclone IV FPGA based control board is designed.

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ABBREVIATIONS

ADC	Analog to Digital Converter
CAN	Controller Area Network
DAC	Digital to Analog Converter
DSP	Digital Signal Processor
DSC	Digital Signal Controller
FPGA	Field Programmable Gate Array
JTAG	Joint Test Action Group
LE	Logic Elements
PWM	Pulse Width Modulation
PLL	Phase Locked Loops
SCI	Serial Communication Interface
SPI	Serial Peripheral Interface
TDI	Test Data Input
TDO	Test Data Output
TMS	Test Mode Select
TRSTn	Test Reset
QEP	Quadrature Encoder Pulse
XINTF	External interface

CHAPTER 1

INTRODUCTION

There is a rising interest in using digital control in power electronic applications, especially electric drives. Digital controllers can be implemented in different control platforms like Digital Signal Controllers(DSC), Application Specific Integrated Circuits(ASIC), Field Programmable Gate Arrays (FPGA) and Complex Programmable Logic Devices (CPLD). Now a days, control implementation in DSC and FPGA are commonly used. *In this report, Texas Instruments TMS320F28335 based DSC and Altera Cyclone IV based platforms are designed to meet the requirements of high power motor control applications. A TMS320F28335 based control platform has been developed and all its functionalities have been tested.*

1.1 Digital motor control

Modern drive control algorithms require high speed computing, efficient signal processing capabilities, fast interrupt response and wide program and data memory spaces. Therefore drive control systems require advanced hardware and software platforms for fast, efficient and reliable implementations. Standard microprocessors or microcontrollers do not always satisfy the demands in applications like:

- AC drives with improved dynamic response
- Multi motor drive systems
- Active filters
- Hgh performance servo drives etc

In the above mentioned applications, the microprocessor must perform a lot of computing-intensive and time critical tasks, PWM generation, software control algorithms, estimation and transformation of the state variables, software models and observers, protection functions, external communications protocols etc. Therefore the

processor kernel of digital control system should have various I/O subsytems with functions like:

- Dedicated I/O pins for analog signal acquisition and generation (ADC and DAC control)
- Interface for absolute and incremental encoders
- General purpose digital I/O pins
- Industrial standard communication interfaces(RS-232, RS-485, CAN BUS, ETHERNET) for Human Machine Interface(HMI)

1.2 DSC based control platform

A Digital Signal Controller (DSC) is a single chip microcomputer with a Digital Signal Processor (DSP) as core unit. With a DSP core, memory and peripherals (ADC,PWM modules,Timers,Capture,SPI,SCI,I2C,CAN modules) in one single chip, it is most effective for motor control solutions that require lots of math operations. So Texas Instruments TMS320F28335,a 32-bit floating point DSC is selected for the control platform development.

Hardware resources like adders, multipliers, shift registers, counters, memory are wired in such a way that users can make use of them to implement thier control algorithm. Users can write suitable software instructions to use this hardware to do suitable job. So the resources of the hardware are fixed and various control algorithms can be implemented using the same hardware. So the reconfigurability of control, which was not possible using analog controllers can be acheived using DSC.
The main advantages of using DSC are:

- Reconfigurability of control without changing hardware.
- Fewer components are used.
- Low sensitivity to temperature variations.

The disadvantages are:

- The hardware resources are fixed and it cannot be changed once the particular processor is selected.
- Design depends more on the hardware architecture of the processor.

1.3 FPGA based control platform

Field Programmable Gate Array has Logic Elements(LEs) as their building blocks. Each LE contains hardware resources such as gates, flipflops, decoder, counter. The hadware resources availble in Logic Elements are wired every time to realize required logic. Altera CYCLONE IV FPGA with 30K logic elements is selcted to build a control platform.

In FPGA the hardware is configurable which was not possible with DSC. Unlike processors, FPGAs use dedicated hardware for processing logic and do not have an operating system. Since FPGAs are truly parallel in nature, different processing operations do not have to compete for the same resources. As a result, the performance of one part of the application is not affected by adding another parallel processing part. The main advantages of using FPGA are:

- Reconfigurability of hardware.
- User is independent of the architecture of the device.

1.4 Organisation of Thesis

Chapter 2 presents the functional features of Texas Instruments digital signal controller TMS320F28335. It elaborates on the analog signal conditioning performed to match the requirements of the inbuilt ADC. It provides details about different interfaces and various communication protocols.

Chapter 3 describes the principle of scalar control of induction machine. It also discusses the hardware setup for implementing the V/f control of induction machine using the developed TMS320F28335 board.

Chapter 4 details the features of Altera Cyclone IV FPGA. It elaborates on different interfaces made with FPGA to suit motor control applications.

Chapter 5 discusses the conclusions and future scope of work.

CHAPTER 2

DESIGN AND DEVELOPMENT OF TMS320F28335 DSC BASED DIGITAL BOARD

2.1 Introduction

A generic control platform based on TMS320F28335 Digital Signal Controller (DSC) has been developed. This chip is a member of C2000 series of DSC's which was released by Texas Instruments recently. It has several advanced features compared to earlier C2000 series processors like F2812, F2806 etc. Therefore it is important to build a control platform with this processor which can be used for motor control and power processing applications that involve considerable amount of real time digital signal processing .

In this chapter, a fuctional overview of TMS320F28335 is discussed. The developed board has an analog interface, Digital to Analog Converter(DAC), JTAG debugger, 2Mb memory (SRAM) interface and communication interfaces (RS-232, RS-485, CAN bus). Each module is described in detail with experimental results.

2.2 C2000 Microcontrollers

C2000 series of DSP processors are designed for power electronics and precision-sensing applications. They have built-in peripherals like Pulse Width Modulation(PWM) modules, Capture modules, Quadrature Encoder Pulse(QEP) modules which are tailor made for drive applications. Older C2000 series DSP processors like F2812, F2806 have a fixed point architecture. TMS320F28335 is a new generation processor having a harware floating point support in addition to fixed point. Also TMS320F28335 supports more communication protocols like Inter Integrated Circuit(I2C), Controller Area Network (CAN) etc.

2.3 Overview of TMS320F28335

The block diagram TMS320F28335 DSC is shown in Fig. 2.1. A functional description of all the modules are discussed in this section.

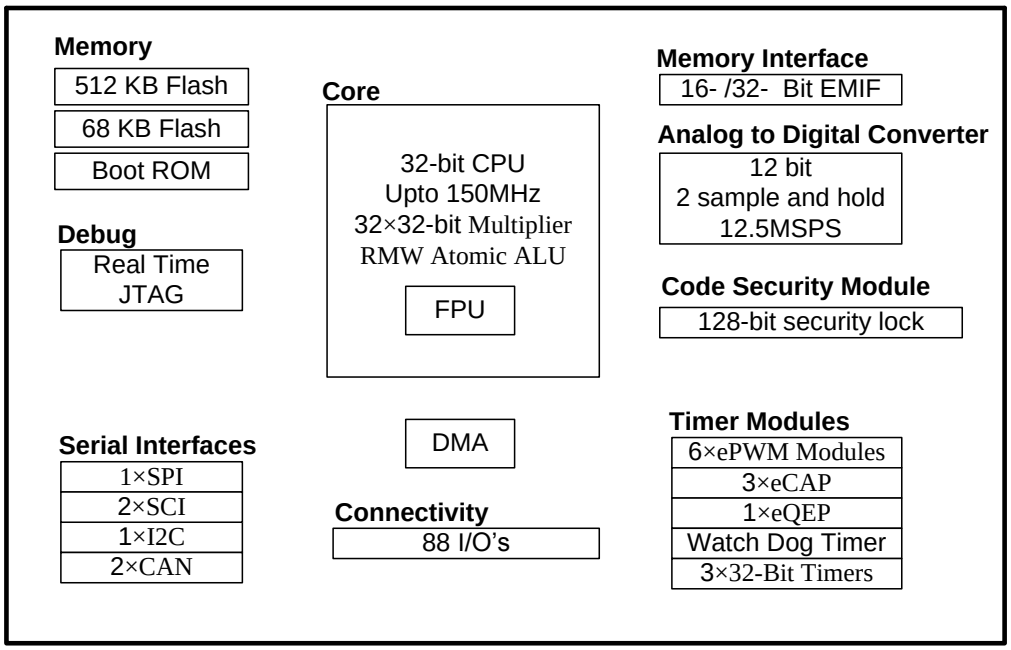

Fig. 2.1 F28335 Block Diagram

2.3.1 Core Details

TMS320F28335 has a 32-bit DSP core with single-precision (32-bit) IEEE 754 floating-point unit (FPU).It has a very efficient C/C++ engine, enabling users to develop their system control software in a high level language. It also enables math algorithms to be developed in C/C++ language. The 32 x 32-bit MAC has 64-bit processing capabilities that enables the controller to handle higher numerical resolution problems efficiently.

Multiple buses are used to move data between memory, peripherals and the CPU. TMS320F28335 memory bus architecture contains a program read bus, a data read bus and a data write bus. The Program read bus consists of 22 address lines and 32 data lines. The Data read and write bus consist of 32 address lines and 32 data lines each. The 32-bit-wide data bus enable single cycle 32-bit operations. The multiple bus architecture commonly known as Harvard Bus enables the processor to fetch an instruction, read a data value and write a data value in a single cycle.

2.3.2 Real-Time JTAG and Analysis

TMS320F28335 uses five of the standard IEEE 1149.1-1990, IEEE Standard Test Access Port and Boundary-Scan Architecture (JTAG) signals (TRST, TCK, TMS, TDI, and TDO) and two of the TI extensions (EMU0 and EMU1).Additionally, this device supports real-time mode of operation where the contents of memory, peripheral and register locations can be modified while the processor is executing code and servicing interrupts.

2.3.3 Memory Map

Fig. 2.2 depicts the memory map of TMS320F28335 processor. The Memory space of TMS320F28335 processor is divided into program space and data space. Memory space width is 16 bits. The Memory space contains independent sections of flash memory, single access RAM (SARAM), one time programmable memory (OTP) and boot ROM. The non-volatile internal memory consists of a group of FLASH-memory sections, a boot-ROM for up to 12 reset-startup options and a one-time-programmable (OTP) area.The volatile Memory is divided into 10 areas called M0, M1 and L0 to L7 that can be used both as code memory and data memory. PF0, PF1 and PF2 are Peripheral Frames that cover the control and status registers of all peripheral units. L0, L1, L2, and L3 memory spaces are dual mapped meaning the memory contents can be accessed with two different address. L0, L1, L2, L3, FLASH, ADC CAL and OTP are code security module protected. L4, L5, L6, L7, XINTF zone 0, zone 6 and zone 7 are Direct Memory Accesible(DMA) means data can be transferred between memory and periherals without the intervention of processor.

2.3.4 External Interface

An XINTF zone is a region in the TMS320F28335 memory map that can be directly connected to the external interface. This asynchronous interface consists of 20 address lines, 32 data lines, and three chip-select lines. The chip-select lines are mapped to three external zones namely XINTF zone 0, zone 6 and zone 7 . Each XINTF zone can be individually configured with unique read and write access timing. Also each zone

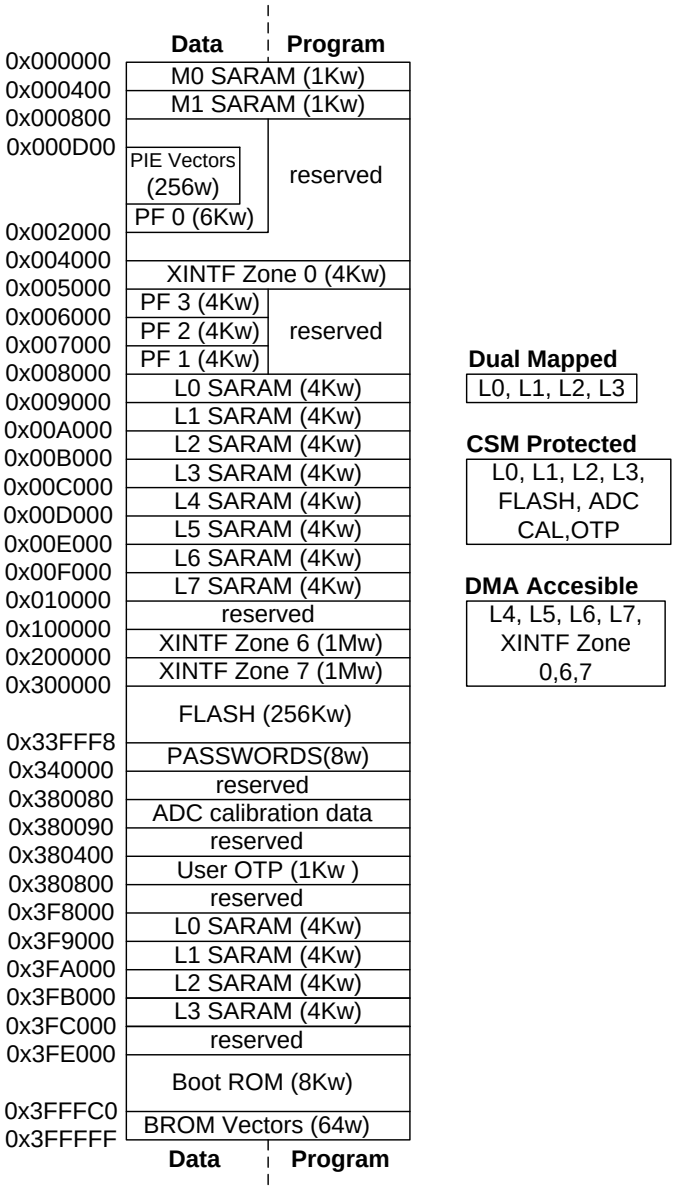

Fig. 2.2 TMS320F28335 Memory Map

has an associated zone chip-select signal that can be pulled low/high to enable/disable access to that zone.

Zone 0 uses external addresses 0x00000 - 0x00FFF. That is, an access to the first location in Zone 0 will issue external addresses 0x00000 along with chip select 0 ($\overline{\text{XZCS0}}$). An access to the last location in the zone will issue address 0x00FFF with $\overline{\text{XZCS0}}$. Zone 6 and Zone 7 both use external addresses 0x00000 - 0xFFFFF. The appropriate zone chip select signal ($\overline{\text{XZCS6}}$ or $\overline{\text{XZCS7}}$) should go low depending on which zone is to be accessed. The XINTF also supports Direct Memory Access (DMA) to its local (off-chip) program and data spaces with the help of $\overline{\text{XHOLD}}$ and $\overline{\text{XHOLDA}}$ lines.

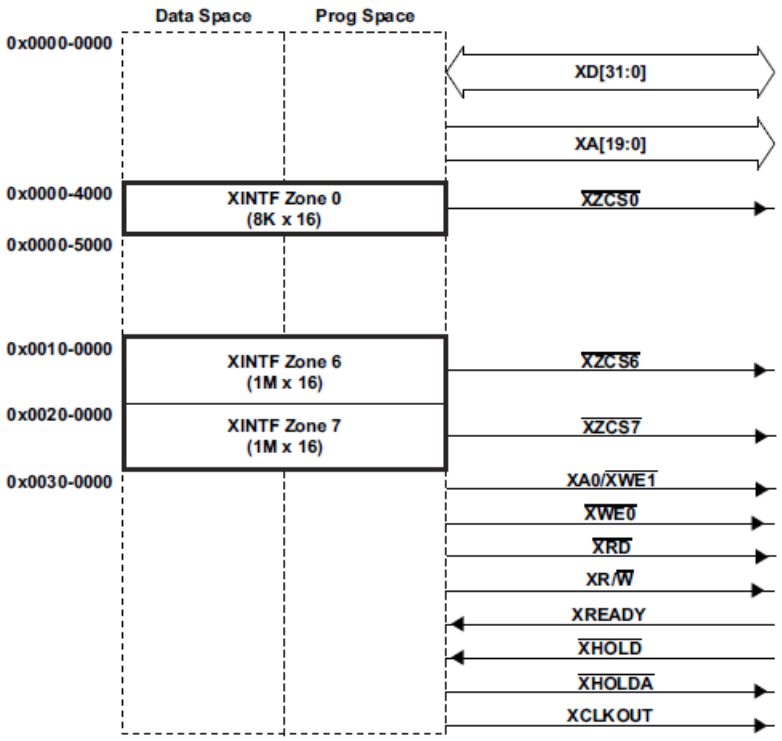

Fig. 2.3 TMS320F28335 External interface Block Diagram

2.3.5 Code Security Module

Code security module (CSM) is a security feature used to protect the FLASH/OTP and the L0/L1/L2/L3 SARAM blocks. This security feature prevents unauthorized users from examining the memory contents via the JTAG port, executing code from external memory or trying to boot-load some undesirable software that would export the secure memory contents. The user must write the correct 128-bit KEY value, which matches the value stored in the password locations within the FLASH to enable access to the secure blocks .

2.3.6 Boot ROM

The Boot ROM is factory-programmed memory space with boot-loading software. Boot-mode signals instructs the bootloader software what boot mode to use during power up. The user can select to boot normally or to download new software from an external connection or to select boot software that is programmed in the internal Flash/ROM. The Boot ROM also contains standard tables, such as sin/cos waveforms, for use in math related algorithms.

The boot loader provides a variety of different ways to download code to accommodate different system requirements. It uses various GPIO signals XA15(GPIO87), XA14(GPIO86), XA13(GPIO85), and XA12(GPIO84) to determine which boot mode to use. Fig. 2.4 shows various types of booting methods.

MODE	GPIO 87	GPIO 86	GPIO 85	GPIO 84	BOOT MODE	
F	1	1	1	1	Jump to Flash	
E	1	1	1	0	SCI-A boot	
D	1	1	0	1	SPI-A boot	
C	1	0	0	0	I2C boot	
B	1	0	0	1	eCAN-A boot	
A	1	0	1	0	McBSP-A boot	
9	1	0	0	0	Jump to XINTF×16	
8	1	0	0	0	Jump to XINTF×32	
7	0	1	1	1	Jump to OTP	
6	0	1	1	0	Parallel GPIO boot	
5	0	1	0	1	Parallel XINTF boot	
4	0	1	0	0	Jump to SARAM	
3	0	0	1	1	Branch to check Boot mode	
2	0	0	1	0	Branch to Flash	Skip ADC Cal
1	0	0	0	1	Branch to SARAM	
0	0	0	0	0	Branch to SCI	

Fig. 2.4 TMS320F28335 Boot Mode Selection

Boot modes 0, 1, and 2 bypass the ADC calibration function call. These boot modes are for TI debug only. The built-in ADC on TMS320F28335 needs to be calibrated before loading program code to prevent malfunctioning of ADC. Therefore in all boot modes by except 0,1 and 2 ADC calibration routine will be executed after boot initialization. Boot mode 3 is for Debug purpose only. Boot mode 4,7,8,9 and F do not call a boot loader. Instead, they jump to a predefined location in the memory. Remaining Boot modes 5, 6, A, B, C, D and E call a boot load routine that loads a data stream from the peripheral into memory. The booting process is shown in Fig. 2.5. On reset, boot loader determines the code entry point based on the status of GPIO 87, GPIO 86, GPIO 85 and GPIO 84.

2.3.7 General-Purpose Input/Output (GPIO) Multiplexer

TMS320F28335 DSC contains total 88 I/O-pins. Most of the GPIO pins are multiplexed. This means that a single physical pin of the device can be used for up to 4 different functions and it is up to the programmer to decide which function to select.

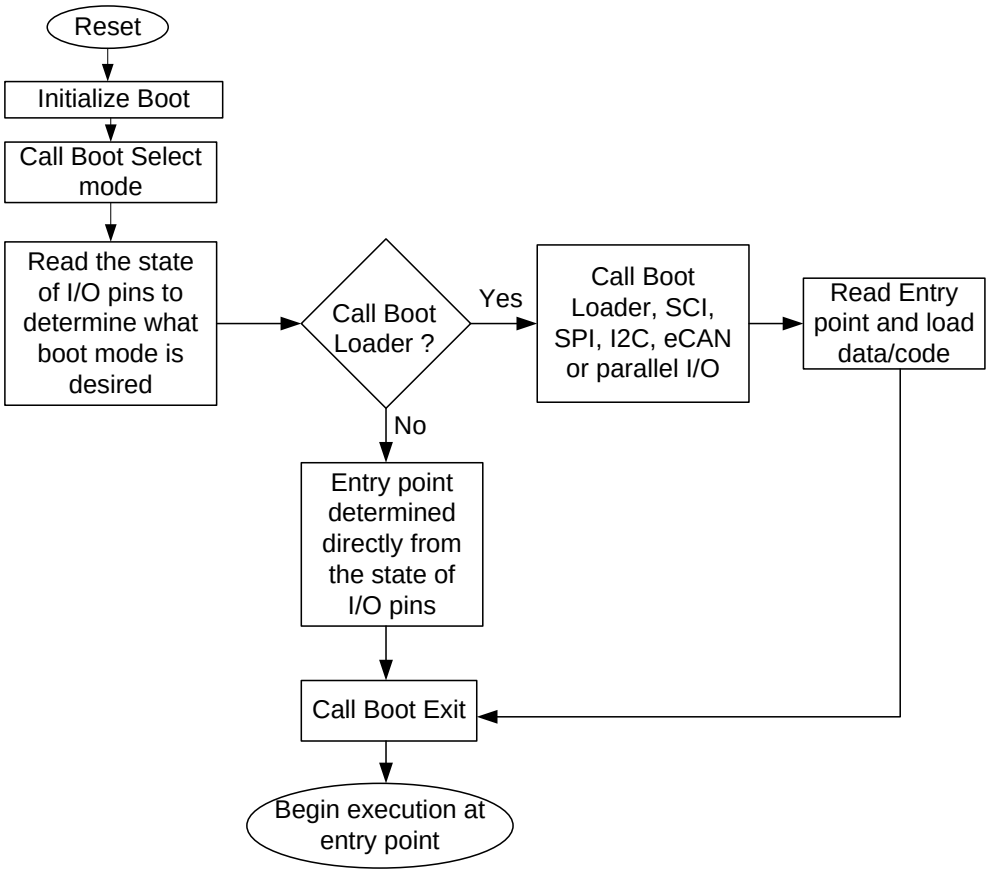

Fig. 2.5 TMS320F28335 Boot ROM Function Overview

2.3.8 Oscillator and PLL

The device can be clocked by an external oscillator or by a crystal attached to the on-chip oscillator circuit. A PLL is provided that supports upto 10 input clock scaling ratios. The PLL ratios can be changed on-the-fly in software.This is implemented by programming the PLL control register (PLLCR). High-speed Clock Pre-scaler (HISPCP) and Low speed Clock Pre-scaler (LOSPCP) are used as additional clock dividers. The outputs of the two pre-scalers are used as the clock source for the peripheral units. The two pre-scalers can be set individually and independently.

2.3.9 Watchdog

TMS320F28335 DSC contain a watchdog timer. The user software must regularly reset the watchdog counter within a certain time frame. otherwise, the watchdog will generate a reset to the processor. The watchdog can be disabled if necessary. In a real

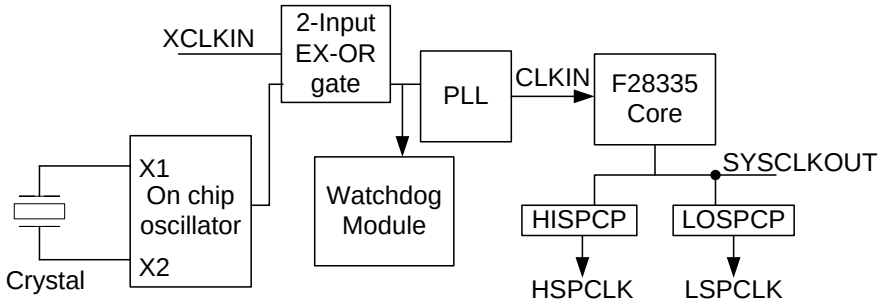

Fig. 2.6 TMS320F28335 Clock Module

time project a watchdog should always be enabled to take a necessary action whenever a software or hardware failure occurs.

2.3.10 32-Bit CPU Timers(0, 1, 2)

CPU timers 0, 1, and 2 are identical 32-bit timers with presettable periods and with 16-bit clock prescaling. The timers have a 32-bit count down register, which generates an interrupt when the counter reaches to zero value. The clock input to the timers are obtained from the SYSCLKOUT by suitable prescalers. When the counter reaches zero, it is automatically reloaded with a 32-bit period value.

2.3.11 ADC Module

TMS320F28335 processor has a built in ADC Module.The ADC module consists of a 12-bit ADC two builtin sample andhold (S/H) circuits. Fig. 2.7 shows the block diagram of ADC module present in TMS320F28335.

The features of the ADC module are listed below :

- 12-bit ADC core with two built in S/H
- Analog input: 0.0 V to 3.0 V (Voltages above 3.0 V produce full-scale conversion results.)
- Fast conversion rate: Up to 80 ns at 25-MHz ADC clock, 12.5 MSPS
- 16 dedicated ADC channels. 8 channels multiplexed per Sample/Hold
- Autosequencing capability provides up to 16 "autoconversions" in a single session. Each conversion can be programmed to select any 1 of 16 input channels

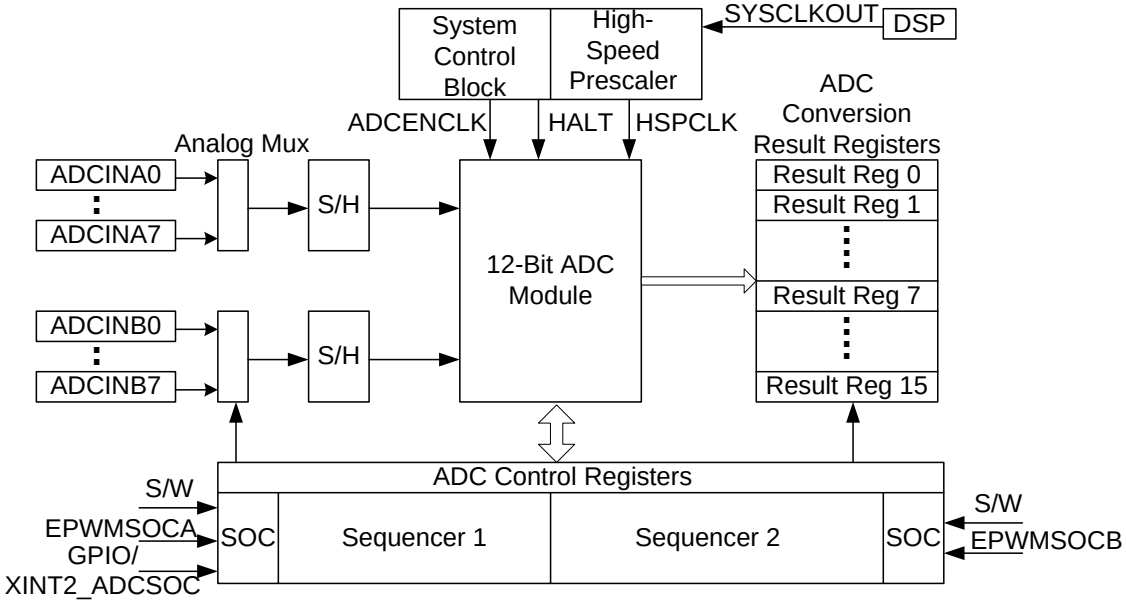

Fig. 2.7 TMS320F28335 ADC Module Block Diagram

- Sequencer can be operated as two independent 8-state sequencers or as one large 16-state sequencer (that is, two cascaded 8-state sequencers)
- Sixteen result registers (individually addressable) to store conversion values
  - The digital value of the input analog voltage is derived by:

$$\begin{array}{ll} DigitalValue = 0, & when\ input \leq 0V \\ DigitalValue = 4096 * \frac{(InputAnlalogVoltage - ADCLO)}{3}, & when\ 0V < input < 3V \\ DigitalValue = 4095, & when\ input \geq 3V \end{array}$$

- Multiple trigger sources for the start-of-conversion (SOC) sequence
  - S/W - software immediate start
  - ePWM 1-6
  - GPIO XINT2
- Flexible interrupt control allows interrupt request on every end-of-sequence (EOS) or every other EOS
- Sequencer can operate in "start/stop" mode, allowing multiple "time-sequenced triggers" to synchronize conversions.
- Sample-and-hold (S/H) acquisition time window with separate prescale control.

2.3.12 ePWM Module

TMS320F28335 processor has six independent enhanced PWM (ePWM) modules. The enhanced PWM peripheral means that it can generate complex PWM waveform with the use of minimum CPU resources. Each ePWM module has two output channels. Each

ePWM module consists of seven submodules. They are time-base(TB) submodule, counter-compare(CC) submodule, action-qualifier(AQ) submodule, dead-band generator(DB) submodule, PWM-chopper(PC) submodule,trip-zone(TZ) submodule and event-trigger (ET) submodule. The complete structure of a single ePWM module with each submodule and the signal connections between its subsections included is shown in Fig. 2.8

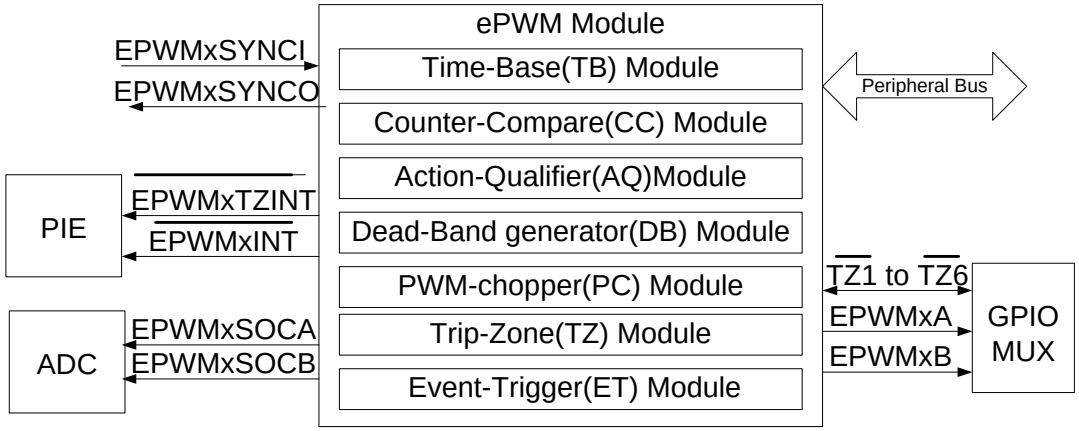

Fig. 2.8 TMS320F28335 ePWM Module Block Diagram

The main signals used by the ePWM module are:

- PWM output signals (EPWMxA and EPWMxB)
- Trip-zone signals (TZ1 to TZ6).
- Time-base synchronization input (EPWMxSYNCI) and output (EPWMxSYNCO) signals.
- ADC start-of-conversion signals (EPWMxSOCA and EPWMxSOCB).
- Peripheral Bus

2.4 Board Design

Fig.2.9 shows the block diagram of TMS320F28335 based control platform. All the peripherals of TMS320F28335 described in the previous section are essential for power electronic control. They are brought outside the board with appropriate electronic interface.

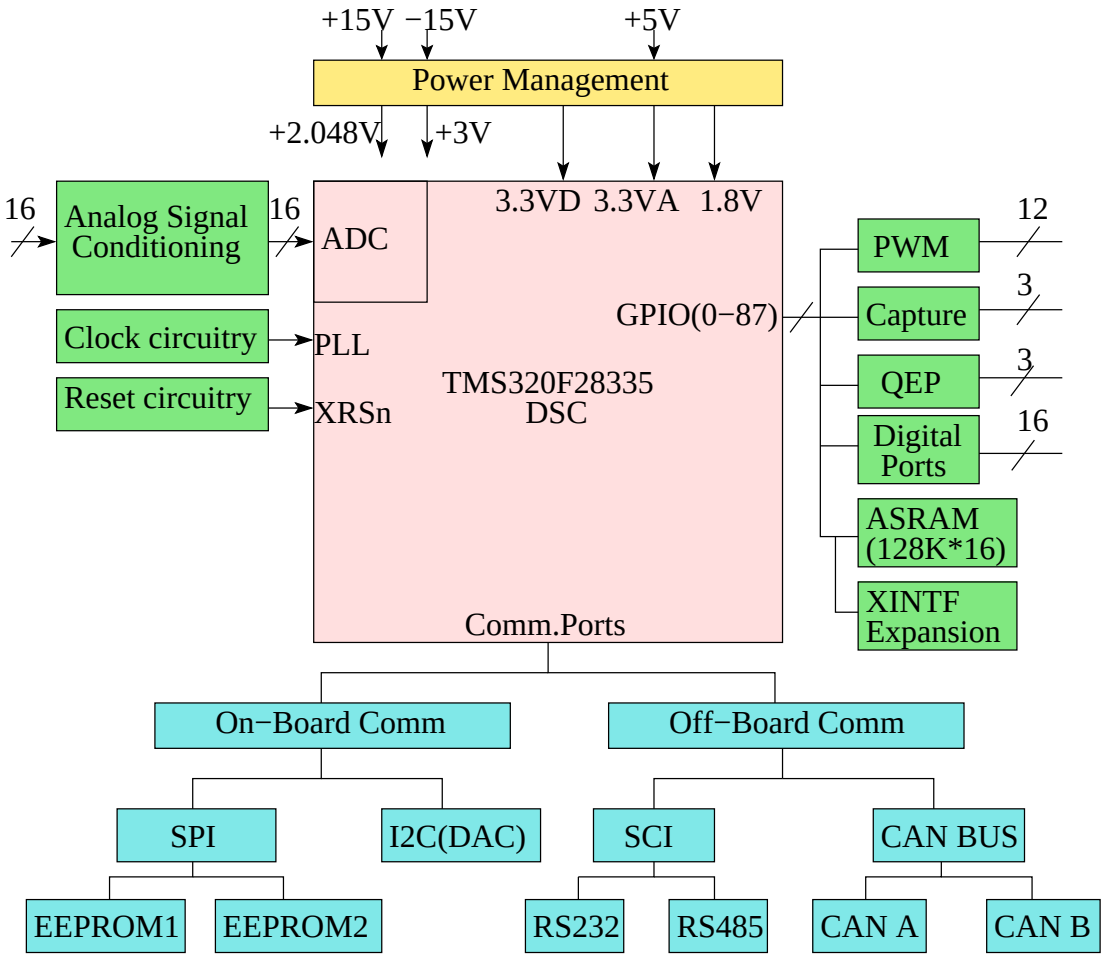

Fig. 2.9 Block Diagram of TMS320F28335 based Digital board

Interface circuitry is provided for the following peripherals:

- Analog signal conditioning
- JTAG debug interface
- Incremental encoder interface (RS-422 Standard)
- Pulse Width Modulated outputs
- EEPROM(serial peripheral interface)
- Quad 12-bit Digital to Analog Converter (I2C interface)
- RS-232, RS-485 serial communication interface
- CAN bus communication interface
- Digital I/O ports, LEDs and slide switchs
- 2Mb Asynchronous SRAM Interface
- Expansion header for external peripheral interface

2.4.1 Power Management

TMS320F28335 based digital board requires external +15V, -15V and +5V. F28335 requires 1.9V for core operation at 150MHz , 3.3V for input and output operations. All the different voltages required by DSC are derived on board using Low Drop Out (LDO)regulator TPS767D301. The ADC in TMS320F28335 has an internal reference voltage with a temperature stability of 50ppm/^{o}C. An optional external reference voltage of 2.048 V is provided to have good ADC accuracy over a wide temperature range by using REF3120. It has a better temperature stability of 25ppm/^{o}C.

2.4.2 Analog signal conditioning

TMS320F28335 has an internal ADC which can accept 16 analog inputs with (0-3) V range. But the analog signals in real world are bipolar. They are to be conditioned to unipolar voltage. The Industrial standard output voltage levels of transducer box is $\pm 10V$. So it is attenuated and level shifted using a single low offset, high precision op-amp OPA2228U from Texas Instruments.

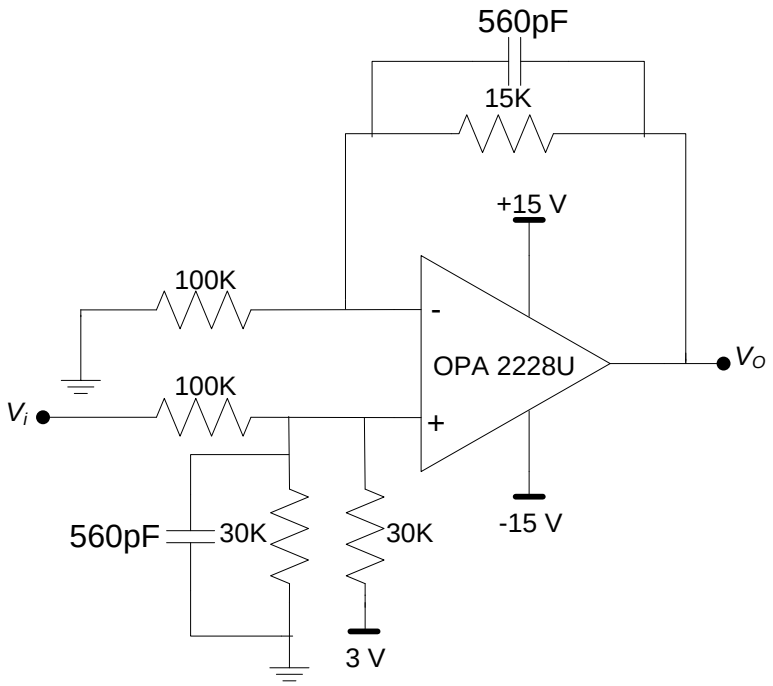

Fig. 2.10 Analog signal conditioning circuit

Fig. 2.10 depicts the analog signal conditioning circuit used in the board. V_i is the

analog input voltage to the board which is bipolar in nature and V_o is the output voltage after signal conditioning which is fed to the ADC input terminals. Using superposition theorem, The output voltage V_O can be expressed by the following equation.

$$V_O = 0.15V_i + 1.5 \tag{2.1}$$

The capacitor of 560pF provided across the 30K and 15K resistors helps to attenuate differential mode noise appeared in V_i.

Simulation results: The circuit is simulated by using the spice file of the op amp OPA2228U and is simulated using TINA software. With an input voltage of 10V peak sine wave, the output is a sinewave with peak 1.5V superimposed on a DC level of 1.5V. Fig. 2.11 shows the simulation results.

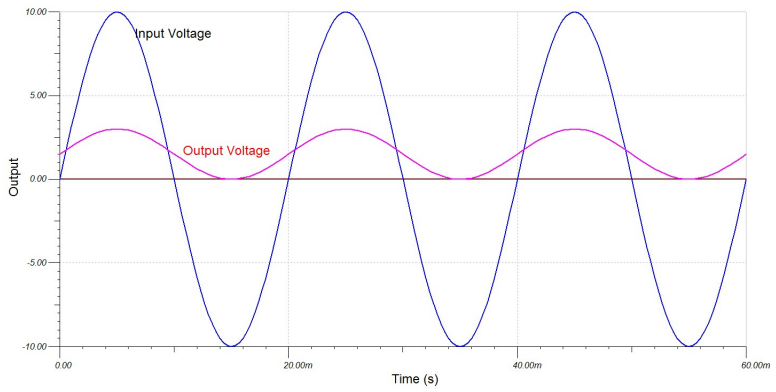

Fig. 2.11 Simulation Result of Analog Signal Conditioning

2.4.3 Incremental encoder interface

An incremental encoder is used to get position, direction, and speed information from a rotating machine. The quadrature encoder outputs two signals which are phase displaced by 90 degrees and an index pulse that is used to indicate absolute position. The power supply for the encoder is provided from the onboard connector. Typically the encoder gives out the information in RS-422 Standard. Differential receiver AM26LV32C is used to acquire single ended quadrature encoder information .The single ended quadrature signals are fed to eQEP module of TMS320F28335. Typical quadrature encoder signals are shown in Fig. 2.12.

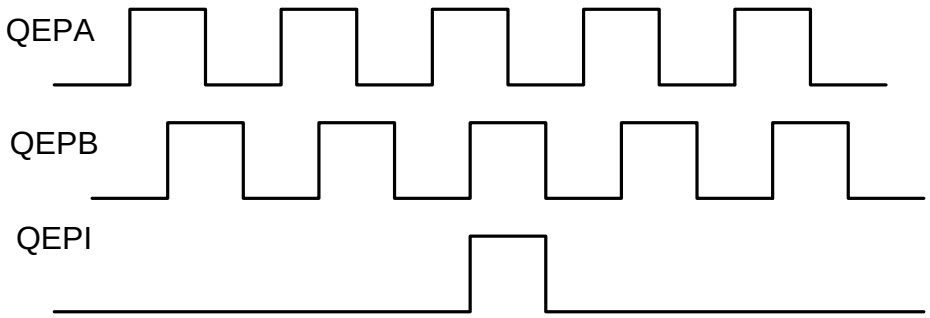

Fig. 2.12 Typical Quadrature Encoder Output Signals

2.4.4 Pulse Width Modulated outputs

Maximum 12 PWM's can be generated from the ePWM module of TMS320F28335 and they are level shifted to 5V with 24 mA output drive capability. The buffer used is SN74ALVC164245.

2.4.5 Serial Peripheral Interface

The SPI module is a synchronous serial I/O port that shifts a serial bit stream of variable length and data rate between the TMS320F28335 and other peripheral devices. Here "synchronous" means that the data transmission is synchronized with a clock signal. During data transfers, one SPI device must be configured as the transfer MASTER, and all other devices configured as SLAVES. The standard SPI has four signals. They are

- SPISTE (SPI Serial Transmit Enable)
- SPIMOSI(SPI Master Output Slave Input)
- SPISOMI(SPI Slave Output Master Input)
- SPICLK (SPI Clock)

The protocol is shown in Fig. 2.13. SPI protocol is basically a programmable shift register. Data is shifted in and out of the shift register. When data is to be transmitted from master to slave, first the data is written into master shift register and then it is shifted into slave shift register using SPIMOSI pin synchronously. Similarly, when slave shifts the data out of its shift register using SPISOMI pin, master shift register accepts the data. Also SPI supports full duplex communication with transmission rates upto 1Mbps.

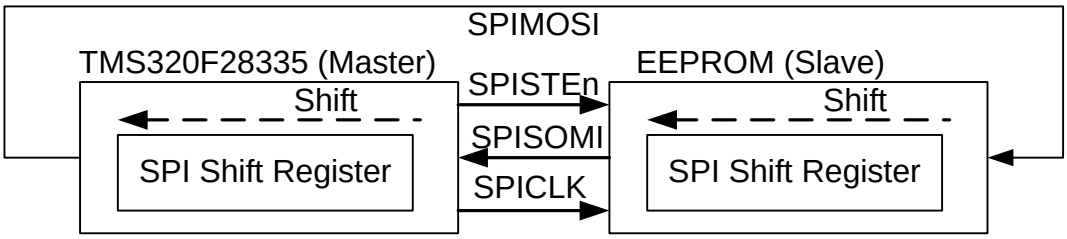

Fig. 2.13 SPI Data Flow

TMS320F28335 has one serial peripheral interface (SPI) module (SPI-A). Using that two EEPROM's are interfaced with DSC, with only one EEPROM being active at a time. Chip select is demultiplexed using a 1:2 decoder. Each EEPROM has 512 Kb memory that can be used with or without write protection.

2.4.6 I2C interface

I2C is a serial communication that uses only two lines for communication namely serial data pin (SDA) and serial clock pin (SCL). The SDA and SCL pins both are bidirectional. They are connected to a positive 3.3 V supply voltage using pull-up resistors. When there is no data transmission on the bus, both pins are high. Each device connected to an I2C bus is identified by a unique address. It can operate as either a transmitter or a receiver, depending on the function of the device. A device connected to the I2C bus can either be considered as the master or the slave when performing data transfers. A master device that initiates a data transfer on the bus and generates the clock signals to permit that transfer. During this transfer, any device addressed by this master is considered as a slave.

DAC AD5625R is interfaced using Inter-Integrated Circuit (I2C) Module of TMS320F28335. The selected DAC can operate at high speeds of 3.25Mbps but I2C module on the processor restricts the data rate to 400kbps which limits the frequency of the signal to be monitored to 1KHz. The features of this DAC are as follows:

- Quad 12 bit DAC core
- Settling time of 3μs
- Internal Reference voltage
- Unipolar output voltage

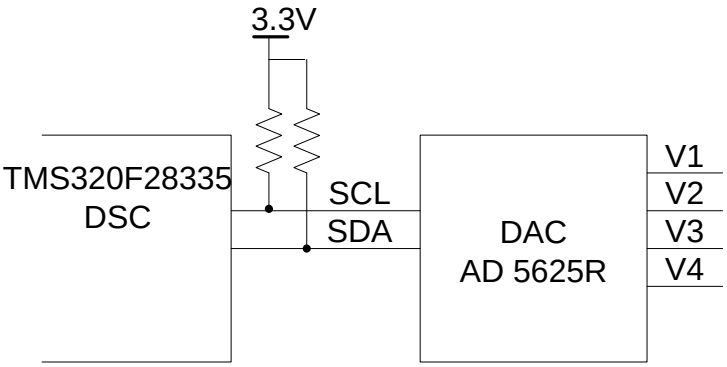

Fig. 2.14 DAC interface with TMS320F28335

The unipolar output of DAC is given by

$$V_1 = (3.3 \times \frac{D}{4096}) \tag{2.1}$$

The DAC output voltage should be level shifted and amplified so that the analog voltage is buffered to -10V to +10V range. The circuit used for amplification and level shifting is shown in Fig. 2.15.

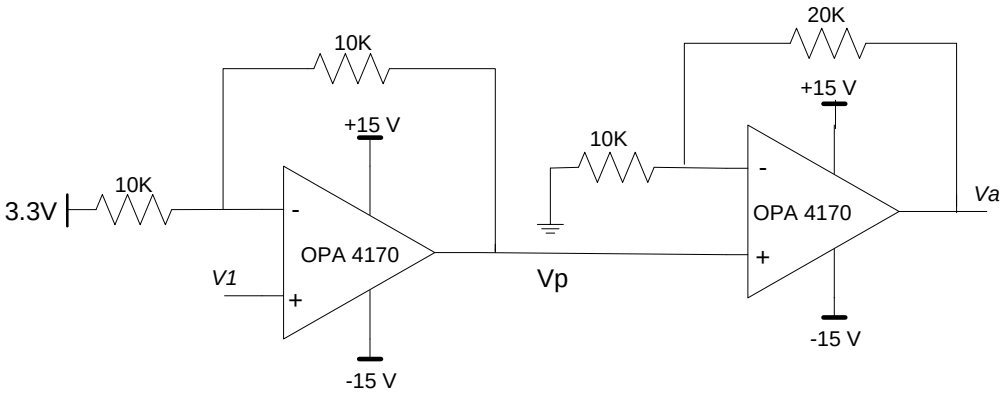

Fig. 2.15 DAC output signal conditioning circuit

Using virtual ground concept,

$$(\frac{3.3 - V_1}{10K}) + (\frac{V_p - V_1}{10K}) = 0 \tag{2.2}$$

Solving the above equation we get

$$V_p = 2V_1 - 3.3 \tag{2.3}$$

Solving the next stage opamp

$$V_a = 3 \times V_p = 6V_1 - 9.9 \tag{2.4}$$

Substituting 2.1 in 2.4, We get

$$V_a = (9.9 \times \frac{D}{2048}) - 10 \tag{2.5}$$

So Output Voltage V_O for any input code is calculated using:

$$V_O \cong (10 \times \frac{D}{2048}) - 10 \tag{2.6}$$

where D is decimal equivalent of 12-bit data.

2.4.7 Digital I/O ports, LEDs and slide switchs

Ten digital ports are used as input or output ports. Three Leds and three slide switches are also interfaced for debugging purpose.Also capture pins are brought out, which can be used for low speed measurements.

2.4.8 External Memory interface

An asynchronous SRAM of 128K*16 (2Mb) is interfaced with zone 7 of external memory interface space. The connections between TMS320F28335 and SRAM are shown in Fig. 2.16

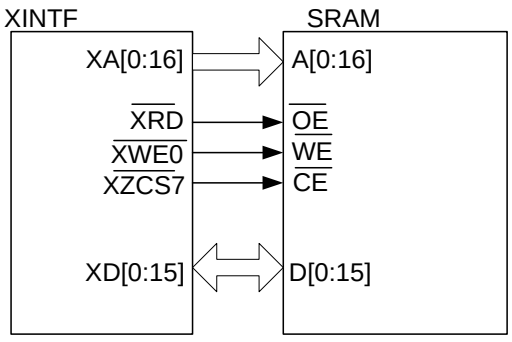

Fig. 2.16 Connection between TMS320F28335 and SRAM

2.4.9 Clock Circuitry

TMS320F28335 has an internal oscillator which is connected with an external crystal. The typical crystal circuit is shown in Fig. 2.6. Fig. 2.17 shows the external circuitry and connections required for using the internal oscillator. A crystal having a CLOAD of around 12 pF is selected so C1 and C2 are choosen as 24 pF.

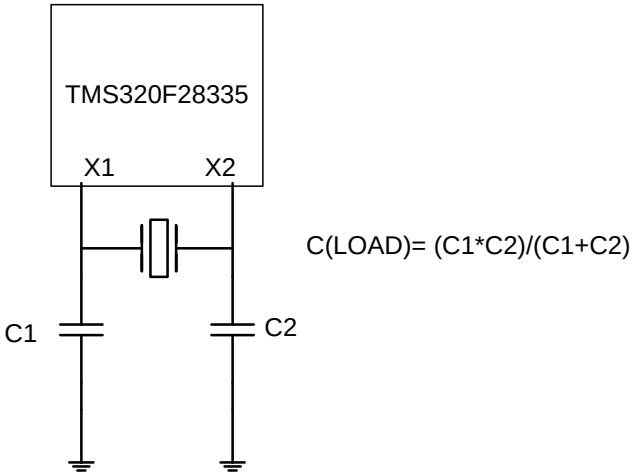

Fig. 2.17 Typical Crystal Circuit

2.4.10 Reset Circuitry

Linear drop out regulator TPS767D301 is used to obtain core voltage(1.9V) and I/O voltage(3.3V) for TMS320F28335. It pulses a reset signal when supply has not reached 95 percent of rated value. The processor should be in reset state if it is not powered properly. A provision for manual reset using a push button is also provided. Fig. 2.18 shows the block diagram of the reset circuitry. Power supply reset and manual reset are logically ANDed and connected to processor XRSn (Reset) pin.

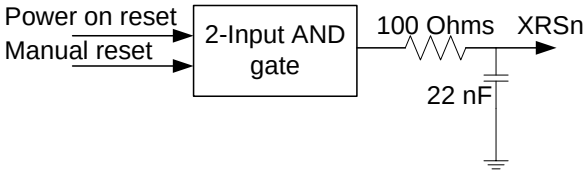

Fig. 2.18 Reset Circuitry for TMS320F28335

2.4.11 JTAG Debug Circuitry

JTAG is the acronym for Joint Test Action Group, the name of the group of people who developed the IEEE 1149.1 standard. With the advent of VLSI, the chips are becoming more compact in packaging. So if test points are to be provided for all pins, PCB will become a bed of nails. So JTAG has developed a technology where in the status of all pins can be read by serially passing a test data in one pin(TDI) and data serially shifted out through all I/O's. So the test data along with all the status of I/O's can be obtained at other pin(TDO). Since it is a serial communication standard a test clock (TCK) is provided. A signal named TRSTn asserting low will initiate start of JTAG process. Apart from real time debug, JTAG is also used for programming TMS320F28335. TMS320F28335 has IEEE Standard Test Access Port and Boundary-Scan Architecture (JTAG) signals (TRST,TCK, TMS, TDI, and TDO) and two of the TI extensions (EMU0 and EMU1). Fig. 2.19 shows the block diagram of the on-board emulator XDS100V2 used in the designed board.

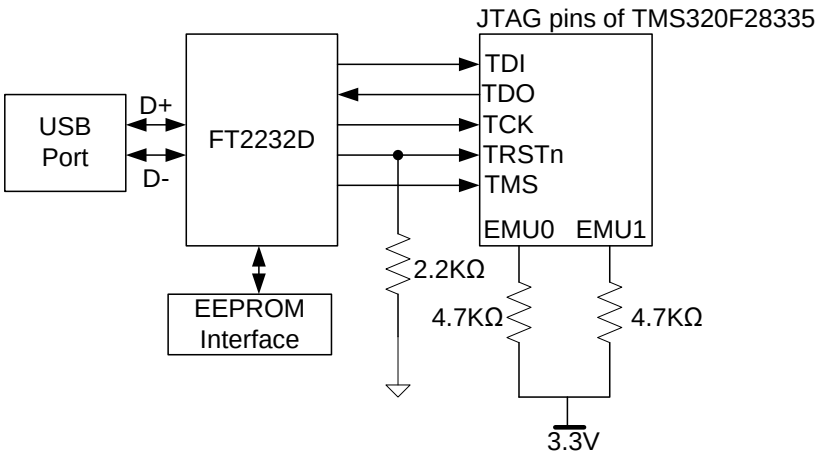

Fig. 2.19 Block Diagram of On-Board JTAG Interface

In Fig. 2.19, USB differential signals D+, D- is converted to JTAG signals by FT2232D which is a dual USB to serial converter. On power up, FT2232D scans the contents of EEPROM attached to it and defines the mode of operation of FT2232D based on the data read from EEPROM. First time after the board is developed and powered on, USB FT2232 will be recognised as a composite device which means that FT2232D is operating as serial device because of the EEPROM being empty. The EEPROM is programmed such that FT2232 acts like a USB to JTAG converter. EEPROM should be

programmed using MProg utility which is provided by FTDI. The programming fields for EEPROM should look like Fig. 2.20. After programming the eeprom with the con-

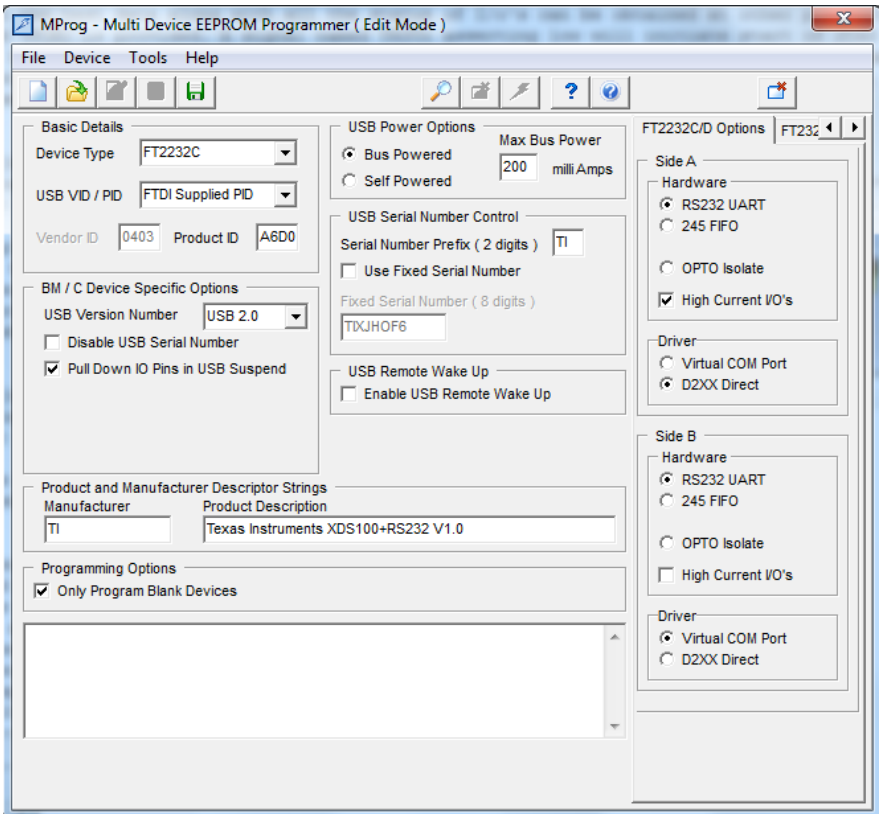

Fig. 2.20 Programming EEPROM using Mprog Utility

tents shown in Fig. 2.20, USB is recognised as TI XDS100 Channel A and Channel B which suggests that it is ready to be used as on-board emulator.

2.4.12 RS-232 Serial Communication Interface

RS-232 is mainly used for serial communication between a computer and peripherals. It supports full-duplex asynchronous communication i.e., bidirectional data flow at the same time. This protocol is used only for short distance communication. Fig. 2.21 shows the RS-232 communication between developed board and computer. The RS-232 transmit data signal from the developed board is level shifted and connected to the receive pin of serial port. Similarly, the board receive data signal after level shifting is connected to transmit pin of serial port. The bit rate is programmable to over 65000 different speeds through a 16-bit baud select register. RS-232 also uses parity check and and overrun on the recieved data for integrity.

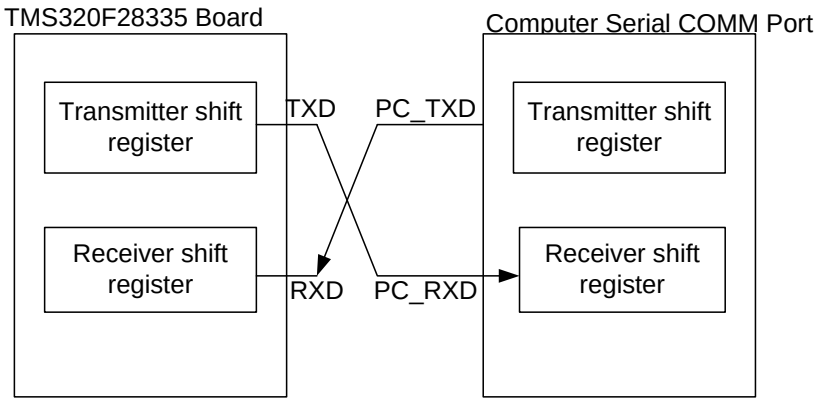

Fig. 2.21 RS-232 Communication between TMS320F28335 and Computer

An electrical interface is required to match the signal levels of TMS320F28335 and PC serial port. The board uses TRSF3221E transceiver and a 9-pin DB9 connector for RS-232 communications. The high level driver output is +5V and low level driver output is -5V. The reciever high and low level inputs are +10 and -10V. The TRSF3221E operates at data signaling rates up to 1 Mbit/s. But the processor restricts the data rate to a maximum of 400Kbit/s.

2.4.13 RS-485 Serial Communication Interface

The RS-485 standard specifies differential signaling on two lines rather than single-ended with a voltage referenced to ground. A logic 1 is a level greater than Ű200 mV, and a logic 0 is a level greater than +200 mV. Typical line voltage levels from the line drivers are a minimum of $\pm$1.5 V to a maximum of about $\pm$ V. Receiver input sensitivity is $\pm$200 mV. Noise in the range of $\pm$200 mV is essentially blocked. The differential format produces effective common-mode noise cancellation. In this board fully isolated RS-485 interface i.e., both data and power isolation is done using ADM2587E. The RS-485 protocol remains same as that of RS-232. The only difference is differential signalling is used in RS-485 compared to single ended transmission in RS-232.

2.4.14 CAN Bus Interface

Controller Area Network is a vehicle bus standard designed to allow microcontrollers and devices to communicate with each other within a vehicle without a host computer. CAN bus is a message-based protocol, designed specifically for automotive applications

but now also used in other areas such as aerospace, maritime, industrial automation and medical equipment.The controller area network (CAN) uses a serial multimaster communication protocol that efficiently supports distributed real-time control, with a very high level of security and communication rates upto 1Mbps. Fig. 2.22 shows typical CAN bus connection.

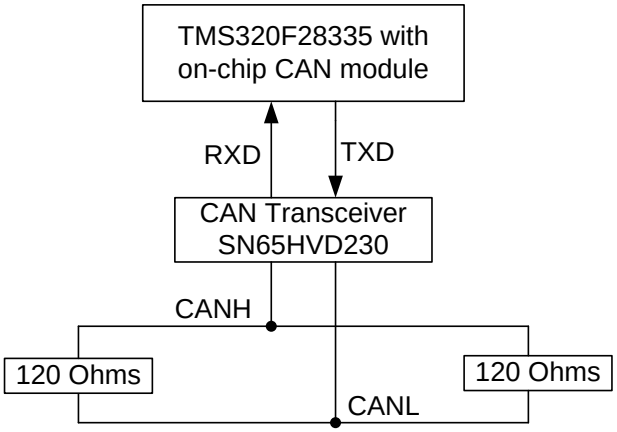

Fig. 2.22 Block diagram of CAN bus.

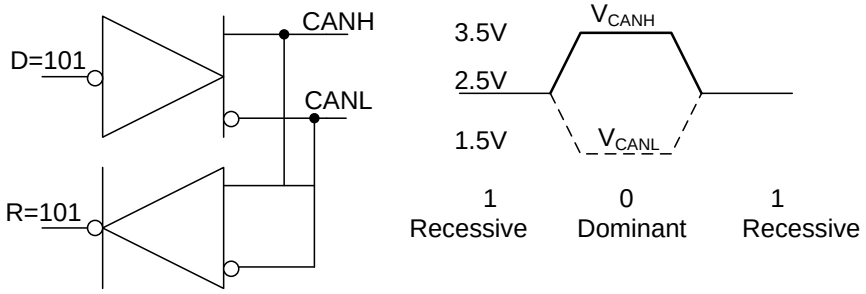

Fig. 2.23 CAN controller and typical CAN levels

Two CAN modules are brought out using CAN controllers. The CAN controllers used on the board is SN65HVD235. These transceivers interface the single-ended CAN controller with the differential CAN bus signals CANH and CANL. The CAN bus termination is done using 120 Ohms resistor. Other devices CANH and CANL can be connected to the bus for communication.The CAN controller driver and receiver circuit diagram and typical CAN bus levels are shown in Fig. 2.23. When the CAN bus is active it is said to be in 'dominant' state otherwise it is said to be in 'recessive' state.

2.5 Testing of the developed board

A 4-Layer PCB is fabricated using the design explained in the above section. Fig. 2.24 is the photograph of developed board showing various interfaces. The developed board is tested. Programming of the board is done using Code Composer Studio(CCS) version 4.4 and the onboard emulator.

2.5.1 Testing of Analog Interfaces

The developed TMS320F28335 board has analog signal conditioning circuitry for ADC input as well as DAC output. In order to ensure the working of all analog sections including ADC and DAC, a simple experiment is conducted. The block diagram of the carried out experiment is shown in Fig. 2.25.

An analog signal is applied to signal conditioning circuit of ADC. The conversion results are sent to DAC AD5625R using I2C protocol. The output signal is conditioned so that the same signal should be reconstructed at the output of DAC signal conditioning circuit. The conditioned signal is converted into 12-bit digital values.

The conversion results are simultaneously sent out to the DAC using I2C protocol. To send a single sample, first the DAC operation code is to be sent, followed by the channel code and the 12 bit data. So for sending 12 bits of data to the DAC roughly 40 bits are being used. The typical activity on I2C bus while data is transmitted to DAC is shown in Fig. 2.27.

A sinusoidal signal of 2.5V peak, 50 Hz is given as input to signal conditioning circuit of ADC. According to equation 2.1 the output voltage should be a sinusoidal signal of 375mV peak and dc level of 1.5V. Fig. 2.26 shows the experimental result after the signal conditioning circuit of the ADC.

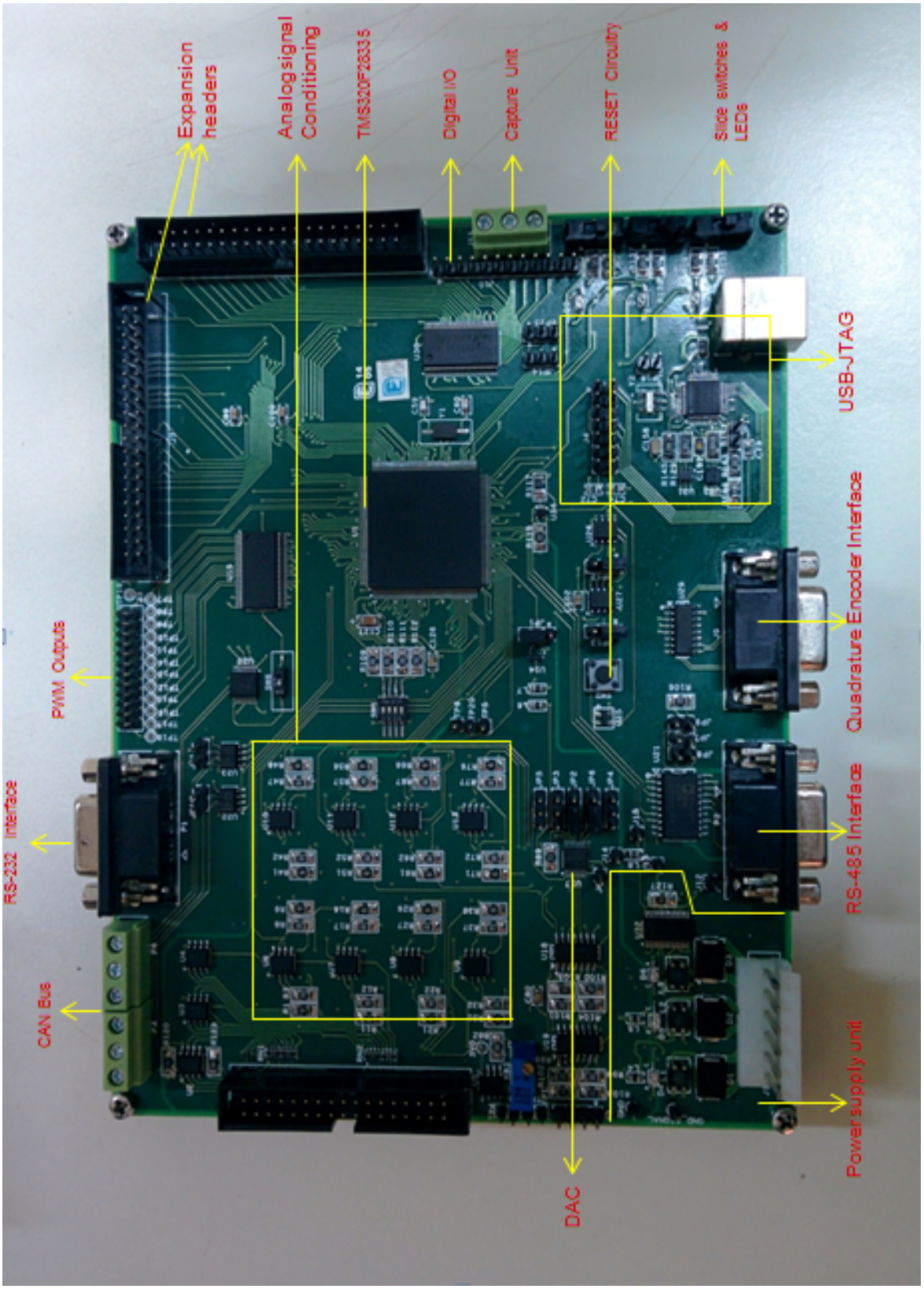

Fig. 2.24 Developed TMS320F28335 based Digital Board

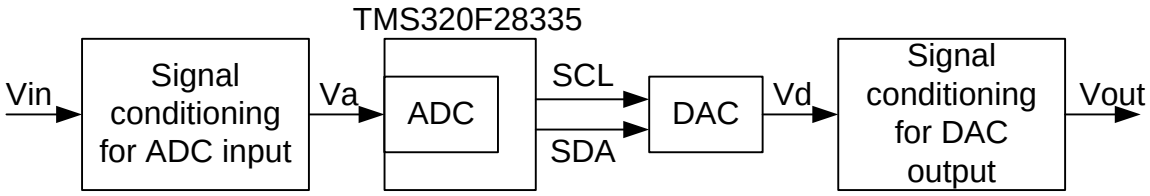

Fig. 2.25 Block Diagram for Testing Analog Interfaces

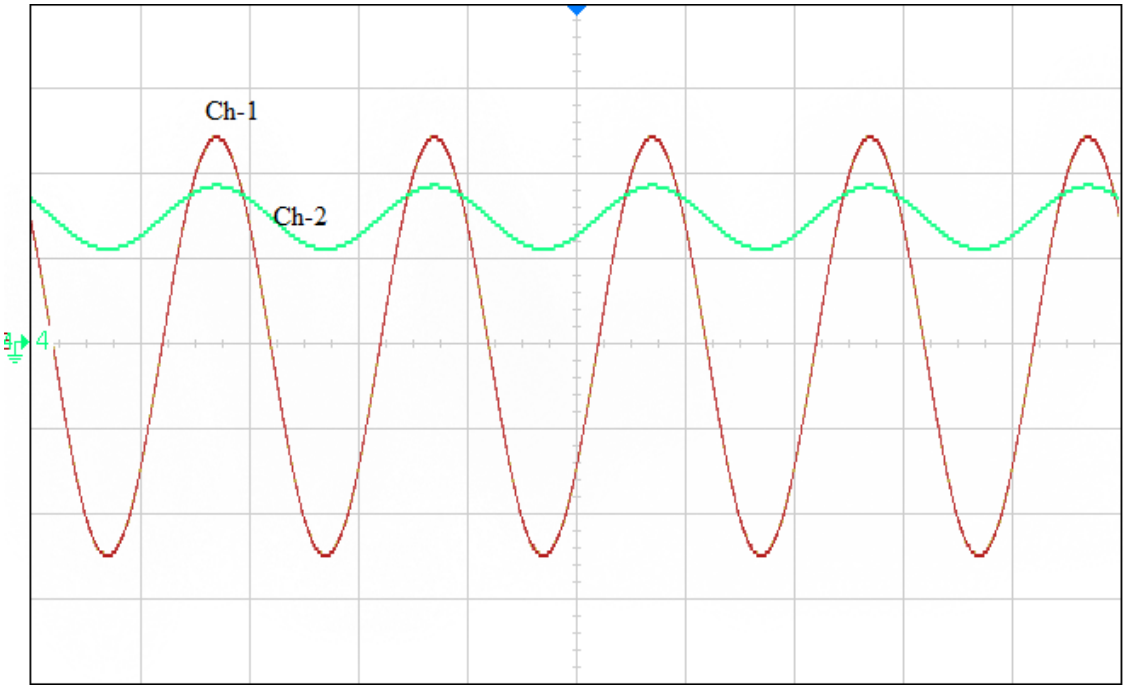

Fig. 2.26 Performance of Analog Signal conditioning Circuit for ADC
$(Ch1 : Vin, Ch2 : Va, X - axis : 10ms/div, Y - axis : 1V/div)$

The output voltage of DAC is based on equation 2.1. The unipolar DAC output Vd is shown in the Fig. 2.28.

The unipolar DAC output Vd, is buffered to 10 V range using OPA4170. Fig. 2.29 shows the analog input voltage Vin and the DAC output voltage Vout after signal conditioning. It can be observed that both the signals are same.

The performance of the test setup at different frequencies is asserted. Analog signal frequency is varied from 50Hz to 28KHz, and at different instances Vin and Vout waveforms are captured. Since the DAC speeds are limited to 400kbps, analog signals with more than 1KHz could not be reconstructed properly. Aliasing effect is also observed in the Fig. 2.32.

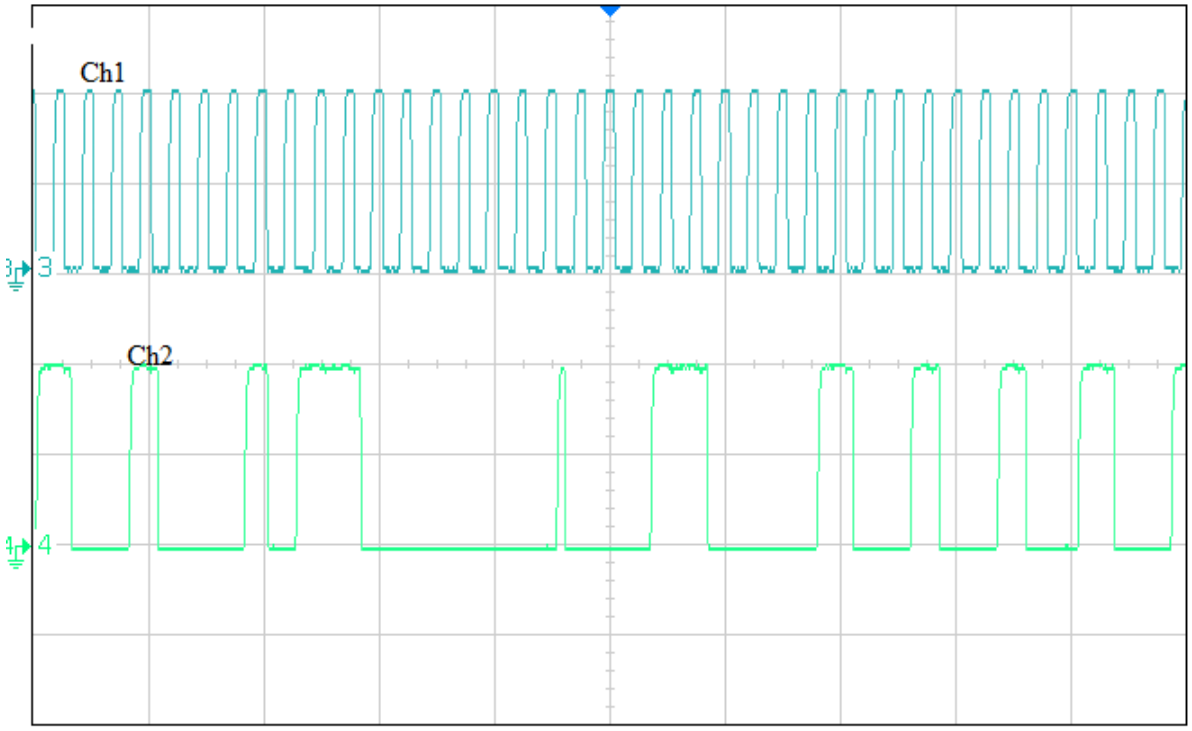

Fig. 2.27 Typical Activity on I2C bus
$(Ch1 : SCL, Ch2 : SDA, X - axis : 10us/div, Y - axis : 1.64V/div)$

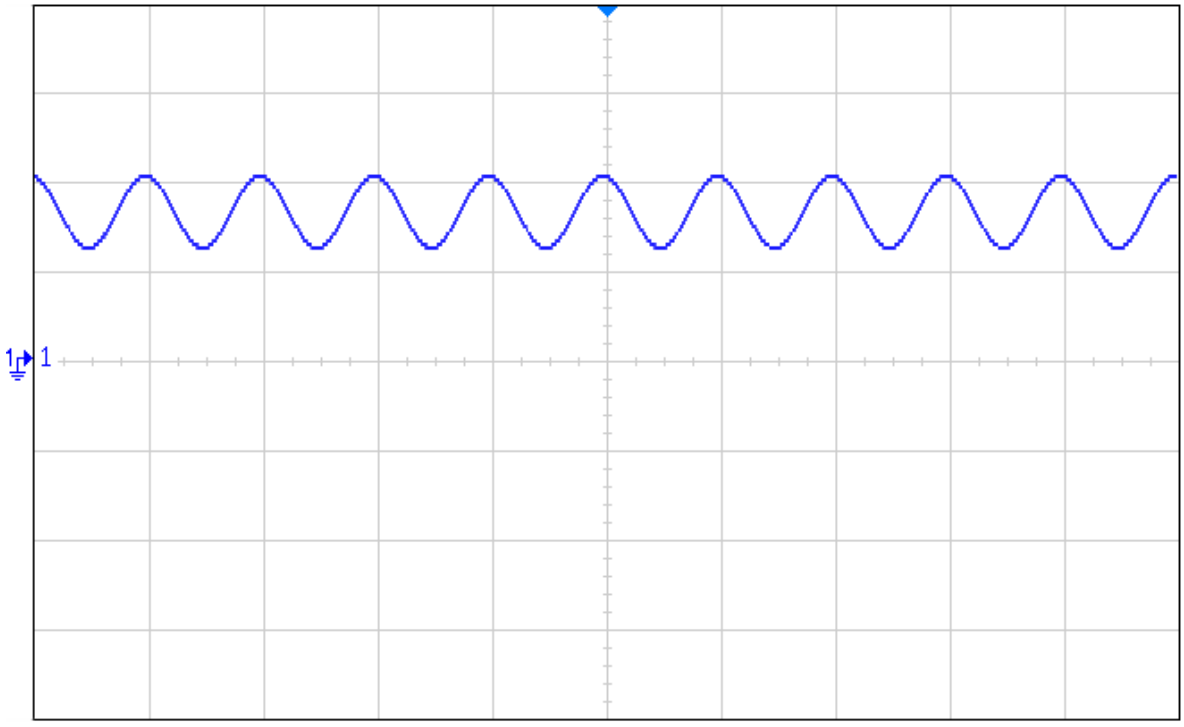

Fig. 2.28 Unipolar DAC output
$(X - axis : 20ms/div, Y - axis : 1V/div)$

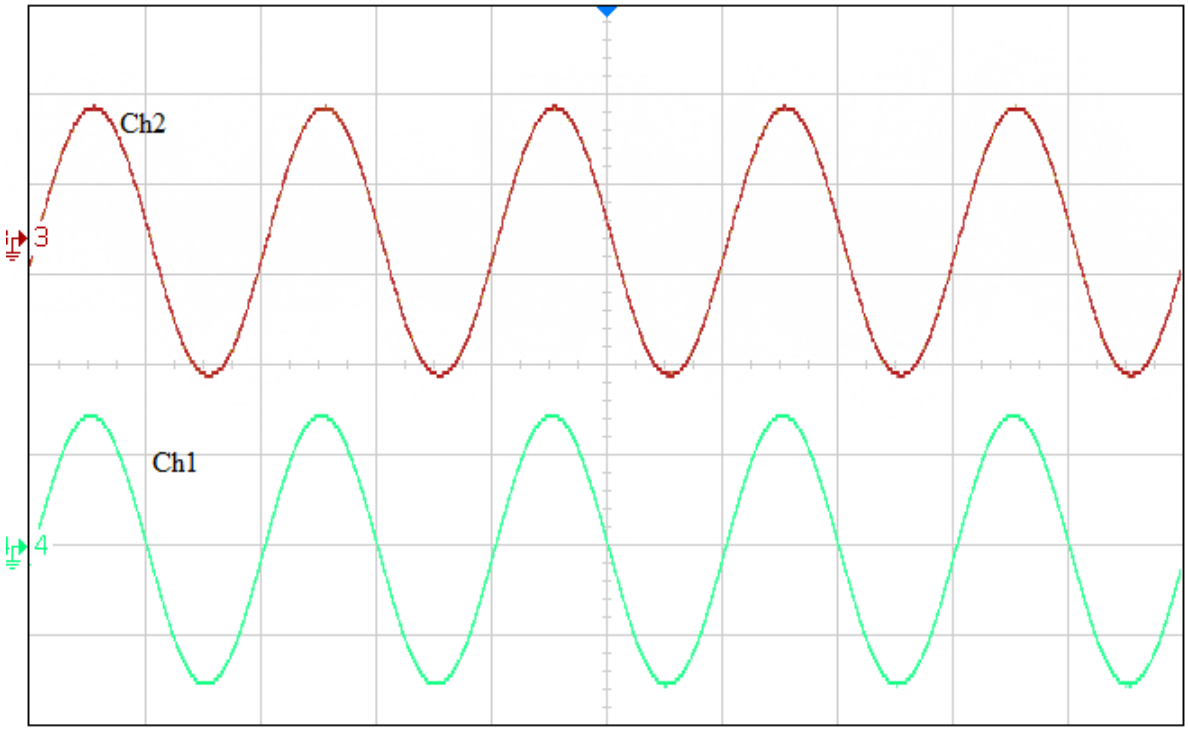

Fig. 2.29 Input analog voltage Vin and output Vout
$(Ch1 : Vin, Ch2 : Vout, X - axis : 10ms/div, Y - axis : 1.64V/div)$

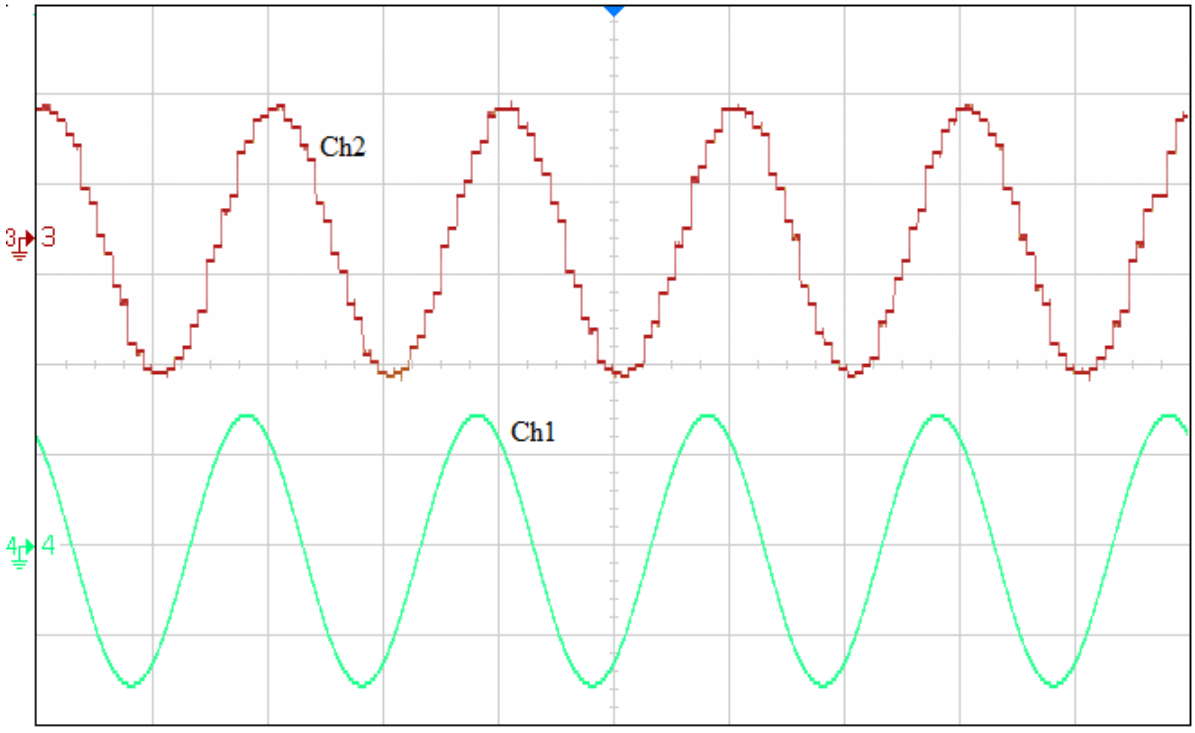

Fig. 2.30 Comparision between Vin and Vout at 500Hz
$(Ch1 : Vin, Ch2 : Vout, X - axis : 1ms/div, Y - axis : 1.64V/div)$

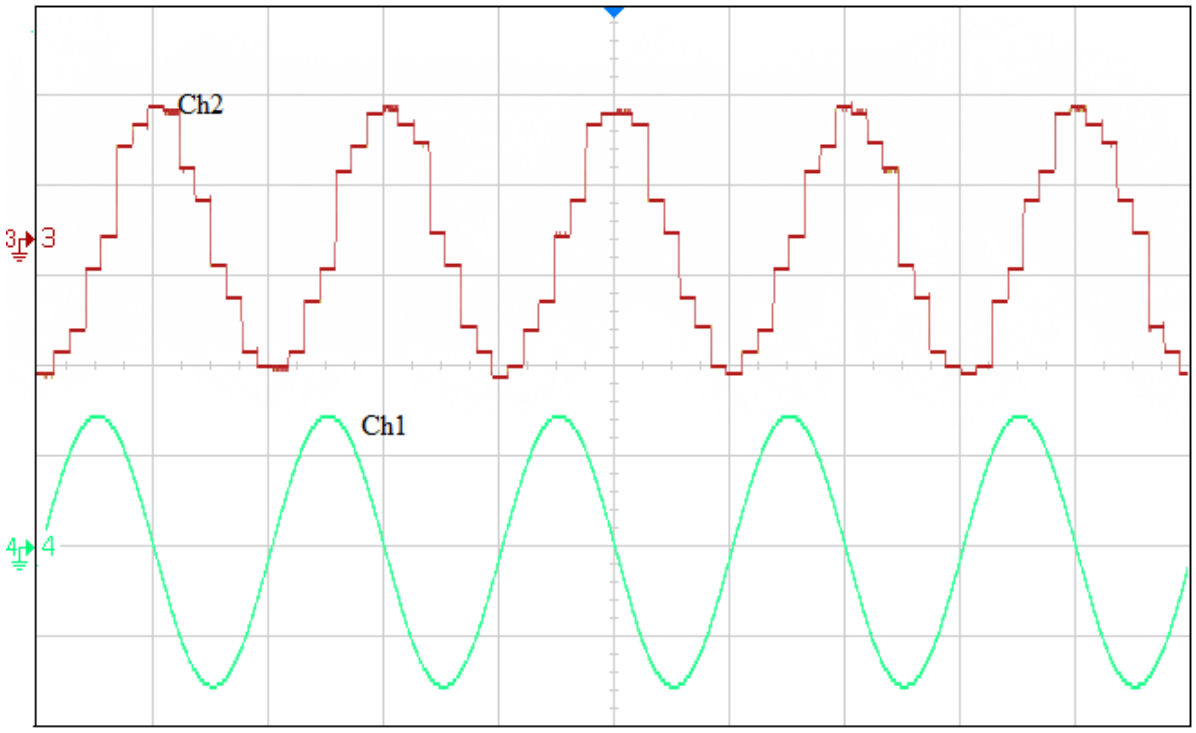

Fig. 2.31 Comparision between Vin and Vout at 1KHz
$(Ch1 : Vin, Ch2 : Vout, X - axis : 500us/div, Y - axis : 1.64V/div)$

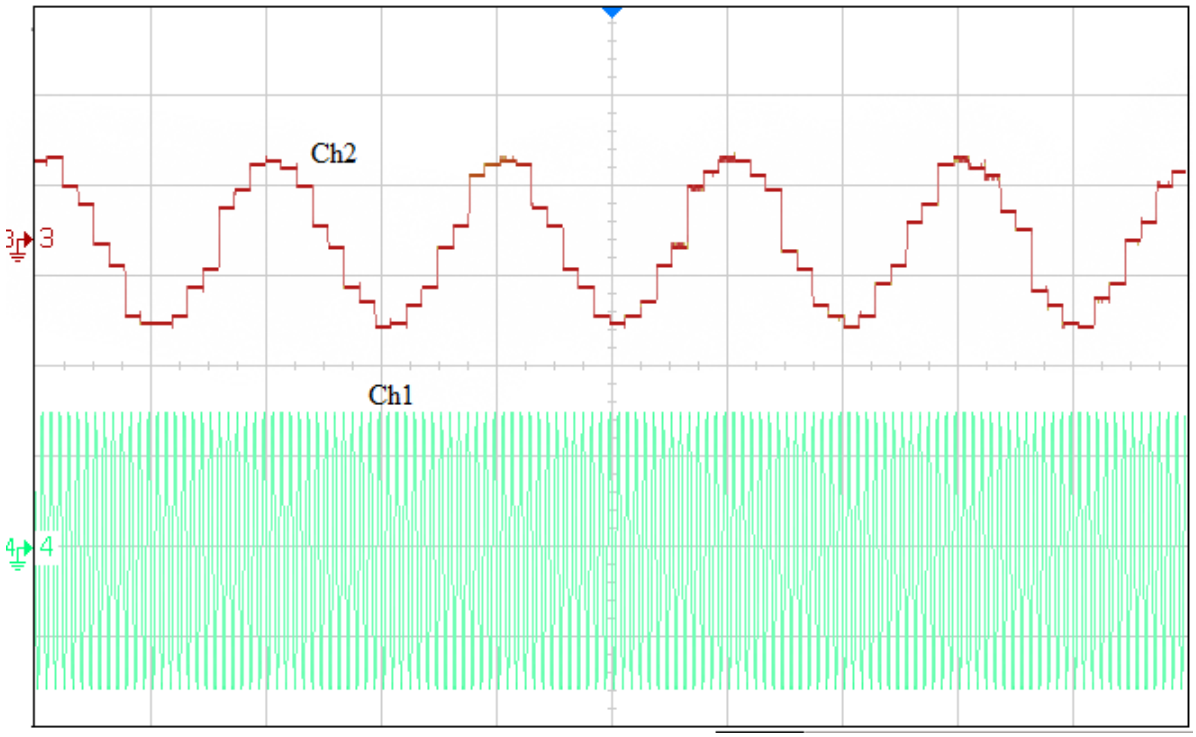

Fig. 2.32 Comparision between Vin and Vout at 28KHz
$(Ch1 : Vin, Ch2 : Vout, X - axis : 500us/div, Y - axis : 1.64V/div)$

2.5.2 Testing of RS-232 Interface

As explained in the subsection 2.4.12 connections are made between the developed board and computer. A hercules utility is used for PC serial port control. A screenshot of the utility is shown in Fig. 2.33.

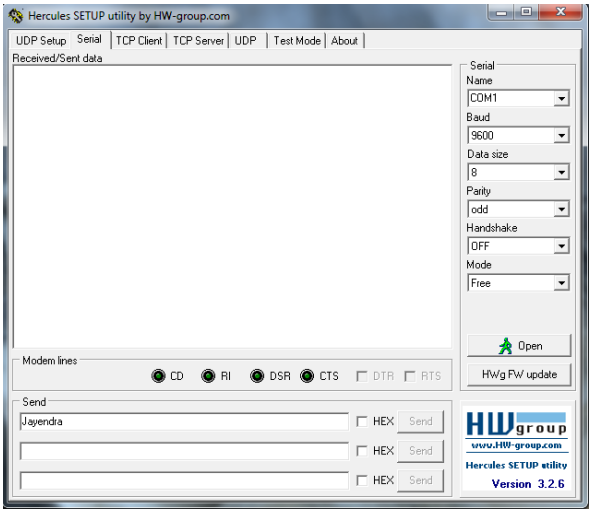

Fig. 2.33 Hercules utility(An alternative for Hyperterminal program)

The baud rate is set at 9600 which means that data transfer rate is 9600 bits per second and an odd parity is chosen. To test the RS-232 module, code is written in such a way that F28335 waits for the string "'Jayendra" . If the processor receives this string, it responds by sending " EE12M034 IITM". The screen shot of the utility after the communication is shown in Fig. 2.34.

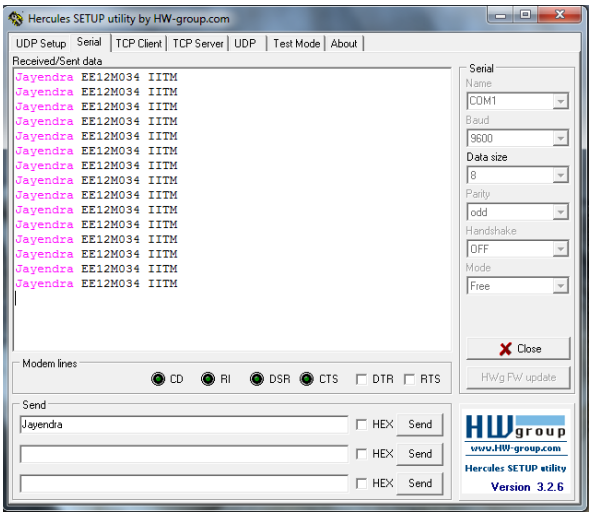

Fig. 2.34 Hercules utility after RS-232 Communication

2.5.3 Testing of CAN Bus

As discussed earlier, CAN is a message based protocol used for communication between processors without intervention of a host computer. To test the CAN bus interface on the developed board, it is used as a transmitter frame. Another peripheral explorer kit based on TMS320F28335 is configured as the receiver frame. The block diagram of test setup is shown in Fig. 2.35. The actual test setup of the CAN is shown in Fig. 2.36. Receiver frame coding is flashed on to the processor on peripheral explorer kit

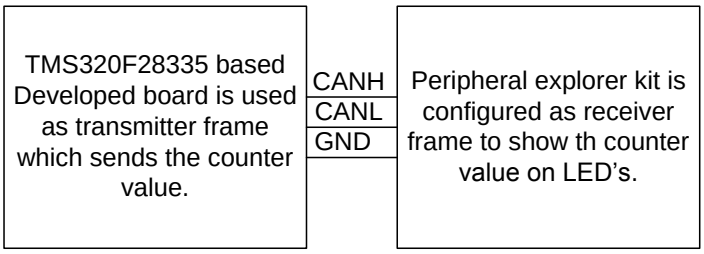

Fig. 2.35 Block Diagram of CAN module test setup

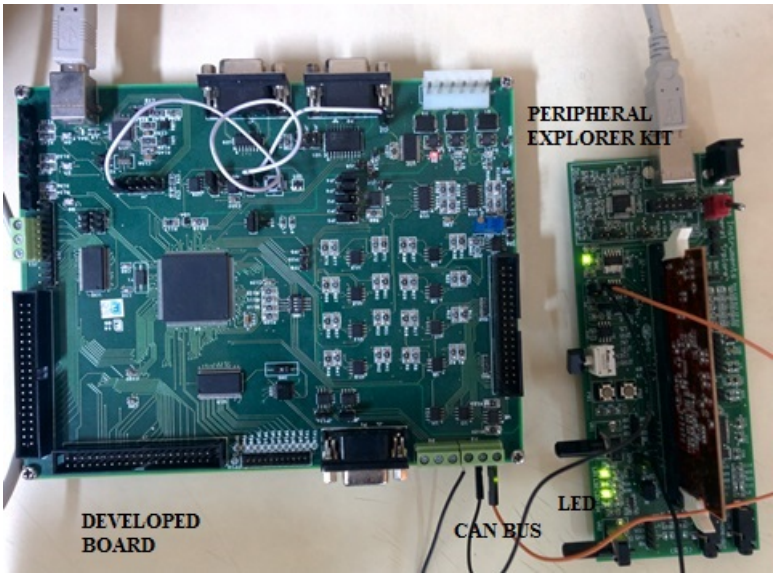

Fig. 2.36 Experimental CAN test setup

while the transmitter frame code is ran from the RAM of developed board which is connected to CCS. Transmitter frame increments a counter and sends the counter information through the CAN bus. The receiver frame reads the message and takes necessary action. The action is to show the counter value on the four LED's present on peripheral explorer kit. The CAN bus activity while testing is shown in Fig. 2.37.

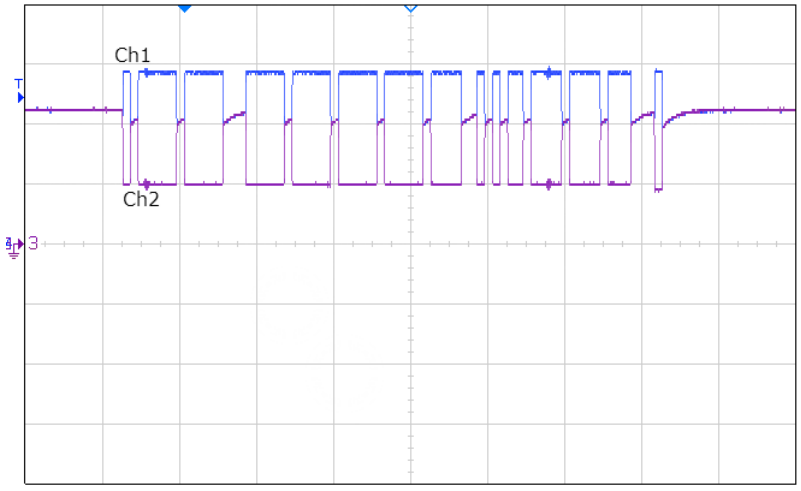

Fig. 2.37 CAN bus activity during testing
$(Ch1 : CANH, Ch2 : CANL, X - axis : 10us/div, Y - axis : 1V/div)$

2.5.4 Testing of other peripherals

The other peripherals on the developed board like LEDs, slide switches, Digital I/O's and PWM ports are tested by writing simple codes.

2.6 Conclusion

In this chapter, the various features of TMS320F28335 DSC has been presented. It is followed by the design details of the control platform like analog signal conditioning for ADC, DAC, quadrature encoder interface etc. Finally testing of all the interfaces were carried out on the developed board . Thus the TMS320F28335 based digital board is completely tested and all the modules are working properly.

CHAPTER 3

V/f CONTROL OF INDUCTION MOTOR DRIVE

3.1 Introduction

Variable Speed Drives are increasingly becoming popular in the industry. Many of the speed control applications such as fan, pump drives do not require very good dynamic performance. In such applications the most suitable method of speed control of induction motor is V/f control. *TMS320F28335 based digital control platform is tested by implementing V/f control of induction machine*.

3.2 Basic principles of *V/f*

In the V/f control, the speed of induction motor is controlled by the adjusting magnitude of stator voltages and frequency in such a way that the air gap flux is always maintained at the desired value at the steady-state. Sometimes this scheme is called the scalar control because it focuses only on the steady-state dynamics.This technique can be better explained by using simplified version of steady state equivalent circuit of induction machine.

Fig. 3.1 shows the steady state equivalent circuit of an induction machine. The stator

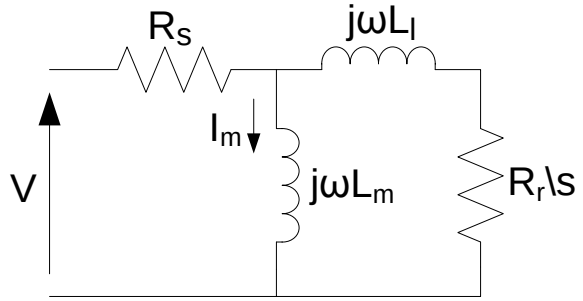

Fig. 3.1 Simplified Steady-State Equivalent Circuit of Induction Motor

resistance (Rs) is assumed to be zero and the stator leakage inductance (Lls) is embedded into the rotor leakage inductance (Llr)(referred to stator) and the magnetizing

inductance, which is representing the amount of air gap flux, is moved in front of the total leakage inductance (Ll = Lls + Llr). As a result, the magnetizing current that generates the air gap flux can be approximated as stator voltage to frequency ratio. Its phasor equation(for steady-state analysis) can be written as:

$$\overline{I}_m \cong \frac{\overline{V}}{j\omega L_m}. \tag{3.0}$$

If the induction motor is operating in the linear magnetic region, then Lm is a constant. Then, (3.0) can be shown in terms of magnitude as:

$$I_m = \frac{\phi_m}{L_m} \cong \frac{V}{(2\pi f)L_m}. \tag{3.1}$$

where, V and ϕ are their magnitude of stator voltage and stator flux, and $\overline{V}$ is the phasor representation respectively.

From the last equation, it follows that if the ratio V/f remains constant for any change in f, then the flux remains constant and the torque becomes independent of the supply frequency. In order to keep ϕ_m constant, the ratio of V/f would also be constant at the different speed. As the speed increases, the stator voltages must, therefore, be proportionally increased in order to keep the constant ratio of V/f. However, the frequency is not the real speed because of a slip as a function of the motor load. At no-load torque, the slip is very small, and the speed is nearly the synchronous speed. Thus the simple open-loop V/f system cannot precisely control the speed in presence of a load torque.

In practice, the stator voltage to frequency ratio is usually based on the rated values of these variables. The typical V/f profile can be shown in 3.2. Basically, there are three speed ranges in the V/f profile as follows:
(a) At 0-fmin Hz, a voltage is required, so the voltage drop across the stator resistance cannot be neglected and must be compensated for by increasing the V. So, the V/f profile is not linear. The cutoff frequency fmin and the suitable stator voltages may be analytically computed from the steady-state equivalent circuit with $Rs \neq 0$.
(b) At fmin-frated Hz, it follows the constant V/f relationship. The slope actually represents the air gap flux quantity as seen in (3.1).

(c) At higher frated Hz, the constant V/f ratio cannot be satisfied because the stator voltages would be limited at the rated value in order to avoid insulation breakdown at stator windings. Therefore, the resulting air gap flux would be reduced, and this will unavoidably cause a decrease in the developed torque correspondingly. This region is usually called the field weakening region. The constant V/f principle is violated at such frequencies. In this implementation, the profile in 3.2 is modified by imposing a lower

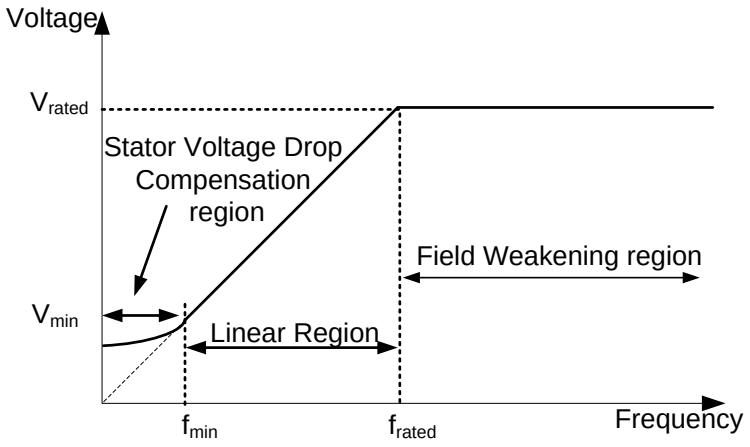

Fig. 3.2 Stator Voltage Versus Frequency Profile Under V/f Control

limit on frequency, which is shown in 3.3. This approach is acceptable to applications such as fan and blower drives where the speed response at low end is not critical. Since the rated voltage, which is also the maximum voltage, is applied to the motor at rated frequency, only the rated minimum and maximum frequency information is needed to implement the profile.

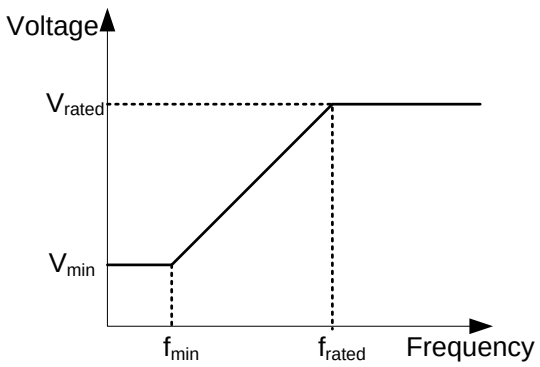

Fig. 3.3 Modified V/f Profile

3.3 Hardware Setup

V/f control technique is implemented using developed TMS320F28335 based control platform on a 30Kw induction motor. A Semikron made 3-phase, 2-level Voltage Source Inverter is used as the drive inverter. Developed board is interfaced with inverter via protection and delay card. The ratings of the machine are given in Table 3.1.

Table 3.1 Ratings for the 30kW motor

Parameters	**Value**
Power	30kW
Voltage	380V
Current	59A
Power factor	0.88
Connection	Δ
Speed	1450 rpm
Rotor type	Squirrel Cage

3.3.1 Three phase inverter module

A 3-phase 2-level Voltage Source Inverter(VSI) from Semikron is used for obtaining the input voltage to motor terminals. The inverter uses 1200V, 100A IGBT modules as power switches with each module forming one leg of the inverter. The inverter has a front end diode bridge rectifier for energising the DC bus from an input 3-phase supply. A pre charging circuit consisting of resistors in parallel with relays is connected in series with each line to prevent large inrush currents into the capacitor during energising. The rectifier and the IGBT modules are mounted on the heat sink and connected to the DC bus capacitor by busbars. Three gate driver cards are mounted on the module for giving proper isolation and to drive IGBT gate terminals.

3.3.2 Protection and delay card

The function of protection and delay card is to provide protection against faults. It also generates complementary signals with appropriate delay between top and bottom switches of an inverter leg. The three top switch PWM signals from developed digital board are fed to protection and delay card. It generates complementary signals with

proper delay using RC circuits and logic gates. These are then given to the gate driver inputs of the inverter module. The Motor line currents and DC bus voltage are sensed using hall sensors (LA100P for current sensing and LV25P for voltage sensing) and they are fed to high speed comparators. The references for protection can be set using potentiometers. The output of comparators indicate fault conditions and are fed to an RS latch using a wired AND logic. LEDs are provided for fault indication. Protection and delay card has provision to provide protection for 6 sensed currents and two voltages. The card also has provisions to transmit and recieve the PWMs in either differential or single ended fashion. It also controls the relays of the precharging circuit thereby protecting the DC link capacitors from large inrush currents.

3.4 Implementation

The overall system implementing a 3-phase induction motor V/f drive implementation is depicted in 3.4. The induction motor is driven by the conventional voltage-source inverter. The developed TMS320F28335 based control platform is used to generate the three pulse width modulation (PWM) signals for top switches using a space vector PWM technique. The protection and delay card generates the PWM signals for bottom switches with appropriate delay from the top switch signals. The generated PWMs are given to inverter module.

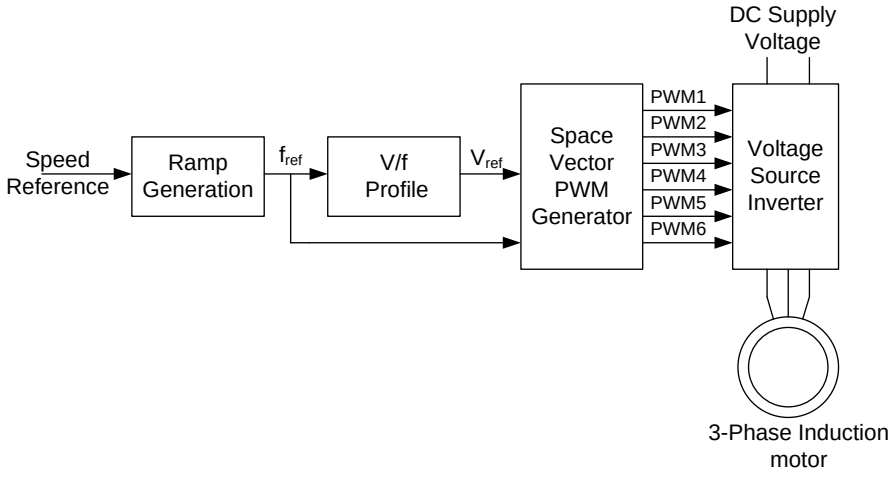

Fig. 3.4 A 3-ph Induction Motor V/f Drive Implementation

The V/f ratio is calculated so as to keep the flux inside the machine to half the rated value. A speed command of full rated value was given and the ramp rate was adjusted

so that full speed was reached in 65 seconds. A space vector PWM scheme is adopted to realise the necessary voltage from the inverter. It is important to note that the machine is operated at half the rated flux to ensure that the inverter does not tripduring its operation as the inverter is rated only for 10 kVA and induction motor is rated for 30kW.

The peak value of phase voltage required for operation at half the rated flux is given as

$$V_{ph} = \frac{380}{2} \times \frac{1}{\sqrt{3}} \times \sqrt{2} = 155.13V \tag{3.1}$$

For a given modulation index m, the peak value of phase voltage in SVPWM switching is given as

$$V_{pk} = 1.15 \times m \times \frac{V_{dc}}{2} \tag{3.2}$$

Assuming a maximum modulation index of 0.9 at 50Hz frequency the required Dc bus voltage as

$$1.15 \times m \times \frac{V_{dc}}{2} = 155.13 \Rightarrow V_{dc} = 300V \tag{3.3}$$

On board DAC is used to output the modulating waveforms which are internal variable

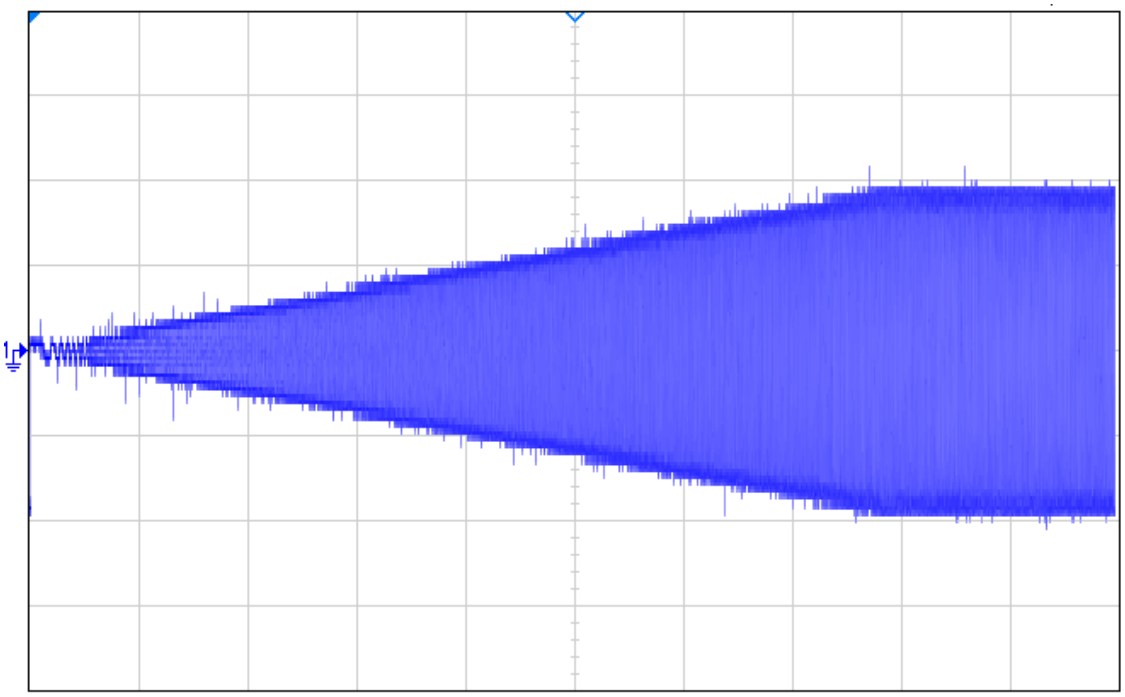

Fig. 3.5 R-phase modulating signal
$(X - axis : 8.4/div, Y - axis : 0.5pu/div)$

in PWM generation. The waveforms obtained by running the V/f control with the cal-

culated values for operation at half the rated flux are shown in Fig.3.5 , 3.6 and 3.7.

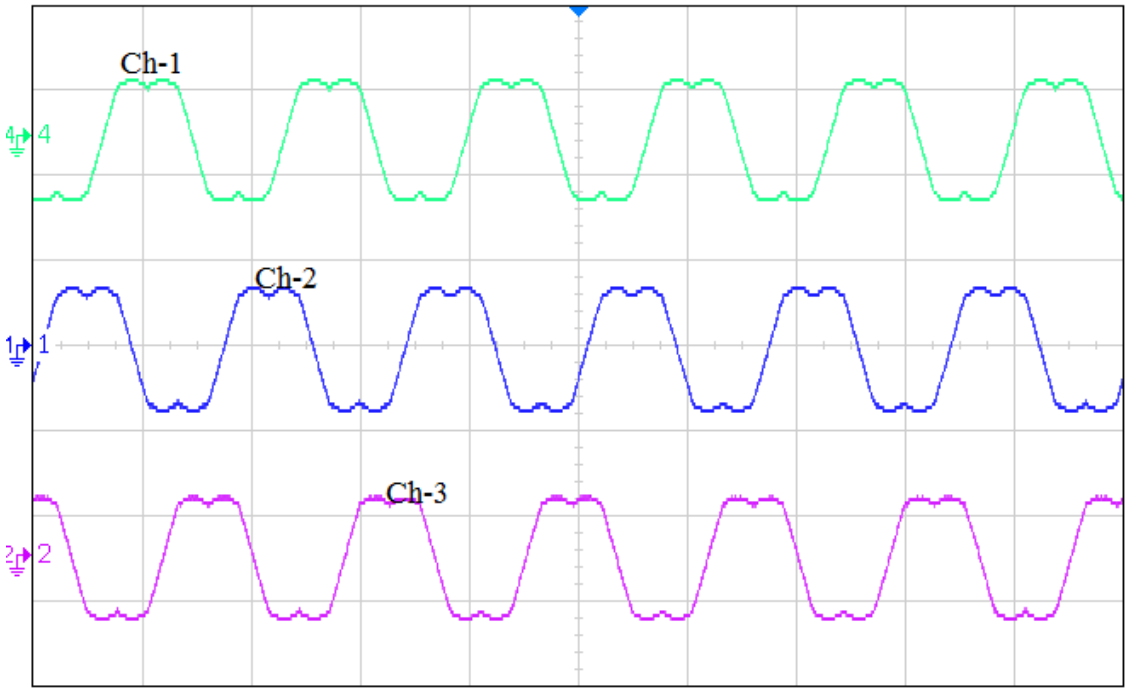

Fig. 3.6 3-Phase modulating waveforms for steady state operation at 50 Hz
$(Ch1 - Rph, Ch2 - Yph, Ch3 - Bph, X - axis : 11.8ms/div, Y - axis : 1.3pu/div)$

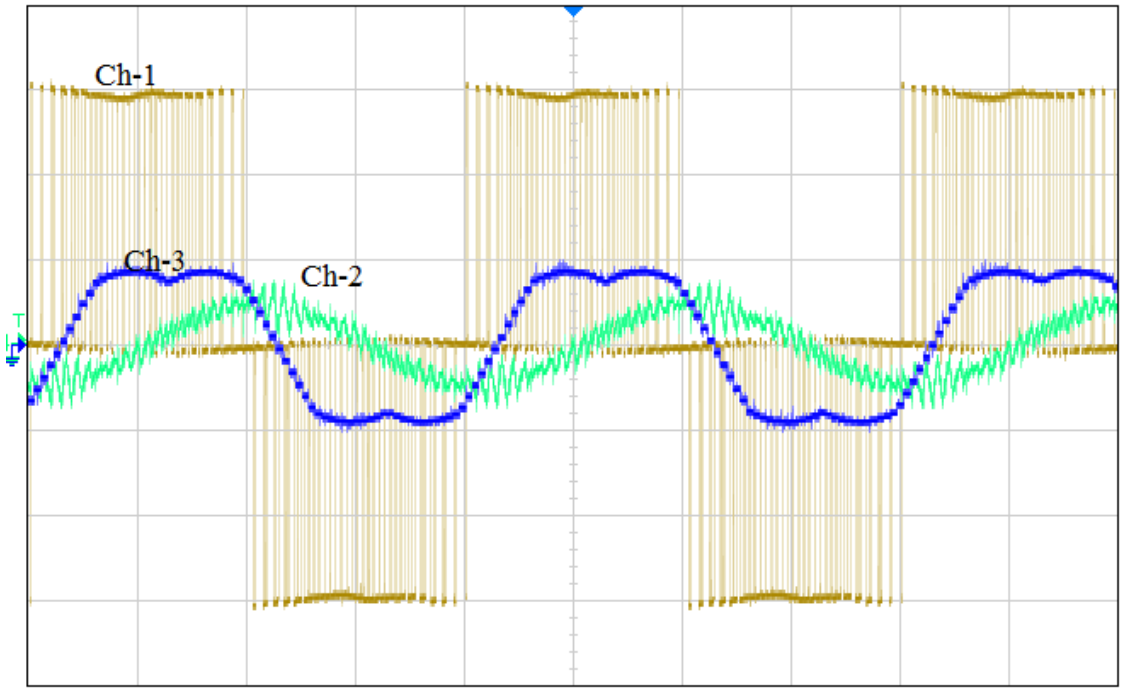

Fig. 3.7 R-Y line voltage, R-phase current and R-phase modulating signal
$(Ch1 - Yaxis : 100V/div, Ch2 - Yaxis : 20A/div, Ch3 - Yaxis :$
$0.5pu/div, X - axis : 5ms/div)$

3.5 Conclusion

This chapter outlined the basic principle of scalar control of induction machine. The modulation used in the controller is space vector modulation. In this chapter, implementation details and hardware setup for the running the V/f control is presented. This shows the capability of the developed DSC based digital board to work as a full fledged real time control platform.

CHAPTER 4

DESIGN OF FPGA BASED DIGITAL BOARD

An attempt has been made to develop a full fledged FPGA control platform for motor drive applications. The digital control board design with Altera Cyclone IV FPGA has been carried out. The PCB layout and testing of the board is to be done. *This chapter outlines the important features of FPGA. It also provides design details of FPGA board.*

4.1 Hardware requirements for FPGA based digital platform

The block diagram of designed digital platform with Cyclone IV FPGA is shown in Fig. 4.1. For control of electric drives, analog signals such as voltages and currents are to be sensed. Therefore analog signal conditioning and ADC is essential. DAC is used to have real time monitoring of some internal variables of the control algorithm. Therefore a DAC interface is provided in this board. Digital I/O ports can be used for PWM outputs. LCD interface is also provided. Interfaces for standard protocols like RS-232, RS-485, CAN, USB , ethernet is also provided to enable industrial level communications with Programmable logic controllers (PLC) and Human Machine Interface(HMI).

4.2 Features of Cyclone IV

The selection of device is carried out by rough estimation of Logic Elements. A Cyclone IV device with around 30K logic gates is chosen suitable to implement motor control algorithms and required communication protocols. The IC is chosen to meet industrial grade temperature(-40/^{o}C to +85/^{o}C). The device that matches above requirement is EP4CE30F23I7N. The description of selected FPGA part number is shown in 4.2.
The features of the selected FPGA are given in Table 4.1.

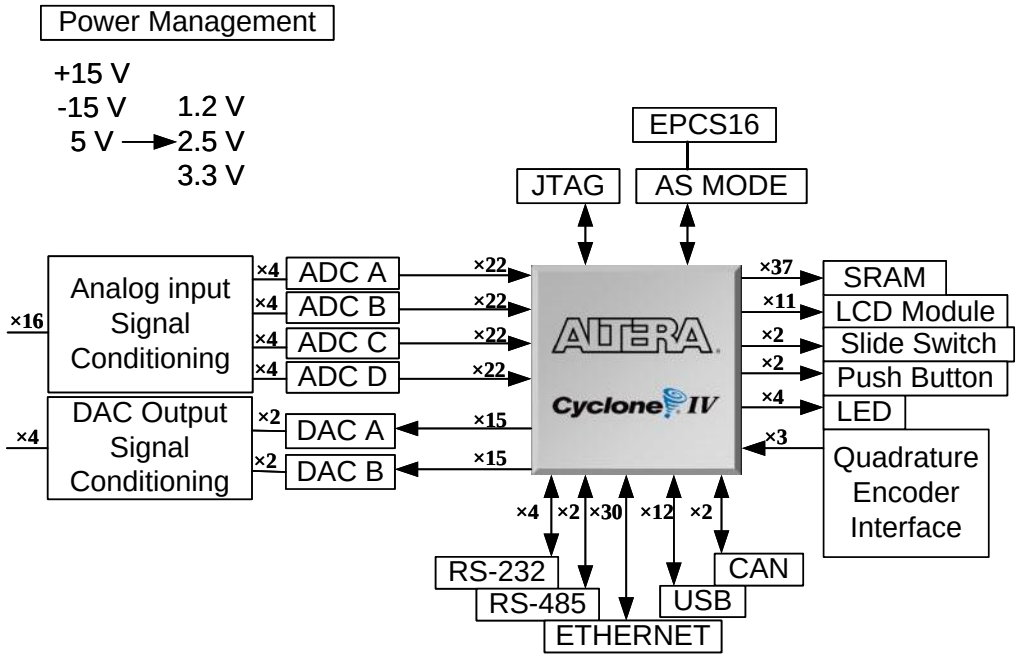

Fig. 4.1 Block diagram of FPGA based digital platform

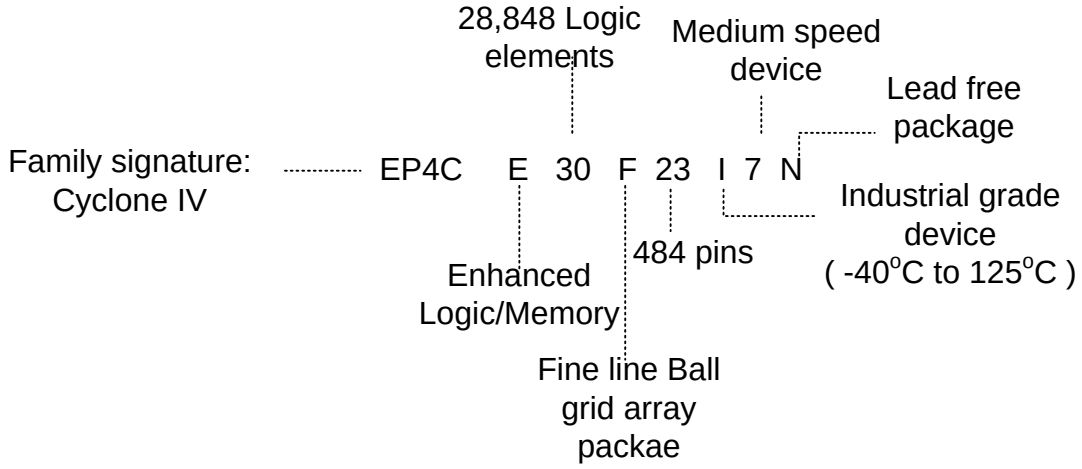

Fig. 4.2 Cyclone IV Device Description

4.3 Configuration of Cyclone IV FPGA

There are two procedures for downloading a circuit developed in a host computer with Quartus II software, to the control board. Both types of programming methods are described in this section.

Table 4.1 Features of Cyclone IV FPGA

Parameters	**Value**
Part No	EP4CE30F23I7N
Manufacturer	ALTERA
Number of pins	484
Package	FBGA
Number of Logic elements	28,848
Number of PLL	4
Embedded 18×18 multipliers	66
Embedded memory	594Kbits
Number of user I/O	324
Power supply for core	1.2V
Power supply for I/O	3.3V
Power supply for PLL	2.5V

4.3.1 JTAG Programming

In this method of programming, named after IEEE standards Joint Test Action Group, the configuration bit stream is downloaded directly into Cyclone IV FPGA. The FPGA will retain this configuration as long as power is supplied to the board. The configuration information will be lost when power is turned off.

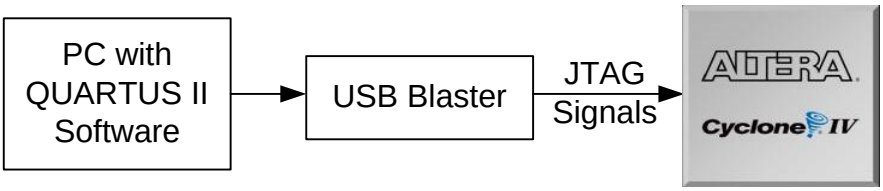

Fig. 4.3 The JTAG Configuration Scheme

4.3.2 Active Serial(AS) Programming

In AS mode of programming, the configuration bit stream is downloaded into Altera EPCS16 serial configuration device. It provides non-volatile storage of bit stream, so that the information is retained even when the power supply to the board is turned off. When board's power is turned on, the configuration data in the EPCS16 device is automatically loaded into Cyclone IV FPGA.

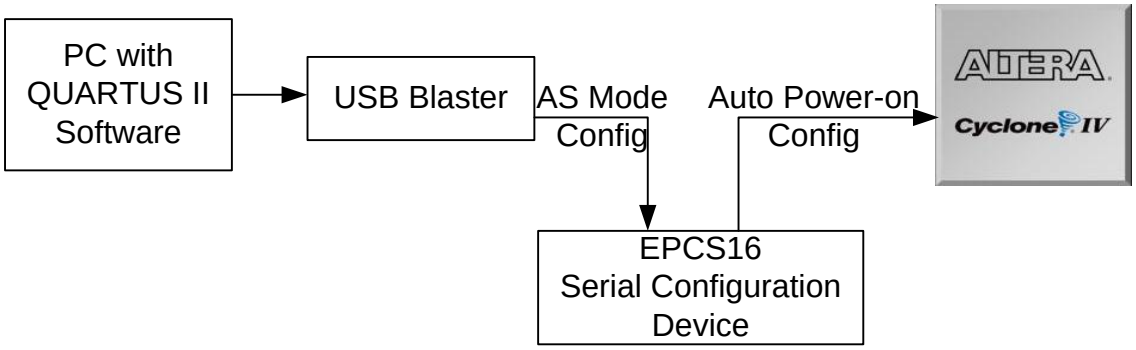

Fig. 4.4 The Active Serial Configuration Scheme

4.4 FPGA board design details

This section presents the detailed design details of all the interfaces done in the board.

4.4.1 Power management

FPGA board requires external +15 V, -15V and +5V. Cyclone IV FPGA requires 1.2 V for core operation, 2.5 V for PLL functioning and 3.3V for input and output operations. All the different voltages required by FPGA is derived on board using Low Drop Out (LDO) regulators. In addition to this, ADC requires 2.5V reference which is provided using AD780. The DAC requires 10V reference voltage which is provided using ADR01. Analog signal conditioning ciruit requires precision 5V for level shifting. It is provided by using ADR02. All the IC's AD780, ADR01, ADR02 are ultra high precision band gap reference voltage ICs.

4.4.2 Analog to Digital Converter

High resolution and fast conversion time are the two factors considered for the selection of Analog to Digital converter. In this board, AD7655 is chosen as the preffered ADC. The AD7655 is a low cost, four channel, 16-bit, charge redistribution SAR Analog to Digital Converter which operates from a single +5V power supply. It contains two low noise, wide bandwidth track/hold amplifiers which allow simultaneous sampling, a high-speed 1 MSPS 16-Bit sampling ADC, an internal conversion clock, error correction circuits, and both serial and parallel system interface ports. Parallel interface has faster conversion time. ADC requires a external precision 2.5V reference which is

provided from precision voltage regulator AD780. The conversion time for each channel is 80nsec. Since 16 analog signals are to be converted, four such ADC's are used. The analog input voltage to the ADC should be unipolar and should be in the range of 0V-5V. So the real world bipolar signals need to be converted to unipolar signals to interface appropriately with the selected ADC. The conditioning of analog signals to match the levels of ADC is presented in next section.

4.4.3 Analog signal conditioning

ADC AD7655 accepts analog signals in the range 0V-5V. The Industrial standard output voltage levels of transducer is $\pm 10V$. So it is attenuated and level shifted using a single, low offset, high precision op-amp OPA2228U from Texas Instruments.

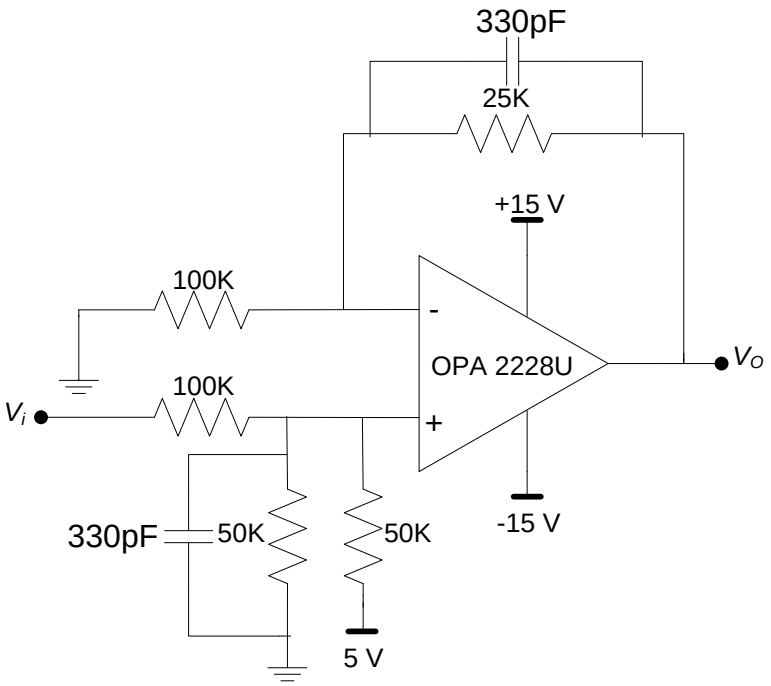

Fig. 4.5 Analog Signal Conditioning Circuit for AD7655

(a) With only 5 V source acting and $V_i = 0$, The circuit can be redrawn as

Applying KCL at inverting node,

$$(\frac{0 - V_a}{100K}) + (\frac{V_{O1} - V_a}{25K}) = 0 \tag{4.0}$$

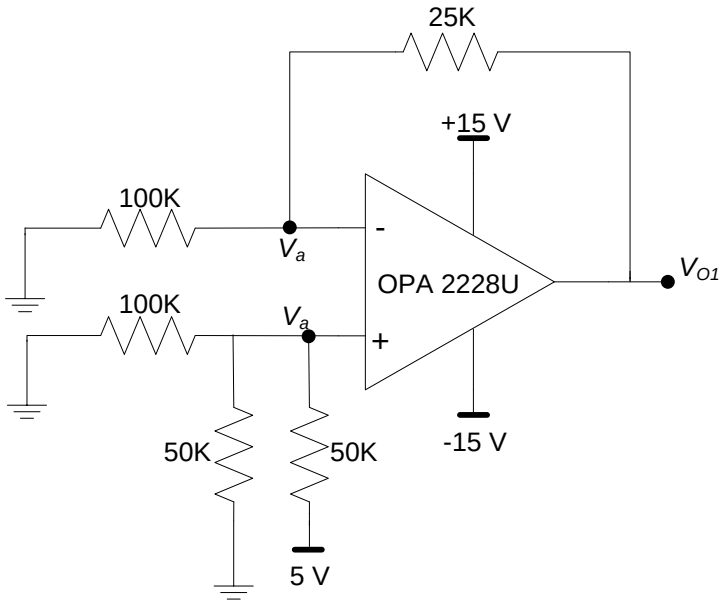

Fig. 4.6 Analog signal conditioning circuit for AD 7655 with only 5 V source acting

Solving 4.0, the output voltage due to 5 V source acting alone is given by

$$V_{O1} = \frac{5}{4} \times V_a \tag{4.1}$$

By using voltage divider rule, V_a is given by

$$V_a = \frac{(100K//50K)}{(100K//50K) + 50K} \times 5V = 2V \tag{4.2}$$

Substituting 4.2 in 4.1, We get

$$V_{O1} = 2.5V \tag{4.3}$$

(b) With only V_i acting and 5 V source grounded, the circuit can be redrawn as
By using voltage divider rule

$$V_b = \frac{25K}{25K + 100K} \times V_i = \frac{V_i}{5} \tag{4.4}$$

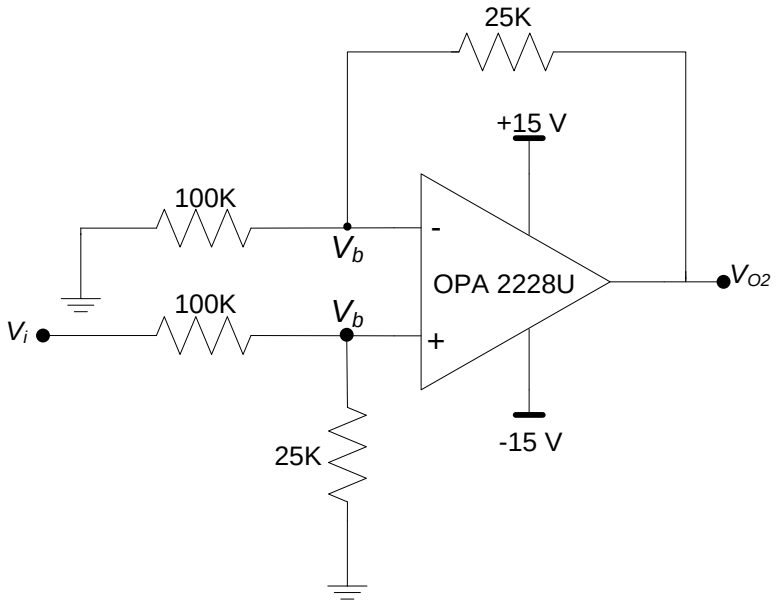

Fig. 4.7 Analog signal conditioning circuit for AD 7655 with only V_i source acting

Applying KCL at inverting node,

$$(\frac{0 - V_b}{100K}) + (\frac{V_{O2} - V_b}{25K}) = 0 \tag{4.5}$$

$$\Rightarrow V_{O2} = \frac{5}{4} \times V_b \tag{4.6}$$

Substituting 4.4 in 4.6, We get

$$V_{O2} = 0.25V_i \tag{4.7}$$

By using superposition theorem, the output voltage V_O when both sources are acting together is given by

$$V_O = 0.25V_i + 2.5 \tag{4.8}$$

Also since it is aground noise will be reduced.

Simulation results: The circuit is simulated by using the spice file of the op amp OPA2228U provided by texas instruments and is simulated using TINA. With an input voltage of 10V peak sine wave, the output is a sinewave with peak 2.5V superimposed on a DC level of 2.5V.

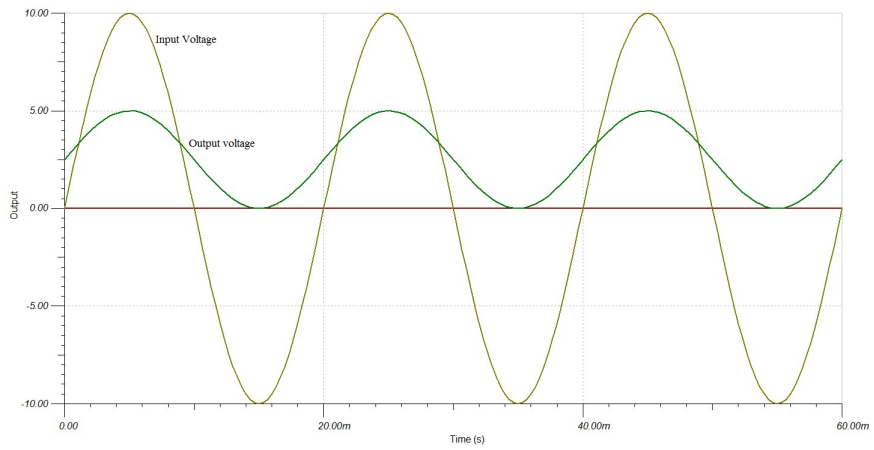

Fig. 4.8 Simulation Result of Anlalog signal conditioning

Fig. 4.10 shows the maximum drift due to input offset voltage and input bias current is 0.26mV. The signal conditioning circuit is simulated for Common Mode Rejection Ratio (CMRR) using 1V, 2MHz signal and the drift in output voltage is not exceeding 0.4mV. With reference IC AD780 drift, a maximum of 1mV drift in output voltage is noticed. The following waveforms shows the various analysis done on signal conditioning circuit.

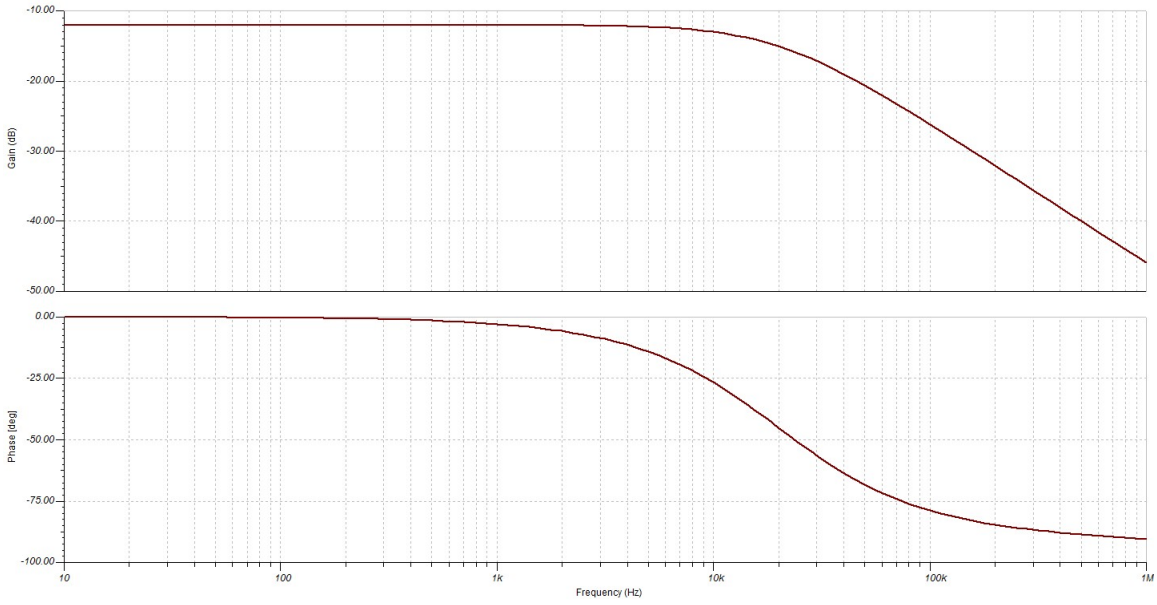

Fig. 4.9 Magnitude and Phase plot of the signal conditioning circuit

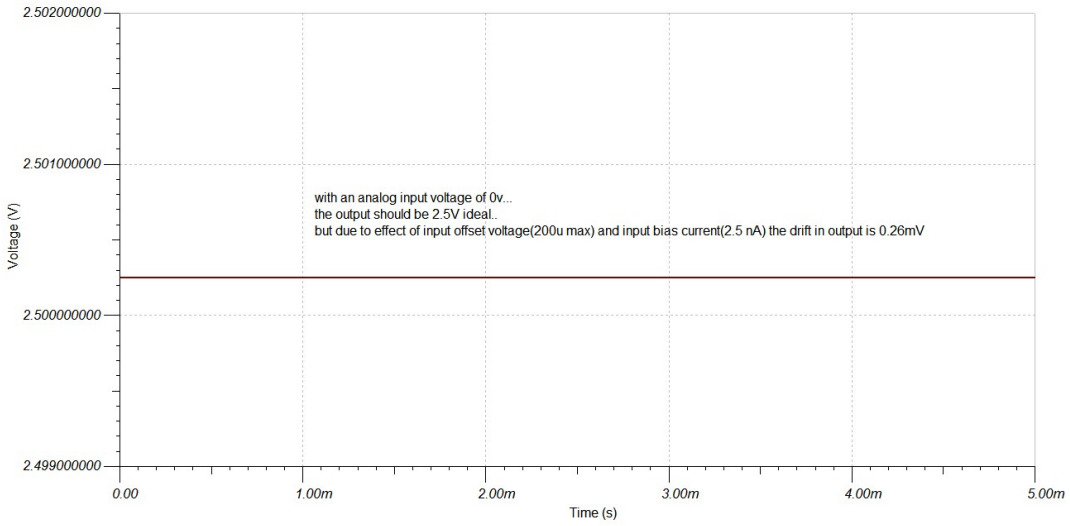

Fig. 4.10 Effect of input offset voltage and input bias current

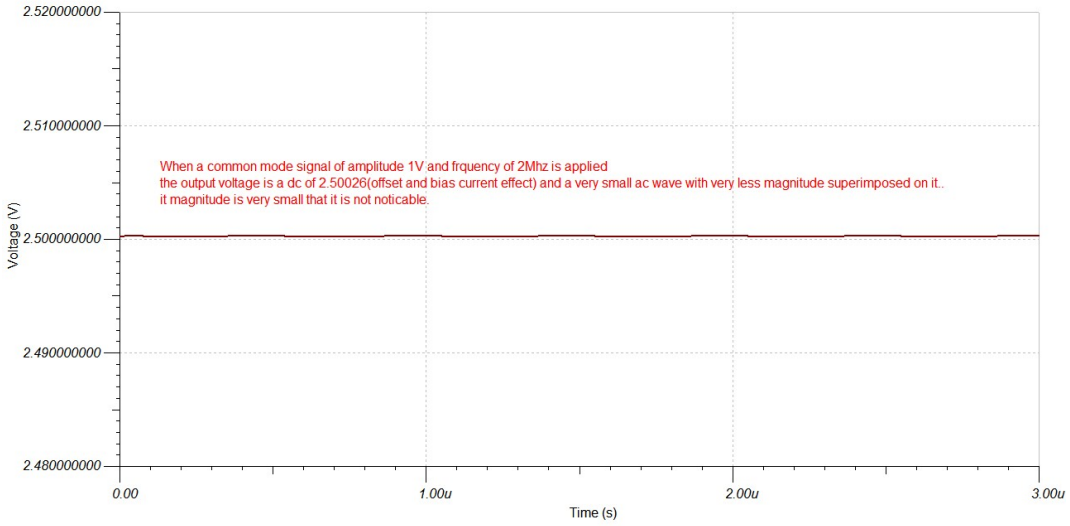

Fig. 4.11 Testing for Common mode rejection ratio

4.4.4 Digital to Analog Converter

DAC is used to convert digital to analog signals. AD5447, a 12 bit, dual-channel, current output DAC is selected. The settling time for the DAC is 80nsec. To have 4 analog outputs two such DAC's are used. DAC requires an external precision 10V reference which is provided using ADR01. So the current output of DAC is converted to voltage and buffered to -10 V to +10 V range.

The output voltage of the DAC module for a given data D is given by

$$V_O = (10 \times \frac{D}{2048}) - 10 \tag{4.9}$$

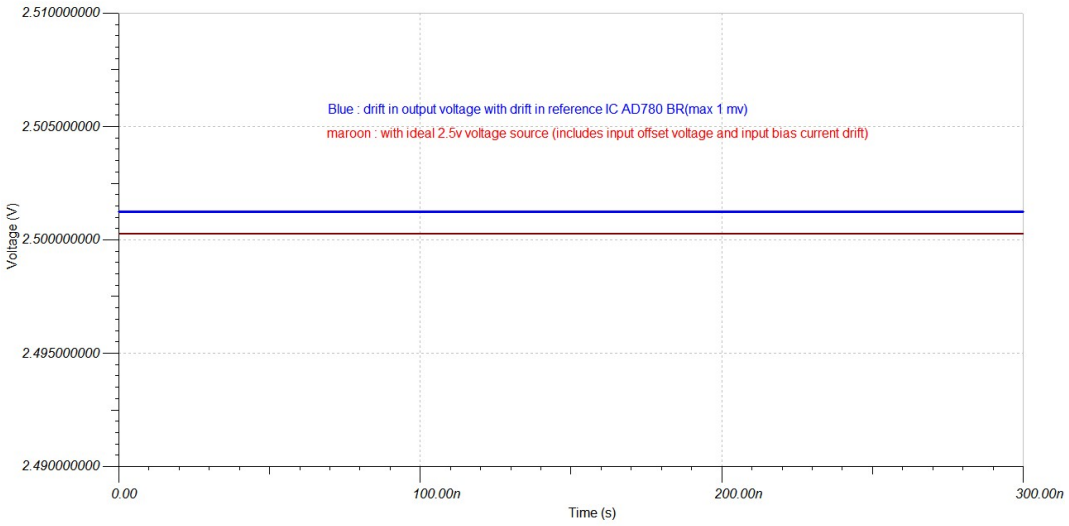

Fig. 4.12 Effect of drift in reference IC

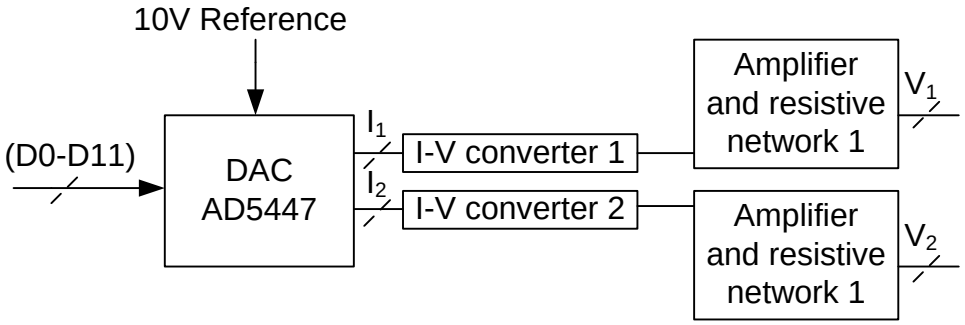

Fig. 4.13 DAC Interface Block Diagram

where D is the decimal equivalent of 12-bit data. With D = 0, output voltage is -10V and as D is increased to full scale i.e., D = 4095, the output voltage is incremented to +10 V.

4.4.5 Incremental encoder interface

Typically incremental encoders installed in the motor drives gives quadrature signals along with index pulse in a differential fashion. Quadrature signals A and B together with index pulse I can be used to measure speed and direction of rotation of machine. Since they are to be transmitted over long distances, differential transmission and receiving will eliminate common mode noises. RS-422 standard differential receiver AM26LV32C is used for proper interfacing with encoders.

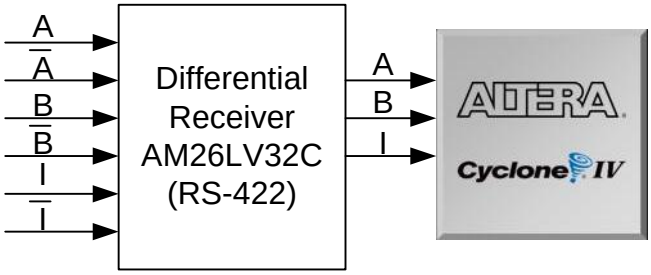

Fig. 4.14 Encoder Interface Block Diagram

4.4.6 Digital I/Os, LEDs, slide switches and push button interface

FPGA I/O's which are at 3.3V are buffered using SN74ALVC164245, a bidirectional buffer. By setting the jumpers to 0V or 3.3V they can be used as input or output port correspondingly. These ports can be used to output generated PWM signals. 48 such digital ports are provided. Four LEDs, two slide switches and two push butttons are also interfaced for debugging purposes. Push button outputs are connected with MAX6817, a switch debouncer.

4.4.7 Clock Circuitry

Cyclone IV EP4CE30F23I7N include 20 global clock networks and has fifteen dedicated pins for clock inputs. Only two of them are used for clocking and remaining pins are used as GPIO's. The board includes an oscillator that produces 50MHz clock. A provision to take external clock is also provided. A clock buffer is used to distribute clock signal with low jitter to the FPGA. In addition, all these clock inputs are connected to Phase Locked Loops(PLL) of FPGA. The clock distribution on the board is shown in Fig. 4.15.

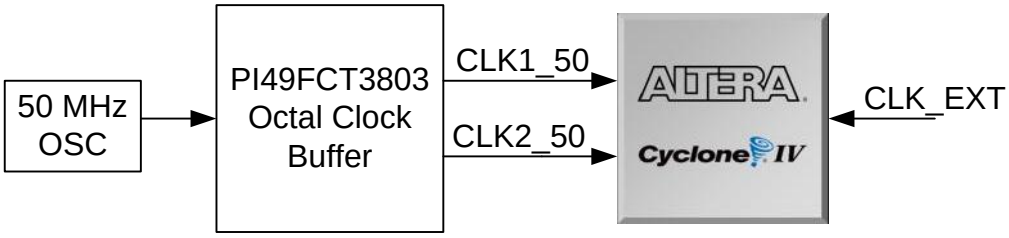

Fig. 4.15 Block Diagram of Clock Distribution

4.4.8 Isolated RS-232 Interface

RS-232 is mainly used for serial communication between computer and peripherals. It supports full-duplex communication i.e., bidirectional data flow at the same time. The board uses ADM3252E transceiver and DB9 connector for RS-232 communications. The ADM3252E is a high speed, 2.5 kV fully isolated(power and data), dual-channel RS-232 transceiver device that is operational from a single power supply. Because of high ESD protection on the transmitter and receiver, the ADM3252E is ideally suited for operation in electrically harsh environments or where RS-232 cables are frequently plugged and unplugged.The connection between FPGA and RS-232 transceiver is shown in Fig. 4.16.

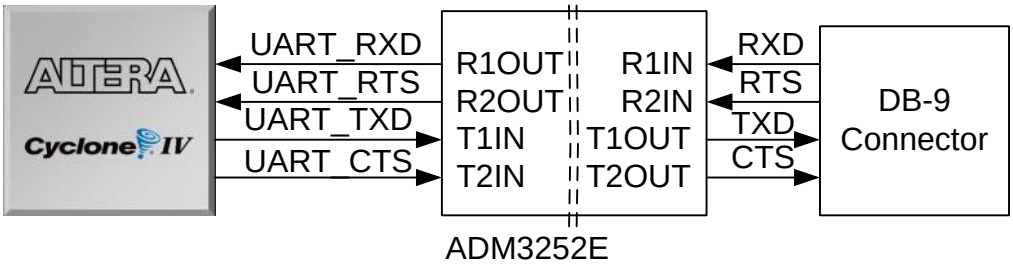

Fig. 4.16 Connections between FPGA and RS-232 Transceiver

4.4.9 Isolated RS-485 Interface

RS-485 is a differential signalling standard which is used in multi point transmission between various PLCs. ADM2587E is a 2.5kV fully isolated(power and data) RS-485 transceiver, configurable for half or full duplex communication. Y and Z are the differential driver outputs where as A and B are THE differential receiver inputs. The connection between FPGA and RS-485 transceiver is shown in Fig. 4.17.

4.4.10 Isolated CAN bus Interface

Controller Area Network (CAN) is a serial network that was originally designed for automotive networks, but has become a popular communication protocol in industrial automation as well as other applications like controlling and monitoring operation between devices. The ADM3053 is an isolated controller area network (CAN) physical

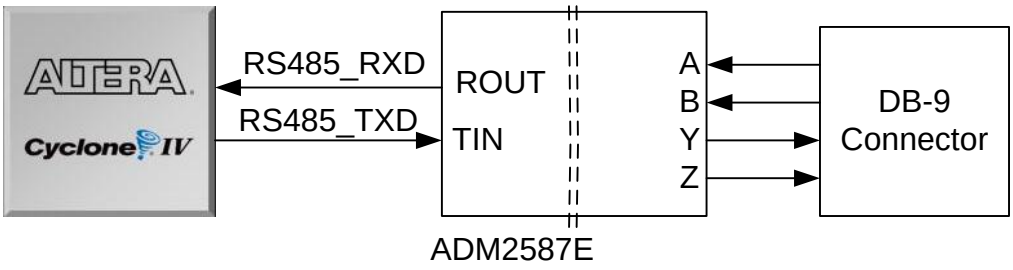

Fig. 4.17 Connections between FPGA and RS-485 Transceiver

layer transceiver with an integrated isolated dc-to-dc converter. The connection between CAN controller and FPGA is shown in Fig. 4.18.

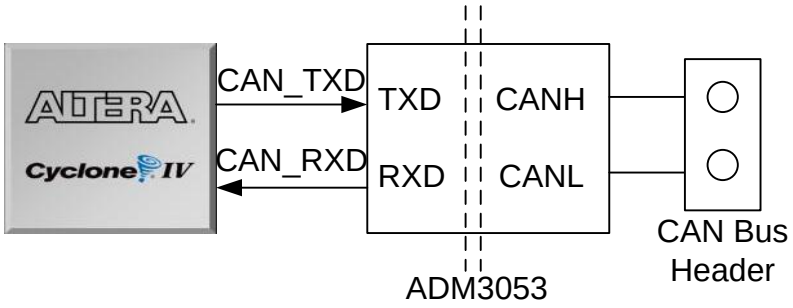

Fig. 4.18 Connections between FPGA and CAN Controller

4.4.11 Universal Serial Bus Interface

The Universal Serial Bus(USB) has evolved to be the standard interconnect between computer and peripherals. It can operate at very high speed rates (12Mb/s to 480 Mb/s). The FT245R is a USB 2.0 Transceiver. It is a single chip, USB to parallel, FIFO bidirectional data transfer interface. The connections between USB to FPGA is shown in Fig. 4.19.

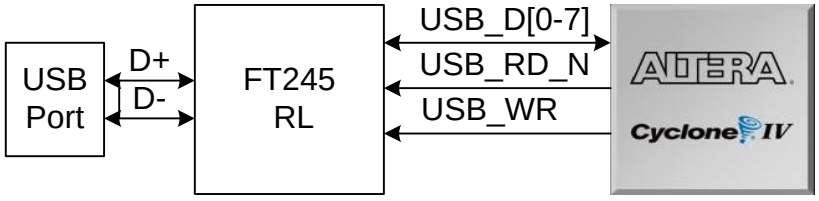

Fig. 4.19 Connections between FPGA and USB

4.4.12 10/100 Ethernet interface

The FPGA board provides ethernet support via LAN9220. The LAN9220 includes an integrated 10/100 Ethernet MAC and PHY with a high-performance SRAM-like slave interface. In addition, it is dynamically configurable to support 10 Mbps. 100Mbps operation using standard cat 5e Unshielded Twisted Pair (UTP) cabling. The connection between FPGA and Ethernet are shown in Fig. 4.20.

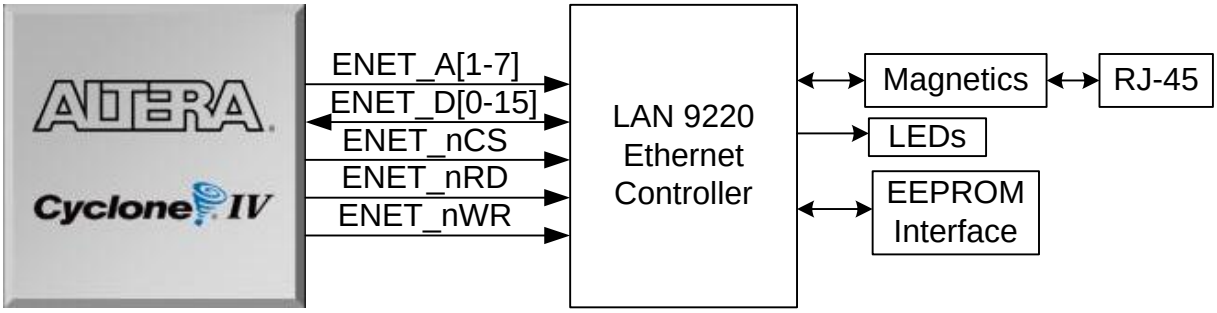

Fig. 4.20 Connections between FPGA and ETHERNET

4.4.13 LCD interface

The LCD used is a 16 character $\times$ 2 line display without backlight. It is interfaced as a write only device. LCD is mainly used for showing parameter values like voltage, current, power and speed. A schematic diagram of the LCD module showing connections to Cyclone IV FPGA is shown in Fig. 4.21.

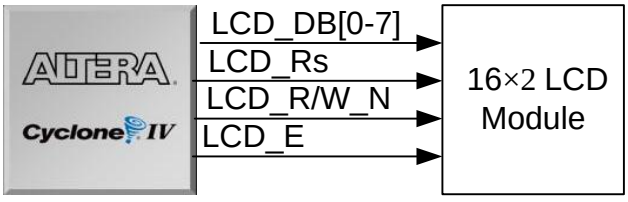

Fig. 4.21 Connections between FPGA and LCD

4.4.14 SRAM Interface

The FPGA based digital board has 1Mb (128K $\times$ 8) SRAM memory with 8 bit width data bus. Being featured with a maximum performance frequency of about 125MHz

under condition of standard 3.3V power supply it is suitable for fast retrieval of data. The high speed access time is 45nsec. The connections between FPGA and SRAM are shown in Fig. 4.22.

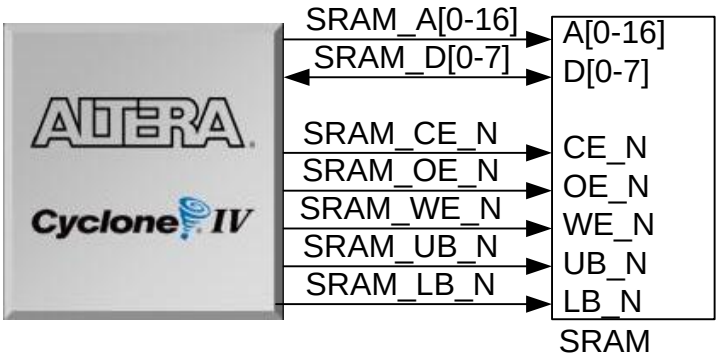

Fig. 4.22 Connections between FPGA and SRAM

4.4.15 Expansion Header for GPIO's

56 GPIO pins are brought out with ESD protection and diode clamping to a header. This pins will be left for the users to interface.

4.5 Conclusion

This chapter outlined the hardware requirements for a FPGA based digital control platform. It is followed by the design details of the control platform like analog signal conditioning for ADC, DAC, quadrature encoder interface and communication protocols like RS-232, Rs-485, USB, Ethernet etc. Thus the FPGA based control platform is designed based on the requirements.

CHAPTER 5

CONCLUSION AND FUTURE SCOPE OF WORK

5.1 Conclusion

In this report, the necessity of DSC and FPGA based control platforms were discussed. An overview on the features of TMS320F28335 was presented. TMS320F28335 DSC based control platform has been designed. A 4-layer PCB is developed and all the peripherals were tested. Also ALTERA Cyclone IV FPFA based control platform has been designed.

5.2 Future Scope

FPGA board PCB layout and testing of the board is to be done. In TMS320F28335 based control platform all the communication protocol interfaces are done without isolation whereas the FPGA board is designed with 2.5kV fully isolated (both power and data) transcievers. The same features can be included in TMS320F28335 based DSC board. EMI and EMC compliance tests form another future prospect .

REFERENCES

[1] Texas Instruments., *"TMS320F28335 Data Manual",* August 2012.

[2] Texas Instruments., *"Hardware Design Guidelines for TMS320F28xx and TMS320F28xxx DSCs",* Application Notes August 2011.

[3] Altera., *"Cyclone IV Handbook",* Data sheet December 2013.