DESIGN OF AN AlGaN/GaN HEMT FOR HIGH FREQUENCY LOW NOISE APPLICATIONS

A THESIS

submitted by

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THESIS CERTIFICATE

This is to certify that the thesis titled **"Design of an AlGaN/GaN HEMT for high frequency low noise applications"**, submitted by **Pulkit Agarwal**, to the Indian Institute of Technology, Madras, for the award of the degrees of **Bachelor of Technology** and **Master of Technology** in **Electrical Engineering**, is a bona fide record of the work done by him under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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ABSTRACT

KEYWORDS: AlGaN/GaN HEMT; Cutoff Frequency; High Frequency; Low Noise Amplification; Maximum Oscillation Frequency; Microwave Frequency; Performance Parameters; Wide Bandgap

An AlGaN/GaN HEMT structure is designed for high frequency low noise applications and its performance parameters are calculated. The designed structure has $150\ nm$ long T-shaped gate, $20\ nm$ thick AlGaN barrier layer having 18% aluminum content, $3\ nm$ thick AlGaN spacer along with $2\ \mu m$ thick GaN channel layer on sapphire substrate. Calculated figures of merit of the device show excellent DC characteristics with maximum drain current density of $1.22\ A/mm$ and maximum transconductance of $310\ mS/mm$ and good RF performance with current gain cutoff frequency, $f_T = 60.66\ GHz$ and maximum oscillation frequency, $f_{max} = 126.95\ GHz$. Noise analysis of the device is also presented to quantify the background noise produced while operating. An excellent noise figure of 0.36 dB at 10 GHz confirms the usefulness of the device for low noise applications.

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ABBREVIATIONS

2-DEG	Two-Dimensional Electron Gas
AlGaN	Aluminum Gallium Nitride
AlGaAs	Aluminum Gallium Arsenide
AlN	Aluminum Nitride
DC	Direct Current
FET	Field Effect Transistor
GaN	Gallium Nitride
GaAs	Gallium Arsenide
HEMT	High Electron Mobility Transistor
InP	Indium Phosphide
MMIC	Monolithic Microwave Integrated Circuit
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MODFET	MOdulation Doped Field Effect Transistor
NF	Noise Figure
RF	Radio Frequency
SCE	Short Channel Effect
SNR	Signal to Noise Ratio
Si	Silicon
SiC	Silicon Carbide
UID	UnIntentionally Doped

NOTATION

μ	Electron Mobility
ϵ_r	Dielectric constant
E_g	Electronic Bandgap
E_c	Electric Breakdown Field
v_{sat}	Saturation Velocity
χ	Thermal Conductivity
D	Density of States
E_f	Fermi Level
f_T	Current Gain Cutoff Frequency
f_{max}	Maximum Oscillation Frequency
L_g	Gate Length
L_{gs}	Gate-Source Length
L_{ds}	Drain-Source Length
I_{max}	Maximum Drain Current Density
$I_{d,max}$	Maximum Drain Current
V_T	Threshold Voltage
g_m	Peak Transconductance
ϕ_B	Schottky Gate Barrier Height
ΔE_C	Discontinuity of Conduction Band
N_D	Doping Concentration of Barrier Layer
d_d	Thickness of Barrier Layer
ϵ	Permittivity of Barrier Layer
d_i	Thickness of Spacer Layer
σ	Polarization Induced Charge Density
g_m	Maximum Transconductance
q	Electronic Charge
k	Boltzmann Constant
V_d	Drain Voltage
SCE_p	Short Channel Effect Parameter
P_{PE}	Piezoelectric Polarization Induced Charge Density
P_{SP}	Spontaneous Polarization Induced Charge Density
C_g	Gate Capacitance
C_{gs}	Gate-Source Capacitance
C_{gd}	Gate-Drain Capacitance
V_g	Gate Voltage
V_{br}	Breakdown Voltage
n_s	2-DEG Carrier Density
R_s	Source Resistance
R_d	Drain Resistance
R_g	Gate Resistance
R_{ds}	Output Resistance

C_{par}	Parasitic Pad Capacitance
τ_T	Transit Time
V_{th}	Thermal Voltage
λ	Channel Length Modulation Parameter
Z	Gate Width

CHAPTER 1

INTRODUCTION

Silicon has been the preferred material for fabrication of solid state devices since the demonstration of first silicon transistor by Gordon Teal in 1954. It has been the dominant semiconductor of choice for a plethora of applications including high-voltage switching applications. But the intrinsic material properties of silicon such as low saturation velocity, low breakdown voltage, low inversion layer mobility and high device resistance impose limits on its use for high power and high frequency applications. Due to these intrinsic limits of silicon, there is growing interest towards new materials which can overcome these limitations and can operate at higher power levels and higher frequencies. Gallium Nitride (GaN), a wide bandgap semiconductor, is a promising material for meeting the requirements to operate at high temperature and high frequencies.

Table 1.1 shows the values of the fundamental material properties of GaN and competing semiconductor materials [1]. Due to its superior physical properties including wide bandgap, high breakdown electric field, high electron saturation velocity and high density of carriers in the form of two-dimensional electron gas (2-DEG) with high mobility, GaN is considered an outstanding material for high-frequency and high-power devices.

Table 1.1: Properties of GaN and competing semiconductor materials [1].

Property	**GaN**	**Si**	**GaAs**	**SiC**	**InP**
$Electron\ Mobility,\ \mu\ (cm^2V^{-1}s^{-1})$	2000	1300	5000	260	5400
$Dielectric\ Constant,\ \epsilon_r$	9.7	11.4	13.1	9.5	12.5
$Bandgap,\ E_g\ (eV)$	3.4	1.1	1.4	2.9	1.35
$Electric\ Breakdown\ Field,\ E_c\ (kV/cm)$	3300	300	400	2500	500
$Saturation\ Velocity,\ v_{sat}\ (\times 10^7 cm/s)$	2.2	1	1	2	1
$Thermal\ Conductivity,\ \chi\ (W/cmK)$	1.3	1.5	0.46	4.9	0.7

1.1 High Electron Mobility Transistor

High frequency low noise applications demand faster field effect transistors which produce less background noise. Millimeter wave region of the electromagnetic spectrum corresponding to the frequencies in the range of $3\ GHz$ to $300\ GHz$ is regarded as the high frequency region. Cellular phones, satellite television receiver, RADAR equipments operate at high frequencies and require low noise amplifiers that amplifies a very low power signal without significantly degrading its signal to noise ratio. Hence, there is a need to make small size FETs with high saturation current and transconductance so that charging and discharging times of the circuit capacitances reduce. This can be achieved by highest possible doping compatible with other device parameters. Since the doping impurities and charge carriers share the same space in the channel of a conventional FET such as MOSFET, the transport properties such as mobility and saturation velocity are impaired due to ionized impurity scattering.

High Electron Mobility Transistors (HEMTs) overcome this limitation by separating charge carriers from doping impurities. A typical structure of a HEMT device is shown in Fig. 1.1. Charge carriers are accumulated at the interface of undoped small bandgap semiconductor material (GaN or GaAs) and wide bandgap semiconductor material (AlGaN or AlGaAs). In modulation doped heterostructures only wide bandgap semiconductor is doped and the channel of charge carriers is free of any doping impurities.

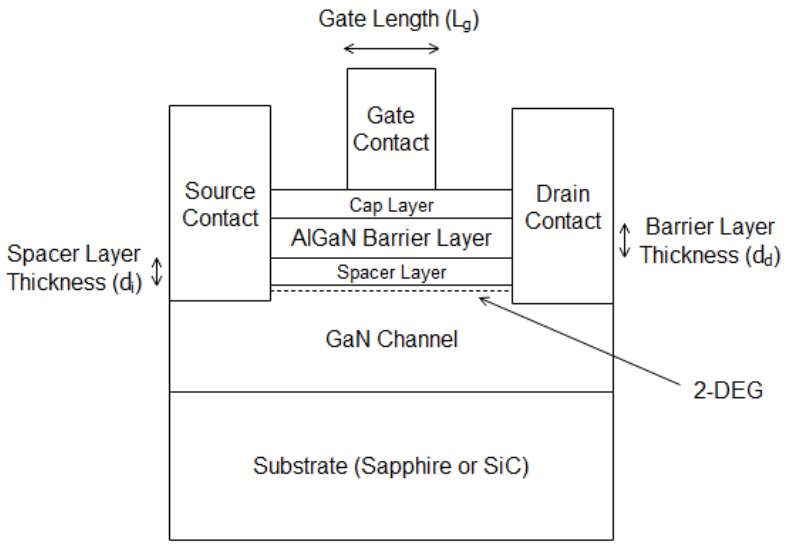

Figure 1.1: Typical structure of High Electron Mobility Transistor.

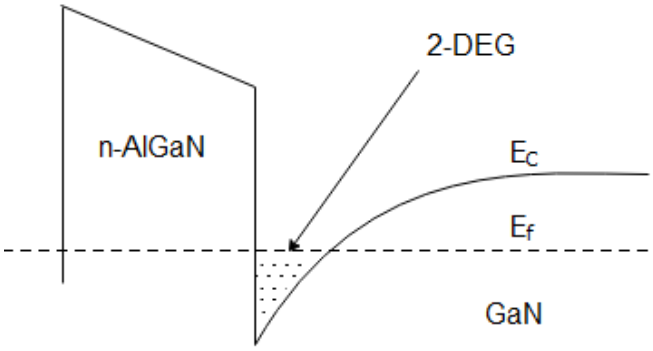

Figure 1.2: Conduction band profile of heterostructure of n-type doped AlGaN and unintentionally doped GaN showing the formation of the 2-DEG in the potential well.

As shown in Fig. 1.2, electrons get trapped in the potential well formed at the interface of two different bandgap semiconductor materials. Since, the movement of these electrons is limited to two directions it is also called two dimensional electron gas or 2-DEG.

1.2 Performance Specifications of AlGaN/GaN HEMT

In this work, an AlGaN/GaN HEMT is designed to meet certain performance specifications listed in Table 1.2. Meaning of each performance parameter is explained in Chapter 2. Various device parameters such as gate length, barrier layer doping, barrier layer thickness, mole fraction of aluminum in barrier layer, etc. as summarized in Table 1.3 are optimized to meet the required performance specifications.

Table 1.2: Required performance specifications of AlGaN/GaN HEMT.

Performance Parameter	**Value**
$I_{max}(mA/mm)\ at\ V_g = 0\ V\ and\ V_d = 28\ V$	1000
$V_T(-V)$	3.5-4
$g_{m,max}(mS/mm)$	300-320
$f_T(GHz)$	>60
$f_{max}(GHz)$	>70
$Power(W/mm)$	4-5

Table 1.3: Device parameters to be optimised to meet specifications.

Device Parameter	**Symbol**
$Gate\ Length$	L_g
$Barrier\ Layer\ Thickness$	d_d
$Barrier\ Layer\ Mole\ Fraction$	x
$Barrier\ Layer\ Doping$	N_D
$Spacer\ Layer\ Thicness$	d_i
$Gate\ Width$	Z

1.3 Organisation of the thesis

Chapter 2 expounds the specifications, various reported AlGaN/GaN HEMT devices and the variation of important performance parameters with device parameters.

Chapter 3 gives design of AlGaN/GaN HEMT and shows calculations of its performance parameters along with noise analysis.

Chapter 4 contains the conclusion of the work.

CHAPTER 2

REVIEW

2.1 Device Specifications

Device specifications include both DC and RF performance parameters of the device.

2.1.1 DC Parameters

DC parameters of the device include the performance parameters such as maximum drain current, maximum transconductance, threshold voltage and power.

Maximum Drain Current ($I_{d,max}$)

Maximum drain current is obtained by biasing the device such that transistor operates in velocity saturation region. Fig. 2.1 and Fig. 2.2 show the variation of drain current with gate voltage and drain-source voltage respectively.

Maximum Transconductance ($g_{m,max}$)

Transconductance (g_m) of a transistor is defined as the change in its drain current per unit change in its gate voltage. Figure 2.1 shows the typical variation in transconductance with the gate voltage of a HEMT.

Threshold Voltage (V_T)

Threshold voltage of a transistor is the value of the gate voltage below which the transistor is off. Hence it is also represented by V_{off}.

Figure 2.2 shows the typical variation of drain current with drain to source voltage of a HEMT. It also shows the value of gate voltage below which there is negligible current marked as V_T.

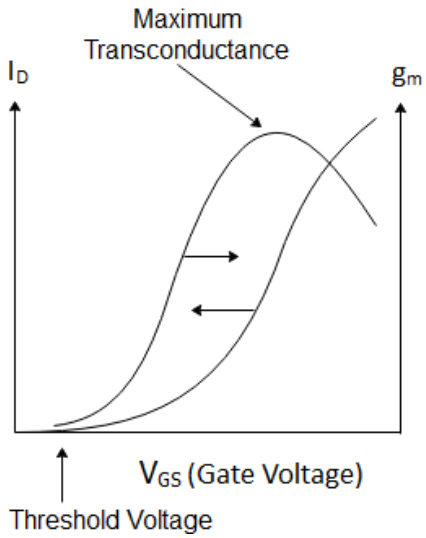

Figure 2.1: Graph showing the typical variation of drain current and transconductance with gate voltage of a HEMT along with the threshold voltage.

2.1.2 RF Parameters

Radio Frequency (RF) parameters of a HEMT include current gain cutoff frequency (f_T) and maximum oscillation frequency (f_{max}). They are used to characterize the device for high frequency applications.

Current Gain Cutoff Frequency (f_T)

Current gain cutoff frequency is defined as the operating frequency of the transistor at which the short-circuit small signal current gain of the transistor becomes unity.

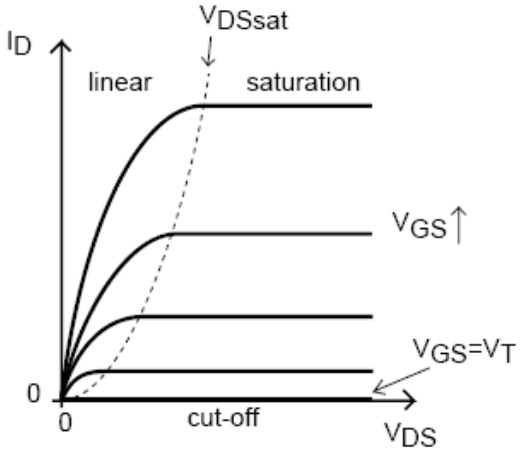

Figure 2.2: Graph showing the typical variation of drain current with drain to source voltage of a HEMT along with the threshold voltage.

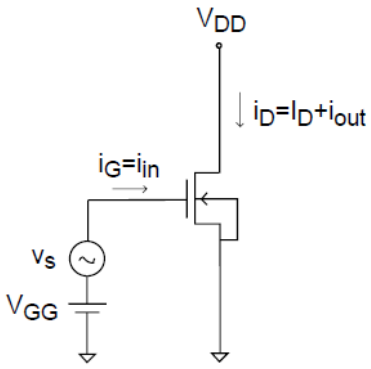

Figure 2.3: Circuit Diagram showing the effect of small signal voltage (v_s) superimposed on the DC bias of an AlGaN/GaN HEMT.

As shown in Fig. 2.3, when a small signal voltage (v_s) is applied over the DC bias of gate of the transistor, small signal drain current (i_{out}) flows due to the transistor effect. Small signal input gate current (i_{in}) also flows into the gate terminal of the device due gate capacitance. Hence, the small signal current gain of the transistor at any frequency f can be written as

$$Current\ Gain = \left| \frac{i_{out}}{i_{in}} \right| \tag{2.1}$$

As operating frequency of transistor increases, the reactance due to gate capacitance decreases leading to increase in small signal input current (i_{in}). But the small signal output current (i_{out}) due to the effect of transistor does not change with the operating frequency. Therefore, the ratio of i_{out} and i_{in} or current gain decreases with increase in frequency. At some high enough frequency, current gain drops to unity and this frequency is termed as current gain cutoff frequency (f_T)

Maximum Oscillation Frequency (f_{max})

Maximum oscillation frequency is defined as the frequency at which the maximum unilateral power gain is unity.

2.2 Existing device structures and their performance

One of the earliest work on gallium nitride based HEMTs was reported by Khan et al. [2]. The device had a gate length of $0.25\ \mu m$ and gate width of $150\ \mu m$. Barrier

thickness of $Al_{0.13}Ga_{0.87}N$ layer was $25\ nm$ with a doping level of $3.5-4\times10^{18}\ cm^{-3}$. Unintentionally doped GaN layer had a thickness of $0.6\ \mu m$. The device had a threshold voltage of -2V, maximum drain current of $27\ mA/mm$ and maximum transconductance of $27\ mS/mm$. The current gain cutoff frequency was reported to be $11\ GHz$ along with maximum oscillation frequency of $35\ GHz$. Clearly, these performance parameters of the device are well short of the required values given in Table 1.2.

More recent works show excellent DC and RF performance due to scaled device geometry and better fabrication technology which reduces parasitic resistances and capacitances. For example, Chung et al. [3] combined low damage gate-recess technology, scaled device geometry and recessed source and drain ohmic contacts to simultaneously enable minimum short-channel effects and very low parasitic resistances. They achieved a maximum oscillation frequency (f_{max}) of $300\ GHz$ and current gain cutoff frequency (f_T) of $70\ GHz$ for $60\ nm$ gate length device. Maximum drain current of $1.2\ A/mm$ along with maximum transconductance of $410\ mS/mm$ was obtained. Threshold voltage of the device was observed to be -2V. These values of the performance parameters are better than the required values, but the gate length of $60\ nm$ is difficult to fabricate.

Another device reported by Bouzid-Driad et al. [4] showed excellent RF performance characteristics. They were able to obtain $f_T = 100\ GHz$ and $f_{max} = 206\ GHz$ along with maximum transconductance of $440\ mS/mm$ for a $90\ nm$ T-shaped gate length AlGaN/GaN HEMT on silicon substrate. The maximum drain current density of $820\ mA/mm$ was achieved with a threshold voltage of -2.7 V.

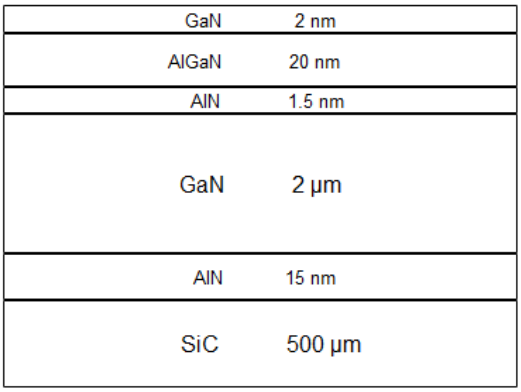

Figure 2.4: Epitaxial layers of AlGaN/GaN HEMT reported by Durmus et al.

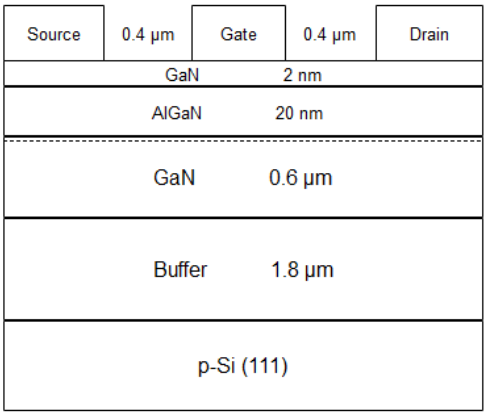

Figure 2.5: AlGaN/GaN HEMT structure reported by Christy et al.

Durmus et al. [5] reported a $100\ nm$ T-shaped gate length AlGaN/GaN HEMT on SiC. The epitaxial layers of the fabricated device is shown in Fig. 2.4. Mole fraction of aluminum in the AlGaN barrier layer was 0.22. They reported the maximum current gain cutoff frequency of $100\ GHz$ and maximum oscillation frequency of $128\ GHz$. Maximum transconductance of $300\ mS/mm$ was achieved.

Another $100\ nm$ gate length AlGaN/GaN HEMT on high resistive silicon substrate was reported by Christy et al. [6]. They achieved good DC characteristics with maximum drain current density of $0.6\ A/mm$ and transconductance of $157\ mS/mm$. RF performance of the device was excellent. Current gain cutoff frequency of $90\ GHz$ and peak maximum oscillation frequency of $150\ GHz$ was achieved. The device structure fabricated is shown in Fig. 2.5.

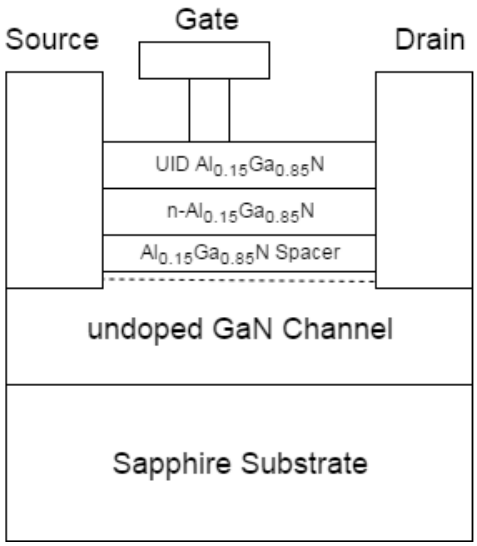

Figure 2.6: AlGaN/GaN HEMT structure reported by Nguyen et al.

Nguyen et al. [7] reported a robust $150\ nm$ gate length AlGaN/GaN MODFET. A $2\ \mu m$ thick unintentionally doped GaN channel layer was grown on sapphire substrate followed by $3\ nm$ $Al_{0.15}Ga_{0.85}N$ spacer layer and $20\ nm$ thick barrier layer of $Al_{0.15}Ga_{0.85}N$ doped at $1 - 2 \times 10^{18}\ cm^{-3}$. The device was capped by an unintentionally doped $15\ nm$ thick $Al_{0.15}Ga_{0.85}N$ layer to protect it.

Figure 2.6 shows the structure of the device reported by Nguyen et al. [7]. They were able to achieve excellent gate-drain breakdown voltage of the device of 68 V making it highly robust for high power applications. They also reported an impressive noise figure of 0.6 dB which ensures that the device doesn't produce much background noise when employed for low noise applications.

Device exhibited excellent DC characteristics by delivering maximum current density of $1.25\ A/mm$ and a peak transconductance of $300\ mS/mm$. RF performance of the device was also good and a maximum current gain cutoff frequency $f_T = 50\ GHz$ was observed along with maximum oscillation frequency of $100\ GHz$. The threshold voltage of the device was -4 V. These performance parameters are very close to the required specifications listed in Table 1.2 and therefore this device is used as a guideline while designing the structure of the AlGaN/GaN HEMT.

2.3 Parameters affecting device performance

While designing a device, it is important to understand how various parameters affect its electrical characteristics so as to come up with the optimised structure that can meet the desired specifications. One of the important factor that influences both DC and RF characteristics of a device is its gate length. Other parameters such as barrier doping, gate-source and gate-drain spacing, surface states also affect the performance of the device.

2.3.1 Effect of gate length

Gate length is an important device parameter that affects the electrical characteristics of a device. Drain current increases with decreasing channel length of the device as the charge carriers have to travel less distance. Christy et al. [6] showed the dependence of

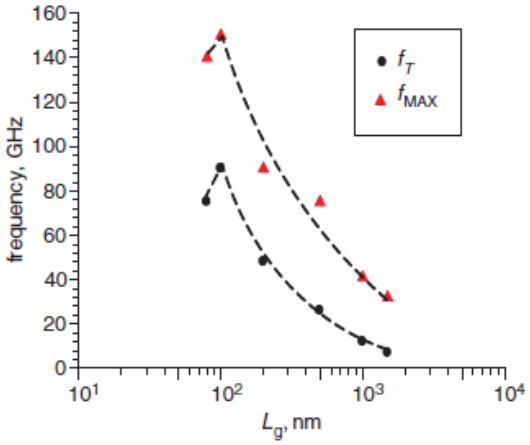

Figure 2.7: Graph showing the dependence of f_T/f_{max} on gate length for AlGaN/GaN HEMTs reproduced from Christy et al.

cutoff frequency on gate length as depicted in Fig. 2.7. It is clear from that current gain cutoff frequency increases when gate length decreases because transit time of charge carriers reduces. Since maximum oscillation frequency directly depends on current gain cutoff frequency, f_{max} is more for short channel devices. Also, Fig. 2.7 shows that f_T/f_{max} reduces for the shortest gate lenghts. This can be attributed to the increased gate resistances at smaller gate lengths.

2.3.2 Effect of doping

Marso et al. [8] investigated the effect of carrier supply doping on the electrical properties of AlGaN/GaN HEMTs. They fabricated both undoped and modulation doped AlGaN/GaN HEMTs. Two different modulation doped HEMTs were fabricated with barrier layer doping levels of $2 \times 10^{18}\ cm^{-3}$ and $5 \times 10^{18}\ cm^{-3}$. They reported an improvement in the DC performance of HEMTs when the barrier layer was doped. However, when the doping level of the barrier layer was too high ($5 \times 10^{18}\ cm^{-3}$) , RF characteristics of the HEMT degraded due to reduction of saturation velocity of the charge carriers leading to increase in transit time.

2.3.3 Effect of access regions

The ungated regions between gate-source and gate-drain of a transistor are called access regions. Length of these access regions affects the RF performance and breakdown volt-

Table 2.1: RF performance of AlGaN/GaN HEMT against L_{gs} and L_{ds}.

	$f_T - f_{max}(GHz)$		
$L_{gs}(\mu m)$ $L_{ds}(\mu m)$	1.5	2	2.5
0.25	80-153	80-146	80-136
0.5	79-150	79-143	79-131
0.75	80-149	79-140	79-130

age of HEMTs, therefore positioning of gate has to be optimised for better performance of the transistor. Bouzid et al. [9] fabricated $105\ nm$ T-shaped gate length devices having different gate-source (L_{gs}) and drain-source (L_{ds}) spacing to study their influence on the electrical device characteristics. The results are summarized in Table 2.1.

It is clear from the Table 2.1 that the RF performance is best for the device having $L_{gs} = 0.25\ \mu m$ and $L_{ds} = 1.5\ \mu m$. This also shows that RF performance is best when the gate is placed asymmetrically.

2.4 Objectives of the work

The objectives of the work include finding the values of device parameter listed in Table 1.3 to meet the required performance specifications given in Table 1.2 along with the noise analysis of the transistor to ascertain that it doesn't produce much background noise when operating at high frequencies.

CHAPTER 3

DEVICE DESIGN

In this chapter, Gallium Nitride based High Electron Mobility Transistor (HEMT) is designed. The device is meant to be used for low noise amplification in millimeter wave frequency regime. The structure of the transistor is optimized to meet the required specifications given in Table 1.2.

3.1 Calibration of models used for calculations

The analytical models used in this work for calculating various figures of merit of the designed AlGaN/GaN HEMT were calibrated using the device reported by Nguyen et al. [7]. The calculated values and measured values of the performance parameters are in good agreement as shown in Table. 3.1.

Note: Doping value of AlGaN barrier layer is taken as $1.2 \times 10^{18}\ cm^{-3}$. Threshold voltage calculation incorporates short channel effect at $V_d = 28\ V$ using the short channel effect parameter, $SCE_p = 25$. Also, the value of parasitic pad capacitances is taken as 90 fF.

Table 3.1: Table showing the measured and calculated values of the AlGaN/GaN HEMT reported by Nguyen et al [7].

Performance Parameter	**Measured value by Nguyen et al.**	**Calculated value**
$I_{max}(mA/mm)\ at\ V_g = 0\ V\ and\ V_d = 28\ V$	1250	1257
$V_T(-V)$	4	4.03
$g_{m,max}(mS/mm)$	300	311
$f_T(GHz)$	50	51
f_{max}	100	108

3.2 AlGaN/GaN HEMT with 0.15 μm gate length

Nguyen et al. [7] demonstrated a high performance 0.15 μm gate length AlGaN/GaN MODFET. They achieved very low noise figure and high gate-drain breakdown voltage ideal for low noise amplifiers operating at high power. The device also exhibited various parameters close to the required specifications in Table 1.2. However, the current gain cutoff frequency (f_T) of the device is less than the required value. Based on the device reported by Nguyen et al. [7], a device structure of AlGaN/GaN HEMT is designed and its various performance parameters are calculated.

3.2.1 Device Structure

The device designed is shown in Fig. 3.1. The T-shaped gate of the device is $0.15\ \mu m$ long. $2\ \mu m$ undoped GaN channel is present on a sapphire substrate. Thickness of the $Al_{0.18}Ga_{0.82}N$ barrier layer is $20\ nm$. The barrier has a doping of 2×10^{18} cm^{-3}. $Al_{0.18}Ga_{0.82}N$ spacer layer of $3\ nm$ is present between the channel and the barrier. The device is capped with a $15\ nm$ thick unintentionally doped $Al_{0.18}Ga_{0.82}N$ layer. Source to drain spacing is $2\ \mu m$ and the gate is placed closer to the source than to the drain to decrease the gate-source access resistance and to increase the gate-drain breakdown voltage.

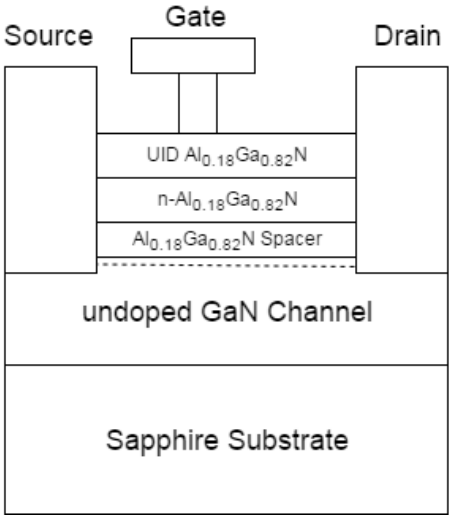

Figure 3.1: Designed device structure of AlGaN/GaN HEMT for high frequency low noise applications.

3.3 Performance Parameter Calculations

In this section, performance parameters listed in Table 1.2 are calculated for the designed device.

3.3.1 Threshold Voltage (V_T)

For the gallium nitride based high electron mobility transistor, the threshold voltage is given by [10]

$$V_T = \phi_B - \Delta E_C - \frac{qN_D d_d^2}{2\epsilon} - \frac{\sigma}{\epsilon}(d_d + d_i) \tag{3.1}$$

where ϕ_B is the barrier height of the Schottky gate, ΔE_C is the discontinuity of the conduction band at the interface between the AlGaN-GaN layers, ϵ is the permittivity of the barrier layer, N_D and d_d are the doping concentration and thickness of n-AlGaN layer respectively, d_i is the spacer layer thickness and σ is the polarization induced charge density at the interface. For the short channel device, short channel effect is incorporated by introducing a shift to the offset voltage ΔV_T as shown by Cheng and Wang [11].

$$V_{T,SCE} = V_T - \frac{V_d}{SCE_p} \tag{3.2}$$

where $V_{T,SCE}$ is the threshold voltage when short channel effect occurs and SCE_p is the short channel effect parameter determined from measurement data.

Barrier height follows linear dependence with the aluminum content in the barrier as [12]

$$\phi_B = 0.91 + 2.44x\ V \tag{3.3}$$

Brunner et al. [13] showed the dependence of band gap of AlGaN on its aluminum content as

$$E_{Al_xGa_{1-x}N} = 3.42 + 1.41x + 1.3x^2\ eV \tag{3.4}$$

From this, the discontinuity of the conduction band can be obtained as [14]

$$\Delta E_C = 0.7[E_{Al_xGa_{1-x}N} - E_{GaN}] \tag{3.5}$$

Static dielectric constant of AlGaN depends on aluminum mole fraction as [15].

$$\epsilon_s(x) = 9.7 - 1.2x \tag{3.6}$$

Spontaneous and piezoelectric polarization contribute to the polarization induced charge density (σ) at the interface of AlGaN and GaN as shown by Ambacher et al. [16].

$$|\sigma(x)| = |P_{PE}(Al_xGa_{1-x}N) + P_{SP}(Al_xGa_{1-x}N) - P_{SP}(GaN)| \tag{3.7}$$

where $P_{PE}(Al_xGa_{1-x}N)$ is the piezoelectric polarization in AlGaN given by

$$P_{PE}(Al_xGa_{1-x}N) = 2\frac{a(0) - a(x)}{a(x)}\left\{e_{31}(x) - e_{33}(x)\frac{C_{13}(x)}{C_{33}(x)}\right\} \tag{3.8}$$

where $a(x)$ is the lattice constant obtained by linear interpolation between the physical properties of AlN and GaN, given by

$$a(x) = (-0.077x + 3.189)10^{-10}\ m, \tag{3.9}$$

similarly, elastic constants:

$$\begin{aligned} C_{13}(x) &= (5x + 103)\ GPa, \\ C_{33}(x) &= (-32x + 405)\ GPa, \end{aligned} \tag{3.10}$$

piezoelectric constants:

$$\begin{aligned} e_{31}(x) &= (-0.11x - 0.49)\ C/m^2, \\ e_{33}(x) &= (0.73x + 0.73)\ C/m^2, \end{aligned} \tag{3.11}$$

Spontaneous polarization is given by

$$P_{SP}(Al_xGa_{1-x}N) = (-0.052x - 0.029)\ C/m^2 \tag{3.12}$$

Now, substituting $x = 0.18$ in Eqs. 3.9 to 3.12 and using them in Eq. 3.8, we get

$$\begin{aligned} P_{PE}(Al_{0.18}Ga_{0.82}N) &= -64 \times 10^{-4}\ C/m^2 \\ P_{SP}(Al_{0.18}Ga_{0.82}N) &= -384 \times 10^{-4}\ C/m^2 \end{aligned} \tag{3.13}$$

On substituting the value of Eq. 3.13 in Eq. 3.7, we get

$$|\sigma(0.18)| = 1.58 \times 10^{-2}\ C/m^2 \tag{3.14}$$

Using the Eqs. 3.3 to 3.6 and Eq. 3.14 in Eq. 3.1 with $N_D = 2\times10^{18}\ cm^{-3}$, $d_d = 20\ nm$ and $d_i = 3\ nm$ we get,

$$\mathbf{V_T = -3.94\ V}$$

which meets our required specification.

3.3.2 Maximum Drain Current ($\mathbf{I}_{d,max}$)

Drain current of a transistor operating in velocity saturation region is given by [17]

$$I_{d,max} = ZQ_n v_{sat} \tag{3.15}$$

where Z is gate width, Q_n is total charge in the channel and v_{sat} is saturation velocity of charge carriers in the channel.

Charge in the channel (Q_n) can be written as

$$Q_n = qn_s = C_g(V_g - V_T) \tag{3.16}$$

where C_g is the gate capacitance given by

$$C_g = \frac{\epsilon}{d_d + d_i} \tag{3.17}$$

so, $I_{d,max}$ can be written as

$$I_{d,max} = Z\frac{\epsilon}{d_d + d_i}(V_g - V_T)v_{sat} \tag{3.18}$$

saturation velocity of the device with barrier doping of $2 \times 10^{18}\ cm^{-3}$ is $0.85 \times 10^{5}\ m/s$ as shown by Marso et al. [8], on substuting the values of parameters in Eq. 3.18, we get

$$\mathbf{I_{d,max} = 0.244\ A}$$

To get drain current per mm width of device, divide $I_{d,max}$ by 0.2 since the width of the device is $0.2mm$, we get

$$\mathbf{I_{max} = 1.22\ A/mm}$$

which is the required value of drain current.

3.3.3 Transconductance ($\mathbf{g}_m$)

Transconductance can be written as

$$g_m = \frac{dI_d}{dV_g} \tag{3.19}$$

Maximum transconductance is achieved when transistor operates in velocity saturation region and can be calculated as [17]

$$g_{m,max} = ZC_g v_{sat} \tag{3.20}$$

where C_g is given by Eq. 3.17. On substituting the values and dividing by Z, transconductance per unit width is

$$\mathbf{g_{m,max} = 310\ mS/mm}$$

which meets the required specified value.

3.3.4 Current Gain Cutoff Frequency (f_T)

The frequency at which the small signal current gain of the transistor given by Eq. 3.21 becomes unity is called f_T.

$$Current\ Gain = h_{21} = \frac{i_{out}}{i_{in}} \tag{3.21}$$

Small Signal Treatment of HEMT to calculate f_T

In Fig. 3.2, v_s is the small signal voltage applied on top of the DC bias, i_{in} is small signal current that flows into gate terminal, v_{gs} is the small signal voltage across the gate-source capacitance (C_{gs}) and v_{bs} is the small signal voltage across the source-bulk capacitance (C_{sb}). C_{gd} and C_{db} are gate-drain capacitance and drain-bulk capacitance respectively, g_m and g_{mb} are the transconductances of the transistor with respect to gate and bulk respectively, r_o is output resistance and i_{out} is the output current flowing due to transistor effect. When v_{bs}, small signal voltage across source-bulk capacitance (C_{sb}), is zero, the small signal model reduces to as shown in Fig. 3.3

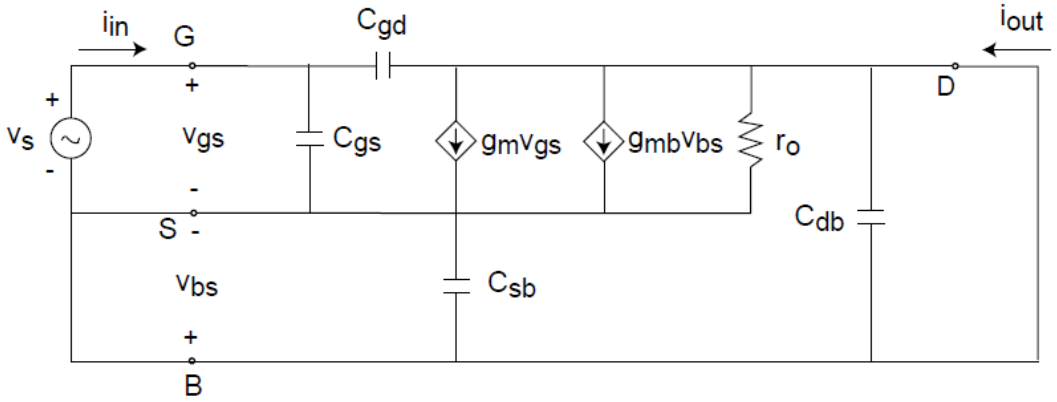

Figure 3.2: Small-signal model of HEMT in saturation including parasitic capacitances.

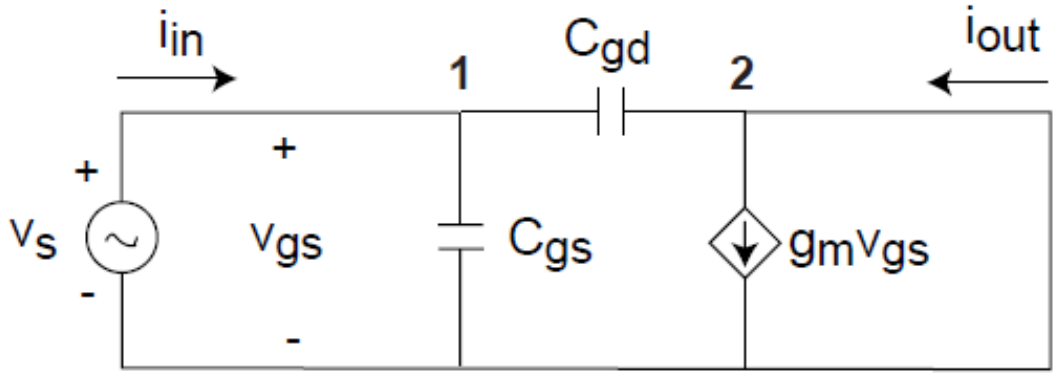

Figure 3.3: Small-signal model of HEMT in saturation with $V_{bs} = 0$. When small signal voltage v_s is applied to the input gate terminal, a small signal input current i_{in} flows into the gate terminal due to gate capacitance. Also, i_{out} is the small signal output current flowing due to transistor action.

Applying Kirchoff's current law at node 1, we get

$$i_{in} - v_{gs} j\omega C_{gs} - v_{gs} j\omega C_{gd} = 0$$

or,

$$i_{in} = v_{gs} j\omega (C_{gs} + C_{gd}) \tag{3.22}$$

Applying Kirchoff's current law at node 2, we get

$$i_{out} - g_m v_{gs} + v_{gs} j\omega C_{gd} = 0$$

or,

$$i_{out} = v_{gs} (g_m - j\omega C_{gd}) \tag{3.23}$$

from Eq. 3.22 and Eq. 3.23, small signal current gain (h_{21}) can be written as

$$h_{21} = \frac{i_{out}}{i_{in}} = \frac{g_m - j\omega C_{gd}}{j\omega (C_{gs} + C_{gd})} \tag{3.24}$$

so, magnitude of the current gain (h_{21}) is

$$|h_{21}| = \frac{\sqrt{g_m^2 + \omega^2 C_{gd}^2}}{\omega (C_{gs} + C_{gd})} \tag{3.25}$$

Magnitude of small signal current gain (h_{21}) becomes unity at

$$\omega_T = 2\pi f_T = \frac{g_m}{C_{gs} + C_{gd}} \tag{3.26}$$

so, current gain cutoff frequency (f_T) is given by

$$\mathbf{f_T} = \frac{\mathbf{g_m}}{\mathbf{2}\pi(\mathbf{C_{gs}} + \mathbf{C_{gd}})} \tag{3.27}$$

Physical Interpretation of f_T

Current gain cutoff frequency is a commonly used metric to determine the performance of a device. It is also known as transit frequency as it can be related to the reciprocal of the transit time (τ_T) of charge carriers in the channel. Therefore, it provides an estimate of the speed of the device. It gives the highest frequency at which the device can be

operated.

Consider

$$\frac{1}{2\pi f_T} = \frac{C_{gs} + C_{gd}}{g_m} \tag{3.28}$$

Gate-drain capacitance and gate-source capacitance contribute to the total gate capacitance of a transistor, therefore sum of C_{gs} and C_{gd} can be written as $L_g Z C_g$

$$\frac{1}{2\pi f_T} = \frac{L_g Z C_g}{g_m} \tag{3.29}$$

where L_g is gate length and Z is gate width of the transistor. Substituting $g_m = Z C_g v_{sat}$ in above equation, we get

$$\frac{1}{2\pi f_T} = \frac{L_g Z C_g}{Z C_g v_{sat}} \tag{3.30}$$

or,

$$\frac{1}{2\pi f_T} = \frac{L_g}{v_{sat}} \tag{3.31}$$

since, L_g is the channel length and v_{sat} is the saturation velocity of charge carriers in the channel, we get

$$\frac{1}{2\pi f_T} = \tau_T \tag{3.32}$$

where τ_T is the transit time of charge carriers from source to drain.

So, f_T gives an idea of the intrinsic delay of the transistor and is a good first-order figure of merit for frequency response.

Calculation of Gate-Source and Gate-Drain Capacitances

To calculate the current gain cutoff frequency of the transistor, we need to calculate gate-source and gate-drain capacitances as is clear from Eq. 3.27. Yigletu et al. [18] developed a compact charge based model for capacitances of AlGaN/GaN HEMTs.

Charge density per unit area accumulated in the potential well formed at the interface of heterostructure of AlGaN/GaN can be calculated with the assumption of a quasi-constant electric field in the potential well and two subbands as [19]

$$n_s = DV_{th}\left[\ln\left(e^{(E_f - E_0/V_{th})} + 1\right) + \ln\left(e^{(E_f - E_1/V_{th})} + 1\right)\right] \tag{3.33}$$

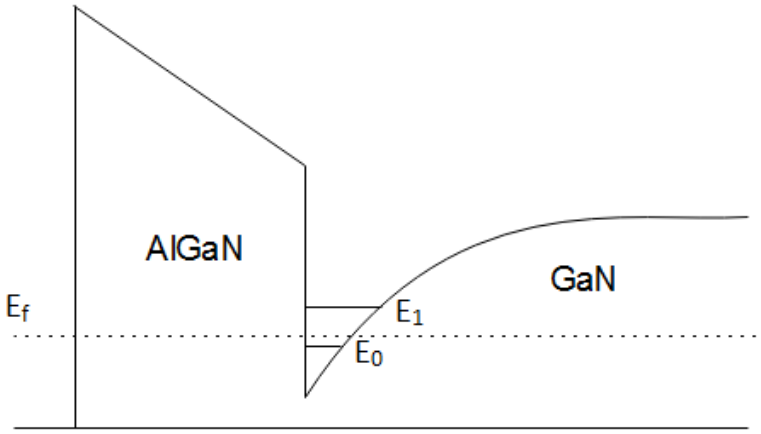

Figure 3.4: Conduction band profile of AlGaN/GaN HEMT showing the position of two subbands relative to the fermi level in the potential well formed at the interface of the heterostructure.

As shown in Fig. 3.4, the second energy level represented by E_1 is well above the Fermi level for the whole operating range of the gate voltage. Hence, the contribution due to second energy level can be neglected. So, the above equation reduces to

$$n_s = DV_{th}\left[\ln\left(e^{(E_f - E_0/V_{th})} + 1\right)\right] \tag{3.34}$$

where D is the density of states and V_{th} is the thermal voltage at the operating temperature of the device.

The subband E_0 is given by [20]

$$E_0 = \gamma_0 n_s^{2/3} \tag{3.35}$$

where $\gamma_0 = 2.5 \times 10^{-12}\ Vm^{4/3}$ [19].

When the entire barrier layer of AlGaN gets depleted, the density of charge carriers is given by [21]

$$n_s = \frac{\epsilon}{qd_d}(V_g - V_T - E_f) \tag{3.36}$$

on substituting the value of E_0 from Eq. 3.35 and the value of E_f from Eq. 3.36 in the Eq. 3.34, we get

$$V_g - V_T = \frac{qd_d n_s}{\epsilon} + \gamma_0 n_s^{2/3} + V_{th}\ln\left[\exp\left(\frac{n_s}{DV_{th}}\right) - 1\right] \tag{3.37}$$

on expanding the exponential term in eq. 3.37 and considering only first two terms, we can write Eq. 3.37 as

$$V_g - V_T = \frac{qd_d n_s}{\epsilon} + \gamma_0 n_s^{2/3} + V_{th} \ln\left(\frac{n_s}{DV_{th}}\right) \tag{3.38}$$

considering V as the local quasi-Fermi potential, Eq. 3.38 can be written as

$$V_g - V_T - V = \frac{qd_d n_s}{\epsilon} + \gamma_0 n_s^{2/3} + V_{th} \ln\left(\frac{n_s}{DV_{th}}\right) \tag{3.39}$$

on differentiating Eq. 3.39, we get

$$dV = -\left(\frac{qd_d}{\epsilon} + \frac{2}{3}\gamma_0 n_s^{-1/3} + V_{th} n_s^{-1}\right) dn_s \tag{3.40}$$

Also, drain current in the channel can be written as

$$I_d = Z\mu q n_s \frac{dV}{dx} \tag{3.41}$$

where μ is the mobility of charge carriers in the channel.

We know that the capacitance is change in charge per unit change in voltage. Similarly, gate-source capacitance is defined as the change in gate charge per unit change in the source voltage and gate-drain capacitance is defined as the change in gate charge

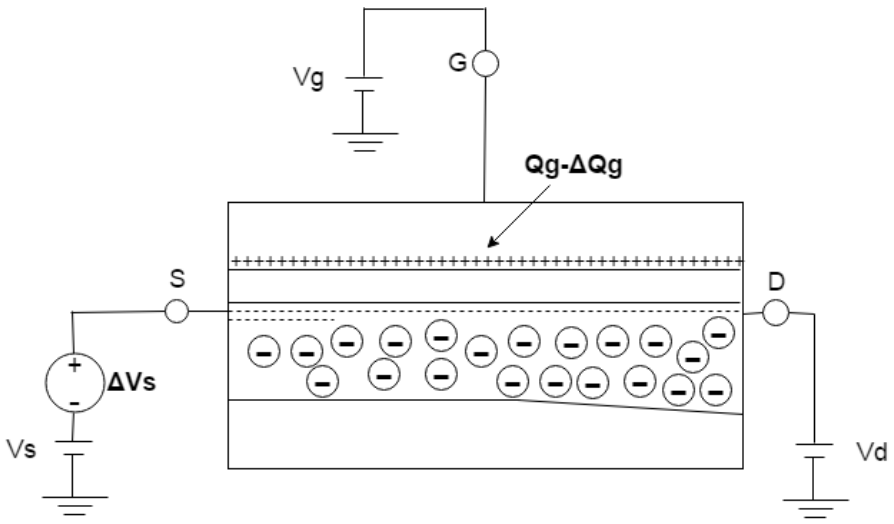

Figure 3.5: This figure shows the change in the total charge under the gate due to the application of small signal source voltage (ΔV_s) over the DC bias source voltage (V_s) of the transistor keeping other voltages constant.

per unit change in drain voltage.

$$\begin{aligned} C_{gs} &= \frac{-\partial Q_g}{\partial V_s}|_{V_g,V_d} \\ C_{gd} &= \frac{-\partial Q_g}{\partial V_d}|_{V_g,V_s} \end{aligned} \tag{3.42}$$

negative sign denotes that the gate charge decreases as source or drain voltage increases.

It is clear that to find gate-source and gate-drain capacitances, we need to know the gate charge as a function of source and drain voltage respectively. Total charge under the gate can be obtained by integrating the charge in the channel along the length of the gate as shown

$$Q_g = Z\int_0^{L_g} qn_s(x)dx \tag{3.43}$$

substituting dx from Eq. 3.41 in Eq. 3.43 and changing the integral limits appropriately, we get

$$Q_g = \frac{Z^2q^2\mu}{I_d}\int_{V_s}^{V_d} n_s^2 dV \tag{3.44}$$

we can integrate both sides of Eq. 3.41 to get I_d as

$$I_d = \frac{Z}{L_g}\int_{V_s}^{V_d} \mu q n_s dV \tag{3.45}$$

substituting the value of I_d from Eq. 3.45 in Eq. 3.44, we get

$$Q_g = ZL_gq\left(\frac{\int_{V_s}^{V_d} n_s^2 dV}{\int_{V_s}^{V_d} n_s dV}\right) \tag{3.46}$$

We can integrate the numerator and denominator of Eq. 3.46 using the relation between dV and dn_s from Eq. 3.40 separately. Representing numerator by $f(n_s)$ and denominator by $g(n_s)$ and integrating them, we get numerator as

$$f(n_s) = \frac{qd_d}{3\epsilon}\Big(n_D^3 - n_S^3\Big) + \frac{1}{4}\gamma_0\Big(n_D^{8/3} - n_S^{8/3}\Big) + \frac{1}{2}V_{th}\Big(n_D^2 - n_S^2\Big) \tag{3.47}$$

and denominator as

$$g(n_s) = \frac{qd_d}{2\epsilon}\Big(n_D^2 - n_S^2\Big) + \frac{2}{5}\gamma_0\Big(n_D^{5/3} - n_S^{5/3}\Big) + V_{th}\Big(n_D - n_S\Big) \tag{3.48}$$

substituting the integral values of numerator and denominator in Eq. 3.46 from Eq. 3.47

and Eq. 3.48, we get the total gate charge as

$$Q_g = ZL_gq\left(\frac{\frac{qd_d}{3\epsilon}\left(n_D^3 - n_S^3\right) + \frac{1}{4}\gamma_0\left(n_D^{8/3} - n_S^{8/3}\right) + \frac{1}{2}V_{th}\left(n_D^2 - n_S^2\right)}{\frac{qd_d}{2\epsilon}\left(n_D^2 - n_S^2\right) + \frac{2}{5}\gamma_0\left(n_D^{5/3} - n_S^{5/3}\right) + V_{th}\left(n_D - n_S\right)}\right) \tag{3.49}$$

Now, we can easily calculate gate-source and gate-drain capacitances by differentiating Eq. 3.49 with respect to source voltage and drain voltage respectively.

In general, we can express capacitance between gate and terminal x by

$$C_{gx} = ZL_gq\left(\frac{\frac{\partial f(n_s)}{\partial V_x}g(n_s) - f(n_s)\frac{\partial g(n_s)}{\partial V_x}}{(g(n_s))^2}\right) \tag{3.50}$$

in the equation above $V_x = V_s$ for gate-source capacitance and $V_x = V_d$ for gate-drain capacitance.

Eq. 3.47 and Eq. 3.48 can also be written as

$$f(n_s) = f_{main}(n_D) - f_{main}(n_S) \tag{3.51}$$

$$g(n_s) = g_{main}(n_D) - g_{main}(n_S) \tag{3.52}$$

where

$$f_{main}(n_x) = \frac{qd_d}{3\epsilon}n_x^3 + \frac{1}{4}\gamma_0 n_x^{8/3} + \frac{1}{2}V_{th}n_x^2 \tag{3.53}$$

$$g_{main}(n_x) = \frac{qd_d}{2\epsilon}n_x^2 + \frac{2}{5}\gamma_0 n_x^{5/3} + \frac{1}{2}V_{th}n_x \tag{3.54}$$

here, $n_x = n_S$ for source terminal and $n_x = n_D$ for drain terminal. Derivatives of Eq. 3.51 and Eq. 3.52 can be written as

$$\frac{df_{main}(n_x)}{dV_x} = \left(\frac{qd_d}{\epsilon}n_x^2 + \frac{2}{3}\gamma_0 n_x^{5/3} + V_{th}n_x\right)\frac{dn_x}{dV_x} \tag{3.55}$$

$$\frac{dg_{main}(n_x)}{dV_x} = \left(\frac{qd_d}{\epsilon}n_x + \frac{2}{3}\gamma_0 n_x^{2/3} + V_{th}\right)\frac{dn_x}{dV_x} \tag{3.56}$$

the factor of $\frac{dn_x}{dV_x}$ can be calculated by using Eq. 3.40 as

$$\frac{dn_x}{dV_x} = -\left(\frac{qd_d}{\epsilon} + \frac{2}{3}\gamma_0 n_s^{-1/3} + V_{th}n_s^{-1}\right)^{-1} \tag{3.57}$$

To calculate $\frac{dn_S}{dV_s}$ and $\frac{dn_D}{dV_d}$, replace n_s by n_S and n_D respectively in Eq. 3.57. n_S and

n_D values are also required to calculate $\frac{df_{main}(n_S)}{dV_s}$, $\frac{dg_{main}(n_S)}{dV_s}$ and $\frac{df_{main}(n_D)}{dV_d}$, $\frac{dg_{main}(n_D)}{dV_d}$ respectively along with $f(n_s)$ and $g(n_s)$ which will be used to calculate gate-source and gate-drain capacitances as shown further.

We can calculate the values of n_S and n_D by substituting V by $V_s = 0$ and $V_d = V_{d,eff}$ respectively in Eq. 3.39 and solving it iteratively.

To get the value of $V_{d,eff}$, we need to know the value of velocity saturation voltage (V_{sat}) of the device. Velocity saturation voltage is modeled as [18]

$$V_{sat} = \frac{v_{sat}(V_g - V_T)}{v_{sat} + (\mu/2L_g)(V_g - V_T)} \tag{3.58}$$

if the applied voltage V_d is greater than V_{sat}, then $V_{d,eff}$ is given by

$$V_{d,eff} = V_{sat}\left[1 - \frac{ln\left[1 + exp\left(1 - \frac{V_d}{V_{sat}}\right)\right]}{ln[1+e]}\right] \tag{3.59}$$

else, $V_{d,eff}$ is equal to applied drain voltage V_d.

From Eq. 3.51 and Eq. 3.52, it is clear that the partial derivatives of $f(n_s)$ and $g(n_s)$ are equivalent to the derivatives of $f_{main}(n_x)$ and $g_{main}(n_x)$ respectively. Hence Eq. 3.50 can also be written as

$$C_{gx} = ZL_g q\left(\frac{\frac{\partial f_{main}(n_x)}{\partial V_x} g(n_s) - f(n_s)\frac{\partial g_{main}(n_x)}{\partial V_x}}{(g(n_s))^2}\right) \tag{3.60}$$

On substituting the values of parameters of the designed device given in Fig. 3.1, we get the values of gate-source and gate-drain capacitances as

$$C_{gs} = 5.10 \times 10^{-14}\ F$$

$$C_{gd} = 4.87 \times 10^{-14}\ F$$

Also, we know the value of transconductance per unit width from section 3.3.3 to be $310mS/mm$. Multiplying it width the width of our device ($0.2mm$), we get

$$g_m = 0.0620\ S$$

on substituting the values of C_{gs}, C_{gd} and g_m in Eq. 3.27, we get the value of current

gain cutoff frequency to be

$$f_T = 98.97\ GHz$$

This value of current gain cutoff frequency meets the required specified range of values for f_T, which is specified in Table 1.2. Also, it is to be noted that higher the value of current gain cutoff frequency better the speed of the device. But the value of f_T calculated by the above method only takes into account gate-source and gate-drain capacitances, which is good for first-order approximation. A more accurate value of f_T can be obtained by incorporating parasitic capacitances and parasitic resistances of drain and source terminals. The formula for calculating f_T including all the parasitic resistances and capacitances is given by [17]

$$f_T = \frac{g_m}{2\pi\left[C_g\left(1+\frac{R_d+R_s}{R_{ds}}\right)+C_{gd}g_m(R_d+R_s)+C_{par}\right]} \tag{3.61}$$

where C_g is the sum of gate-source capacitance and gate-drain capacitance, C_{par} is parasitic pad capacitance, R_s and R_d are parasitic contact source and drain resistances and R_{ds} is the output resistance of the device given by

$$R_{ds} = \frac{1}{\lambda I_d} \tag{3.62}$$

where λ is channel length modulation parameter determined from experiment. For purpose of calculation, $\lambda = 1\times10^{-3}\ V^{-1}$ is chosen by appropriately scaling the values of λ reported by Yigletu et al. [18]. Radhakrishna et al. [22] reported the values of parasitic contact resistances and parasitic pad capacitances for their device. It must be noted that the values of parasitc resistances and parasitic capacitances are experimentally determined and vary depending upon the fabrication process. For the purpose of calculation, $R_s = 0.4\ \Omega$, $R_d = 0.6\ \Omega$ and $R_g = 3\ \Omega$ are taken. Also, the value of parasitic pad capacitance is chosen to be $60 \times 10^{-15}\ F$ by appropriately scaling the values reported by Radhakrishna et al. [22].

On substituting all the values in Eq. 3.61, current gain cutoff frequency is calculated as

$$\mathbf{f_T = 60.66\ GHz}$$

The above value of current gain cutoff frequency calculated after incorporating all the

parasitics meets the required value. This substantiates the performance of the designed AlGaN/GaN HEMT structure for high frequency applications.

3.3.5 Maximum Oscillation Frequency (f_{max})

Maximum oscillation frequency is defined as the frequency at which the maximum unilateral power gain is unity. f_T is often referred to as the most relevant figure-of-merit for transistors operating at millimeter wave frequencies however, f_{max} is a far more relevant parameter for most circuits, since it accounts for gate parasitics of the device as well and measures the frequency at which power can be delivered to a load.

f_{max} is defined for a transistor with its input and output ports conjugate-matched for maximum power transfer. So, we need to know the input and output impedance to define the input and output power as well as achieve the maximum power transfer matching condition.

An analytical formula to calculate the maximum oscillation frequency (f_{max}) is given by [4]

$$f_{max} = \frac{f_T}{2\sqrt{2\pi f_T R_g C_{gd} + \frac{R_s+R_g}{R_{ds}}}} \tag{3.63}$$

on substituting the values of all the parameters of our device in the Eq. 3.63, we get

$$\mathbf{f_{max} = 126.95\ GHz}$$

The value of maximum oscillation frequency obtained by incorporating all the device parasitics meets the required value of f_{max}. This again validates the high frequency operation ability of the designed AlGaN/GaN HEMT structure.

3.3.6 Power

Power is one of the most important performance parameter of a transistor. It gives an idea of the level of power the device can withstand without breaking down while operating. It is desired that the device should have higher power endurance so that it can be used in high power applications. Since AlGaN and GaN both are wide bandgap semiconductors they have excellent power tolerance levels. Hence, AlGaN/GaN HEMT

is capable for high power applications.

To calculate the maximum power of the transistor, the following formula is used [23]

$$P = \frac{1}{8}(V_{br} - V_{knee})I_{d,max} \tag{3.64}$$

where V_{br} is the breakdown gate-drain voltage and V_{knee} is the knee voltage of the device which can be approximately taken as the threshold off voltage of the device V_T.

To calculate maximum power per millimeter width, $I_{d,max}$ per millimeter width is taken. Also, the breakdown voltage of the device is taken as 60V which is congruent with the breakdown voltage reported by Nguyen et al. [7].

On substituting the values, we get

$$\mathbf{P = 9.78\ W/mm}$$

This value of power is more than the required value which is $4 - 5\ W/mm$. It is always desired to have high power as this makes the device more robust and capable to operate even at higher voltage levels. Hence, we can say that the designed device is capable to operate at desired voltage levels without breaking down.

3.4 Noise Analysis of the device

Noise is an important performance metric of communication circuits. It is desired that any communication system should produce as less noise as possible. Since, transistors are the building blocks of communication circuits like transmitter and receiver, it is important to analyse the noise performance of a transistor. Low noise amplifiers are most commonly used in communication systems and there is a need of low noise devices to build them. AlGaN/GaN HEMTs are promising devices for this application since they can operate at high frequency and tolerate high power. This renders the need of protection circuitry in communication systems reduntant which makes them more compact and robust.

To characterize noise of a device, phase noise and noise figure are commonly used.

3.4.1 Phase Noise

Phase noise is defined as the noise produced at frequencies close to reference frequency. It is generally produced by oscillators which are used to generate signal of a desired frequency. In addition to the desired signal, an oscillator produces other signals at frequencies close to the desired frequency. These signals contribute to the phase noise.

It is understood that various device noise sources contribute to the phase noise. These include thermal, shot, and low-frequency (also called flicker, or 1/f) sources. The quantitative analysis of how these sources contribute to the phase noise is difficult even for the simplest of cases. A qualitative description that embodies many important points was presented by Leeson [24], which is described as

$$L(\Delta\omega) = 10log\left[\frac{2NFkT}{P_{sig}}\left\{1+\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right\}\left(1+\frac{\frac{\Delta\omega_1}{f^3}}{|\Delta\omega|}\right)\right] \tag{3.65}$$

where L is the phase noise in 1 Hz bandwidth at an offset angular frequency, $\Delta\omega$, from the carrier angular frequency, ω_0, Q is the quality of the resonator, Psig is the signal power, and NF is the effective noise figure. Shot and thermal noise sources contribute to F, a measure of the background noise of the device and circuit. The low frequency noise (LFN) contributes through $\Delta\omega_1/f^3$.

It is clear from Eq. 3.65 that to reduce phase noise we need to reduce various background noise sources in a device and circuit. Eq. 3.50 also tells us that phase noise is less for more signal power.

3.4.2 Noise Factor and Noise Figure

Noise Factor is defined as the ratio of SNR at input to SNR at output. Mathematically, noise factor is given by

$$F = \frac{SNR_i}{SNR_o} \tag{3.66}$$

where SNR_i is signal to noise ratio at input and SNR_o is signal to noise ratio at output.

Noise Figure is a convenient way to represent noise factor. It is defined as the noise factor in logarithmic units, as

$$NF = 10log(F) \tag{3.67}$$

or,

$$NF = 10log\left(\frac{SNR_i}{SNR_o}\right) \tag{3.68}$$

We can also write noise figure as

$$NF = SNR_{i,dB} - SNR_{o,dB} \tag{3.69}$$

where $SNR_{i,dB}$ is the signal to noise ratio at input represented in decibels and $SNR_{0,dB}$ is the signal to noise ratio at output represented in decibels. From the above equation, it can be inferred that noise figure is a measure of degradation of the SNR from input to output.

3.4.3 Noise Calculation of the device

To quantify the noise of the device, its minimum noise figure is calculated. Fukui [25] reported a useful empirical expression for estimating the room temperature minimum noise figure (NF_{min}) of a GaAs field effect transistor. The Fukui equation is given by

$$NF_{min} = 10log\left\{1 + \frac{K_F F}{f_T}[g_m(R_g + R_s)]^{0.5}\right\} \tag{3.70}$$

where f_T is the current gain cutoff frequency, F is the frequency of operation, g_m is the transconductance, R_g and R_s are gate and source resistances respectively and K_F is the empirical fitting factor.

Oxley [26] used the Fukui equation to calculate the minimum noise figure of GaN HEMTs by appropriately choosing the empirical fitting factor K_F. For short gate-length transistors empirical fitting factor is given by [27]

$$K_F = 2\left(\frac{I_{opt}}{E_c L_g g_m}\right)^{0.5} \tag{3.71}$$

where I_{opt} is the optimum current for minimum noise operation, L_g is the gate length and E_c is the critical electric field.

using Eq. 3.71 in Eq. 3.70, we get

$$NF_{min} = 10log\left\{1 + \frac{2F}{f_T}\left[\frac{I_{opt}(R_g + R_s)}{E_c L_g}\right]^{0.5}\right\} \tag{3.72}$$

Oxley [26] chose $E_c = 150\ kV/cm$ for calculating the minimum noise figure of the device reported by Nguyen et al. [7]. Since the designed device is based on the device reported by Nguyen et al. [7], it is a good approximation to take $E_c = 150\ kV/cm$. Also, the optimum current is chosen as 20% of the maximum current similar to that chosen by Nguyen et al. [7]. The operating frequency of device is assumed to be $10\ GHz$.

On substituting the values of all parameters in Eq. 3.72, we get

$$\mathbf{NF_{min} = 0.36\ dB}$$

This value of minimum noise figure is better than the value of the minimum noise figure reported by Nguyen et al. [7]. This shows that the designed device is capable of operating at high frequencies without producing much background noise. Hence, the device is ideal for designing Low Noise Amplifiers.

CHAPTER 4

CONCLUSIONS

An AlGaN/GaN High Electron Mobility Transistor (HEMT) device structure is designed based on one of the reported structure to meet the required electrical performance for high frequency low noise applications. The electrical performance of the device is validated by calculating its various performance parameters. While calculating the RF figures of merit such as current gain cutoff frequency and maximum oscillation frequency, it is found that parasitic resistances and pad capacitances influence them directly. Hence an accurate knowledge of parasitics of the device is necessary for more accurate calculations. However for the purpose of calculation values of parasitic resistances and pad capacitances are chosen by appropriately scaling the reported values of parasitic resistances and pad capacitances.

Low Noise operation capability of the device is ascertained by calculating its noise figure. An excellent noise of 0.36 dB upto the operating frequency of 10 GHz ensures that the designed device is capable of operating at millimeter wave frequencies while producing less background noise.

APPENDIX A

MATLAB FILE FOR CALCULATIONS

```
x = 0.18; % mole fraction
L = 150e-9; % gate length (m)
W = 0.2e-3; % width (m)
D = 3.24e17; % density of states (m-2V-1)
gamma0 = 2.5e-12;% gamma nought (V m4/3)
mu = 0.1; % low field mobiltiy (m2/Vs)
q = 1.6e-19; % electron charge (C)
Vth = 0.026; % thermal voltage (V)
Nd = 2e24; % barrier doping (m-3)
dd = 20e-9; % barrier thickness (m)
di = 3e-9; % spacer thickness (m)
Rs = 0.4; % Parasitic Source resistance (ohm)
Rd = 0.6; % Parasitic Drain resistance (ohm)
Rg = 3; % Gate Resistance (ohm)
clm = 1e-3; % Channel length modulation parameter
sce = 25; % Short Channel Effect parameter
Eg = 3.43 + 1.44*x + 1.33*x*x; % band gap pf AlGaN (V)
eps = 9.7 - 1.2*x; % dielectric constant of AlGaN
e0 = 8.85e-12; % epsilon nought
delEc = 0.7*(Eg - 3.43); % band offset delta Ec (V)
phin = 0.91 + 2.44*x; % barrier height (V)
Vp = (q*Nd*dd^2)/(2*eps*8.85e-12); % pinch off voltage (V
    )
ax = (-0.077*x + 3.189)*10^(-10); % lattice constant (m)
C13 = 5*x + 103;   % elastic constants
C33 = -32*x + 405;
e31 = -0.11*x - 0.49; % piezoelectric constants (C/m-2)
e33 = 0.73*x + 0.73;
```

```
Psp = -0.052*x - 0.029; % spontaneous polarization (C/m
    -2)
Ppe = (2*((3.189e-10) - ax)/ax)*(e31-(e33*C13/C33)); %
    piezo polar (C/m-2)
sig = abs(Ppe + Psp + 0.029); % piezoelectric charge
    density (C/m-2)
Vg = 0; % gate voltage (V)
Vs = 0; % source voltage (V)
Vd = 28; % drain voltage (V)
Vgs = Vg - Vs; % gate-source voltage
Vds = Vd - Vs; % drain-source voltage
Vgd = Vgs - Vds; %source-drain voltage

%Finding Voff
Voff = phin - delEc - Vp - (sig*(dd+di))/(eps*8.85e-12);

Vg0 = Vg - Voff;
vs = 0.85e5; % saturation velocity (m/s)
gm = ((eps*e0)*vs*W)/(dd+di);
gmpermm = gm/W;
qns = ((eps*e0)*(Vg-Voff))/(dd+di);
Imax = (qns*vs);
Cinv = (eps*e0)/(dd+di);

% calculating ns at source end
syms ns
 eqn1 = (q*(dd+di)*ns)/(eps*e0) + gamma0*(ns^(2/3)) + Vth
    *log(ns/(D*Vth)) + Voff - Vgs;
 sol1 = solve(eqn1, ns);
 nss = double(abs(sol1));

% calculating saturation voltage
Vsat = (vs*Vg0)/(vs + (mu/(2*L))*Vg0);
```

```
57
58 % checking whether Vd is below Vsat or not and using it
       effectively
59 if Vds>=Vsat
60       Vdeff = Vsat*(1-(log(1+exp(1-Vds/Vsat)))/(log(1+2.72)
           ));
61 else
62       Vdeff = Vds;
63 end
64 Vds = Vdeff;
65
66 % calculating ns at drain end considering voltage
       saturation
67 syms nd
68  eqn2 = (q*(dd+di)*nd)/(eps*e0) + gamma0*(nd^(2/3)) + Vth
       *log(nd/(D*Vth)) + Voff - Vgs + Vds ;
69  sol2 = solve(eqn2, nd);
70  ndd = double(abs(sol2));
71
72 % Finding the current including CLM
73 Ids = (q*mu*W/L)*((q*(dd+di)/(2*eps*e0))*(nss^2 - ndd^2)
      + 0.4*gamma0*(nss^(5/3)-ndd^(5/3)) + Vth*(nss-ndd));
74 Ids = Ids*(1+clm*Vd);
75 Idsmax = (Ids*1e-3)/W;
76
77 % Finding Capacitances
78 fns = ((q*(dd+di))/(3*eps*e0))*(ndd^3 - nss^3) + 0.25*
       gamma0*(ndd^(8/3) - nss^(8/3)) + 0.5*Vth*(ndd^2-nss^2);
79 gns = ((q*(dd+di))/(2*eps*e0))*(ndd^2 - nss^2) + 0.4*
       gamma0*(ndd^(5/3) - nss^(5/3)) + Vth*(ndd-nss);
80 Qg = W*L*q*(fns/gns); % Gate Charge
81
82 fmns = ((q*(dd+di))/(3*eps*e0))*nss^3 + 0.25*gamma0*(nss
```

```
    ^(8/3)) + 0.5*Vth*(nss^2);
fmnd = ((q*(dd+di))/(3*eps*e0))*ndd^3 + 0.25*gamma0*(ndd
    ^(8/3)) + 0.5*Vth*(ndd^2);
gmns = ((q*(dd+di))/(2*eps*e0))*nss^2 + 0.4*gamma0*(nss
    ^(5/3)) + Vth*(nss);
gmnd = ((q*(dd+di))/(2*eps*e0))*ndd^2 + 0.4*gamma0*(ndd
    ^(5/3)) + Vth*(ndd);

dns = -(((q*(dd+di))/(eps*e0)) + (2/3)*gamma0*(nss^(-1/3))
    ) + Vth*nss^(-1))^(-1);
dnd = (((q*(dd+di))/(eps*e0)) + (2/3)*gamma0*(ndd^(-1/3))
     + Vth*ndd^(-1))^(-1);

dfmns = (((q*(dd+di))/(eps*e0))*nss^2 + (2/3)*gamma0*(nss
    ^(5/3)) + Vth*(nss))*dns;
dfmnd = (((q*(dd+di))/(eps*e0))*ndd^2 + (2/3)*gamma0*(ndd
    ^(5/3)) + Vth*(ndd))*dnd;
dgmns = (((q*(dd+di))/(eps*e0))*nss + (2/3)*gamma0*(nss
    ^(2/3)) + Vth)*dns;
dgmnd = (((q*(dd+di))/(eps*e0))*ndd + (2/3)*gamma0*(ndd
    ^(2/3)) + Vth)*dnd;

Cgs = W*L*q*(((dfmns*gns) - (fns*dgmns))/(gns^2));
Cgd = W*L*q*(((dfmnd*gns) - (fns*dgmnd))/(gns^2));
Cpar = 60e-15; % Parasitic pad caps
% ft and fmax
ft = gm/(2*pi*((Cgs+Cgd)*(1+(Rd+Rs)*(clm*Ids))+(gm*Cgd*(
    Rs+Rd)) + Cpar));
ft2 = gm/(2*pi*(Cgs+Cgd+Cpar));
%fmax = (ft/(8*pi*Cgd*Rg))^0.5;
fmax = (0.5*ft)/(2*pi*ft*Cgd*(Rg)+((Rg+Rs)/(1/(clm*Ids)))
    )^0.5;

```

```
104 % Minimum Noise Figure
105 C1 = 2.5; % s/F
106 f = 10^10;
107 Iopt = 0.2*Imax*W;
108 Ecrit = 15e6; % Critical Electric Field V/m
109 Fmin = 1 + 2*(f/ft2)*((Iopt*(Rg+Rs))/(Ecrit*L))^0.5;
110 Fdb = 10*(log(Fmin)/log(10));
111
112 % Power Calculation
113 Vbr = 60; % Breakdown Voltage V
114 power = (Vbr-Voff)*(Imax*1e-3)*(1/8);
```

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