Digitally Controlled Oscillator implementation in TSMC 65nm CMOS Technology

A Project Report

By

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A project report submitted in partial fulfillment
of the requirements for the
Dual Degree
Bachelor of Technology & Master of Technology

DEPARTMENT OF ELECTRICAL ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY MADRAS

June 2017

CERTIFICATE

This is to certify that the report entitied **Digitally Controlled Oscillator implementation in TSMC 65nm CMOS Technology**, submitted by **M A K ARTHUR COTTON MANDELA, EE12B097**, to the **Department of Electrical Engineering, Indian Institute of Technology Madras**, for the award of the **Dual Degree**, is a bona fide record of the research work carried out by him under my supervision. The contents of this project, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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June, 2017

Abstract

This project involves conversion of a voltage controlled oscillator(VCO) into a Digitally controlled oscillator(DCO). This can be achieved either by using a Digital to Analog converter (DAC) with VCO so that it works with the digital inputs or by replacing the varactor control with a fine-tuning capacitor bank. Both the implementations are discussed in this thesis. The supply to the oscillator is given by an LDO. The LDO is a two stage Miller compensated Opamp which drives the PMOS output stage. The design is implemented in a 65nm CMOS process from TSMC.

Acknowledgements

It gives me a great pleasure to express my sincere and heartfelt gratitude to my mentor Dr. Nagendra Krsihnapura for his guidance, motivation and constant support. I want to become a professor and I take great motivation from him and Dr. Shanthi Pavan after having attended their courses as student and Teaching assistant respectively. This motivation dragged me to work under Dr. Nagendra Krishnapura's tutelage.

His dedication and interest and above all his overwhelming attitude to help his students has been solely responsible for completing my work. Weekly meetings with him, kept me motivated and also improved interaction with colleagues. I would like to thank him for is courses Analog circuits and Analog IC design which I enjoyed the most. I want to appreciate him for giving me sufficient time to work peacefully and also being gentle with his students. I am greatly saddened for not performing to my fullest due to personal issues which took great toll on me and had to give my immediate attention to. I thank him for taking his time to listen to few of my problems. I am also grateful for the laboratory facilities provided by him in the analog lab, Department of Electrical Engineering, which facilitated my work.

I would like to thank various faculty members of IIT Madras from whom I have benefited as a student. I would like to thank Dr. Qadeer Ahmed Khan for giving me opportunity to mentor students for Analog Lab. I thoroughly enjoyed helping them with their laboratory assignments. I would like to thank Dr. Shreepad Karmalkar for his wonderful course on Device modelling. This course helped me understand methods to analyze subtleties in concepts, which I not only use in academics but also in personal life. I would like to extend my sincere thanks to Dr. Sreerama Srinivas for making me feel homely and taking several hours in every interaction to clear my thoughts about higher studies and research.

I express my sincere gratitude to Abishek Bhat and Ashwin whose support was very valuable. I would also like to thank Raviteja, Amal, Niveditha, Deepthi, Raviteja(MS), Ankesh, Saravana for their support and friendly environment in lab. I would also like to thank Janaki mam for helping with several technical issues I incurred during my project. I would like to thank my friends Anoushka, Sandeep, Shekhar, Sowrya and Vandana for all the memories during the last year at IIT Madras.

Finally, I would like to acknowledge the people who mean world to me, my parents, my brother and my sister. Thanks for all your support.

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Abbreviations

VCO	**Voltage Controlled Oscillator**
DCO	**Digitally Controlled Oscillator**
DAC	**Digital to Analog Converter**
LDO	**Low Drop Out regulator**
PN	**Phase Noise**
MOSFET	**Metal Oxide Semiconductor Field Effect Transistor**
OPAMP	**Operational Amplifier**
Q	**Quality Factor**
PMOS	**P-type Metal Oxide Semiconductor**
NMOS	**n-type Metal Oxide Semiconductor**
DNL	**Differential Non Linearity**
INL	**Integral Non Linearity**

Chapter 1

Introduction

1.1 Overview

An oscillator generates a periodic output. As such, the circuit must involve self-sustaining mechanism that allows its own noise to grow and eventually become a periodic signal. An oscillator may be viewed as a badly designed negative feedback amplifier such that its phase margin is zero or negative.

In VCO designs, the preferred way is to use LC cross-coupled oscillator owing to its good phase noise performance. One disadvantage is that use of inductor makes the circuit consume more space. We wish to build a negative feedback oscillator using LC-tuned amplifier stages.

1.2 Basic Principles of LC Oscillators

The figure given below shows a stage where C_1 denotes the total capacitance seen at the output node and R_p is the total parallel resistance at the resonant frequency. At low frequencies L_1 dominates the load. At this point the gain is very small and phase is around -90^0.

$$\frac{V_{out}}{V_{in}} = -g_m L_1 s \tag{1.1}$$

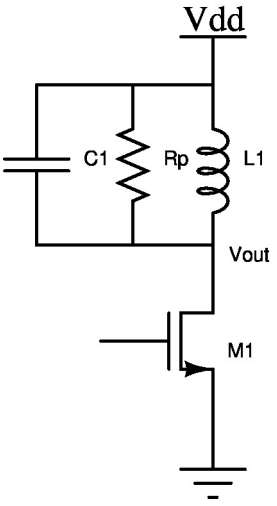

FIGURE 1.1: Tuned Amplifier

At resonance frequency ω, the tank reduces to R_p and the phase shift is now -180^0.

$$\frac{V_{out}}{V_{in}} = -g_m R_p \tag{1.2}$$

At high frequencies the gain again diminishes and the phase is $+90^0$.

$$\frac{V_{out}}{V_{in}} = -g_m \frac{1}{C_1 s} \tag{1.3}$$

We see that the circuit provides a phase of 180^0 with possible gain of $g_m R_p$ at ω_0. We

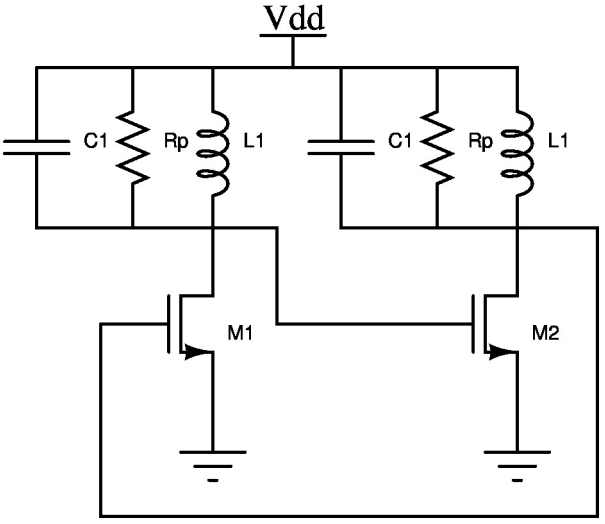

FIGURE 1.2: Cascade of two tuned amplifier in feedback loop

simply need to increase the phase shift to 360^0 by inserting another stage in the loop as

shown in Figure1.2. The circuit oscillates if the loop gain is equal to or greater than unity

$$(g_m R_p)^2 \geqslant 1 \tag{1.4}$$

1.3 VCO Architecture

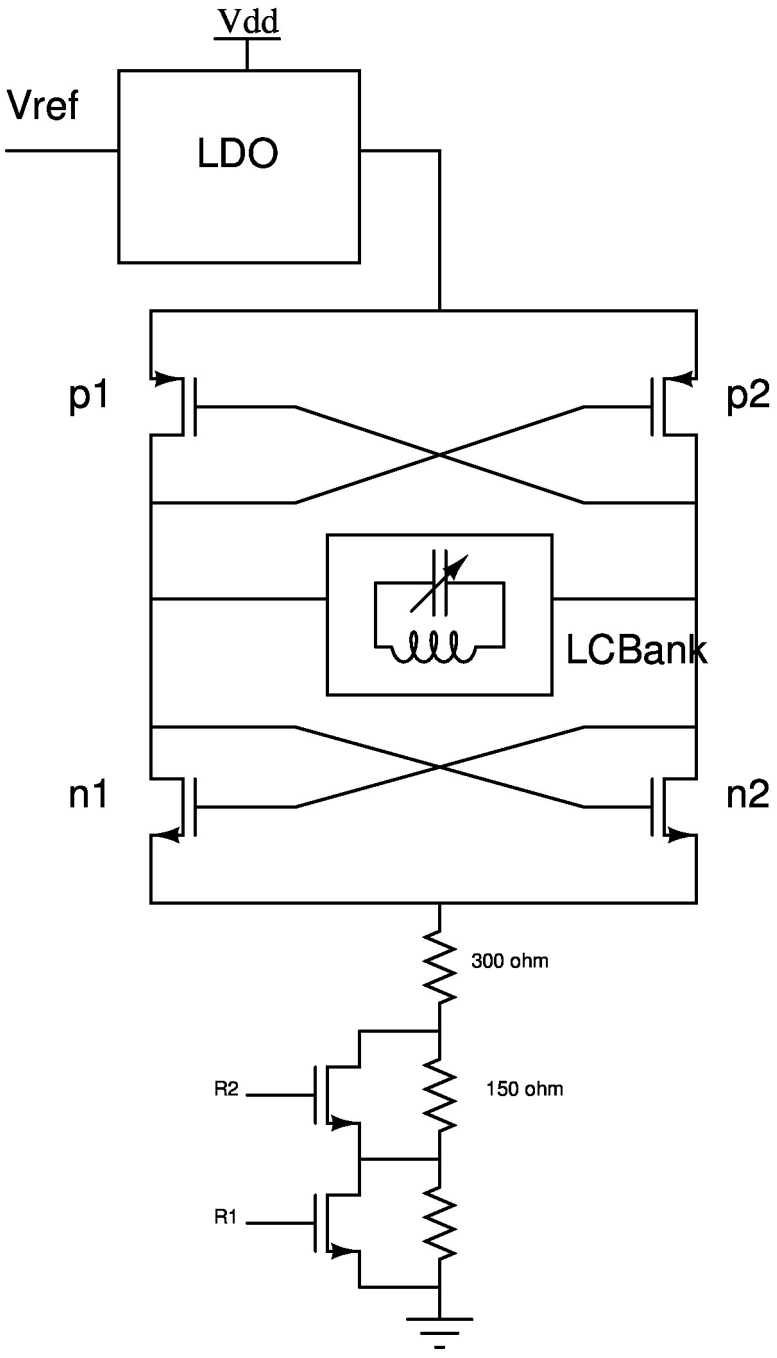

FIGURE 1.3: VCO Schematic

The output power of the VCO is directly dependent on the dc power consumption of VCO. In a given process, the Q is fixed. Thus increasing output amplitude is the easiest way to reduce the phase noise. There are many architectures proposed in literature. Some include nMOS cross couples with pMOS current source or nMOS current source with pMOS cross coupled, but in these architectures the main problem is due to the flicker noise of the current source. Hence to reduce the PN relatively more current needs to be burnt. nMOS (or pMOS) only architecture does not have best dc to RF power conversion efficiency for given tank load.

Complementary CMOS architecture reuses the current, hence provides double the amplitude of that of an nMOS or pMOS only VCO and in the voltage biased architecture, there is no current source and the flicker noise contribution by it is absent. The VCO is powered by a 1V supply derived as the output of an 1.2V to 1V LDO (Discussed in AppendixA).

Analog control of the VCO can be masked by using a DAC with VCO. The analog control can be totally removed by replacing the varactor with a fine tuning capacitor bank.

1.3.1 Choice of Inductor

The Q of the tank is mainly dominated by the inductor as the capacitor Q are usually much high. If we use very high inductor values we need to use very low capacitor values for vocering the same fequency band and this may degrade the tuning range, also use of high value inductor would occupy large space. In our case library inductor of 2nH with Q of 21 at 5GHz is used.

1.3.2 Tail Resistance

In the voltage biased VCO, the current is not well defined and changes from corner to corner. Hence, we have a programmable tail resistance to maintain a well defined current. A fixed resistance of 300ω is used and a 2-bit resistor bank of 150Ω and 300Ω is used. The resistors are in parallel with nMOS whose on-state resistance is 4Ω which can act as an effective short. R1 corresponds to 300Ω and R2 corresponds to 150Ω

1.3.3 Negative Resistance

We have used an nMOS-pMOS cross-coupled pair in the design. The inductor and capacitor always come with a resistive component. This resistive component is responsible for decaying down the oscillations. We therefore need active devices which can act as a negative resitance to overcome the loss. This cross-coupled device need to have a transconductance such that the loss is appropriately compensated. As we are using both pMOS-nMOS pair, the oscillation condition becomes:

$$\frac{2}{g_{mp} + g_{mn}} \leqslant R_p \tag{1.5}$$

1.4 Organisation of thesis

Chapter1 introduces the basics of LC oscillators and VCO Architecture

Chapter2 deals with conversion of VCO into DCO using a DAC.

Chapter3 deals with DCO obtained by replacing the varactor with fine tuning capacitor bank.

Chapter4 presents the conclusions of the project.

Chapter 2

DAC with VCO

The analog control to the varactor in the capacitor bank of the VCO for fine tuning can be replaced with a DAC to enable digital control to the VCO. A 10 bit resistive DAC is designed to convert a 10bit digital input(D_{in}) to a corresponding analog output which controls the varactor to tune it to specific frequency.

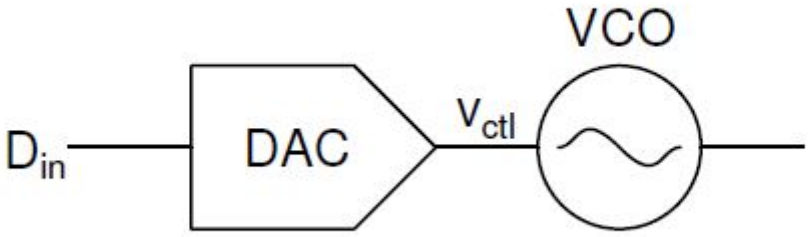

FIGURE 2.1: VCO with DAC illustration

2.1 DAC

DAC (Digital to analog converter) is a device to convert the input signal in digital (usually binary) form into an output signal in the analog form (voltage). The resulting DAC output voltage is proportional with the digital value supplied into the DAC. The most common type of electronic DACs are: pulse width modulator, delta-sigma DAC, binary-weighted DAC, R-2R ladder DAC, thermometer-coded DAC, and Hybrid DACs.

We use R-2R topology as shown in Figure2.2.

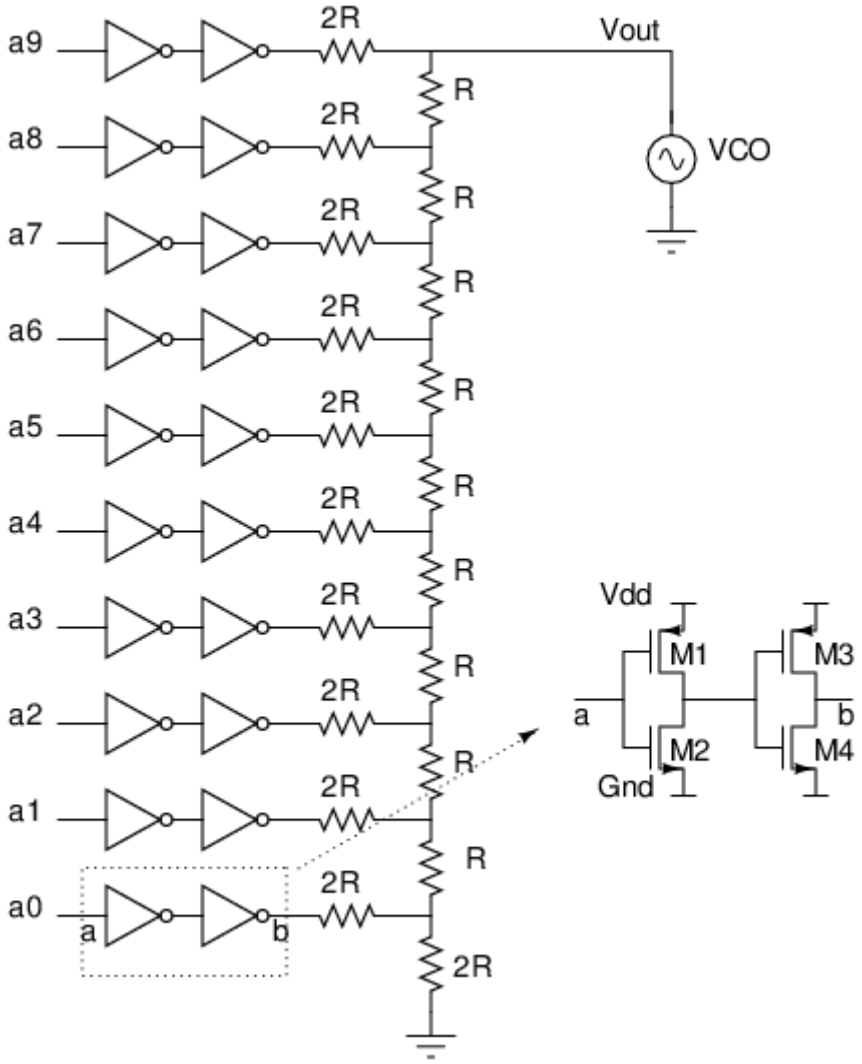

FIGURE 2.2: 10 bit resistive DAC connected to VCO

2.2 MOSFET as a digital switch

A simple description treats the MOSFET transistor as a switch. The gate terminal is analogous to the light switch on the wall. When the gate has a high voltage, the transistor closes like a wall switch, and the drain and source terminals are electrically connected. Just as a light switch requires a certain force to activate, the transistor gate terminal needs a certain voltage level to switch and connect the drain and source terminals. This voltage is usually called as the transistor threshold voltage V_t and is a fixed voltage for nMOS and for pMOS devices in a given fabrication process.

The switch is realized with a series of two CMOS inverter as shown in Figure2.2. if the input a is signed 0, the transistor type N (M2) is open and transistor type P(M1) is closed so VDD voltage passes through M1 and output is 1. This given as input to the next inverter, transistor type P(M3) is open and transistor type N(M4) is closed so GND voltage passes through M4 and the output b is 0.

The MOSFETs M1, M2, M3, M4 are sized apropriately to supply sufficient amount of current based on the requirements of the DAC. The sizes chosen are as follows: M1,M3 - pMOS - 500u with multiplier 3 and M2,M4 - nMOS - 130u with multiplier 1. The resistor value R is chosen to be $5k\Omega$ to allow less contribution of the DAC as a whole in the phase noise of VCO.

2.3 Simulation results

This section deals with the simulation results observed with the 10bit resistive DAC.

The following Figure2.3 shows the transfer curve of the resistive DAC. It can be observed

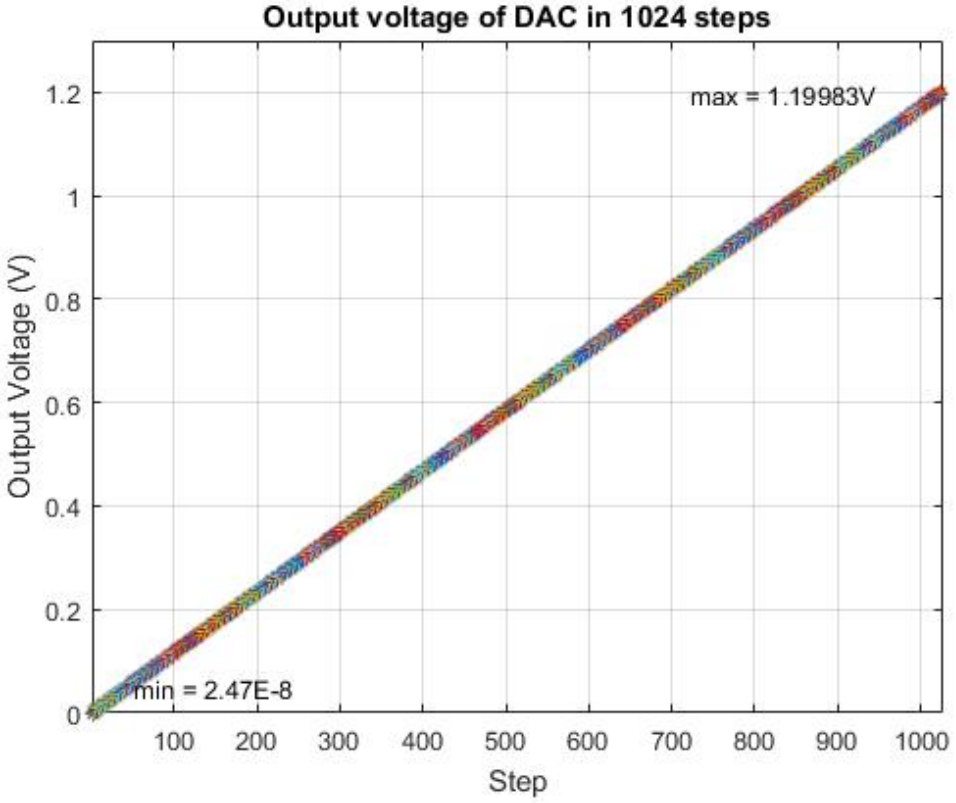

FIGURE 2.3: DAC output voltage VS digital input

that the maximum output voltage of the resistive DAC is $1.19983V$ which is denoted as Full-Scale Voltage V_{FS}.

$$\begin{aligned} V_{out} &= \frac{2^{N-1}a_9 + 2^{N-2}a_8 + ... + 2a_1 + a_0}{2^N} \\ &= \frac{2^9a_9 + 2^8a_8 + ... + 2a_1 + a_0}{2^{10}} \\ &= \frac{2^9.1 + 2^8.1 + ... + 2.1 + 1}{2^{10}}(FullScale) \\ &= 1.19883V \end{aligned} \tag{2.1}$$

2.3.1 Differential Nonlinearity (DNL)

In an ideal DAC each adjacent output increment should be exactly $\frac{Vdd}{1024}$ (=1LSB). However, nonideal components cause the analog increments to differ from their ideal values. The difference between the ideal and nonideal values is known as Differential Nonlinearity or DNL. DNL for the 10bit resistive DAC is as shown in Figure2.4.

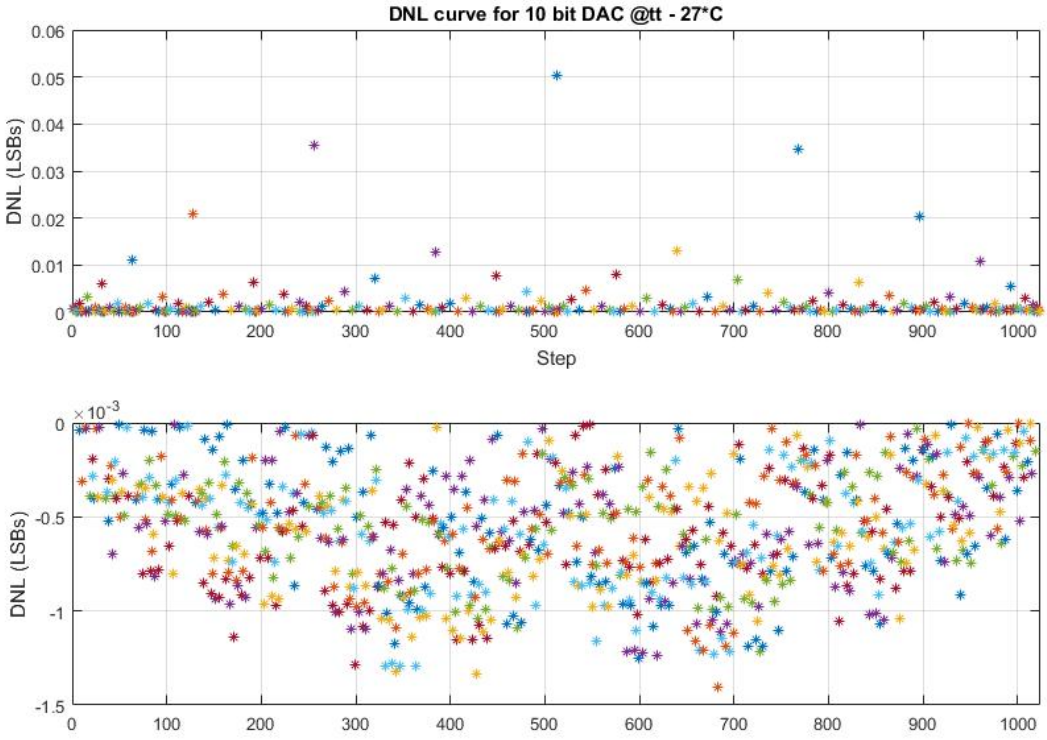

FIGURE 2.4: DNL of 10bit DAC @tt -27^*C

Generally, a DAC will have less than $\pm\frac{1}{2}$LSB. if the DNL for a DAC is less than -1 LSBs, then the DAC is said to be nonmonotonic. The DNL for the entire converter is $+0.05$ LSB to -0.0014 LSB and hence the DAC is monotonic.

2.3.2 Integral Nonlinearity (INL)

The difference between the data conveter output values and a reference straight line drawn through the first and last output values, INL defines the linearity of the overall transfer curve. It is common practice to assume that a converter with N-bit resolution will have less than $\pm\frac{1}{2}$LSB of DNL and INL. The term $\frac{1}{2}$LSB, is a common term that typically denotes the maximum error of a data converter (both DACs and ADCs).

INL for the 10 bit resistive DAC is as shown in Figure2.5.

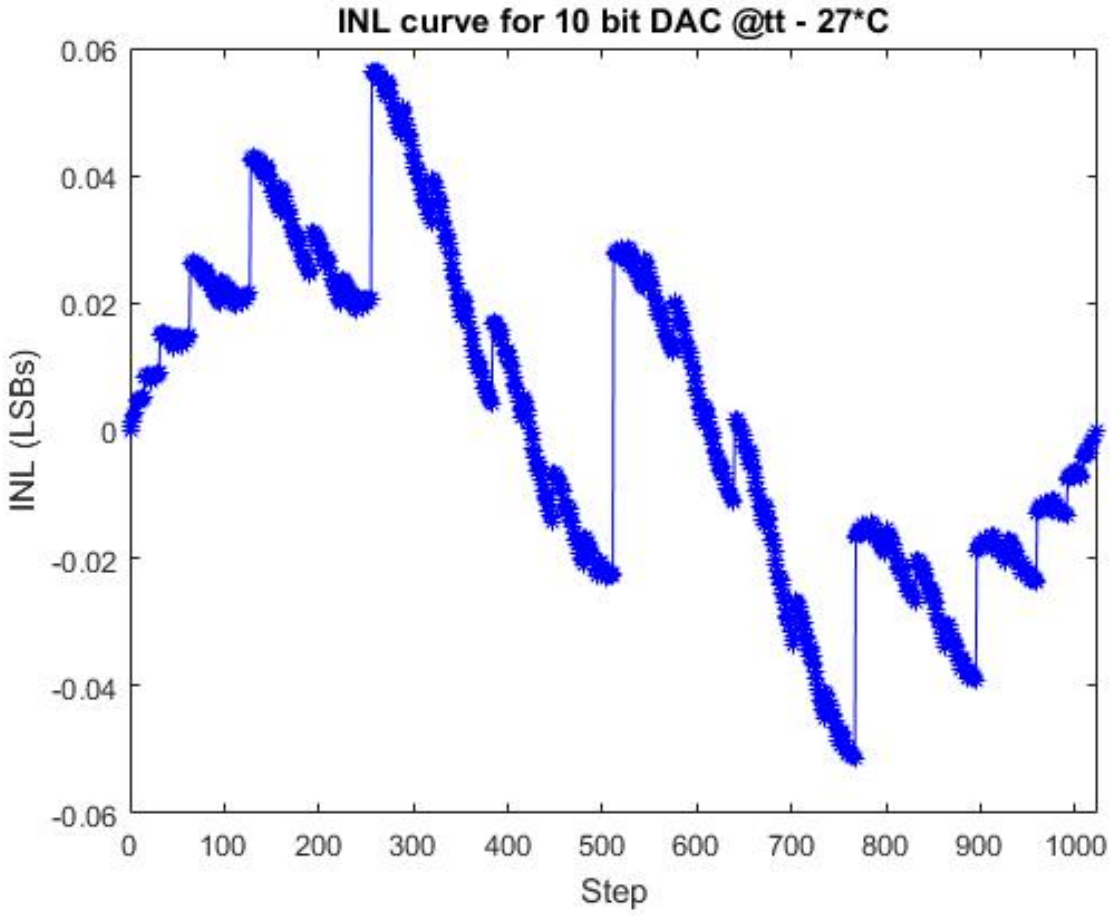

FIGURE 2.5: INL of 10bit DAC @tt $-27^{*}C$

2.3.3 Offset

The analog input should be $0V$ for input 10bit binary word 0. However, an offset exists if the analog output voltage is not equal to zero. This can be seen as a shift in the transfer curve as illustrated in Figure2.3. The offset of the 10bit resistive DAC is $2.47x10^{-8}$V

2.3.4 output Frequency

The output frequency of VCO after controlled by a DAC are increasing monotonically for increase in input voltage in 1024 steps. This is shown in Figure2.6. The maximum step increase in the output frequency is 0.26MHz and minimum step increase in output frequency is 0.03MHz.

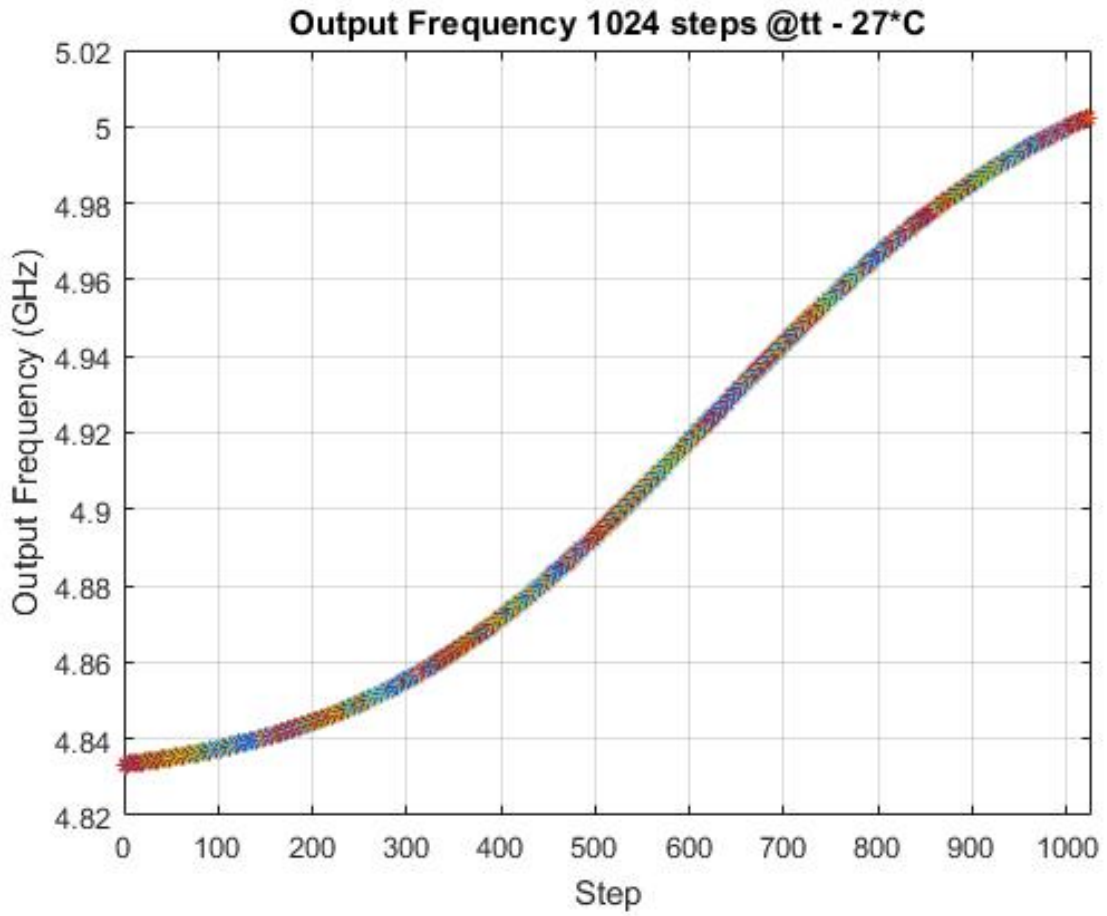

FIGURE 2.6: Monotonic increase in output frequency of VCO @tt $-27^{*}C$

K_{vco} is shown in Figure2.7. It is calculated by dividing the step increase in output frequency to step increase in output voltage of DAC.

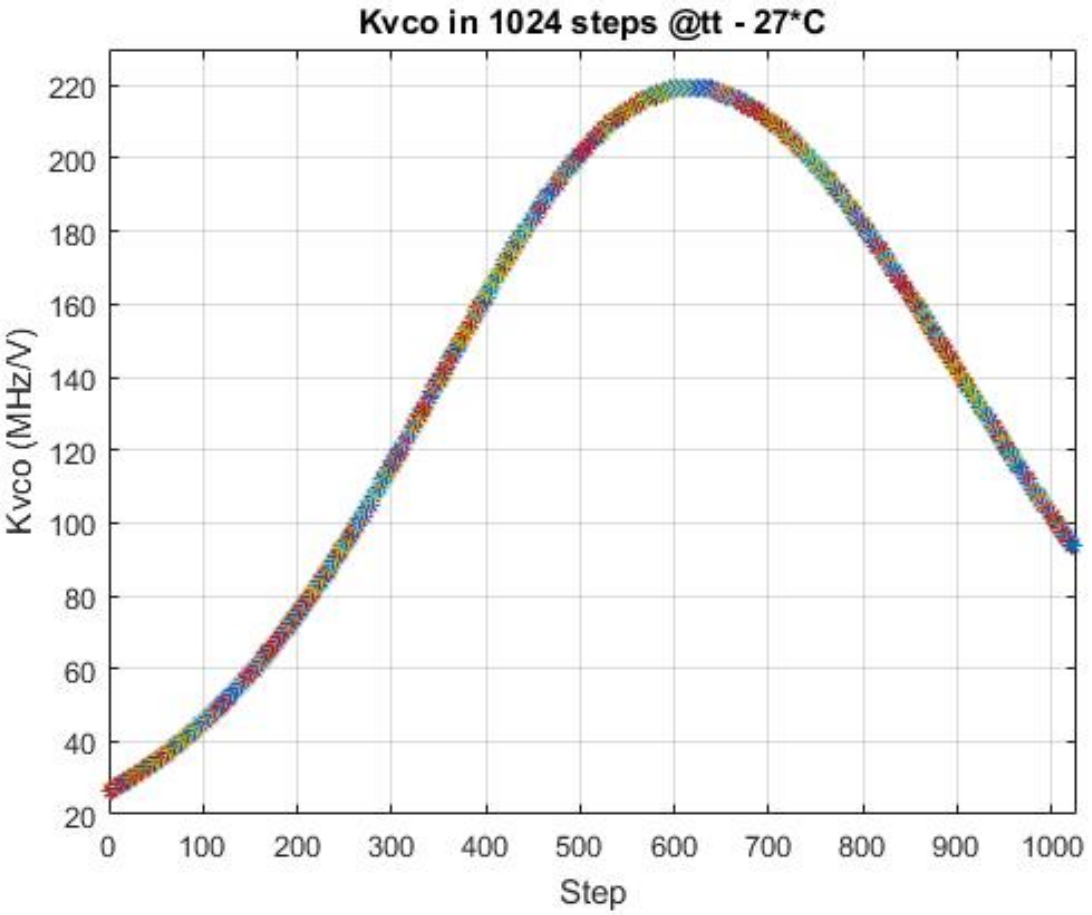

FIGURE 2.7: K_{vco} of VCO @tt $-27^{*}C$

Few important parameters such as output frequency, Phase noise, Peak-peak value of output sinusoidal, Power consumed by DCO simulated over all corners and temperatures are shown in AppendixB.

Chapter 3

Fully Digital Control

The analog tuning control to the Voltage controlled oscillator can be avoided by replacing the varactor with a fine tuning capacitor bank i.e the digitally controlled capacitor array is extended in resolution to the finest capacitor such that the analog voltage-controlled varactor could be completely eliminated.

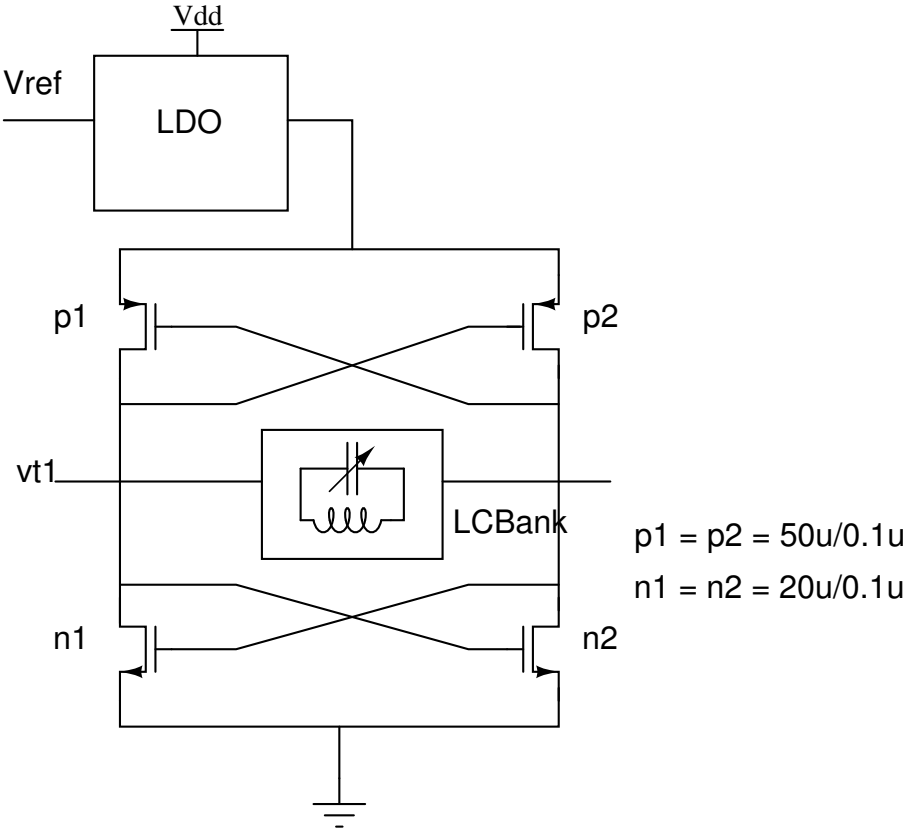

FIGURE 3.1: DCO Schematic

3.1 Varactor

The varactor in the voltage controlled oscillator is chosen such that there should not be any dead zone in the tuning range and the minimum value of ΔC should be greater than the step size in the capacitor bank. The varactor used is a nMOS capacitor in a n-well which has a monotonic change in capacitance with applied bias voltage. The gate of the varactor (positive) is connected to a fixed bias voltage of 600mV, and the input to the VCO is given to the negative terminal of the varactor. Very high value of varactors give rise to high values of Kvco. Kvco is kept between 100 - 200 MHz/V.[5]

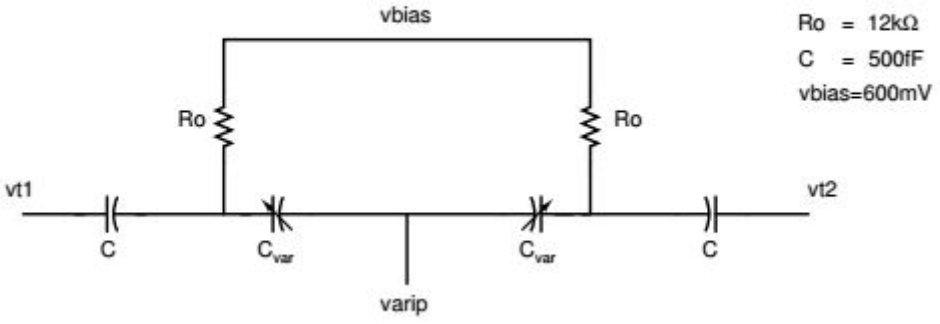

FIGURE 3.2: Varactor Biasing

3.2 Capacitor Bank

The varactor control has been replaced with a fine tuning capacitor bank to tune the frequencies in a discrete fashion. The implementation of the capacitor bank is shown in Figure3.2. The switches in the capacitor bank should be as large as possible so that it does not degrade the Q of the bank. MOM capacitor is used owing to its high density and better Q for the same value of capacitor in MIM type. The capacitor bank ha capacitance of sizes 1X, 2X, 4X, 8X, 16X, 32x, 64X and 128X where X is the minimum value of the single ended capacitor whose value is $3fF$.

The minimum value of the capacitor (single ended) used in the bank is $3fF$ and the maximum value is $384fF$. An external capacitor of $176fF$ is used for tuning correction. When all the capacitors in the bank are turned off, the tuning is determined by the external capacitor and the overlap capacitance of the switches.

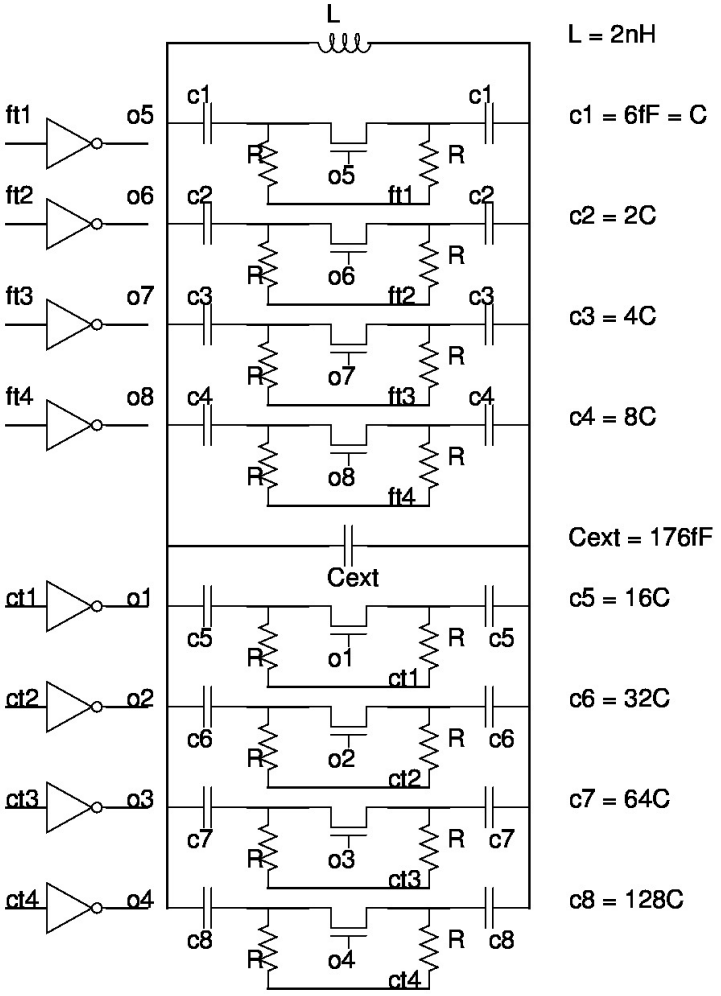

FIGURE 3.3: LC bank

3.2.1 Quality Factor

The approximate Q of the tank is given by the following formula:

$$\frac{1}{Q_{tank}} = \frac{1}{Q_L} + \frac{C_1}{C_{total}Q_1} + \frac{C_2}{C_{total}Q_2} + ... + \frac{C_n}{C_{total}Q_n} \tag{3.1}$$

$$C_{total} = C_1 + C_2 + C_3 + ... + C_n \tag{3.2}$$

In the above equation the capacitor values are differential. The effective parallel resistance and the Q_{tank} are related as given by the following formula:

$$Q_{tank} = \frac{R_p}{\omega_0 L} \tag{3.3}$$

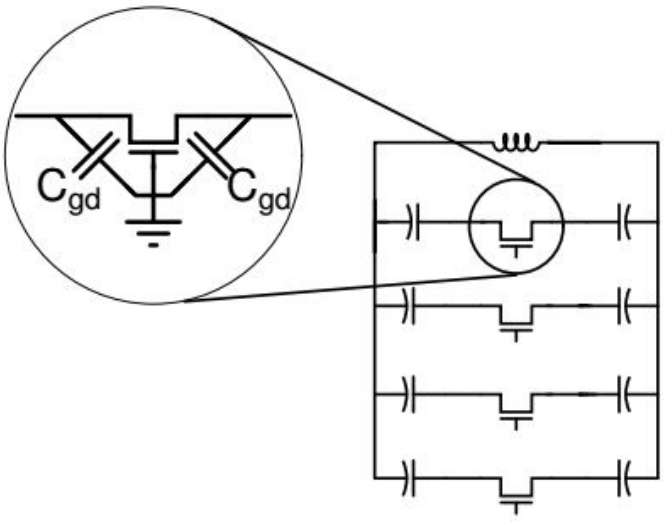

FIGURE 3.4: MOS switch parasitic

The calculation results in Q_{tank} of 14. Now the R_p of the tank is 880Ω. For a fixed value of current in the VCO the differential output swing is given by

$$V_{out} = \frac{2}{\pi} I_0 R_p \tag{3.4}$$

By rule of thumb, the capacitance associated with the gate-drain overlap of the switch is kept ten times lower than the single ended capacitor of the particular branch in off state.The on-state overlap capacitance does not matter as the MOS switch acts as an effective short for the current.

3.3 Simulation Results

It can be easily observed that when the input bit is LOW, the output of the inverter is HIGH and the MOSFET switch is ON. This connects the capacitance to the bank. On the other hand when the input bit is HIGH, the output of the inverter is LOW and the MOSFET switch is OFF. This does not contribute the capacitor value to the bank.

The output frequency of the Digitally controlled oscillator when the input bits are toggled in an increasing fashion are shown in Figure3.4. The frequency step in the output frequency

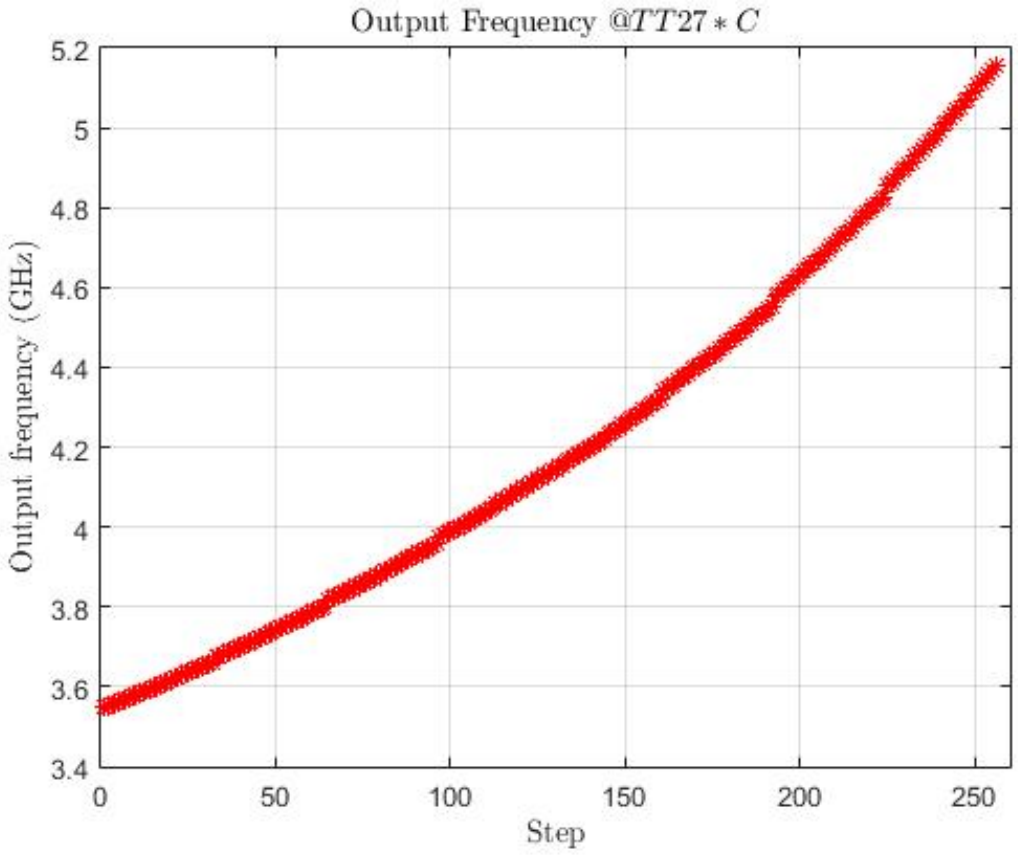

FIGURE 3.5: Output frequency of DCO over 8 bit word

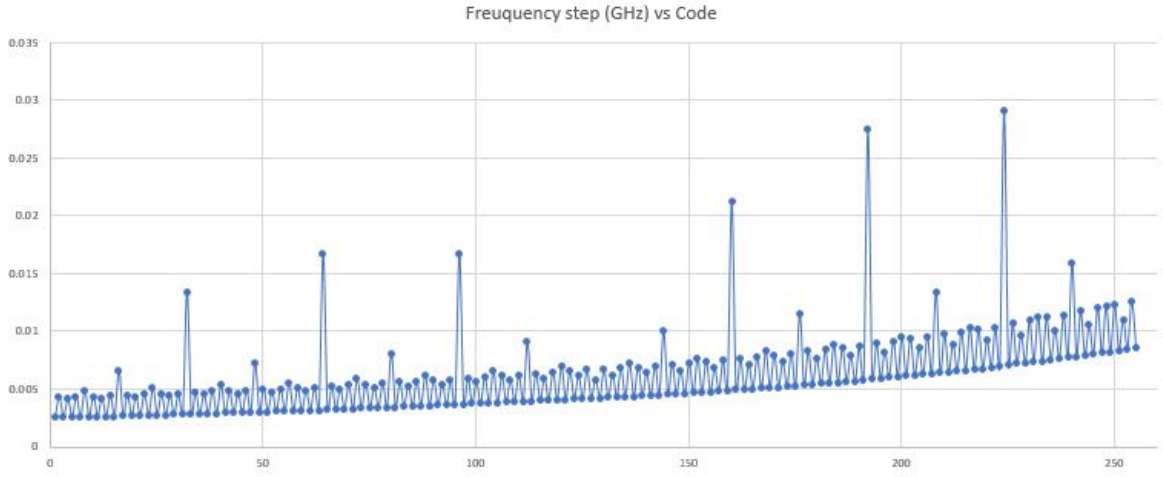

FIGURE 3.6: Frequency step Vs code

versus the digital code is shown in the Figure3.5. The maximum output frequency step is 29.1MHz. The minimum output frequency step is 2.5MHz.

Few important parameters such as output frequency, Phase noise, Peak-peak value of output sinusoidal, Power consumed by DCO simulated over all corners and temperatures are shown

in AppendixC.

Chapter 4

Conclusions

Two different ways of avoiding direct analog control to the VCO are implemented in the TSMC 65nm CMOS technology. The frequency range of operation is assumed to be that of the Bluetooth. The phase noise requirement for Bluetooth is $-121dBc/Hz$ at $2MHz$ offset @2.4GHz. This is same as $-115dBc'Hz$ at $2MHz$ offset @4.8GHz. Quadrature carriers are obtained by dividing the VCO output by a factor of 2.

The required tuning range of 4.8GHz to 5GHz across process corners is achieved. This is done by using a DAC with VCO to mask the analog control and also by replacing continuous varactor tuning with a fine tuning capacitor bank.

Appendix A

LDO[5]

A.1 Design of LDO

The supply rail is noisy and cannot be used to power the DCO. The supply noise needs to be filtered out. Thus we need an LDO to power the VCO. The LDO needs to be of low output noise and better PSSR. In this design, a two stage OPAMP driving an output PMOS transistor which provides current to the DCO. The phase noise of the VCO at $2MHz$ offset is to be -121dBC/Hz at 2.4GHz. The LDO bandwidth therefore should be maintained above 2MHz. By burning more current in the First stage or increasing the g_m of the input stage transistors the output noise can be reduced.

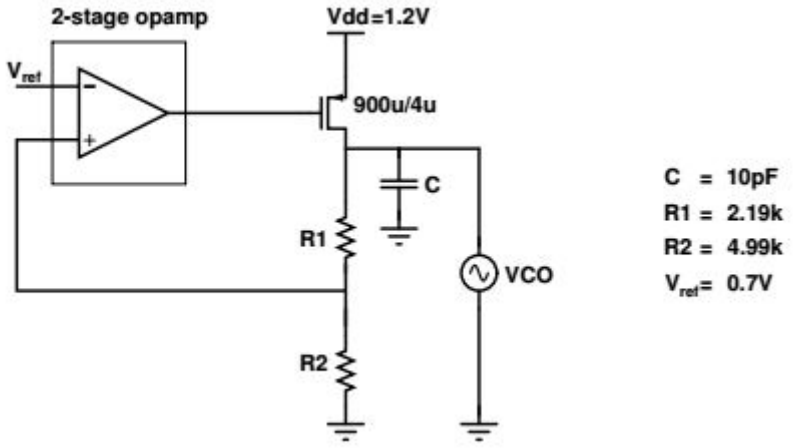

FIGURE A.1: LDO with VCO load

A.2 Implementation of LDO

The schematic of the two-stage OPAMP used in the LDO is given below.

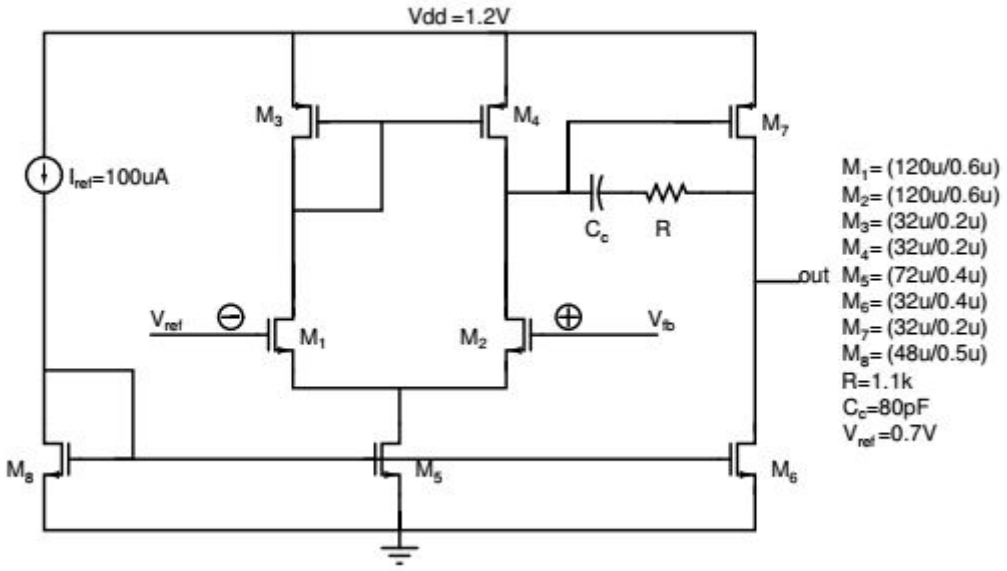

FIGURE A.2: 2-stage OPAMP

The two stage OPAMP is used in the LDO. A miller capacitor (moscap) of 80fF is used for stability. The loop gain and phase plot are shown in FigureA.3.

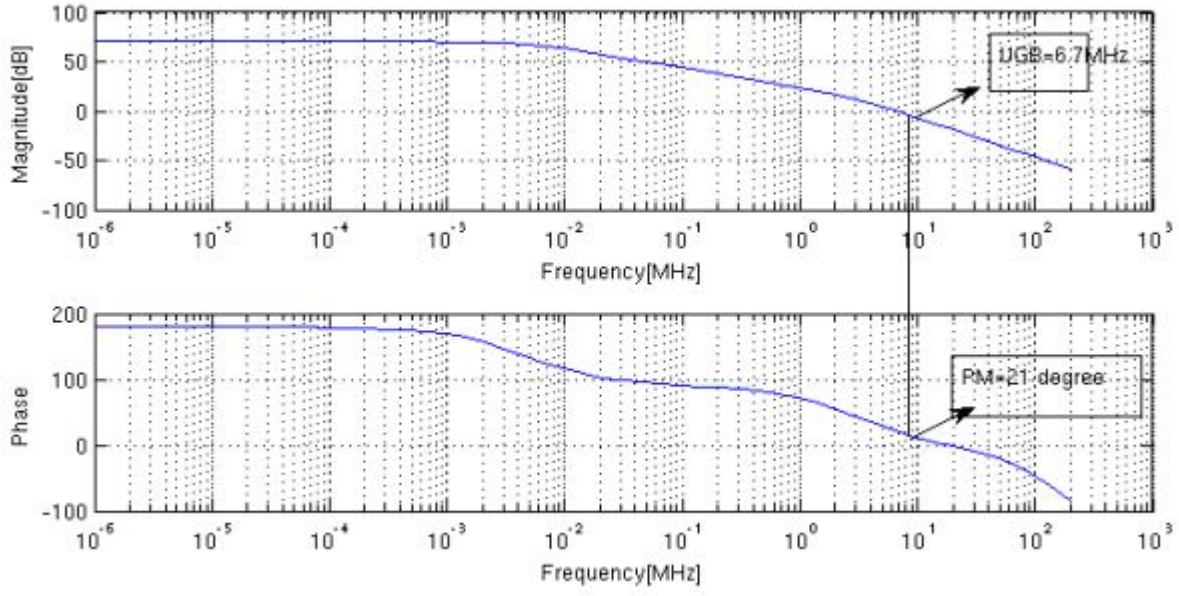

FIGURE A.3: Loop gain and phase plot without load

The bandwidth of the LDO without loading is 6.7MHz. The DC gain of the loop is 77dB and phase margin 21^0.

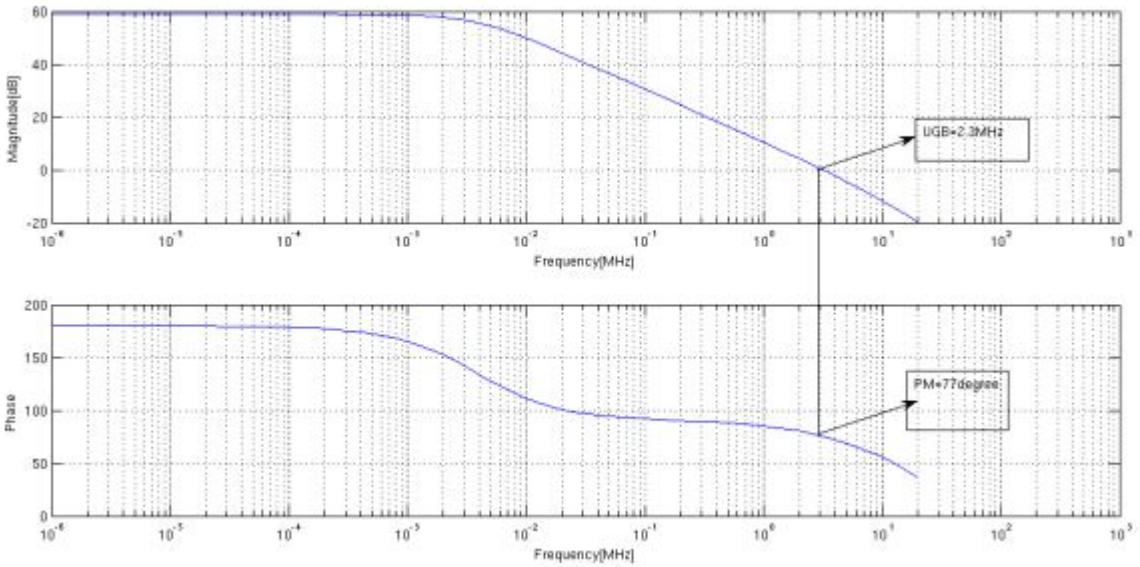

FIGURE A.4: Loop gain and phase plot with load

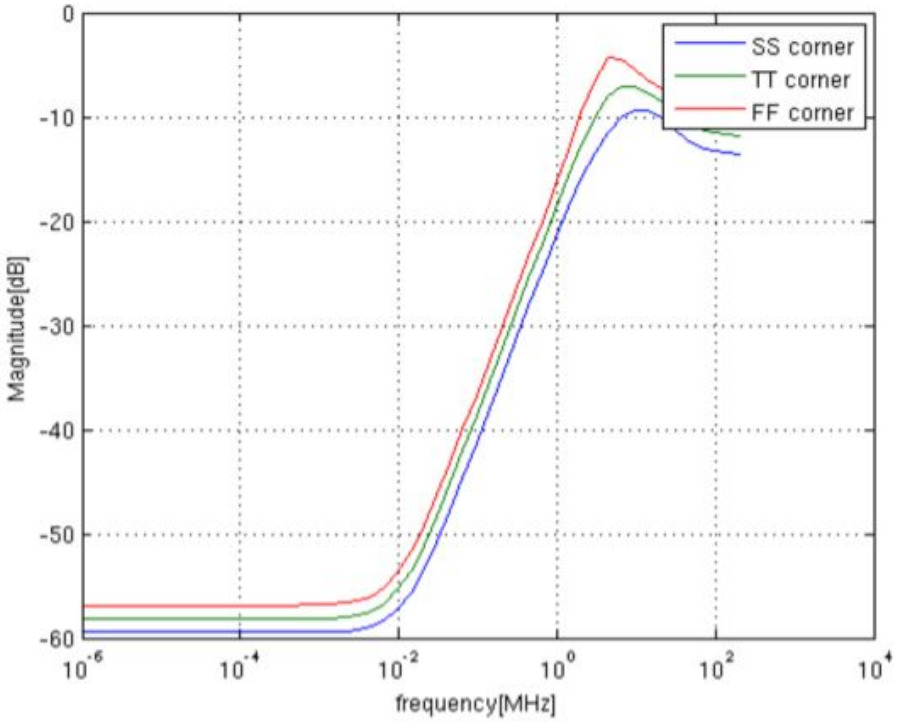

FIGURE A.5: PSSR plot

The bandwidth of the LDO with VCO load is 2.3MHz. The DC gain of the loop is 55dB and phase margin is maintained at 77^0 for stability. If the phase margin is kept too low, then

there is a sudden voltage drop at the output during the start of the circuit and the VCO may stop oscillating. To avoid this a good phase margin is maintained. The LDO needs to reject the supply noise and a good PSSR is required to avoid degradation of PN due to supply noise. As the loop gain is maintained high upto the bandwidth, any noise injected will be rejected by the LDO. The FigureA.5 shows the PSSR of the LDO with VCO load. A worst case phase noise degradation of 1.8dBC/Hz is observed for 9nV/sqrt(Hz) of white noise.

The LDO noise is shown in FigureA.6. The output noise at 2MHz is 12nV/sqrt(Hz).

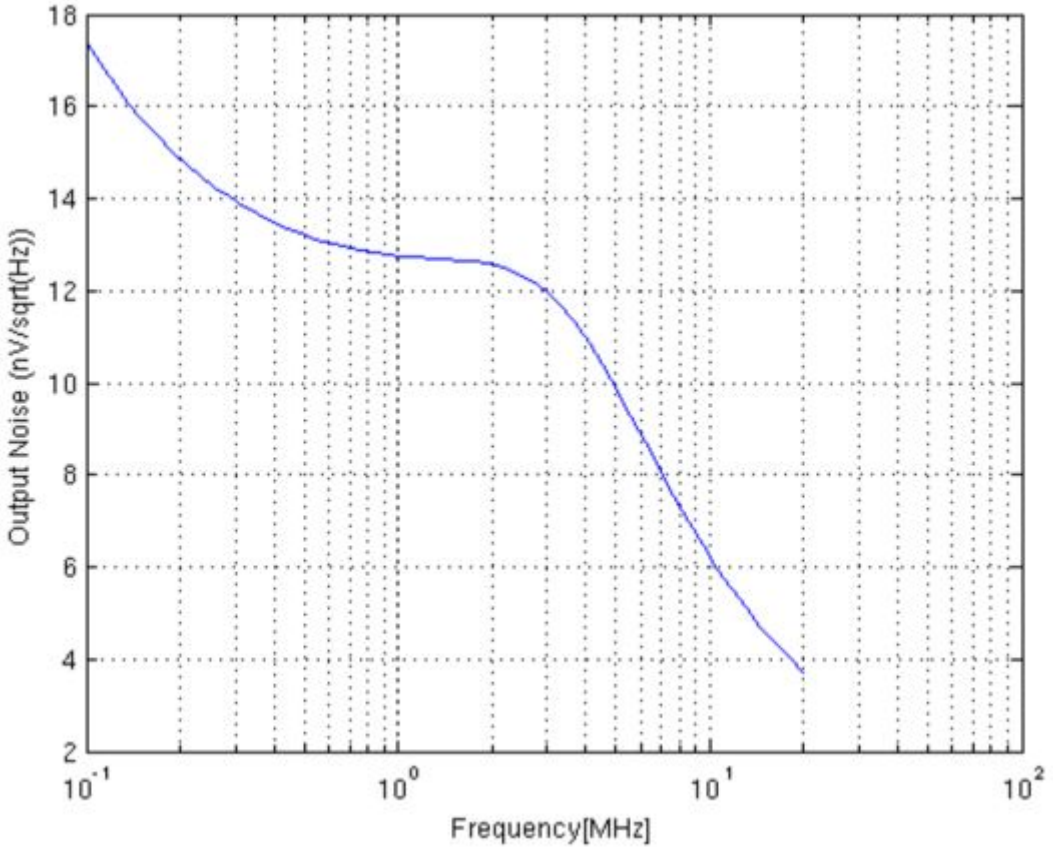

FIGURE A.6: LDO noise plot

Appendix B

Simulation results DAC with VCO

The tables presented below gives an idea of choice of bits for the capacitor bank and resistor bank in respective corners. The first set of rows of each table gives the idea of bits to be used for tuning in 5GHz range and lower four rows gives an idea of tuning in 4.8GHz range. Here ct1 ct2 ct3 ct4 is the capacitor bank bits where ct1 is LSB and ct4 is MSB. R1 R2 corresponds to the resistor bank where R1 is MSB (300Ω) and R2 is LSB (150Ω)

Note: The frequency range of operation is assumed to be that of the Bluetooth. The phase noise requirement for Bluetooth is $-121dBc/Hz$ at $2MHz$ offset @2.4GHz. This is same as $-115dBc'Hz$ at $2MHz$ offset @4.8GHz. Quadrature carriers are obtained by dividing the VCO output by a factor of 2.

VCO cannot be operated in the region where the specs are not met. However, to tune the required frequency range it can be operated at R! R2 = —1 1— and —1 0—

TABLE B.1: SS-corner simulation results at 0^0C

SS 0c						
R1 R2	C4 C3 C2 C1	VCO i/p (V)	Output Freq(GHz)	PN@2MHz (dBc/Hz)	Power VCO(uW)	Power LDO VCO(uW)
1 1	1 1 0 1	1.2	5.073	-117.3	525.1	1052
		0	4.887	-119	530	1058
1 0	1 1 0 1	1.2	5.099	-116.8	408	912.1
		0	4.91	-119.4	386.9	886.9
0 1	1 1 0 1	1.2	5.11	-118.7	284.9	765.2
		0	4.901	-113(spec not met)	213	679.6
1 1	1 0 1 1	1.2	4.914	-118	529.3	1056.8
		0	4.744	-120	530.8	1058.5
1 0	1 0 1 1	1.2	4.939	-117.8	397.5	899.5
		0	4.763	-121.1	355.9	849.9
0 1	1 0 1 1	1.2	4.939	-114.4	233.4	703.9
		0	4.749	-112(spec not met)	189.6	651.6

TABLE B.2: SS corner simulation results at 80^0C

SS 80c						
R1 R2	C4 C3 C2 C1	VCO i/p (V)	Output Freq(GHz)	PN@2MHz (dBc/Hz)	Power VCO(uW)	Power LDO VCO(uW)
1 1	1 1 0 1	1.2	5.062	-117	532.8	1075
		0	4.884	-118.5	530.8	1073
1 0	1 1 0 1	1.2	5.087	-116.9	391.5	906.9
		0	4.9	-117.6	358.3	867.3
0 1	1 1 0 1	1.2	5.089	-115.1	286.1	781.4
		0	4.891	-112.4(spec not met)	248.6	736.7
1 1	1 0 1 1	1.2	4.905	-118	532.7	1074.9
		0	4.741	-119	526.1	1067.1
1 0	1 0 1 1	1.2	4.925	-117.6	373.3	885.2
		0	4.75	-115.9	332.4	836.5
0 1	1 0 1 1	1.2	4.92	-113.5	261.1	751.6
		0	4.741	-111(spec not met)	232.8	718

TABLE B.3: TT corner simulation results at 0^0C

TT 0c						
R1 R2	C4 C3 C2 C1	VCO i/p (V)	Output Freq(GHz)	PN@2MHz (dBc/Hz)	Power VCO(uW)	Power LDO +VCO(uW)
1 1	1 0 1 0	1.2	5.073	-118	637.3	1215
		0	4.895	-119.7	658.6	1240
1 0	1 0 1 0	1.2	5.092	-117.7	539.9	1099
		0	4.912	-119.3	553.9	1115
0 1	1 0 1 0	1.2	5.108	-117.8	462.7	1007
		0	4.926	-119.3	470.5	1016
0 0	1 0 1 0	1.2	5.122	-117.6	407.6	940.9
		0	4.938	-119.1	409.7	943.5
1 1	1 0 0 1	1.2	5.005	-118.3	641.2	1220
		0	4.834	-119.9	661.6	1244
1 0	1 0 0 1	1.2	5.024	-118.1	542.7	1102
		0	4.851	-119.6	555.8	1118
0 1	1 0 0 1	1.2	5.039	-118.1	464.4	1009
		0	4.864	-119.6	471.4	1017
0 0	1 0 0 1	1.2	5.053	-117.9	408.3	941.8
		0	4.876	-119.4	409.6	943.3
1 1	1 0 0 0	1.2	4.939	-118.7	640.9	1219
		0	4.774	-120.2	660.8	1243
1 0	1 0 0 0	1.2	4.957	-118.4	542.5	1102
		0	4.79	-119.9	555.4	1117
0 1	1 0 0 0	1.2	4.972	-118.4	464.3	1009
		0	4.803	-119.9	471.2	1017
0 0	1 0 0 0	1.2	4.985	-118	408.3	941.7
		0	4.814	-119.7	409.6	943.3
1 1	0 1 1 1	1.2	4.873	-119	663	1246
		0	4.713	-120.5	679.4	1265
1 0	0 1 1 1	1.2	4.891	-118.6	556.9	1119
		0	4.73	-120.1	566.3	1130
0 1	0 1 1 1	1.2	4.906	-119	472.1	1018
		0	4.742	-120	475.1	1021
0 0	0 1 1 1	1.2	4.919	-118.5	409.9	943.7
		0	4.754	-119.9	405.7	938.7

Because at higher currents phase noise is over met and more power is consumed, VCO can be operated with lower currents to reduce power consumption and still meet the required tuning range.

TABLE B.4: TT corner simulation results at 80^0C

TT 80c						
R1 R2	C4 C3 C2 C1	VCO i/p (V)	Output Freq(GHz)	PN@2MHz (dBc/Hz)	Power VCO(uW)	Power LDO VCO(uW)
1 1	1 0 1 0	1.2	5.063	-118.2	662.9	1259
		0	4.893	-119.7	682.9	1283
1 0	1 0 1 0	1.2	5.084	-117.5	547.6	1122
		0	4.911	-118.9	558	1135
0 1	1 0 1 0	1.2	5.099	-117.2	467.7	1027
		0	4.924	-118.4	470.9	1031
0 0	1 0 1 0	1.2	5.113	-116.8	403.1	950.1
		0	4.935	-118.1	398.9	945.2
1 1	1 0 0 1	1.2	4.996	-118.5	666.7	1264
		0	4.832	-119.9	685.6	1286
1 0	1 0 0 1	1.2	5.016	-117.8	549.8	1125
		0	4.85	-119.1	559.2	1136
0 1	1 0 0 1	1.2	5.03	-117.4	468.7	1028
		0	4.862	-118.7	471	1031
0 0	1 0 0 1	1.2	5.044	-117.1	402.9	949.9
		0	4.873	-118.3	397.7	943.7
1 1	1 0 0 0	1.2	4.931	-118.7	667.1	1264
		0	4.772	-120.2	685.5	1286
1 0	1 0 0 0	1.2	4.95	-118.1	550	1125
		0	4.79	-119.4	559.2	1136
0 1	1 0 0 0	1.2	4.964	-117.7	468.8	1028
		0	4.801	-118.9	471	1031
0 0	1 0 0 0	1.2	4.977	-117	402.8	949.8
		0	4.812	-118.6	397.7	943.7
1 1	0 1 1 1	1.2	4.865	-118.9	686.2	1287
		0	4.712	-120.2	700.2	1304
1 0	0 1 1 1	1.2	4.885	-118.2	559.7	1137
		0	4.73	-119.3	564.3	1142
0 1	0 1 1 1	1.2	4.898	-118	471.2	1031
		0	4.74	-118.9	468.4	1028
0 0	0 1 1 1	1.2	4.91	-117.5	397.8	943.8
		0	4.749	-118.5	386.3	930.1

Because at higher currents phase noise is over met and more power is consumed, VCO can be operated with lower currents to reduce power consumption and still meet the required tuning range.

TABLE B.5: FF corner simulation results at 0^0C

FF 0c						
R1 R2	C4 C3 C2 C1	VCO i/p (V)	Output Freq(GHz)	PN@2MHz (dBc/Hz)	Power VCO(uW)	Power LDO +VCO(uW)
1 1	0 1 0 1	1.2	5.045	-118.5	770.7	1410
		0	4.897	-120	802.3	1448
1 0	0 1 0 1	1.2	5.058	-118.1	676.8	1298
		0	4.892	-119.5	702.1	1328
0 1	0 1 0 1	1.2	5.074	-118	589.5	1194
		0	4.905	-119.4	608.3	1217
0 0	0 1 0 1	1.2	5.084	-117.9	535.7	1130
		0	4.915	-119.2	551.3	1149
1 1	0 1 0 0	1.2	4.991	-118.7	767.8	1407
		0	4.83	-120.2	799	1444
1 0	0 1 0 0	1.2	5.004	-118.3	674.5	1296
		0	4.842	-119.8	699.5	1325
0 1	0 1 0 0	1.2	5.019	-118.2	587.8	1192
		0	4.855	-119.6	606.4	1214
0 0	0 1 0 0	1.2	5.029	-118.1	534.3	1128
		0	4.865	-119.5	549.8	1147
1 1	0 0 1 1	1.2	4.94	-119	778.7	1420
		0	4.784	-120.4	808.6	1456
1 0	0 0 1 1	1.2	4.953	-118.6	683.3	1306
		0	4.796	-120	707.1	1335
0 1	0 0 1 1	1.2	4.968	-118.4	594.5	1200
		0	4.809	-119.8	612.1	1221
0 0	0 0 1 1	1.2	4.978	-118.3	539.9	1135
		0	4.818	-119.7	554.4	1152
1 1	0 0 1 0	1.2	4.89	-119.2	775.8	1416
		0	4.738	-120.6	805.3	1452
1 0	0 0 1 0	1.2	4.902	-118.8	680.9	1303
		0	4.749	-120.2	704.5	1331
0 1	0 0 1 0	1.2	4.916	-118.7	592.7	1198
		0	4.762	-120	610.2	1219
0 0	0 0 1 0	1.2	4.925	-118.6	538.5	1133
		0	4.771	-119.9	552.9	1150

Because at higher currents phase noise is over met and more power is consumed, VCO can be operated with lower currents to reduce power consumption and still meet the required tuning range.

TABLE B.6: FF corner simulation results at 80^0C

FF 80c						
R1 R2	C4 C3 C2 C1	VCO i/p (V)	Output Freq(GHz)	PN@2MHz (dBc/Hz)	Power VCO(uW)	Power LDO +VCO(uW)
1 1	0 1 0 1	1.2	5.039	-119.2	808	1469
		0	4.88	-120.6	841.2	1508
1 0	0 1 0 1	1.2	5.053	-118.6	698.4	1338
		0	4.893	-120	723.4	1368
0 1	0 1 0 1	1.2	5.068	-118.1	607.6	1230
		0	4.906	-119.4	625.5	1251
0 0	0 1 0 1	1.2	5.078	-117.7	545.4	1156
		0	4.916	-118.9	559.2	1172
1 1	0 1 0 0	1.2	4.985	-119.4	806.2	1467
		0	4.831	-120.9	839	1506
1 0	0 1 0 0	1.2	4.999	-118.8	697	1337
		0	4.844	-120.2	721.7	1366
0 1	0 1 0 0	1.2	5.013	-118.3	606.5	1229
		0	4.856	-119.6	624.3	1250
0 0	0 1 0 0	1.2	5.023	-118	544.6	1155
		0	4.866	-119.2	558.3	1171
1 1	0 0 1 1	1.2	4.934	-119.6	816.4	1479
		0	4.785	-121	847.6	1516
1 0	0 0 1 1	1.2	4.948	-119	704.8	1346
		0	4.797	-120	728.1	1374
0 1	0 0 1 1	1.2	4.962	-118.5	612.3	1236
		0	4.81	-119.7	628.8	1255
0 0	0 0 1 1	1.2	4.972	-118.1	549.1	1160
		0	4.819	-119.3	561.7	1175
1 1	0 0 1 0	1.2	4.884	-119.9	814.5	1476
		0	4.739	-121.2	845.4	1513
1 0	0 0 1 0	1.2	4.897	-119.2	703.4	1344
		0	4.751	-120.5	726.5	1372
0 1	0 0 1 0	1.2	4.911	-118.7	611.3	1234
		0	4.763	-119.9	627.7	1254
0 0	0 0 1 0	1.2	4.921	-118.4	548.3	1160
		0	4.772	-119.5	560.8	1174

Because at higher currents phase noise is over met and more power is consumed, VCO can be operated with lower currents to reduce power consumption and still meet the required tuning range.

TABLE B.7: FS corner simulation results at 0^0C

FS 0c						
R1 R2	C4 C3 C2 C1	VCO i/p (V)	Output Freq(GHz)	PN@2MHz (dBc/Hz)	Power VCO(uW)	Power LDO+VCO(uW)
1 1	1 0 1 0	1.2	5.076	-118.3	635.6	1218
		0	4.898	-120	657.7	1245
1 0	1 0 1 0	1.2	5.094	-118	539.9	1104
		0	4.914	-119.7	554.7	1122
0 1	1 0 1 0	1.2	5.11	-118	463.9	1013
		0	4.927	-119.6	472.1	1023
0 0	1 0 1 0	1.2	5.123	-117.8	408.9	947.8
		0	4.939	-119.3	411.2	950.6
1 1	1 0 0 1	1.2	5.008	-118.6	639.5	1223
		0	4.837	-120.3	660.7	1248
1 0	1 0 0 1	1.2	5.026	-118.3	542.7	1107
		0	4.852	-119.9	556.6	1124
0 1	1 0 0 1	1.2	5.041	-118.3	465.6	1015
		0	4.865	-119.8	473.1	1024
0 0	1 0 0 1	1.2	5.053	-118.1	409.7	948.8
		0	4.876	-119.6	411.2	950.5
1 1	1 0 0 0	1.2	4.942	-119	639	1222
		0	4.777	-120.6	659.7	1247
1 0	1 0 0 0	1.2	4.959	-119	542.3	1107
		0	4.792	-120.2	556	1123
0 1	1 0 0 0	1.2	4.973	-119	465.4	1015
		0	4.804	-120.1	472.8	1024
0 0	1 0 0 0	1.2	4.985	-118.4	409.6	948.6
		0	4.815	-119.8	411.2	950.5
1 1	0 1 1 1	1.2	4.875	-119.3	662.1	1250
		0	4.716	-120.8	679.2	1270
1 0	0 1 1 1	1.2	4.892	-118.9	557.7	1125
		0	4.731	-120.4	567.7	1137
0 1	0 1 1 1	1.2	4.906	-118.8	473.7	1025
		0	4.743	-120.2	477	1029
0 0	0 1 1 1	1.2	4.919	-118.6	411.5	950.9
		0	4.754	-120.1	407.5	946.1

Because at higher currents phase noise is over met and more power is consumed, VCO can be operated with lower currents to reduce power consumption and still meet the required tuning range.

TABLE B.8: FS corner simulation results 80^0C

FS 80c						
R1 R2	C4 C3 C2 C1	VCO i/p (V)	Output Freq(GHz)	PN@2MHz (dBc/Hz)	Power VCO(uW)	Power LDO VCO(uW)
1 1	1 0 1 0	1.2	5.066	-118.4	662.1	1263
		0	4.895	-119.9	683.2	1288
1 0	1 0 1 0	1.2	5.086	-117.7	548.6	1128
		0	4.913	-119.1	559.9	1142
0 1	1 0 1 0	1.2	5.1	-117.3	469.7	1034
		0	4.925	-118.6	473.6	1039
0 0	1 0 1 0	1.2	5.114	-117	405.1	957.4
		0	4.936	-118.3	401.5	953.1
1 1	1 0 0 1	1.2	4.999	-118.6	665.9	1268
		0	4.834	-120.2	685.9	1292
1 0	1 0 0 1	1.2	5.018	-118	550.8	1131
		0	4.851	-119.3	561.1	1143
0 1	1 0 0 1	1.2	5.032	-117.6	470.8	1036
		0	4.863	-118.9	473.7	1039
0 0	1 0 0 1	1.2	5.044	-117.3	405	957.3
		0	4.874	-118.5	400.5	951.9
1 1	1 0 0 0	1.2	4.933	-118.9	666.2	1268
		0	4.775	-120.4	685.7	1291
1 0	1 0 0 0	1.2	4.951	-118	551	1131
		0	4.791	-119.6	561	1143
0 1	1 0 0 0	1.2	4.965	-118	470.8	1036
		0	4.802	-119.1	473.7	1039
0 0	1 0 0 0	1.2	4.977	-117.5	405	957.2
		0	4.813	-118.8	400.5	951.9
1 1	0 1 1 1	1.2	4.867	-119.1	686.4	1292
		0	4.714	-120.5	701.4	1310
1 0	0 1 1 1	1.2	4.885	-118.4	561.5	1144
		0	4.73	-119.6	567	1150
0 1	0 1 1 1	1.2	4.898	-118	474	1039
		0	4.741	-119.1	471.8	1037
0 0	0 1 1 1	1.2	4.91	-117.7	400.7	952.1
		0	4.749	-118.7	390.3	939.7

Because at higher currents phase noise is over met and more power is consumed, VCO can be operated with lower currents to reduce power consumption and still meet the required tuning range.

TABLE B.9: SF corner simulation results at 0^0C

SF 0c						
R1 R2	C4 C3 C2 C1	VCO i/p (V)	Output Freq(GHz)	PN@2MHz (dBc/Hz)	Power VCO(uW)	Power LDO +VCO(uW)
1 1	1 0 1 0	1.2	5.066	-117.7	641.8	1215
		0	4.889	-119.3	661.9	1239
1 0	1 0 1 0	1.2	5.087	-117.4	541.4	1095
		0	4.908	-118.9	554.1	1110
0 1	1 0 1 0	1.2	5.103	-117.6	461.9	1000
		0	4.922	-119	468.6	1008
0 0	1 0 1 0	1.2	5.118	-117.5	405.6	933.1
		0	4.934	-118.9	406.9	934.5
1 1	1 0 0 1	1.2	4.999	-118	645.7	1219
		0	4.828	-119.6	664.9	1.242
1 0	1 0 0 1	1.2	5.02	-117.7	544	1096
		0	4.847	-119.2	555.9	1112
0 1	1 0 0 1	1.2	5.035	-117.9	463.4	1002
		0	4.86	-119.3	469.4	1009
0 0	1 0 0 1	1.2	5.049	-118	406.2	933.8
		0	4.873	-119.2	406.6	934.2
1 1	1 0 0 0	1.2	4.934	-118.4	645.6	1219
		0	4.769	-119.8	664.3	1242
1 0	1 0 0 0	1.2	4.953	-118.1	544	1098
		0	4.787	-119.5	555.6	1112
0 1	1 0 0 0	1.2	4.968	-118.2	463.4	1002
		0	4.8	-119.5	469.2	1009
0 0	1 0 0 0	1.2	4.982	-118.1	406.2	933.8
		0	4.812	-119.5	406.6	934.2
1 1	0 1 1 1	1.2	4.868	-118.7	666.3	1244
		0	4.709	-120.1	681.6	1262
1 0	0 1 1 1	1.2	4.888	-118.3	557	1114
		0	4.727	-119.7	565.3	1124
0 1	0 1 1 1	1.2	4.903	-118.4	470	1010
		0	4.74	-119.7	472	1012
0 0	0 1 1 1	1.2	4.916	-118.3	406.8	934.5
		0	4.751	-119.8	401.7	928.4

Because at higher currents phase noise is over met and more power is consumed, VCO can be operated with lower currents to reduce power consumption and still meet the required tuning range.

TABLE B.10: SF corner simulation results at 80^0C

SF 80c						
R1 R2	C4 C3 C2 C1	VCO i/p (V)	Output Freq(GHz)	PN@2MHz (dBc/Hz)	Power VCO(uW)	Power LDO VCO(uW)
1 1	1 0 1 0	1.2	5.058	-118	665.8	1258
		0	4.888	-119.4	684.3	1280
1 0	1 0 1 0	1.2	5.08	-117.3	547.5	1117
		0	4.908	-118.6	556.4	1128
0 1	1 0 1 0	1.2	5.094	-117	465.6	1019
		0	4.92	-118.2	467.5	1022
0 0	1 0 1 0	1.2	5.109	-116.7	400	941.4
		0	4.932	-117.9	394.9	935.3
1 1	1 0 0 1	1.2	4.991	-118.3	669.5	1264
		0	4.827	-119.7	686.9	1283
1 0	1 0 0 1	1.2	5.013	-117.6	549.5	1119
		0	4.847	-118.8	557.4	1129
0 1	1 0 0 1	1.2	5.027	-117.3	466.3	1020
		0	4.858	-118.4	467.4	1022
0 0	1 0 0 1	1.2	5.04	-117	399.6	940.9
		0	4.87	-118.1	393.5	933.7
1 1	1 0 0 0	1.2	4.926	-118.5	670	1263
		0	4.768	-119.9	686.9	1283
1 0	1 0 0 0	1.2	4.947	-117.8	549.8	1120
		0	4.787	-119.1	557.5	1129
0 1	1 0 0 0	1.2	4.96	-117.5	466.4	1021
		0	4.798	-118.7	467.4	1022
0 0	1 0 0 0	1.2	4.974	-117.2	399.5	940.8
		0	4.809	-118.4	393.4	933.5
1 1	0 1 1 1	1.2	4.861	-118.7	687.5	1284
		0	4.708	-119.9	700.1	1299
1 0	0 1 1 1	1.2	4.882	-117.9	557.9	1129
		0	4.727	-119.1	561.2	1133
0 1	0 1 1 1	1.2	4.895	-117.6	467.6	1022
		0	4.737	-118.6	463.6	1017
0 0	0 1 1 1	1.2	4.907	-117.3	393.4	933.6
		0	4.746	-118.2	381.5	919.4

Because at higher currents phase noise is over met and more power is consumed, VCO can be operated with lower currents to reduce power consumption and still meet the required tuning range.

Appendix C

Fully Digital Control

The tables presented below gives an idea of choice of bits for the Coarse capacitor bank and fine capacitor bank in respective corners. Here ct1 ct2 ct3 ct4 are the coarse capacitor bank bits and ft1 ft2 ft3 ft4 are the fine capacitor bank bits.

TABLE C.1: SS corner simulation results at 80^0C

SS 80c						
C4C3C2C1	f4f3f2f1	Freq (GHz)	Phase noise @2MHz	Vpeak-peak (V)	Power DCO (uW)	Power DCO + LDO (uW)
1 1 1 1	1 1 1 1	5.191	-119.5	2.049	1129	1486
	0 0 0 0	5.107	-119.9	2.049	1126	1485
1 1 1 0	1 1 1 1	5.058	-120.1	2.042	1138	1496
	0 0 0 0	4.98	-120.4	2.042	1137	1495
1 1 0 1	1 1 1 1	4.751	-120.9	1.933	1317	1.673
	0 0 0 0	4.686	-121.1	1.934	1311	1668
0 0 1 0	1 1 1 1	3.488	-123.2	1.382	1688	2038
	0 0 0 0	3.461	-123.4	1.393	1689	2038
0 0 0 1	1 1 1 1	3.378	-123.4	1.339	1682	2032
	0 0 0 0	3.354	-123.7	1.351	1684	2034
0 0 0 0	1 1 1 1	3.34	-123.7	1.348	1684	2034
	0 0 0 0	3.316	-123.9	1.36	1686	2035

TABLE C.2: SS corner simulation results at 0^0C

SS 0c						
C4C3C2C1	f4f3f2f1	Freq (GHz)	Phase noise @2MHz	Vpeak-peak (V)	Power DCO (uW)	Power DCO + LDO (uW)
1 1 1 1	1 1 1 1	5.197	-118.4	2.105	1043	1392
	0 0 0 0	5.112	-118.7	2.108	1040	1389
1 1 1 0	1 1 1 1	5.063	-119	2.101	1051	1399
	0 0 0 0	4.984	-119.3	2.104	1048	1396
1 1 0 1	1 1 1 1	4.754	-120.6	2.024	1214	1561
	0 0 0 0	4.688	-120.8	2.029	1207	1554
0 0 1 0	1 1 1 1	3.486	-125.7	1.661	1682	2026
	0 0 0 0	3.46	-125.9	1.669	1677	2021
0 0 0 1	1 1 1 1	3.377	-126.1	1.634	1696	2040
	0 0 0 0	3.353	-126.3	1.643	1692	2036
0 0 0 0	1 1 1 1	3.336	-126.4	1.642	1692	2037
	0 0 0 0	3.316	-126.6	1.649	1688	2032

TABLE C.3: TT corner simulation results at 80^0C

tt 80c						
C4C3C2C1	f4f3f2f1	Freq (GHz)	Phase noise @2MHz	Vpeak-peak (V)	Power DCO (uW)	Power DCO + LDO (uW)
1 1 1 1	1 1 1 1	5.431	-118.8	2.135	1265	1646
	0 0 0 0	5.357	-119.1	2.136	1262	1643
1 1 1 0	1 1 1 1	5.31	-119.2	2.131	1272	1654
	0 0 0 0	5.24	-119.5	2.133	1269	1650
1 1 0 1	1 1 1 1	4.99	-120.1	2.064	1422	1802
	0 0 0 0	4.94	-120.4	2.066	1416	1796
0 0 1 0	1 1 1 1	3.725	-123.9	1.76	1940	2295
	0 0 0 0	3.701	-124	1.765	1933	2290
0 0 0 1	1 1 1 1	3.61	-124.3	1.74	1962	2313
	0 0 0 0	3.588	-124.4	1.747	1956	2308
0 0 0 0	1 1 1 1	3.573	-124.5	1.744	1957	2309
	0 0 0 0	3.551	-124.6	1.751	1951	2304

TABLE C.4: TT corner simulation results at 0^0C

tt 0c						
C4C3C2C1	f4f3f2f1	Freq (GHz)	Phase noise @2MHz	Vpeak-peak (V)	Power DCO (uW)	Power DCO + LDO (uW)
1 1 1 1	1 1 1 1	5.43	-117.6	2.177	1185	1558
	0 0 0 0	5.355	-117.9	2.178	1181	1553
1 1 1 0	1 1 1 1	5.309	-118.1	2.176	1190	1562
	0 0 0 0	5.238	-118.4	2.177	1185	1557
1 1 0 1	1 1 1 1	4.997	-119.6	2.129	1320	1691
	0 0 0 0	4.939	-119.8	2.13	1312	1684
0 0 1 0	1 1 1 1	3.724	-125.2	1.922	1812	2180
	0 0 0 0	3.699	-125.3	1.928	1803	2171
0 0 0 1	1 1 1 1	3.609	-125.7	1.909	1837	2204
	0 0 0 0	3.587	-125.8	1.914	1828	2196
0 0 0 0	1 1 1 1	3.572	-125.9	1.913	1830	2198
	0 0 0 0	3.551	-126	1.917	1822	2190

TABLE C.5: FF corner simulation results at 80^0C

ff 80c						
C4C3C2C1	f4f3f2f1	Freq (GHz)	Phase noise @2MHz	Vpeak-peak (V)	Power DCO (uW)	Power DCO + LDO (uW)
1 1 1 1	1 1 1 1	5.711	-117.8	2.197	1435	1845
	0 0 0 0	5.647	-118	2.198	1.431	1.841
1 1 1 0	1 1 1 1	5.604	-118.2	2.193	1439	1849
	0 0 0 0	5.543	-118.4	2.197	1434	1844
1 1 0 1	1 1 1 1	5.292	-119.1	2.154	1549	1957
	0 0 0 0	5.241	-119.3	2.156	1542	1951
0 0 1 0	1 1 1 1	4.016	-123.2	1.967	2006	2396
	0 0 0 0	3.993	-123.3	1.973	1999	2389
0 0 0 1	1 1 1 1	3.895	-123.7	1.957	2028	2414
	0 0 0 0	3.874	-123.8	1.961	2021	2408
0 0 0 0	1 1 1 1	3.86	-123.9	1.961	2023	2410
	0 0 0 0	3.84	-124	1.964	2015	2404

TABLE C.6: FF corner simulation results at 0^0C

ff 0c						
C4C3C2C1	f4f3f2f1	Freq (GHz)	Phase noise @2MHz	Vpeak-peak (V)	Power DCO (uW)	Power DCO + LDO (uW)
1 1 1 1	1 1 1 1	5.698	-116.8	2.23	1368	1769
	0 0 0 0	5.634	-117.1	2.231	1.362	1.763
1 1 1 0	1 1 1 1	5.591	-117.3	2.23	1369	1770
	0 0 0 0	5.53	-117.5	2.232	1363	1765
1 1 0 1	1 1 1 1	5.281	-118.6	2.203	1461	1861
	0 0 0 0	5.23	-118.8	2.205	1453	1854
0 0 1 0	1 1 1 1	4.011	-124	2.075	1866	2264
	0 0 0 0	3.988	-124.1	2.078	1857	2255
0 0 0 1	1 1 1 1	3.89	-124.5	2.069	1885	2283
	0 0 0 0	3.87	-124.6	2.07	1877	2274
0 0 0 0	1 1 1 1	3.856	-124.7	2.071	1879	2277
	0 0 0 0	3.836	-124.8	2.074	1871	2268

TABLE C.7: FS corner simulation results at 80^0C

fs 80c						
C4C3C2C1	f4f3f2f1	Freq (GHz)	Phase noise @2MHz	Vpeak-peak (V)	Power DCO (uW)	Power DCO + LDO (uW)
1 1 1 1	1 1 1 1	5.436	-118.7	2.133	1276	1661
	0 0 0 0	5.361	-118.9	2.133	1273	1658
1 1 1 0	1 1 1 1	5.314	-119.1	2.129	1283	1668
	0 0 0 0	5.243	-119.4	2.13	1280	1665
1 1 0 1	1 1 1 1	5.002	-120	2.069	1422	1806
	0 0 0 0	4.942	-120.3	2.07	1416	1800
0 0 1 0	1 1 1 1	3.724	-123.9	1.777	1930	2280
	0 0 0 0	3.699	-124	1.782	1923	2275
0 0 0 1	1 1 1 1	3.609	-124.3	1.759	1950	2295
	0 0 0 0	3.586	-124.5	1.765	1944	2290
0 0 0 0	1 1 1 1	3.572	-124.5	1.764	1945	2292
	0 0 0 0	3.55	-124.7	1.769	1939	2287

TABLE C.8: FS corner simulation results at 0^0C

fs 0c						
C4C3C2C1	f4f3f2f1	Freq (GHz)	Phase noise @2MHz	Vpeak-peak (V)	Power DCO (uW)	Power DCO + LDO (uW)
1 1 1 1	1 1 1 1	5.434	-117.5	2.175	1195	1571
	0 0 0 0	5.358	-117.8	2.176	1190	1567
1 1 1 0	1 1 1 1	5.312	-1118	2.174	1199	1575
	0 0 0 0	5.241	-118.3	2.175	1194	1571
1 1 0 1	1 1 1 1	4.999	-119.5	2.13	1319	1694
	0 0 0 0	4.94	-119.7	2.132	1312	1687
0 0 1 0	1 1 1 1	3.723	-125.1	1.934	1799	2171
	0 0 0 0	3.698	-125.3	1.937	1790	2162
0 0 0 1	1 1 1 1	3.608	-125.7	1.924	1822	2194
	0 0 0 0	3.585	-125.8	1.928	1813	2185
0 0 0 0	1 1 1 1	3.571	-125.9	1.927	1815	2187
	0 0 0 0	3.549	-126	1.931	1807	2179

TABLE C.9: SF corner simulation results at 80^0C

sf 80c						
C4C3C2C1	f4f3f2f1	Freq (GHz)	Phase noise @2MHz	Vpeak-peak (V)	Power DCO (uW)	Power DCO + LDO (uW)
1 1 1 1	1 1 1 1	5.423	-118.9	2.133	1267	1644
	0 0 0 0	5.349	-119.1	2.134	1264	1642
1 1 1 0	1 1 1 1	5.303	-119.3	2.13	1275	1652
	0 0 0 0	5.234	-119.6	2.13	1272	1649
1 1 0 1	1 1 1 1	4.994	-120.2	2.054	1437	1812
	0 0 0 0	4.936	-120.4	2.057	1431	1806
0 0 1 0	1 1 1 1	3.726	-123.7	1.733	1963	2319
	0 0 0 0	3.701	-123.9	1.74	1956	2314
0 0 0 1	1 1 1 1	3.61	-124.1	1.712	1986	2339
	0 0 0 0	3.588	-124.3	1.719	1980	2334
0 0 0 0	1 1 1 1	3.574	-124.3	1.717	1981	2334
	0 0 0 0	3.552	-124.5	1.724	1975	2329

TABLE C.10: SF corner simulation results at 0^0C

sf 0c						
C4C3C2C1	f5f4f3f2f1	Freq (GHz)	Phase noise @2MHz	Vpeak-peak (V)	Power DCO (uW)	Power DCO + LDO (uW)
1 1 1 1	1 1 1 1 1	5.422	-117.8	2.177	1189	1556
	0 0 0 0 0	5.348	-118.1	2.178	1184	1552
1 1 1 0	1 1 1 1 1	5.302	-118.3	2.176	1193	1561
	0 0 0 0 0	5.232	-118.5	2.177	1189	1556
1 1 0 1	1 1 1 1 1	4.992	-119.7	2.124	1334	1701
	0 0 0 0 0	4.934	-120	2.127	1327	1694
0 0 1 0	1 1 1 1 1	3.724	-125.1	1.907	1840	2203
	0 0 0 0 0	3.669	-125.3	1.912	1831	2194
0 0 0 1	1 1 1 1 1	3.609	-125.7	1.892	1866	2229
	0 0 0 0 0	3.587	-125.8	1.897	1858	2221
0 0 0 0	1 1 1 1 1	3.573	-125.9	1.896	1860	2223
	0 0 0 0 0	3.551	-126	1.901	1851	2214

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