High Speed DAC for Delta Sigma Modulator in SCL 180nm Technology

A Project Report

submitted by

AMAL S S

in partial fulfilment of requirements
for the award of the dual degree of

BACHELOR OF TECHNOLOGY AND MASTER OF TECHNOLOGY

DEPARTMENT OF ELECTRICAL ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY MADRAS

JUNE 2017

THESIS CERTIFICATE

This is to certify that the thesis titled **High Speed DAC for Delta Sigma Modulator in SCL 180nm Technology**, submitted by **AMAL S S**, to the Indian Institute of Technology, Madras, for the award of the degree of **Bachelor of Technology and Master of Technology**, is a bonafide record of the research work done by him under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma

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ACKNOWLEDGEMENTS

I take this oppertunity to express my deepest gratitude to my project guide Dr. Nagendra Krishnapura for His valuable guidance throughout this project.I am very grateful to him for giving me an oppertunity to work under him and providing his value time to guide me throught the project.

I would also like to thank everyone in the analog group for being really supportive of me during the course of the project. I am really indebted to Praveen M V and Sumit Kumar for their constant support and guidance with doubts and difficulties. I express my gratitude towards Ashwin Kumar and Aditya Narayanan who advised me throughout the duration.

I would like to thank my lab-mates for their support during course.

Finally I am extremly thankful for my parents for be living in me, my teachers for the academic insight provided and all the friends in IIT Madras for their support.

ABSTRACT

KEYWORDS: Delta Sigma Modulator, Digital to Analog Converter, Calibration, SCL 180nm Technology

Data converters are one key components in any electronics system. One of the most interesting class of data converters among them are the Delta Sigma Modulators (DSM), which are noise shaped over sampled Analog to Digital (ADC) converters. DSMs can implemented either in continuous-time or discrete-time. One of the key components for a Continuous-Time DSM (CTDSM) is the Digital to Analog (DAC) converter used in the feed back loop.

This thesis focus on the implementation of a 4-bit high speed calibrated DAC on the SCL 180nm technology, which can be used as a part of a high speed DSM. The transistor level simulation results gives an output SNR of 93 dB for the DAC over the test bench, which yields SNR of 96 dB over an ideal DAC.

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ABBREVIATIONS

ADC	Analog to Digital Converter
CTDSM	Continuous-Time Delta Sigma Modulator
DAC	Digital to Analog Converter
DSM	Delta Sigma Modulator
LNA	Low Noise Amplifier
PSD	Power Spectral Density
SNR	Signal to Noise Ratio

CHAPTER 1

INTRODUCTION

1.1 Motivation and Prior Work

From the last decade there is an immense growth in wireless technology and numerous standards have arisen categorized by data rate and range of communication. Most of the architectures intended to support these comprises of elements like LNA, IQ mixer, High resolution ADC and appropriate filters. The to meet the requirements on ADCs in these components, most common architecture used is the Delta-Sigma Modulator(DSM) with a multi-bit quantifier. Delta-Sigma ADCs are widely used in the wireless domain due to their oversampling, dynamic range and low power consumption and a continuous-time delta sigma modulator (CTDSM) is better in terms of power consumption and input allowable bandwidth. Basic parts which make up a CTDSM are loop filter, quantizer and a Digital-to-Analog converter(DAC).

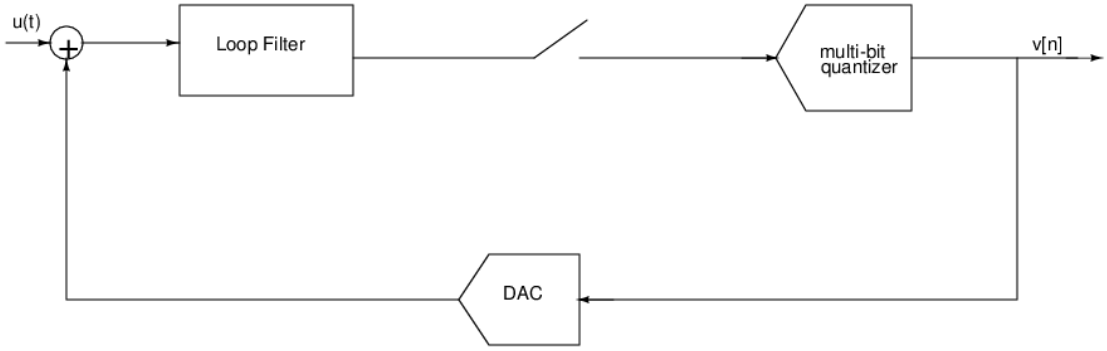

Figure 1.1: Block diagram of a CTDSM

In this thesis we consider the architecture of a multi-bit high speed DAC, which is part of a high speed DSM, in SCL 180nm process technology.

1.2 Thesis Outline

Chapter 2 focus on the architecture of the DAC implemented and the issue of mismatch in the DAC.

Chapter 3 has detailed circuit diagrams of the DAC implementation.

Chapter 4 contains the simulations results of the DSC in SCL technology.

CHAPTER 2

ARCHITECTURE

2.1 4-Bit Calibrated DAC

Basic function of the DAC is to convert the Digital signals to analog counterparts. Depending on the method to implement the many non-linearities are expected to occur in the implementation. The predominant case of these non-linearities are mostly the mismatch between DAC elements. Two prominant methods used to deal with this issue are Dynamic Element Matching(DEM) and DAC Calibration.

2.1.1 Current Steering DAC

Current Steering DAC, one of the popular architecture is used here for the DAC implementation. To reduce the input noise power, current steering DAC with complementry architecture is used (Fig 2.1). The noise current at the output due to the DAC cell is[1]

$$I_{noise} = I_1 + I_2 \tag{2.1}$$

and the input referred noise power spectral density (PSD) is given by

$$S_{noise} = R_{in}^2(S_1 + S_2) \tag{2.2}$$

since I_1 and I_2 are equal

$$S_{noise} = 2.R_{in}^2.S_1 \tag{2.3}$$

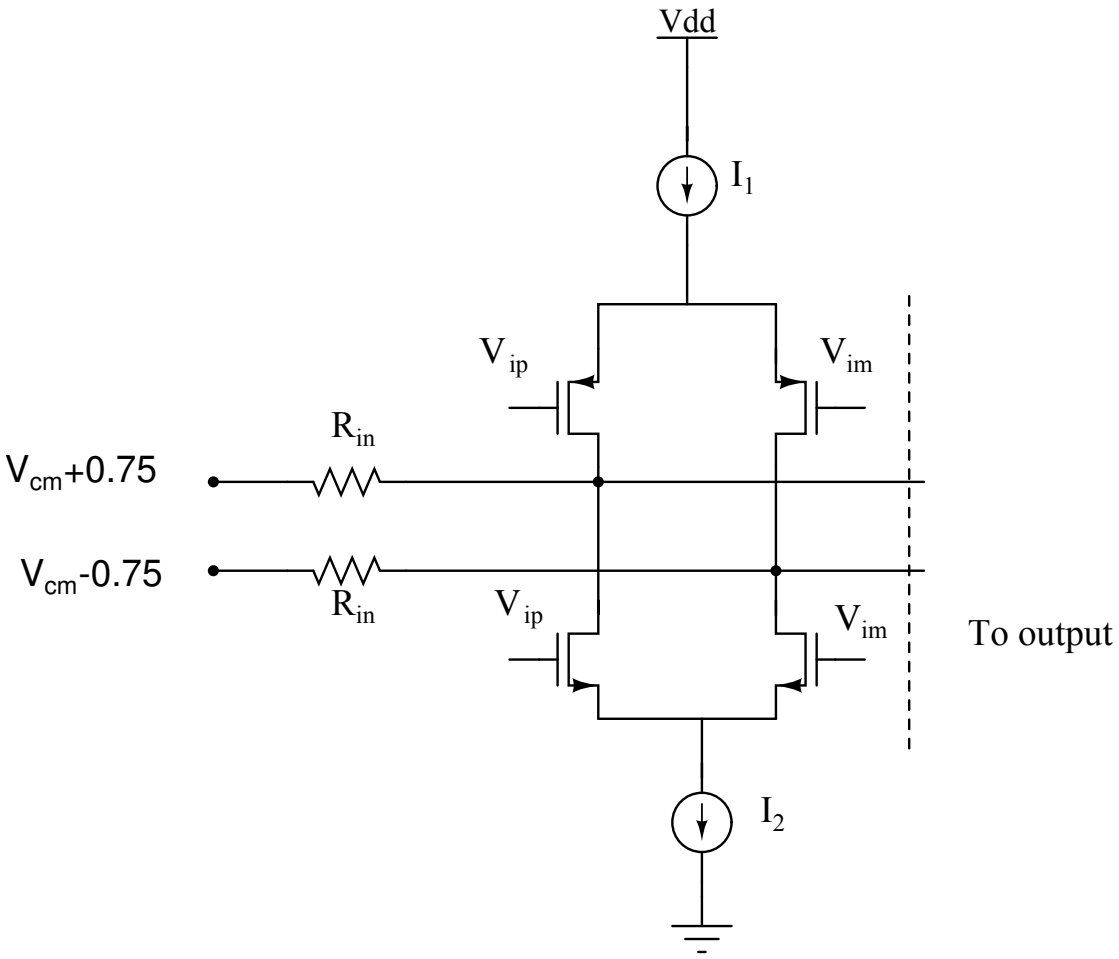

Figure 2.1: complementary current steering DAC

2.2 DAC Calibration

One of the methods to tackle DAC mismatch is the calibration. Here a reference current source is used to trim each current source. The principle of calibration is such that, during the calibration phase a reference current is passed to the transistors and made the bias voltages settle to the appropriate values(which is stored using appropriate capacitance). During the operational phase, keeping the bias voltages the same(using the voltages stored in the capacitance in the earlier phase) transistors are connected to output node. The output current will be same as that of reference current since the bias voltages are not changed. For a multi-bit DAC, the calibration must be extended to array of current sources (Fig 2.2). The N+1 current sources generate N equal currents. An extra current source is used to take place of the one being calibrated to ensure the continuity of the output. The shift register is used to select the cell being calibrated.

One major concern when implementing the calibration for the DAC is the Excess

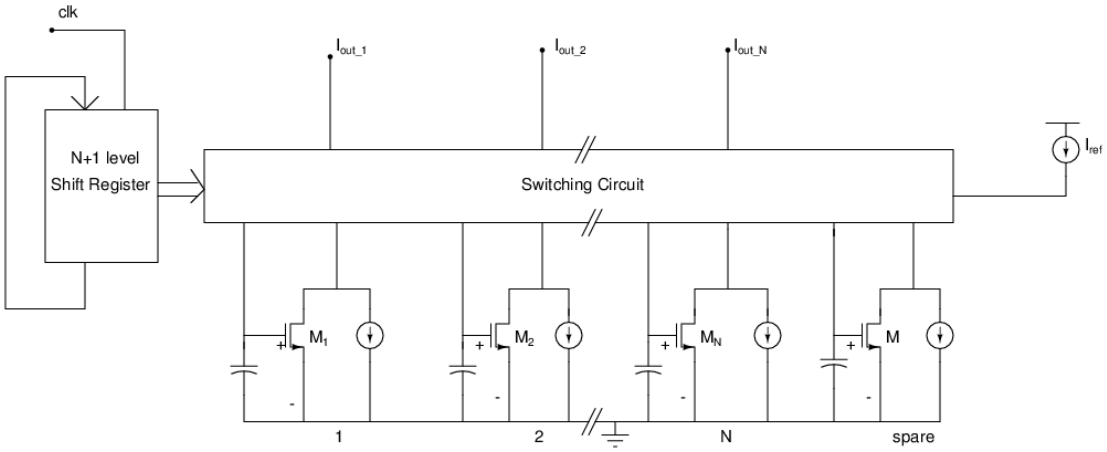

Figure 2.2: Calibration of N element current steering DAC

Loop Delay(ELD), since at high speeds delay through the switches for the calibration is significant compared to the clock period and contribute towards increasing ELD. Hence a scheme of connecting two DAC cells to output of each the flash comparator is adopted. So at anytime one cell is being calibrated and another contributes to the output.

CHAPTER 3

CIRCUIT IMPLEMENTATION

3.1 Unit DAC Cell

Schematic of the DAC unit cell with circuitry to hold the the input for one cycle is given in (Fig 3.1). Here M_{p1} and M_{p2} act as the current sources while M_{n1} and M_{n2} act as the current sinks.

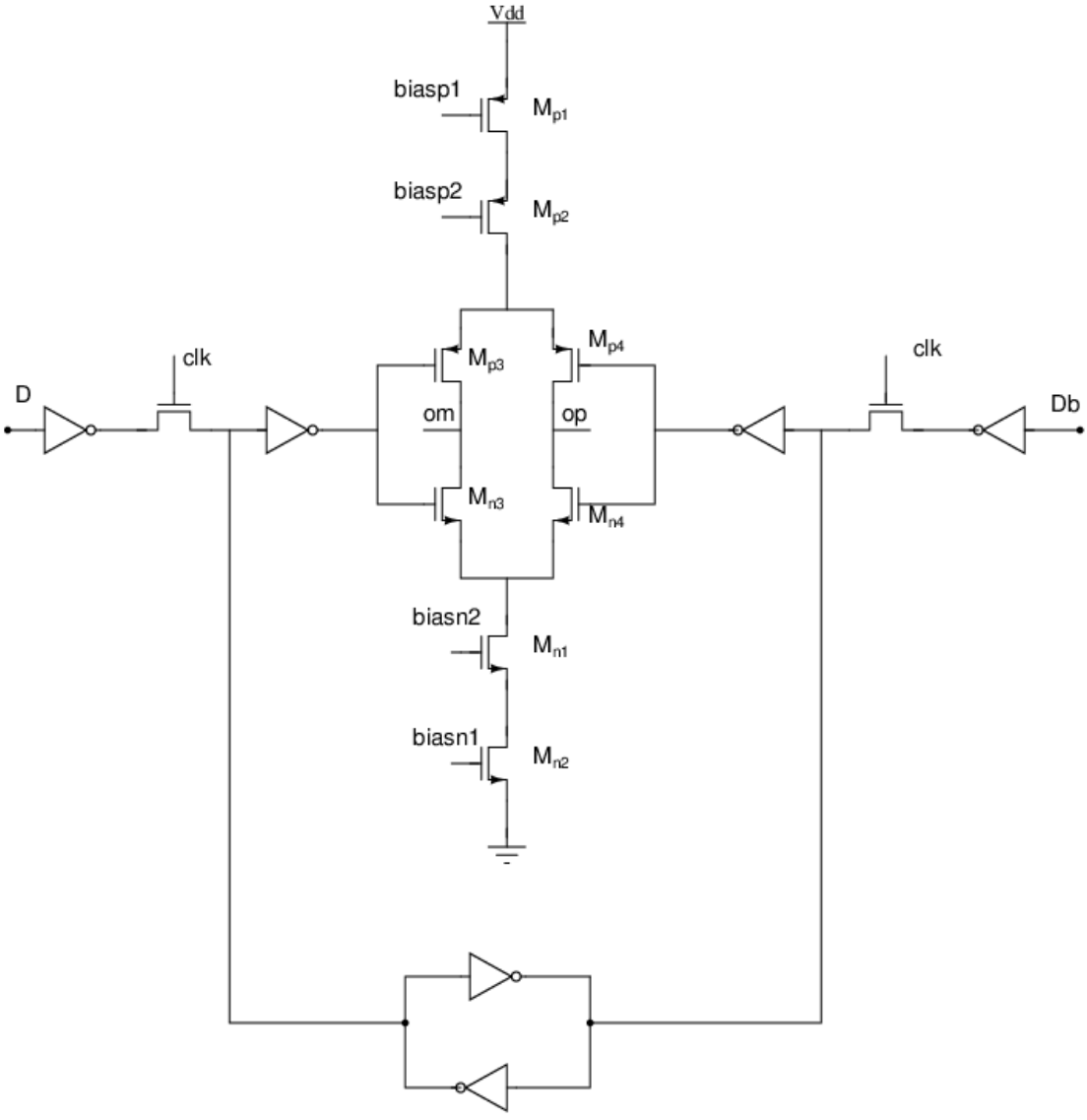

Figure 3.1: [1]

3.2 DAC Cell With Calibration Loop[1]

The 4-bit DAC used in the needs to 30 unit DAC cells for implementation. The unit cells with the calibration is given in Fig 3.2. The current sources I_{refn} and I_{refp} are derived from a single master source, and are used to calibrate the transistors M_{1b} and M_{10b}.

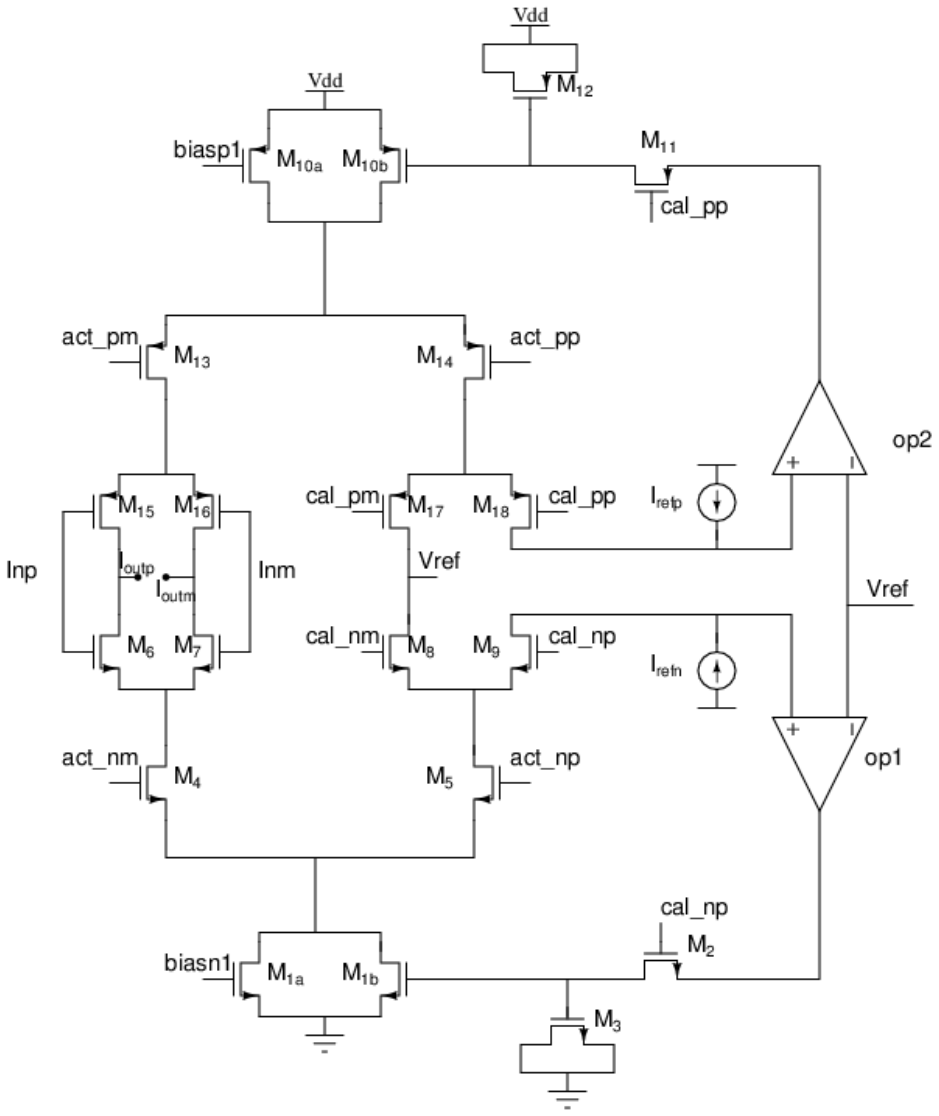

Figure 3.2: Unit cell of the calibrated DAC[1]

$M1a, M1b$	$2(1.2\mu m/4\mu)$
$M2$	$(0.48\mu m/0.18\mu)$
$M3$	$2(4.3\mu m/3\mu)$
$M4, M5$	$(2\mu m/0.18\mu)$
$M6, M7, M8, M9$	$(0.5\mu m/0.18\mu)$
$M11$	$(1.2\mu m/0.18\mu)$
$M10a$	$5(2.5\mu m/2.5\mu)$
$M10b$	$3(2.5\mu m/2.5\mu)$
$M12$	$2(4.5\mu m/4\mu)$
$M13, M14$	$(6\mu m/0.18\mu)$
$M15, M16, M17, M18$	$2(0.5\mu m/0.18\mu)$

Table 3.1: Transistor sizes of unit cell of the calibrated DAC[1]

3.3 Biasing[1]

Circuit for generating biasn1 and biasp1, used for the biasing of calibrated DAC unit cell is Fig 3.2 is given in Fig 3.3. V_{ref_dac} is an off chip control signal which can control DAC current. The resistive network used for generating biasn2 and biasp2 also generates the voltage required by the signals act_np, act_nm, act_pp and act_pm

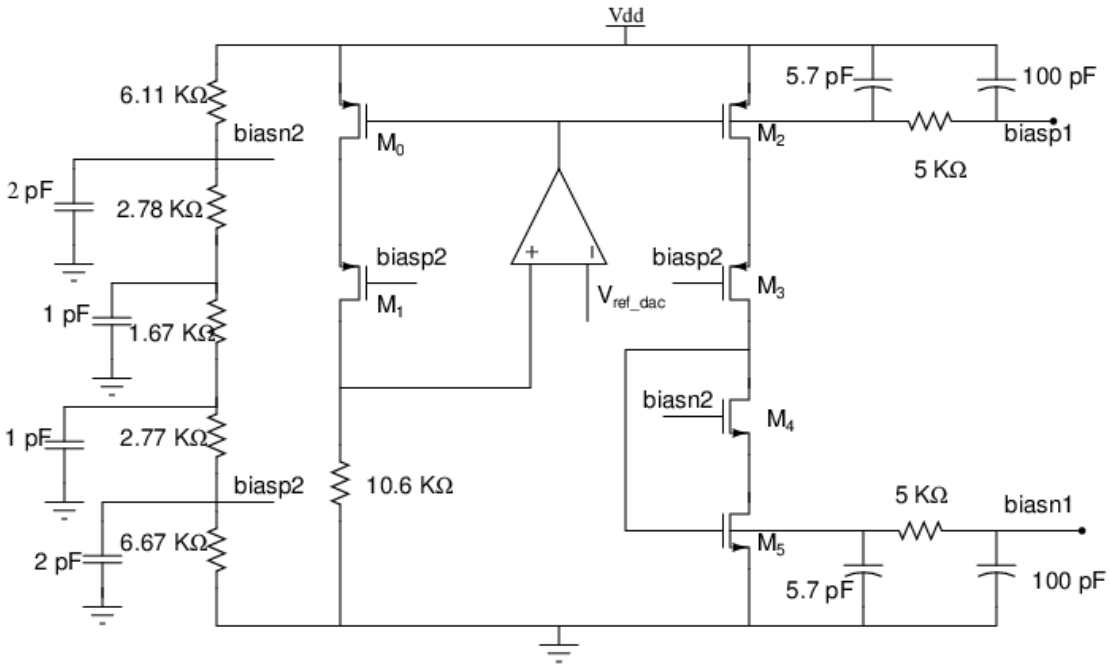

Figure 3.3: Circuit for generating biasn1 and biasp1[1]

Fig 3.4 shows the circuit for generating the currents I_{ref_n} and I_{ref_p} to bias the calibrated DAC unit cell.

$M0, M2$	$80(2.5\mu m/2.5\mu)$
$M1, M3$	$4(6\mu m/0.18\mu)$
$M4$	$4(2\mu m/1.2\mu)$
$M5$	$8(2\mu m/0.18\mu)$

Table 3.2: Transistor sizes of Circuit in Fig 3.3[1]

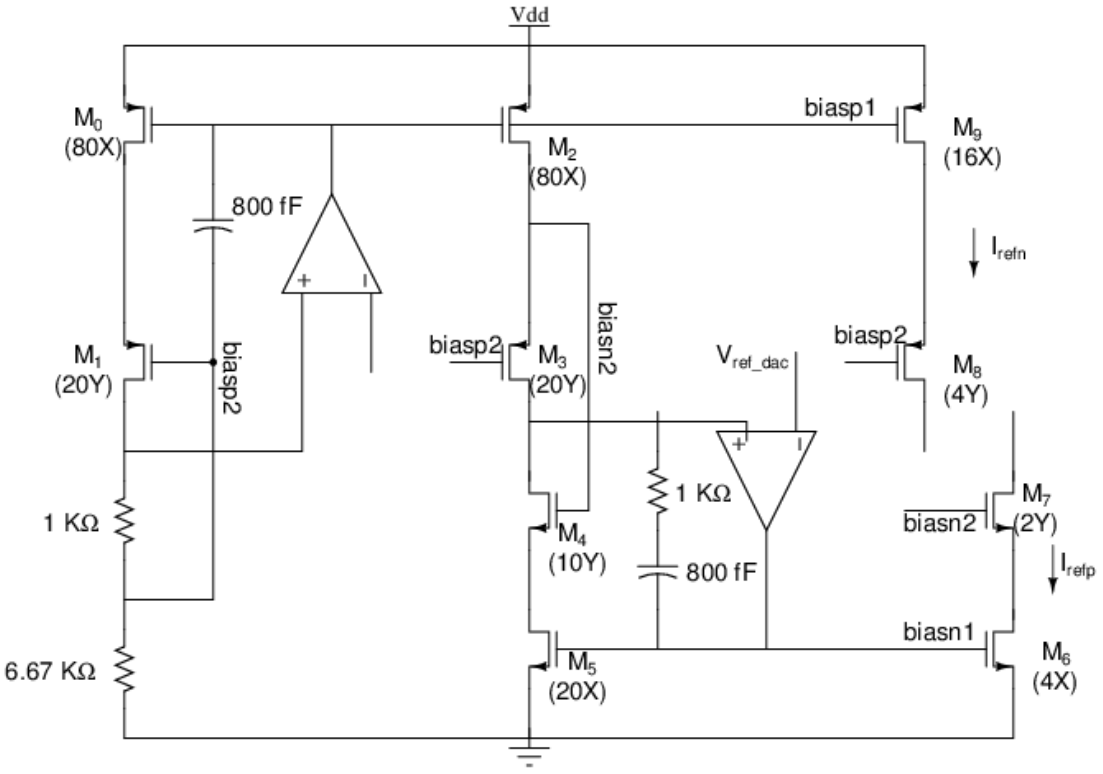

Figure 3.4: Circuit for generating I_{refn} and I_{refp}[1]

X	$2\mu m/1\mu$
Y	$2\mu m/0.18\mu$

Table 3.3: Transistor sizes of Circuit in Fig 3.4[1]

CHAPTER 4

CIRCUIT SIMULATION AND RESULTS

4.1 Schematic Simulations

Fig 4.1 shows the schematic setup for the circuit simulations. The DAC block contains all the unit cells and the bias voltage generaters. Thermometer is used to convert the test signal to flash levels. Operating voltage is fixed at 1.8 V and vcmref at 0.9 V. V1 and V2 are current controlled voltages sources with values 2 kΩ and -2 kΩ with reference currents being currents from outp and outm respectively.calp,calp1,activep and activen are signals used in calibration of the DAC.

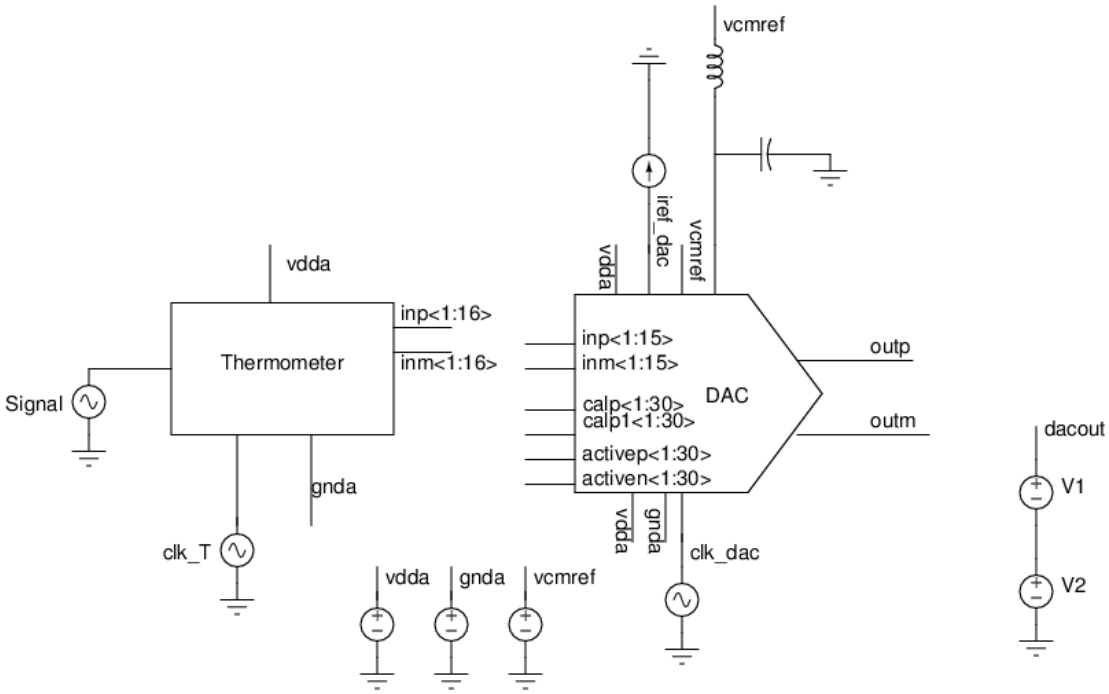

Figure 4.1: Schematic for the DAC simulations

The DAC schematic was built in SCL 180nm technology and simulated. The clock speed of the circuit is fixed at 800 MHz. The input used in the simulation is the output of an ideal delta sigma modulator. Fig 4.2 shows the PSD of the DAC output. The in-band SNR for the DAC was found to 93 dB. There is an improvement compared to the DAC built in the UMC 180nm process which had an in-band SNR of 89 dB[1].

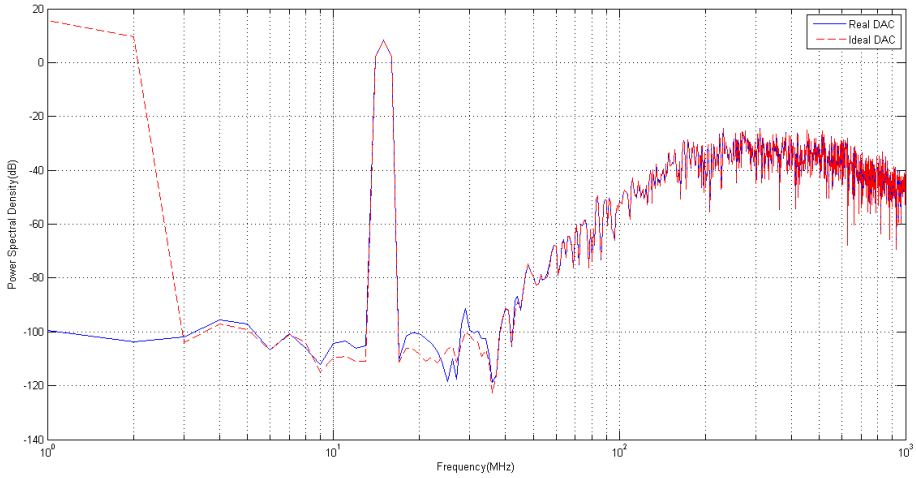

Figure 4.2: Output PSD of an ideal DAC and the schematic implemented in SCL technology

Fig 4.3 shows the input output characteristics of the DAC. The output shown is after passing the output current of the DAC through a current controlled voltage source of value 2 kΩ.

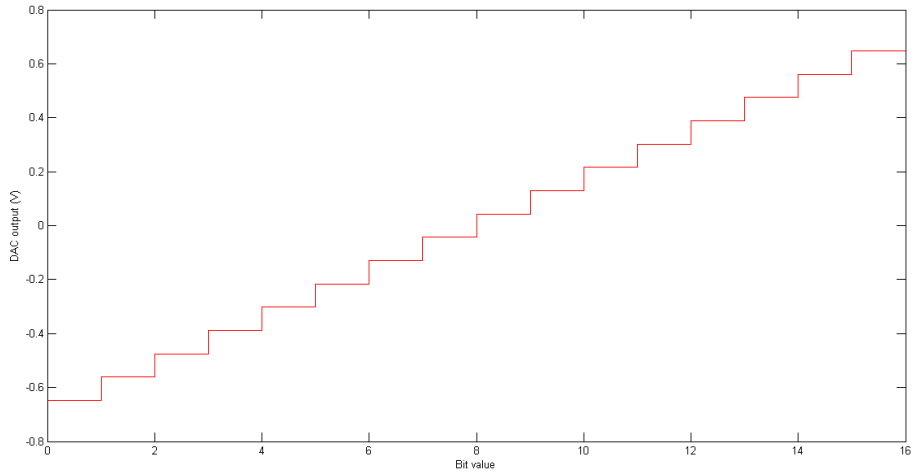

Figure 4.3: The input-output characteristics of the DAC in SCL 180nm technology

REFERENCES

[1] Vikas Singh, "Design of a High Speed High Resolution Continuous-Time Delta Sigma Modulator", *Master of Science Thesis, June 2011*