Design of P-N Junction Phase Shifter for Traveling Wave Modulator

A Project Report

submitted by

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THESIS CERTIFICATE

This is to certify that the thesis titled **Design of P-N Junction Phase Shifter for Traveling Wave Modulator**, submitted by **Dudekula Dadavali** , to the Indian Institute of Technology, Madras, for the award of the degree of **Master of Technology**, is a bonafide record of the research work done by him under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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Dedicated to My Parents

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ABSTRACT

Silicon photonics in Silicon-on-Insulator (SOI) platform is the leading candidate in optical communication due to the CMOS compatibility and of lower cost. However the capability of high speed communication can be utilized only with the enhancement of modulation speed. Generally, in SOI platform electro-optic modulation is achieved by plasma dispersion effect. There are two types of modulation techniques used in general, injection based (forward biased PIN diode) and depletion based (reverse biased PN diode). Modulation using PIN diode is comparatively slower ($\sim$100 MHz) than that of depletion based p-n diode ($\sim$50 GHZ) due the higher diffusion capacitance. Further the speed of lumped depletion based PN diode is limited by RC time constant due to the higher modulator length. This issue can be rectified by replacing lumped electrode by travelling wave electrode where the coplanar waveguide (CPW) serves as electrode. In this work, we optimized rib waveguide dimensions for 2 μm SOI, and 1 μm to satisfy the single-mode guidance using lumerical mode solver. For 2 μm (1 μm) SOI rib waveguide the effective index of TE and TM modes are found to be 3.434923 (3.317561) and 3.433221 (3.282051) respectively and birefringence ($n_{eff_{TE}}$ - $n_{eff_{TM}}$) 1.702×10^{-3} (3.551×10^{-2}). The electrical simulation of reverse biased p-n junction phase shifter of 2 μm and 1 μm SOI rib waveguide has been carried out using the commercial device software MEDICI. The refracive index profiles for applied bias are imported into Lumerical Mode solver to find the change in effective index of guided mode profiles to calculate the L_π. The achieved figure of merit ($V_\pi L_\pi$) for 2 μm and 1 μm SOI rib waveguide are 8.193 V.cm and is 6.06 V.cm respectively. Fabrication process flow for p-n phase shifter on 1 μm SOI platform has been optimized using the process simulator Tsuprem4.

The optimization of doping concentration profiles to improve the Figure of merit ($V_\pi L_\pi$) and modulation efficiency and Traveling Wave Electrode design could be carried out in the future.

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CHAPTER 1

INTRODUCTION

Silicon Photonics has been largely investigated in recent years and has been found that optical interconnects on an Silicon-on-Insulator (SOI) are an attractive alternative to traditional electronic interconnects because they provide higher bandwidth, compatible with lower cost and mature CMOS processing. Silicon is transparent in the range of optical telecommunications wavelengths (absorption loss at $\lambda = 1.55\ \mu m$, is as low as 0.004 dB/cm) and optical waveguides fabricated in SOI and have very high index contrast ($\Delta n = 2$, for Si and SiO_2 interface and $\Delta n > 2$ for Si and air interface), which will provides tight confinement of propagation mode. The schematic view of a commercially available SOI wafer has been shown in Fig 1.1

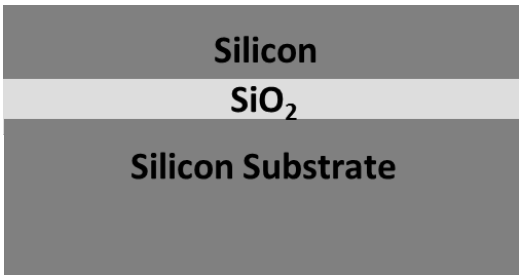


Figure 1.1: Schematic view of SOI wafer

The capability of high bandwidth can be utilized only with the enhancement of modulation speed i.e., how fast one can convert electrical data into an optical information. Various optical modulators in silicon have been reported with differing tradeoffs. Achieving efficient modulation in the silicon has always been one of the key challenges of silicon photonics.

Generally phase modulation in a silicon is achieved by varying the refractive index of medium. The main methods to alter the refractive index in Si are the thermo-optic effect and free carrier dispersion effect.

The Thermo-optic effect: The change in refractive index of material due to change in temperature. However, this is not viable for designing circuits as other elements on-chip might be affected by temperature changes. The thermo-optic effect is rather slow and can be used only up to approximately 1 MHz modulation frequencies.

Free carrier dispersion effect: This is the most effective way of performing optical modulation in silicon [1]. This effect relates the variation in the concentration of electrons (ΔN_e) and holes (ΔN_h) in a semiconductor to changes in the absorption coefficient ($\Delta\alpha$) and refractive index (ΔN). This effect has been mathematically described by Drude and Lorenz relating the change in electron and hole concentration to the absorption is,

$$\Delta\alpha = \frac{e^3\lambda_0^2}{4\pi^2c^3\epsilon_0 n}\left(\frac{N_e}{\mu_e(m_{ce}^*)^2} + \frac{N_h}{\mu_h(m_{ch}^*)^2}\right) \tag{1.1}$$

and the corresponding equation for change in real part of refractive index(Δn) is,

$$\Delta n = \frac{e^2\lambda_0^2}{8\pi^2c^2\epsilon_0 n}\left(\frac{N_e}{m_{ce}^*} + \frac{N_h}{m_{ch}^*}\right) \tag{1.2}$$

N_e, N_h are the electron and hole concentrations, μ_e, μ_h are the electron and hole mobilities, m_{ce}^*, m_{ch}^* are the electron and hole effective masses respectively. e is the electron charge. λ_0 is the free space wavelength $1.55\mu m$. ϵ_0 is the free space permittivity and n is the refractive index. ΔN_e, ΔN_h, are the Change in electron and hole concentrations, μ_e, μ_h are electron and hole mobilities are m_e, m_h the hole and electron effective masses respectively.

Soreff and Benett model for free carrier dispersion in silicon at the wavelength of $\lambda = 1.55\ \mu m$ are expressed as,

$$\Delta n = \Delta n_e + \Delta n_h = -[8.8 \times 10^{-22}\Delta N_e + 8.5 \times 10^{-18}(\Delta N_h)^{0.8} \tag{1.3}$$

$$\Delta\alpha = \Delta\alpha_e + \Delta\alpha_h = [8.5 \times 10^{-18}\Delta N_e + 6.0 \times 10^{-18}\Delta N_h] \tag{1.4}$$

Here Δn and $\Delta\alpha$, which was found to be close agreement with the Drude-Lorentz equation. For a communication wavelength of $\lambda = 1.55\ \mu m$ the relation as follows. where $\Delta N_e, \Delta N_h$ are the change in electron and hole concentrations respectively.

1.1 Motivation:

Three different techniques have been studied in the literature to achieve phase modulation in silicon, namely, 1) Carrier Accumulation (MOS capacitor)[2], 2) Carrier Injection (Forward biased p-i-n diode)[3], 3) Carrier Depletion (Reverse biased p-n

diode)[4], [5].

Carrier Accumulation: This technique can be achieved by MOS capacitor device configuration as shown in Fig. 1.2 [2]. Operating MOS capacitor in accumulation conditions will cause the change in the free carrier density on top and bottom of gate oxide which induces the phase shift in the guided mode. The advantage of this device configuration is possible to achieve high modulation speed (1 GHz) because the operates by accumulating the majority carriers. The disadvantage is poor modulation efficiency high figure of merit ($V_\pi L_\pi$) because of small overlap between guided mode and carriers density.

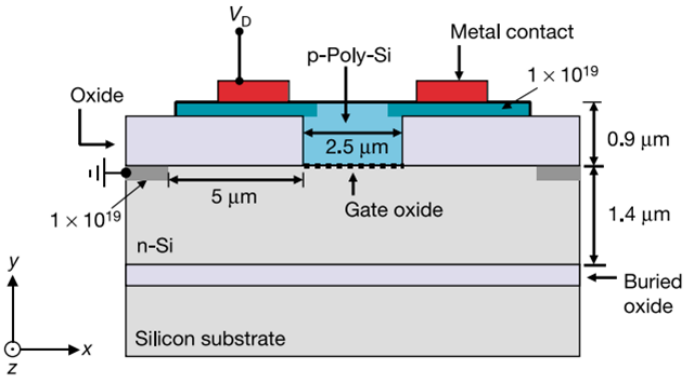


Figure 1.2: The cross sectional view of carrier accumulation based phase shifter using the MOS capacitor [2].

Carrier Injection: This technique can be achieved by forward biased p-i-n diode device configuration as shown in Fig. 1.3 [6], [3]. Under forward biased conditions the injection or removal of free carrier density in the intrinsic region will cause the change in effective index of the guided mode.

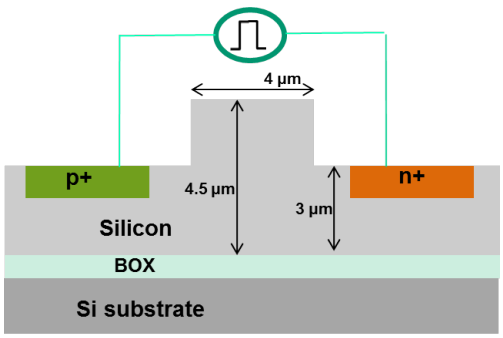


Figure 1.3: The cross sectional view of carrier injection based phase shifter using the forward biased p-i-n diode [6].

The advantage of this device configuration is high modulation efficiency and low figure of merit ($V_\pi L_\pi$). The disadvantage is operating speed of the device is low be-

cause of slow carrier generation and/or recombination processes and high diffusion capacitance. in the forward bias operation.

Carrier Depletion: This technique can be achieved by reverse biased p-n diode device configuration as shown in Fig. 1.4 [4]. Under reverse biased conditions the changing the depletion width of the p-n diode will cause the change in free carrier density, which will cause the change in phase of the guided mode. The advantage of this device configuration is possible to achieve high modulation speed (∼50 GHz); in reverse bias, the operation is with the majority carrier dynamics; since the electric field is high the velocity of majority carriers is $10^7 cm/sec$ so the intrinsic response time will very less ($\sim psec$) [7]. Due to less refractive change the length required for π phase shift will be ∼mm. The RC time constant will depend on the type of electrical driving scheme, namely 1) Lumped electrode [5], 2) Traveling wave Electrode [4], [8], [9]. It can be reduced by using Traveling wave Electrode. The disadvantage is high figure of merit, complex structure and high birefringence ($n_{eff_{TE}}$ - $n_{eff_{TM}}$).

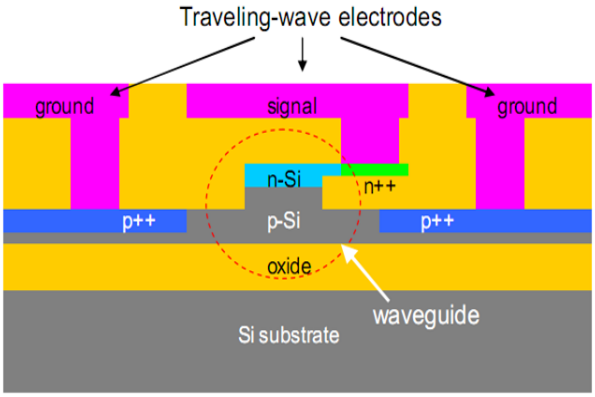


Figure 1.4: The cross sectional view of carrier depletion based phase shifter using the reverse biased p-n diode placed in active region of sub-micron waveguide [4].

Among these mechanisms, the method using carrier depletion in a reverse-biased p-n junction has shown superior performances with high operation speed (∼50 Gbps), high extinction ratio and low power consumption.

1.2 Objective

The main objective of this project is 1)Single mode waveguide design with < 2um SOI using Lumerical Mode solver. 2) P-N junction phase shifter design for traveling wave

modulator using MEDICI and Lumerical Mode solver. 3) Optimization of process parameters for the phase shifter using Tsuprem-4.

1.3 Organization of thesis

The work done in the thesis was primarily aimed at developing an understanding of high speed travelling wave Silicon optical modulator and designing a phase shifter section for 2 μm and 1 μm SOI rib waveguide. After this Introduction, Chapter 2 presents the simulation results showing the optimization of for 2 μm and 1 μm SOI to satisfy the single-mode guidance using lumerical mode solver. Chapter 3 describes electrical and optical simulation results of p-n phase shifter design for 2 μm and 1 μm SOI rib waveguide. Chapter 4 discusses the fabrication process flow simulation results and parameters for p-n phase shifter design on 1 μm SOI platform. Chapter 5 summarizes the work done and outlines the scope for future work.

CHAPTER 2

Single Mode SOI Rib Waveguide Design

In this chapter various parameters of a SOI Rib waveguide (see Fig. 2.1) are optimized to satisfy single mode guidance. For a fixed slab height and rib width, the rib height have been varied to find the single mode regime. These optimized single mode waveguide dimensions are used to design the Travelling Wave Modulator.

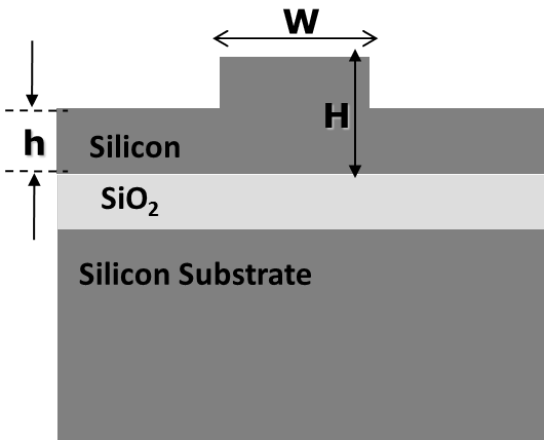


Figure 2.1: Schematic view of SOI Rib waveguide

2.1 Single mode condition for 2 μm SOI:

For fixed slab height (h) = 1.0 μm, rib width (W) has been varied from 1.6 μm to 2 μm and rib height(H) has been varied from 1.7 μm to 2.2 μm to obtain the single mode condition. The simulation has been carried out using the Lumerical mode solver which uses the Finite Difference method to solve effective index of rib waveguide geometry. Simulation results shows that for W = 1.6 μm, H = 2 μm and h = 1 μm, both the effective indices of both TE and TM first order modes of the rib geometry are less than fundamental mode effective index of the slab which ensures the single mode operation of the rib geometry.

The Fig.2.5(a) and Fig.2.5(b) shows single mode TE and TM polarizations of silicon rib waveguide having a width(W) 1.6 μm, rib height(H) 2 μm and slab height is 1 μm,.

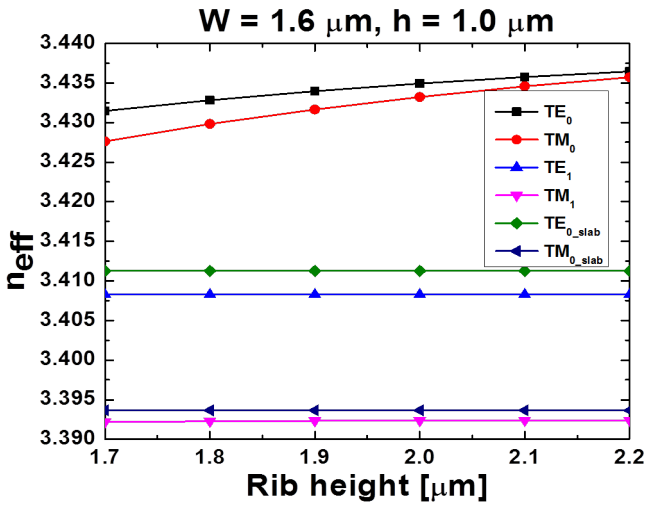
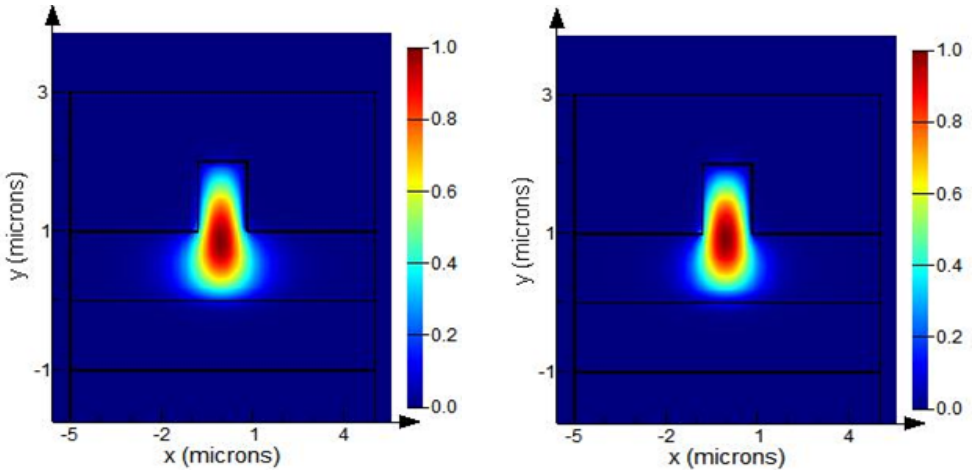


Figure 2.2: Effective indices as a function of waveguide dimensions under Single mode condition



(a) (b)

Figure 2.3: (a) TE Mode profile and (b) TM Mode profile of 2 μm SOI rib waveguide with top oxide cladddding

2.2 Single mode condition for 1 μm SOI:

A similar analysis has been carried out for sub-micron rib geometries. For a fixed rib width (W) = 0.8 μm and slab height (h) = 0.5 μm rib height (H) has been varied from 0.7 μm to 1.1 μm to find the effective indices of rib geometry. The simulation results shows that for the rib height (H) below 0.9 μm, the rib geometry will maintain the single mode operation.

The Fig.2.5(a) and Fig.2.5(b) shows single mode TE and TM polarizations of silicon rib waveguide having a width(W) 0.8 μm, rib height(H) 0.8 μm and slab height 0.3 μm,.

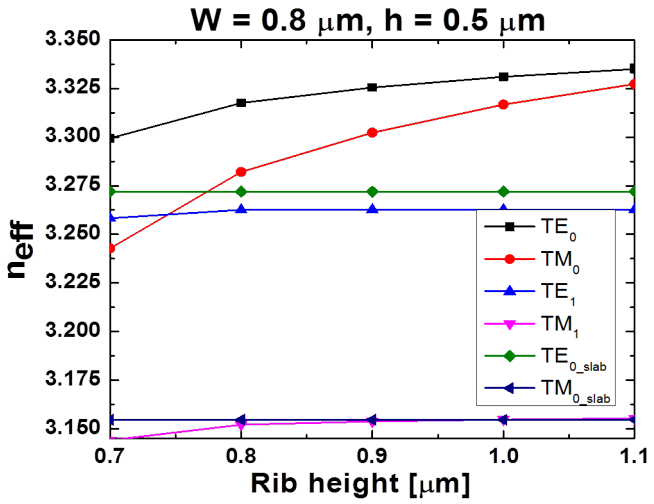
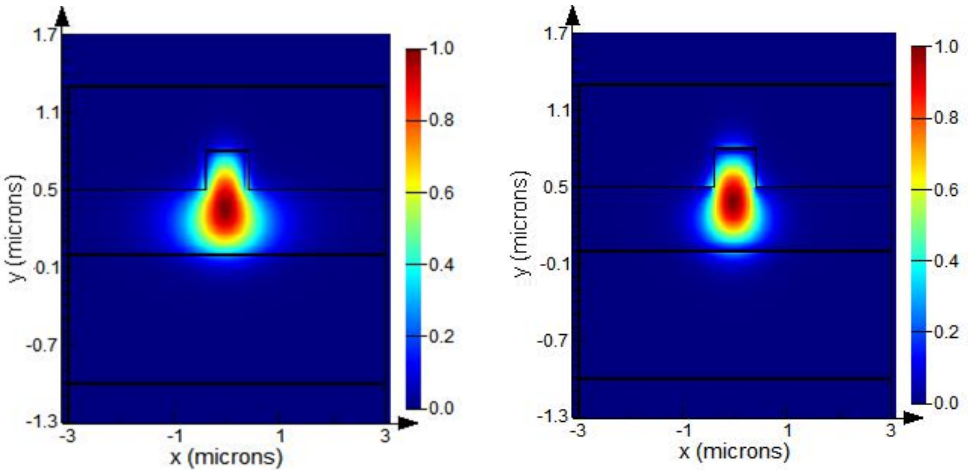


Figure 2.4: Effective indices as a function of waveguide dimensions under Single mode condition



(a) (b)

Figure 2.5: (a) TE Mode profile and (b) TM Mode profile of SOI sub-micron rib waveguide with top oxide claddding

2.3 Conclusion

In this chapter, SOI rib waveguide dimensions are optimized for two different device layer thickness (i.e., H = 2 μm, H = 0.8 μm) for single-mode guiding using lumerical mode solver. Single-mode condition is necessary to ensure that the device operation is not dispersive and can provide a better performance of the modulator.

CHAPTER 3

Design of P-N junction for Travelling Wave Optical Modulator

In this chapter simulations of a p-n junction phase shifter for the dimensions $W = 1.6\ \mu m$, $H = 1.6\ \mu m$ and $h = 1.6\ \mu m$ and for $W = 0.8\ \mu m$, $H = 2.0\ \mu m$ and $h = 0.5\ \mu m$ have been discussed. The device design is done by using Lumerical Mode solutions and MEDICI.

3.1 P-N Junction Design for 2 μm SOI Rib Waveguide

The Fig. 3.1, shows the cross sectional view a single mode SOI rib wavwguide of W = 1.6 μm, H = 2 μm, and h = 1 μm with top oxide cladding . we form a p-n^+ junction under the rib and To insure good Ohmic contact between silicon and metal contacts, two slab regions 1.5 mum away from both sides of the rib edge and the junction depth of 0.5 mum away from the rib edge are heavily doped with a dopant concentration of $1 \times 10^{20} cm^{-3}$. The distance between the inner edges of n^{++} and p^{++} doping window is kept at 3 μm so that the guided mode does not overlap with these regions. The electron and hole concentration profile and two dimensional profile of the depletion width (W_{dep}) of the structure are monitored for the structure at 0V bias and -10V bias respectively by medici simulations. The above mentioned simulations are repeated for different values of the offset to the middle of the rib waveguide of metallurgical p-n^+ junction.

From the soref and benett experimental fit one can observe that change in hole concentration will cause more change in background refractive index and less absorption loss than change in electron concentration. Since the p-doping plays a dominant role in changing the refractive index. From equation 3.1 we understand to achieve a wider p-type depletion region, the p-doping concentration has to be lower than the n-doping concentration. The p-n junction position was also optimized such that for a given reverse

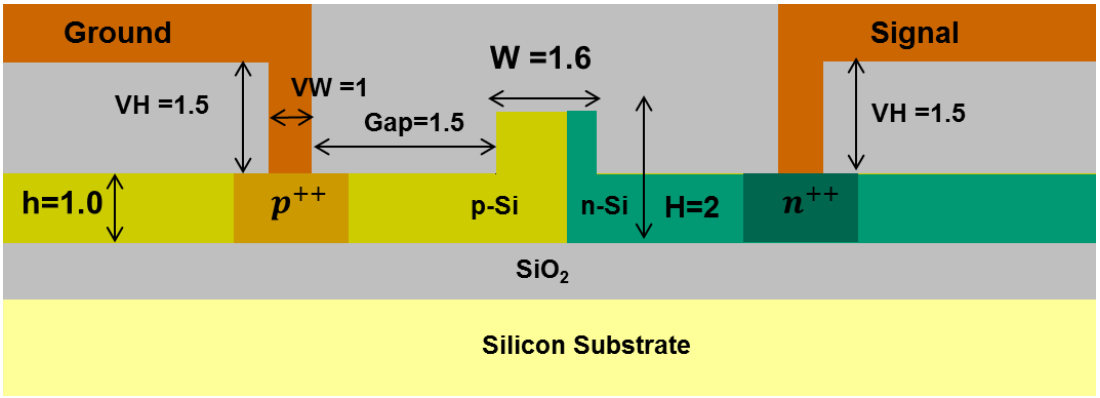


Figure 3.1: Cross sectional view of p-n phase-shifter section for 2 μm SOI platform. The dimensions mentioned are in μm.

bias the depletion width in the rib geometry will be symmetrical with the rib edges so as to increase the core part of optical mode overlapping region with the depletion region.

$$W_{dep} = \sqrt{\frac{2\epsilon_{si}\epsilon_0(V_r + V_{bi})}{q}\left(\frac{1}{N_a} + \frac{1}{N_d}\right)} \tag{3.1}$$

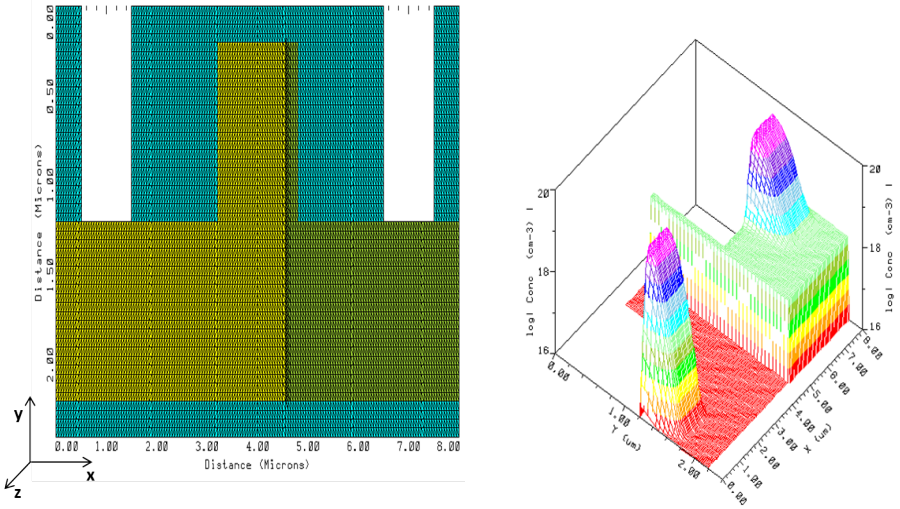
Where ϵ_{si} dielectric constant of silicon, ϵ_0 free space permittivity, V_r applied reverse bias voltage, V_0 built in voltage, N_d electron concentration, N_a hole concentration, q charge of electron.

In the following section we have varied the p-type impurity and p-n junction position for fixed $N_d = 1 \times 10^{18} cm^{-3}$ to get the change in effective index of p-n phase shifter for a applied reverse bias of 10V and we calculated length required to achieve π phase shift ($L\pi$) for 0V and applied reverse bias of 10V.

3.1.1 Calculation of Lπ of p-n phase shifter with uniform concentration profiles of $\mathbf{N_a = 1 \times 10^{16} cm^{-3}}$, $\mathbf{N_d = 1 \times 10^{18} cm^{-3}}$

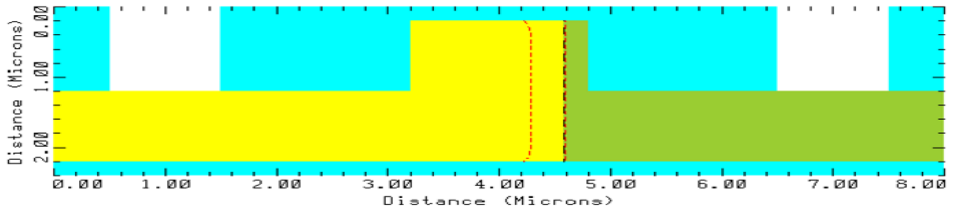
The mesh structure created in MEDICI device simulator for uniform doping profiles of $\mathbf{N_a = 1 \times 10^{16} cm^{-3}}$, $\mathbf{N_d = 1 \times 10^{18} cm^{-3}}$ and p-n^+ junction placed 0.6 μm offset to the middle of the rib waveguide structure so that for applied 10 Volts reverse bias the depletion width will be symmetrical about the rib walls has been shown in Fig. 3.2(a) and 3.2(b).

Calculation of L_π:

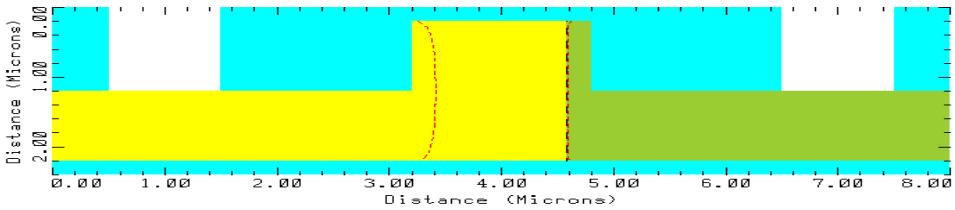


(a) (b)

Figure 3.2: (a)Meshing of the structure for MEDICI simulation of p-n^+ diode embedded in a rib waveguide. (b) Doping profiles of p-n^+ diode with uniform doping concentration of $N_a = 1 \times 10^{16} cm^{-3}$, $N_d = 1 \times 10^{18} cm^{-3}$ in p and n^+ regions respectively and for contacts is has Gaussian profiles with surface impurity concentration $N_s = 1 \times 10^{20} cm^{-3}$ and junction depth 0.5 μm from the contact in device simulator for p-n junction phase shifter for 2 μm rib waveguide



(a)



(b)

Figure 3.3: Depletion width of p-n junction phase shifter for 2μm rib waveguide with uniform doping concentrations $N_a = 1 \times 10^{16} cm^{-3}$, $N_d = 1 \times 10^{18} cm^{-3}$ under applied reverse bias of (a) 0V and (b) 10V

Table 3.1: Calculation of L_π for $2\mu m$ SOI rib waveguide with uniform doping concentrations $N_a = 1 \times 10^{16} cm^{-3}$, $N_d = 1 \times 10^{18} cm^{-3}$

	n_{eff} (for $V_r = 0V$)	n_{eff} (for $V_r = 10V$)	Δn_{eff}	L_π (mm)
TE	3.436553	3.436578	2.484×10^{-5}	31.118
TM	3.434822	3.434850	2.834×10^{-5}	27.734

The change in electron and hole concentrations for the applied reverse bias of 0V and 10V have been imported from MEDICI device simulator. The background refractive index change (Δn) and absorption coefficient ($\Delta \alpha$) is calculated using the the soref and bennet equations 1.3 and 1.4.

$$n_0(x, y) = n_B - n_0(x, y) \tag{3.2}$$

$$n_v(x, y) = n_B - n_v(x, y) \tag{3.3}$$

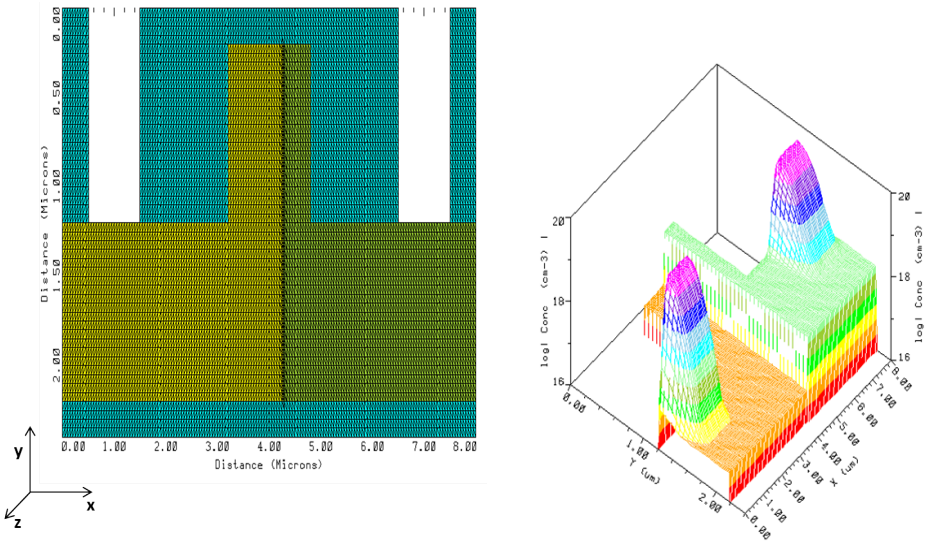
Where, n_B - Background Refractive Index, $n_0(x, y)$ and $n_v(x, y)$ are change in background refractive indices for 0 Volts and V_r Volts. These Calculated refractive index change and absorption coefficient is imported into Lumerical Mode solver to find the effective index of optical modes. The length required to achieve the π phase shift for reverse bias (v_r) of 10 V has been calculated using the following equations.

$$\Delta\Phi = (\frac{2\pi}{\lambda})(n_{eff_v} - n_{eff_0})L \tag{3.4}$$

$$\Delta\Phi = \frac{2\pi}{\lambda}\Delta n_{eff} L \tag{3.5}$$

$$L\pi = (\frac{\lambda}{2\Delta n_{eff}}) \tag{3.6}$$

where $\Delta\Phi$ Phase difference between in optical mode for 0V and applied reverse bias (V_r) = 10 Volts, n_{eff_v} effective index for V_r Volts, n_{eff_0} for V_0 Volts



(a) (b)

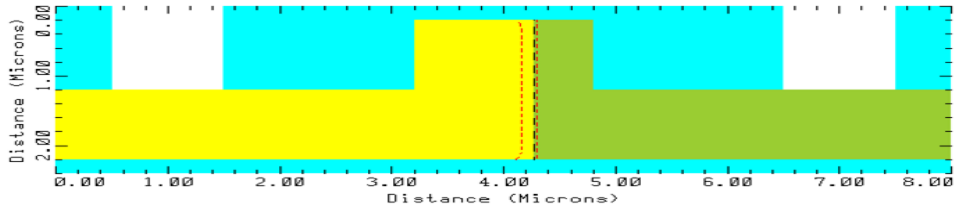
Figure 3.4: (a)Meshing of the structure for MEDICI simulation of p-n^+ diode embedded in a rib waveguide. (b) Doping profiles of p-n^+ diode with uniform doping concentration of $N_a = 5 \times 10^{16} cm^{-3}$, $N_d = 1 \times 10^{18} cm^{-3}$ in p and n^+ regions respectively and for contacts is has Gaussian profiles with surface impurity concentration $N_s = 1 \times 10^{20} cm^{-3}$ and junction depth 0.5 μm from the contact in device simulator for p-n junction phase shifter for 2 μm rib waveguide

Table 3.2: Calculation of L_π for $2\mu m$ SOI rib waveguide with uniform doping concentrations $N_a = 5 \times 10^{16} cm^{-3}$, $N_d = 1 \times 10^{18} cm^{-3}$

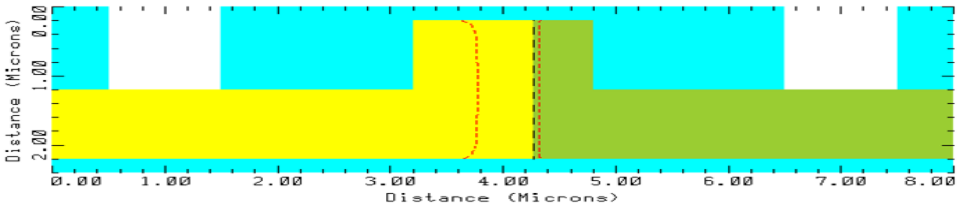
	n_{eff} (for $V_r = 0V$)	n_{eff} (for $V_r = 10V$)	Δn_{eff}	L_π (mm)
TE	3.436274	3.436348	7.438×10^{-5}	10.418
TM	3.434538	3.434616	7.838×10^{-5}	9.8873

3.1.2 Calculation of Lπ of p-n phase shifter with uniform concentration profiles of $\mathbf{N_a = 5 \times 10^{16} cm^{-3}}$, $\mathbf{N_d = 1 \times 10^{18} cm^{-3}}$

The mesh structure created in MEDICI device simulator for uniform doping profiles of $\mathbf{N_a = 5 \times 10^{16} cm^{-3}}$, $\mathbf{N_d = 1 \times 10^{18} cm^{-3}}$ and p-n^+ junction placed 0.3 μm offset to the middle of the rib waveguide structure so that for applied 10 Volts reverse bias the depletion width will be symmetrical about the rib walls has been shown in Fig. 3.4(a) and 3.4(b).



(a)



(b)

Figure 3.5: Depletion width of p-n junction phase shifter for $2\mu m$ rib waveguide with uniform doping concentrations $N_a = 5 \times 10^{16} cm^{-3}$, $N_d = 1 \times 10^{18} cm^{-3}$ under applied reverse bias of (a) 0V (b) 10V

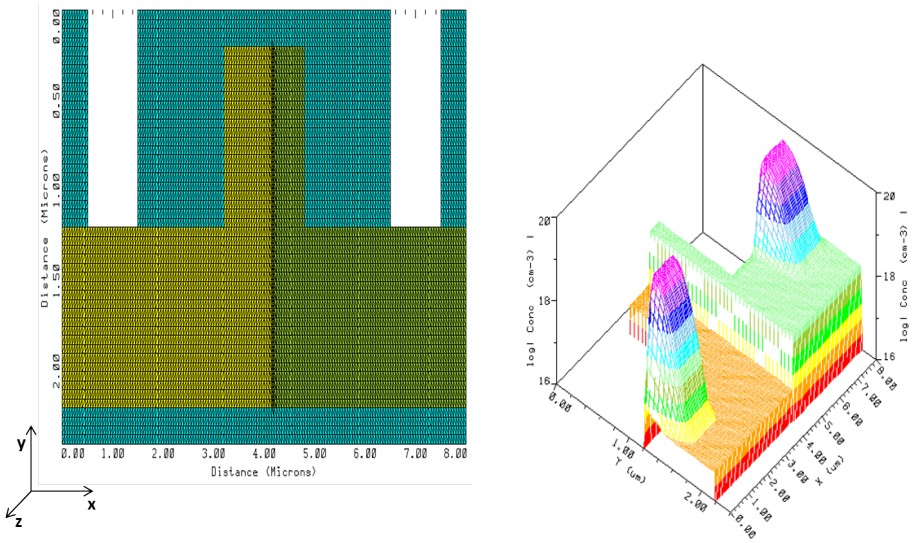
Table 3.3: Calculation of L_π for $2\mu m$ SOI rib waveguide with uniform doping concentrations $N_a = 1 \times 10^{17} cm^{-3}$, $N_d = 1 \times 10^{18} cm^{-3}$

	n_{eff} (for $V_r = 0V$)	n_{eff} (for $V_r = 10V$)	Δn_{eff}	L_π (mm)
TE	3.436054	3.436142	8.814×10^{-5}	8.7925
TM	3.434312	3.434407	9.458×10^{-5}	8.1934

3.1.3 Calculation of Lπ of p-n phase shifter with uniform concentration profiles of $\mathbf{N_a = 1 \times 10^{17} cm^{-3}}$, $\mathbf{N_d = 1 \times 10^{18} cm^{-3}}$

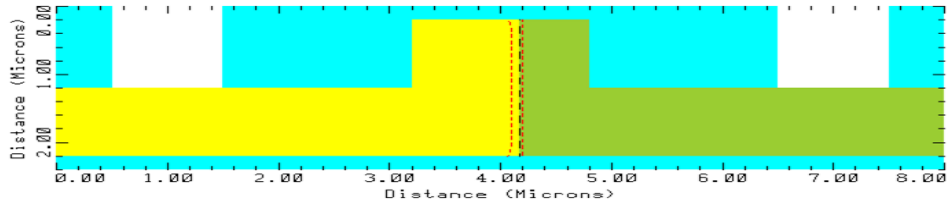
The mesh structure created in MEDICI device simulator for uniform doping profiles of $\mathbf{N_a = 1 \times 10^{16} cm^{-3}}$, $\mathbf{N_d = 1 \times 10^{18} cm^{-3}}$ and p-n^+ junction placed 0.2 μm offset to the middle of the rib waveguide structure so that for applied 10 Volts reverse bias the depletion width will be symmetrical about the rib walls has been shown in Fig. 3.6(a) and 3.6(b).

From the following sections we understood that even though the depletion width of the p-type doping concentration $\times 10^{17} cm^{-3}$ is less compared to the doping profiles $1 \times 10^{16} cm^{-3}$ and $5 \times 10^{16} cm^{-3}$, it will cause large change in refractive index change.

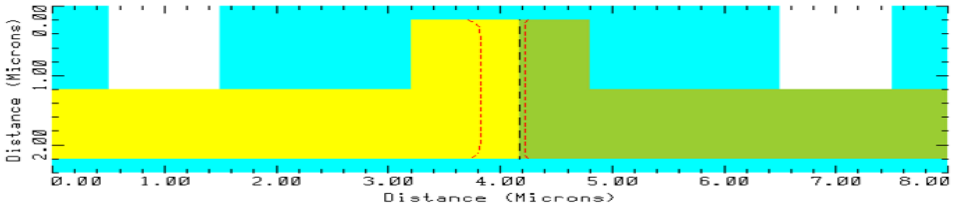


(a) (b)

Figure 3.6: (a)Meshing of the structure for MEDICI simulation of p-n^+ diode embedded in a rib waveguide. (b) Doping profiles of p-n^+ diode with uniform doping concentration of $N_a = 1 \times 10^{17} cm^{-3}$, $N_d = 1 \times 10^{18} cm^{-3}$ in p and n^+ regions respectively and for contacts is has Gaussian profiles with surface impurity concentration $N_s = 1 \times 10^{20} cm^{-3}$ and junction depth 0.5 μm from the contact in device simulator for p-n junction phase shifter for 2 μm rib waveguide



(a)



(b)

Figure 3.7: Depletion width of p-n junction phase shifter for 2μm rib waveguide with uniform doping concentrations $N_a = 1 \times 10^{17} cm^{-3}$, $N_d = 1 \times 10^{18} cm^{-3}$ under applied reverse bias of (a) 0V and (b) 10V

3.2 P-N Phase Shifter Design for 1 μm SOI platform

From the results of P-N Phase Shifter Design for $2\mu m$ rib waveguide we understood that in order to reduce the Figure of Merit of the device, we need to increase the mode profile overlap with the depletion width. Having fixing the p-type doping concentration $\times 10^{17} cm^{-3}$ we can either increaase the reverse bias to get higher depletion width, but increasing the reverse bias will lead to breakdown in the device. Mathematically from the equations from equation (1.3) one can see that a doping of concentration $N_a = 1 \times 10^{17} cm^{-3}$, gives a change in background refractive index of about 3.383×10^{-4} and effective index change will be $\sim 10^{-4}$ if and only if the mode profile dimensions are same as that of depletion width. To increase the mode overlapping area with the depletion width the device dimensions has been reduced to sub-micron.

we consider the oxide cladded single mode rib waveguide with parameters as W = 0.8 μm, H = 0.8 μm and h = 0.5 μm as the basic platform for the design of p-n phase shifter. By using device simulator we introduced a p-n junction under the rib waveguide with the p-type doping concentration $(N_a) 1 \times 10^{17} cm^{-3}$ and n- type doping concentration of Gaussian diffusion profile with surface concentration $N_d = 5 \times 10^{18} cm^{-3}$ in order to increase the overlapping of core part of the optical field with p- type depletion region the p-n junction is positioned to the right of the middle of the core with an offset of 0.2 μm. To ensure good Ohmic contact between silicon and metal contacts, two slab regions 1 μm away from both sides of the rib edge and the junction depth of 0.3 mum away from the rib edge are heavily doped with a dopant concentration of $1 \times 10^{20} cm^{-3}$. The distance between the inner edges of $n^+ +$ and $p^+ +$ doping window is kept at 2 μm so that the guided mode does not overlap with these regions. A schematic cross section view of the phase shifter for sub-micron rib waveguide geometry is shown in Fig. 3.8

Fig. 3.9(a) and 3.9(b) shows the mesh structure created in MEDICI device simulator for uniform doping profile of $\mathbf{N_a = 1 \times 10^{17} cm^{-3}}$, and Gaussian diffusion profile with surface concentration $N_d = 5 \times 10^{18} cm^{-3}$ and p-n^+ junction placed 0.2 μm offset to the middle of the rib waveguide.

Using MEDICI device simulator by varying the reverse bias V_r from 0 V to 20 V the current, depletion width and electric field across the device was found. The I-V charac-

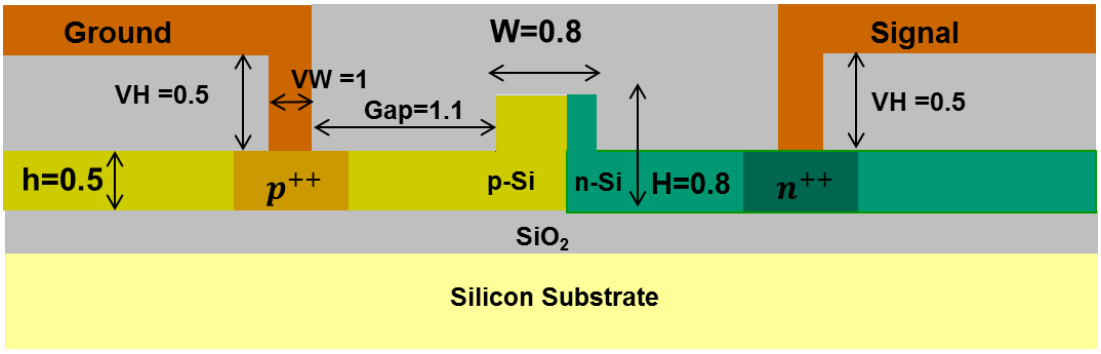
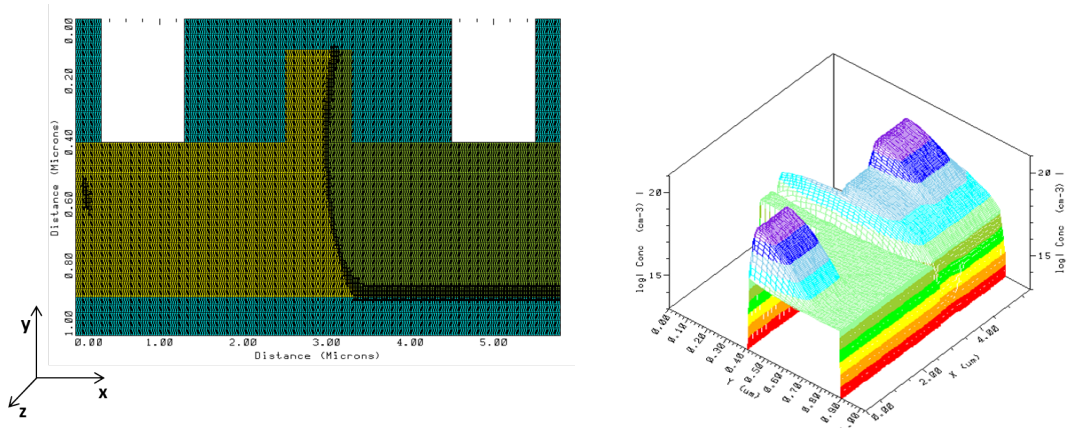


Figure 3.8: Cross sectional view of p-n phase-shifter section for 1 μm SOI platform.



(a) (b)

Figure 3.9: (a) Generated Mesh structure (b) Doping profiles of concentrations $N_a = 1 \times 10^{17} cm^{-3}$, $N_d = 5 \times 10^{18} cm^{-3}$ in MEDICI device simulator for p-n junction phase shifter for $2\mu m$ rib waveguide

teristics of diode have been shown in the Fig. 3.10, which shows the reverse saturation current (I_0) $2.353 \times 10^{-11} A$ the Break down voltage is 16.87 V. The simulated peak electric field in the depletion region is $7 \times 10^4 V/cm$ for V_r = 0V and $3 \times 10^5 V/cm$ for V_r = 12V is shown in Fig 3.11(a) and3.11(a). As earlier discussed under large electric fields (> 10^3 V/cm) in reverse bias operation, the carrier drift will be at their saturation velocity (10^7 cm/sec), so the intrinsic response time is order of few picoseconds. We can achieve high speed modulation with the designed p-n phase shifter.

Fig. 3.12(a) and 3.12(b) shows the depletion width of p-n phase shifter on 1 μm SOI platform with uniform doping profile of $\mathbf{N_a = 1 \times 10^{17} cm^{-3}}$, and Gaussian diffusion profile with surface concentration $N_d = 5 \times 10^{18} cm^{-3}$ for 0V bias and 12V bias respectively.

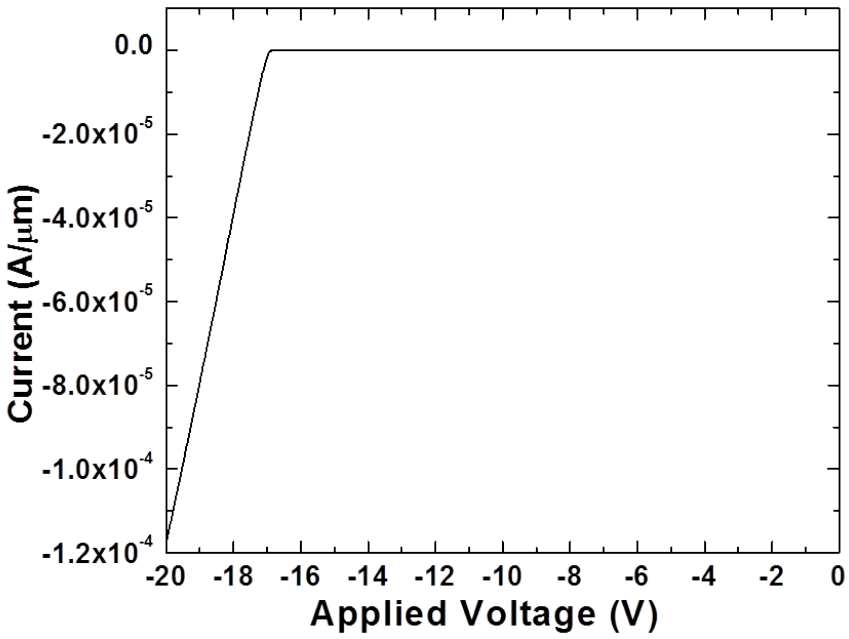
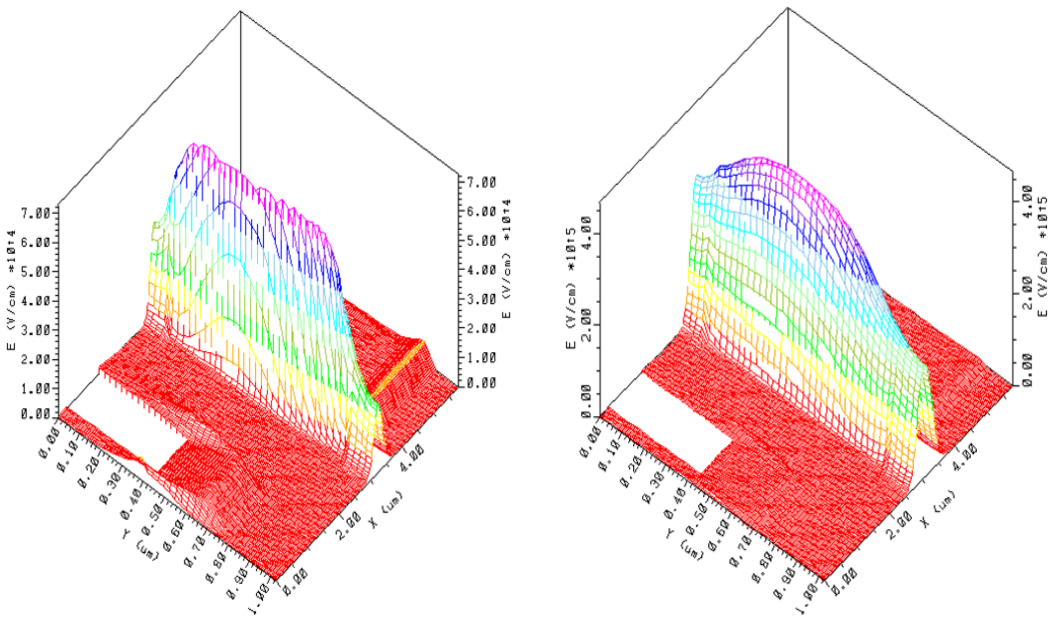
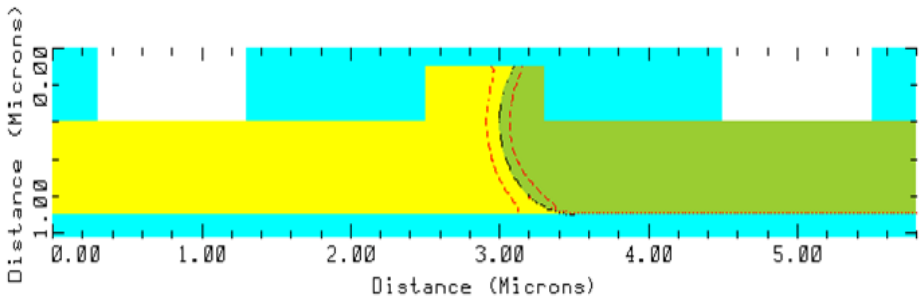


Figure 3.10: Reverse bias I-V characteristics for sub-micron p-n phase shifter with Gaussian doping concentrations $N_a = 1 \times 10^{17} cm^{-3}$, $N_d = 1 \times 10^{18} cm^{-3}$

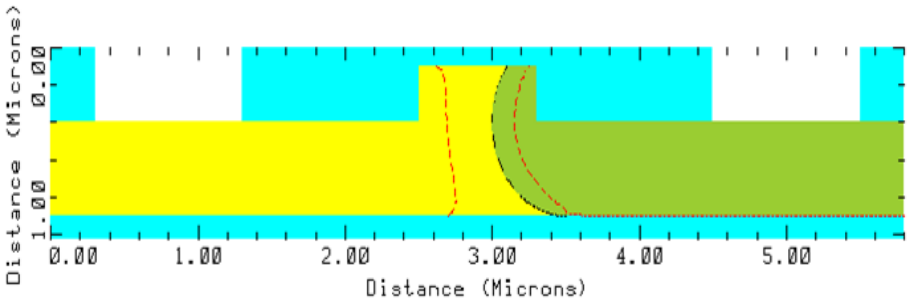


(a) (b)

Figure 3.11: Electric profiles obtained from MEDICI device simulator for p-n phase shifter on 1 μm SOI platform with Gaussian doping concentrations $N_a = 1 \times 10^{17} cm^{-3}$, $N_d = 1 \times 10^{18} cm^{-3}$ under applied reverse bias of (a) 0V (b) 12V



(a)



(b)

Figure 3.12: Calculated depletion width from MEDICI device simulator for p-n junction phase shifter for sub-micron rib waveguide with uniform doping profile of $\mathbf{N_a = 1 \times 10^{17} cm^{-3}}$, and Gaussian diffusion profile with surface concentration $N_d = 5 \times 10^{18} cm^{-3}$ under applied reverse bias of (a) 0V (b) 12V

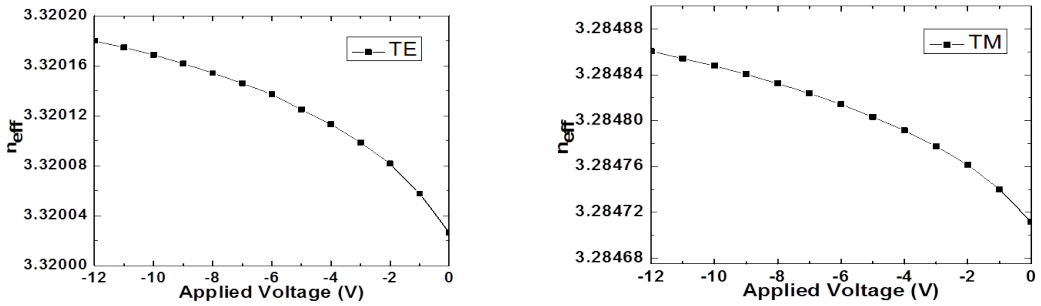
3.2.1 L_π calculation for p-n phase shifter on 1 μm SOI platform

Here we applied the reverse bias voltage from 0V to 12V in steps of 1V and calculated the difference in charge density between 0V to 1V, 0V to 2V and so on till 12V. By using the equation 1.3 and 1.4, the change in background complex refractive index (n+ik) has been calculated and imported into Lumerical Mode solver to calculate the effective index for both TE and TM polarizations. The change in effective index of TE and TM respectively with the applied reverse bias from 0V to 12V has been shown in Fig. 3.13(a) and 3.13(b). Since the change in depletion width of a p-n diode is proportional to the $\sqrt{V_r}$, one can observe that effective index change for both TE and TM is high for low applied bias and less for higher voltages.

The length required to achieve π phase shift is calculated using the equation 3.6. Figure shows 3.14 that the Δn_{eff} is more for TE than TM because core part of TE mode is interacting more with change in carrier density than TM mode. So the length required to achieve π phase shift is less for TE than TM. The calculated $V_\pi L_\pi$ for TE is

6.06 V.cm and TE is 6.23 V.cm for the applied reverse bias of 12V.

Since the p-n phase shifter length ($L\pi$) is 5.05 mm, the modulation bandwidth will be limited by high RC time constant if lumped metal contacts are used. To avoid this speed limitation factor, we need to go for the traveling wave electrode [4], [8], [10], design based on coplanar waveguide or coplanar strip lines, where both the electrical and optical signals co-propagate along the length of the phase shifter experiencing the distributed capacitance, resistances and thus bandwidth limiting factor can be eliminated.



(a) (b)

Figure 3.13: Variation of n_{eff} with applied reverse bias for (a) TE (b) TM for submicron p-n phase shifter

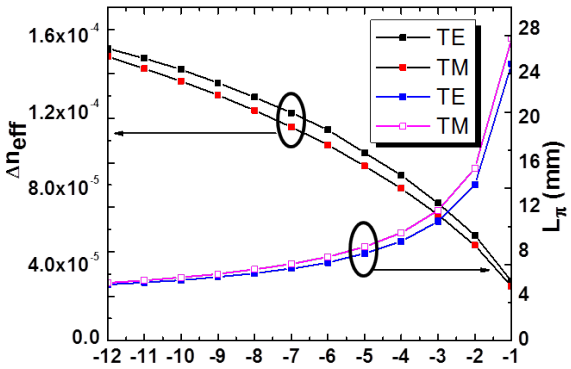


Figure 3.14: Variation of Δn_{eff} and L_π with applied reverse bias for p-n phase shifter on 1 μm SOI platform

3.3 Conclusion

In this chapter, we designed the p-n phase shifter for $2\mu m$ SOI p-n phase shifter by varying the p-type impurity and p-n junction position for fixed $N_d = 1 \times 10^{18} cm^{-3}$ and $L\pi$ was calculated for 0V and applied reverse bias of 10V. The simulation results showed that $N_a = 1 \times 10^{17} cm^{-3}$ will cause large change in refractive index change than $1 \times 10^{16} cm^{-3}$ and $5 \times 10^{16} cm^{-3}$. For p-n phase shifter on 1 μm SOI platform with uniform doping profile of $N_a = 1 \times 10^{17} cm^{-3}$, and Gaussian diffusion profile with surface concentration $N_d = 5 \times 10^{18} cm^{-3}$ the calculated $L\pi$ is 5.05 mm.

CHAPTER 4

Optimization of Fabrication Process flow

The fabrication steps for the device are simulated in TSuprem4. The steps proposed to fabricate the P-N phase shifter for sub-micron waveguide are explained below, with the corresponding parameters and results.

4.1 Waveguide Fabrication

Initially we started with the SOI wafer having the device layer thickness of 1 μm having the background concentration $N_a = 2{\times}10^{17} cm^{-3}$ has shown in Fig. 4.1. We defined the mesh structure of silicon device layer having the thickness of 1 μm, crystal orientation of <100> and the p-type background doping concentration of $2 \times 10^{17} cm^{-3}$.

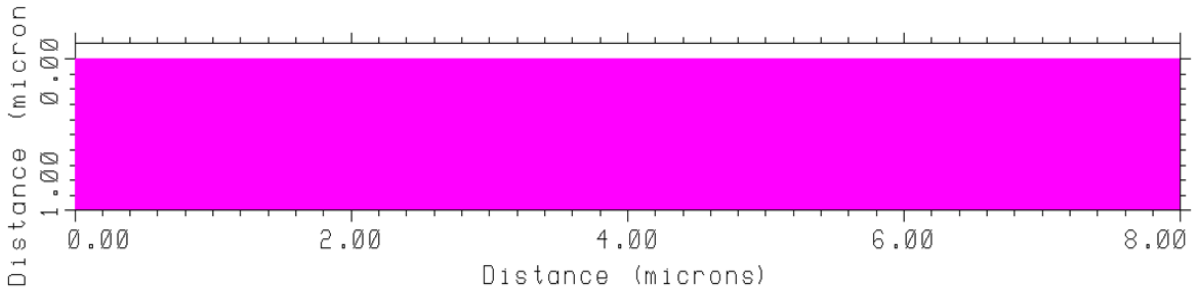


Figure 4.1: P-type substrate of $1\mu m$ thickness

The Fig. 4.2 shows the background concentration of device layer thickness of 1 μm.

A rib structure having width of 0.8 μm ,height of 1 μm and etch depth of 0.3 μm is formed photo-lithography and reactive ion etching. The cross section view of resulted structure is shown in Fig. 4.3

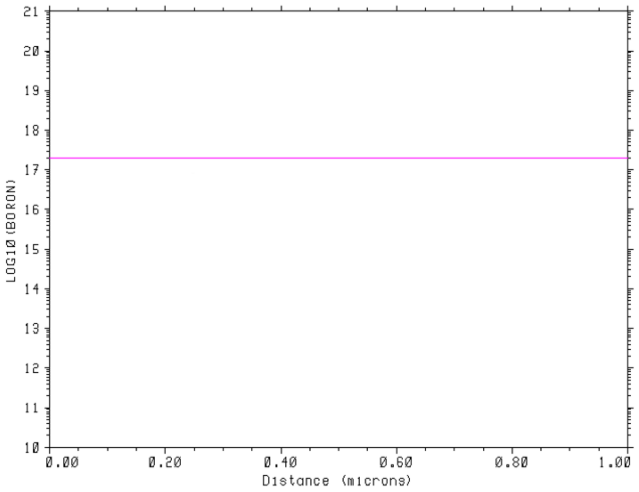


Figure 4.2: Background concentration of p-type substrate

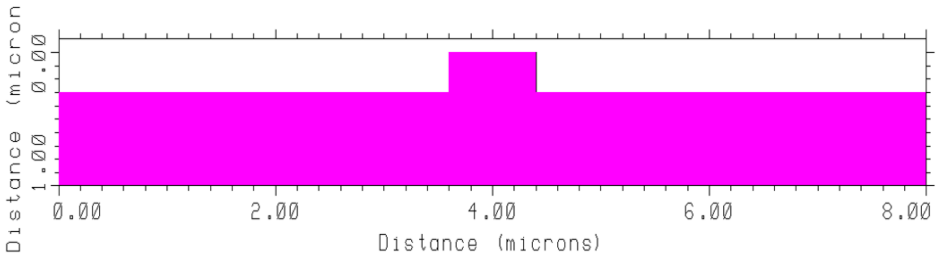


Figure 4.3: Cross sectional view of rib structure formed by photo-lithography and reactive ion etching

4.2 Phosphorous (n-type) Diffusion to form p-n Junction

The next step is to form a p-n junction under the rib by using phosphorus diffusion with SiO_2/Si_3N_4 as masking layer.

A thin layer (150 nm) of Silicon dioxide (SiO_2) is grown over the structure by using dry oxidation process at 1000 ^0C for 25 minutes, in O_2 ambient followed by wet oxidation for 15 minutes in steam ambient. The reason for growing small oxide layer is to reduce the consumption of Silicon from the device layer. Over SiO_2 layer we deposite a thin layer Silicon Nitride (Si_3N_4) of thickness 100nm. Since Silicon Nitride (Si_3N_4) is dense material, diffusivity of dopants is very less compared to the Silicon dioxide. So 100 nm thickness would be sufficient to use as a diffusion mask. This oxide layer also acts as a good interface between Silicon and Silicon Nitride (Si_3N_4). The resulting structure is as shown in Fig. 4.4.

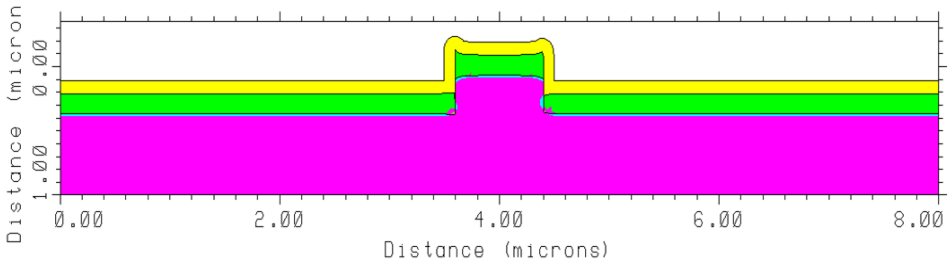


Figure 4.4: Cross sectional view of rib structure after oxidation and nitride depostion

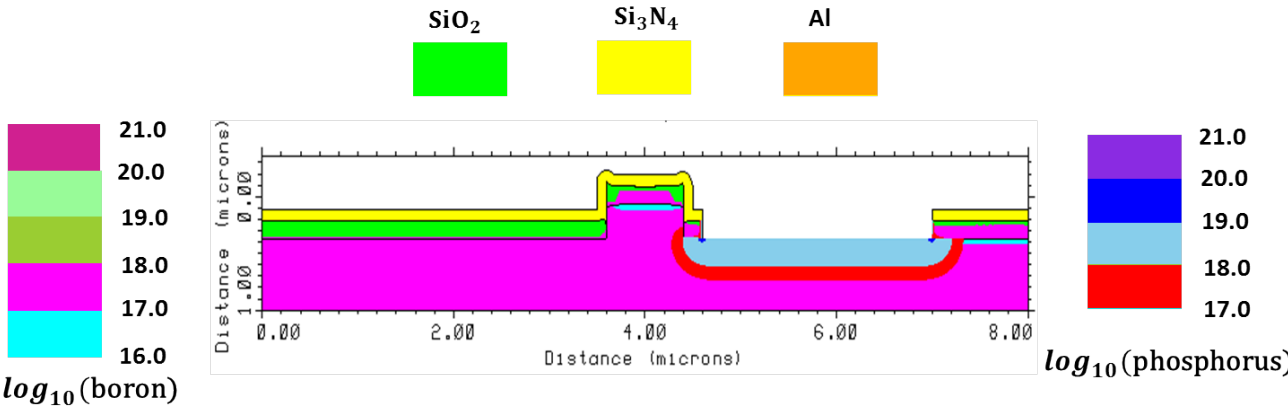


Figure 4.5: Cross sectional view of rib structure after phosphorus predepostion

After coating the PPR on top surface, it is patterned to open diffusion window to the right side of rib by photo-lithography and SiO_2 and Si_3N_4 etching. Now Phosphorous diffusion is done for 2 hours at $1000\,^0C$ to get a surface concentration, $N_d = 1 \times 10^{19} cm^{-3}$. The resulting structure is as shown in Fig. 4.4.

The remaining SiO_2 and Si_3N_4 are etched from the top surface for further processes

4.3 Drive-In:

To ensure the formation of p-n junction in the active region of the rib geometry, Silicon dioxide SiO_2 of 150 nm is grown on top surface by dry oxidation $1000\,^0C$ for 25 minutes, followed by wet oxidation at $1000\,^0C$ for 15 minutes. After that 100 nm Si_3N_4 is deposited on top of SiO_2 in order to control the outdiffusion process during drive-in. Drive-In has been done for 2 hours at $1000\,^0C$ in N_2 ambient. The resulting structure is shown in Fig. 4.6.

Then SiO_2 and Si_3N_4 are etched from top surface for further processes. The resulting structure is shown in Fig. 4.7.

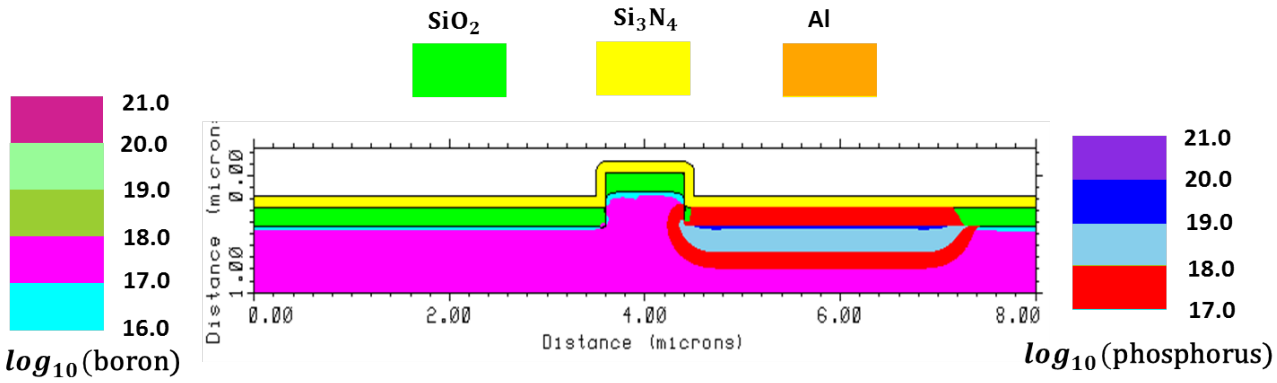


Figure 4.6: Cross sectional view of rib structure after oxidation and nitride depostion

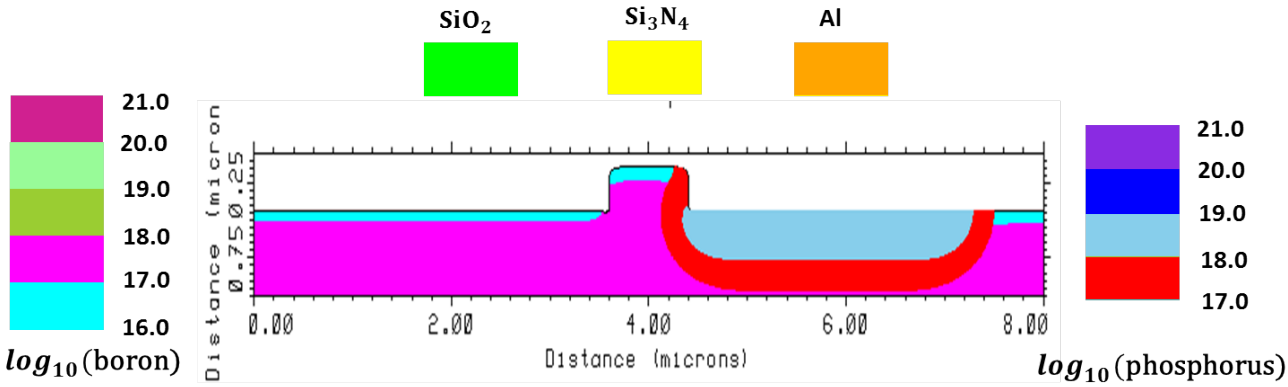


Figure 4.7: Cross sectional view of rib structure after Drive-in

4.4 Phosphorous (n) Diffusion for n-contact

After the drive-in process, due to impurity redistribution the surface concentration will be reduced. In order to increase the surface concentration, again the Phosphorous diffusion has been done. This ensures good Ohmic contact between silicon and metal interface as shown in Fig. 3.8, right side of slab region is doped with the Phosphorous of doping concentration $N_d = 1 \times 10^{20} cm^{-3}$ and junction depth of 0.3 μm which is 1 μm away from the rib edge.

A thin layer (50 nm) of Silicon dioxide (SiO_2) is grown over the structure by using dry oxidation process at 900 ^0C for 30 minutes, in O_2 ambient followed by wet oxidation for 15 minutes in steam ambient. The reason for growing small oxide layer is to reduce the consumption of Silicon from the device layer. Over SiO_2 layer we deposite a thin layer Silicon Nitride (Si_3N_4) of thickness 100nm. The resulting structure is shown in Fig. 4.8.

After coating the PPR on top surface, it is patterned to open diffusion window to

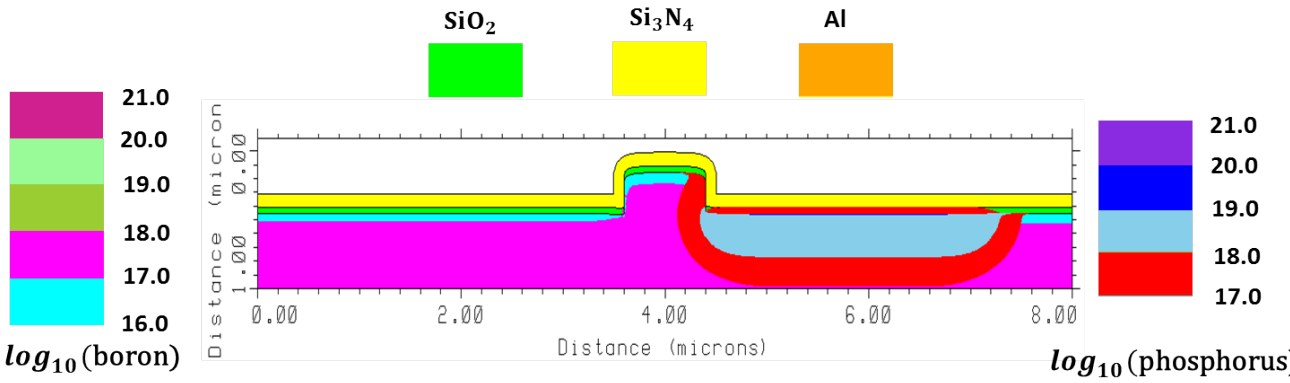


Figure 4.8: Cross sectional view of rib structure after oxidation and nitride depostion

the left side of rib by photo-lithography and SiO_2 and Si_3N_4 etching. Now phosphorus diffusion is done for 45 minutes at 950 ^0C to get a surface concentration, $N_d = 1 \times 10^{20} cm^{-3}$. The resulting structure is shown in Fig. 4.9.

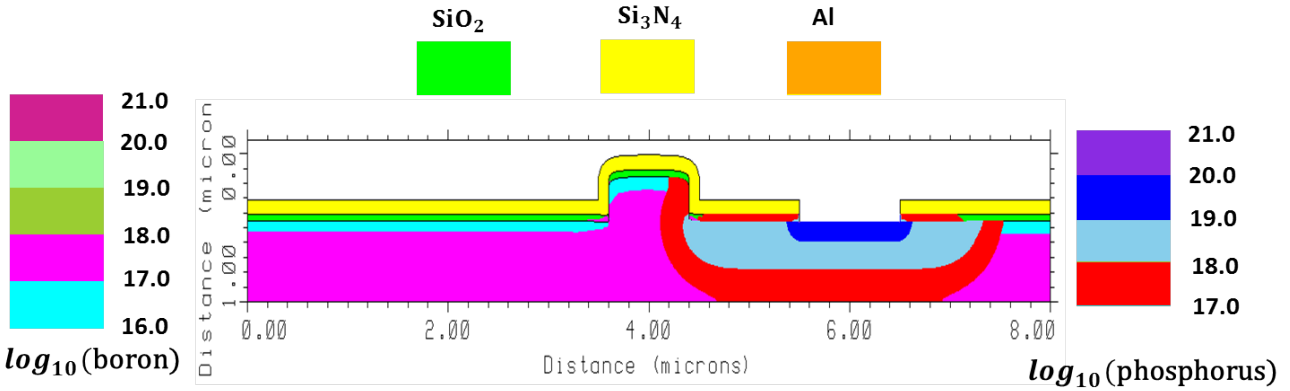


Figure 4.9: Cross sectional view of rib structure after phosphorus predepostion for n-contact

Then remaining SiO_2 and Si_3N_4 are etched from top surface for further processes. The resulting structure is shown in Fig. 4.10.

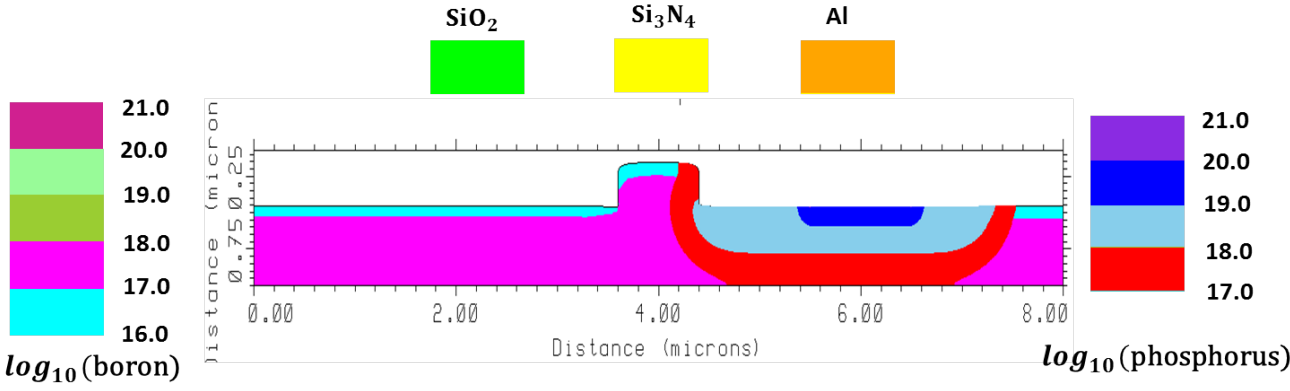


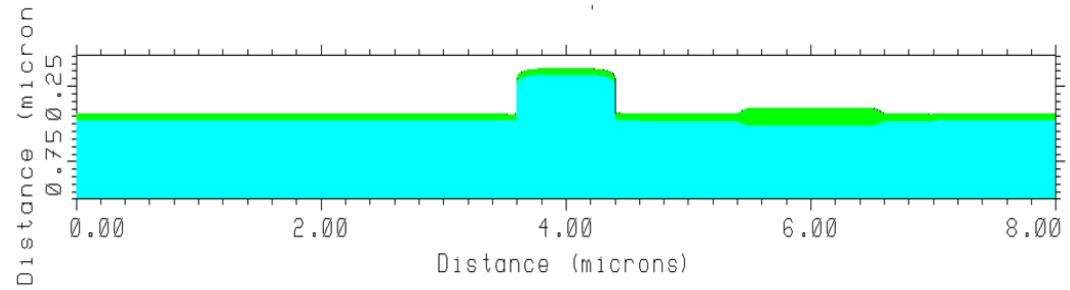
Figure 4.10: After etching remaining oxide and nitride

4.5 Boron (p) Diffusion for p-contact

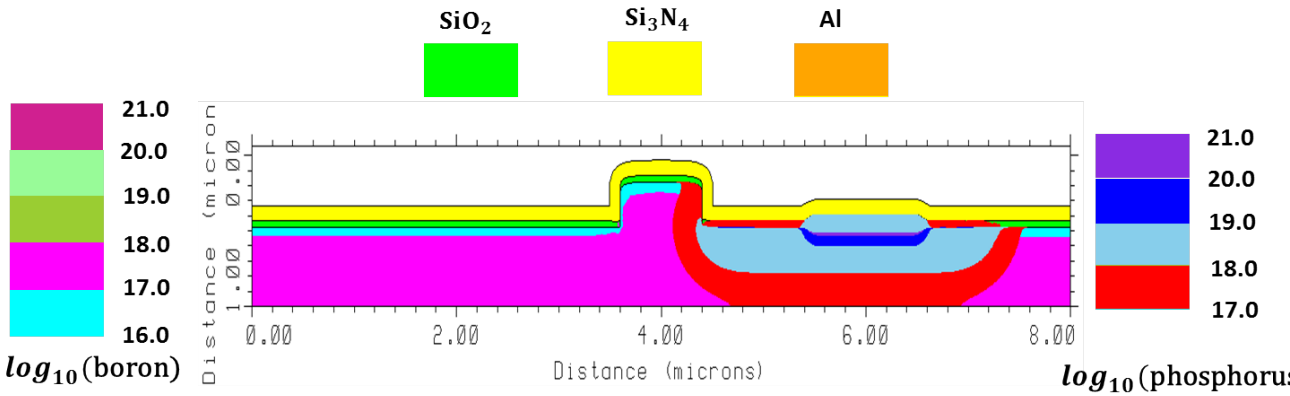
In order to make good p-electrical contact we do boron diffusion with SiO_2/Si_3N_4 as masking layer.

The left side of slab region is doped with the boron of peak doping concentration $1 \times 10^{17} cm^{-3}$ and junction depth of 0.3 μm thickness which is 1 μm away from the rib edge.

If the oxidation is done at 1000 ^0C the oxidation growth rate will be 4-5 times high in highly doped Phosphorus region, making a small vertical projection in the region shown in Fig. 4.11(a), which may lead to violation of single mode condition as effective index changes. So Silicon dioxide (SiO_2) of 50 nm is grown on top by dry oxidation at 850 ^0C for 30 minutes, followed by wet oxidation at 850 ^0C for 30 minutes. Here the oxidation temperature is decreased to reduce the rate of oxidation. After that 100 nm Si_3N_4 is deposited on top of SiO_2. The resulting structure is as shown in Fig. 4.11(b).



(a)



(b)

Figure 4.11: Cross sectional view of rib structure after oxidation and nitride depostion (a) without concentration profiles (b) with concentration profiles

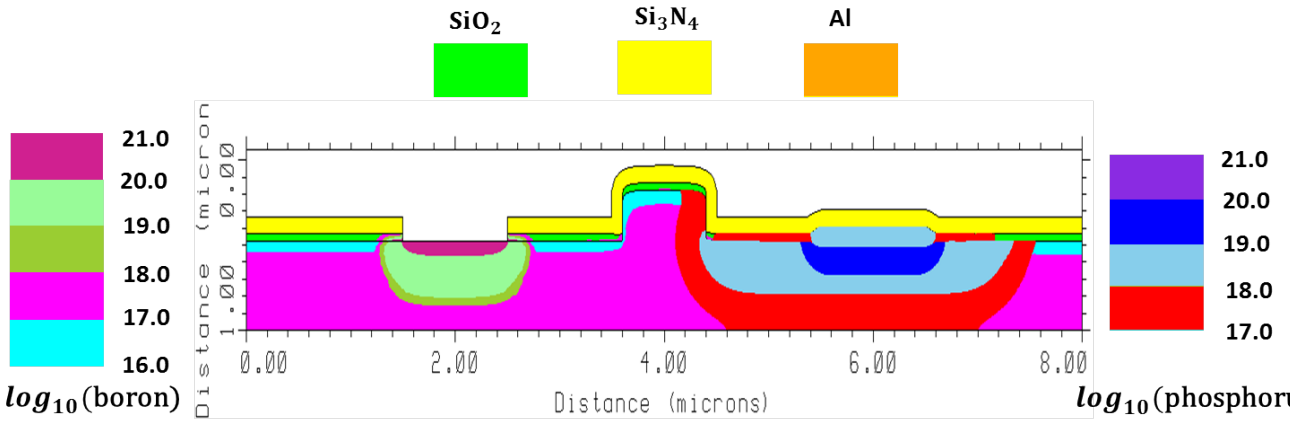


Figure 4.12: Cross sectional view of rib structure after boron predepostion for p- contact

After coating the PPR on top surface, it is patterned to open diffusion window to the left side of rib by photo-lithography and SiO_2 and Si_3N_4 etching. Now boron diffusion is done for 30 minutes at 1000 ^0C to get a surface concentration, $N_a = 1 \times 10^{20} cm^{-3}$. The resulting structure is shown in Fig. 4.12

The remaining SiO_2 and Si_3N_4 are etched from top surface.

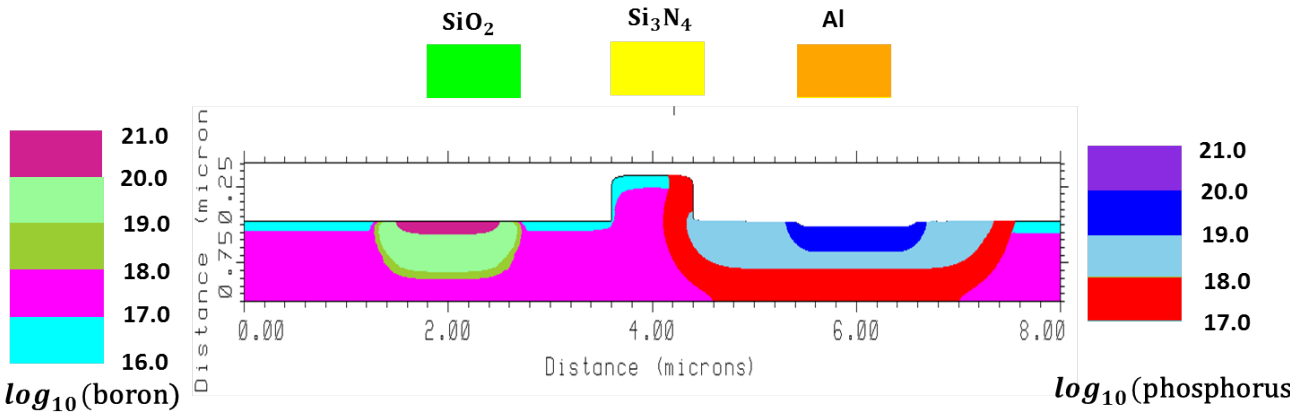


Figure 4.13: Cross sectional view of rib structure after etching remaining oxide and nitride

4.6 Deposition of Metal

The next step is to create vias on the top of highly doped n^{++} and p^{++} regions of the device and deposition of metal as shown in Fig. 3.8.

A thin layer (50 nm) of Silicon dioxide (SiO_2) is grown over the structure by using dry oxidation process at 850 ^0C for 30 minutes, in O_2 ambient followed by wet oxi-

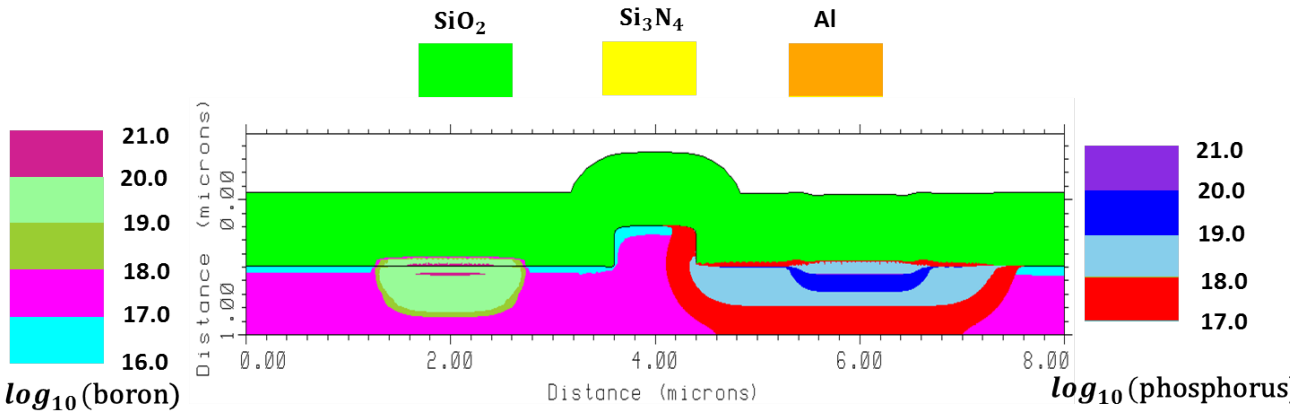


Figure 4.14: Cross sectional view of rib structure after oxide deposition for top cladding

dation for 30 minutes in steam ambient. After that 500 nm SiO_2 is deposited on top surface. The resulting structure is shown in Fig. 4.14.

After this process SiO_2 of width 1 μm is etched to form vias which is 1 μm away from both sides of the rib edge. The resulting structure is shown in Fig. 4.15. Then Aluminum of thickness 0.7 μm has been deposited to make the metal contact by sputtering. The resulting structure is shown in Fig. 4.16.

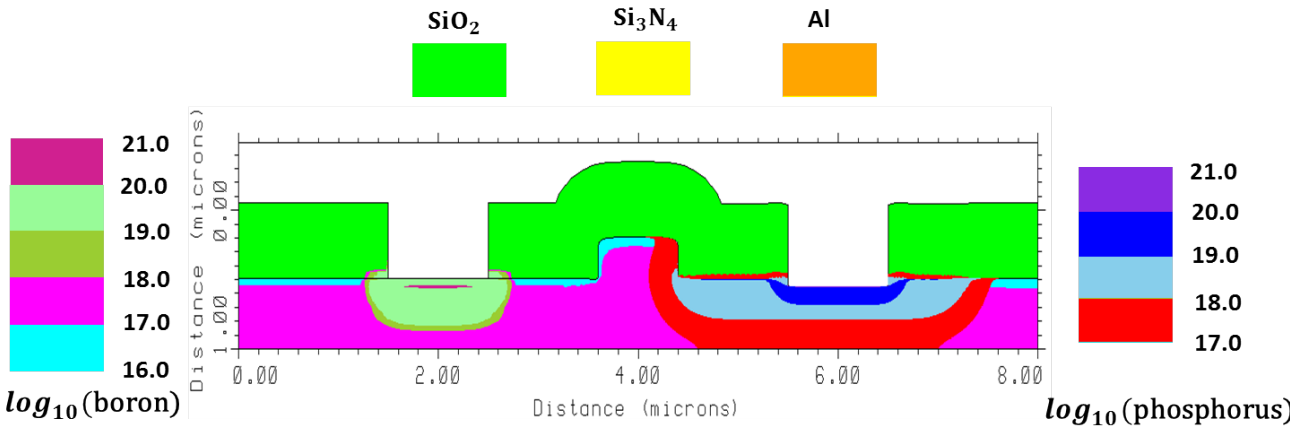


Figure 4.15: Cross sectional view of rib structure after forming vias for metal contact

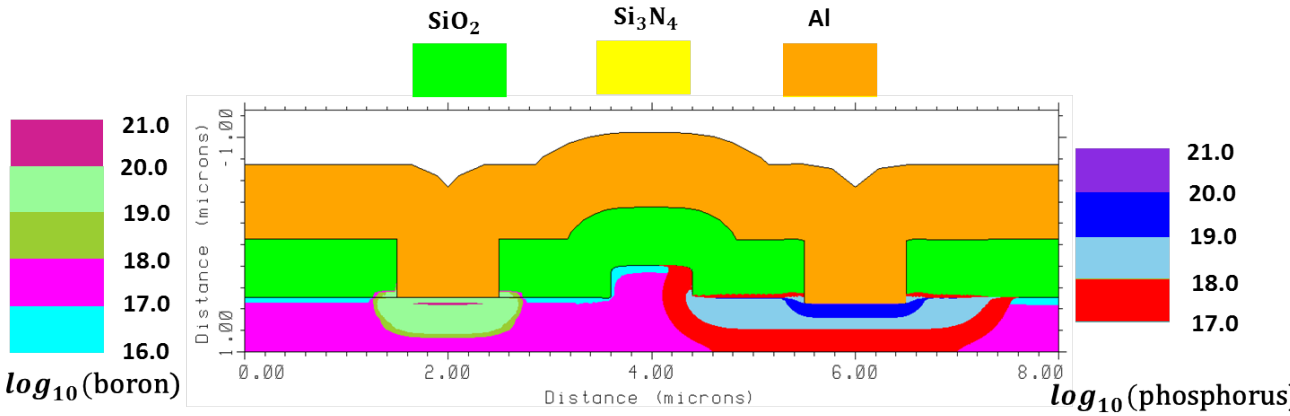


Figure 4.16: Cross sectional view of rib structure after aluminum deposition

To get required geometry the aluminum has been ethed from the top surface as shown in Fig 4.17.

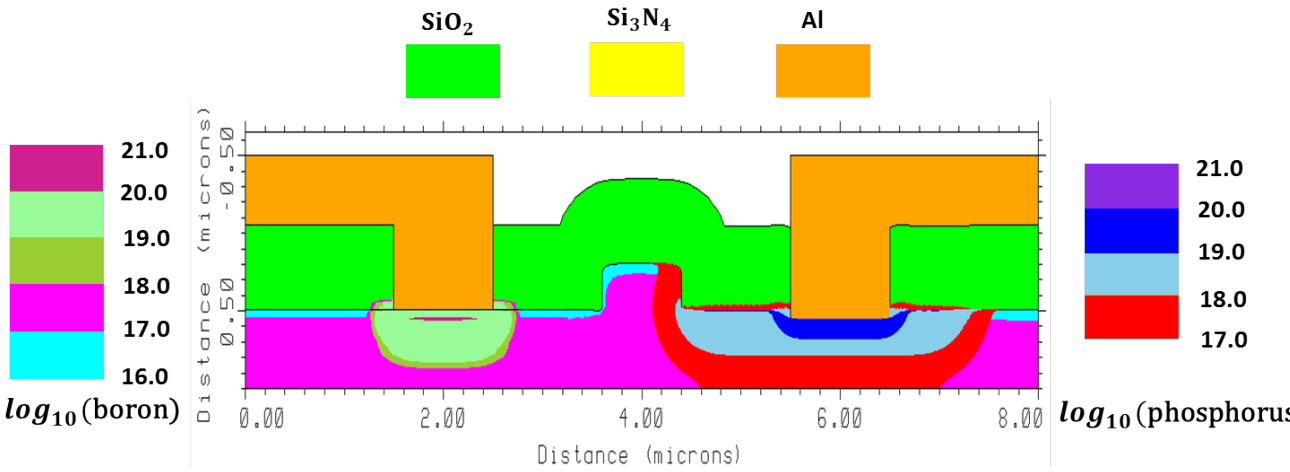


Figure 4.17: Cross sectional view of rib structure after aluminum deposition

4.7 Conclusions

In this chapter, we proposed the steps to fabricate the for p-n phase shifter on 1 μm SOI platform are explained. The fabrication process flow has been optimized using the TSuprem4 process simulator and the corresponding parameters and results are given.

CHAPTER 5

Summary

This chapter summarizes the design, fabrication process flow of a high-speed travelling wave Silicon optical modulator and suggestions for further improvement are provided.

In this thesis, to design the p-n phase shifter for $2mum$ and sub-micron rib waveguide, the waveguide dimensions were optimized such that to operate in sigle mode regime using the Lumerical Mode solver. The p-n junction desgin has been carried out in MEDICI device simulator. The refractive index change for different bias voltages have been calculated form the obtained carrier concentration profiles from MEDICI device simulator. The refracive index profiles were imported into Lumerical Mode solver to find the change in effective index of guided mode profiles to calculate the L_π. The fabrication process flow has been optimized for the designed p-n phase shifter on 1 μm SOI platform using the TSuprem4.

The device can be improved by optimizing the dopant profile and pn junction placement in the waveguide to increase phase efficiency and reduce the Figure of Merit ($V_\pi L_\pi$) and phase shifter loss. The drive-in voltage (V_π) can be reduced by operating the MZI in a push-pull configuration ($\pi/2$ phase shift is required in each arm). The travelling-wave electrode design has to be carried out to avoid the speed limiting factor due to high RC time constant.

In conclusion, we have presented design and fabrication process flow of a high-speed silicon optical modulator.

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