Design of a power efficient 16-bit Discrete Time Delta-Sigma Modulator for audio applications

A THESIS

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THESIS CERTIFICATE

This is to certify that the thesis titled **Design of a power efficient 16-bit Discrete Time Delta-Sigma Modulator for audio applications**, submitted by **Sanjukta Roy**, to the Indian Institute of Technology, Madras, for the award of the degree of **Master of Technology**, is a bona fide record of the work done by her under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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ABSTRACT

The thesis presents the design of a Discrete-Time Delta-Sigma modulator for analog to digital conversion. The primary motivation for exploring Discrete-Time converter is the small gain variation in integrator time-constant due to component mismatch as opposed to about 30% variation in the Continuous-Time equivalent.

The proposed converter is a third order modulator operated at 3.072 MHz and is intended for audio applications. It consists of a 4-bit internal quantizer and targets a resolution of 16-bits for a signal bandwidth of 24 kHz.

Two different op amp architectures have been explored for the loop filter. A comparative study of power vs performance has been done. The best perfomance topology has a simulated SQNR of 109.3 dB and SNDR of 106dB for a correspoding power consumption of 122μA.

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ABBREVIATIONS

SoC	System-on-Chip
ADC	Analog-to-Digital Converter
DTDSM	Discrete-Time Delta Sigma Modulator
CTDSM	Continuous-Time Delta Sigma Modulator
DAC	Digital-to-Analog Converter
STF	Signal Transfer Function
NTF	Noise Transfer Function
OSR	Over Sampling Ratio
MSA	Maximum Stable Amplitude
SNR	Signal-to-Noise ratio
DWA	Data Weighted Averaging
SC	Switched- Capacitor
ELD	Excess Loop Delay
UGB	Unity Gain Bandwidth
UGF	Unity Gain Frequency
DEM	Dynamic Element Matching
CMFB	Common Mode Feedback

CHAPTER 1

Introduction

1.1 Motivation

With System-on-Chip (SoC) integration being the norm of the day, most of on-chip signal processing is done in digital domain. This is mainly because digital signals can convey information with greater noise immunity and fabrication processes these days are optimized for high-density digital design. However, all real world signals are analog and hence data converters are required to form an interface between the real world and the digital world. As digital processing gains more ground, the importance of analog-to-digital converters (ADC) correspondingly increase.

An ADC is characterized by its resolution, speed and power consumption. The motive is always to maximize the first two parameters and minimize the third. A popular architecture is the Delta-Sigma ($\Delta\Sigma$) modulator [1] which are oversampled noised shaped converters. They are closed loop negative feedback converters wherein the quantization noise is high pass filtered by the loop without affecting the input signal strength. These converters are preferred for high resolution, low speed and low power applications. Hence, it is the converter of choice for modern audio applications.

The $\Delta\Sigma$ modulators are implemented either as continuous time (CTDSM) or discrete time (DTDSM) modulators. Most $\Delta\Sigma$ ADCs are built using discrete-time (DT) circuitry. However, continuous-time (CT) circuits are becoming popular now as they operate at higher speeds and consume lesser power compared to

their DT counterparts. The motive to explore DT $\Delta\Sigma$ modulator is to avoid the problems faced by CT modulators like frequency tuning, excess loop delay and clock jitter [2].

In this thesis, design of a DT $\Delta\Sigma$ modulator is presented and a comparative analysis of power vs performance has been done for two different architectures of op amps for the loop filter. A detailed discussion of the theory and design of each building block is presented.

1.2 Organization

Chapter 2 explains the basic concepts of $\Delta\Sigma$ modulators and gives a comparison between CT and DT modulators.

Chapter 3 discusses the implementation issues dealt with while designing a $\Delta\Sigma$ modulator.

Chapter 4 explains the different architectures and design of the loop filter.

Chapter 5 explains the flash ADC and feedback DAC used in the modulator.

Chapter 6 discusses the simulation results.

Chapter 7 concludes the thesis and discusses any future work that may be done.

CHAPTER 2

$\Delta\Sigma$ Modulator Concepts

In this chapter, it will be shown how a $\Delta\Sigma$ modulator converts an analog signal to a digital signal. Thereafter, a comparison of continuous-time and discrete-time modulators is done.

2.1 Operating Principle

Fig. 2.1 shows the block diagram of a $\Delta\Sigma$ ADC. The building blocks are as follows:

1. Loop Filter H(z)
2. Quantizer
3. Digital-to-Analog Converter (DAC)

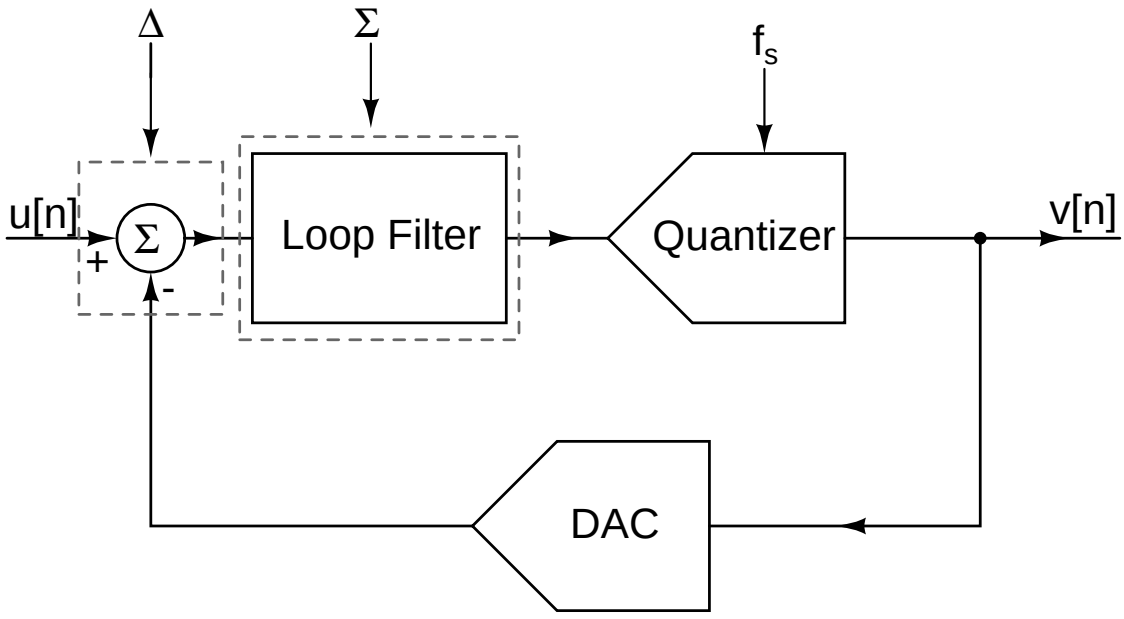

Figure 2.1: Block Diagram of a $\Delta\Sigma$ Modulator

The above structure realizes the shaping of noise with an error minimizing negative feedback loop in which low frequency noise is pushed to higher frequencies outside

the band of interest. The result of this strategy is a close match of input signal and quantized output in the pass-band of the filter. Fig. 2.2 shows the spectrum of the shaped quantization noise.

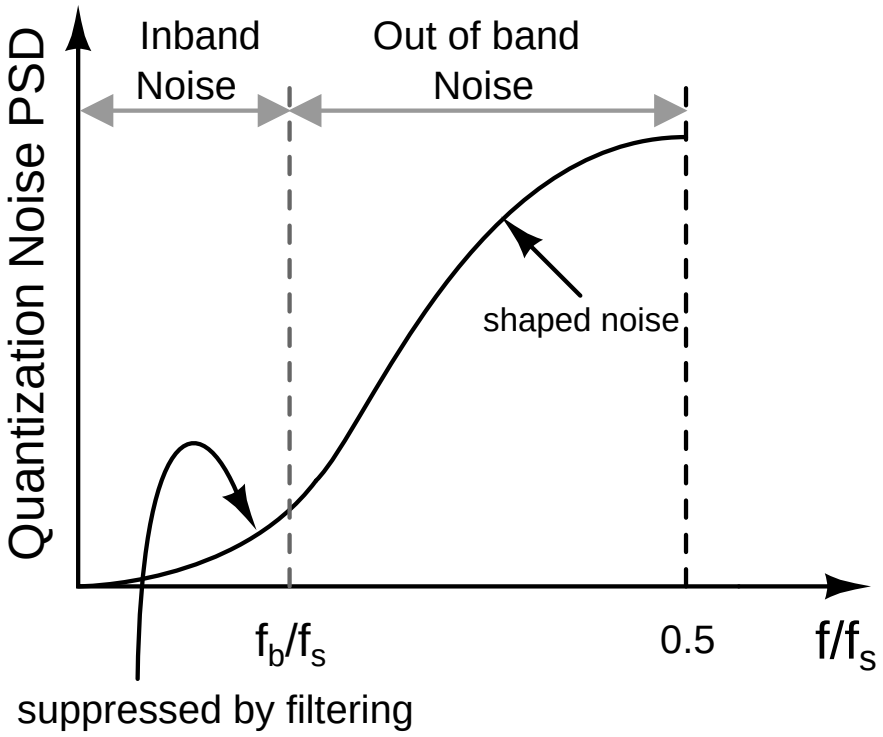

Figure 2.2: Spectrum of Shaped Quantization Noise

Fig. 2.3 shows an equivalent linear model of the system where the quantizer is replaced by an adder, assuming that the adder has 2 independent inputs [3]. Quantization noise added by the quantizer is denoted as e[n] and we assume that it is independent of the input signal u[n].

Output of the modulator is

$$V(z) = \frac{H(z)}{1+H(z)}U(z) + \frac{1}{1+H(z)}E(z) \tag{2.1}$$

$$= STF(z)U(z) + NTF(z)E(z) \tag{2.2}$$

where $STF(z)$ and $NTF(z)$ are signal transfer function and noise transfer function respectively. The loop filter should have a large magnitude in the frequency band

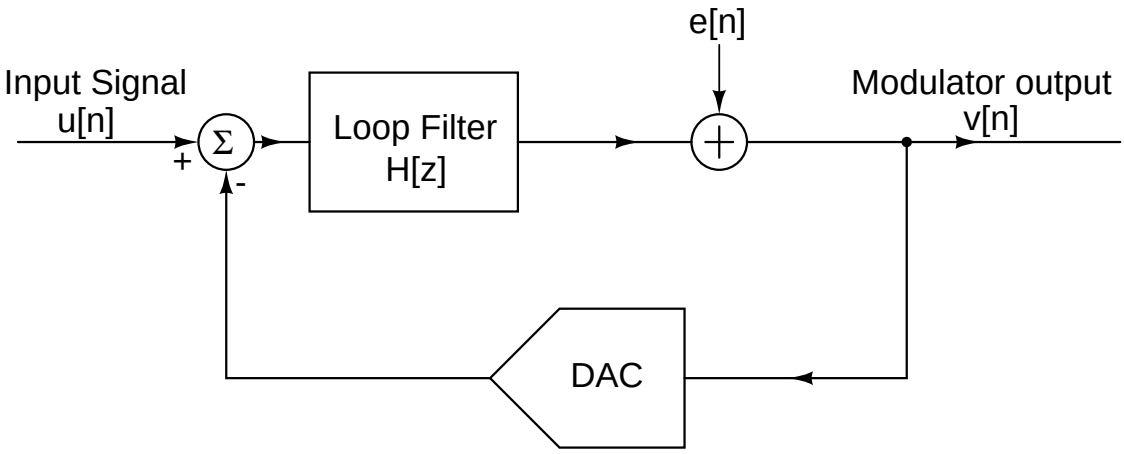

Figure 2.3: Linear model of the Modulator

of interest. If so, $STF(z)$ will approximately evaluate to unity in the frequency band of interest and output will resemble the input very closely. However, the $NTF(z)$ will be close to zero over the same range of frequencies. Thus, we can see that the quantization noise is reduced in the band of interest.

For example, if we take a first-order $\Delta\Sigma$ modulator, then $H(z) = \frac{1}{z-1}$. So from (2.1)

$$STF(z) = z^{-1}, NTF(z) = 1 - z^{-1} \tag{2.3}$$

As can be seen, the $STF(z)$ is just a delay, while the $NTF(z)$ is a discrete-time high-pass filter. Hence, we can see that the quantization noise will be shaped away. In order to obtain a high resolution, the signal must be band-limited to a frequency value much less than the sampling frequency f_s. This is achieved by sampling the signal at very high frequency such that $f_s \gg f_n$ (Nyquist Rate). Hence, $\Delta\Sigma$ ADCs are also called oversampling converters where the oversampling ratio (OSR) is defined as $\frac{f_s}{f_n}$

2.2 Design Considerations

In order to design a $\Delta\Sigma$ modulator, there are several choices that need to be made before starting the design. Some major ones are discussed below.

2.2.1 Order of the Loop Filter

Order of the loop filter is the highest power of z in the polynomial expression of the denominator of H(z). A loop filter of order m is implemented by cascading m integrators with feed-forward or feedback co-efficients.
Order of the modulator can be one or more. As we increase the order beyond 2, system becomes conditionally stable. The maximum value of input signal amplitude, that can be applied to the modulator, known as Maximum Stable Amplitude (MSA), goes on decreasing, as beyond this limit, quantizer will get overloaded.

2.2.2 Oversampling Ratio

Sampling at a rate higher than the Nyquist rate is beneficial as quantization noise reduces by half as OSR doubles and there's an improvement of 3 dB/octave. For a modulator of order m, the improvement is $6m + 3$ dB/octave due to the noise shaping property. This can be shown as follows:

$$NTF(z) = (1 - z^{-1})^m \tag{2.4}$$

Substituting $z = e^{j\omega t} = e^{j2\pi f/f_s}$ gives:

$$|NTF(z)| = 2^m sin^m(\frac{\pi f}{f_s}) \tag{2.5}$$

If Δ is quantizer step-size and f_0 is signal bandwidth, then quantization noise

power evaluates to :

$$P_e = \frac{\Delta^2}{12 f_s} \int_{-f_0}^{f_0} |NTF(z)|^2 df \tag{2.6}$$

Assuming $f_s \gg f_0 (OSR \gg 1)$, value of P_e is

$$P_e = \frac{\Delta^2}{12} \frac{\pi^{2m}}{2m+1} (\frac{1}{OSR})^{2m+1} \tag{2.7}$$

Taking log of the above expression tells us that doubling the OSR reduces the quantization noise power by a factor of $6m + 3$ dB/octave.
The process technology in which the design is implemented and the architecture of the modulator puts a limit on the maximum sampling frequency and hence the OSR.

2.2.3 Quantizer Resolution

We can use either a single-bit or multi-bit quantizer [4]. A single-bit design will be a linear system. However, multi-bit design also has some advantages:

1. For every bit added to the quantizer, quantization error reduces by 6 dB.

2. It improves stability of higher order modulators and hence NTF can be chosen more aggressively which gives better signal-to-noise ratio (SNR).

3. The DAC input to loop filter will change less with every sample, and hence the slew rate requirements of the input op-amp of loop filter is reduced. This leads to lesser power consumption.

4. Quantizer non-idealities don't affect system performance much, as several high gain stages preceed the quantizer, thereby reducing the input referred noise.

The disadvantages of a multi-bit quantizer is that it increases the complexity and the non-idealities in feedback DAC. Any non-ideality in feedback DAC is directly referred to the input. The DAC elements are bound to have mismatch, which

affects the in-band performance of the modulator. Techniques like data weighted averaging (DWA) have to be used to mitigate this problem [5].

2.3 Discrete-time vs. Continuous-time

This section compares the two types of circuitry which are used to implement $\Delta\Sigma$ ADCs.

1. **Process Variation**: The DT modulators are implemented with switched-capacitor(SC) loop filters. SC filters offer the advantage of being more accurate and linear as opposed to the CT modulators which suffer from inferior accuracy and non-linearity. This is because of the RC time constant of the CT loop filter whose value can vary by about 30% due to process variation. On the contrary, the transfer function of an SC circuit is the ratio of capacitors which can be as accurate as 0.5%.

2. **Scaling with clock frequency**: The difference equations describing an SC circuit are independent of the clocking frequency and hence the transfer function scales automatically with clock frequency. However, CT loop filter transfer function doesn't scale naturally with clock frequency. In fact, the calibration done for CT loop filters is valid only at a single frequency.

3. **Clock Jitter**: DT circuits are more robust to clock jitter as compared to CT circuits. As we can see from Fig. 2.4, in DT modulator, most of the charge transfer takes place only at the start of a clock. Whereas, in CT modulator, charge is transferred over the entire clock cycle and jitter will cause an error in the amount of charge transferred. Though the error due to the clock jitter at the input to quantizer will be shaped by the loop filter, any error due to jitter in feedback DAC clock, will be directly referred to the input.

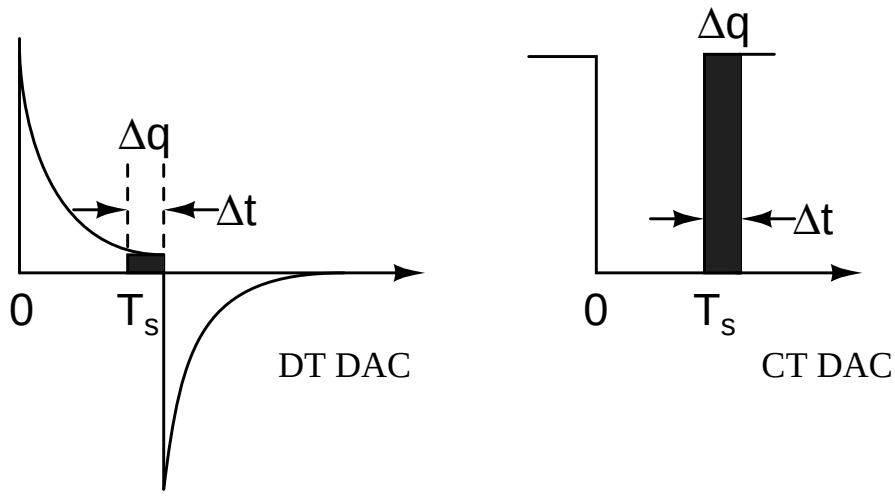

Figure 2.4: Clock jitter effect in DT vs CT modulators

4. **Excess Loop Delay**: The delay introduced due to the finite transient response of the quantizer and the DAC circuitry in the modulator loop filter is known as excess loop delay (ELD) [2]. ELD introduces additional poles that increase the order of both STF and NTF, which may lead to an unstable behaviour of the resulting CT modulator. In order to compensate for this, a number of techniques are present in literature and need to be implemented. ELD isn't a problem for DT modulator as it can tolerate a loop delay of upto one clock cycle due to its discrete-time nature of operation.

5. **Inherent Anti-Aliasing**: CT modulators possess inherent anti-aliasing feature as it postpones the sampling process which is now done at output of the loop filter. This reduces the requirement of the anti-alias filter to be placed at the input of an ADC. In case of a DT modulator, an anti-alias filter is explicitly needed.

6. **Maximum frequency of Operation**: The clock rate for a CT modulator is decided by the response time of the quantizer and feedback DAC. However, in a DT modulator, clock frequency is determined by op-amp settling time requirements. As such, a CT modulator can operate at clock rates of about 2-4 times higher than a DT modulator for a given technology.

7. **Power Consumption**: Due to the requirements of faster op-amp settling in

DT modulators, gain-bandwidth product of the op-amps in loop filter need to be higher in comparison to CT modulators leading to higher power consumption.

CHAPTER 3

Implementation issues in DT $\Delta\Sigma$ Modulators

Here, we will discuss the various non-idealities which affect the performance of DT modulators.

3.1 Settling of Op amp Output

Settling is a very important factor for SC-DT modulators. If the output doesn't settle to the correct value before next clock edge, an incorrect output will be sampled, leading to degraded results.

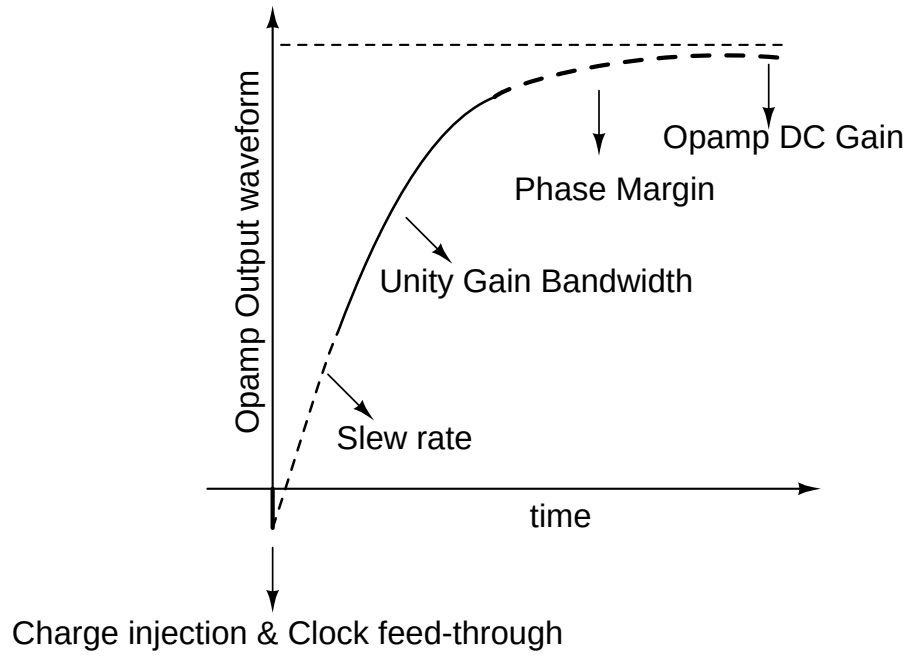

Figure 3.1: Typical output waveform of an op amp and factors affecting it

Fig. 3.1 shows a typical output waveform of an op amp and the various factors which affect its settling.

1. **Charge injection and clock feed-through**: Channel charge will get injected into op amp output in a switched capacitor circuit. Also, due to the input capacitance of the switch, clock gets coupled to signal path and causes clock feed-through. Clock feed-through can be minimized by using CMOS switches at the expense of increased capacitance.

2. **Slew rate**: The output of an op amp will tend to slew, if enough current is not provided to charge the output capacitor to the desired value. Slewing, due to insufficient current, can cause a long time for the capacitor to charge, which if exceeds a clock cycle, can lead to erroneous results.

3. **Unity Gain Bandwidth (UGB)**: Ideally, we want an op amp with infinite UGB. However, a finite UGB introduces additional poles and affects the settling. A more detailed discussion of this factor is done in the next section.

4. **Phase Margin**: Phase margin affects the stability and settling of an op amp. A phase margin > 1 degree is enough to ensure stability. However, a phase margin of 60 degrees allows for the fastest settling time when attempting to follow a voltage step input.

5. **Op amp DC gain**: The DC gain of the op amp decides how close the final settled value is to desired one. Higher the DC gain, less is the error. Normally a 2% to 5% error is tolerable.

3.2 Finite Op Amp Gain

We know

$$NTF(z) = \frac{1}{1 + H(z)} \tag{3.1}$$

where $H(z)$ is the transfer function of the loop filter. If $H(z)$ has a finite value at DC, gain of the NTF at DC changes from zero to 1/A (A=finite DC gain of loop filter).This reduces the amount of attenuation of the quantization noise in the in-band region of interest and therefore degrades the SNR. A rule of thumb to follow is that the DC gain of the op amp, A > OSR [6][7]. This condition ensures that the additional noise that is generated by the finite op amp gain is less than 0.2 dB as against that when A = ∞ [3]. Higher op amp gain also minimizes the input referred noise of the modulator.

3.3 Unity Gain Frequency of Op amp

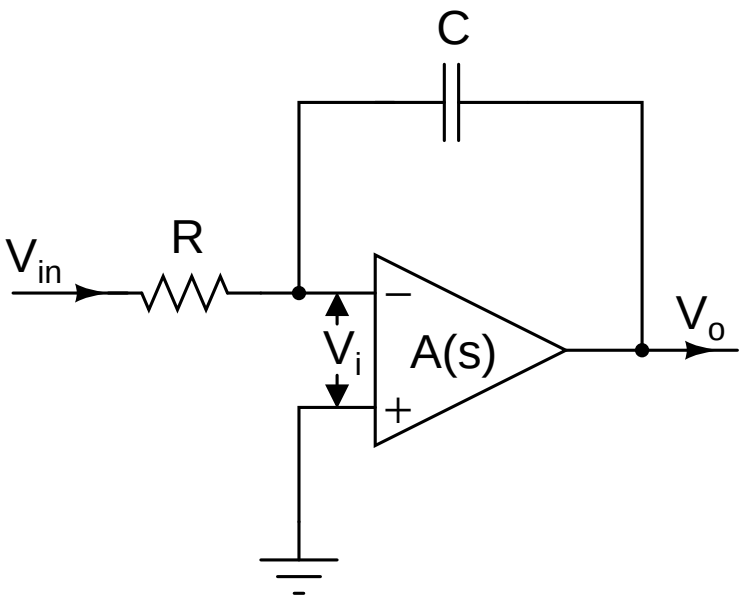

Figure 3.2: First order RC Integrator

Fig. 3.2 shows an integrator having an op amp of gain $A(s)$. Due to unity gain frequency (UGF) ω_u , op amp gain is given by:

$$A(s) = \frac{V_0(s)}{V_i(s)} = \frac{\omega_u}{s} \tag{3.2}$$

Now, integrator transfer function from $V_{in}(s)$ to $V_0(s)$ is:

$$\frac{V_0(s)}{V_{in}(s)} = \frac{-1}{sRC(1 + \frac{1}{\omega_u RC} + \frac{s}{\omega_u})} \tag{3.3}$$

$$= \frac{-1}{sRC(1 + k_1)(1 + \frac{s}{\omega_u(1+k_1)})} \tag{3.4}$$

where $k_1 = \frac{1/RC}{\omega_u} = \frac{UGF\ of\ Integrator}{UGF\ of\ opamp}$

(3.3) shows that due to the finite UGF of op amp, integrator gain is changed from $\frac{1}{sRC}$ to $\frac{1}{sRC(1+k_1)}$ and the second pole introduces an additional delay of $\frac{1}{\omega_u(1+k_1)}$. This is shown in Fig. 3.3.

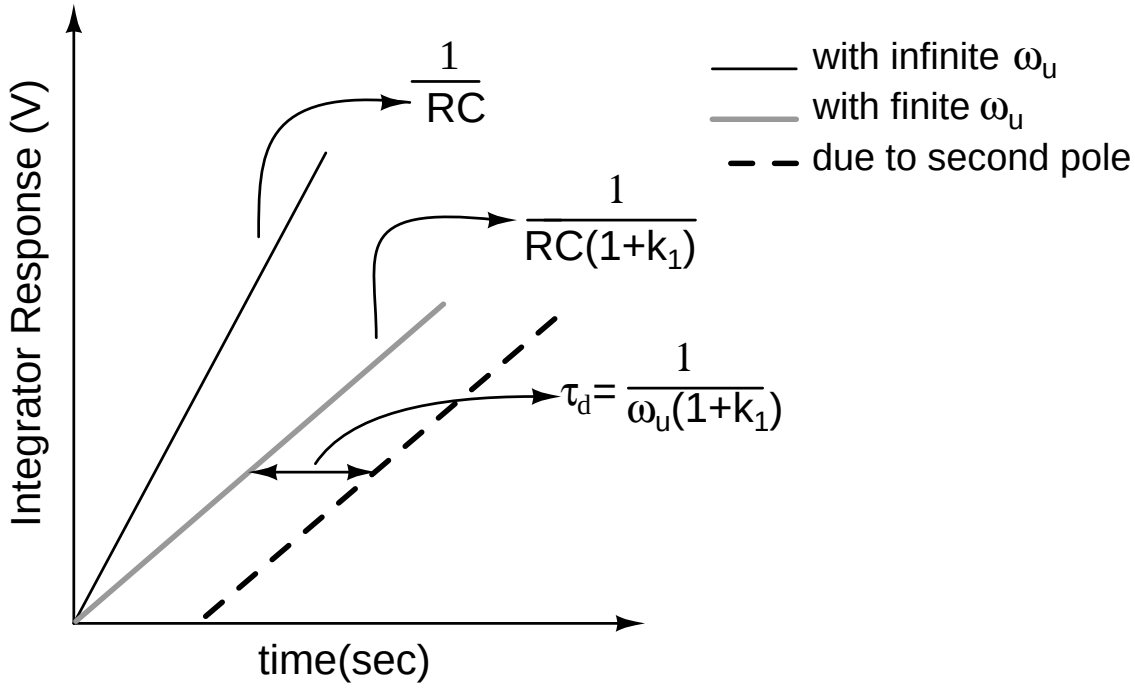

Figure 3.3: Integrator Response due to finite UGFs of op amps in loop filter

Hence, finite UGF of the op amp modifies the UGF of the integrator and causes a delay due to the additional pole introduced. In literature it is suggested that the unity-gain bandwidth of the op amp must be at least an order of magnitude

greater than the sampling rate [8].

3.4 Mismatch in DAC

The primary advantage of noise-shaping modulators employing multi-bit quantizers is that the quantization noise power reduces by 6 dB for every additional bit. An additional benefit of multi-bit quantization is that it enhances system stability. For a $\Delta\Sigma$ modulator employing a multi-bit internal quantizer, the internal DAC also needs to be multibit.

However, the integral linearity of the noise shaping converter is no better than the integral linearity of the internal multi-bit DAC. Hence, any error in the spacing between the DAC levels will be directly referred to the input. As a result the noise shaping property of the modulator will be lost. As such, the overall resolution of the converter is only as good as the matching across the DAC elements. The DAC non-linearity increases the in-band noise floor along with harmonics in the in-band region. To achieve a high degree of linearity, the DAC components must be precisely matched. However, CMOS VLSI process are optimized for high density digital design than high performance analog design.
The above problem can be mitigated by using the techniques of dynamic element matching (DEM) wherein the same output code is represented by a different set of mismatched DAC elements each time.

3.5 Intrinsic Noise

Intrinsic noise is the one that is generated in the device itself as opposed to noise that couples from an external interfering source. Intrinsic noise cannot be eliminated since it is a property of the device. However, we can modify its value by proper choice of circuit topology and component sizes. The various sources of

intrinsic noise are:

1. In a switched-capacitor DT $\Delta\Sigma$ modulator, the voltage sampled on the input capacitor has an uncertainty of kT/C [8] where k is Boltzmann's constant, T is absolute temperature, and C is the sampling capacitor. The in-band contribution will be kT/(C.OSR). The value of the sampling capacitor will be determined from the resolution of the converter. For relatively high resolutions large values of sampling capacitors might be necessary.

2. Thermal noise is caused by the random fluctuation of carriers due to thermal energy. The thermal noise contribution of the first op amp in the loop filter needs to be kept small as it will directly get referred to the input. Since the thermal noise contribution is inversely proportional to g_m of the input differential pair, it can be reduced by proper sizing of the transistors.

3. The MOS flicker noise is also called 1/f noise since it has a spectral density that inversely varies with frequency. The input referred 1/f noise of a $\Delta\Sigma$ modulator is very nearly equal to the input-referred 1/f noise of the op amp in the first integrator. One method for decreasing the 1/f noise is to increase the gate area of MOS transistors of the first op amp that contribute to the op amp noise.

3.6 Limited Output Swing

An m^{th} order loop filter has m op amps that are connected as integrators. If the integrator op amps do not have sufficiently large output swings, modulator behaviour will be affected. It may lead to clipping of integrator outputs which will result in an increased noise floor. In order to avoid clipping of integrator outputs, node-scaling can be performed where the modulator components are scaled so that there's no clipping at its output.

CHAPTER 4

Loop Filter

The loop filter is one of the major building block of the $\Delta\Sigma$ modulator which shapes the quantization noise away from signal band. This chapter discusses the various topologies of a loop filter and then describes the design of the 3^{rd} order DT loop filter.

4.1 Working Principle of a Loop Filter

The general block diagram of a $\Delta\Sigma$ modulator with quantizer is shown in Fig. 4.1.

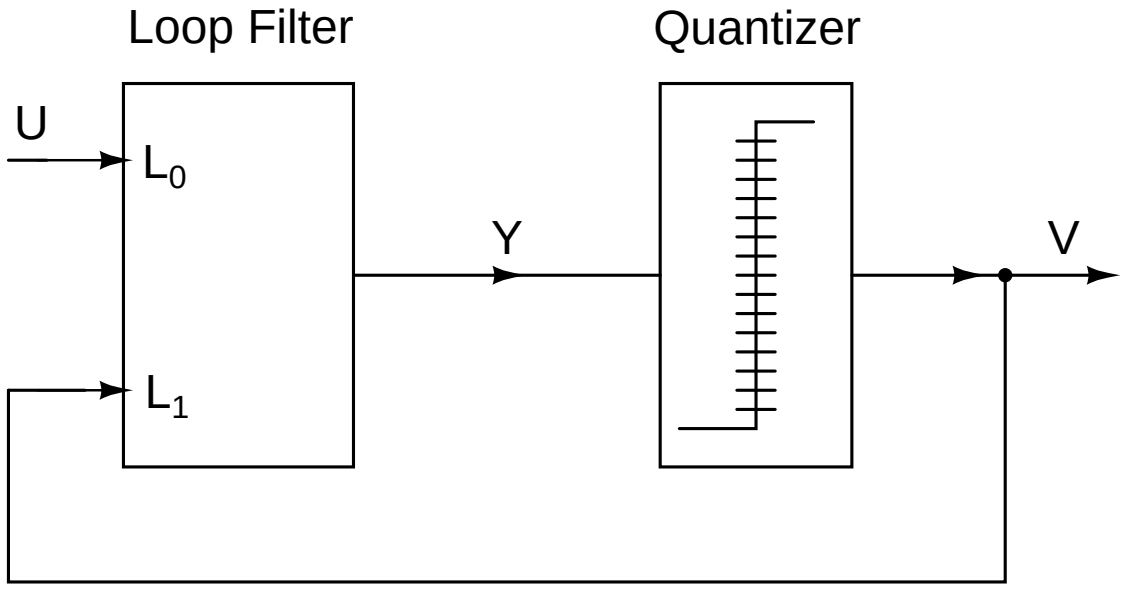

Figure 4.1: General Structure of $\Delta\Sigma$ modulator

The modulator is modeled as a two-input system with a single output [3]. The output of the modulator in terms of its inputs U and V is:

$$Y(z) = L_0(z)U(z) + L_1(z)V(z) \tag{4.1}$$

The quantizer is modeled as before. It adds an error signal to its input.

$$V(z) = Y(z) + E(z) \tag{4.2}$$

Using the above two equations the output of the modulator can be written as a linear combination of the input signal U and the quantization error E as follows:

$$Y(z) = STF(z)U(z) + NTF(z)E(z) \tag{4.3}$$

where,

$$STF(z) = \frac{L_0(z)}{1 - L_1(z)} \tag{4.4}$$

$$NTF(z) = \frac{1}{1 - L_1(z)} \tag{4.5}$$

From (4.4) and (4.5), it can be seen that L_1 must have a large magnitude in the signal band 0 to $f_s/(2.\text{OSR})$ to reduce the NTF magnitude within the signal bandwidth. Also, L_0 must have a large magnitude in the same band so that the STF magnitude is unity.

When the loop filter has a single input and only the difference u[n] - v[n] enters the loop filter then $L_0 = L_1 = L$ and (4.4) and (4.5) become:

$$STF(z) = \frac{L(z)}{1 + L(z)} \tag{4.6}$$

$$NTF(z) = \frac{1}{1 + L(z)} \tag{4.7}$$

Fig. 4.2 shows another case where a direct path is added [9]. While L_1 remains unchanged, L_0 changes to $L + 1$. Hence, the NTF remains the same as given in (4.7) while the STF becomes:

$$STF(z) = \frac{L(z) + 1}{1 + L(z)} = 1 \tag{4.8}$$

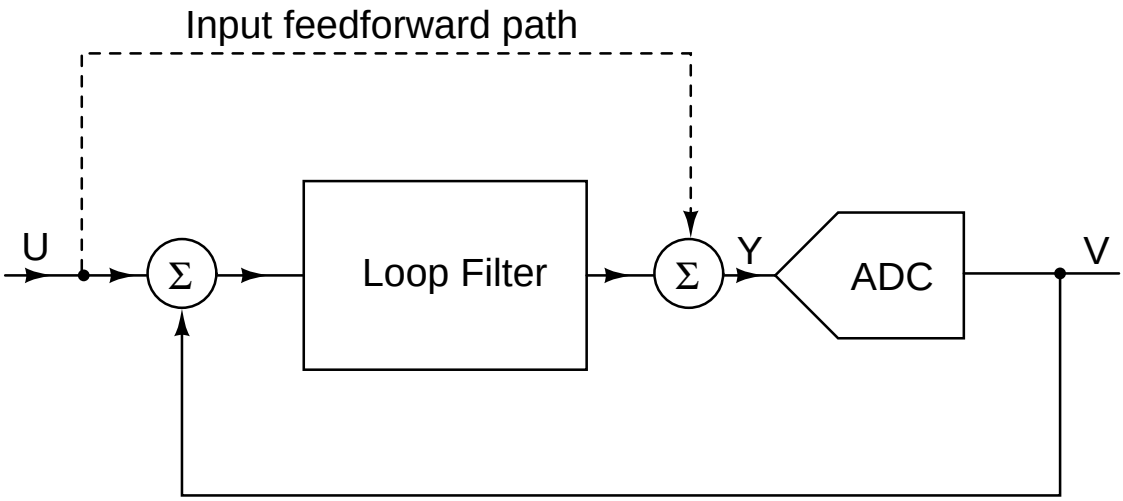

Figure 4.2: Single feedback topology with feed-forward path

Since the signal transfer function is unity, the input U appears at the output directly. The loop filter input is given by:

$$U - V = U - (STF.U + NTF.E) = -NTF.E = \frac{-E}{1+L} \tag{4.9}$$

The above equation indicates that the loop filter input no longer contains the input signal, but only the filtered quantization noise. This simplifies the design of the loop filter since it need not have high linearity, thereby decreasing power consumption.

4.2 Architectures

In this section two different loop filter architectures are discussed as follows:

1. Cascaded Integrators with distributed feedback (CIFB)
2. Cascaded Integrators with distributed feed-forward (CIFF)

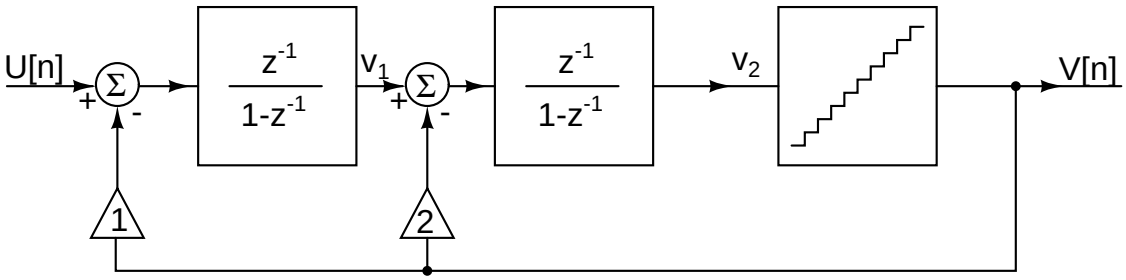

Figure 4.3: CIFB architecture

4.2.1 CIFB Architecture

Fig. 4.3 shows the block diagram of a 2^{nd} order loop filter with a CIFB structure. It contains a cascade of two integrators where each integrator is fed the feedback signal with different weight factors. The transfer functions are as follows:

$$STF(z) = \frac{Y}{X} = z^{-2} \tag{4.10}$$

$$NTF(z) = \frac{Y}{Q} = (1 - z^{-1})^2 \tag{4.11}$$

$$v_1 = z^{-1}(1 + z^{-1})X - z^{-1}(1 - z^{-1})Q \tag{4.12}$$

$$v_2 = z^{-2}X - z^{-1}(2 - z^{-1})Q \tag{4.13}$$

where Q is the quantization error.

As can be seen from the above equations, the first integrator will have the largest input signal component and minimum amount of quantization noise, while the last one will contain a small part of the input signal and the maximum amount of noise. Since the output of an integrator represents the input of the subsequent stage, it follows that the linearity of the first integrating stage is more critical than the linearity of the final ones. Hence, the first op amp will be power hungry. The final op amp will also be power hungry due to speed requirements as it is the fastest path in the loop.

4.2.2 CIFF Architecture

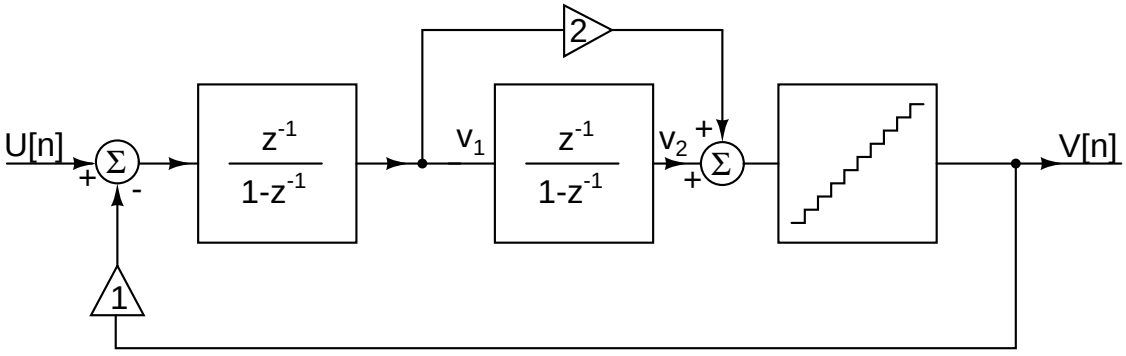

Figure 4.4: CIFF architecture

Fig. 4.4 shows the block diagram of a 2^{nd} order loop filter with a CIFF architecture. The transfer functions are as follows:

$$STF(z) = \frac{Y}{X} = z^{-1}(2 - z^{-1}) \tag{4.14}$$

$$NTF(z) = \frac{Y}{Q} = (1 - z^{-1})^2 \tag{4.15}$$

$$v_1 = z^{-1}(1 - z^{-1})X - z^{-1}(1 - z^{-1})Q \tag{4.16}$$

$$v_2 = z^{-2}X - z^{-2}Q \tag{4.17}$$

where Q is the quantization error.

For this topology the first integrator will contain small amount of the input signal and a large amount of filtered quantization noise. The last integrator will introduce large amount of in-band distortions but this will be shaped by the loop filter. Again only the linearity of the first integrator is critical. Also, the fastest path in the loop is through the first integrator and hence is power hungry to meet speed requirements. Hence, only the first integrator is power hungry for this topology. So, for low power applications, CIFF structure is preferred over CIFB.

4.3 Design Process for Implementation of Loop Filter Transfer Function

The first step in the design of a $\Delta\Sigma$ modulator is the choice of the modulator order and its noise transfer function (NTF). The modulator to be designed is of order 3, has an OSR of 64 and with an internal quantizer of 4 bits. The NTF of the modulator has an out-of-band gain (OBG) of 2.5. OBG is defined as the gain of the NTF at frequencies close to $\omega = \pi$. A modulator with the above characteristics was simulated in MATLAB.

The following steps were followed to find the transfer function of the DT loop filter:

1. Using the Sigma-Delta toolbox in MATLAB, the NTF of a 3rd order DT $\Delta\Sigma$ modulator with an OBG of 2.5 is determined.

$$NTF(z) = \frac{(z-1)^3}{(z-0.417)(z^2-0.8778z+0.3804)} \tag{4.18}$$

2. The DT loop filter transfer function L(z) is given by:

$$L(z) = \frac{1-NTF(z)}{NTF(z)} = 1.7052(\frac{z^2-1.3216z+0.4934}{(z-1)^3}) \tag{4.19}$$

3. Splitting the above equation into partial fractions gives the coefficients as:

$$L(z) = \frac{1.7052}{(z-1)} + \frac{1.1568}{(z-1)^2} + \frac{0.2930}{(z-1)^3} \tag{4.20}$$

The above equation for $L(z)$ can implemented by a cascade of three integrators and a summer. Fig. 4.5 shows the block diagram for the implementation of $L(z)$.

Fig. 4.6 shows the schematic for the modulator loop filter built using op amps:

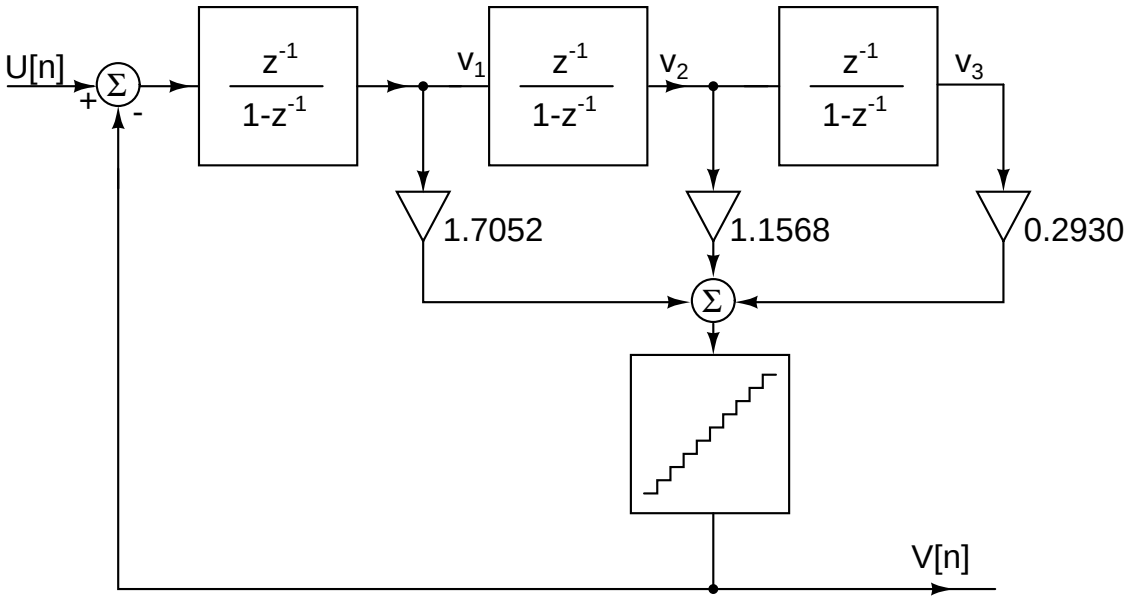

Figure 4.5: Block Diagram of 3^{rd} order loop filter

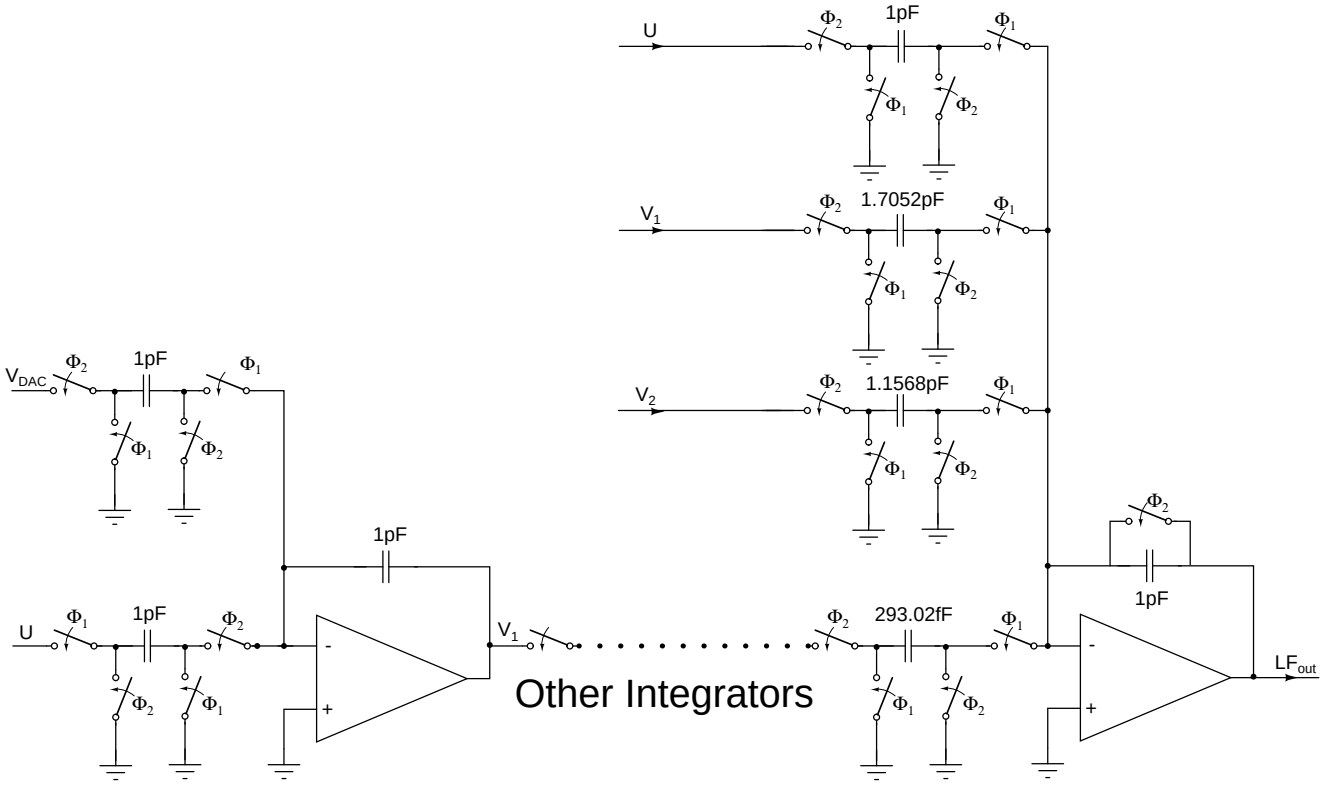

Figure 4.6: Schematic of Loop filter

4.4 First Integrator Op amp

The first integrating op amp needs to be carefully designed since it determines the overall distortion of the data converter. Any distortion in the succeeding op amps becomes insignificant when referred back to the input due to the high gain of the previous stages. The first integrating op amp is a single-stage op amp. It has been made single-stage to get good phase margin, as settling of op amp output is crucial here. The op amp architecture is an inverter-based CMOS amplifier. This topology was chosen to get more gain by consuming same current in comparison to conventional topology. Fig. 4.7 shows the schematic of the first op amp.

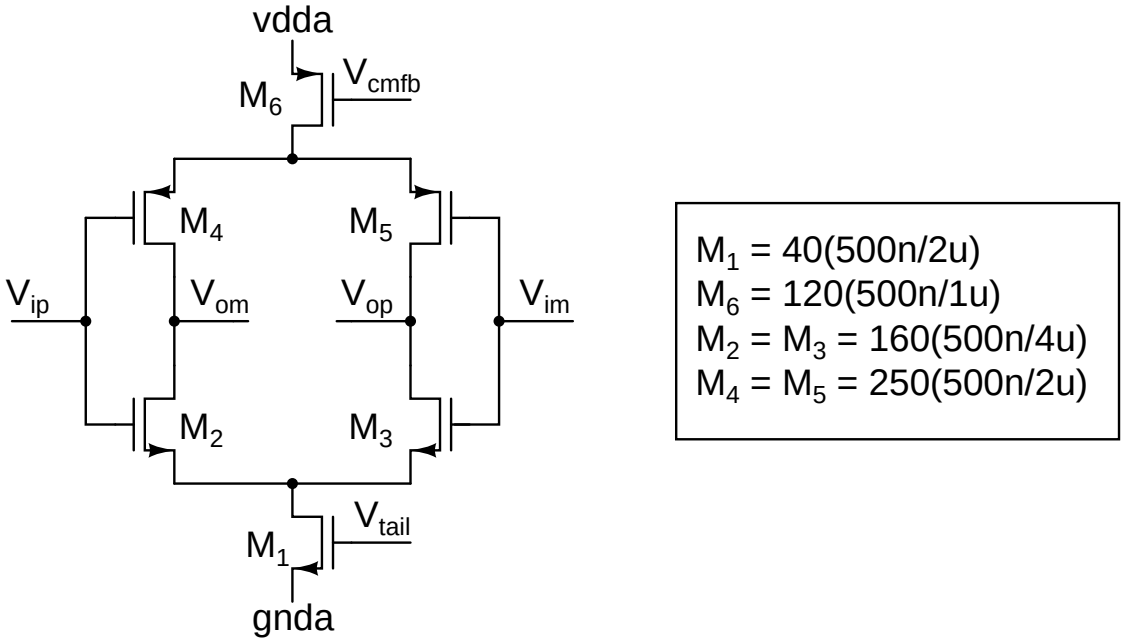

Figure 4.7: Schematic of First Integrator Op Amp

Noise is an important consideration while choosing the op amp input stage. The major source of noise at low frequencies is the 1/f noise of the MOS transistors. This topology is advantageous in case of noise performance as here both PMOS and NMOS are contributing to signal power as well as noise power unlike the case of conventional differential amplifier where input NMOS or PMOS stage contribute to both signal power as well as noise power but load PMOS or NMOS stage contributes to noise power only. Hence, to achieve same dynamic range, this

configuration will need less power compared to conventional structure.

4.4.1 Common-Mode Feedback Circuit (CMFB)

In fully-differential circuits with feedback, the feedback determines the differential signal voltages, but does not affect the common mode voltages. Hence, additional circuitry is needed to control the output common mode voltage and set it to some specified voltage.

The typical common-mode feedback techniques that are used suggest that, sensing the output common-mode level by means of resistors, lowers the differential voltage gain of the circuit considerably. Also, sensing techniques using MOSFETs that operate as source followers or variable resistors suffer from a limited linear range. Switched-capacitor common-mode networks [10] provide an alternative that avoids both of these difficulties.

The main advantages of SC-CMFBs are that they impose no restrictions on the maximum allowable differential input signals, have no additional parasitic poles in the common-mode loop, and are highly linear. However, SC-CMFBs inject nonlinear clock-feedthrough noise into the op amp output nodes and increase the load capacitance that needs to be driven by the op amp. Hence, SC-CMFBs are typically only used in switched-capacitor applications.

Fig. 4.8 shows a switched-capacitor common-mode feedback circuit.

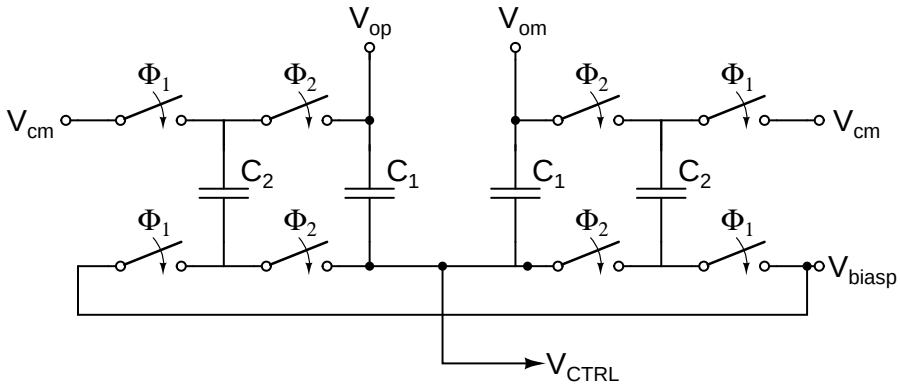

Figure 4.8: First op amp CMFB circuit

The operation of the above circuit consists of two phases.

1. Precharge capacitors to desired value.

2. Sense the difference and adjust the bias accordingly. Part of the tail current source can be controlled by a constant bias voltage. Two capacitors are used so that only a fraction of the charge is shared to adjust the bias voltage.

The following graph shows the reponse of the CMFB circuit to a 1μA current pulse.

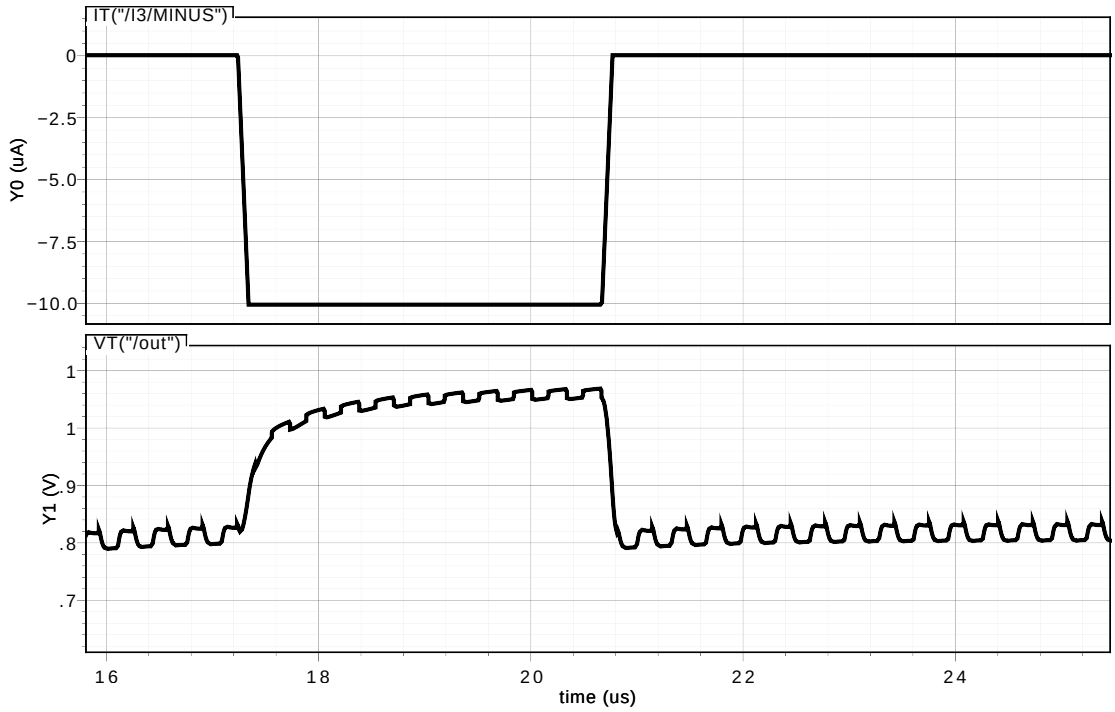

Figure 4.9: CMFB circuit response to current pulse.

The second and the third op amp of the loop filter have an architecture that is identical to the first op amp.

4.4.2 Noise Analysis

At low frequencies the major source of noise is the flicker noise or 1/f noise of the MOS transistors. Only the first op amp in the loop filter will contribute to noise. The noise contribution of the first op amp transistors is tabulated below.

Transistor	**1/f Noise (f_n)**	**Thermal Noise (i_d)**	**f_n at o/p**	**i_d at o/p**
M_2	$V_{n2}^2 G_2^2 R_1^2$	$I_{n2}^2 R_1^2$	23.09%	16.44%
M_4	$V_{n4}^2 G_4^2 R_1^2$	$I_{n4}^2 R_1^2$	1.82%	8.45%

Table 4.1: Transistor Noise Contributions

The symbols used in the above table are explained below:

G_2 = Transconductance of M_2

R_1 = Output impedance of the first stage

G_4 = Transconductance of M_2

V_{n2} = Flicker noise at the input of M_2

V_{n4} = Flicker noise at the input of M_3

I_{n2} = Thermal noise current of M_2

I_{n4} = Thermal noise current of M_4

The total noise at the output of the amp is sum of the above:

$$v_{n,out}^2 = 2(V_{n2}^2 G_2^2 R_1^2 + I_{n2}^2 R_1^2 + V_{n4}^2 G_4^2 R_1^2 + I_{n4}^2 R_1^2) \tag{4.21}$$

The gain of the op amp is $Gain = (G_2 + G_4)R1$. Hence, the input referred noise of the op amp is given by:

$$v_{n,i/p}^2 = \frac{v_{n,out}^2}{Gain} \tag{4.22}$$

The total noise power at the input of the op amp integrated over 10 Hz to 24 kHz is $3.28 * 10^{-12}\, V^2$.

The target specification for this modulator is 98 dB. The noise transfer function of this modulator is selected so as to achieve 106 dB signal-to-quantization noise ratio at least. Therefore modulator can be designed to have a 98 dB signal-to-thermal noise ratio.

As maximum amplitude of differential input signal to modulator is 1.3 V, signal

power of the modulator is

$$SignalPower_{input,diff} = \frac{1.3^2}{2} \tag{4.23}$$

While the in-band noise power will be

$$NoisePower_{inband,diff} = \frac{4kT}{C * OSR} + v_{n,i/p}^2 \tag{4.24}$$

Therefore, to achieve 98 dB signal-to-thermal noise ratio, value of sampling capacitor evaluates to 1 pF.

4.5 Summing Amplifier

The summing op amp has a huge capacitive load due to the 4-bit flash ADC. Hence, the summing op amp has to satisfy very tight specifications on the UGF (to reduce delay), and the output swing. The bandwidth of the summing amplifier has to be greater than f_s to ensure that the pulse response of the summing amplifier settles within one clock period.

The summing op amp is a two-stage amplifier as the output signal swing is high, and single-stage will not be able to meet the requirements. The first stage is class A while second is a class AB stage. Fig. 4.10 shows the schematic of the summing op amp.

First stage of this amplifier is a conventional differential amplifier loaded with current mirror. Both NMOS input and PMOS input differential amplifier drive the second stage of this op amp, which is a push pull amplifier. First stage works in class A fashion while second stage works in class AB fashion and thus optimize the current consumption. Output of first stage goes to both PMOS and NMOS of second stage which helps in increasing the signal power for the same noise power

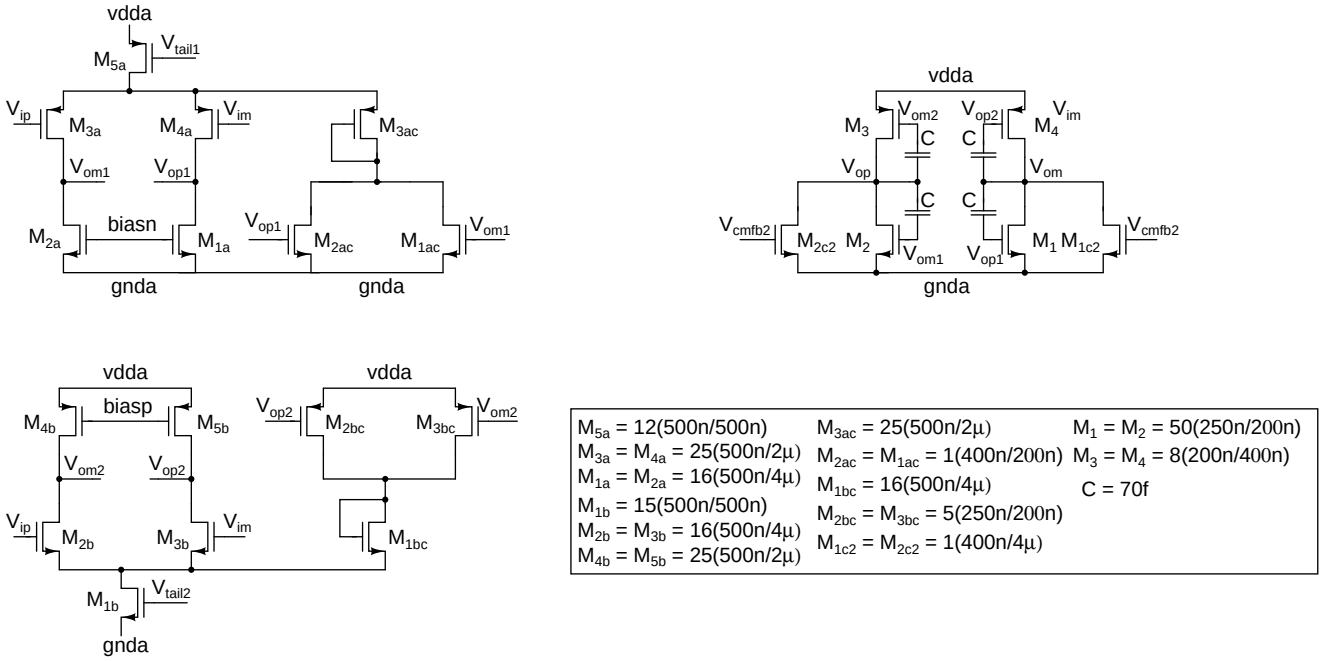

Figure 4.10: Summing Amplifier

and thus increases the power efficiency. Miller compensation has been used here.

4.5.1 CMFB Circuits

CMFB circuit of first stage is based on shared current sensing method used in [11], where bias current of CMFB stage is shared with bias current of differential amplifier stage in negative feedback fashion, which helps in bringing back common mode of first stage to its desired potential.

The first stage CMFB loop [11] consists of the transistors $M_{1ac}, M_{2ac}, M_{3ac}, M_{3,4a}$. If the common-mode level of v_{om1} and v_{op1} increases, the currents in M_{1ac} and M_{2ac} will increase, which will increase the current in M_{3ac}. Since the total tail current is constant, this will result in a decrease in the currents in $M_{3,4a}$ thus bringing down the common-mode output level of the first stage.

A unique feature of this CMFB circuit is that it has also been used to bias the second stage of the amplifier.

The response of the CMFB circuit to a current pulse is as follows:

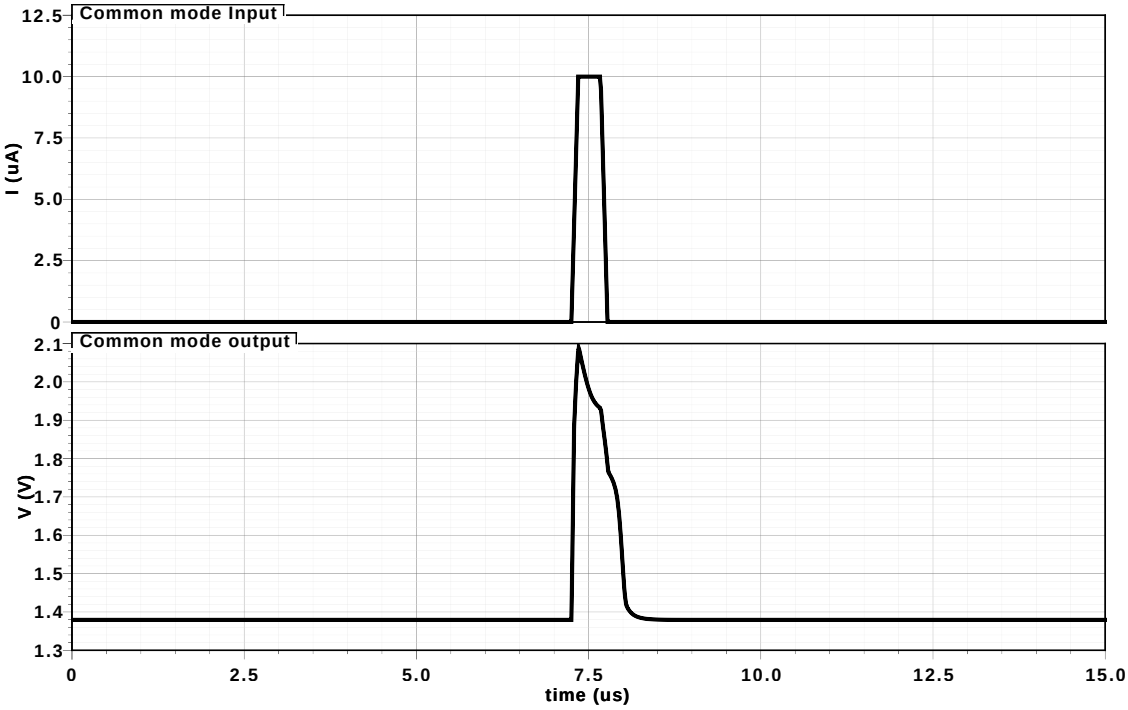

Figure 4.11: CMFB circuit response to current pulse.

CMFB circuit of second stage is based on switched capacitor CMFB circuit as presented in [10].

CHAPTER 5

Flash ADC and Feedback DAC

This chapter gives a brief overview of the Flash ADC and the Feedback DAC used in the modulator.

5.1 Flash ADC

The Flash ADC has been re-used from a previous CTDSM design [12]. A few major points of the ADC are discussed below. More detailed explanations can be obtained from [12].

5.1.1 Architecture

Sigma delta modulator is based on a feedback loop where ADC and DAC have to perform their operation within a clock cycle. It requires the internal ADC to be fast. Flash ADCs are the fastest ADC as it trades hardware size for speed. In case of sigma delta modulator, internal ADC need not have high resolution and a coarse ADC can be used. Therefore, Flash ADC becomes the ADC of choice for implementing the internal quantizer. Up to 4-bit flash converters are commonly used in quantizers. Fig. 5.1 shows the basic architecture of a 4-bit differential Flash ADC.

The differential input signal is fed to $2^N - 1$ comparators in parallel (in this case N = 4). Each comparator is also connected to a different node of two resistor strings. The two resistive ladders provide the differential reference voltage for the comparators. Whenever the differential input voltage to a comparator exceeds its

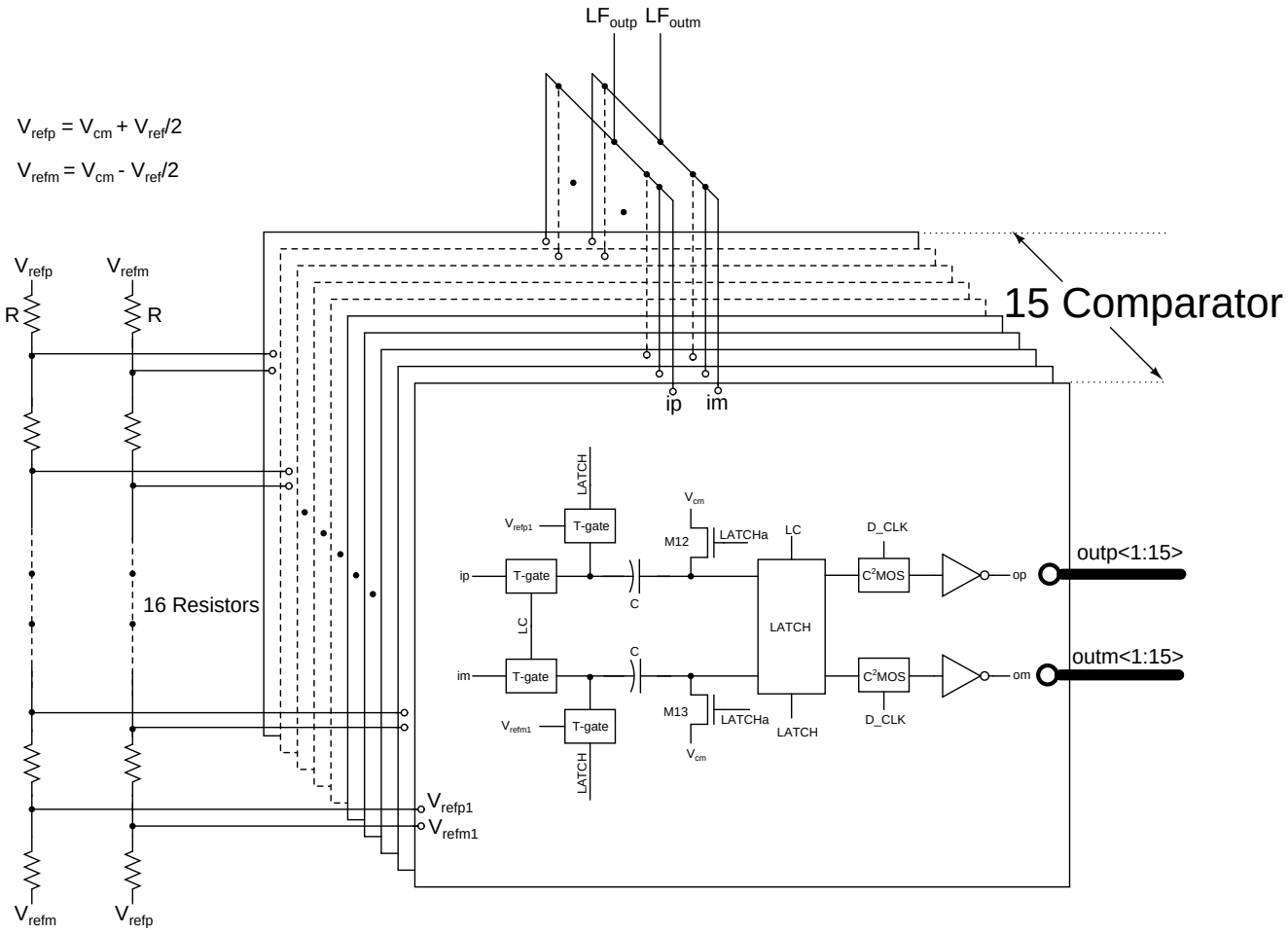

Figure 5.1: 4-bit Flash ADC

differential reference voltage, the output of the comparator goes high. Otherwise the output goes low. The Flash ADC gives a thermometer code at its output.

The basic building blocks of the 4-bit flash are:

1. Resistive ladder
2. Latch
3. Comparator

5.1.2 Resistive Ladder

The resistive ladder is a string of sixteen 100 k resistors that generates the differential reference voltage for the comparators. Larger resistors in the ladder minimize the power consumed by it. For one of the resistive ladders the top and bottom voltages are 1.65 V and 0.15 V respectively. For the other ladder it is vice-versa. The voltage difference between two successive nodes of the resistive ladder is 93.75 mV. The LSB voltage of the flash ADC is twice this voltage and equals 187.5 mV. The center node of the two resistive ladders are at $V_{cm} = 0.9$ V.

5.1.3 Latch

The latch consists of two back-to-back inverters as shown in Fig. 5.2 [12].

The latch operation has three phases. These phases are:

1. Track
2. Regeneration
3. Reset

In the track phase, ϕ_1, the parasitic capacitance at the inputs of the latch get charged to the differential input voltage (ip-im). Regenerative section of latch is OFF in this phase as back-to-back inverters are clocked by regenerative phase. Since no path exists between V_{ddd} and gnda the latch burns zero static power in

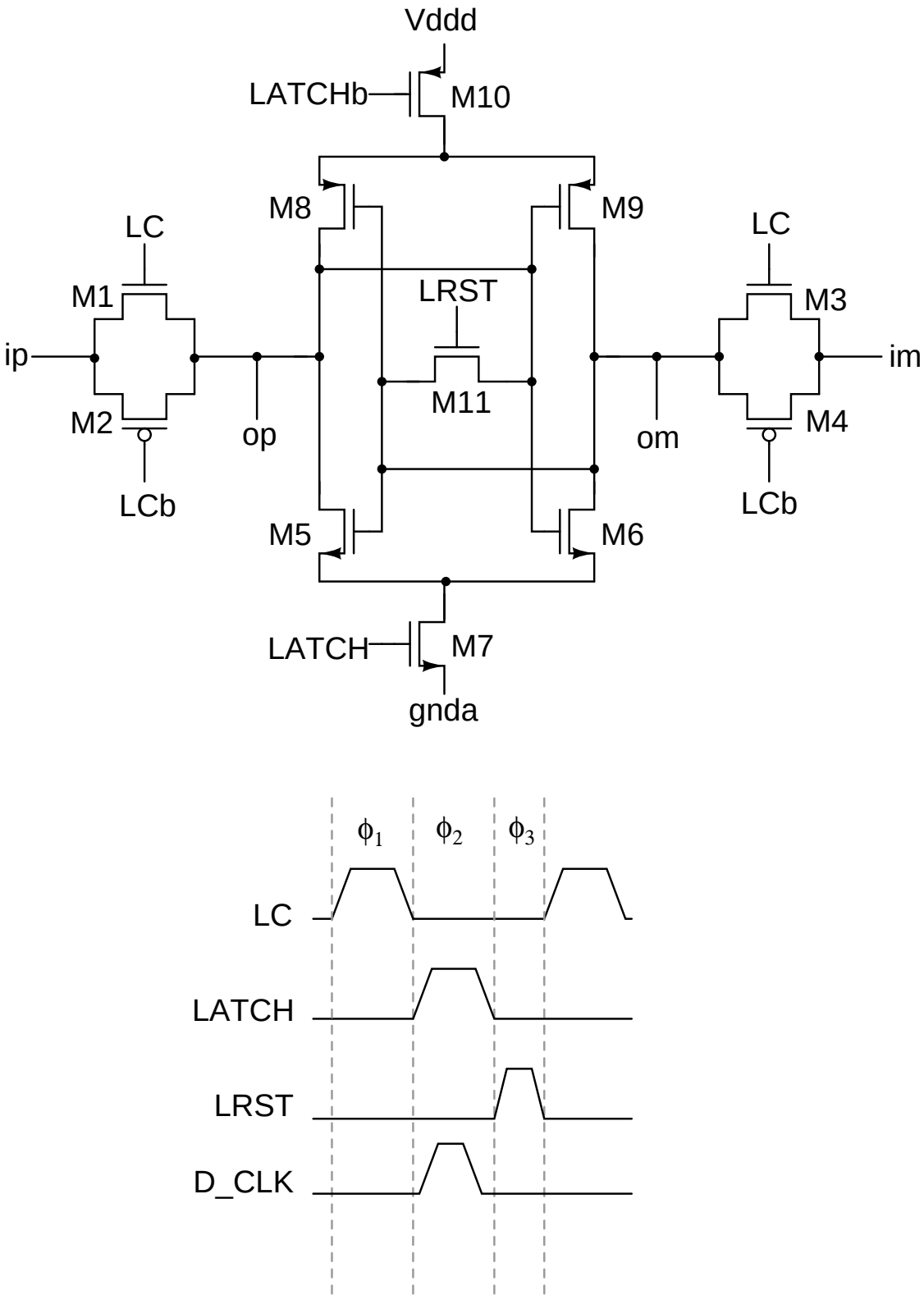

Figure 5.2: Regenerative Latch

this phase.

In the regeneration phase, ϕ_2, the latch is a simplified circuit consisting of two back-to-back inverters. Due to its positive feedback action, it regenerates the differential input sampled in tracking phase to either V_{ddd} or gnda depending upon the sign of the sampled value.

In the reset phase, ϕ_3, the outputs of the latch are re-initialized to the common-mode voltage of the latch. It is important to ensure that no memory is transferred from one decision cycle to the next. If the latch toggles in one direction it might have a tendency to stay in that direction. This is referred to as *hysteresis*. In order to eliminate it, the latch outputs are reset before entering the track mode.

5.1.4 Comparator

The latch discussed in the previous section is the basic building block of the comparator shown below in Fig. 5.3

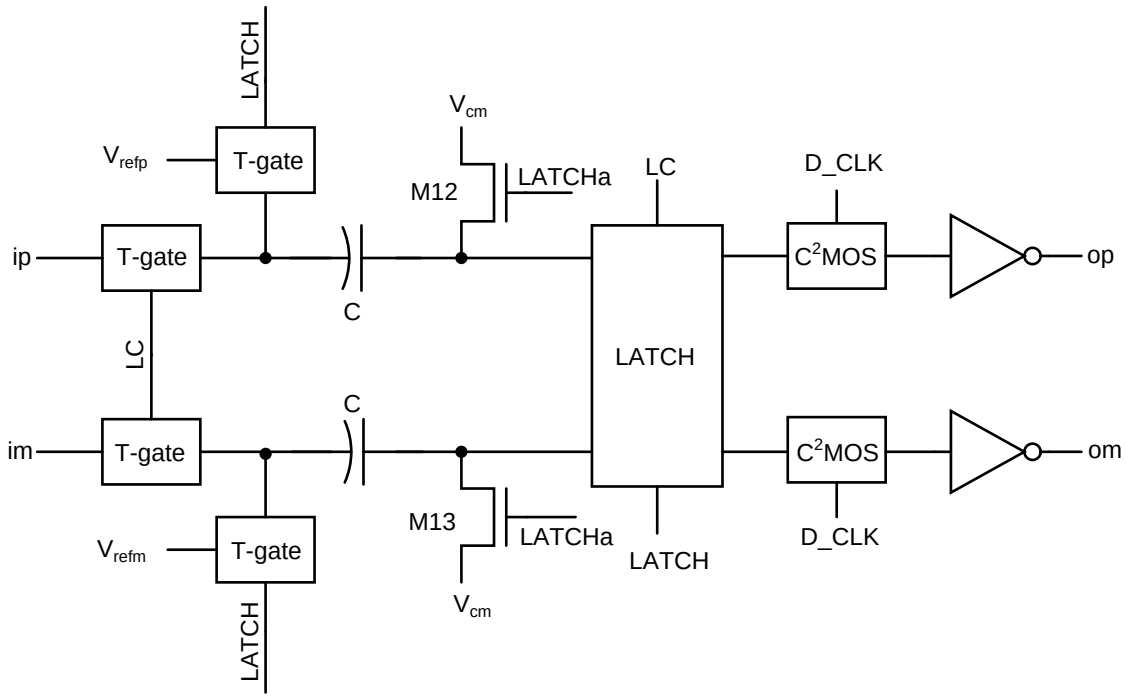

Figure 5.3: Comparator

The C^2MOS latches the output of the latch after the regeneration is complete. The clock to the C^2MOS, D_CLK, should go high only after the output of the latch has reached one of the two logic levels.

The comparator is connected to the resistive ladder only during ϕ_2. In this phase the comparator draws a small amount of transient current from the ladder to charge the 50 fF capacitor. In order to minimize the variation in the ladder node voltages, each ladder node is connected to ground by a 1 pF capacitor.

5.2 Feedback DAC

This section describes the architecture of the multi-bit DAC along with a brief description of dynamic element matching (DEM) technique.

5.2.1 DAC Architecture

The most common architecture for the internal DAC employs $2^N - 1$ parallel unit elements, where N is the number of bits of the internal quantizer. In such a DAC, the k^{th} output level is generated by turning on k approximately equal valued elements and summing up their charges or currents. Fig. 5.4 shows the schematic of the 4-bit switched-capacitor (SC) DAC implemented in the design.

The DAC implemented in the design is a differential SC-DAC. When the input control bits to any DAC element in the section is 1 it dumps a proportional amount of charge on the capacitors.

5.2.2 Dynamic Element Matching (DEM)

DEM aims to modulate mismatch errors away from the signal bandwidth in order to remove them by post filtering [13]. The DAC elements are selected in such a way

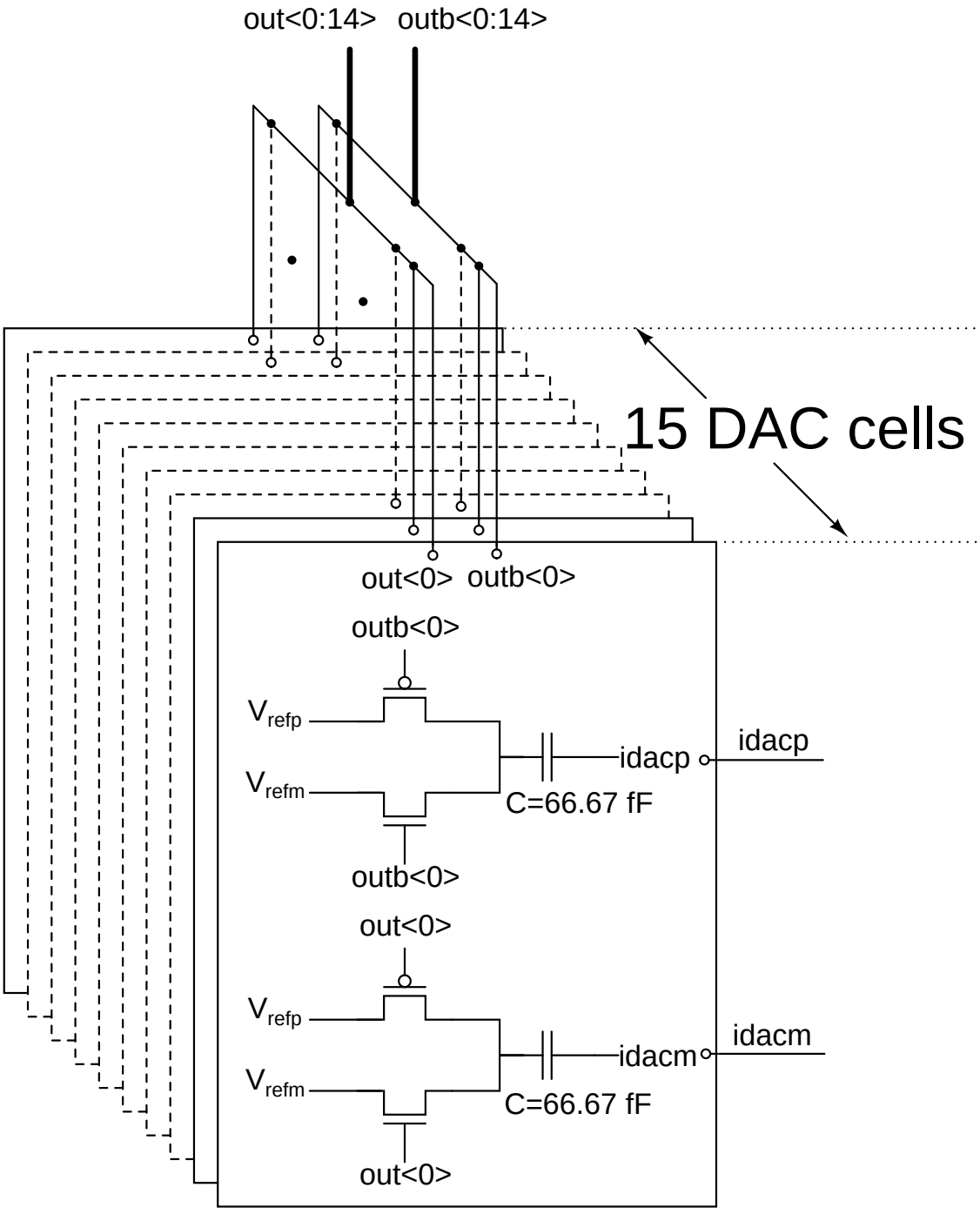

Figure 5.4: DAC schematic

that the DAC errors sum to zero over multiple sample instances. The static DAC errors are converted into a wide-band noise signal. By choosing the DAC elements at random the DAC error at the output averages out to zero quickly thereby moving the distortion due to DAC component mismatch to higher frequencies. Subsequent filtering leaves the signal band free of distortion.

There are many choices for the DEM. Data weighted averaging (DWA) which provides first order shaping using a simple element rotator algorithm is a very commonly used technique. DWA has been used here to mitigate distortion due to mismatch [5]. The DWA technique uses all the DAC elements at the maximum possible rate. At the same time it ensures that each DAC element is used the same number of times. This is done by sequentially selecting the DAC elements, beginning with the next available unused element. The DEM circuit has been re-used. More details of the DEM, DWA algorithm and its implementation can be found at [12]

CHAPTER 6

Simulation results

6.1 Simulation results

The simulation of a DT $\Delta\Sigma$ modulator is time consuming. In order to ease this during the design and simulation phase, each of the building blocks had an associated Verilog-A view or ideal-view wherein the functionality of the block was realized using ideal active elements. Thus during the design and simulation phase only a few blocks are run at the transistor level. This greatly reduces the design iteration time. The results of the various simulations run on the design is tabulated in Table 6.1. The input signal to the modulator is a $2.6\,V_{pp,d}$ sinusoid at a frequency of 6 KHz. The following notations are used in the table:

1. Ideal - Ideal view
2. Verilog - Verilog-A view
3. SS - Schematic view of Single stage op amp
4. TS - Schematic view of Two stage op amp
5. RSS - Schematic view of Ramalingam's op amp modified to single stage op amp
6. Sch - Schematic view

The voltage supplies, bias currents and reference voltages are all ideal.

Table 6.1 gives the performance numbers for 97 μA of current consumption by loop filter for different topologies. SNDR denotes signal-to-noise ratio where the noise includes third harmonic.

First Int	Second Int	Third Int	Summing Amp	Flash ADC	DAC	SQNR (dB)	SNDR (dB)
Ideal	Ideal	Ideal	Ideal	Verilog	Verilog	115.1	109.3
Ideal	Ideal	Ideal	Ideal	Sch	Verilog	114.1	108.6
Ideal	Ideal	Ideal	Ideal	Sch	Sch	113.2	108.25
SS	SS	SS	TS	Verilog	Verilog	113.1	109.7
TS	TS	TS	TS	Verilog	Verilog	95	94
RSS	RSS	RSS	TS	Verilog	Verilog	98.8	98.3
SS	SS	SS	TS	Sch	Sch	109.3	106

Table 6.1: Simulation Results

The output PSD of the modulator for best performance,is shown below:

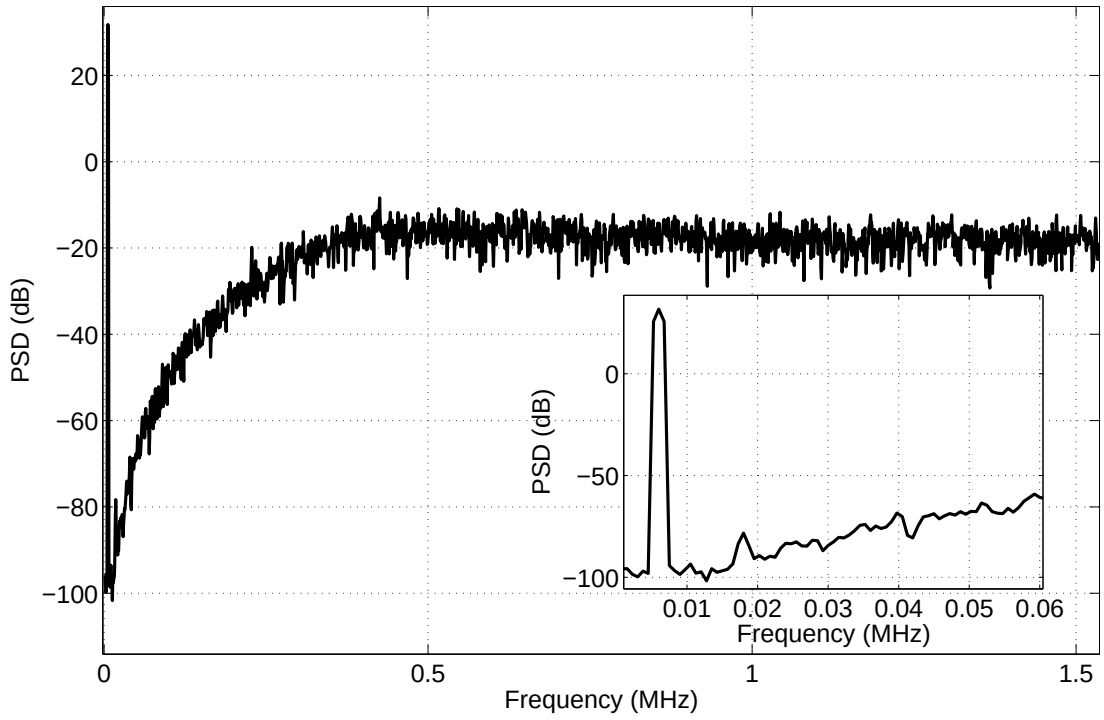

Figure 6.1: PSD of Modulator output

6.2 Power Dissipation of different blocks of the Modulator

The following table shows the power consumed by each of the building blocks of the modulator in the best performance and lowest power consumption case:

Building Block	**Power (Vdd=1.8 V) μA**
First Integrator	21.5
Second Integrator	21.5
Third Integrator	10.7
Summing Amplifier	43.4
ADC + DAC + DEM	24.8
Total	**121.9**

Table 6.2: Power dissipation of different blocks

6.3 Final Results

The best performance toplogy has a power number of 122 μA and a corresponding SQNR of 109.3 dB and SNDR of 106 dB.

Table 6.3 below shows the achieved ADC specifications:

Specification	**Value**
Resolution	16 bits
Best case SQNR	109.3 dB
Sampling Rate	3.072 MHz
Signal Bandwidth	24 KHz
Best case Power Dissipation	122μA

Table 6.3: Achieved ADC specifications from schematic-based simulation

The power number of the [3] of the CTDSM design (from which this design was derived) was 87 μA for similar performance.

CHAPTER 7

Conclusions and Future Work

7.1 Conclusions

In this project, an existing design of a 3^{rd} order CT $\Delta\Sigma$ modulator was taken and converted into an equivalent DT $\Delta\Sigma$ modulator having same specifications.

The block which largely differed in power consumption from the CTDSM is the loop filter. Two types of architecture for the op amps in the loop filter have been explored. A power versus performance analysis is done for both these architectures.

Single-stage op amps have been used to get better phase margin for settling and also to reduce power consumption. Moreover, the loop filter op amps are operated in the sub-threshold region for further minimizing the power consumed by the modulator.

The best performance has a power number of 122μA for a corresponding SQNR of 109.3 dB and SNDR of 106 dB.

7.2 Future Work

Layout for the modulator needs to be done. Any further scope of optimization in power consumption may only be done after investigating the extracted results.

REFERENCES

[1] H. Inose and Y. Yasuda, "A unity bit coding method by negative feedback," *Proceedings of the IEEE*, vol. 51, no. 11, pp. 1524–1535, 1963.

[2] J. Cherry and W. Snelgrove, "Loop delay and jitter in continuous-time delta sigma modulators," in *Circuits and Systems, 1998. ISCAS '98. Proceedings of the 1998 IEEE International Symposium on*, vol. 1, 1998, pp. 596–599 vol.1.

[3] R. Schreier and G. C. Temes, "Understanding delta-sigma data converters," vol. 74, 2005.

[4] L. Carley, "A noise-shaping coder topology for 15+ bit converters," *IEEE Journal of Solid-State Circuits,*, vol. 24, no. 2, pp. 267–273, 1989.

[5] R. Baird and T. Fiez, "Linearity enhancement of multibit Δ Σ A/D and D/A converters using data weighted averaging," *IEEE Transactions on Circuits and Systems II,*, vol. 42, no. 12, pp. 753–762, 1995.

[6] M. W. Hauser and R. W. Brodersen, "Circuit and technology considerations for MOS delta-sigma A/D converters," in *IEEE Proc. ISCAS*, vol. 86, 1986, pp. 1310–1315.

[7] B. Boser and B. Wooley, "The design of sigma-delta modulation analog-to-digital converters," *IEEE Journal of Solid-State Circuits,*, vol. 23, no. 6, pp. 1298–1308, 1988.

[8] R. Gregorian and G. C. Temes, "Analog MOS integrated circuits for signal processing," *New York, Wiley-Interscience, 1986, 614 p.*, vol. 1, 1986.

[9] J. Silva, U. Moon, J. Steensgaard, and G. Temes, "Wideband low-distortion

delta-sigma ADC topology," *Electronics Letters*, vol. 37, no. 12, pp. 737–738, 2001.

[10] O. Choksi and L. R. Carley, "Analysis of switched-capacitor common-mode feedback circuit," *IEEE Transactions on Circuits and Systems II: Analog and digital signal processing,*, vol. 50, no. 12, pp. 906–917, 2003.

[11] V. Singh, N. Krishnapura, S. Pavan, B. Vigraham, N. Nigania, and D. Behera, "A 16 MHz BW 75 dB DR CT Sigma Delta ADC compensated for more than one cycle excess loop delay," pp. 1–4, 2011.

[12] R. P., "Design of 16 bit Continuous time Delta Sigma Modulator for Digital Audio," *Masters Thesis, IIT Madras*, 2006.

[13] B. H. Leung and S. Sutarja, "Multibit Sigma Delta Analog to Digital converter incorporating a novel class of dynamic element matching techniques," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing,*, vol. 39, no. 1, pp. 35–51, 1992.