Testing and Characterization of Head Phone Driver

A THESIS

submitted by

GVSRK PRASAD

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THESIS CERTIFICATE

This is to certify that the thesis titled **Testing and Characterization of a Head Phone Driver**, submitted by **G.V.S.R.K Prasad**,to the Indian Institute of Technology, Madras, for the award of the degree of **Master of Technology** , is a bona fide record of the work done by him under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

Dr. Nagendra Krishnapura

Advisor,

Assistant Professor,

Dept. of Electrical Engineering,

IIT-Madras, 600 036

Place: Chennai

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Finally, I dedicate this thesis to my family members and friends for their support and encouragement through all these years.This work would not have been possible without their love and understanding.

ABSTRACT

This project involves the testing and validating the Head Phone Driver chip. This chip is designed to work in audio frequencies.

The headphone driver utilizes a simple ac coupling to achieve class-AB operation in the audio bandwidth of 20 Hz - 24 kHz.The driver is driven from a dual supply of 1.8 V and -1.8 V to avoid a large dc blocking capacitor. Further-more, the dual supply driver can support higher output voltage swing compared to the single supply driver, thus delivering higher output power. The -1.8 V is derived from the 1.8 V using a negative voltage converter.

Head phone driver is charecterised by changing input signal amplitude. Distortion becomes dominant at higher input signal amplitudes. By increasing feed forward current source performance(SNDR,SDR) is improving. Head phone driver is also charecterised by changing bias currents, Resistor non-linearity with mismatch. With Negative voltage converter, Performance was decreasing so much because of series trace+bondwire inductance with the capacitors of negative voltage converter. Exact reason why distortion becomes dominant at higher amplitudes need to be sorted out.

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ABBREVIATIONS

SNDR	Signal to Noise and Distortion Ratio
SDR	Signal to Distortion Ratio
SNR	Signal to Noise Ratio
THD	Total Harmonic Distortion
THD+N	Total Harmonic Distortion and Noise

CHAPTER 1

Headphone driver

1.1 Headphone driver [3]

A headphone driver is used to drive a load of 16 Ω. The motivation is to drive the load by consuming minimum quiescent power possible. The class-A amplifier requires the output bias current equal to the maximum load current (100 mA in this case). This degrades the efficiency of the power amplifier. In class-B amplifier, the output bias current is zero. Although its efficiency is high compared to class-A amplifier, it gives significant distortion. In class-AB amplifier, a minimum output bias current is kept to improve the distortion. So, we use a class-AB type of amplifier to minimize the power dissipation for a given distortion.

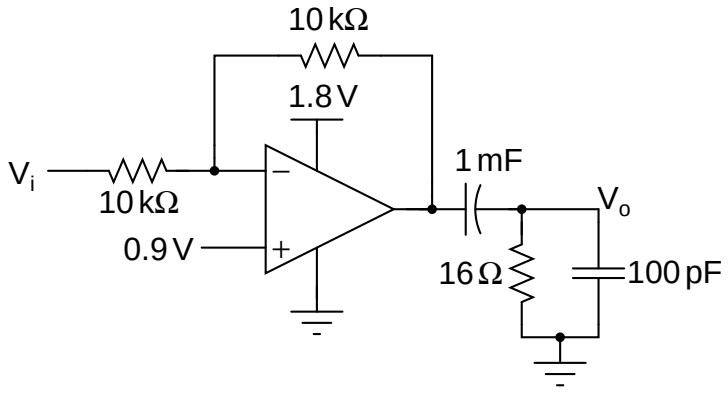


Figure 1.1: Driver with 0.9 V common mode.[3]

1.2 Ground-centered driver[3]

The conventional way of powering the op-amp from 1.8 V and 0 V requires the output common mode to be 0.9 V. Since the load is very heavy, a quiescent current of $0.9/16 = 56.25$ mA should be supplied by the op-amp. To avoid this large

DC current, we have to connect a very large capacitor in series with the load. The value of this capacitor should be $> 500\,\mu$F for $<20\,$Hz cut-off. As already mentioned in the introduction, such a large capacitor consumes large area, and is not suitable for portable audio applications. During start-up or shutdown, this capacitor has to be charged or discharged which causes an audible pop.

If the output bias is kept at 0 V, the DC blocking capacitor is not required, thus eliminating the disadvantages associated with it. To achieve this, a ground-centered amplifier is used. The schematic is shown in Fig. 1.2. It is an op-amp used in an unity gain inverting configuration. The values of the resistors are chosen based on noise constraints. The resistors contribute 32%, while the opamp contributes 68% to the total input referred noise. The simulated input referred noise in the typical case is $5\,\mu V_{rms}$. A charge pump based negative voltage converter is used to provide negative rail for the op-amp. Table 1.1 shows the required driver specifications.

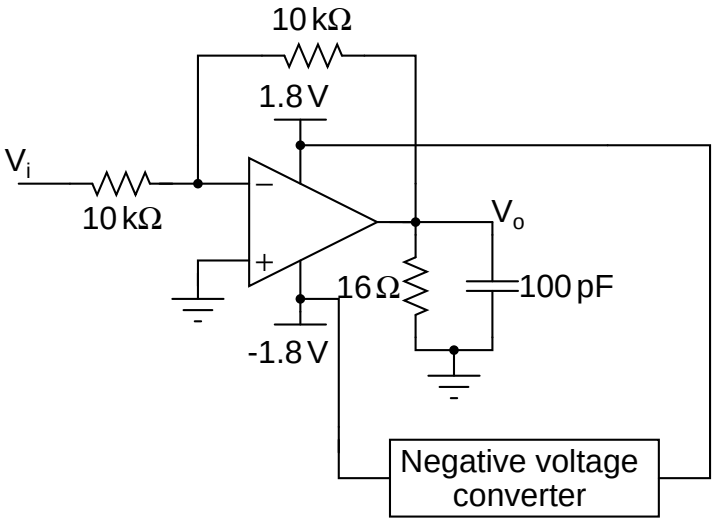


Figure 1.2: Ground-centered driver schematic.[3]

1.3 Op-amp macromodel[3]

A three-stage opamp is used for driving the 16Ω load. To compensate the op-amp, a combination of feedforward and Miller compensation is used. Fig.1.3 shows the

Table 1.1: Driver specifications.

Load	$16\,\Omega \parallel 100\,\text{pF}$
Maximum output power	80 mW
Bandwidth	20 Hz-24 kHz
THD	<-90 dB
Input noise	$5\,\mu\text{V}_{\text{rms}}$
Power	1 mW
Technology	$0.18\,\mu$m CMOS

macromodel of the opamp.

The transfer function is given by

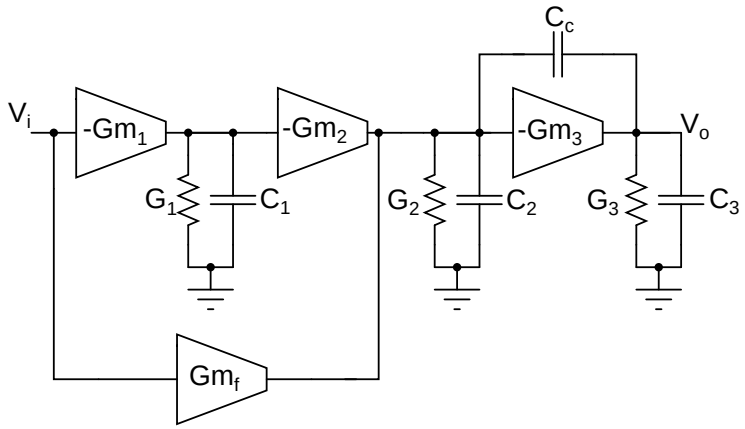


Figure 1.3: Opamp macromodel.[3]

$$\frac{V_o}{V_i} = \frac{(Gm_1Gm_2 + Gm_fG_1 + sC_1Gm_f)(sC_c - Gm_3)}{(G_1 + sC_1)((G_2 + sC_2 + sC_c)(G_3 + sC_3 + sC_c) - sC_c(sC_c - Gm_3))} \tag{1.1}$$

The approximate poles are

$$p_1 = \frac{-G_2G_3}{G_2(C_3 + C_c) + G_3(C_2 + C_c) + Gm_3C_c} \tag{1.2}$$

$$p_2 = \frac{-(G_2(C_3 + C_c) + G_3(C_2 + C_c) + Gm_3C_c)}{C_2C_3 + C_c(C_2 + C_3)} \tag{1.3}$$

$$p_3 = \frac{-G_1}{C_1} \tag{1.4}$$

Zeros of the transfer function are

$$z_1 = \frac{Gm_3}{C_c} \tag{1.5}$$

$$z_2 = \frac{-(Gm_1 Gm_2 + Gm_f G_1)}{Gm_f C_1} \tag{1.6}$$

For compensating the first two stages, the zero (z_2) introduced by the feedforward path should be much less than the unity gain frequency of the first two stages standalone.

$$|z_2| << \sqrt{\frac{Gm_1 Gm_2}{C_1 C_2}} \tag{1.7}$$

For $Gm_3/G_3 >> 1$, the unity gain frequency is approximately

$$w_u = \frac{Gm_f}{C_c} \tag{1.8}$$

1.4 Op-amp design[3]

As mentioned earlier, the output common mode is at 0 V. This makes the input common mode of the op-amp also 0 V. So we choose a pMOS transistor input stage. Also to have a lower flicker noise, a pMOS input stage is preferable. To get a very high DC gain, we use a folded cascode structure. Fig.1.4 shows the first stage op-amp schematic along with the bias section.

Transistors M1-M12 form the folded cascode first stage of the opamp. Transistors M5 and M6 have large lengths to minimize their flicker noise. The current in each input transistor is 25 μA to meet the noise specification. The DC gain of the first stage is 82 dB. Thus most of the DC gain is obtained from the first stage itself. The first stage is operated from the positive rail and 0 V instead from positive and negative rail. Since the negative rail is obtained from a charge-pump based negative voltage converter, there will be significant signal dependent noise voltage on it. Also, since it is a single-ended output stage, any noise on the negative rail will be completely reflected at the output of the first stage. This degrades the distortion performance of the driver.

Fig.1.5 shows the circuit diagram of the second and the third stage of the op-amp. The second stage (M32-M35) is a common source stage with a cascode for the

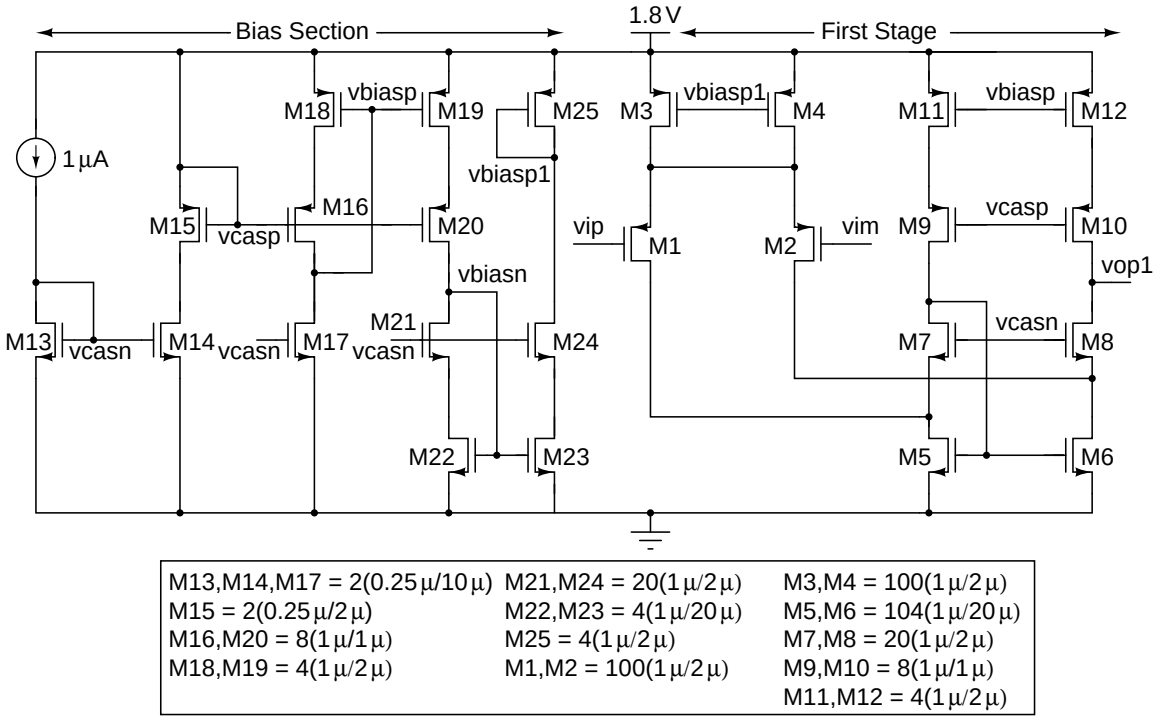
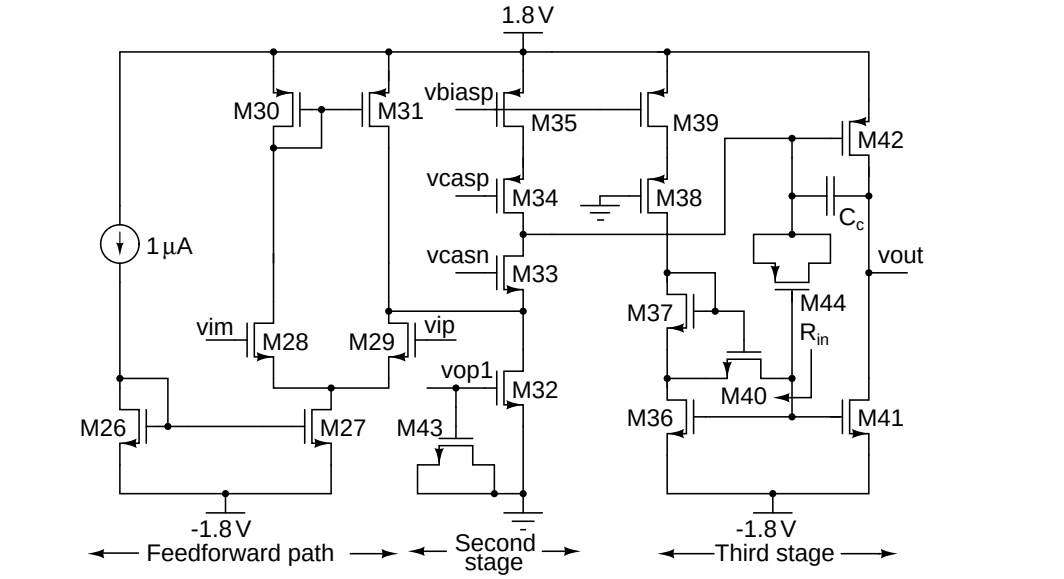


Figure 1.4: First stage op-amp schematic.[3]

main and the bias transistor. It gives a gain of 40 dB. Transistor M43 is used as a MOS capacitor of value 10 pF. This capacitance is C_1 in the op-amp's macro-model shown in Fig.1.3. So having high value for C_1, the zero z_2 is moved to lower frequencies giving higher phase margin without increasing the feedforward transconductance Gm_f[1]. Transistors M27-M31 form the feedforward stage. A five transistor op-amp is used for giving correct gain polarity from the input of the first stage to the second stage's output. This feedforward op-amp's output is not connected directly to the second stage output to avoid its loading. Also the feedforward op-amp is operated from the positive and the negative rail, as the input common mode is at 0 V.

The third stage (M41-M42) forms the class-AB driving stage. A very simple biasing scheme formed by the transistors M36-M40 is used. To have a output common mode of 0 V, it is operated from the dual supply. Signal from the second stage output is directly fed to the pMOS (M42) input, and is AC coupled to the nMOS (M41) input. Transistor M44 acts as a coupling capacitor of value 50 pF, while the transistor M40 is biased in the sub-threshold region to give a high resis-



M26 = 2(0.5 µ/2 µ)	M32 = 20(1 µ/20 µ)	M36 = 2(26.67 µ/0.34 µ)	M41 = 150(26.67 µ/0.34 µ)
M27 = 140(0.5 µ/2 µ)	M33 = 100(1 µ/2 µ)	M37 = 100(1 µ/0.34 µ)	M42 = 400(30 µ/0.34 µ)
M28,M29 = 200(2 µ/2 µ)	M34 = 40(1 µ/1 µ)	M38 = 8(1 µ/0.18 µ)	M44 = 5(72 µ/25 µ)
M30,M31 = 2(1.75 µ/2 µ)	M35 = 20(1 µ/2 µ)	M39 = 4(1 µ/2 µ)	C_c = 5 pF
	M43 = 60(10 µ/2 µ)	M40 = 2(0.24 µ/20 µ)	

Figure 1.5: Second and third stage op-amp schematic.[3]

tance of 1.3 GΩ. Since the load is very heavy, this stage gain can be improved only by increasing the transconductance of the transistors M41 and M42. Transistors M41 and M42 widths are sized very large to have a transconductance of 4 mS each. The bias current for the output class AB stage is approximately given by

$$I_{out} = I_{M36}\frac{(W/L)_{M41}}{(W/L)_{M36}} \tag{1.9}$$

Since the output common mode is 0 V, there is a significant V_{DS} mismatch between the transistors M36 and M41 (higher V_{DS} for M41). Due to channel-length modulation effect, current mirroring is not accurate, thus increasing the actual output bias current. The value of the output bias current is fixed to 176 μA to have a phase margin of 46^0.

1.5 Simulation results[3]

1.5.1 Frequency and step response

The ground-centered driver is simulated to check its stability. Fig. 1.6 shows the magnitude response of the loop gain. Fig. 1.7 shows the phase response of the loop gain. Table 1.2 shows the op-amp characteristics.

The loop should be stable in no-load condition. Miller capacitor C_c is used to

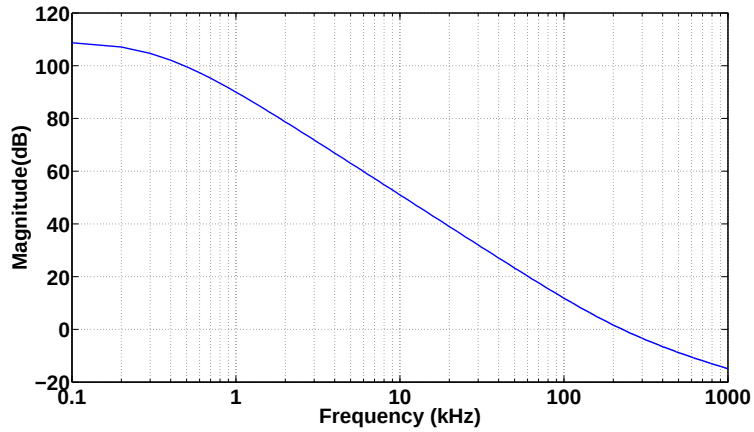


Figure 1.6: Magnitude response.[3]

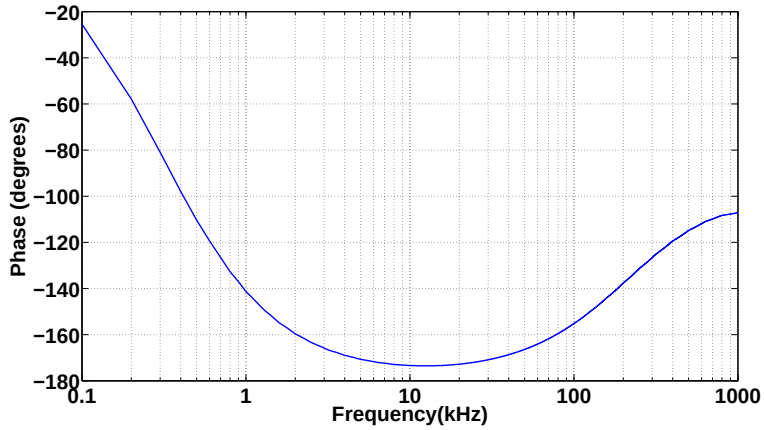


Figure 1.7: Phase response.[3]

stabilize the loop. Its value is chosen to have a phase margin of 41^0 in no-load condition. The loop stability is tested by giving a step input of 10 mV with 0.1 ns rise time to the inverting unity gain op-amp. The output is shown in Fig. 1.8.

Table 1.2: Op-amp characteristics.[3]

DC Gain	108 dB
Unity gain frequency	226 kHz
Phase margin	46^0
Input noise	$5\,\mu V_{rms}$
Quiescent power	1 mW

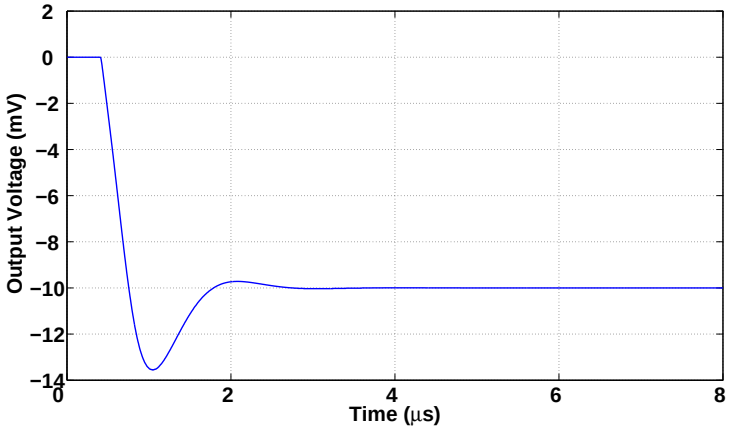


Figure 1.8: Step response.[3]

1.5.2 Transient response[3]

The driver is driven by an ideal dual rail supply of 1.8 V and -1.8 V. It is simulated for an input signal of 1.6 V_p amplitude and 1.25 kHz frequency. For the positive half cycle of the input, the nMOS transistor drives the load, while the pMOS transistor is off. For the negative half cycle of the input, the pMOS transistor drives the load, while the nMOS transistor is off. The output current waveforms are shown in Fig. 1.9.

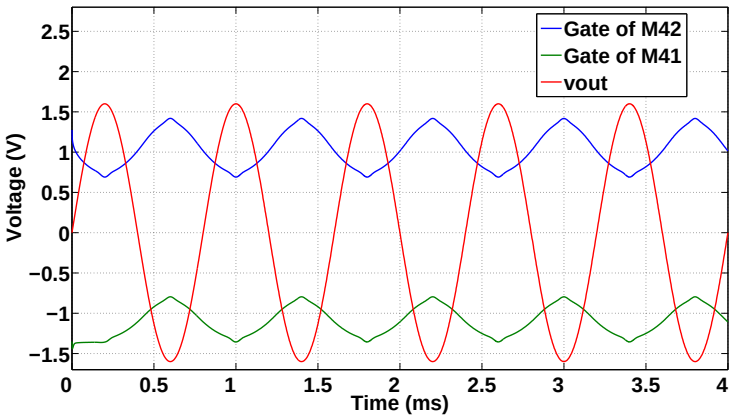


Figure 1.9: Output currents waveform.[3]

CHAPTER 2

Audio driver chip measurements

2.1 Pin Description

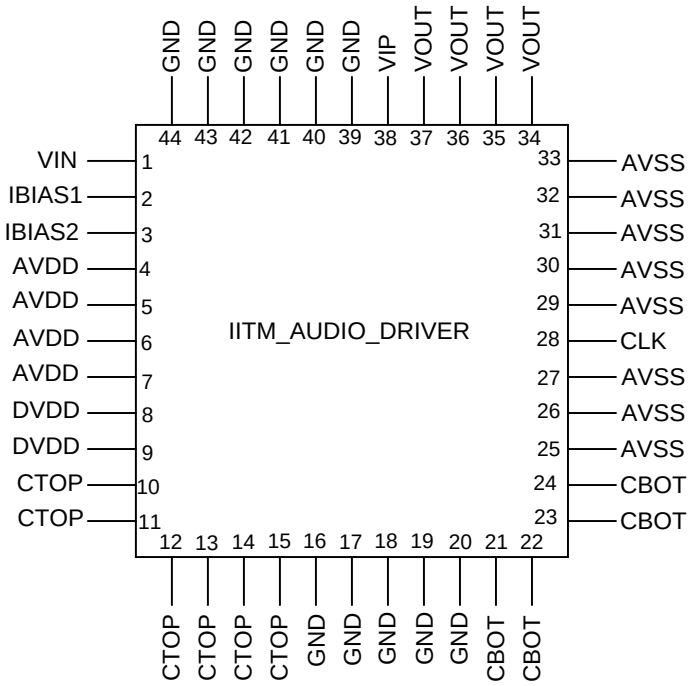


Figure 2.1: Headphone driver chip pinout.

The pin arrangement of the chip is as shown in Fig. A.1.

Table 2.1: Pin details of the headphone driver chip.

Pin No.	Pin name	Pin description
1	VIN	Input of the driver
2	IBIAS1	Bias current for the first stage(1 μA)
3	IBIAS2	Bias current for the third stage(1 μA)
4, 5, 6, 7	AVDD	Positive supply voltage for the driver
8, 9	DVDD	Supply voltage for negative voltage converter
10-15	CTOP	Top pin for external capacitor C1
16-20, 39-44	GND	Common ground pin
21-24	CBOT	Bottom pin for external capacitor C1
25-27, 29-33	AVSS	Negative supply voltage for the driver
28	CLK	Clock input for the negative voltage converter
34-37	VOUT	Output voltage of the driver
38	VIP	Non-inverting input terminal of the driver

2.2 Board Description

To test Head phone driver, a PCB Board was designed. PCB is designed using orcad software.

2.2.1 Power supply

Audio driver chip has two power supplies. Two power supplies are given from two load regulators namely AVDD and AVSS. Positive power supply(AVDD) is regulated through TPS74401 regulator. Two provisions for giving Negative supply is given in the board. One provision is to give Negative supply(AVSS) is regulated through LM337 regulator. Another provision is using on-chip negative voltage converter by providing a clock to the chip. Before passing supply to chip, it is filtered using parallel bank of surface mount capacitors.

2.2.2 Current references

This Audio driver chip requires two current sources. One current source for first stage, second stage and final stage. Another current source for feed forward stage.

2.2.3 Inputs

Analog signal(sine wave) is given from analog generator of audio analyzer. If we use negative supply from load regulator LM337, clock input for chip should be grounded. If we are using on-chip negative voltage converter, clock should be provided using signal generator.

2.2.4 Outputs

Analog output from chip is given to audio analyzer input, which will plot the spectrum of output signal using FFT Spectrum analyzer.

2.2.5 Others

BNC connectors are used to connect input signal to driver, to take output signal from driver and to give clock input to driver.

2.3 Measurement setup

Top level block diagram is as shown in Fig. 2.2.

Audio analyzer is used to measure performance of audio driver. Audio Precision

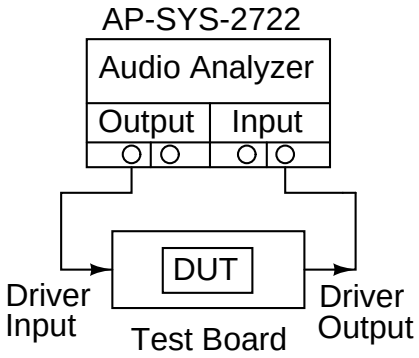


Figure 2.2: Measurement setup.

AP-SYS-2722 audio analyzer is used to give an analog input signal to the Head

phone driver. The filtered output is analyzed using audio analyzer for measuring the performance of the Head phone driver. Test board is as shown in figure. Driver performance is measured using external supply and with the negative voltage converter.

2.4 Testing and simulation results

2.4.1 PMOS in slow corner and NMOS in slow corner

Fig. 2.3 shows test-bench to measure performance. Comparison of simulation and testing results were made for SNR, SDR, SNDR vs Amplitude is as shown in Fig. 2.4. All transistors are in ss corner, Resistors, Capacitors in min corner.

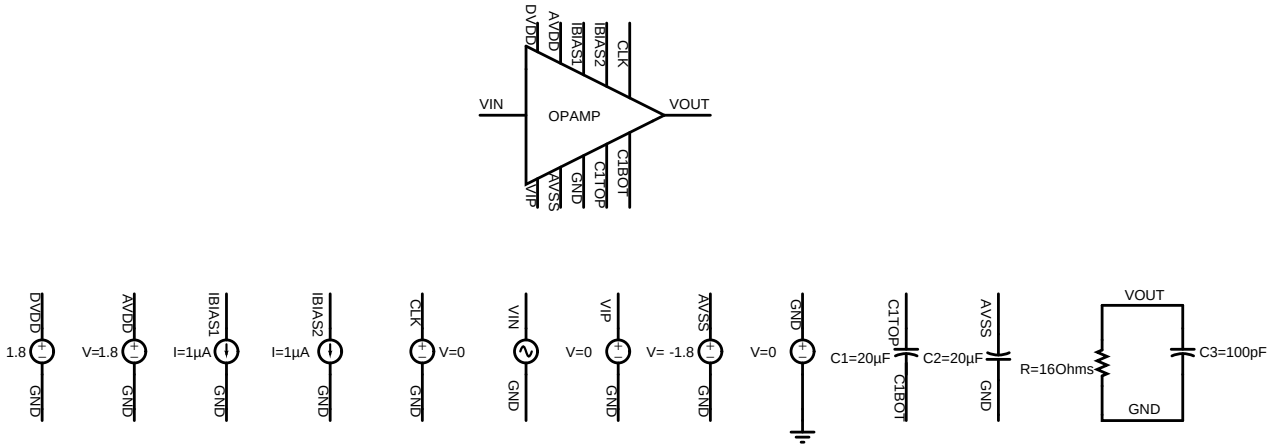


Figure 2.3: Testbench for measuring performance

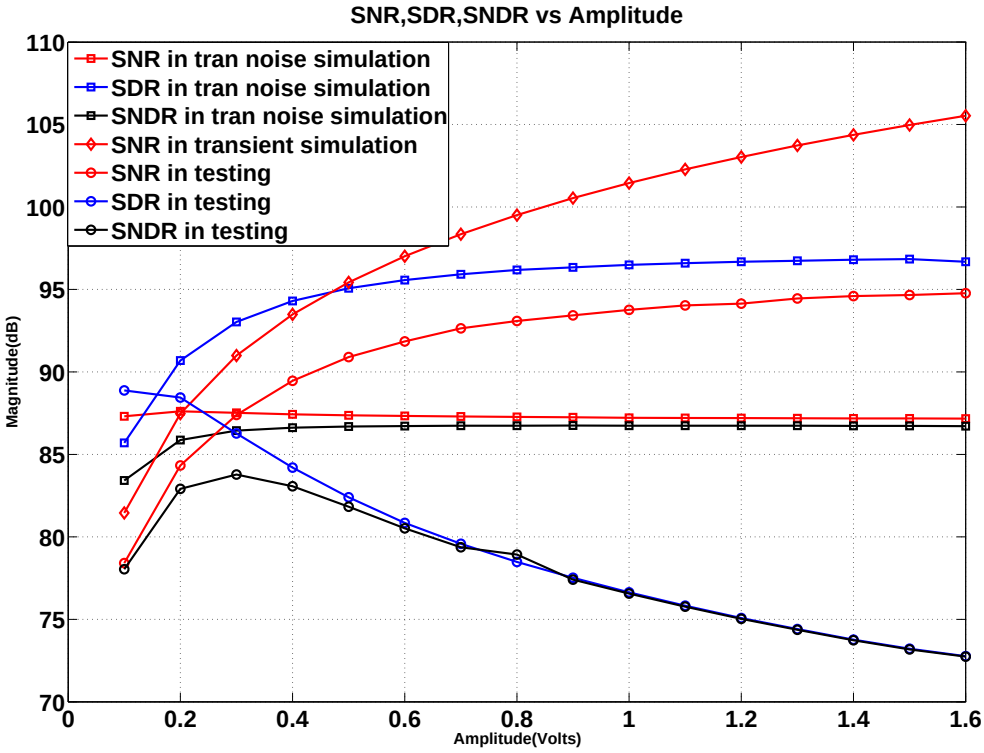


Figure 2.4: SNR,SDR,SNDR vs AMPLITUDE.

2.4.2 Idle channel noise

Idle channel noise is measured by grounding the driver input. In simulation, Idle channel noise is 5.42 μV_{rms}.In testing, Idle channel noise is 8 μV_{rms}.

Fig. 2.5 shows the test bench to measure Idle channel noise.

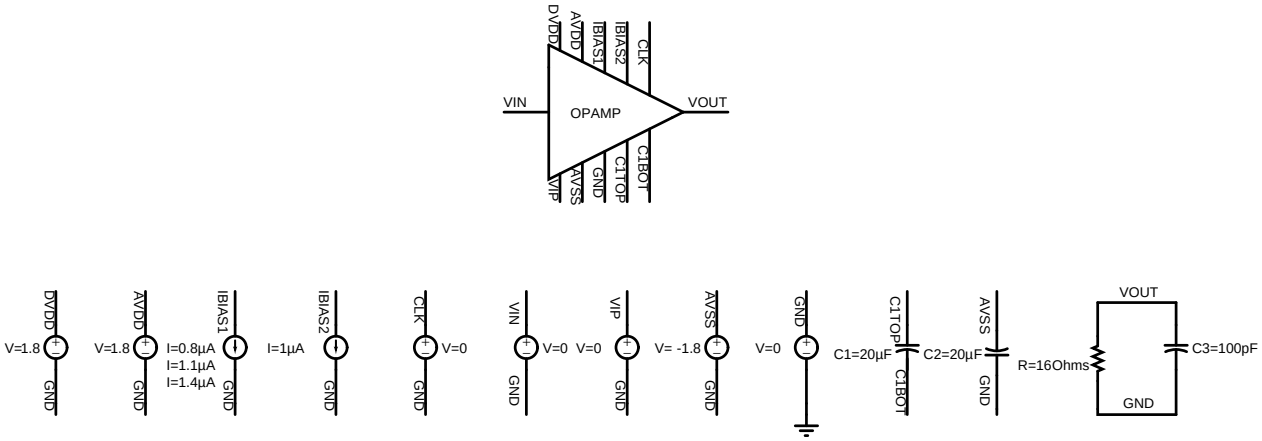


Figure 2.5: Testbench for measuring idle channel noise

2.4.3 Resistor non-linearity

Resistor(rnhr_1000_mm) equation is as shown below.

$R = ((2 * rend/(wr + dw)) + (rs * lr/(wr + dw))) * (1.0 + vcr1 * abs(v(n1, n2)/lr) + vcr2 * pow(abs(v(n1, n2))/lr, 2)) * tcoef$

Simulation of resistor nonlinearity with mismatch is carried out for input resistor and feedback resistor of opamp. The simulation considered the mismatch between the parameters rend, rs, dw and neglected the mismatch between wr and lr. For these conditions, the performance of driver was not changing considerably. The performance is tabulated in table 2.2.

Operating conditions are as follows. Input frequency is 1.25 kHz. Width(wr) of

SNR	86.95 dB
SDR	96.52 dB
SNDR	86.59 dB

Table 2.2: Performance with mismatch in rend, rs, dw

resistor is varied keeping lr, dw, rend, rs as constant.Table 2.3 shows performance with resistor non-linearity with mismatch in width(wr). We placed input resistor width as 1μm and varied the feedback resistor width as shown in the table. Output amplitude in testing is 0.9912 Volts. So, Closed loop gain of op-amp is 0.9912. Closed loop gain matches when feedback resistor width is 1.008μm. So, there is degradation of 3 dB in SDR with the mismatch in width(wr).

By slight mismatch of 0.1μm change in width, performance was changed and is shown below. So, It is better to have higher width poly resistors in design.

wr(in μm)	o/p amp(in Volts)	SNR(in dB)	SDR(in dB)	SNDR(in dB)
0.93	1.0782	87.28	77.81	77.34
0.93	1.0782	87.28	77.81	77.34
0.94	1.0663	87.28	79.26	78.62
0.95	1.0546	87.28	80.93	80.03
0.96	1.0432	87.28	82.94	81.58
0.97	1.032	87.29	85.42	83.24
0.98	1.0210	87.29	88.67	84.91
0.99	1.0103	87.29	93.07	86.27
0.991	1.0093	87.29	93.56	86.37
0.992	1.0082	87.29	94.05	86.46
0.993	1.0072	87.29	94.53	86.54
0.994	1.0061	87.29	94.98	86.61
0.995	1.0051	87.29	95.40	86.67
0.996	1.0040	87.29	95.77	86.71
0.997	1.0020	87.29	96.08	86.75
0.998	1.0019	87.29	96.30	86.77
0.999	1.0009	87.29	96.42	86.79
1	0.9998	87.29	96.44	86.79
1.001	0.9988	87.29	96.35	86.78
1.002	0.9978	87.29	96.17	86.76
1.003	0.9967	87.29	95.90	86.73
1.004	0.9957	87.29	95.56	86.69
1.005	0.9947	87.29	95.17	86.63
1.006	0.9936	87.29	94.74	86.57
1.007	0.9926	87.29	94.29	86.50
1.008	0.9916	87.29	93.82	86.42
1.009	0.9906	87.29	93.36	86.33
1.01	0.9896	87.29	92.89	86.23
1.02	0.9795	87.29	88.82	84.98
1.03	0.9696	87.29	85.89	83.52
1.04	0.96	87.29	83.69	82.12
1.05	0.9505	87.29	81.95	80.84
1.06	0.9412	87.30	80.53	79.70
1.07	0.9321	79.33	78.69	78.69
1.08	0.9321	87.30	78.30	77.79
1.09	0.9144	87.30	77.40	76.98

Table 2.3: Resistor nonlinearity with mismatch

2.4.4 Performance by varying bias currents

In simulations, Noise is dominant at higher amplitudes. But in testing, Distortion is dominant at higher amplitudes. So we varied bias currents to check whether chip is working at any other bias currents. Fig. 2.6 test-bench for varying IBIAS2 Current source and placing IBIAS1 Current source constant. At higher bias current in feed forward path, Performance was improving. Fig. 2.7 shows how performance varied with bias currents.

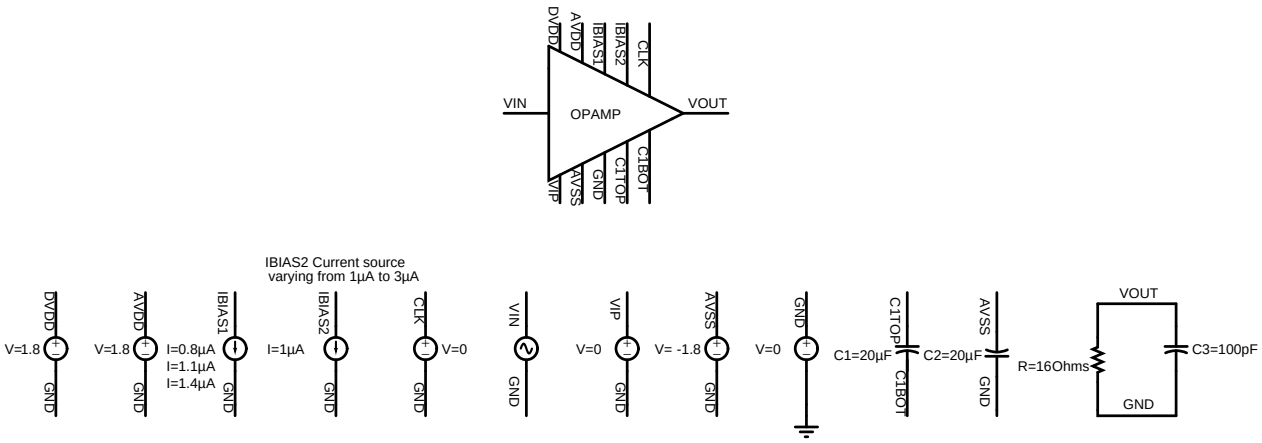


Figure 2.6: Testbench for measuring performance with varying IBIAS2 Current source

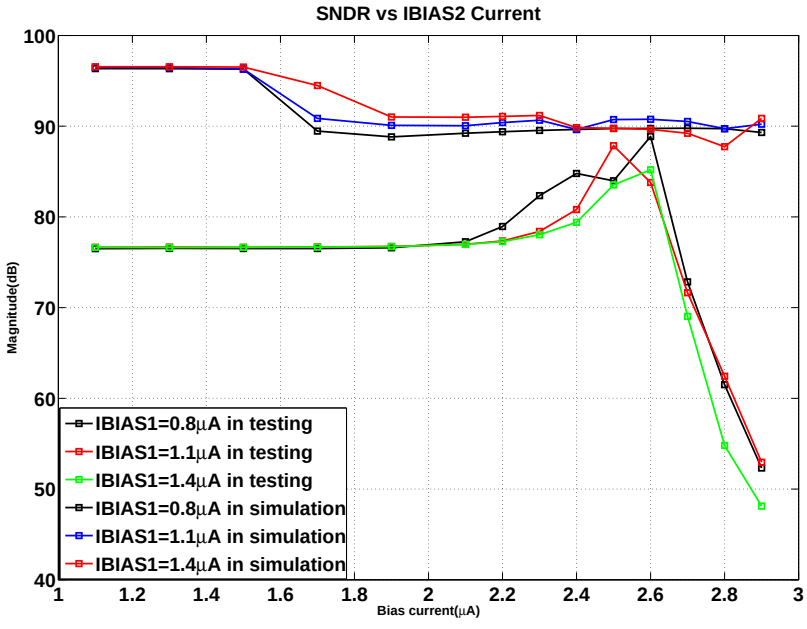


Figure 2.7: SNDR vs IBIAS2 Current

2.4.5 Current in first, second and its bias stages

Fig. 2.8 is used to find the currents through first,second and its bias stages. Fig. 2.9 shows total current in first two stages in simulation and testing with no load condition.

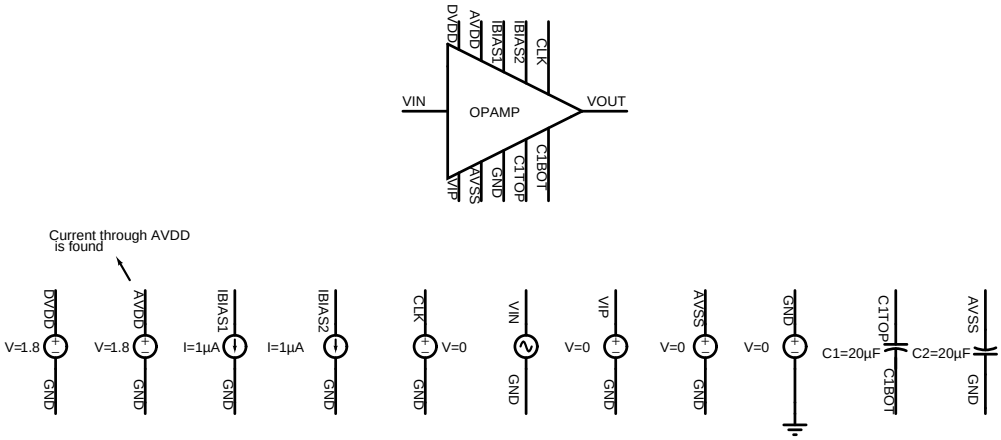


Figure 2.8: Testbench for finding currents in first, second and its bias stages

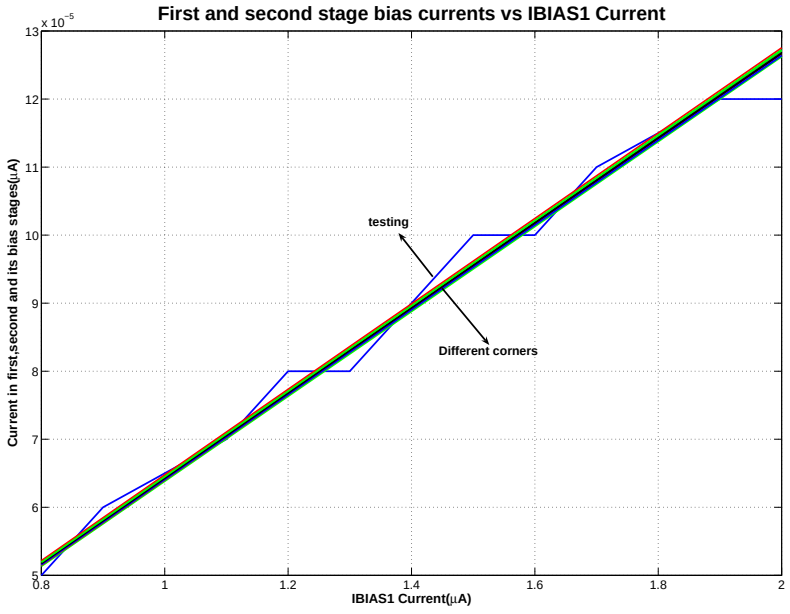


Figure 2.9: Current through first, second and its bias stages.

2.4.6 Current in feedforward, output and its bias stages

Fig. 2.10 shows test bench to find the currents through feed forward, output and its bias stages. From Fig. 2.11, Output stage current mirroring is not happening correctly. This is observed in Monte carlo mismatch simulation.

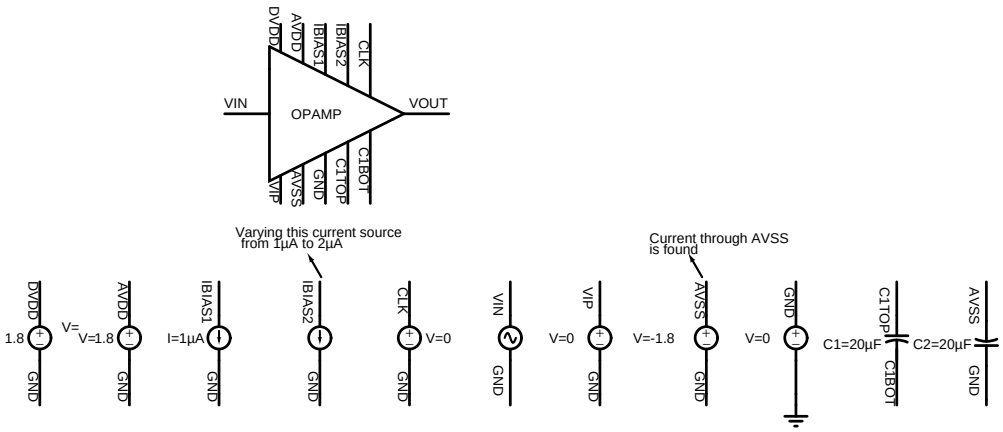


Figure 2.10: Testbench for finding currents in feedforward, output and its bias stages

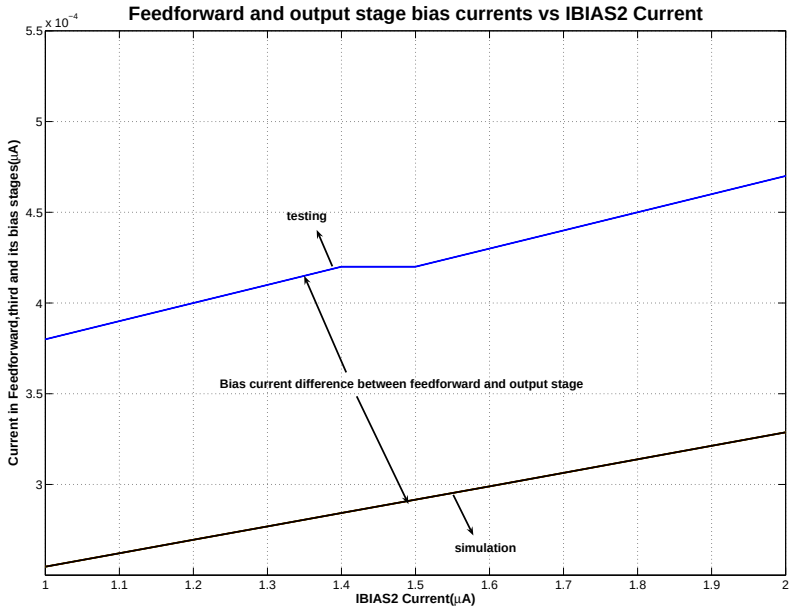
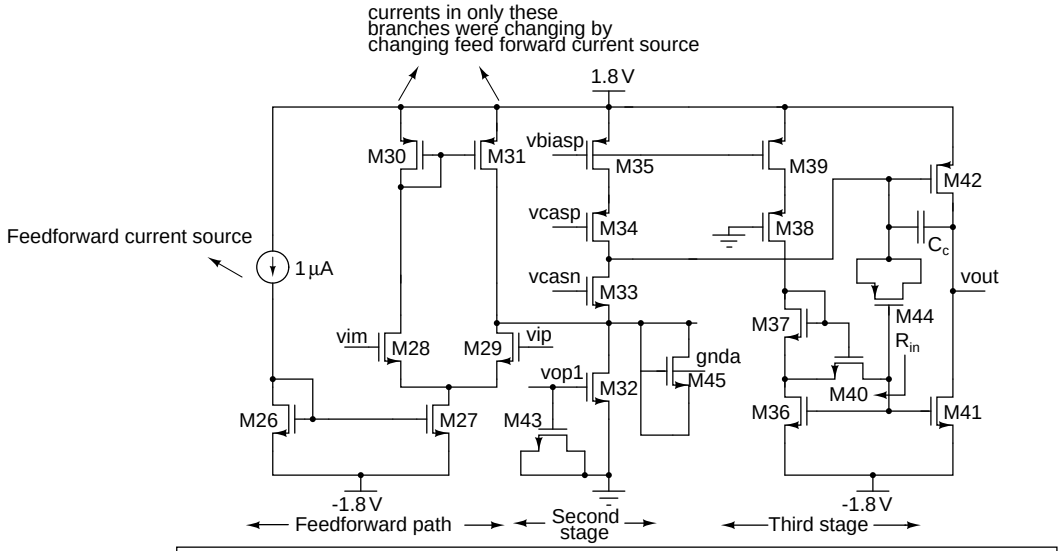


Figure 2.11: Current through feedforward, Output stage and their bias stages.

2.4.7 Possible problems with Op-amp

(1) Bulk of transistor should be connected to lowest potential. Bulk of dummy transistor placed in between second stage and feed forward stage is connected to ground in this design. Second stage is connected between vdda and gnda. Feed forward stage is connected between vdda and vssa. So bulk of this dummy transistor(M45) should be connected to vssa. But in design,Bulk is connected to gnda. Fig. 2.12 shows this.

(2) By increasing current in feed forward current source, Performance is improv-



M26 = 2(0.5 µ/2 µ)	M32 = 20(1 µ/20 µ)	M36 = 2(26.67 µ/0.34 µ)	M41 = 150(26.67 µ/0.34 µ)
M27 = 140(0.5 µ/2 µ)	M33 = 100(1 µ/2 µ)	M37 = 100(1 µ/0.34 µ)	M42 = 400(30 µ/0.34 µ)
M28,M29 = 200(2 µ/2 µ)	M34 = 40(1 µ/1 µ)	M38 = 8(1 µ/0.18 µ)	M44 = 5(72 µ/25 µ)
M30,M31 = 2(1.75 µ/2 µ)	M35 = 20(1 µ/2 µ)	M39 = 4(1 µ/2 µ)	M45 =10(1u/180n)
	M43 = 60(10 µ/2 µ)	M40 = 2(0.24 µ/20 µ)	C_c = 5 pF

Figure 2.12: Second and third stage op-amp schematic.

ing as shown in fig. 2.12. So, Biasing may be one of the problem.

(3)In simulation, as input amplitude increases noise floor is increasing. This is observed in transient noise simulation. Reason for this need to found out.

(4)By increasing feed forward current source, distortion is reducing(SDR is increasing). Exact reason for this need to be found out.

2.4.8 Best results from chip

Fig. **??** shows best results from the chip.Operating conditions are as follows. Input frequency is 1.25 kHz. IBIAS2 Current source is 2.59 μA and IBIAS1 Current source is 1 μA.

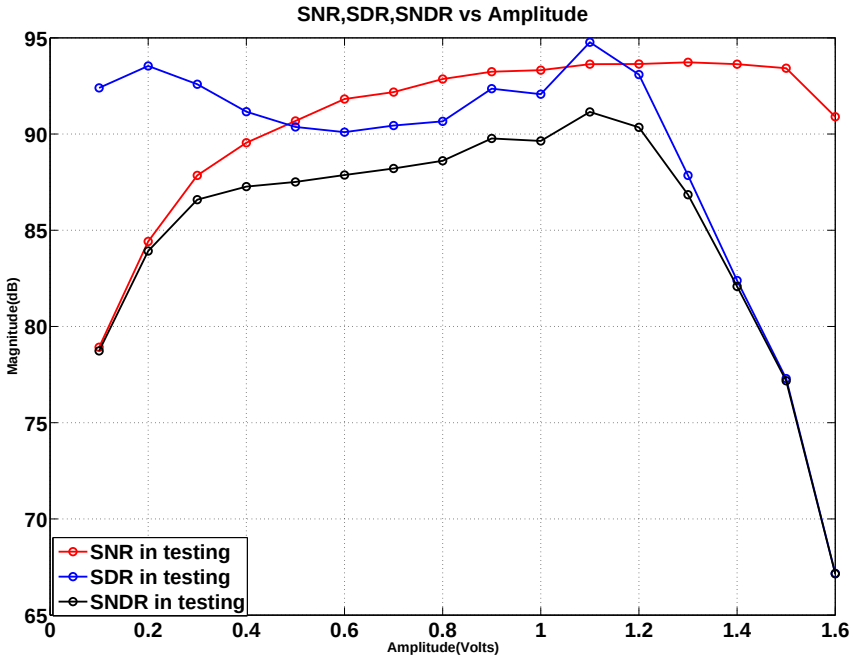


Figure 2.13: Best result of opamp.

CHAPTER 3

Negative Voltage Converter

3.1 Architecture[3]

A simple architecture based on a charge pump is used for the negative voltage converter[2]. Fig. 3.1 shows the circuit for the negative voltage converter. Here, all the transistors (M1-M4) are used as switches. During the first half-cycle, the capacitor C1 is charged to 1.8 V through the switches M3 and M4. During the second half-cycle, capacitor C1 transfers the charge through the switches M1 and M2 to the capacitor C2, thus inverting the input voltage. The switching frequency and the ripple specification at the output decides the capacitor value. During the time when the capacitor C1 is charged by the input voltage, the output capacitor C2 must supply the load current. The load current flowing out of C2 causes a droop in the output voltage which causes a ripple in the output voltage.

The relation between the operating frequency, output voltage ripple and the value

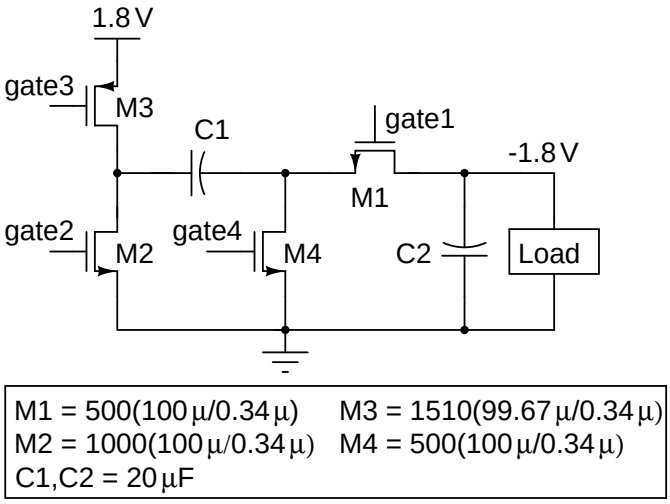


Figure 3.1: Negative voltage converter schematic.[3]

of the capacitor C2 is given below. Let ΔV be the output voltage ripple and f

be the frequency of operation. When C1 is connected between 1.8 V and 0 V, the output capacitor C2 supplies the load current. Thus

$$C2 \cdot \Delta V = I_L \cdot T_{off}, T_{off} = \frac{1}{2f} \tag{3.1}$$

A ripple of 12 mV is tolerable for a THD < -90 dB. For a 16 Ω load, the peak load current is $I_L = 1.6/16 = 100$ mA. For f = 200 kHz, and $\Delta V = 12$ mV, we get C2 = 20 μF. To achieve a maximum efficiency of operation, the impedances of C1 and C2 at the switching frequency f should be very small compared to the load impedance. So an equally high value for C1 is used as is used for C2. The design of this negative voltage converter mainly consists of two parts[2]: switch sizing and switch control signal generation.

3.2 Design[3]

3.2.1 Switch sizing

The sizes of the four switches are shown in Fig. 3.1. The ON resistance (R) of the switches should be very small to satisfy $RC < T_{off}$. The gate-source voltage of the transistors control their ON resistances. Higher the V_{GS}, lower the ON resistance. So to turn on the pMOS transistor M3, we pull down the gate voltage to -1.8 V, thus giving a $V_{GS} = 3.6$ V. Similarly, for the transistor M1, we get $V_{GS} =$ 3.6 V. So without actually boosting the voltage, a $V_{GS} = 3.6$ V is obtained for the transistors M1 and M3. For turning ON the transistor M4, we cannot boost the gate voltage to 3.6 V, as the swing at the gate will become 5.4 V, since its turn-off requires a gate voltage of -1.8 V, violating the reliability of the device. For the gate of the transistor M2, the width is increased to twice the width of M1 (instead of boosting the gate to 3.6 V) to get the same ON resistance as that of M1. The swings at the gates of all transistors are from -1.8 V to 1.8 V.

3.2.2 Switch control signal generation

During one phase the switches M3 and M4 are turned on, and the switches M1 and M2 are turned off. The capacitor C1 is charged to 1.8 V. In the next phase of the clock, the switches M1 and M2 are turned on and the switches M3 and M4 are turned off. To avoid any short circuit current during the transition, the switches must be operated in a particular sequence. While turning off M1 and M2 and turning on M3 and M4 the following order is followed[2]: turn off M1 → turn off M2 → turn on M4 → turn on M3. While turning on M1 and M2 and turning off M3 and M4, the following order is followed: turn off M3 → turn off M4 → turn on M2 → turn on M1.

The external reference clock signal varies from 0 V to 1.8 V. The lower clock voltage level should be shifted from 0 V to -1.8 V for turning off M1, M4. Thus, a level shifter is used to change the clock signal swing from 1.8 V_{pp} to 3.6 V_{pp}. Before

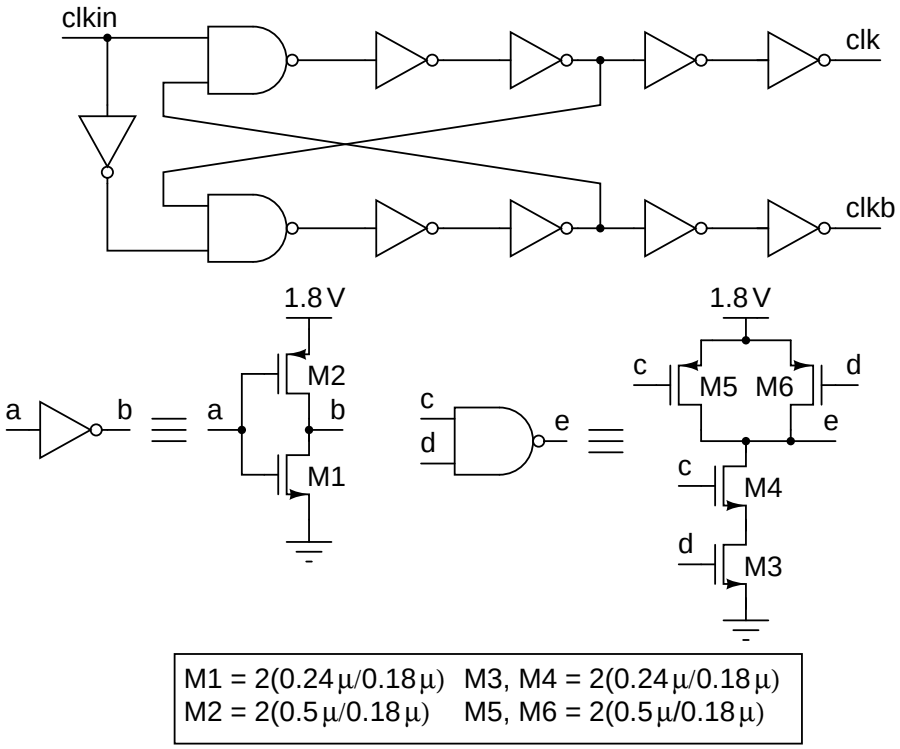


Figure 3.2: Non-overlapping clock generator.[3]

connecting to the level shifter the clock signal passes through a non-overlap generator shown in Fig. 3.2 for generating complementary non-overlapping low signals

required for the level shifter. This eliminates the possibility of short circuit current in the level shifter. The non-overlap generator is supplied from 1.8 V and 0 V. The level shifter is shown in Fig. 3.3[2]. The output of the level shifter swings from

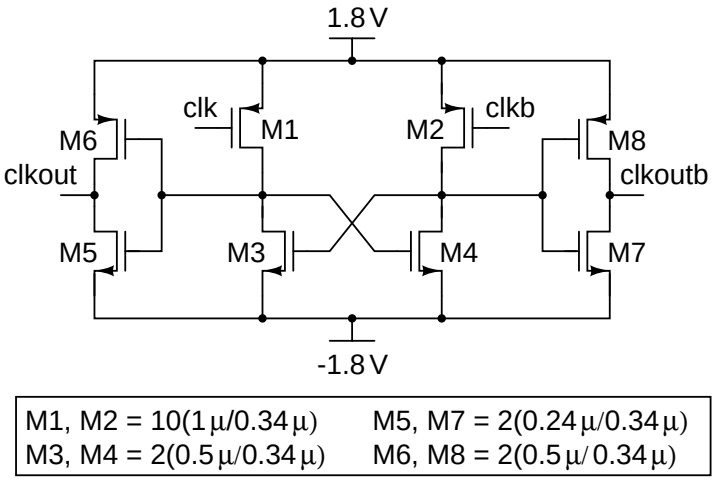


Figure 3.3: Level shifter.[3]

-1.8 V to 1.8 V.

To turn on or turn off the switches M1-M4 in the above mentioned sequence, we need to generate the delayed control signals. The output of the level shifter is passed through a chain of inverters shown in Fig. 3.4, to get different delayed clocks[2]. These delayed clocks from appropriate nodes are OR-ed together to get

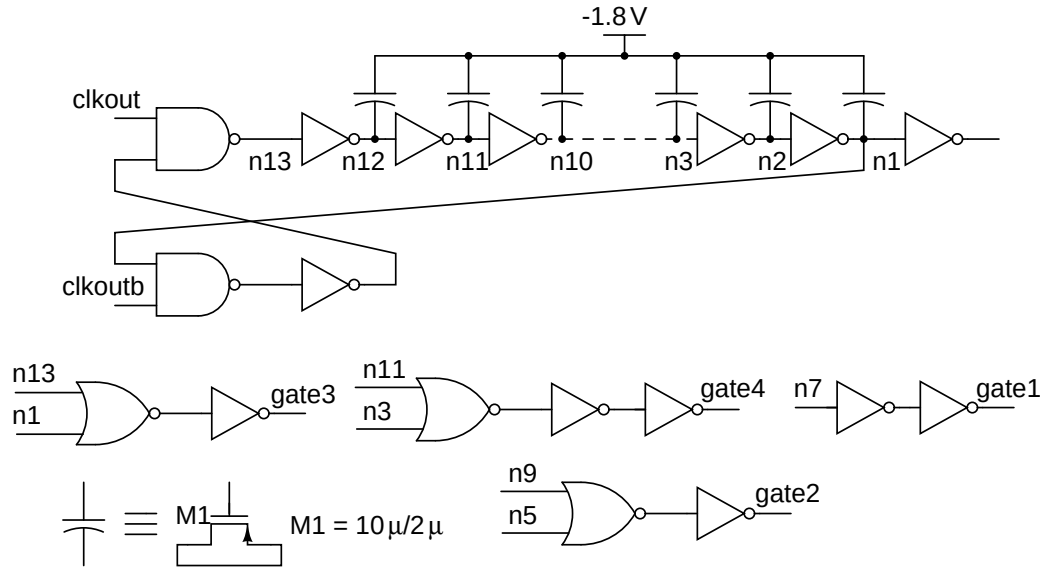
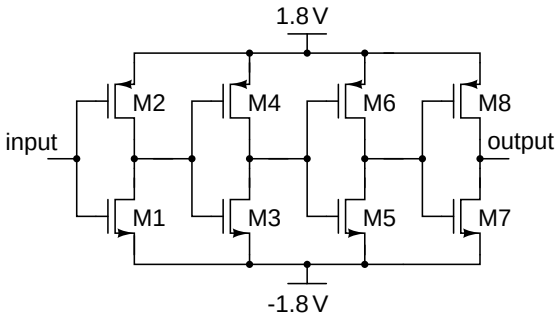


Figure 3.4: Clock delay generator.[3]

gate2, gate3 and gate4 signals with the required delays. The gate1 signal is di-

rectly obtained from the middle of the chain. The pMOS capacitors are included in the chain to increase the delay in the chain without further increase in the number of inverters. The total transition duration for the four gate signals is 5 ns. The charge pump is operated at 200 kHz. The transition time is only 0.2 % of the steady on or off duration. This circuit is operated from 1.8 V and -1.8 V.

The gate control signals generated from the delay chain are fed to the respective gates through a buffer chain for each gate control signal. The buffer chain is shown in Fig. 3.5. The buffered outputs when C1 gets disconnected from 1.8 V and connects between the output and 0 V are shown in Fig. 3.6. The outputs of the buffer chain when C1 gets disconnected from the output and connects between 1.8 V and 0 V are shown in Fig. 3.7.



M1 = 2(0.5 µ/0.34 µ)	M3 = 4(2.5 µ/0.34 µ)	M5 = 8(12.5 µ/0.34 µ)	M7 = 100(10 µ/0.34 µ)
M2 = 2(2 µ/0.34 µ)	M4 = 10(4 µ/0.34 µ)	M6 = 20(20 µ/0.34 µ)	M8 = 110(36.36 µ/0.34 µ)

Figure 3.5: Clock buffer.[3]

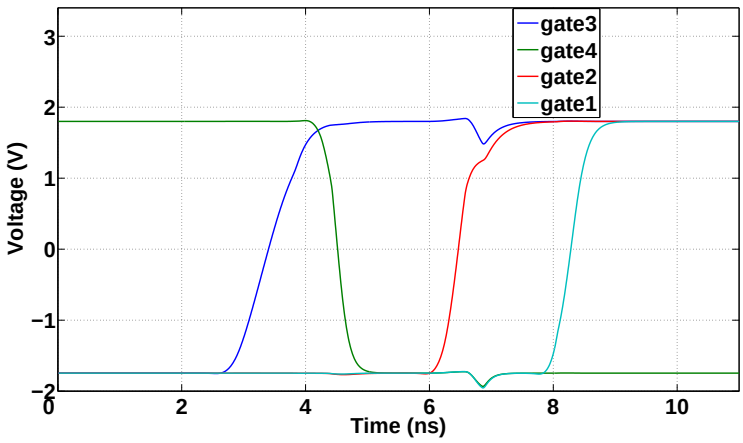


Figure 3.6: Buffer stage outputs during one transition.

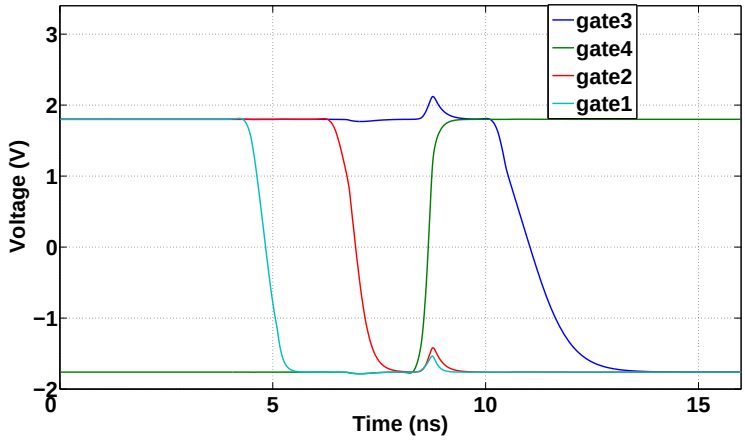


Figure 3.7: Buffer stage outputs during another transition.[3]

3.3 Performance analysis[3]

Efficiency $\left(\frac{\text{Power delivered to the load}}{\text{Power drawn from the supply}}\right)$ of the converter is analyzed by varying the frequency. The values of the capacitors C1 and C2 are scaled appropriately to get the same output voltage ripple of 12 mV for each frequency. It is observed that the efficiency decreases with increasing frequency as shown in Fig. 3.8. This is because switching power increases with frequency. Lower switching frequency ensures high efficiency but with the trade-off of using a large capacitor. A switching frequency of 200 kHz is used which results in a negative voltage conversion efficiency of 96 % and requires two capacitors of 20 μF each.

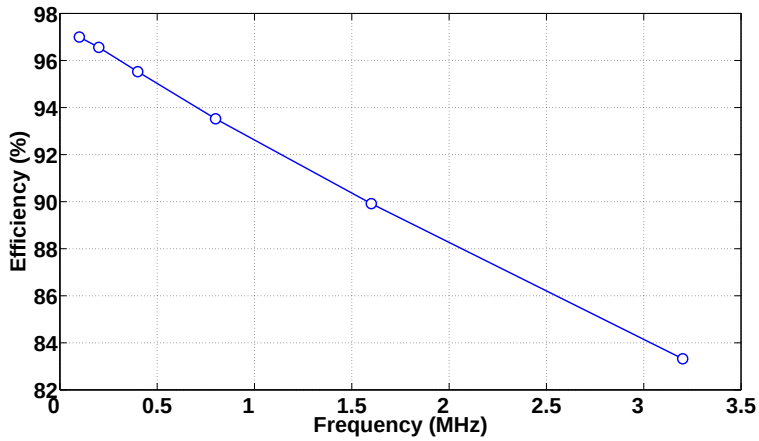


Figure 3.8: Converter efficiency for varying frequency.[3]

3.4 Simulation results[3]

The output voltage of the driver and the negative voltage converter for a 1.6 V_p, 1.25 kHz input is shown in Fig. 3.9. The ripple in the negative voltage is around 12 mV. The driver is simulated with the bond wires of the QFN48 package for slow

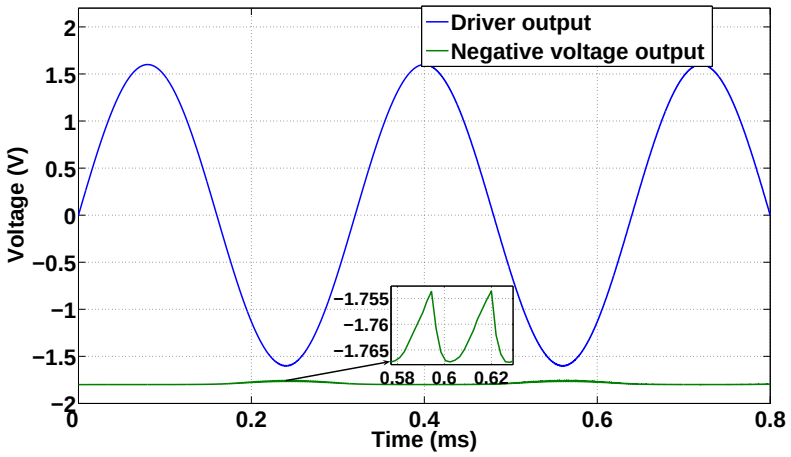


Figure 3.9: Voltage waveforms for 1.6 V_p input.[3]

nMOS and pMOS corner, minimum resistor and capacitor corner at 70^0 C. The $\text{THD}+\text{N}\left(\sqrt{\frac{\text{Harmonic power}+\text{Noise power}}{\text{Signal power}}}\right)$ for an input amplitude varying from 0.1 V_p to 1.6 V_p is plotted in Fig. 3.10. The driver has an efficiency of 63 % for an output power of 80 mW as shown in Fig. 3.10.

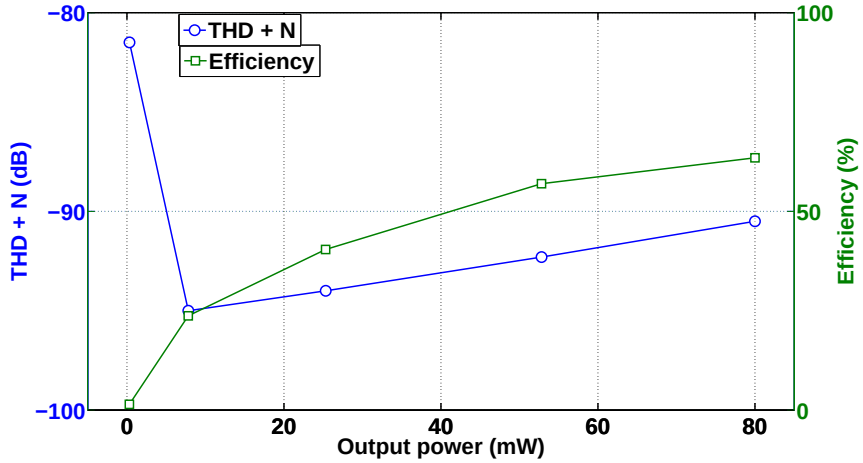


Figure 3.10: THD+N and efficiency of the driver.[3]

3.5 Layout of the headphone driver chip[3]

The headphone driver is integrated with the negative voltage converter and the combined layout is shown in Fig. 3.11. The total area is 1 mm x 1 mm.

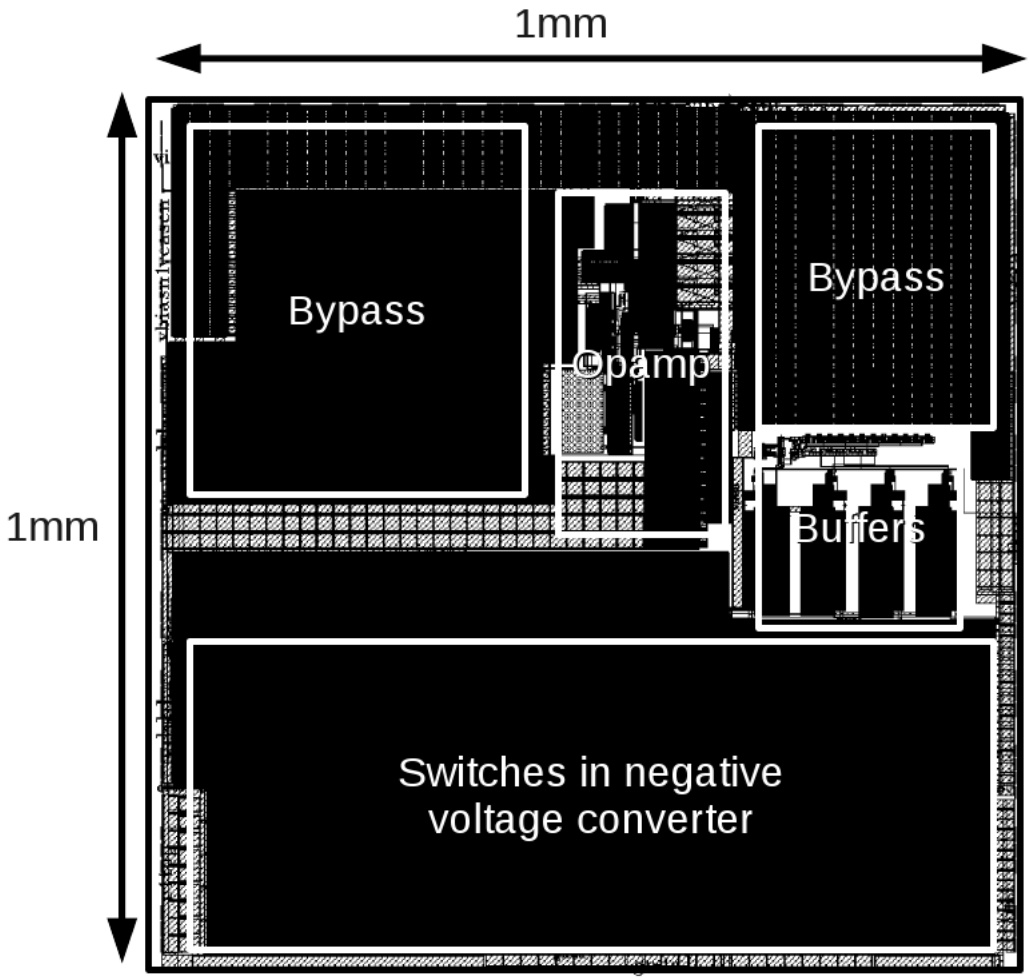


Figure 3.11: Layout of the driver.[3]

CHAPTER 4

Audio Driver chip measurements with Negative Voltage Converter

4.1 Measurement results

4.1.1 Test setup with Negative voltage converter

Fig. 4.1 shows test setup with negative voltage converter. Audio analyzer is used to measure performance of audio driver. Audio Precision AP-SYS-2722 audio analyzer is used to give an analog input signal to the Head phone driver. The input to this driver is an 200 kHz clock.It is given from agilent signal generator.

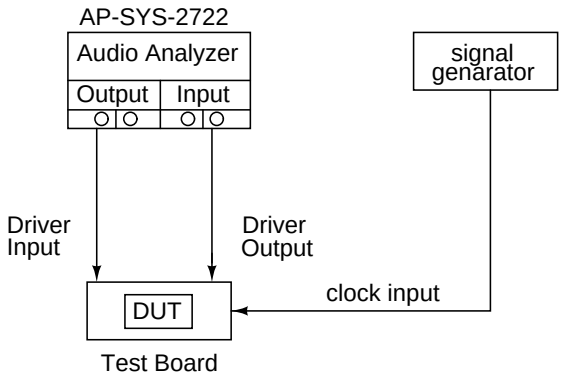


Figure 4.1: Test setup with Negative voltage converter

4.2 Testing and simulation results

4.2.1 series resistance and series inductance problem

Fig. 4.2 shows testbench to measure performance with Negative voltage converter.

Comparison of simulation and testing results were made for SNDR vs Amplitude

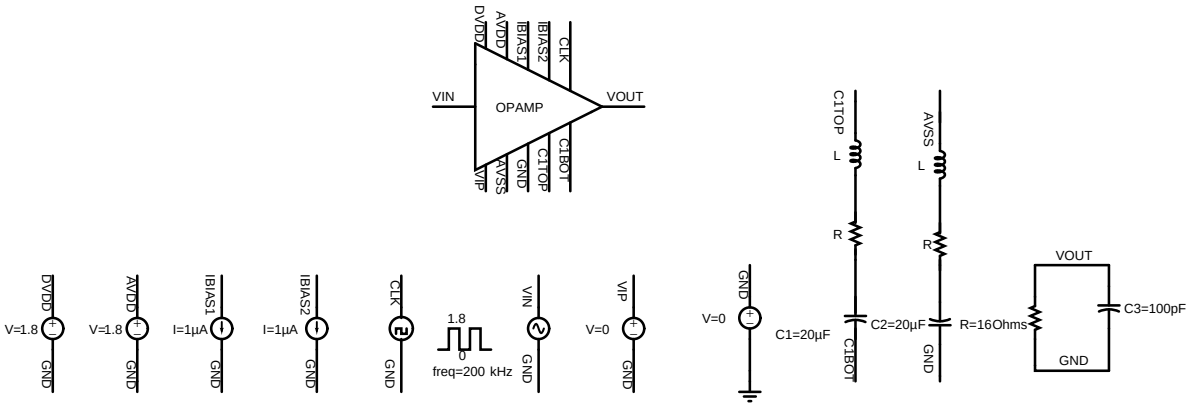


Figure 4.2: Testbench for measuring performance

is as shown in Fig. 4.3. Performance is changing in various process corners. All transistors are in tt corner, Resistors, Capacitors in typ corner.

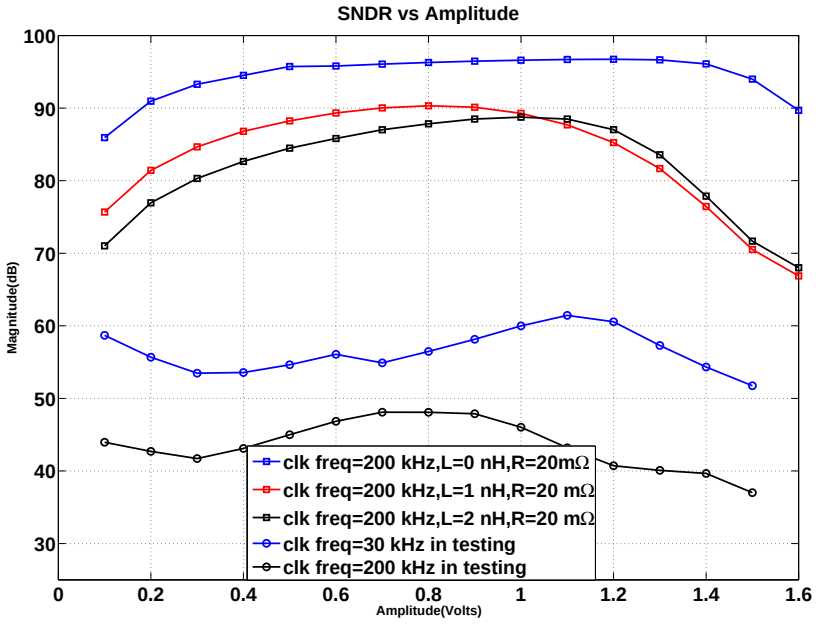


Figure 4.3: Performance with negative voltage converter

Fig. 4.4 shows time domain wave form of output with bondwire+trace inductance of 2 nH and resistance of 20 mΩ in simulation. Operating conditions are as follows. Input frequency is 1.25 kHz. Clock frequency for negative voltage converter is 200 kHz. Test amplitude is 1 V.

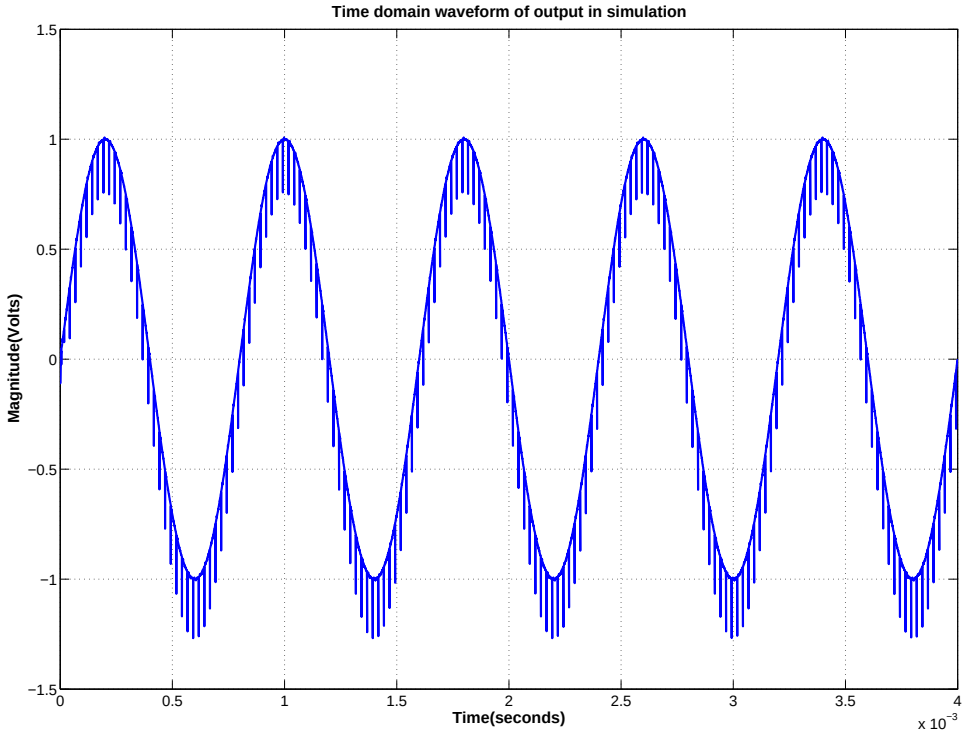


Figure 4.4: Time domain waveform of output with 1 V peak input signal and input frequency of 1.25 kHz in simulation

Fig. 4.5 shows time domain of output in testing. Operating conditions are as follows. Input frequency is 1.25 kHz. Clock frequency for negative voltage converter is 200 kHz. Test amplitude is 1 V. But Fig. 2.6 output amplitude shows 3.24 V in testing. This is because of high frequency signal dependent ripple at the output.

Fig. 4.6 shows time domain wave form of vssa with bondwire+trace inductance of 2 nH and resistance of 20 mΩ in simulation. Operating conditions are as follows. Input frequency is 1.25 kHz. Clock frequency for negative voltage converter is 200 kHz. Test amplitude is 1 V.

Figure 4.5: Time domain waveform of output with 1 V peak input signal and input frequency of 1.25 kHz in testing

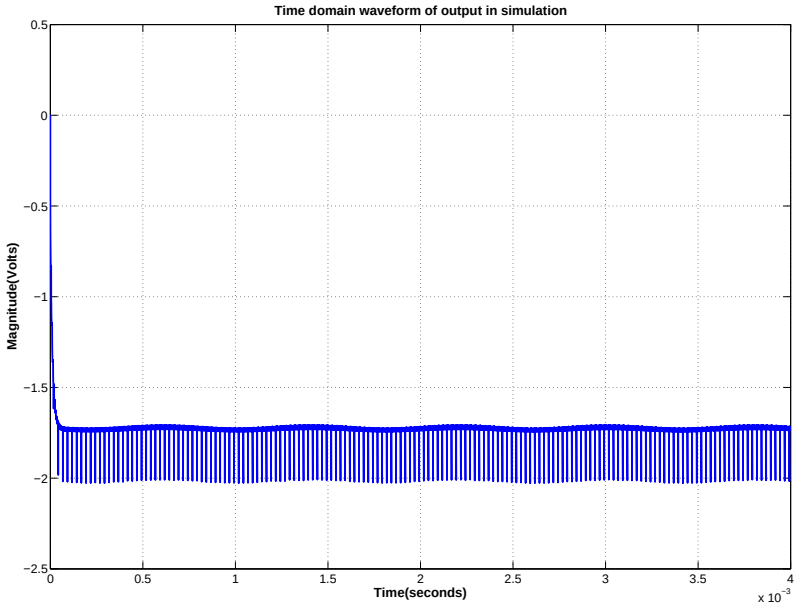


Figure 4.6: Time domain waveform of vssa with 1 V peak input signal and input frequency of 1.25 kHz in simulation

Fig. 4.7 shows time domain wave form of output with bondwire+trace inductance of 2nH and resistance of 20m Ω in simulation. Operating conditions are as follows. Input frequency is 1.25 kHz. Clock frequency for negative voltage converter is 200 kHz. Test amplitude is 1 V.

As shown in this section, One of the reason for performance degradation with

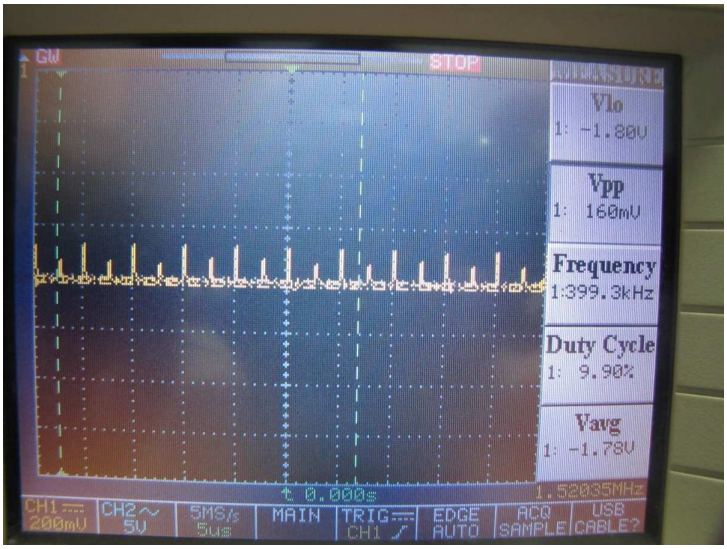


Figure 4.7: Time domain waveform of vssa with 1 V peak input signal and input frequency of 1.25 kHz in testing

negative voltage converter is series bondwire+trace inductance and resistance in negative voltage converter. Negative voltage regulator need to be designed for negative voltage converter. By designing such type of regulator, we can even reduce the capacitor values in negative voltage converter.

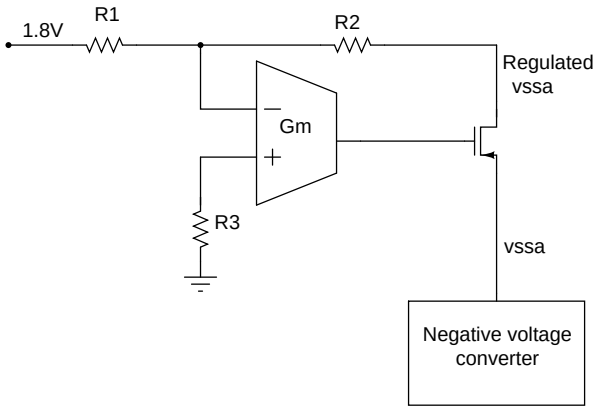


Figure 4.8: One of the possible architecture for Negative voltage regulator

4.2.2 Measurement results of different operating conditions

Ideally in negative voltage converter, As clock frequency increases ripple will decrease on negative supply and performance should improve. But in testing, by decreasing clock frequency from 200 kHz to 30 kHz, performance(SNDR) is improved in testing. By reducing further, Performance is degraded. Fig. 4.9shows SNDR vs AMP for different clock frequencies(i/p frequency of 1.25 kHz). This behavior may be because of gate series resistance of transistors in design.

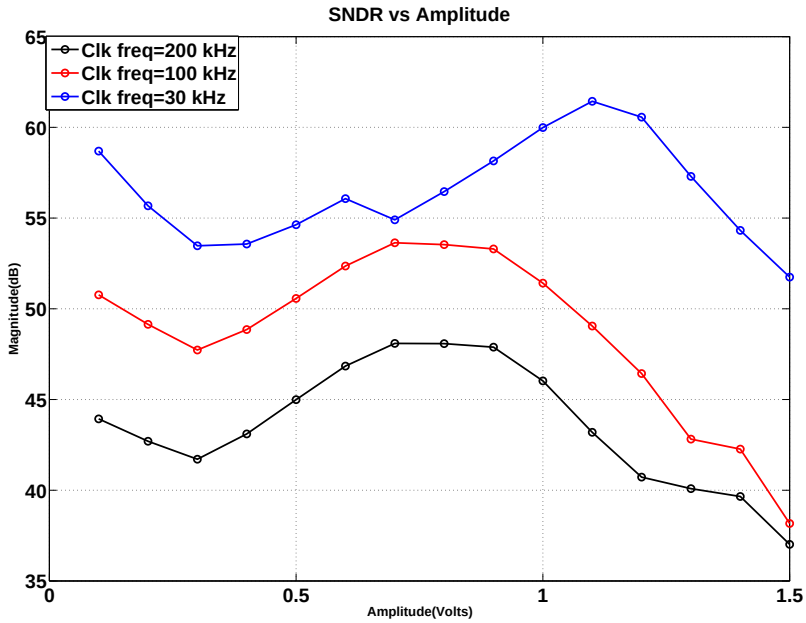


Figure 4.9: Performance with 16 Ω load and i/p frequency of 1.25 kHz

Fig. 4.10 shows SNDR vs Input Amplitude at 1.25 kHz with 1 kΩ load . As clock frequency reduces from 200 kHz to 42 kHz performance was improving and it degrades by further reducing clock frequency.

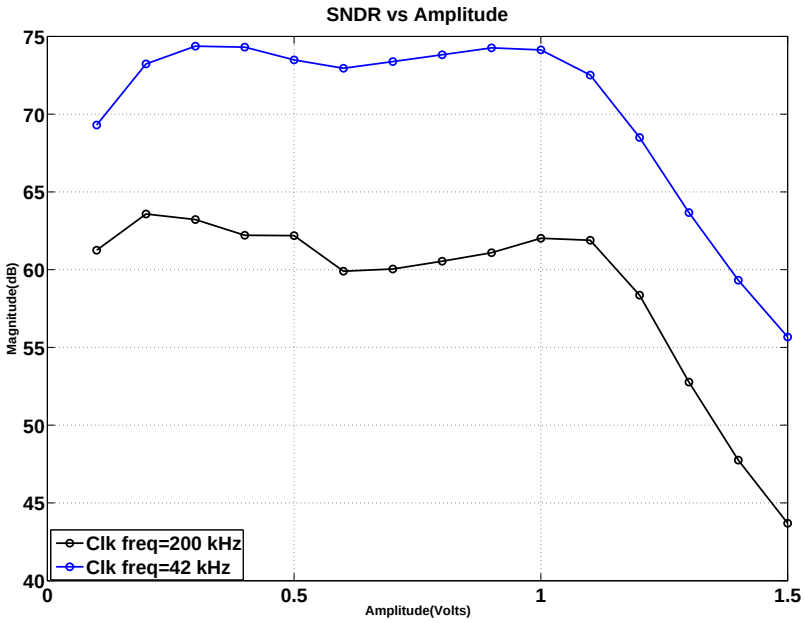


Figure 4.10: Performance with 1k Ω Ohms load and i/p frequency of 1.25 kHz

4.2.3 Possible problems with negative voltage converter

(1)In design of negative voltage converter, large finger widths are used(100 μm) is used.It is maximum finger width that can be used in this technology. Gate resistance may be an issue for switching speed /frequency.

(2)Because of bond-wire+trace inductance and resistance, Performance was reducing. So negative voltage regulator need to be designed.

APPENDIX A

PCB schematic headphone driver chip

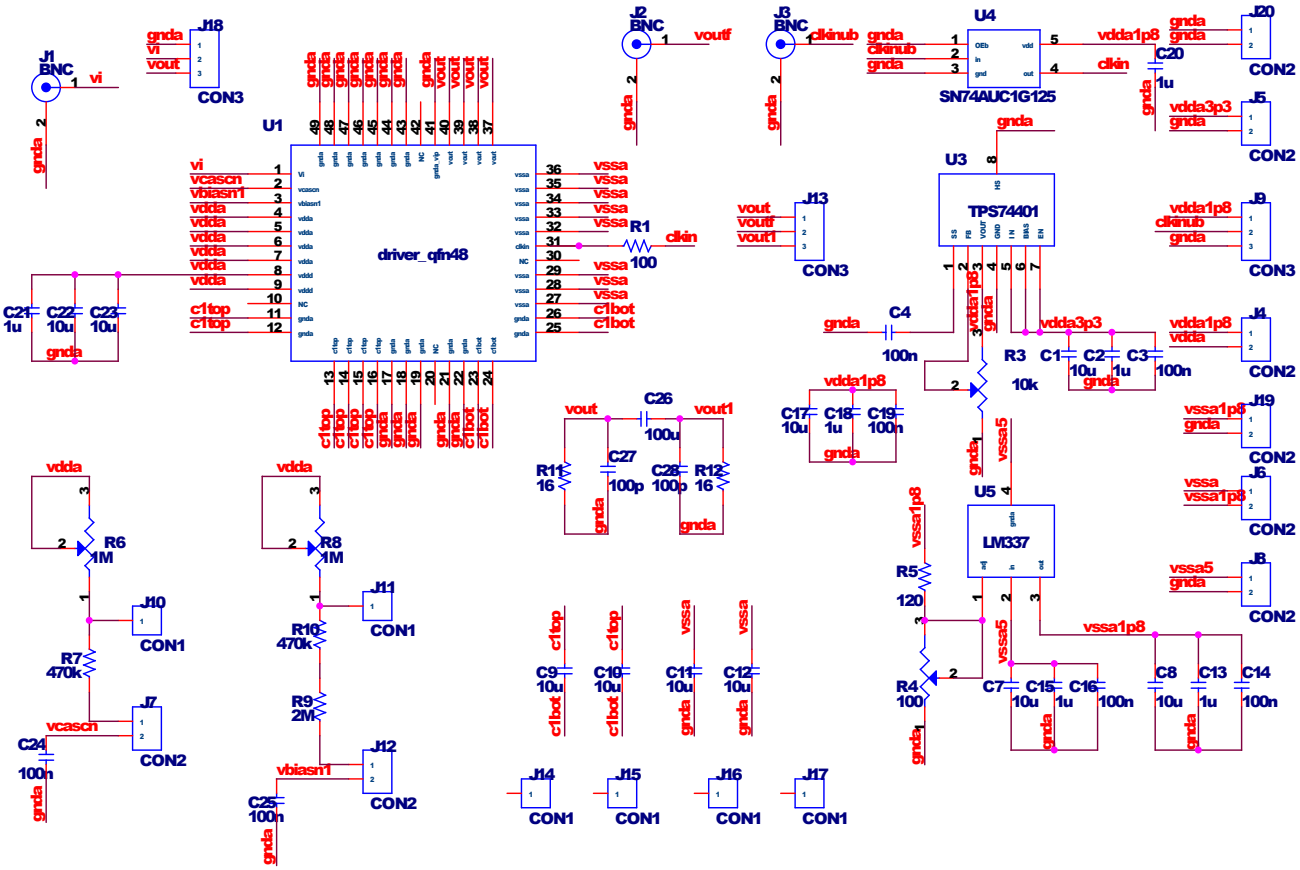


Figure A.1: Headphone driver chip pinout.

REFERENCES

[1] Sandeep Monangi, "Feedforward opamp for pipeline A/D converters and audio drivers and 16 bit R-2R digital-to-analog converter for audio applications," M.Tech Thesis, IIT-Madras, Chennai, Jun. 2009.

[2] Siladitya Dey, "Design of three-stage class-AB 16 Ω headphone drivers having 0.9 V and 0 V common mode voltages and a negative voltage converter for 16 Ω load," M.Tech Thesis, IIT-Madras, Chennai, Jun. 2009.

[3] Kunal Karanjkar,"Design of High Performance Blocks for a Hearing Aid and a Headphone Driver,"M.Tech Thesis, IIT-Madras, Chennai, June, 2012