Design Of High Speed Front End Detection System For India Based Neutrino Observatory

A Project Report

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MAY 2013

DEDICATED TO

MY

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THESIS CERTIFICATE

This is to certify that the thesis titled **"High Speed Frontend Detection System For India Based Neutrino Observatory"**, submitted by **Anoop M.K**, to the Indian Institute of Technology, Madras, for the award of the degree of **Master of Technology**, is a bona fide record of the research work carried out by him under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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ABSTRACT

KEYWORDS: Transimpedance Amplifier; Offset Cancellation; Comparator; LVDS.

A frontend detection system for India based neutrino observatory is presented in this thesis. The deign accepts current pulses as input and marks the presence or absence of input by a differential voltage at the output. It has a good sensitivity of 1μA all over the process corners and 0° C to 100° C temperature variation . It has a very small input to output delay of 1 nS.

The system follows a differential architecture consisting of eight parallel channels. Each channel has one transimpedance amplifier, differential amplifiers, cross coupled comparator and a LVDS driver. A temperature process invariant differential reference voltage is developed from a bandgap reference and used to compare input signal. It has a very good input impedance matching , the S_{11} is below -15 dB up to 1 GHz over all the process corners and temperature. The trans impedance amplifier has a very high bandwidth of the order of 1.37 GHz. But the overall bandwidth is limited by the differential amplifier stage. The input signal amplitude can vary from 1μA to 80μA and the minimum pulse width is 3 nS.

CMOS UMC180nm technology has been chosen for the design of the system and at a supply voltage of 1.8 V. Cadence's Spectre has been used to simulate the behavior of the circuit and for simulations. Cadence's Virtuso is used to do the layout editing and paracitic extraction.

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NOTATION

I_D	Mosfet Drain Current
I_C	BJT Collector Current
I_S	BJT Junction Reverse Saturation Current
μ	Mobility
C_{ox}	Oxide Capacitance
W	Width Of The Transistor
L	Length Of The Transistor
ΔL	Variation In Transistor Length L
ΔW	Variation In Transistor Width W
A_K	Proportionality Constant For $\mu c_{ox}(W/L)$ Mismatch
A_{VTH}	Proportionality Constant For V_{th} Mismatch
R_{on}	Transistor On Resistance
g_m	Transistor Transconductance
g_{d0}	Transistor Output Conductance At V_{DS} = 0
γ	Transistor Thermal Noise Empirical Parameter

CHAPTER 1

Introduction

Many multi-disciplinary researches are going on in the field of particle physics and provided many significant results. The India-based Neutrino Observatory (INO) is one such particle physics research project which primarily aims to study atmospheric neutrinos. For this purpose INO has built a massive magnetized Iron Calorimeter(ICAL). A resistive plate chamber (RPC) is used for particle detection and it is like two planar resistive electrodes separated by few milli meter. Signal pickup panels are mounted on either side of the RPC detector. The charge produced inside RPC induces signals on the strips of the pickup panels due to capacitive coupling. The frontend detection system process the generated current pulses from RPC pickup strips [1]. The input current can vary in amplitude and in pulse width. The input current signal can be as low as 1 μA and can go up to 80 μA. The pulse width can vary from 3 ns to some 10 ns.

1.1 Overall Circuit Description

Fig. 1.1 show the overall block diagram of the system. Eight channels has to be implemented in parallel. Each channel consist of a trans impedance amplifier , a comparator stage and a Low Voltage Differential Signaling driver. Each blocks are described in detail in subsequent chapters. The front end detector plays an important role in overall system . Because it determines sensitivity of the system. Signal current as small as $1uA$ can be detected and occurrence of a current pulse acknowledged by a LVDS output.

The input impedance of TIA matched to 50 Ω input lines. Interleaved offset cancellation scheme is employed and for four channels at a time so that it never misses an input. The generation of additional offset cancellation pulses, for interleaved offset cancellation, consumes very little amount of power as pulse generating circuits consume zero static power.

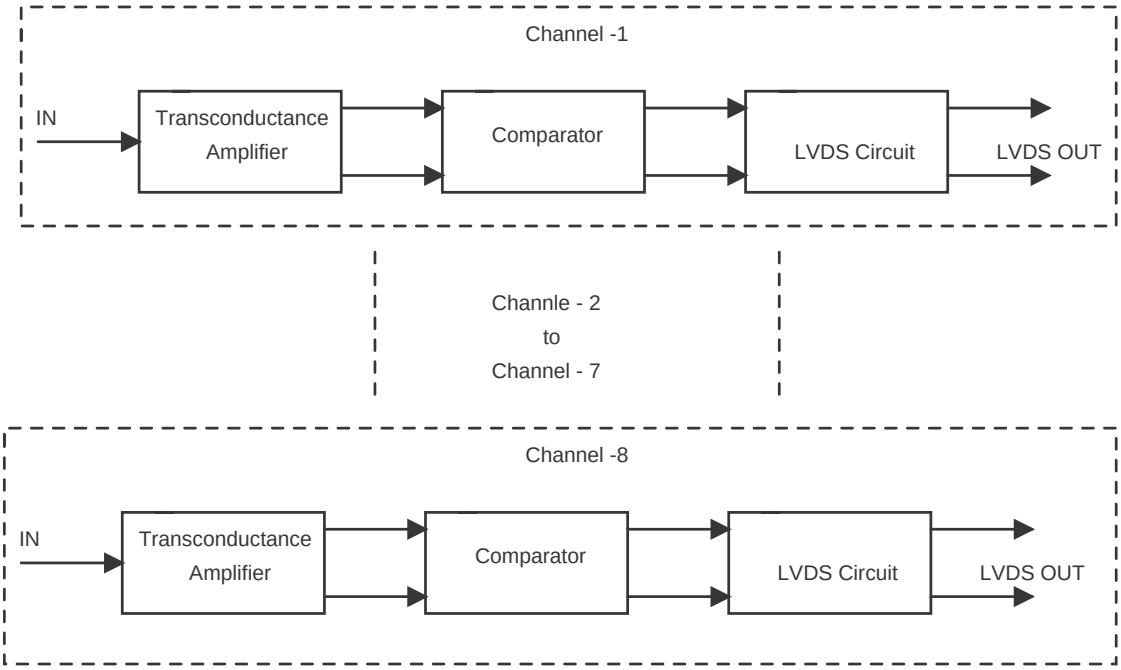


Figure 1.1: Proposed System

The comparator blocks provide necessary amplification with differential amplifiers. This differential topology suppress all common mode disturbances happening in the circuit from supply or from devices. Input offset cancellation method is employed to store offset value in capacitor and cancel the same. Cross coupled comparator provide quick decision making and give high speed transition. Inverter buffers are used to make the swing rail to rail and to provide sufficient strength to drive the LVDS stage.

The Low Voltage Differential Signaling(LVDS) driver uses a current mode logic circuit which switches the polarity of the current over output lines. Output common mode voltage and current kept at the required level by feedback mechanism. A constant differential reference voltage generating circuit implemented in the chip itself by a bandgap reference.

CHAPTER 2

Transimpedance Amplifier - TIA

The primary function of a Trans Impedance Amplifier(TIA) is to convert the incoming current pulse, which is the input signal, to a voltage signal with a sufficient gain and minimum noise contribution. TIA input should be matched to incoming line impedance for maximum power transfer and minimum reflection.

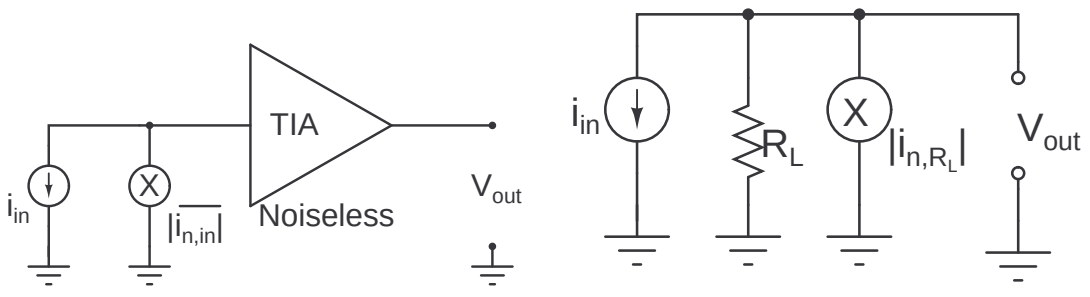
The small signal transimpedance gain (Z_t) and small signal input impedance Z_{in} is given as

$$Z_t = \frac{v_{out}}{i_{in}} \tag{2.1a}$$

$$Z_{in} = \frac{v_{in}}{i_{in}} \tag{2.1b}$$

The amount of noise added by TIA can be represented by input referred noise current spectral density. The input referred noise equivalent current when applied to the input of a noiseless TIA, will produce the same amount of noise at the output which is produced by a noisy TIA without any input. The above concept is illustrated in 2.1a . The output noise voltage and input noise current are related by

$$\overline{i_{n,in}^2} = \frac{\overline{v_{nout}^2}}{z_{in}^2}. \tag{2.2}$$



(a) TIA Equivalent Noise Model (b) Resistance as TIA

Figure 2.1: TIA Noise Model And Simple Implementation

A simple implementation of TIA is a resistor R_L as in 2.1b. The trans impedance gain and input impedance will be simply equal to the resistance R_L. Even though the input impedance can be easily matched, by default it fixes the gain. For low value impedance matched circuit the gain will be small. The noise power spectral density from the resistor is given as $\overline{|i_{n,in}|^2} = \frac{4KT}{R_L}$ where K is Boltzmann constant and T is temperature in kelvin. Obviously the smaller the resistance larger will be the noise. So we must design a circuit which gives high gain with a low input impedance and a very little noise contribution.

2.1 Regulated Cascode RGC

Regulated Cascode RGC can be considered as a common gate amplifier but with a local feedback.This feedback makes the common gate amplifier's performance much better and make it a good choice. The RGC's input impedance is reduced approximately by the gain of local feed back. So input matching with a 50 Ω line can be achieved with a relatively smaller power consumption and with a small area. The proposed front end system has eight input channels so this improvement, in power and area, creates a larger impact in overall design. Local feedback helps to set the dc operating point and it also minimizes the variation in voltages and current.

2.1.1 Circuit Design And Operation

RGC provides a good trade off among Impedance matching, Transimpedance gain, Bandwidth and power consumption. Fig 2.2 shows the schematic of regulated cascode circuit. Transistor M_1 with resistor R_2 acts as common gate transistor and resistor R_1 fixes the current through the branch. M_2 and and R_3 acts as common source amplifier which gives a transconductance boosting. When the voltage at input node increases due to some reason the voltage at drain of M_2 decreases by a large amount. So the V_{gs} of M_1 and current through M_1 decreases and reduced current through R_1 decreases the voltage at the input node. Thus local negative feed back ensures constant current and dc bias stability.

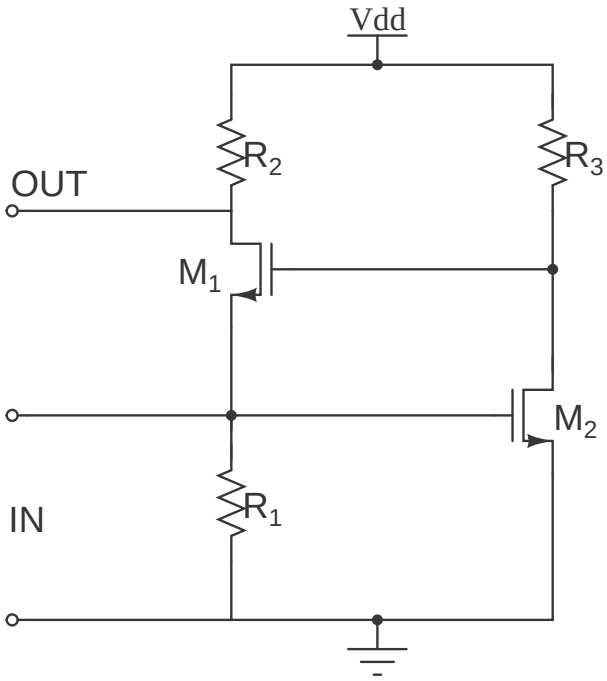


Figure 2.2: Regulated Cascode.

$$Z_{in}(0) = \frac{1}{g_{m1}(1 + g_{m2}R_3)}. \tag{2.3}$$

$Z_{in}(0)$ gives the low frequency input impedance. The input impedance is reduced by a factor of $(1 + g_{m2}R_3)$, when compared to a common gate amplifier, where $(1 + g_{m2}R_3)$ is the gain of the feedback loop.Effectively regulated cascode circuit behaves like a common gate transistor with an effective transconductance $G_m = g_{m1}(1 + g_{m2}R_3)$. The input capacitance coming from gate to source capacitance of transistor M_2. The effective capacitance between gate and drain of M_2 is $C_{gs1} + C_{db2}$. Because of miller multiplication the effective input capacitance is given by

$$C_{in} = (1 + g_{m2}R_3)(C_{gs1} + C_{db2}) + C_{gs2} \tag{2.4}$$

Larger the size of M_1 larger the C_{gs1} and effectively it is multiplied by $1 + g_{m2}R_3$ and increases the effective input capacitance very much. Sizing of the transistors will also make an impact on input impedance as shown in Eq. (2.3). By keeping the effective input impedance of 50Ω a smaller size is chosen for M_1 and larger size is chosen for M_2. The capacitors C_{gs1} and C_{db2} and resistor R_3 creates a zero and a peaking in the

frequency response. The zero causes the effective input impedance to go high at a frequency given as

$$\omega_z = \frac{1}{R_3(C_{gs1} + C_{db2})}. \tag{2.5}$$

The zero can be pulled far apart by lowering the sizes of M_1 or M_2 or R_2. Lowering

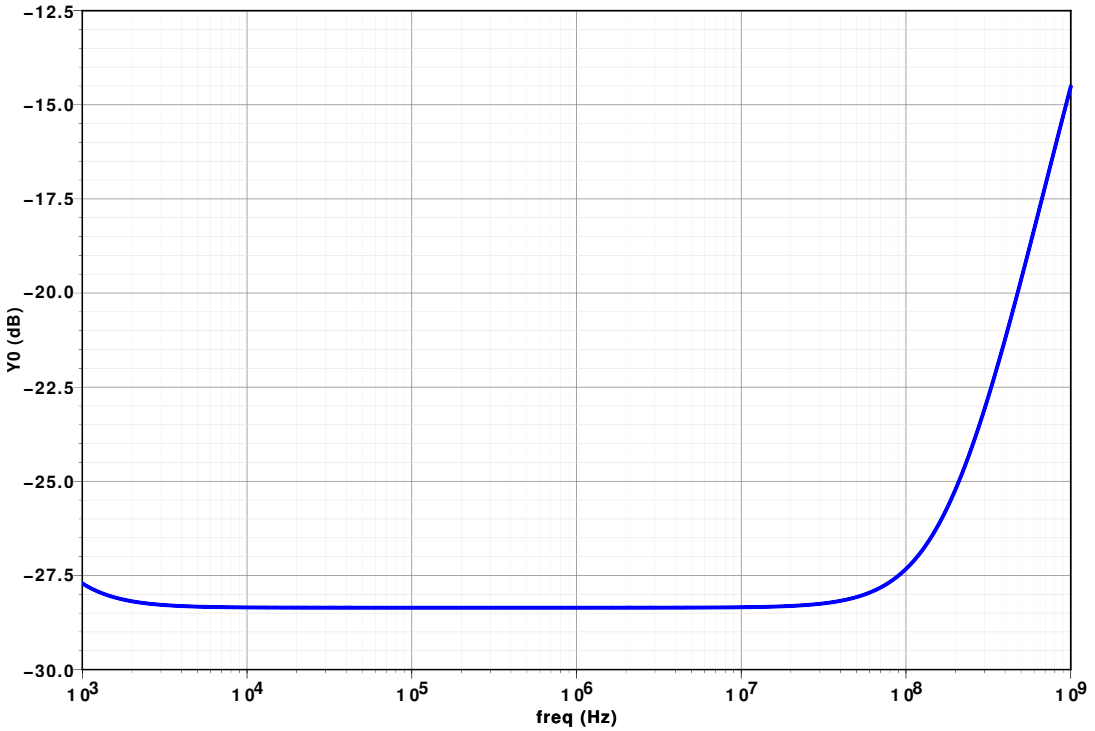


Figure 2.3: RGC Reflection Coefficient.

the size of transistor M_1 helps keeping the zero far and decreases the effective input capacitance. The Fig 2.3 shows variation of S_{11} with frequency, the S_{11} is less than -15 dB up to 1 GHz. The input signal bandwidth is less than 500 MHz and S_{11} is less the -20 dB in the required frequency range.

The transimpedance gain and output 3 dB bandwidth is determined by R_2 and output load. The transimpedance gain is equal to magnitude of R_2 itself and bandwidth of the RGC stage is given by $\omega_{3dB} = \frac{1}{R_2 C_2}$. Improvement in bandwidth can be made by adding a buffer stage to RGC output.

2.1.2 Noise Analysis

On a cascaded system of blocks the first stage has great impact on noise performance of the overall system. So RGC should add minimum noise to the circuit. Fig 2.4 shows the thermal noise current from each of the circuit component. Without considering flicker noise the equivalent input referred noise current spectral density as a first order approximation can be given as [2]

$$\overline{i_{eq}^2} = \frac{4KT}{R_1} + \frac{4KT}{R_2} + 4KT\frac{\gamma g_{d02} + \frac{1}{R_3}}{(g_{m2} + \frac{1}{R_3})^2}(\frac{1}{R_1^2} + \omega^2(c_{gs2} + c_{sb1})^2) \tag{2.6}$$

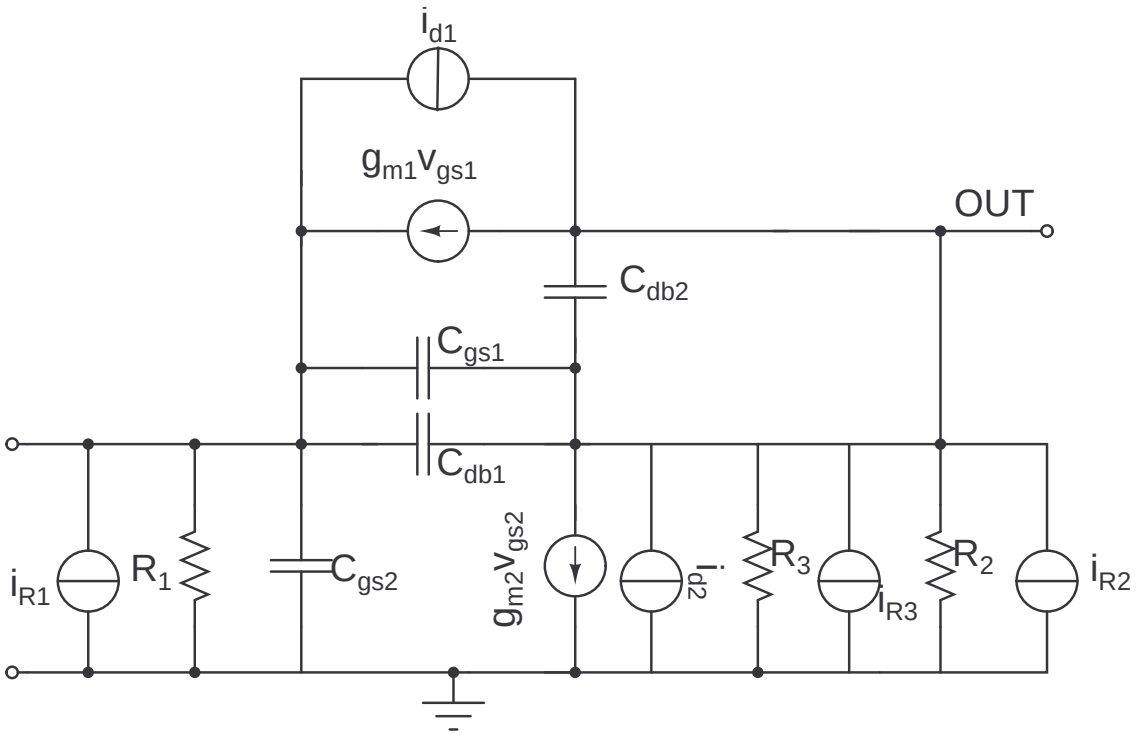


Figure 2.4: Noise Sources In RGC

Where i_{d1} and i_{d2} are noise currents from transistors M_1 and M_2 respectively, i_{R1} to i_{R3} are thermal noise currents from R_1 to R_3, K is the Boltzmann constant and T is the temperature in kelvin. Thermal noise contributions from R_1 and R_2 dominates at lower frequencies and at higher frequencies the capacitive terms could have larger impact. Higher values of resistor decreases the equivalent noise current at the input and these higher resistor will help in attaining better gain and better feedback, lower current consumption and even lower input impedance. The noise from M_2 and R_3 are reduced

by the gain of the feedback loop even at low frequency. The local feedback helps in reducing the noise by a greater extend and helps to achieve bias stability. From the equation a small g_{m2} and a large R_2 gives a lesser noise. Fig 2.5 shows the input noise

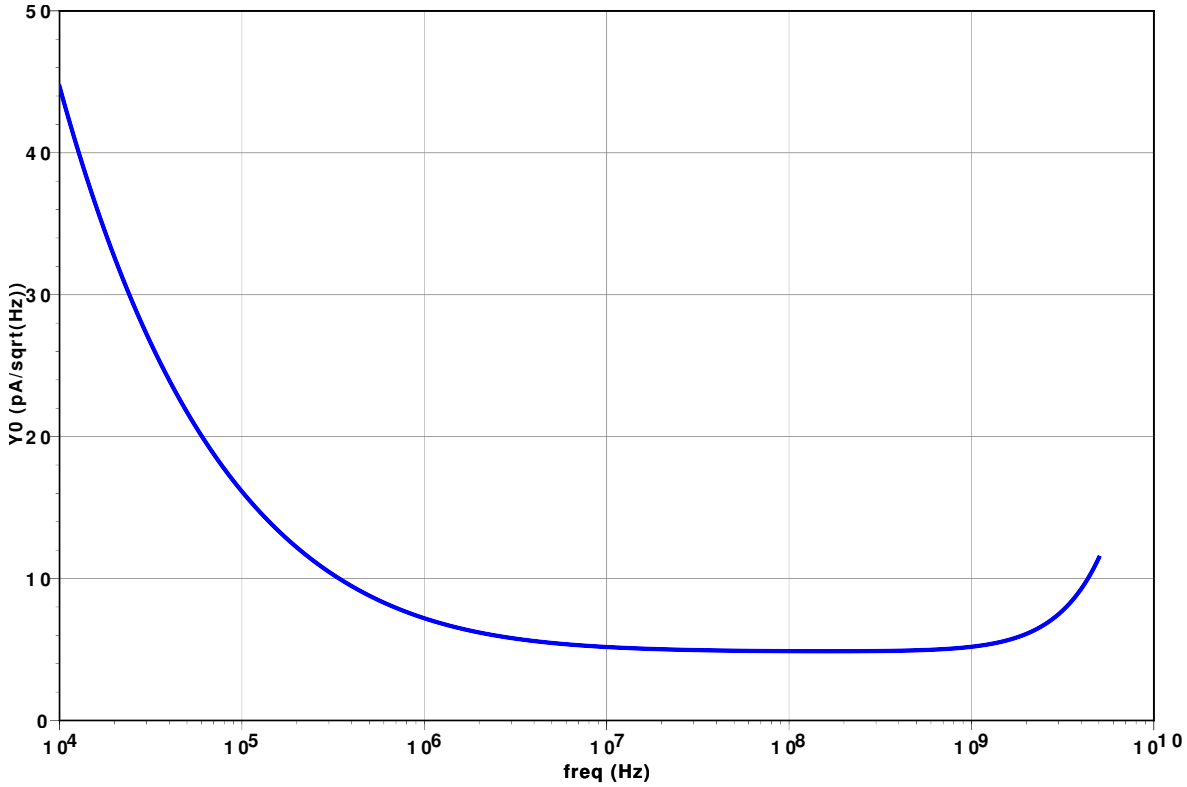


Figure 2.5: RGC Noise Spectral Density.

equivalent current power spectral density. The effective equivalent noise is less than 5 $pA/\sqrt{Hz}$ on operating frequencies.

2.1.3 Circuit isolation And Charge Injection

The signal input current can vary from 1 μA to 80 μA. For small input current amplitude, the output voltage will also be small and it could be even less the dc offset of subsequent differential amplifier stage in the comparator block shown in Fig 1.1. An offset cancellation scheme is adopted and explained in later section. In the offset storage phase, the offset between differential amplifier input is stored in offset storage capacitor and in the normal operation mode the stored offset is used to cancel the offset difference in differential amplifier.

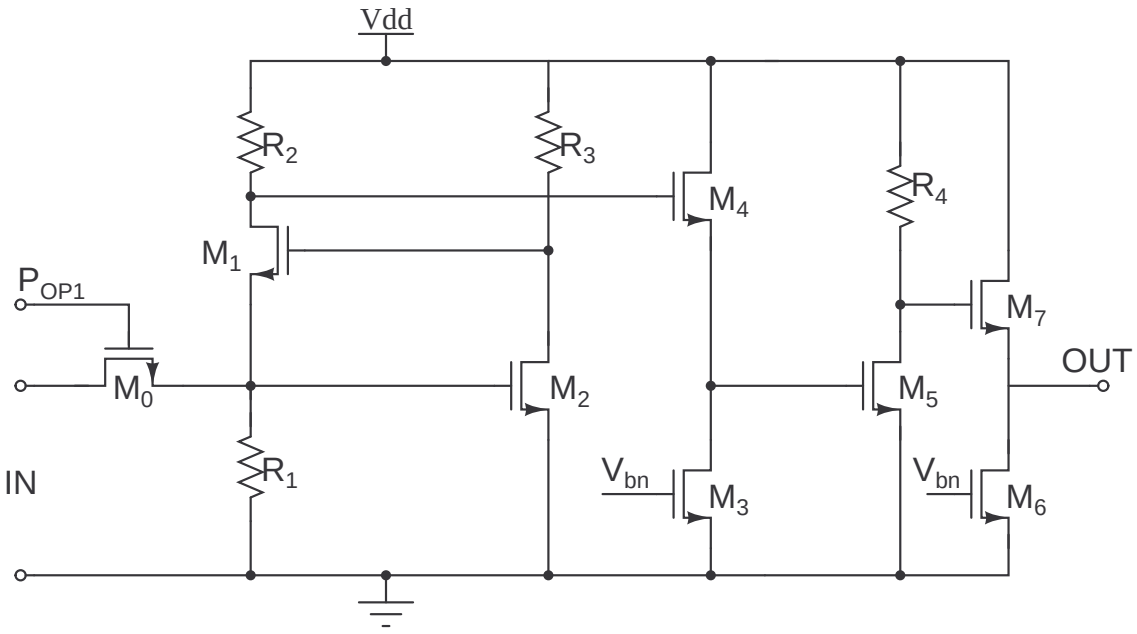


Figure 2.6: Complete TIA Circuit

At the beginning of offset cancellation phase the RGC will be isolated from the input and the dc offset will be stored in capacitor C_1 and C_2 shown in Fig. 3.5. Consider Fig 2.6, the complete circuit diagram of TIA, when signal P_{OP} goes low the transistor M_0 turns off and circuit will be isolated from the input. At normal operation the transistor M_1 is turned on and keep it in on to allow the signal current to flow into the circuit. This transistor will have an on resistance and so the input matching might be get affected and the input impedance of RGC has to be redesigned to make total impedance matched to 50 Ω. A large sized transistor offers low impedance and as it will be in the linear region when it is on. Now the total input resistance going to be resistance of transistor M_0 and input resistance of RGC. The on resistance is around 10 Ω so the RGC has to be designed for 40 Ω. The total input impedance is matched to 50 Ω and the S_{11} is less than -15dB over temperature and process corners over 1 GHz of frequency range.

On turning transistor M_0 on or off charge accumulated in the channel has to be squeezed into the transistor and out of the transistor respectively via the source and drain terminals. Larger the size of the transistor greater will be the amount of charge injected. Output dc levels has to be settled very fast because the offset cancellation time is very small and it needs a settled dc voltage values to store the offset difference. The injected charges will make the same effect of an input current pulse. Fig. 2.7 shows the

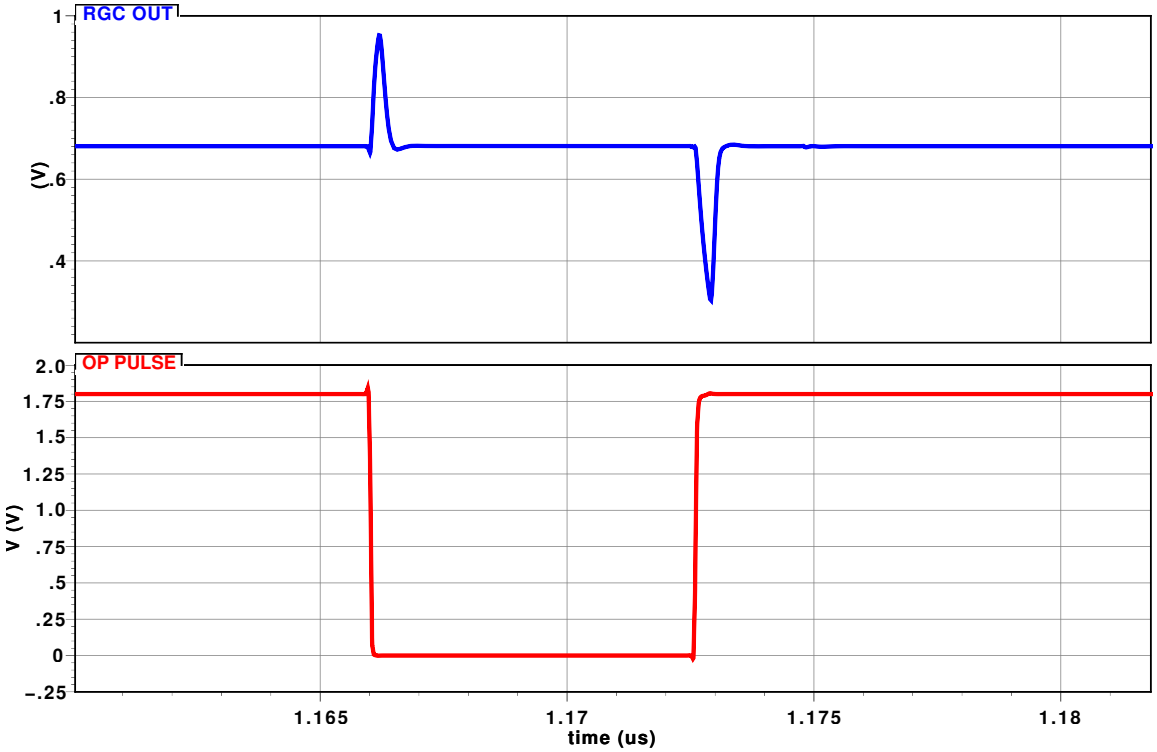


Figure 2.7: Spikes Due To Charge Injection At RGC Output.

pulse OP which is used to turn on and off transistor M_0 and the charge injection effect at RGC's output. It can be seen that even though the injection produces a significant amount of disturbance at output, it is settling out very fast and gives enough time to store offset voltage in capacitor. The amount of time required to settle the output is of the order of pico seconds.

2.1.4 Buffer Stage

The RGC output is given to a differential amplifier for amplification. The input pair of the differential amplifier will have higher sizes for better gain and so it offers a significant amount of capacitive load to the RGC. More the sizes of the RGC the slower will be the response. Adding a buffer stage in between offers a very small capacitive load at the output of RGC and a very small output impedance to the differential amplifier. So we will have an effective enhancement in the total bandwidth. Fig. 2.6 shows RGC with buffer stage.

Transistors M_3 and M_4 acts as first buffer stage , the sizes are quite small and it offers very little load to the RGC. Transistors M_7 and M_8 acts as the output buffer with a small output impedance. These two buffer stages attenuates the signal to compensate that a common source stage is added in between buffers. The common source stage transistor size is very small and it has a very small output load so it will not reduce the bandwidth considerably. The buffers uses a current mirroring biasing scheme. The gate bias voltages V_{bn} derived from the reference circuit explained in Chapter 4. The total output ac gain is shown in Fig. 2.8. The Transimpedance amplifier(TIA) as from the frequency response has a transimpedance gain of 68 dB with a bandwidth of 1.4 GHz. Over process and temperature variations the transistor parameters and resistances varies and it makes variations in gain and bandwidth too.

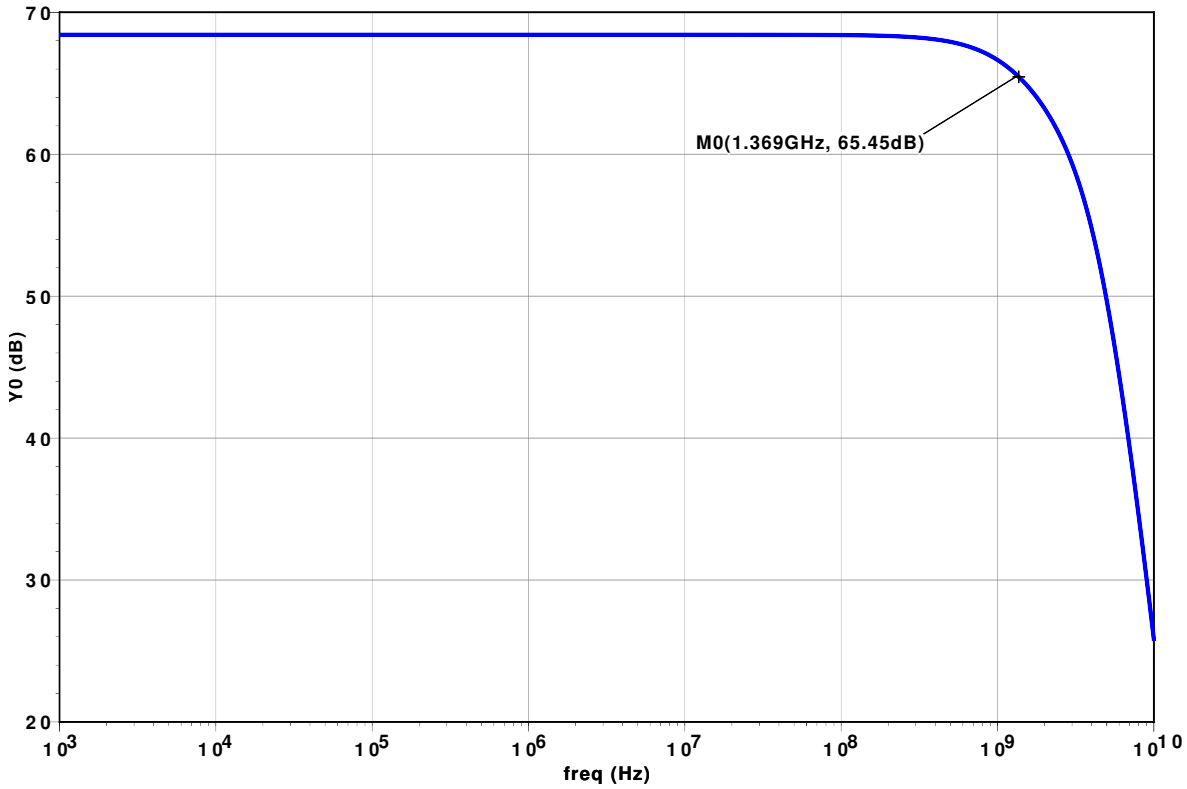


Figure 2.8: TIA Transimpedance Gain.

2.2 Performance Summary And Layout

Performance of the transimpedance amplifier summarized below and the lay out of the complete trans impedance amplifier is given in Fig. 2.9.

Parameters Of Transimpedance Amplifier	Simulated Results
Technology	UMC180nm
Supply Voltage	1.8 V
Transimpedance Gain	68.42 dB
Transimpedance Bandwidth	1.37 GHz
Current Consumption	1.1 mA
Isolation Pulse Width P_{OP1}	5 nS
Input Referred Noise Current Of RGC (from 10MHz To 2GHz)	< 6 $pA/\sqrt{Hz}$
Reflection Coefficient S_{11} (Up to 500 MHz)	< - 20 dB

Table 2.1: TIA Performance Parameters

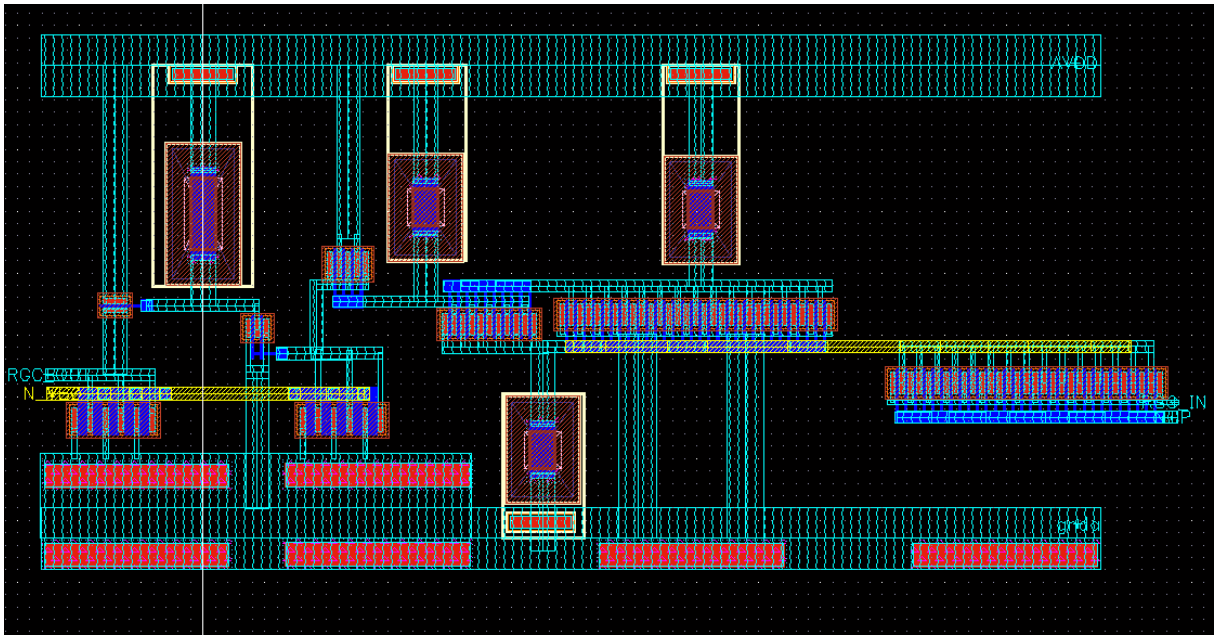


Figure 2.9: Layout Of TIA.

CHAPTER 3

Comparator

Comparator block is the decision making block in the circuit. It amplifies the output of TIA and compares it with a reference threshold to make a decision. Periodic offset cancellation employed to give high accuracy of operation. The output is used to drive a Low Voltage Differential Signaling(LVDS) transmitter circuit.

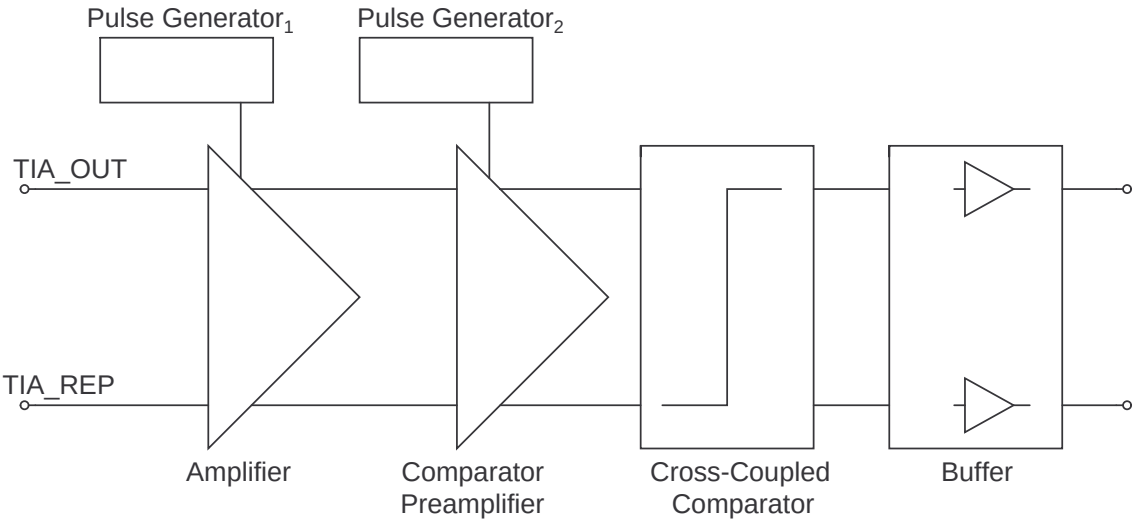


Figure 3.1: Comparator Block Diagram.

Fig. 3.1 shows a block diagram of proposed comparator. Single ended to differential conversion happens at input of comparator block. A replica of TIA is employed to bias differential amplifier's other input so that any variation in output voltage of TIA, other than from input, appears as a common mode signal to differential amplifier. However there would be a finite offset difference between TIA and its replica and this could be even larger than input voltage amplitude. A cross coupled comparator structure is adopted which gives a state 1 on presence of the input and state 0 on absence of the input. A preamplifier is used before comparator to minimize the overall offset effect by a factor of preamplifier gain. The reference signal is combined with the incoming signal at the input of preamplifier by an offset cancellation mechanism. The signal at

the input of cross-coupled comparator will be an amplified version of incoming signal subtracted by reference voltage.

The design of comparator block involves lots of challenges as input signal is very small and can be even less than the amplifier offset. The Offset between TIA and its replica can be large enough such that it can mask smaller inputs from making a switching in the comparator. A proper offset cancellation mechanism has to be employed and cancellation has to be done periodically. Reference is derived from a constant current source as explained in chapter 4.

3.1 Amplifier

The output of TIA should be amplified together with rejection of any common mode signal.A differential architecture adopted for amplifier which has a high common mode suppression and good differential mode gain. Two differential amplifier added in cascade to obtain high gain and lower load to driving stage. Fig. 3.2 shows a single differential amplifier with resistive loads The gate bias voltage of M_0 derived from the reference circuit explained in Chapter 4. The differential mode gain(A_d) and common mode gain(A_{CM}) is given by l

$$A_d = g_{m1}R1 \tag{3.1a}$$

$$A_{CM} = \frac{R_1}{2r_{ds0}} \tag{3.1b}$$

where g_{m1} is the transconductance of transistor M_1 and g_{ds0} is the output resistance of the transistor M_0. As obvious from Eq. (3.1) the differential amplifier can in fact give an attenuation to common mode signal and gain to differential mode signals. The gain can be achieved from a single stage will be small so two of these differential amplifier set in cascade to get a better gain. The band width of a single differential amplifier decided by the resistive loads and the load capacitor. Single stage differential amplifier gives a gain of 16 dB and bandwidth approximately 950 MHz. The total gain of the amplifier is shown Fig. 3.3, with process variation the two stage amplifier gain can vary from 34 dB to 28 dB and bandwidth varies from 500 MHz to 750 MHz.

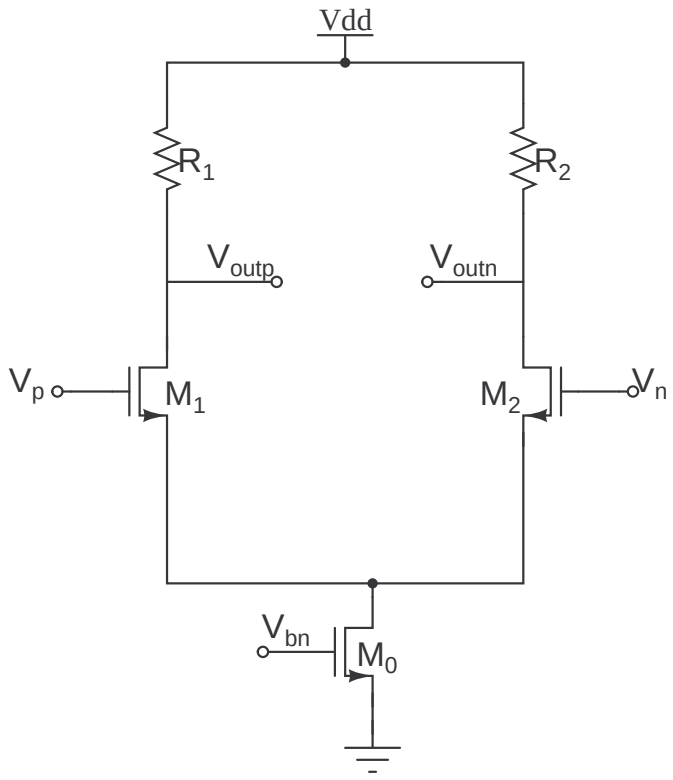


Figure 3.2: Differential Amplifier.

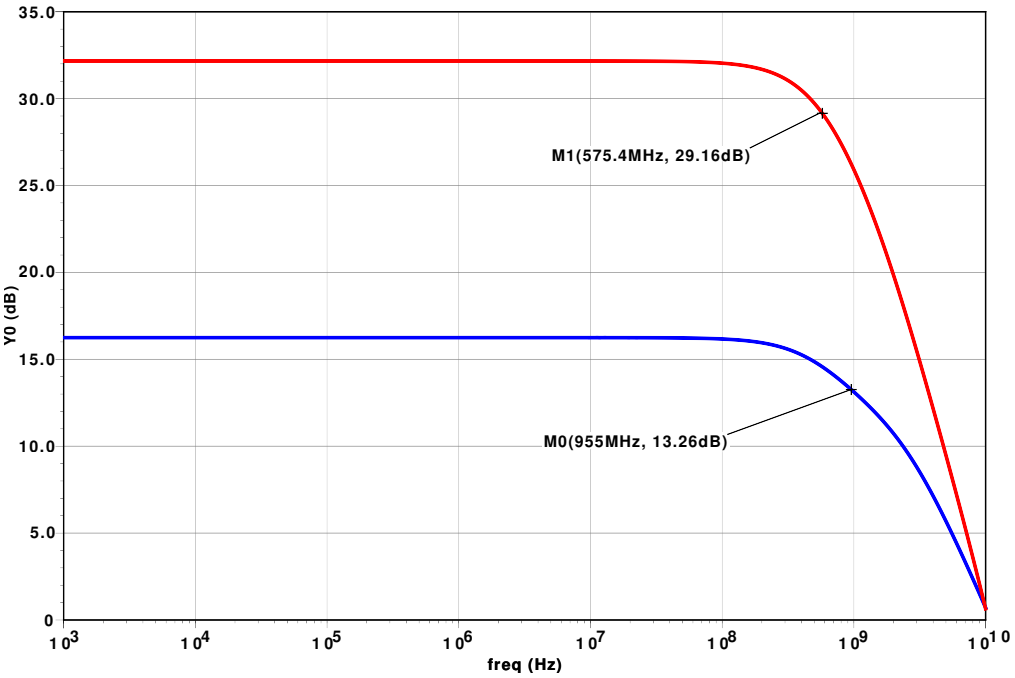


Figure 3.3: Differential Amplifier Gain.

3.1.1 Mismatch And DC Offsets In Differential Pair

Mismatch are two types systematic and random. Systematic can be avoided by proper lay-outing and careful design. All the transistors fabricated will have a finite variation from one to another, all of them will not be identically matched. The random microscopic variation in transistor lay out and variations in doping concentration gives rise to mismatches in mosfets and other components.

Consider MOSFET current equation in saturation region

$$I_D = (\frac{1}{2})\mu C_{ox}\frac{W}{L}(V_{GS} - V_{th})^2 \tag{3.2}$$

For transistors laid out with exact same conditions μ, C_{ox}, W, L, V_{TH} suffers minute variations. As W and L increases the average microscopic variation among the layout structure approaches more close to zero and mismatch decreases. If the transistor is laid down as many parallel transistors the mismatch in length can be reduced as [3]

$$\Delta L_0 = \frac{\Delta L_0}{\sqrt{n}} \tag{3.3}$$

where ΔL_0 is the statistical variation of the length among these transistor with width W_0. For a given W_0 larger the number of fingers smaller will be the mismatch. The variation in V_{TH} and $\mu C_{ox}\frac{W}{L}$ can be quantified as shown in Eq. (3.4) where A_K and A_{VTH} are proportionality constants [3].

$$\Delta V_{TH} = \frac{A_{VTH}}{\sqrt{WL}} \tag{3.4a}$$

$$\Delta \mu C_{ox}\frac{W}{L} = \frac{A_K}{\sqrt{WL}} \tag{3.4b}$$

Consider the differential pair shown in the Fig. 3.2, due to mismatch in M_1 - M_2 and resistors R_1 - R_2 the current splits unequally and cause a across output offset value of $V_{OS,out} = V_{outp} - V_{outn}$. The input referred offset $V_{OS,in}$ is given as

$$V_{OS,in} = \frac{|V_{OS,out}|}{A_v} \tag{3.5}$$

where A_v is the small signal dc gain of the amplifier.

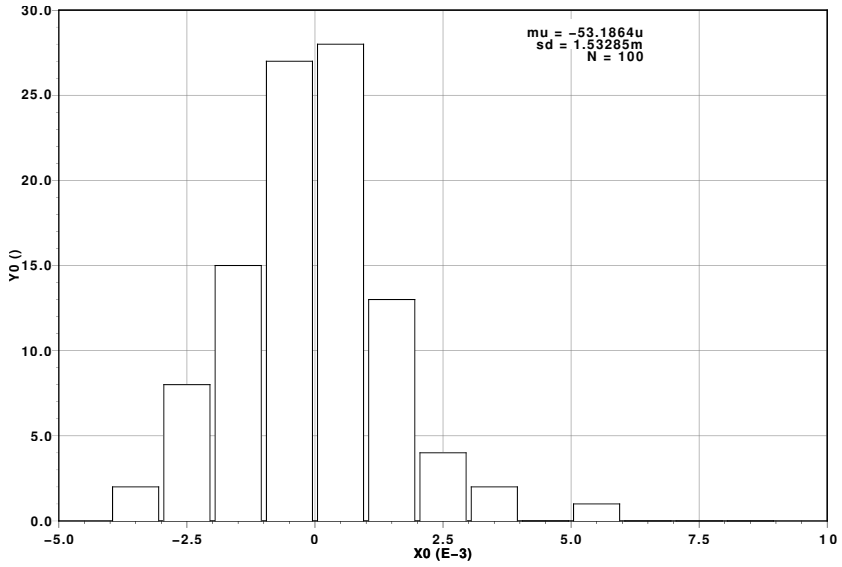


Figure 3.4: Differential Amplifier Offset.

Fig. 3.4 shows input offset voltage variation of a two stage differential amplifier with process and mismatch. It varies from -4.5 mV to 4.5 mV.

3.1.2 Implementing Offset Cancellation In the Circuit

Consider the Fig. 3.1, in the over all block diagram, the TIA output is used to feed the differential amplifier. We have discussed the offset at the differential amplifier input. In the same way the TIA and its replica will have some mismatch between them and as a result there will be a finite amount of offset between them. This offset can also be even greater than the input signal. The offset cancellation circuit discussed above has to be modified to accommodate offset between TIA and its replica.

Consider the circuit in Fig. 3.5, when switches SW_1 and SW_2 are on, the TIA will be isolated from the input. So the Nodes N_1 and N_2 will have its dc node voltage and a finite amount of dc offset in between them. The voltage across capacitor C_1 is $V_{N1} - V_A$ similarly across C_2 the voltage stored is $V_{N2} - V_B$. On normal operation the switches SW_1 and SW_2 are off so voltage at A is $V_{N1} - V_{C1}$ and voltage at B is $V_{N2} - V_{C2}$. The

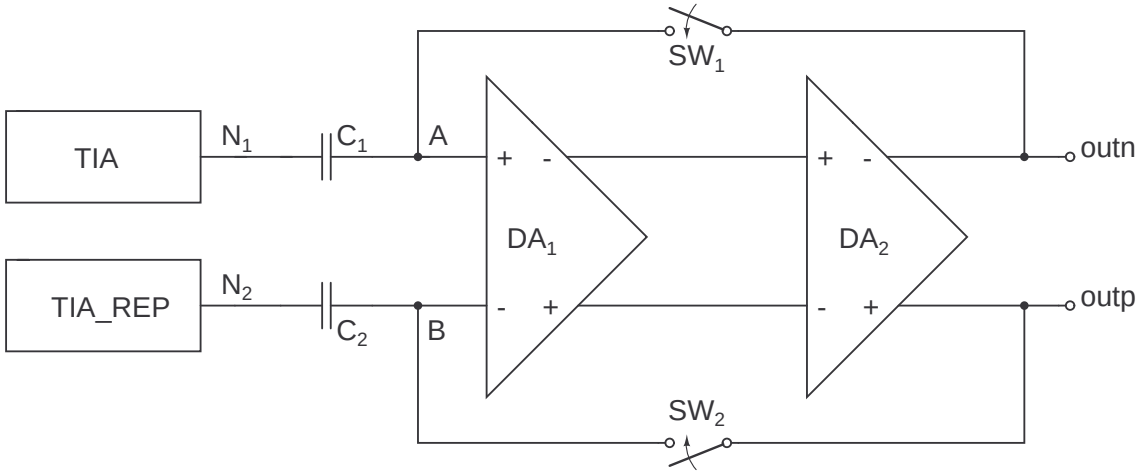


Figure 3.5: Offset Cancellation Of Firststage.

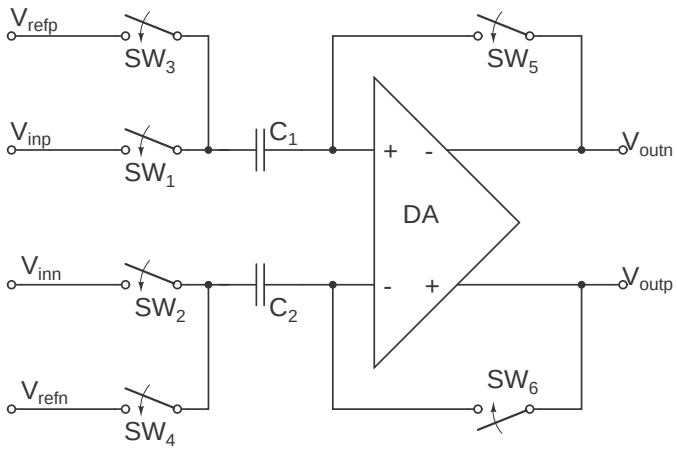
differential voltage across the capacitor is given as

$$V_{C1} - V_{C2} = (V_{N1} - V_{N2}) + (V_B - V_A) \tag{3.6}$$

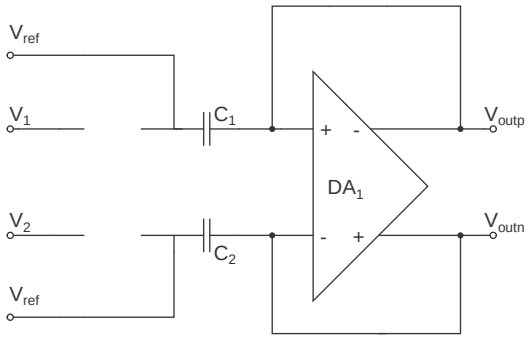
So the capacitors stores offset between TIA and its replica and offset of differential amplifier, differentially, across it.

Offset Cancellation of comparator preamplifier can be done in the same way and we can combine the reference voltage in the same circuit. So offset cancellation not only helps to cancel offset but also provides a very easy way of subtracting reference from the input signal. Now that we have discussed the offset cancellation in detail in the current analysis we assume zero offset in differential amplifier. Consider the Fig. 3.6b is in the offset storage phase when SW_1 to SW_4 are closed the voltage across capacitor C_1 is $V_{refp} - V_A$ and across C2 is $V_{refn} - V_B$. So capacitor stores a voltage $V_{C1} - V_{C2}$ differentially and is equal to $V_{refp} - V_{refn}$ which is the reference voltage. So when SW_1 to SW_4 are open and the circuits operates as an amplifier the voltage between differential amplifier input terminals is $V_{id} = (V_{inp} - V_{inn}) - (V_{refp} - V_{refn})$. So the differential reference voltage is subtracted from the output of differential amplifier.

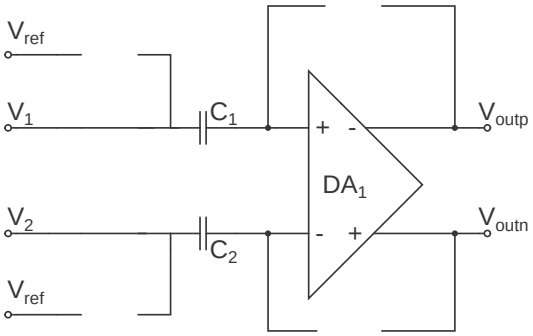
For canceling offset the circuit is isolated from input for a duration of 5 to 10 nS . Any input signal at this instance are totally blocked and cannot reach the comparator. This may cause some signal to go undetected. But the system has 8 parallel channels. Offset cancellation of four channels done at one time instant of time and other four



(a) Offset Cancellation Circuit



(b) Offset Storage Phase



(c) Offset Cancellation Phase

Figure 3.6: Offset Cancellation

channels done at a another time instant. So even if four channels are in cancellation mode the other four channels will be at operational mode.

3.1.3 Circuit Level Implementation Of Offset Cancellation

Fig. 3.7 shows circuit level implementation of Fig. 3.5. The differential amplifier is realized with transistors M_1, M_2 and M_4 and M_5. R_1 to R_4 acting as load to the differential amplifier. The switches SW_1 and SW_2 realized by NMOS transistor. A high signal at NMOS gate turn it on and a low signal at NMOS gate turn it off. The width of pulse CAN1 determines the offset cancellation time period. The two stage amplifier in feedback gives rise to stability issue. To make the circuit very stable a phase margin of 60 $^\circ$ is adopted and to achieve a 60 $^\circ$ phase margin two feedback resistors R_{f1} and R_{f2} added in the feedback path with minimum sized transistors.

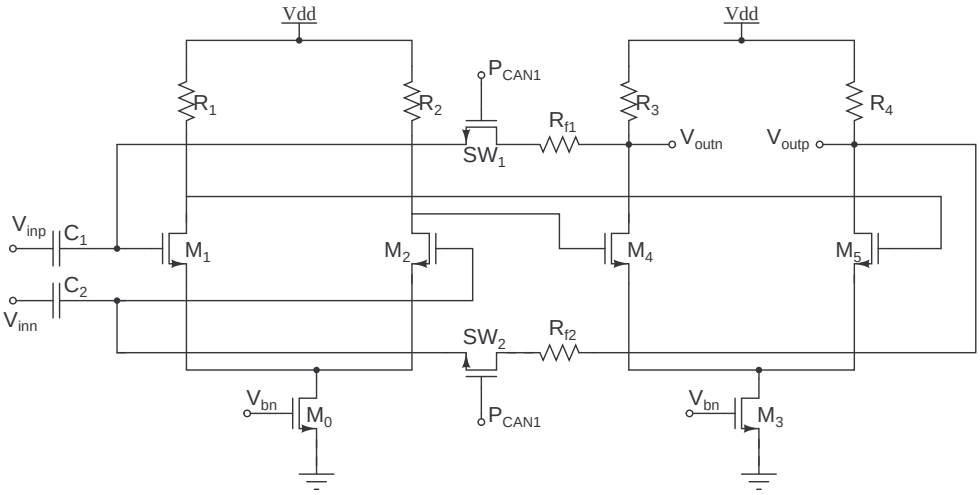


Figure 3.7: Implementation Of Offset Cancellation-1.

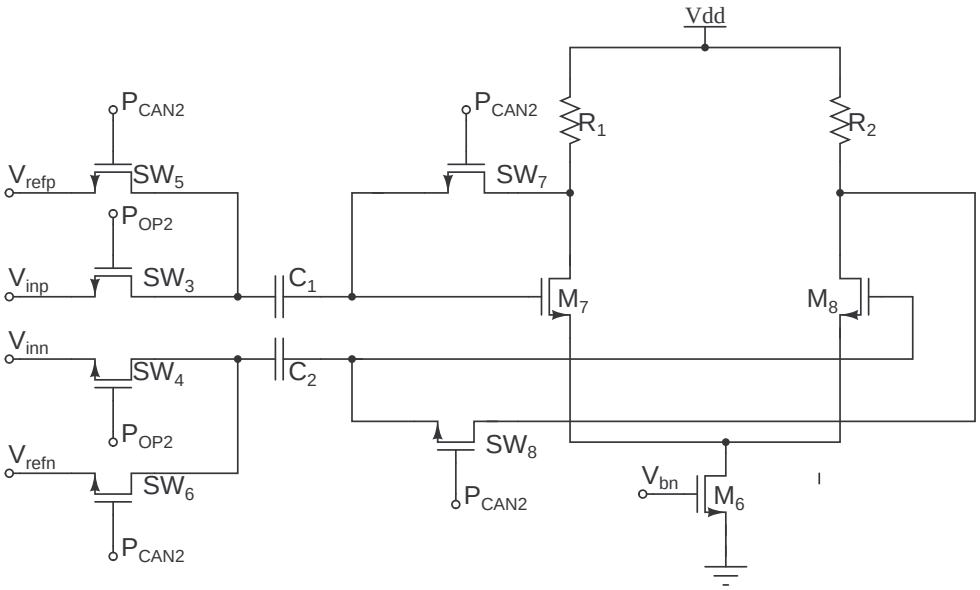


Figure 3.8: Implementation Of Offset Cancellation-2.

Fig. 3.8 is the circuit level implementation of Fig. 3.6a. The transistor M_7 and M_8 forms differential amplifier input pair. Transistor M_6 acts as a current source. R_1 and R_2 acts as loads. Switches SW_3 to SW_8 are realized by NMOS transistors. The pulses P_{CAN2} and P_{OP2} used to turn the switches on and off.

3.1.4 Nonidealities In Implementing Switches

Mosfet in linear and cutoff state can acts as an on switch and off switch respectively. The transistor can be switched from linear to cutoff by controlling the gate voltage. But the transistor will have a finite on resistance in triode region and is given as

$$R_{on} = \frac{1}{\mu C_{ox} \frac{W}{L}(V_{GS} - V_{th})} \tag{3.7}$$

As obvious from the equation the larger the value of $\frac{W}{L}$ smaller will be the resistance and high value of μC_{ox} cause small on resistance . So NMOS transistor becomes a better choice in implementing the switch. In Fig. 3.8, in offset cancellation phase, capacitor C_1 and C_2 are charged through switches SW_5 and SW_6. So the RC time constant will be $R_{on}C_1$ and this should be much much smaller than the offset cancellation interval.

When the gate voltage goes high, transistor will be turned on and a channel is formed from drain to source of the transistor. The channel is formed with accumulated electrons from drain to source . When the gate signal goes low, the transistor goes in to cutoff region and there will be no charge accumulation from drain to source. So when switching the transistor from on to off the accumulated charges are squeezed out through source and drain terminals. So on the instance of turning off a mosfet switch there will be a sudden injection of charges from the mosfet to the circuit. This is called charge injection and it happens not only at turning on but also at turning off, but in the opposite direction.

The crude approximation of amount of charge in the channel charge is given as

$$Q_{ch} = WL\mu C_{ox}(V_{GS} - V_{th}). \tag{3.8}$$

When the transistor turns off a fraction of charges get injected on to the capacitor, the exact amount of charges depends on looking in impedance on both sides. The change in the stored capacitive voltage is given by

$$\Delta V = \frac{Q_{ch}}{C}. \tag{3.9}$$

If the value of capacitance is small the change in stored voltage can be large. Larger the value of capacitor smaller will be the change in voltage, but making capacitance value large, to maintain the same time constant, we might want to increase the width of the transistor which will increase the amount of charge injected.

So changing the value of capacitor and transistor sizes will not give much improvement in the performance. Thanks to the differential architecture adopted in the design, the disturbances appears as a common mode signal and get rejected. The charge injection duration depends on the rise time and fall time of the offset cancellation pulses and will be of the order of few pico seconds . The variation in capacitive voltage due to charge injection will decay very soon to its steady state values as they are constantly connected to supply and has a smaller time constant. The settling time will only be a fraction of offset cancellation pulse width.

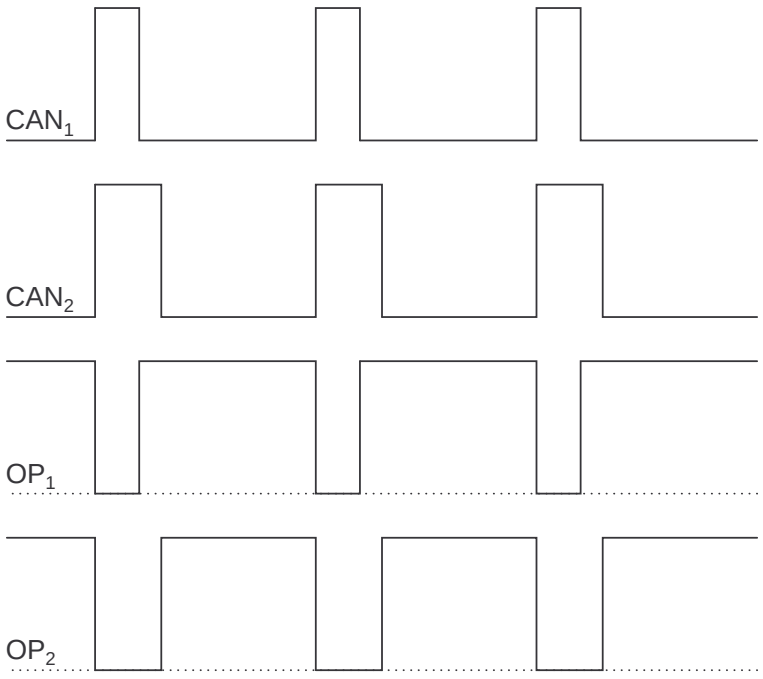


Figure 3.9: Offset Cancellation Pulses.

A more severe problem due to charge injection happens, as shown in Fig. 2.7, when turning on the isolation switch at the input of TIA . Up on turning on the switch a channel is formed in the transistor, the formation of channel need accumulation of electrons which is taken from its drain and source terminal respectively. So in fact the transistor up on turning on draw some current from the TIA circuit. Which is as good

as applying a current input to the ideal TIA circuit. So the circuit will just behave as like it got some current input signals. This leads to false detection which can be avoided by using different offset cancellation pulses for first stage differential amplifier and for preamplifier.

Fig. 3.9 show the offset cancellation pulses. Pulses P_{OP1} and P_{CAN1} are given to first stage offset cancellation circuit Fig. 3.7. When P_{OP1} the transistor M_0 will turn on and produce a current signal. It will have a very short time duration of the order of 100s of pico seconds. It will get amplified by the differential amplifier stage and reaches offset cancellation circuit of comparator preamplifier Fig. 3.8. The preamplifier offset cancellation is done by P_{OP2} and P_{CAN2} pulses which has the same starting point as P_{OP1} and P_{CAN1} but has higher width. By the time this pseudo input reaches preamp, preamplifier will still be at offset cancellation phase and will mask all the signal appearing from the differential stage. So this pseudo input totally get blocked and cannot reach cross coupled comparator.

3.2 Cross Coupled Comparator

Voltage comparator circuit is an analog circuit that will take small analog signal as input and compare with a reference signal and give a high or low signal at the output. When the input signal is less than the reference voltage the comparator will give a low output . If input signal greater than the reference the comparator gives a high at the output. The comparator operation can be summarized as below

$$V_{OUT} = V_{DD} \qquad when V_{in} > V_{ref} \tag{3.10a}$$

$$V_{OUT} = 0 \qquad when V_{in} < V_{ref} \tag{3.10b}$$

Generally a comparator will have three stages. The first stage is the input preamplifier, second stage is the decision making circuit and the third stage is the output buffer stage. The first stage, the preamplifier, is described in the previous section and its offset cancellation circuit subtracts the reference voltage from the input [4]. The buffer stage converts output of decision making circuit to a rail to rail output. This section described

the cross coupled comparator operation which is acting as the decision making circuit here.

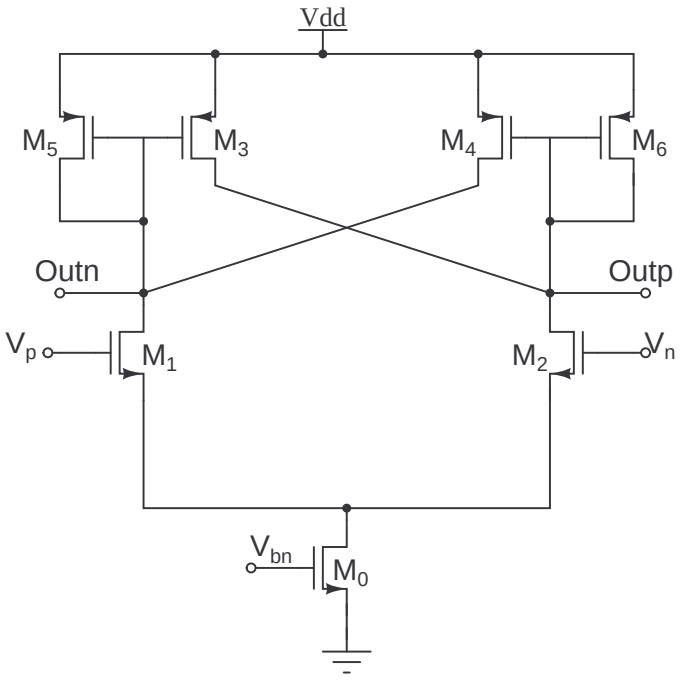
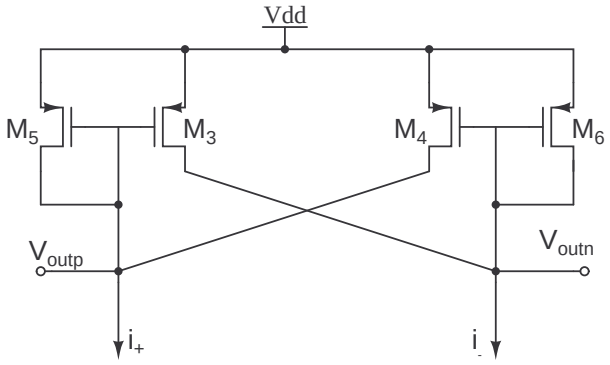
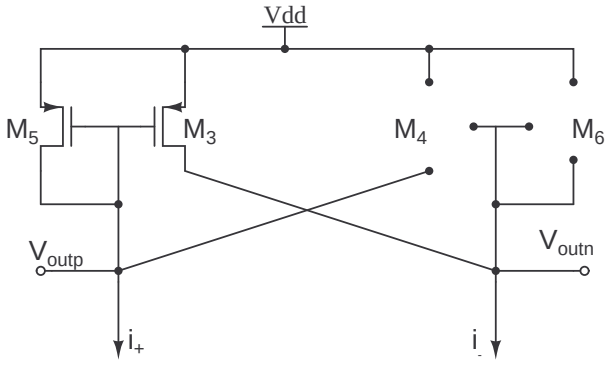


Figure 3.10: Cross Coupled Comparator

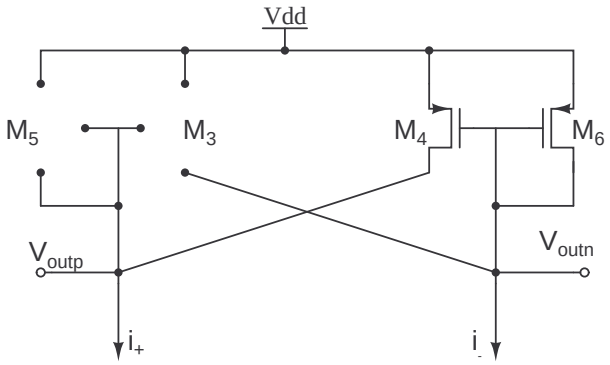
Fig. 3.10 shows the comparator circuit diagram. The gate bias voltage of M_0 derived from bandgap reference circuit described in chapter 4. M_1 and M_2 acts as the input pair of the differential comparator. M_5 an M_6 acting as load. Transistors M_3 and M_4 are cross coupled pairs which offers a negative resistance of value -$\frac{2}{g_m}$ where g_m is the small signal transconductance of the cross coupled pair M_3 and M_4. If the cross coupled impedance offered is greater than the gate-drain connected pair the small signal load resistance will be negative and this feedback eases the switching from one state to another. V_p and V_n are input signal to the circuit which is the output of preamplifier.The preamplifier amplifies the difference between output of amplifier and reference voltage. If reference voltage is lesser than output of opamp the $V_p - V_n$ would be a positive signal and vice verse. When $V_p = V_n$ the cross coupled equivalent circuit will be as shown as in Fig. 3.11a. All the load transistors are on and V_{outp} is same as V_{outn}. The current I splits equally between each branch and $i_+ = i_-$. When $V_p > V_n$ the voltage V_outp will be less than V_{outn} . It will decrease the current through M_4 and increase the current through M_3. If the cross coupled transistors is stronger than the gate to drain connected



(a) OP-AMP



(b) OP-AMP



(c) OP-AMP

Figure 3.11: Feedback Perspective

transistors that positive feed back helps to switch the state faster. Finally the V_{outn} goes to VDD and the transistor M_4 and M_6 are turned off. The Fig. 3.11c shows when V_{outp} greater than V_{outn}.

Consider the Fig. 3.11a the current equations are given as follows

$$i_+ = i_5 + i_4 \tag{3.11a}$$

$$i_- = i_6 + i_3 \tag{3.11b}$$

$$I_s = i_+ + i_- \tag{3.11c}$$

When V_{outp} is high the transistor M_4 and M_6 are off and M_3 and M_5 are on the equation reduces as

$$i_+ = i_5 \tag{3.12a}$$

$$i_- = i_3 \tag{3.12b}$$

Under these condition we can get the value of i_+ from M_5 .

$$i_+ = \frac{1}{2}\mu C_{ox}(\frac{W}{L})_5(V_{DD} - V_{outp} - V_{th})^2 \tag{3.13}$$

Now after changing the input polarity V_{outp} increases and V_{outn} decreases. Eventually V_{outp} increases and turns off M_3 and M_5. The value of i_- immediately before M_3 turned off is given as

$$i_- = \frac{1}{2}\mu C_{ox}(\frac{W}{L})_3(V_{DD} - V_{outp} - V_{th})^2 \tag{3.14}$$

Dividing the equation

$$\frac{i_+}{i_-} - = \frac{(W/L)_5}{(W/L)_3} \tag{3.15}$$

The input voltage V_d can be expressed as

$$V_d = \frac{2}{g_m}(i_+ - \frac{I_s}{2}) \tag{3.16a}$$

$$= \frac{I_s}{g_m}(\frac{2i_+}{I_s} - 1) \tag{3.16b}$$

$$= \frac{I_s}{g_m}(\frac{i_+ - i_-}{i_+ + i_-}) \tag{3.16c}$$

when the circuit is about to switch from one state to another, when M_3 about to turn off

$$V_d = \frac{I_s}{g_m}\frac{(\frac{(W/L)_5}{(W/L)_3} - 1)}{(\frac{(W/L)_5}{(W/L)_3} + 1)} \tag{3.17}$$

So to switch one state to another we need a differential voltage of V_d across it. So to make a transition either $V_p - V_n$ should be greater than or equal to V_d and $V_n - V_p$ should be greater than ore equal to V_d. The amplifier and the comparator preamp give enough gain so that the differential input is greater than V_d.

3.3 Output Buffer

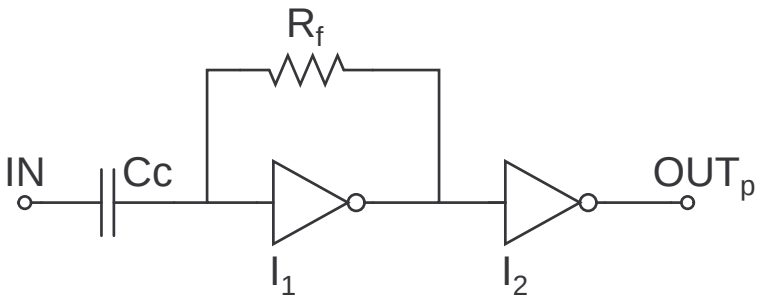


Figure 3.12: Buffer Circuit

The output buffer converts the comparator output to rail to rail signals. The buffer circuit should offer very minimum load to the comparator. The signal output of cross coupled comparator is in between V_{DD} and 0.8 V. The circuit shown in Fig. 3.12 can convert the cross coupled comparator output to a rail to rail signal. The inverter biased at its self biasing voltage by a high resistive feedback connection. The inverter will have high gain at this biasing point. The capacitor C_c decouples inverter dc bias point from comparator dc bias point . The pulse width of the input signal will be very small and it is less frequent. This small width high amplitude pulse appear at the input of inverter I_1 and changes the output of the inverter. The self biasing voltage of the second inverter I_2 will be different from that of first inverter. So that when no inputs are present the output off the buffer should either be at low state or at high state.

3.4 Offset Cancellation Pulse Generating Circuit

In offset cancellation circuits pulses are used to turn on and off switches. Offset correction is done once in every one milli second and has a duration of 5 to 10 ns. Offset

cancellation of first stage amplifier and comparator preamplifier done with different pulses to prevent charge injection from the input isolation switch making a change in the output state. In order to avoid missing input signals at offset cancellation phase offset cancellation of first four channels done at one time and at the next four channels at a different instant of time.

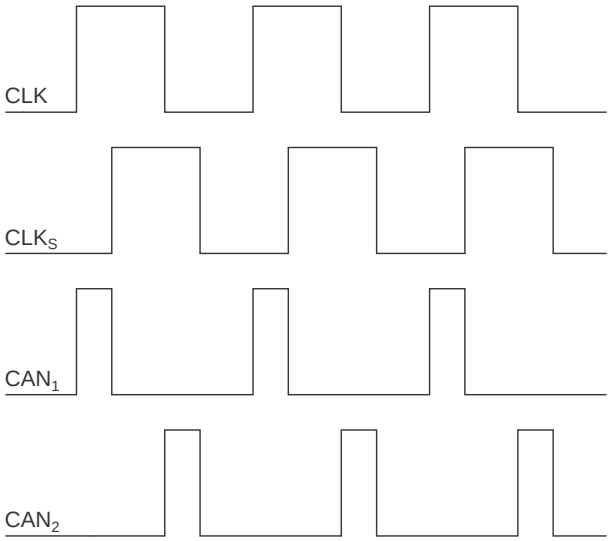


Figure 3.13: Pulses From Clock

The basic idea behind generation of small width pulses from 1 KHz clock is to delay the clock by some small amount of time and make some logical operation with the incoming clock signal and delayed version of clock. Consider the Fig. 3.13 it shows a clock CLK and delayed version of the clock CLK_s. The offset cancellation pulses CAN and CAN_2 can be generated from CLK and shifted version of the clock.

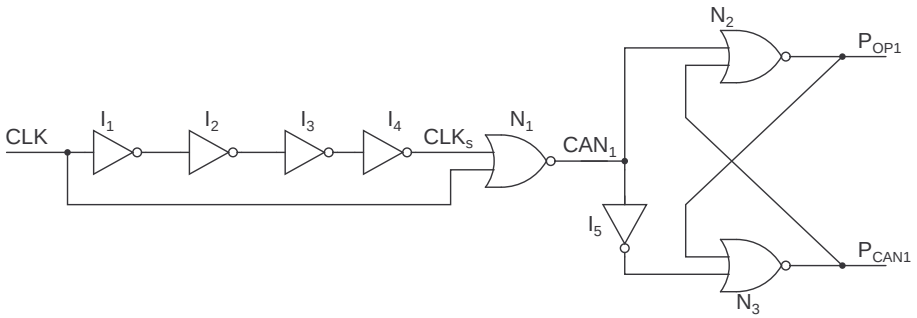


Figure 3.14: Generation of CAN_1

Fig. 3.14 shows generation of offset cancellation pulses P_{OP1} and P_{CAN1} for the first four channels. The delayed version of clock is implemented by adding four invert-

ers, I_1,I_2, I_3 and I_4 in cascade. It generates a delayed version of CLK, CLK_s as shown in figure. The overlapping region of high and low in CLK and CLK_s can be combined via some logical operation to give short duration pulses. The output CAN_1 is given as.

$$CAN_1 = \overline{\overline{CLK} + CLK_s} \tag{3.18a}$$

$$= CLK\overline{CLK_s} \tag{3.18b}$$

A non overlapping pulse generator is used to create P_{OP1} and P_{CAN1} from CAN_1. Similarly the CAN_2 can be generated by the logic operation shown below

$$CAN_2 = \overline{CLK + \overline{CLK_s}} \tag{3.19a}$$

$$= CLK_s\overline{CLK} \tag{3.19b}$$

and its circuit implementation given in Fig. 3.15. The next four channels are done by pulses P_{OP2} and P_{CAN2}

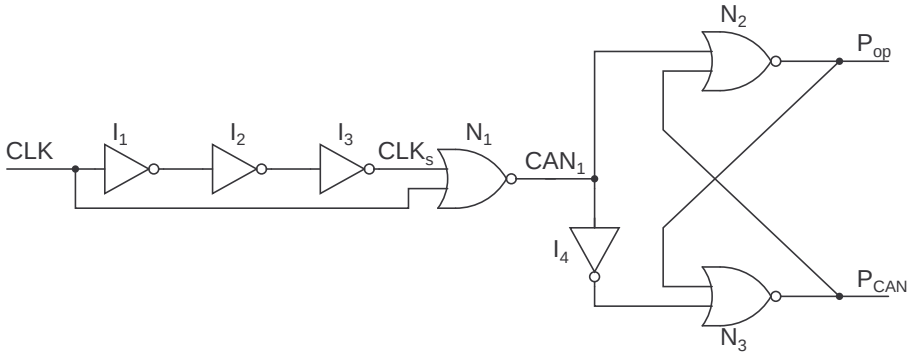


Figure 3.15: Generation of CAN_2

Offset cancellation pulses P_{OP1} and P_{CAN1} is used to cancel offset of first four channels and P_{OP2} and P_{CAN2} are used for next four channels. The pulses generated from these circuits used in offset cancellation of first stage amplifier. To do offset cancellation of preamplifier wider pulses are required and can be generated by increasing the delay amount. Delay can be increased by increasing the transistor length in inverter chain and making them slower.

3.5 Supply Decoupling Capacitance

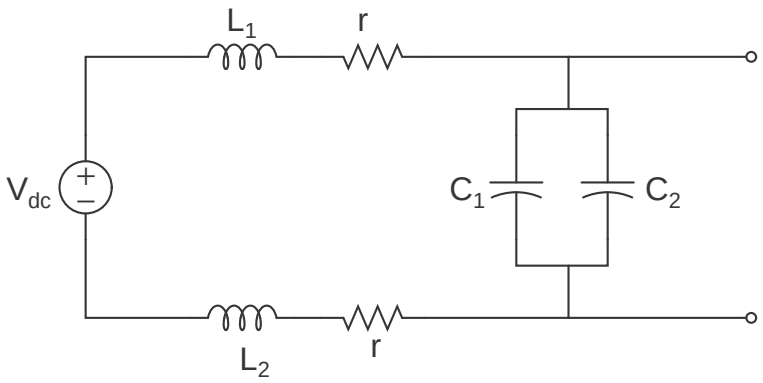


Figure 3.16: Generation of CAN_2

The supply and ground lines in the chip will have certain pad inductance and resistance . Sudden switching currents cause the voltage to drop across the inductor and supply available to the circuits decreases. To avoid this sudden large variations in supply a parallel capacitor is added which acts as a reservoir of charges. A combination of MIM cap and MOS cap with a value of 100 pF together added across the supply and variation is found out to be less than 8 mV.

3.6 Circuit Performance

Parameters Of Comparator	Simulated Results
Technology	UMC180nm
Supply Voltage	1.8 V
Voltage Gain Of First Stage Amplifier	28 dB to 34 dB
Bandwidth Of First Stage Amplifier	500 MHz to 750 MHz
Offset Of First Stage Amplifier	between -4.5 mV to 4.5 mV
Cross Coupled Comparator Rise Time	500 pS
Cross Coupled Comparator V_d	40 mV
Total Current Consumption	8 mA
Offset Cancellation Pulse Width P_{CAN1}	5-7 nS
Offset Cancellation Pulse Width P_{CAN2}	8-10 nS
Reference Voltage	25.12 mV

Table 3.1: Comparator Performance Parameters

CHAPTER 4

Bias Current And Reference Voltage Generator

The current mirroring bias mechanism needs a reference current source which should remain constant irrespective of process,temperature and supply variations. The preamplifier and the crosscoupled comparator are biased by this reference current and variation in the reference current cause degradation in the performance. The comparator compares the incoming signal with a reference threshold and switches the state if incoming signal greater than the reference. This reference voltages will give immunity against unwanted disturbances in the input. The reference voltage is set sufficiently high such that even disturbances which has around 50% of the input amplitude cannot make a change at the output.

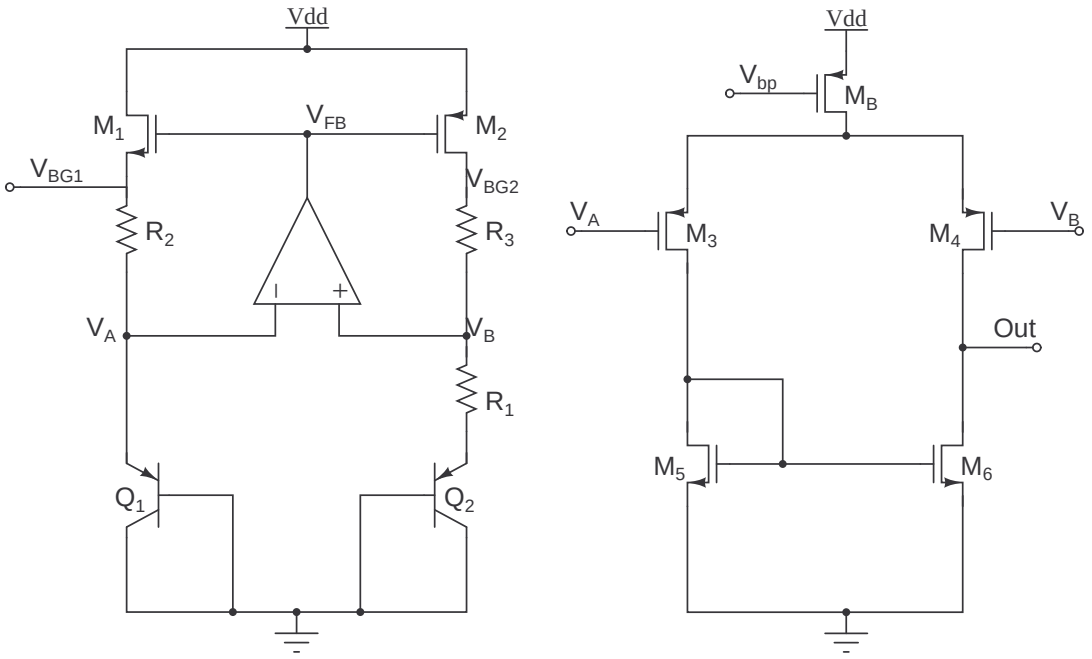
Almost all of the device parameters vary with the temperature so do the node voltages and branch currents. We should bring our attention to completely eliminate or minimize the effects of temperature variations in these references. Change in the temperature changes the device parameters so making the circuit immune to temperature variation will make the circuit very much immune to device variations too.

4.1 Bandgap Reference

Bandgap reference circuit can provide a constant output voltage irrespective of temperature process and supply variations. The basic idea behind bandgap design is to combine two voltage sources which has positive and negative temperature coefficients and add them together with proper weightage so that the effective reference will have a zero temperature coefficient. For example if we have two voltage sources say V_1 and V_2 with positive and negative temperature coefficients and if we can find α_1 and α_2 so that $\alpha_1 \frac{\partial(V_1)}{\partial t} + \alpha_2 \frac{\partial(V_2)}{\partial t} = 0$ we are effectively getting a temperature independent reference $V_{REF} = \alpha_1 V_1 + \alpha_2 V_2$. The name bandgap reference is because at absolute temperature $V_{REF} = \frac{E_g}{q}$ where E_g is bandgap energy of silicon and q is electronic charge.

4.1.1 Circuit Design And Operation

Fig. 4.1a[3] shows the schematic of bandgap circuit. Q_1 and Q_2 are PNP bipolar junction transistors with its collector and base connected to ground. It develops a voltage of V_{BE} across its emitter and collector. The resistors R_1,R_2 and R_3 are made up of same material so the variations to these resistance values will be alike. M_1,M_2 forms a PMOS current mirror, large channel length is used in M_1,M_2 to minimize channel length modulation effects and to minimizes mismatch in mirroring.



(a) Bandgap Reference (b) OP-AMP

Figure 4.1

The temperature coefficient of V_{BE} is given as [3]

$$\frac{\partial(V_{BE})}{\partial t} = \frac{V_{BE} - (3+m)V_T - E_g/q}{T}. \tag{4.1}$$

Eq. (4.1) reveals at a given temperature the V_{BE} has a negative temperature coefficient approximately -1.5 mV/$^\circ K$ at $300^\circ K$. But as evident from Eq. (4.1) the temperature coefficient by itself is depended on temperature so with a constant positive temperature coefficient it is not possible to attain a zero temperature coefficient over wide range of temperature.

Consider two base emitter connected bipolar transistors as in Fig. 4.1a which are not equal on their I_s but operating at the same current, there will be a difference in V_{BE} and is is given by

$$\Delta V_{BE} = V_{BE1} - V_{BE2} = \frac{KT}{q} \ln \frac{I_{s2}}{I_{s1}} \tag{4.2}$$

If Q_2 is created as m Q_1 transistors in parallel I_{s2} will be equal to mI_{s1} and ΔV_{BE} can be written as

$$\Delta V_{BE} = \frac{KT}{q} \ln(m). \tag{4.3}$$

The temperature coefficient of ΔV_{BE} given as

$$\frac{\partial(V_{BE})}{\partial t} = \frac{K}{q} \ln(m). \tag{4.4}$$

Bandgap reference circuit in Fig. 4.1a combines both these negative and postie temperature coefficients and create an overall temperature independent reference voltage. Voltage developed across emitter and collector for the transistor Q_1 is $V_A = V_{BE1}$.An opamp keeps V_A and V_B equal and voltage developed on the resistor R_1 is going to be ΔV_{BE}. The current going through transistor Q_2 is $I = \frac{\Delta V_{BE}}{R} = \ln(m)\frac{V_T}{R_1}$. The upper PMOS pairs acting as a current mirror will mirror the current to other branch of bandgap too. PMOS with higher channel length are used to mitigate short channel effects and resistors R_3 and R_4 keeps the V_{DS} of the M_1 and M_2 the same and minimizes channel length modulation effects. The voltage V_{REF} is given

$$V_{REF} = V_A + IR_2 \tag{4.5a}$$

$$= V_{BE1} + \frac{R_2}{R_1} V_T \ln(n). \tag{4.5b}$$

The resistors are made using same material so they do have same variations with temperature which makes the resistance ratio R_2/R_1 independent of temperature variations. Proper design of $\frac{R_2}{R_1} V_T \ln(n)$ will cancel the negative temperature coefficient from V_{BE} and achieves a zero voltage variation with temperature. As mentioned earlier the negative temperature coefficient by itself is a function of temperature so an absolute zero temperature sensitivity is achieved around room temperature.

4.1.2 OP-AMP Feedback And Compensation

An opamp is used to keep V_A = V_B which helps to create the positive temperature coefficient. The opamp is a single stage differential pair with current mirror load as shown in Fig. 4.1b. The voltage level at the nodes V_A = V_B will be around 650 to 750 mV and using an NMOS differential pair may cause itself to be biased in subthreshold region. So for ensuring operation in saturation region PMOS input pair is used. The transistor M_B is acting as a current source, the bias voltage V_{bp} is generated from another diode connected transistor with resistive load as shown in Fig. 4.4. The current variation in these circuit, to a large extend will not be a matter of concern because over wide range of gain variation the OP-AMP can keep both of its input terminal at the same potential. Fig. 4.2 shows open loop gain of opamp.

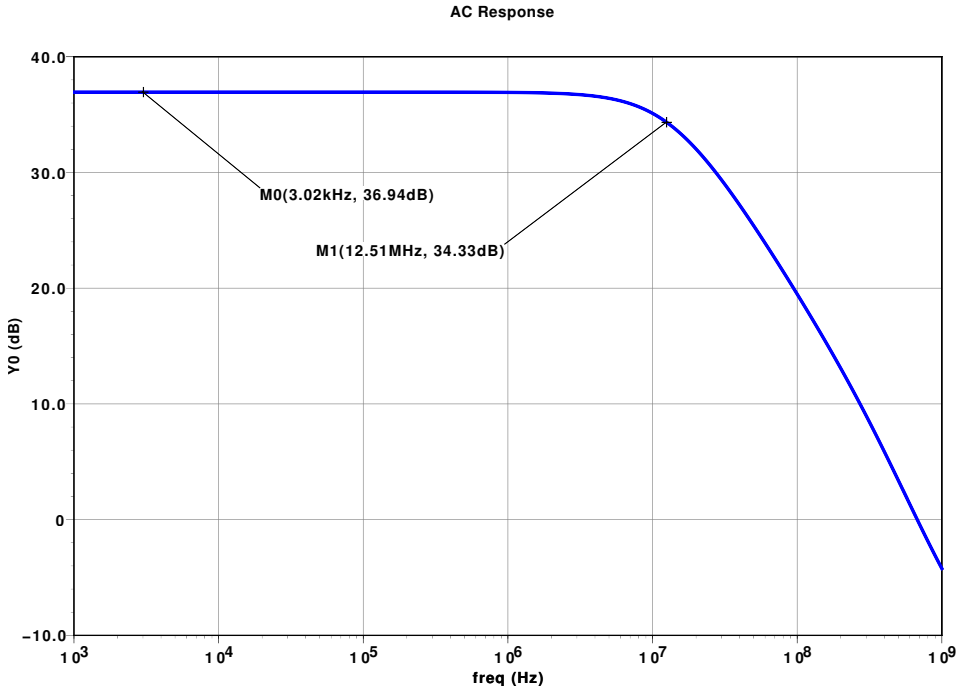


Figure 4.2: OPAMP Gain

Fig. 4.3 shows opamp feedback perspective of Fig. 4.1a. In order to keep V_A and V_B equal opamp should be in a negative feedback. From Fig. 4.3 it is clear that the opamp output is fed back to both of its input terminal. To ensure an overall negative feedback the feedback to the negative terminal(f_n) should be greater than feedback to the positive terminal(f_p) in magnitude. Assuming small signal variation at V_FB, the

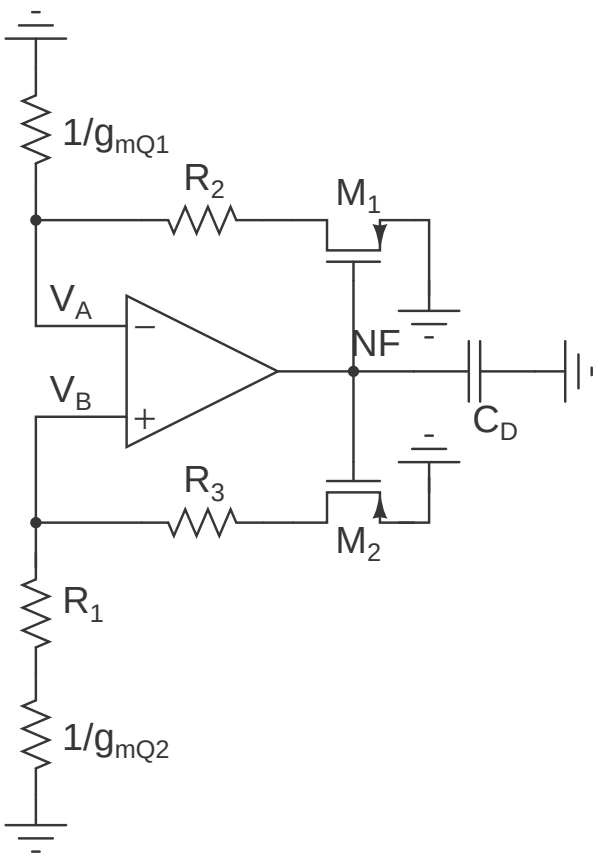


Figure 4.3: OPAMP CMFB

feedback factors to both the terminals are given as

$$f_n = \frac{V_B}{V_{FB}} = -g_{m2}(R_1 + \frac{1}{g_{mQ2}}) \tag{4.6a}$$

$$f_p = \frac{V_A}{V_{FB}} = -g_{m2}(\frac{1}{g_{mQ1}}). \tag{4.6b}$$

Here $|f_n| > |f_p|$ and the circuit establishes an overall negative feedback. The opamp feedback consists of two stages, first stage is the opamp itself and the second stage is half circuit of bandgap core which is equivalent to a common sources amplifier. As it is two stage we should ensure it's stability over operating frequency range and do the necessary compensation to ensure a good phasemargin. A dominant pole compensation method is followed to achieve better phase margin. The dominant pole of the opamp feedback circuit is at the output node and we shift the dominate pole further towards lower frequencies by adding additional capacitance(C_D) at output node as shown in

Fig. 4.3. A phasemargin around 85° is achieved by this compensation method. A high value of capacitance at NF reduces the magnitude of fluctuations but at the expense of recovery time. As disturbances from output happens once in 1 mS we can sacrifice recovery time for attaining lower fluctuations at NF.

4.1.3 Buffer And Reference Voltage Generator

Now we have generated a temperature independent reference voltage. The comparator follows a fully differential architecture and it requires two reference voltages which are apart by a small voltage of 25 mV. We need to derive a constant bias current from this bandgap reference voltage. Directly loading the bandgap circuit will degrade the performance of the bandgap circuit[5] . The buffer circuit shown in Fig. 4.4 achieves both of this requirements. An NMOS differential pair will be a better option because bandgap voltage will be around 1.2 V.

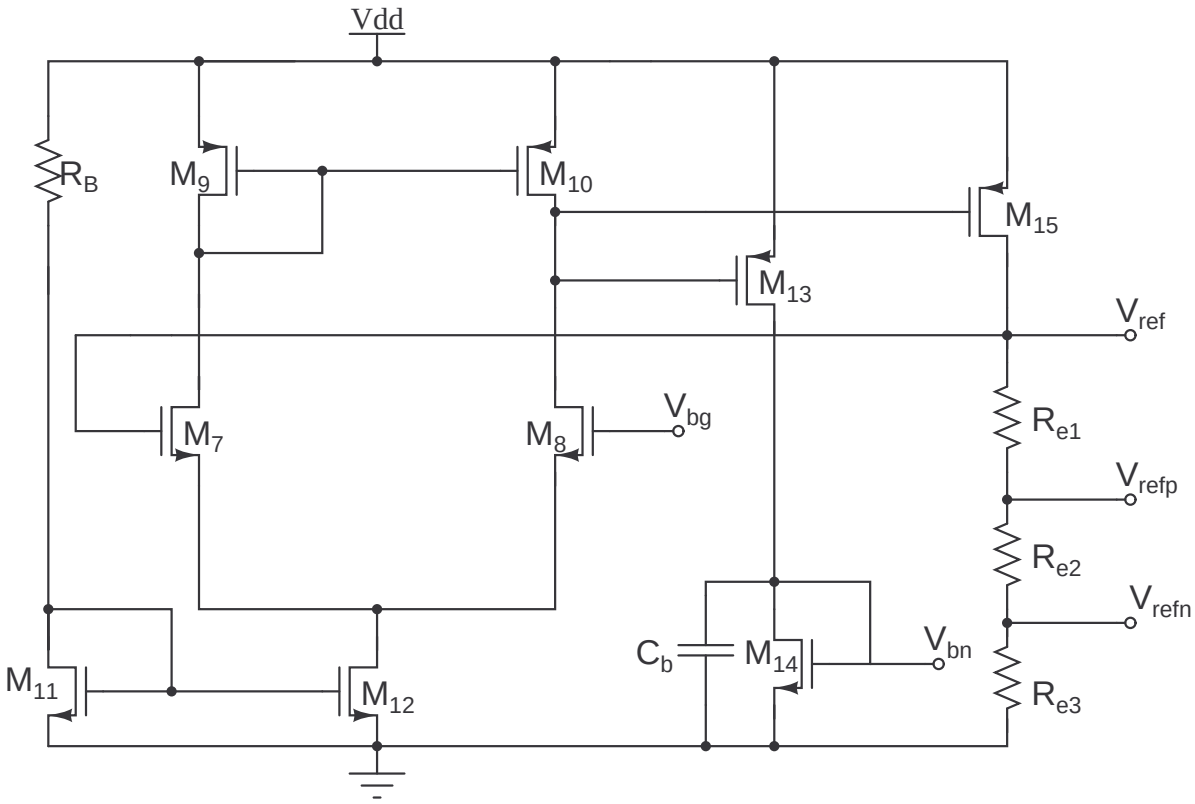


Figure 4.4: Buffer

The buffer circuit is a two stage opamp connected in unity gain feedback. The

output voltage V_{REF} is maintained at V_{bg} by negative feedback and this voltage applied across external resistor keeps constant current through that. $M_7 - M_{10}$ and M_{12} forms the first stage opamp,M_{12} acts as a current source. The gate biasing voltage derived from a drains source connected mosfet M_{11} with a resistive load. The voltage V_{bn} will be very much prone to temperature process and supply variations but the buffer can keep V_{REF} equal to V_{bg}. M_{15} and R_{e1} to R_{e3} forms a common source amplifier and acting as its second stage. R_{e1} to R_{e3} are external resistors which offers a constant load to V_{REF} and therefore a constant current flows through M_{15}. Resistance R_{e3} is used to generate reference voltage, R_{e3} is chosen such that the voltage developed across it is 25 mV. The gate source voltage of M_{13} is adjusted such that it always drive a 100 μA current through M_14. M_{14} is used to supply gate bias voltages to all NMOS current sources used in the design.

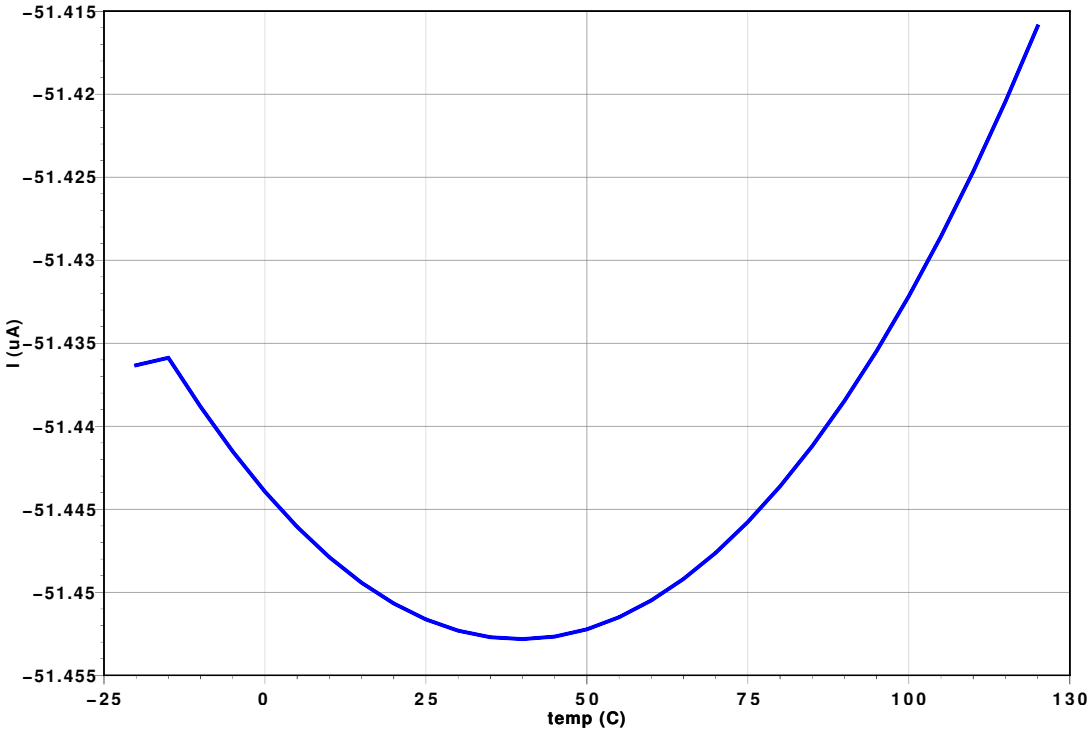


Figure 4.5: Variation Of I_{REF}

V_{refp} and V_{refn} are the reference voltage to the comparator. V_{REF} applied to LVDS to set its common mode output level. The buffer circuit provides reference voltage to a comparator through an offset cancellation circuit shown in Fig. 3.8. A high load capacitance helps not only in reducing the integrated noise($\frac{KT}{C}$) but also suppress all

the distortion from the subsequent offset cancellation stage to the buffer circuit.

Variations of output reference voltage V_{REF} from 0°C to 100°C less than is 5 mV only. Fig. 4.5 shows variation of current with temperature. Variation of $V_{refp} - V_{refn}$ with temperature from 0°C to 100°C the variation is only less than 10 μ V. The variation in $V_{refp} - V_{refn}$ over process and temperature variation is less than 1 mV. By small signal analysis the Power Supply Rejection Ratio (PSRR) is given as

$$\frac{v_{BG1}}{v_{dd}} = (\frac{\frac{1}{g_{mQ1}} + R_2}{R_1})(\frac{1 - A_{dd}}{A})[6] \tag{4.7}$$

where A is vfb/vdiff and Add is pow supply rejection ratio of OP-AMP.

High value capacitors are added across reference voltages V_{refp} and V_{refn} to suppress the variation of voltage due to charge injection from offset cancellation circuit. This will also reduce the effective integrated output noise ($\frac{KT}{C}$) from reference because it is inversely proportional to capacitance value.

4.1.4 Succeeding Stage And Speed of Operation

The reference voltage applied to the comparator through an offset cancellation circuit as shown in Fig. 3.8. The switches are realized with NMOS transistors and they have a finite resistance and injects charge on switching. Due to the charge injection, on every on and off switching it will have some distortion coming inside to the reference setup. It could change the reference voltage level to some extend. But immediately after switching on SW_3 and SW_4 , the offset cancellation circuits charges capacitors C_1 and C_2 and the reference voltage should remain constant over this period. So we need the effect of charge injection minimum and the disturbances should be settled with very little time. A large value of capacitance at the output of the reference make the disturbances minimum but it take a large time to settle. Very small value of capacitance will have smaller settling time but will have large voltage variation. So an intermediate value of capacitance has been chosen for V_{refp} and V_{refn} nodes. From Fig. 4.6 the variation in the reference voltage is less than 1 percentage of the reference voltage. And it recovers very quickly after the opening of SW_2

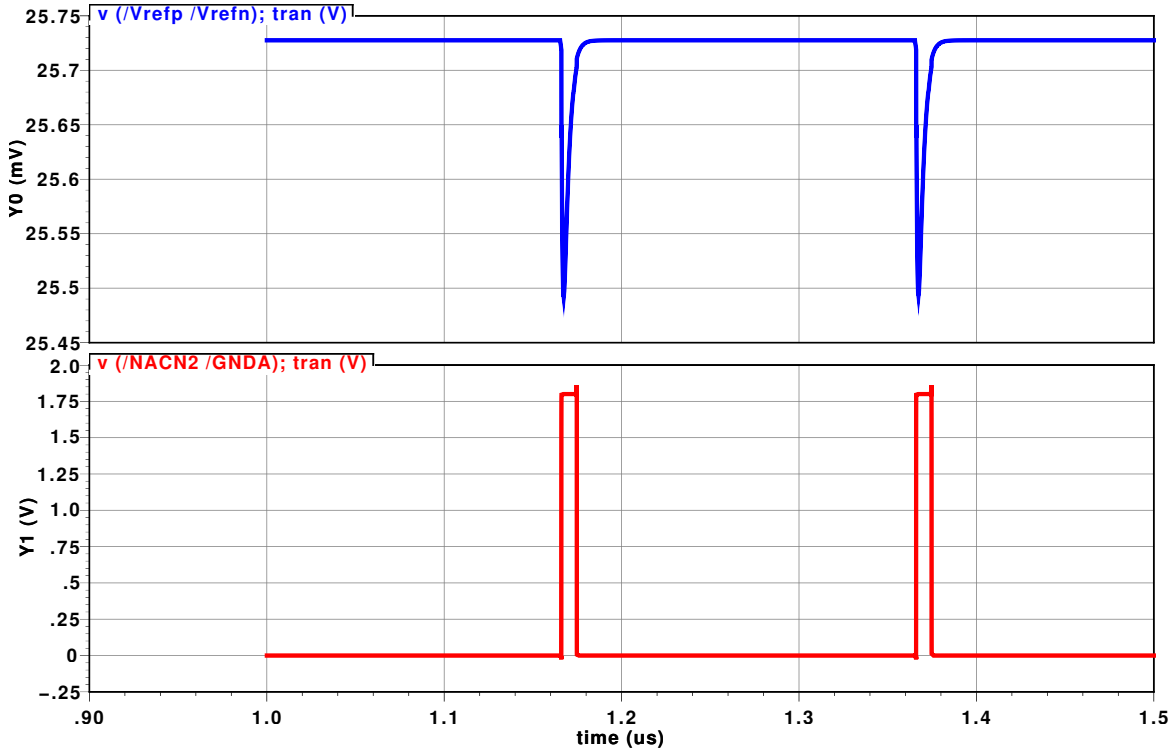


Figure 4.6: Distortion Due To Charge Injection

4.2 Circuit Performance

Parameters Of Comparator	Simulated Results
Technology	UMC180nm
Supply Voltage	1.8 V
Voltage Gain Of Core OPAM	37 dB
Bandwidth Of Core OPAM	12 MHz
Open Loop Gain of Buffer	48 dB
Reference Current V_d	50 μA
Bandgap Voltage	1.26 V
Total Current Consumption	640 μA V
PSRR To Differential Reference	< -50 dB

Table 4.1: Reference Generator Performance Parameters

CHAPTER 5

Low Voltage Differential Signaling

Low voltage differential signaling technique provide a way of high speed chip to chip data transfer at a low voltage and low power consumption. Differential signals are transmitted over two parallel lines and is terminated at the receiver end. The termination resistance has the characteristic impedance of the transmission line. The differential topology gives immunity from supply line variations,common mode voltage variations, coupling and radiated electro magnetic interference and many sources of noise. The circuit should be driving transmission line of impedance 100 Ω, so it can consume a large amount of current for rail to rail signals. But limiting the swing to a relatively lower value reduces the power consumption a lot.

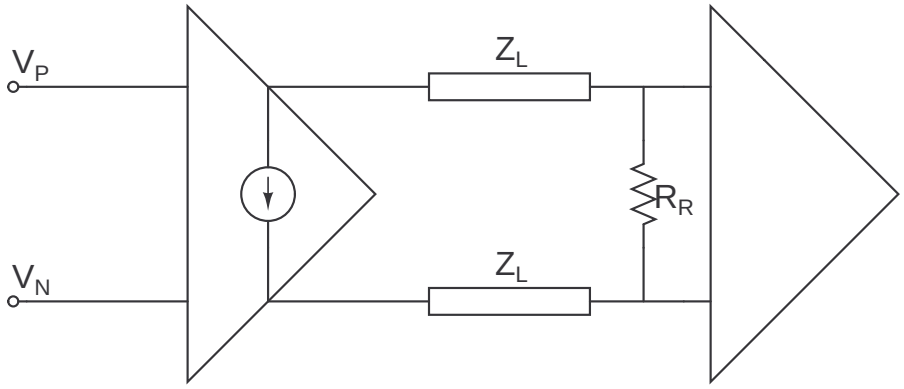


Figure 5.1: LVDS Driver.

Fig. 5.1 shows a point to point topology with single LVDS transmitter and receiver receiver arrangement. It generally works on switched polarity current generator, the load resistor R_R at the receiver provide a good impedance matching and current to voltage conversion. The transmitter is a constant current source that can switch its polarity based on the transmitter input. The transmission lines have characteristic impedance Z_L as shown in figure. The R_T is the is the termination impedance at the receiver side and is of the amount $R_L = 2 * Z_L$. So the looking in impedance as seen by the transmitter is

R_L. The line characteristic impedance is 50 Ω so the effective load to the transmitter is 100 Ω. The circuit pumps a constant amount of current over the load, with alternating polarity based on the input.

5.1 LVDS Standards

Low voltage differential signaling standards [7] are defined by ANSI/TIA/EIA-644 and IEEE 1596.3. EIA-644 defined with an output swing of 350 mV at a speed greater than 400 MHz into a 100 Ω load. LVDS standards are summarized as

$$250mV <= V_{OD} <= 450mV \tag{5.1a}$$

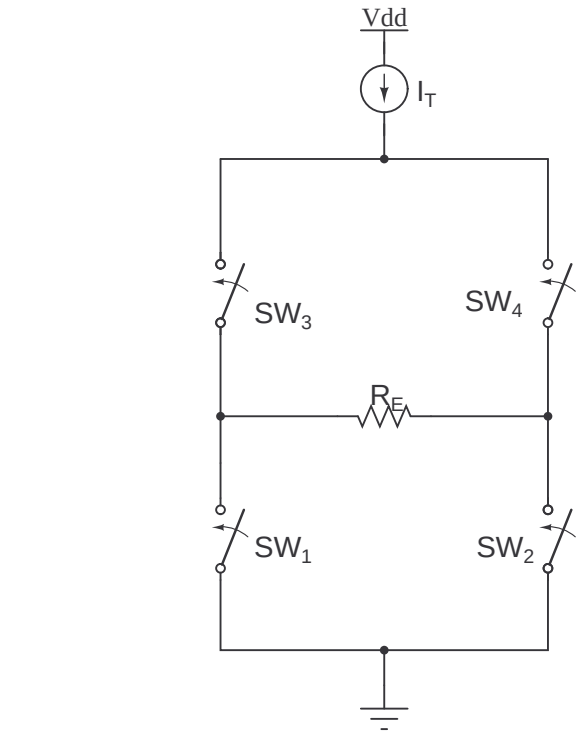
$$1.125V <= V_{CM} <= 1.375V \tag{5.1b}$$

Typically a differential swing(V_{OD}) of 350 mV over a common mode level(V_{CM}) of 1.25 V is well adopted for design.

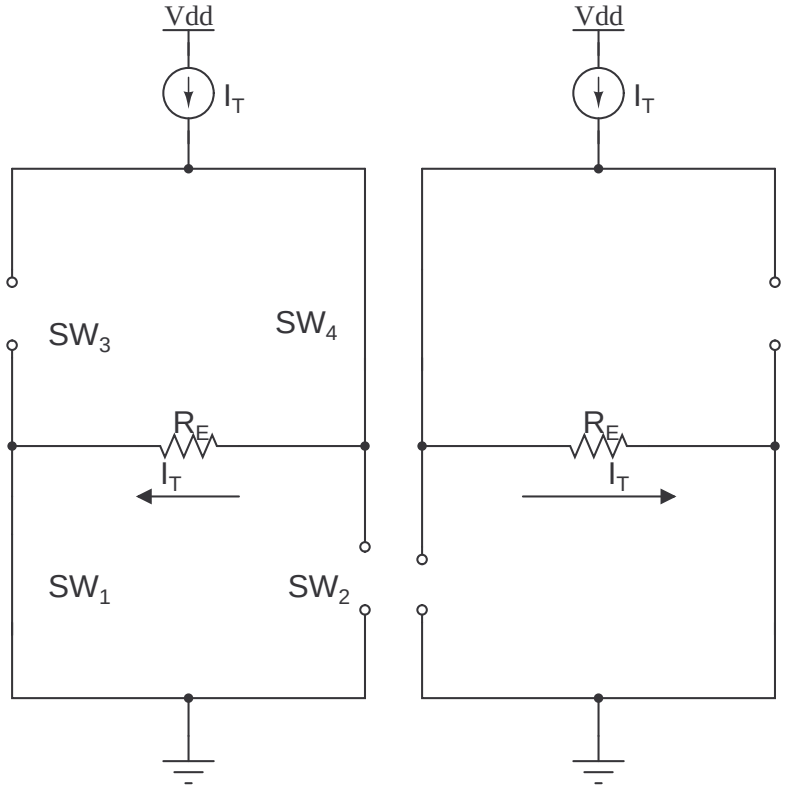
5.2 Bridged Switched Current Source

Fig. 5.2a shows a model of bridged switched current source LVDS transmitter. The current sources CS_1 pumps a current of the value I_T. The core of the circuit is formed by switches SW_1 to SW_4 arranged in bridge configuration. At one instance, when Input_1 is high and Input_2 is low, SW_1 and SW_4 will be on and current will flow through the resistor R_E in one direction as illustrated in Fig. 5.2b. At other instance when $Input_1$ is low and $Input_2$ is high as shown in Fig. 5.2c the current flowing through R_E is at opposite direction. So by changing the direction of current flow through the load the desired amount of signal swing achieved at the output. But the current source always pumps the current through the same direction the switching action in the bridge circuit forces the current to follow opposite paths.

Fig. 5.3 shows circuit level implementation of bridged switched current source LVDS core circuit. The four transistors M_1 to M_4 implements the switches SW_1 to



(a) LVDS



(b) State 1 (c) State 2

Figure 5.2: Bridged Switched Current Source
[8]

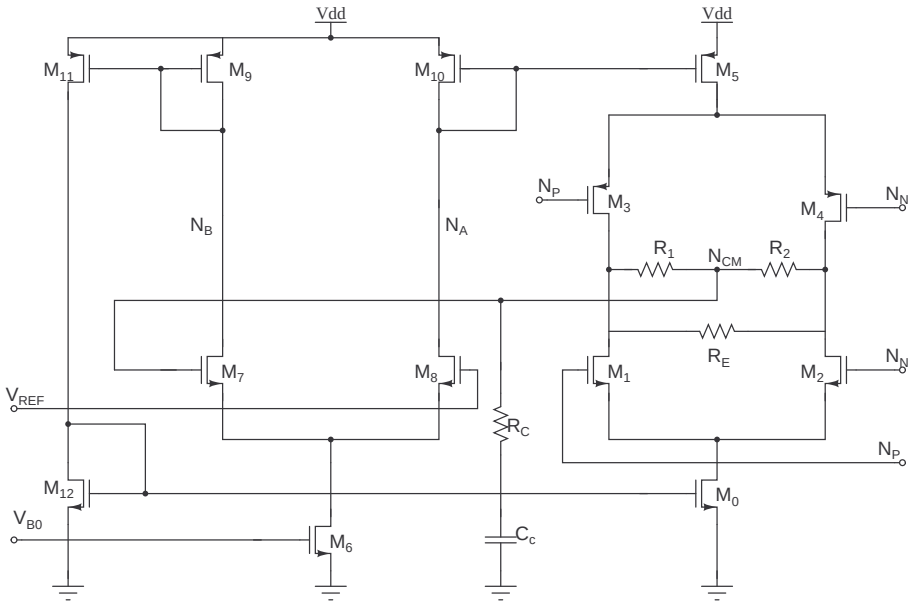


Figure 5.3: LVDS Transmitter.

SW_4. It is arrange in a bridge like configuration such that at any time two of the diagonally opposite switches are on. The transistor M_0 and M_5 acts as current sources that drives and sinks a constant current I_T respectively. using two current sources helps to implement a common mode feedback and keeps the output voltage at constant level. Signals V_P and V_N are the inputs, they are complementary to each other. When V_P becomes high transistor M_1 turned on and transistor M_3 turned off. The low value at N_N turns on M_4 and turns M_2 off , so current flows through the R_E and develops a voltage across the load. When V_P is high and V_N is low the current direction get reversed but magnitude of the current will be the same.

5.2.1 Common Mode Feedback

The $R_1 - R_2$ resistors forms a resistive divider and detects a common mode voltage. The sensed common mode voltage compared with a reference voltage and the feedback mechanism keep the current and common mode output level constant. The reference is generated from a bandgap reference circuit and will have a value about 1.2 V. Fig. 5.4 shows the circuit when M_1 and M_4 are turned on.The transistor M_6 has a base bias voltage V_{B0} and it generates a current I_0 in M_6 by current mirroring mechanism. Half of I_0 passes through M_9 and M_10 and it is mirrored to M_5 and M_11. The mirroring should

be such that current driven by M_5 is I_T. Similarly current in $M_1 1$ flows through $M_1 2$ also and that current is mirrored to M_0 and that should also be I_T. If there is a mismatch between these two currents , pumped by M_0 and M_5 , the voltage at NCM changes. When the common mode voltage,voltage at $N_C M$, increases and is greater than the reference voltage the voltage at NA increases so the V_{SG} across M_5 decreases and the current decreases and the common mode voltage V_{CM} decreases. So this feedback action keeps the output common mode voltage to V_{REF}. It keeps the balance between common mode voltage level and the switching current through the circuit. The common mode feedback stabilizes the current to I_T and the common mode voltage to V_{REF}. For a 350 mV swing the current I_T should be $I_T = \frac{V_{OD}}{R_E}$ where R_E is the effective load impedance and its value is 100 Ω so I_T is chosen as 3.5 mA.

These transistors will have finite on resistance and will be different for PMOS and NMOS. The transistor M_1 and M_5 creates a path for the current flow. The circuit now can be viewed as a two stag amplifier with feed back. The circuit is now two stage and it is in feed back so we have to closely examine the stability of the circuit. If the feed back is on the verge of instability or in instability the feedback action won't take place

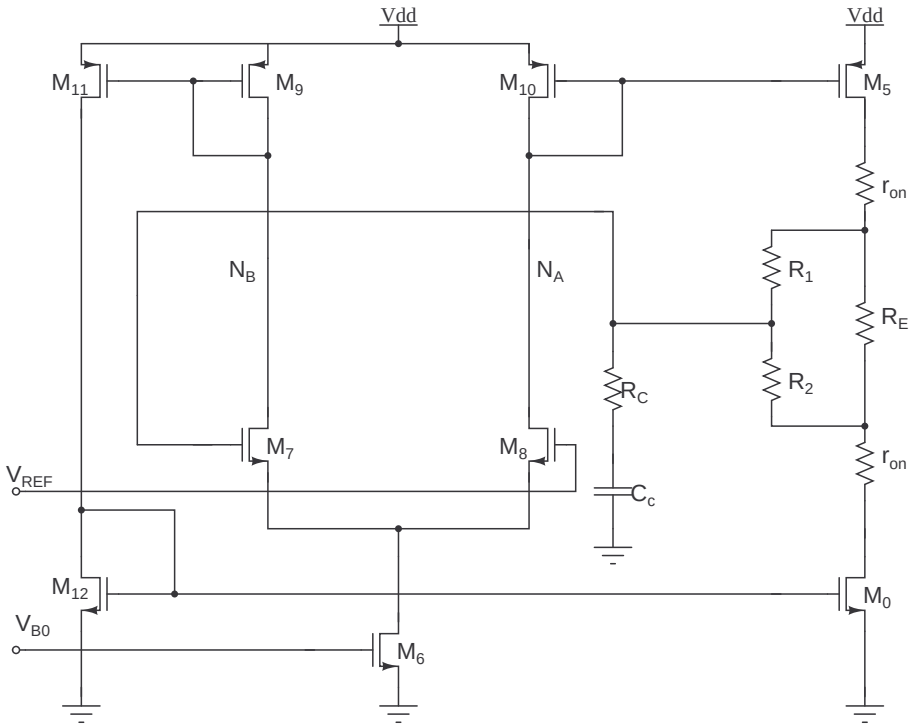


Figure 5.4: LVDS Common Mode Feedback.

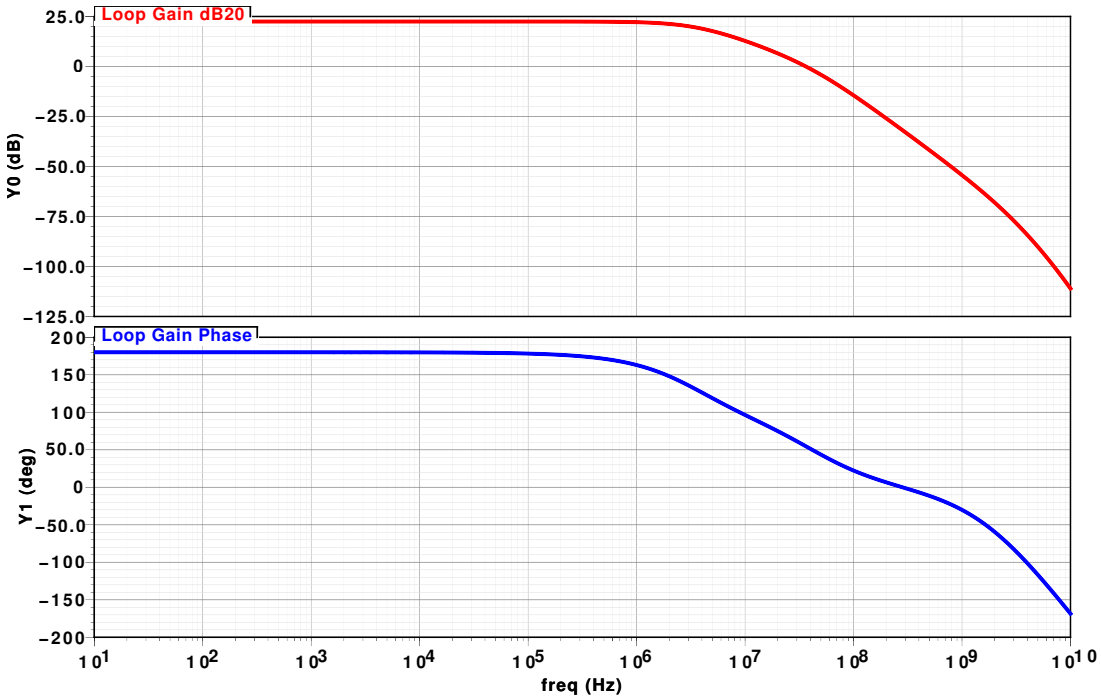


Figure 5.5: LVDS CMFB Gain And Phase.

and circuit will not be able to maintain its common mode level. The open loop gain and phase of the LVDS common mode feed back is shown in Fig. 5.5. The feedback has a gain of 24 dB, bandwidth of 3.5 MHz and a phase margin around 56° which is enough to stabilize the bias current and common mode voltage level. The variation of phase margin over process and mismatches analyzed using Monte-carol simulations and a standard deviation of 4 found with a sigma value 3.

5.3 Circuit Performance

Parameters Of LVDS	Simulated Results
Technology	UMC180nm
Supply Voltage	1.8 V
Drive Current	3.5 mA
Bandwidth Of CMFB	12 MHz
Open Loop Gain of CMFB	48 dB
Total Current Consumption	6 mA V
LVDS Rise Time (With a 2.5 pF Load)	800 pS

Table 5.1: LVDS Performance Parameters

CHAPTER 6

CONCLUSIONS

A high speed front end detection system is designed for India based neutrino observatory. It is designed and simulated in UMC180nm technology. Layout of first block of the design completed and tested for design rule and lay out verses schematic match. The system can detect input current pulses as small as 1 μA over an temperature region 0 to 100° C.

Eight parallel channels has been established and each channel consist a transimpedance amplifier, comparator and a LVDS driver. Differential architecture is followed in the design to get better supply and noise rejection. Comparator reference signal and current mirror bias reference generated internally. Offset cancellation done at a period of 1 KHz in an interleaved manner. Global offset cancellation adopted for a two stage differential amplifier to achieve high gain and make the offset cancellation more effective. Input impedance matched to incoming 50Ω line over a wide range of frequency and temperature variations. LVDS transmitter drives the output transmission lines terminated at a load of 100Ω.

The channel has 1ns total delay and a power consumption of 28 mW per channel. Decoupling capacitor of 100 pF added per channel to avoid sudden variation in supply voltage because of switching. One high precision reference circuit is used to generate reference current for biasing and comparator reference threshold and supplied to all channels. Two pulse generation circuit also implemented and used for offset cancellation of four channels at a time.

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