DESIGN OF GATE DRIVE CIRCUIT FOR IGBT WITH SHORT CIRCUIT PROTECTION

A Project Report

submitted by

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THESIS CERTIFICATE

This is to certify that the thesis titled **DESIGN OF GATE DRIVE CIRCUIT FOR IGBT WITH SHORT CIRCUIT PROTECTION**, submitted by **N.RAMESHBABU** , to the Indian Institute of Technology, Madras, for the award of the degree of **Master of Technology**, is a bonafide record of the research work done by him under our supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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ABSTRACT

KEYWORDS: gate drive;short circuit;protection;buck converter;inverter;

Insulated Gate Bipolar Transistors(IGBTs) are widely used in high power drive systems, it will capable of blocking high voltages when OFF, and passing high currents when ON. IGBTs are sensitive to voltage and current stresses. Gate driver circuit is required for IGBT. A gate drive scheme is investigated which realizes low-noise, without an excessive increase in switching losses, and capable of protection of IGBTs against short circuit conditions. Isolated power supply is generated by flyback converter to drive high and low side switches. Gate drive circuit is designed, which uses MIC 4425 as driver for high voltage applications. Identification of fault current during the operation of a IGBT and activation of suitable remedial actions are important for reliable operation of power converters. A gate drive circuit capable of protecting the IGBT against short circuit conditions by sensing the switch collector-emitter voltage has been developed. For evaluation of this gate drive circuit against short circuit condition, primarily buck converter is designed. This thesis deals with the development and implementation of a three-phase 1KVA IGBT inverter to evaluate the gate drive circuit. The Sinusoidal Pulse Width Modulation SPWM control scheme is implemented in digital platform and gating signals are applied to the inverter through the gate drive circuit. The inverter design incorporated a laminated sandwich busbar structure to reduce stray inductance. Experimental tests are carried out to evaluate the performance of the gate drive circuit.

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CHAPTER 1

INTRODUCTION

Insulated gate bipolar transistor (IGBT) devices play a major role in power applications due to their high current, voltage capability. Driving these devices in medium or large power applications requires separate high and low side drivers with insulation. IGBT requires power for turn-on and turn-off stages, at turn-on, the positive gate current is necessary to charge the IGBT input capacitance to create an electron channel between collector and emitter. At turn-off, a negative gate current is necessary to discharges the IGBT input capacitance for removing the electron channel. The threshold gate voltage of the IGBT is around 4 V, but to ensure switching ON and OFF of the devices at higher frequencies, the gate voltage range is between +15 V and 15 V. The gate resistor R_G controls the IGBT gate current and collector current slope. Power supply is required to drive the driver and protection circuit ICs. For driving the IGBTs in inverter applications, gate drive circuit needs isolation supply. Flyback converter is designed to provide isolation supply for gate drive circuit.

Control and protection functions are also required to ensure reliable operation of the gate drive circuit. The gate driver circuit has to minimize switching losses, limit di/dt and dv/dt, peak reverse recovery current at turn-on and voltage overshoot at turn-off. Short circuit and over current are severe fault conditions that can result in failure of the IGBT if appropriate remedial action is not taken. Short circuit results in high current causing rise in the junction temperature of the device, which eventually destroys the device. In this thesis, a suitable gate drive circuit is designed with shoot through protection. The protection circuit senses the collector-emitter on state voltage and during the short circuit conditions, gate signals are deactivated. Protection circuit has the advantage that the current is always monitored. This is a simple and low cost over-current detection circuit. In high power converters, the design of the gate drive circuit strongly influence the switching behavior and losses.

The gate drive circuit is evaluated for IGBT in chopper and inverter mode of operation.

1.1 Objectives

The scope of the project is the design of gate drive circuit. The project is focused on evaluation of the gate drive circuit using inverter and buck converter. The objectives are

1. Design and implementation of gate drive circuit
2. Design and implementation of buck converter
3. Design and implementation of three phase 1KVA three phase inverter
4. Evaluation of the gate drive circuit

1.2 Organization of Thesis

Chapter 2 presents about the dynamic characteristics and switching losses of the IGBT, necessity of isolation power supply, flyback converter and hardware implementation of gate drive circuit with short circuit protection were discussed.

In **Chapter 3** presents design of buck converter and inverter with sandwich busbar arrangement.

Chapter 4 presents evaluation results of the gate drive circuit.

Chapter 5 presents conclusions and future scope of the work.

CHAPTER 2

GATE DRIVE CIRCUIT DESIGN

The Insulated gate bipolar transistor (IGBT) devices are used as power switches in high power drive applications. The power devices used in power power electronics applications need to turn-on and turn-off fast to minimize the switching losses. The drive circuit should have a high performance to drive the IGBT. This chapter explains about the switching characteristics of the IGBT and design of gate drive circuit.

2.1 Insulated gate bipolar transistor (IGBT)

IGBT is a hybrid device which combines the advantages of MOSFET and BJT. The IGBT has fast switching capability of the MOSFET and is capable of handling the high currents like a BJT. IGBT is a voltage controlled bipolar device, has a lower on-state voltage drop and are capable of blocking higher voltages. IGBT is approximately modeled as PNP transistor driven by n-channel power MOSFET as shown in Figure 2.1. This approach is useful to explain the turn on and turn off characteristics of IGBT.

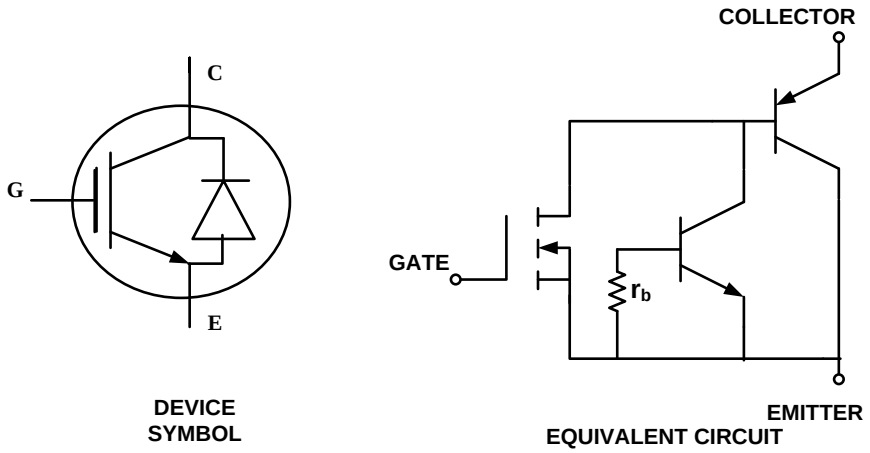

Figure 2.1 IGBT device symbol and equivalent circuit

To turn a BJT on and off quickly, the gate current driven hard in each direction to move the carriers into and out of the base region. When the gate of the MOSFET

is driven high, it provides base current for the transistor. This turns that transistor on quickly, collector current begins to flow faster when gate is driven faster. The turn off scenario is a bit different. When the gate of the MOSFET is pulled low, there is no current path for the base current in the BJT. The lack of base current begins the turn off process. however, for a fast turn off, current should be forced into the base terminal. There is no mechanism available to sweep the carriers out of the base, so the turn off of the BJT is relatively slow. This leads to a phenomenon called tail current since the stored charge in the base region must be swept away by the emitter current [6].

2.1.1 IGBT I-V Characteristics

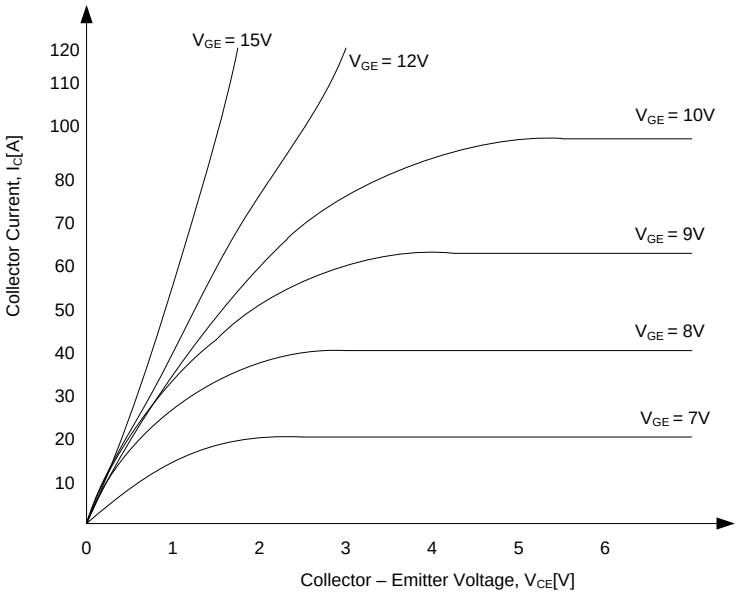

Figure 2.2 IGBT I-V Characteristics

The I-V characteristics of an n-channel IGBT are shown in Figure 2.2, for different values of V_{GE}. In the forward direction IGBT I-V characteristics are similar to those of a logic-level BJT expect that the controlling parameter is input voltage V_{GE}, rather than the input base current. Since the IGBT is basically a MOSFET, the gate-emitter voltage controls the state of the device. When V_{GE} less than a certain voltage which is called threshold voltage, there is no inversion layer created to connect the collector from the emitter hence, the device is in the off state. When V_{GE} exceeds the threshold value, the IGBT is turned to the on-state.

2.1.2 Turn-on switching Characteristics

As shown in the Figure 2.3, during the delay time $t_{d,on}$ the gate current charges the input capacitances C_{GC} and C_{GE} through the gate resistance R_g, then gate-emitter voltage increases to the threshold voltage $V_{GE,th}$ of the device. Beyond this time the collector current starts to increase linearly until it reaches to the full load current. Due to the reverse recovery of diode few amperes peak current is added to the collector current i_C. During the time when collector current is equal to the load current, the voltage V_{GE} is first kept constant and at this moment the collector current flows through C_{GC} only, that causes the voltage V_{CE} decreases to the on-state voltage $V_{CE(sat)}$. After this moment the voltage V_{GE}starts to increase until it reaches to full gate to emitter voltage [6].

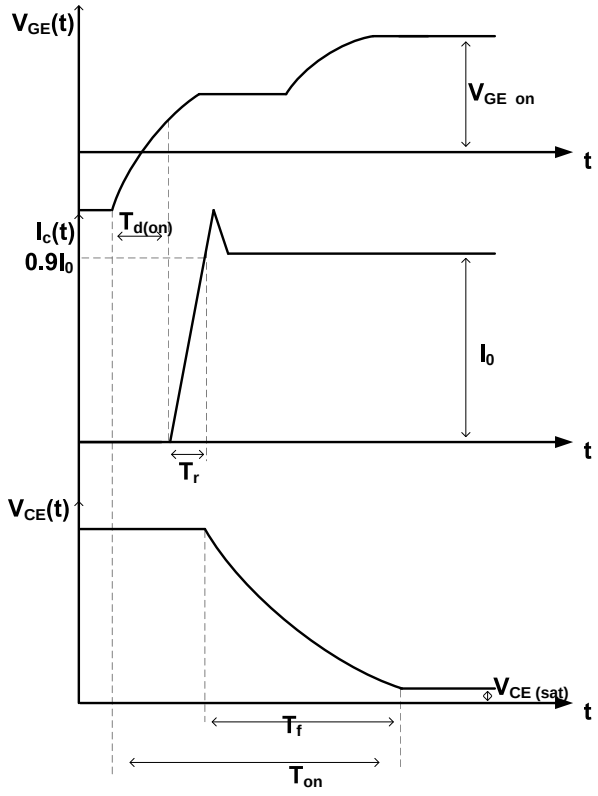

Figure 2.3 Turn On Characteristics

Turn-on switching losses are the amount of total energy losses during turn-on time of the device. It is normally measured from the point where the collector current starts to flow to the point where the collector-emitter voltage drops completely to zero. The

turn-on energy loss calculation is given by the equation below.

$$E_{loss}(on) = \int_0^{ton} \left[V_{ce}\left(t\right) i_c\left(t\right)\right] dt \tag{2.1}$$

where, ton is the duration for the turn-on transient.

2.1.3 Turn-off switching Characterstics

The IGBT is turned off by removing the gate voltage, V_{GE}. As shown in the Figure 2.4, both the voltage $V_{CE}(t)$ and the current $i_C(t)$ are kept constant until the gate voltage reaches the voltage $V_{GE,th}$, which is used to keep the current $i_C(t)$ in steady on state. This moment is called the delay off time. After this the collector voltage V_{CE} starts to increase. The rate of rise of collector voltage is determined by the gate resistance.

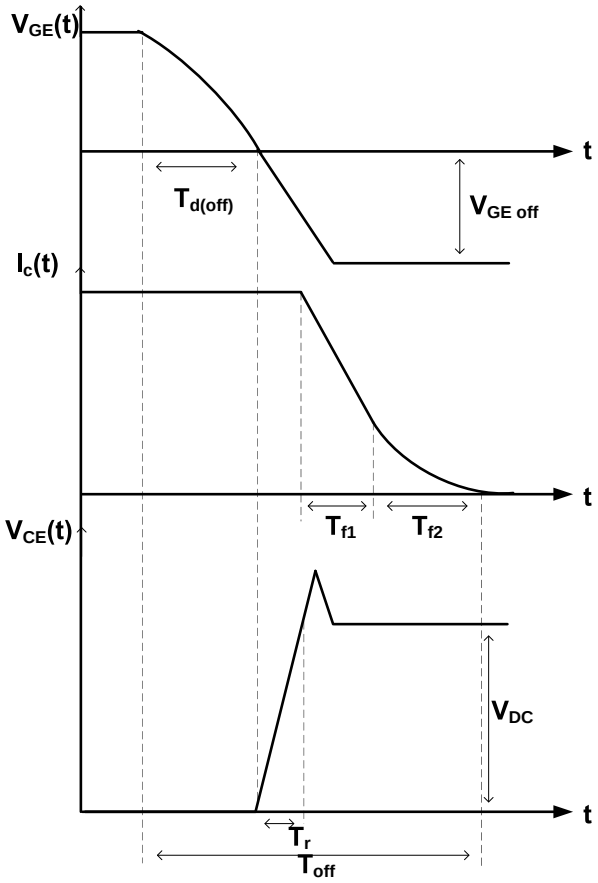

Figure 2.4 Turn Off Characterstics

When the collector voltage reaches the input voltage the collector current starts to

decrease and the free-wheeling diode starts to conduct. The major difference between the IGBT turn-off and the MOSFET turn-off is observed in the collector current waveform where there are two distinct time intervals. The rapid drop corresponds to the turn-off of the MOSFET section of the IGBT and the tailing of the collector current due to the stored charge in the n-drift region of the transistor section of the IGBT.

Turn-off switching losses are the amount of total energy losses during the turn-off. It is measured from the point where the collector-emitter voltage begins to rise to the point where the collector current falls completely to zero. The turn off energy loss calculation is given by the equation below.

$$E_{loss}(off) = \int_0^{toff} \left[V_{ce}\left(t\right) i_c\left(t\right)\right] dt \tag{2.2}$$

where,

t_{off} is the duration for the turn-off transient.

2.2 Gate Drive Circuit

The primary function of the gate drive circuit is to convert logic level control signals into the appropriate voltage and current for efficient switching of the IGBT. It provides required electrical isolation between the power switch and the logic-level control circuits and between top and bottom power switches.

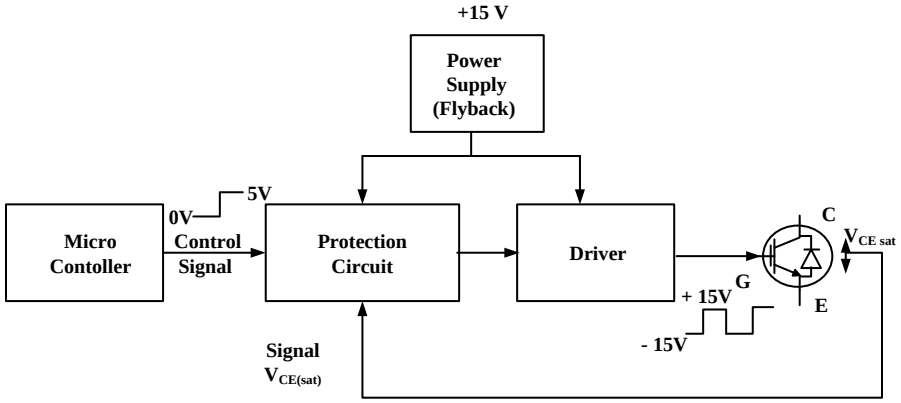

Figure 2.5 Block Diagram of Gate Drive Circuit

The driver has to immune to the severe electromagnetic noise produced by the fast switching of IGBT at high voltage and high current. Careful layout and component selection is critical to avoid problems with coupled noise.The main components of a gate drive circuit are illustrated in the simplified block diagram as shown in the Figure 3.1, are,

(1). Isolation power supply

(2). Protection and driver circuit

2.2.1 Isolatation Power Supply

Isolated power supplies are required for the high side switches in inverter circuits, because the emitter potential of the high side IGBT changes when the low side IGBT is switched. As shown in Figure 2.6, the individual control signal for the switches needs to be provided across the gate and emitter terminals of the particular switch. When upper switch is on, the emitter of the upper switch is at positive DC bus potential. When lower switch is on, the emitter of upper switch is at the negative DC bus potential. Therefore the gate voltage of all the upper switches must be floating with respect to the DC bus line potentials. This calls for isolation between the gate control signals of upper switches and lower switches.

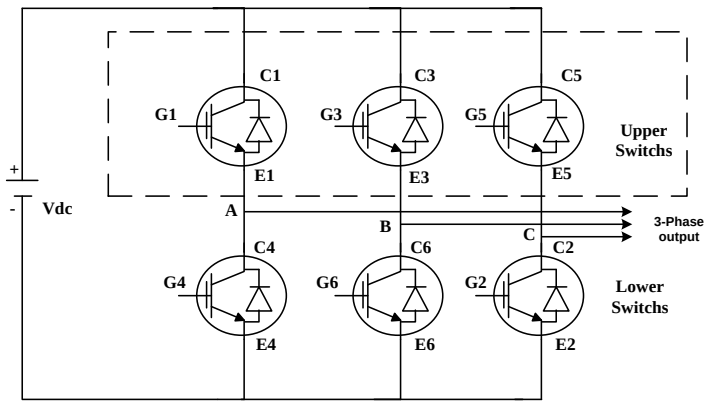

Figure 2.6 Three Phase Inverter

By having separate isolated power supplies, any $\frac{dv}{dt}$ coupled noise generated by the power device switching stays within the gate power supply circuits and shoot through current through the device may be avoided. The basic ways to provide electrical isola-

tion are either by optocouplers, fiber optics or by transformers. In this project, isolation between the power switch and the logic-level control circuit is done by using HCPL 3101 optocouplers and isolation between top and bottom devices is provided by the flyback converter.

Flyback Converter

The flyback converter is based on the buck-boost converter by replacing inductor with isolation transformer is shown in Figure 2.7. The behavior of the converter is understood by modeling the physical transformer with a simple equivalent circuit consisting of an ideal transformer in parallel with the magnetizing inductance L_M. When MOSFET Q_1 conducts, energy from the DC source is transfered to L_M. When diode D_1 conducts, this stored energy is transferred to the load $[1]$.

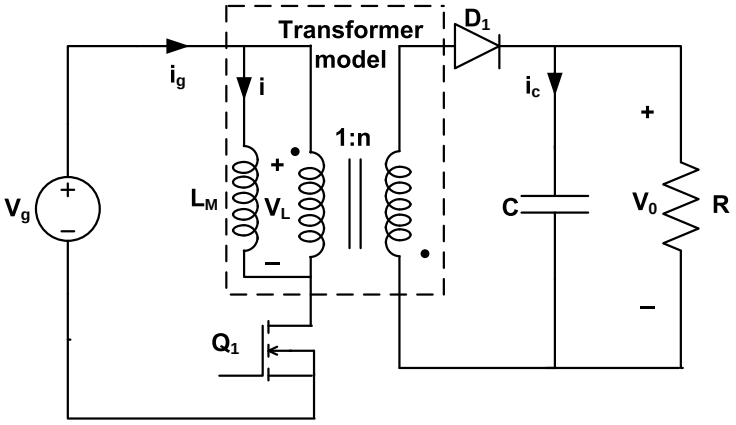

Figure 2.7 Equivalent Circuit Of Flyback Converter

During the on-time of the MOSFET, the primary winding of the transformer gets connected to the input supply, which results linearly increasing current I_1. with reference to the dotted end of primary winding, diode D_1 connected in series with the secondary winding gets reverse biased. The load connected to the output capacitor gets uninterrupted current due to the previously stored charge on the capacitor. The voltage across secondary winding is,

$$V_0 = nV_g \tag{2.3}$$

The voltage stress across the diode is,

$$V_D = nV_g + V_0 \tag{2.4}$$

When the MOSFET is turned off the primary current I_1 is interrupted and according to laws of magnetic induction, the voltage polarities across the windings reversed. The reversal of voltage polarities makes the diode in the secondary circuit forward bias. The energy moves from the transformer to the output capacitor C_o. The output voltage V_o will be transformed back to the primary side as

$$V_1 = V_o \frac{1}{n} \tag{2.5}$$

. The voltage across drain-source of MOSFET is,

$$V_{DS} = V_g + V_o \frac{1}{n} \tag{2.6}$$

Application of the principle of volt second balance to the primary-side magnetizing inductance yields

$$\frac{V_o}{V_g} = \frac{D}{(1-D)} n \tag{2.7}$$

Application of the principle of charge balance to the output capacitor C leads to

$$I = \frac{V_o}{R} \frac{n}{(1-D)} \tag{2.8}$$

For continuous operation, load current should be greater than ripple current $I > \Delta i$.

$$\frac{2L}{RT_s} > \frac{(1-D)^2}{n^2} \tag{2.9}$$

At turn-off instant, additional voltage is observed across MOSFET due to ringing associated with the transformer leakage inductance. A snubber circuit required to clamp the magnitude of this ringing voltage. When MOSFET switches off, it interrupts the current through the L_l, then it induces voltage spike according to $v_l(t) = L\frac{di_l}{dt}$. If the

peak magnitude of the voltage spike exceeds the voltage rating of MOSFET, then Q_1 fails. The RCD snubber circuit absorbs the current in the leakage inductor by turning on the snubber diodeD_s, when V_{ds} exceeds $V_g + nV_o$. At the instant of turn-off, the current through the leakage inductance L_l is diverted through the diode D_s, it charges the capacitor C_s and which is dissipated in resistor R_s. Voltage v_s rises until the power dissipated by R_s is equal to the average power transfered from L_l, then

$$\frac{v_s^2}{R_s} = \frac{1}{2} L_l I^2 f_s \tag{2.10}$$

C_s can be choose according to the following equation

$$C_s >> \frac{T_s}{R_s} \tag{2.11}$$

The flyback converter design details and schematic is discussed in the appendix 1. Design specifications of flyback converter as follows.

$V_g = 15 \pm 10$ Volts

$V_o = 18$ Volts

$P_o = 5$ Watts

$f_s = 25$ kHz

$\eta = 0.7$

$D_{Max} = 0.5$

$n = 2$

555 timer circuit produces a square wave with sharp transitions between low(zero Voltage) and high(supply Voltage). The switching frequency and the duty cycle are accurately controlled with two external resistors and one capacitor as shown in Figure 2.8. It triggers itself and when the output is high the external capacitor c_1 charges through R_1, when trigger voltage reaches to the threshold voltage $\frac{2}{3}V_s$, the output becomes low and discharge pin is connected to zero volts. Now the capacitor c_1 discharges through R_2 into the discharge pin. When the voltage falls to trigger voltage $\frac{1}{3}V_s$, then output becomes high again and the discharge pin is disconnected, allowing the capacitor to start charging again. Thus the duty cycle precisely set by the ratio of these two resistors.
The charge time (output HIGH) is given by

$$T_{on} = 0.69 R_1 C_1 \tag{2.12}$$

The discharge time (output LOW) is given by

$$T_{off} = 0.69 R_2 C_1 \tag{2.13}$$

Thus the total period T is given by

$$T_s = T_{on} + T_{off} = 0.69 \left(R_1 + R_2\right) C_1 \tag{2.14}$$

Duty cycle is given by

$$D = \frac{R_1}{R_1 + R_2} \tag{2.15}$$

The implementation of flyback converter is shown in Figure 2.8. The 555 Timer circuit is used to generate switching signals for the MOSFET IRF540. For getting 15V isolated output voltage, 555 timer should generate pulses with the duty ratio of 0.375 at the switching frequency 25 kHz. To achieve 0.375 duty at 25 kHz frequency, values of R_1, R_2 and C_1 are 38 kΩ, 82 $k\Omega$ and 470 μF respectively.

In between 555 timer circuit and MOSFET a totem pole arrangement with NPN CK100 and PNP BEL 100N transistors are used to boost the timer output, to switching of the MOSFET. Base terminals of both the transistors are connected to logic pulses through 220 Ω resistors, to limit base current. When pulse voltage signal is High, the NPN transistor is switched on and the gate of the MOSFET is connected to the supply, and MOSFET switched on. When pulse voltage signal is Low, PNP transistor is switched on and gate of the MOSFET is connected to the supply ground, and MOSFET is switched off. A 10 k resistor is connected in between the gate and source of the MOSFET to protect it against the miller effect, and one 15V zener diode is connected,

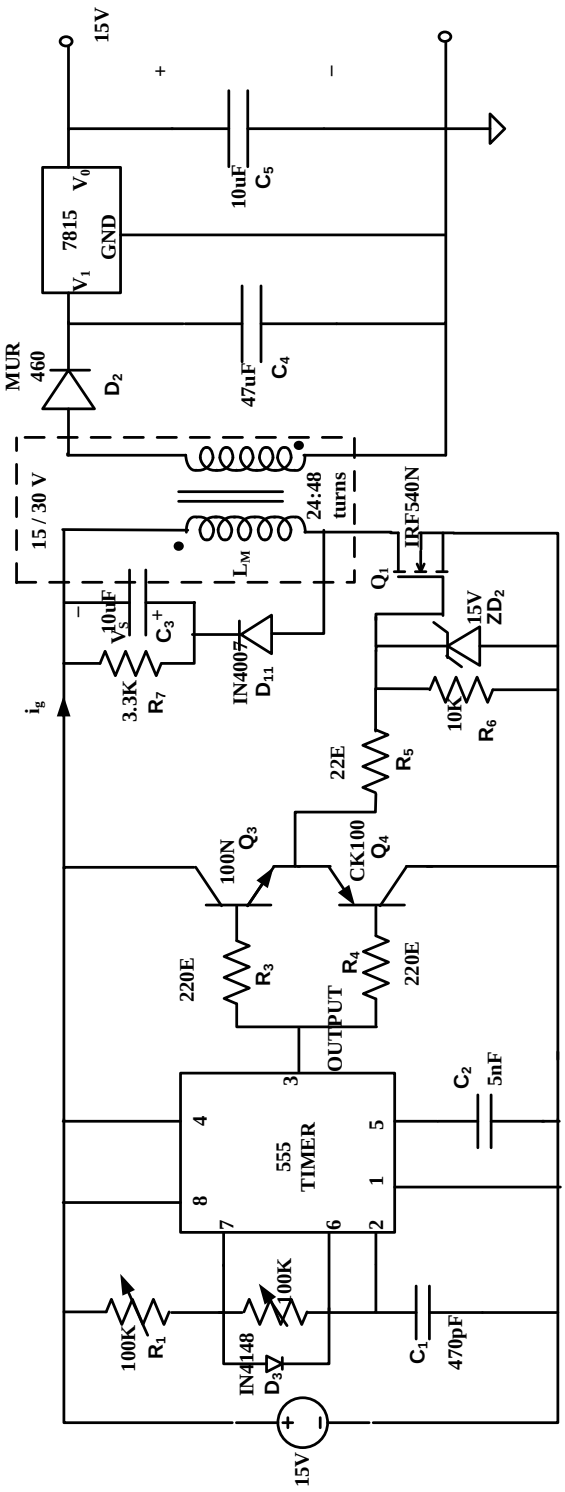

Figure 2.8 Implementation of Flyback Converter

to protects the gate-emitter junction of the IGBT from over voltage spikes. A 22 Ω gate resistor used to charge and discharge the gate capacitance faster, resulting in increased switching speed and reduced switching losses of MOSFET. In the secondary side of the transformer MUR460 power diode is used. A 7815 voltage regulator is used to regulate the isolated output voltage to 15 V.

2.2.2 Protection and driver Circuit

The switching devices are selected to reliably handle circuit currents under normal and overload conditions. If short circuit is sustained on a device, high current will cause a rise in the junction temperature of the device, which is extremely fast due to its high thermal time constant and collector-emitter voltage shoot up. To save the switching device from failure, external protection circuits are used to sense the fault and turn off the the gate drive. It is necessary to design appropriate protection circuit. Switching devices are rated for a specified short circuit time. The specified short circuit time of a device is a measure of how much time a device would survive from start of a short circuit until the current is cutoff. If short circuit occurs in the device, due to short circuit current device will fails. In order to protect the IGBT under short circuit conditions, the fault condition has to detected and IGBT has to be turn off by removing the gate-emitter drive signal before the junction temperature exceeds thermal limitations. The gate drive circuit has to react faster during short circuit conditions to protect the switch [4].

IGBTs are having a short circuit withstand capability order of 8 to 10 μs. Therefore, the fault detection circuit needs to be designed such that it takes minimum time in the order of 1 to 3 μs. Various types of detection circuits based on the measure of the collector voltage and collector current is reported in citation.

1. Detection through resistance

This is the general method for detecting fault current where a resistor is connected in parallel to the load current path and the voltage across it is measured to trigger the protection circuit.

2. Current sensing through sensors

Hall effect sensors are used for detecting fault current where the transformer is placed around the fault current carrying conductor. Hence, the increase in fault current will induce a rise in current in these current transformers, which will be used to activate the

protection circuit.

3. Collector Emitter Voltage Sensing

Under short circuit condition, the device is subjected to higher voltage than its normal ON-state voltage. Hence, by monitoring the low ON-state value, a fault condition can be detected. The desaturation voltage detection is used in applications where timely and quick detection of fault current takes precise over accurate measurement of fault current. This is the method used to implement the short circuit protection in this gate drive circuit.

Implementation of protection circuit is shown in Figure 2.9. The main components of a protection and drive circuit are illustrated as

A. Comparator for comparing $V_{CE,sat}$ with V_{trip}

B. Optocouplers to provide isolation between (i).control circuit and driver circuit. (ii).driver circuit and status signal

C. Blanking circuit is to provide blanking time in the order of 1 to 3 μs

D. NAND gate to generate of the status signal for protection

E. Flipflop circuit to termination of gate drive output during short circuit conditions

F. Driver circuit

A. Comparator

LM 339 comparator is used to compare on state collector-emitter voltage $V_{CE(sat)}$ with the trip voltage $6.2V$ provided by the zener diode ZD1. A $6.2V$ zener diode is connected across supply through the 330 Ω resistor to limit the zener diode current. A high voltage fast recovery diode MUR 1100E (D1) is connected in between the IGBT's collector and non inverting pin of comparator. The blocking voltage rating of this diode is $1100V$ and it is sufficient to sustain the DC bus voltage. This diode is used to monitor the collector-emitter on state voltage $V_{CE,sat}$ of the device $[4]$.

B. Opto-isolation

In gate drive circuit, it is necessary to electrically isolate power switches from the control circuit to provide significant protection from over voltage conditions. Optocouplers provides isolation voltage in the range of 2500 V to 5000V . An isolated power supply is required to feed the output side of the optocoupler and the driver connected to it. Optocoupler B_1 is used to isolate the driver circuit from the control circuit. The control signal from the flipflop circuit (explained in the next sections) is fed to the optocoupler through the 2N2222 transistor. When the control signal is at high state, capacitor C_7

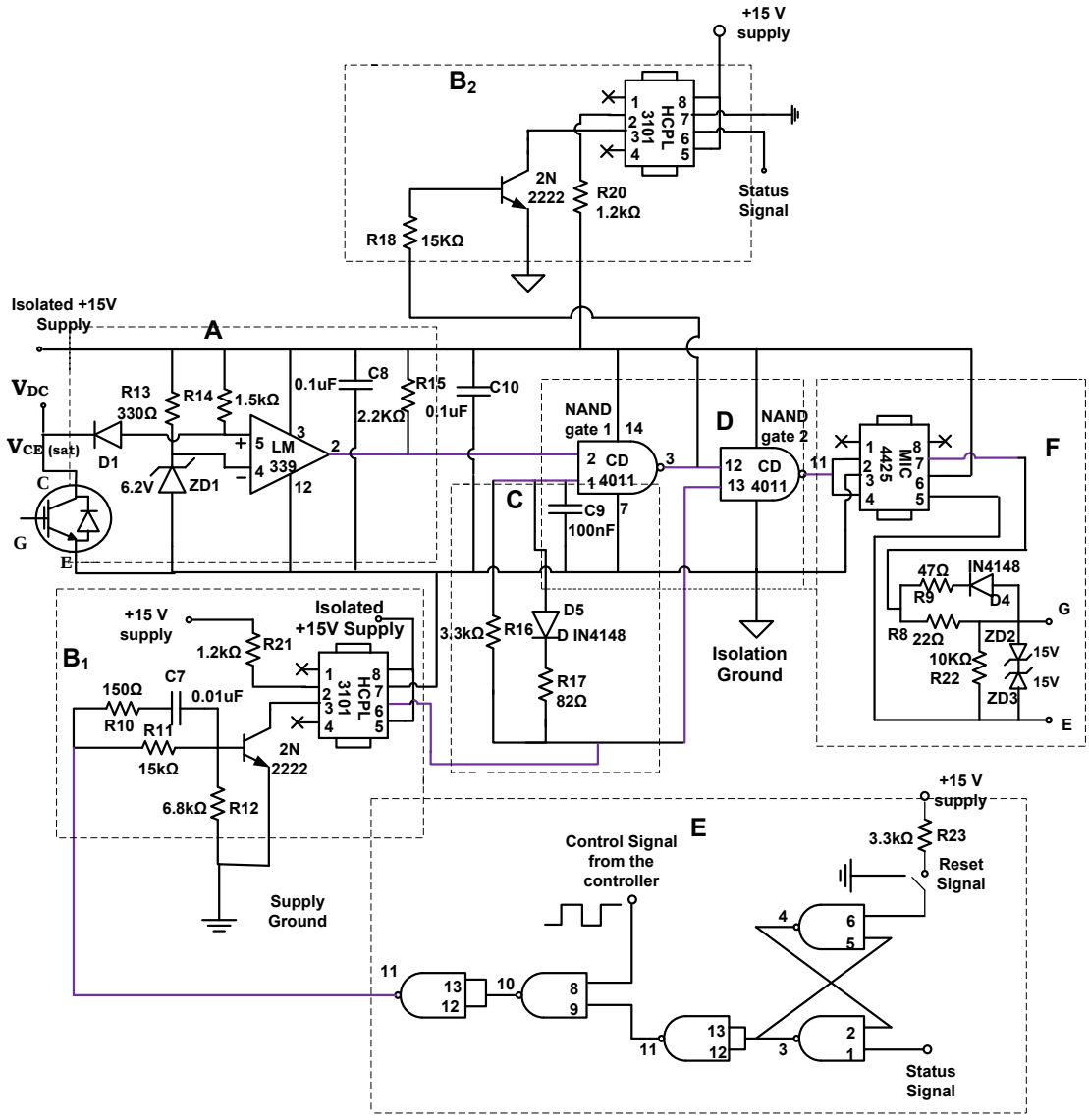

Figure 2.9 Implementation of protection circuit

provides peak current to the transistor to turn on. Output of the optocoupler B_1 is connected to the NAND gate 1 through the blanking circuit at pin 1. Optocoupler B_2 is used to isolate the status signal from the driver circuit. Output of the optocoupler B_2 is connected to the NAND gate 2 at pin 13. The status signal, which is generated by the NAND gate 1, is fed to the optocoupler B_2 through the transistor 2N2222. when the status signal is at high position, transistor turns on and optocoupler B_2 gives the status signal to the flipflop circuit.

C. Blanking circuit

During IGBT turn-on transients, the voltage across the switch V_{CE} is higher than the normal on state voltage, this could cause a false triggering of the protection circuit. Hence, in order to overcome the false triggering, a blanking time is provided by the RC circuit. According to the IGBT $(FGA25N120ANTD)$ data sheet, switch on and switch off time in the order of 200 ns to 4 μs. TO get a blanking time of 3.3 μs, the required values of R=3.3 $k\Omega$ and C = 100 nF.

D. NAND gate

It is used to generation of the status signal. Status signal indicates the fault condition. In this thesis $CD4011$ IC is used as NAND gate. NAND gate 1 generated the status signal by nanding the comparator output with the isolated control signal. NAND gate 2 nanded the status signal with the isolated control signal to produce pulses to the driver IC.

E. Flipflop circuit

SR flip flop is used to terminate the control signal under fault conditions. Set input is taking as a status signal and reset input is taking as a signal, which is either supply voltage or power ground. Under normal conditions status signal is at high position and output of flipflop circuit is same as control signal. If fault occurs status signal goes to low position, then the output of flipflop circuit is goes to low and stay until reset the flipflop. Truth table for the flip flop circuit is shown in table 3.1.

Table 2.1 Truth table for SR Flipflop

Status Signal	Reset Signal	Output
H	H	H
L	H	L
H	H	L
H	L	H

Operation of protection circuit under normal conditions

Under normal conditions, during off state of the IGBT, D1 is reverse biased and the (+) input of the comparator is pulled up to 15V supply. During on state of the IGBT, the comparators (+) input is pulled down by D1 to the IGBT's $V_{CE}(sat)$. Hence, comparator output high when the IGBT is off and low when the IGBT is on. Comparator output nanded with the isolated control signal, to generate high status signal as shown in figure 2.10. Status signal nanded with isolated control signal to generate pulses to driver MIC 4425, which are inverted and amplified to drive the IGBT [4].

Operation of protection circuit under fault conditions

Under short circuit conditions, high current will cause the collector-emitter on state voltage $V_{CE,sat}$ to rise above V_{TRIP} 6.2V, then comparator output goes to high, NAND gate 1 produces status signal as low is shown in figure 2.10. NAND gate 2 produces high signal, which is inverted as low signal by the driver MIC4425 to switch off the IGBT.

Under fault condition the switching signal is turned off for every switching cycle, after few switching cycles, switch junction temperature goes to high and switch may be damaged. To protect the switch, gate signal should be turned off at first instant of switching pulse, is done by using SR flipflop. During normal conditions both status signal and reset signal are at high position. Then output of SR flipflop is a high signal, which is anded with the control signal to generate same control signal. Under fault conditions, status signal goes to low then output of SR flipflop circuit goes to low until and unless reset the flipflop as shown in the table 2.1. This low signal anded with the control signal to produce low signal to switch off the device. The protection circuit monitors the collector-emitter on state voltage $V_{CE,sat}$, and turn off the gate-emitter

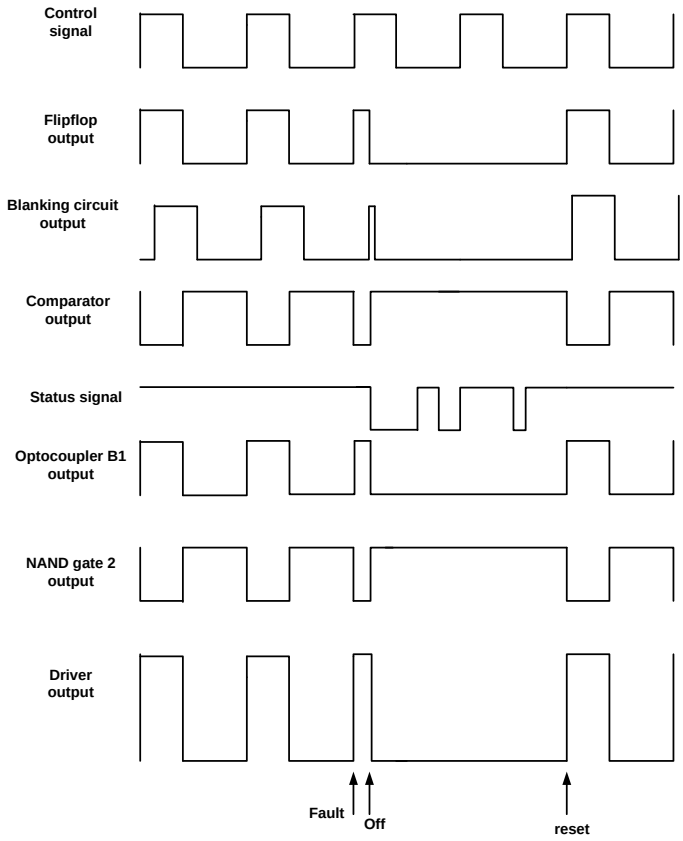

Figure 2.10 Timing diagram of protection circuit

signal if short circuit occurs.

E. Driver circuit

The gate of the IGBT requires peak gate current to charge the input capacitance. MIC 4425 is used as IGBT driver, which is a high speed driver with independent high and low side input signals. It gives 3A peak current to the gate of IGBT. The output of NAND gate 2 is inverted and amplified to switching of the IGBT.

Gate resistance

The gate driver has to supply the high peak current to rapidly charge and discharge the input capacitance of IGBT. Gate current is controlled by a series gate resistance R_G. To establish collector to emitter conduction in an IGBT, a positive voltage which is greater than device threshold voltage is applied to the gate-emitter terminals. The positive gate-emitter voltage is chosen as 15 V, to switch on the IGBT. To switch off IGBT, a negative gate-emitter voltage is produced to remove charge on the C_{GE} and C_{GC}, which is generally from -5 to -15V [6].

The external series gate resistance R_G has a significant effect on the IGBT's dynamic performance. IGBT is switched on and off by charging and discharging its gate

capacitance. A smaller series gate resistor will charge and discharge the gate capacitance faster resulting in increased switching speed and reduced switching losses, also helps to improve dv/dt noise immunity. Gate resistor controls the IGBT turn off time and also controlling the $\frac{dv}{dt}$ stress. As shown in figure 2.11, to drive the gate upto the 15 V ON level in a rise time T_r, the required current I_1 is,

$$I_1 = C_{iss}\frac{dV_{GE}}{dt} \tag{2.16}$$

From the IGBT data sheet, C_{iss} is gate-emitter capacitance equal to 3700 PF and rise time T_r is 60 ns.

$$I_1 = 0.925A \tag{2.17}$$

However in driving the gate upto 15V, the switch turn on and voltage across it drops

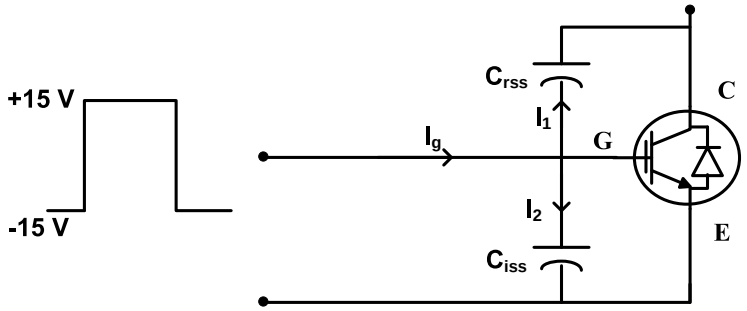

Figure 2.11 Model of IGBT

from supply voltage V_{DC} to $V_{CE,sat}$ on state voltage, the current I_2 required to achieve this,

$$I_2 = C_{rss}\frac{V_{DC} + 15}{T_r} \tag{2.18}$$

From the IGBT data sheet, C_{rss} is gate-collector capacitance equal to 80 PF. At 700 V DC supply, current is,

$$I_2 = 0.953\,A \tag{2.19}$$

Total current required to drive the gate of IGBT is,

$$I_g = I_1 + I_2 = 1.878\,A \tag{2.20}$$

Gate resistance is calculated by using gate current, gate-emitter on and off voltage, as

$$R_G = \frac{(V_{GEon} - V_{GEoff})}{I_{Gpeak}} \tag{2.21}$$

$$R_G = 16\,\Omega \tag{2.22}$$

Gate on resistance $R_8 = 22\,\Omega$, is used to reduce stress in the gate of IGBT, gate off resistance $R_9 = 15\,\Omega$ is used to fast turn off of the IGBT[2].

The fall rate of current induces a voltage equal to $L\frac{di}{dt}$ in the circuit stray inductance. This voltage overshoots, device may failure due to excessive power surge. The over voltages are reduced by minimizing the circuit stray inductances. To reduce the emitter lead inductance and parasitic oscillations, drive circuit is located as close as possible to the gate-emitter terminals of the switch. During switching miller effect currents cause $i_g x R_g$ voltage drop across series gate resistor and Ldi/dt voltage on gate driver parasitic inductance. These voltages can add to the normal on-state gate voltage causing a surge voltage on the gate of the IGBT. This gate voltage surges damage the gate of the IGBT. To clamp the gate voltage, back-to-back 15 V zener diodes connected from gate to emitter and to protect the gate,a $10\,k\Omega$ resistance is connected in between gate and emitter [5].

2.3 Testing results of gate drive circuit

Hardware implementation of gate drive circuit is shown in figure 2.12.

Figure 2.12 Hardware implementation of gate drive circuit

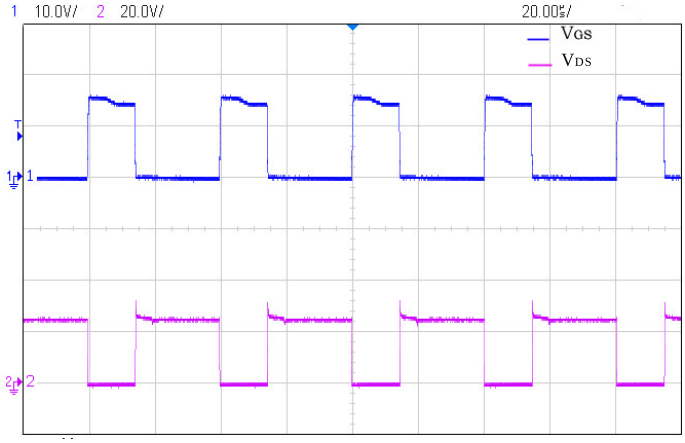

Figure 2.13 Flyback converter: gate-source and drain-source voltage waveforms.

Figure 2.13 shows voltage across the gate-source and drain-source of MOSFET. At turning off the MOSFET voltage across drain-source is 24 V and starting peak over voltage is 32 V.

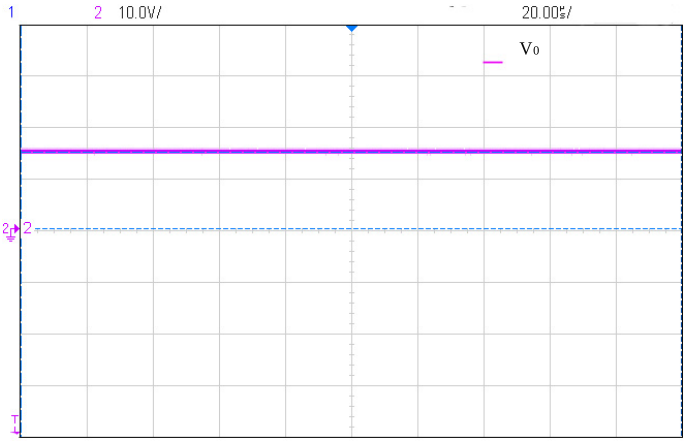

Figure 2.14 Flyback converter: output voltage waveform

Figure 2.14 shows output voltage across flyback converter. For the duty ratio of 0.4, isolated output voltage is 15 V.

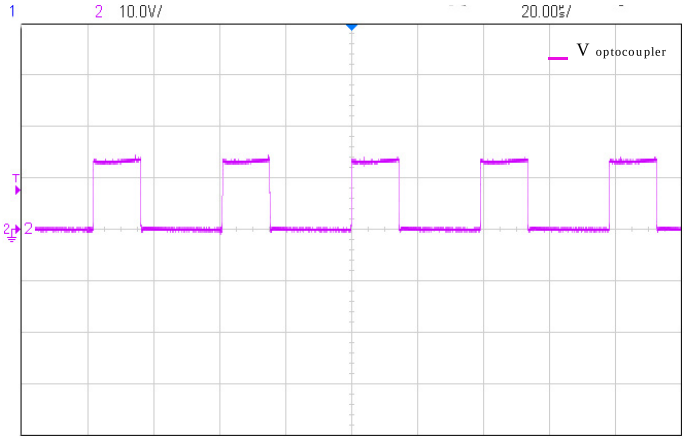

Figure 2.15 Protection circuit: optocoupler B_1 output voltage waveform

Figure 2.15 shows optocoupler output voltage, with magnitude of 14 V.

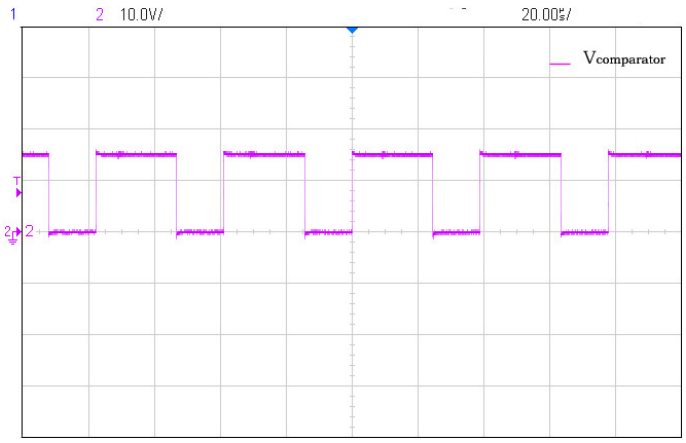

Figure 2.16 Protection circuit: comparator output voltage waveform

Figure 2.16 shows comparator output voltage waveform. During switch on condition, it is goes to 0 V and during switch off condition, it is goes to 15 V.

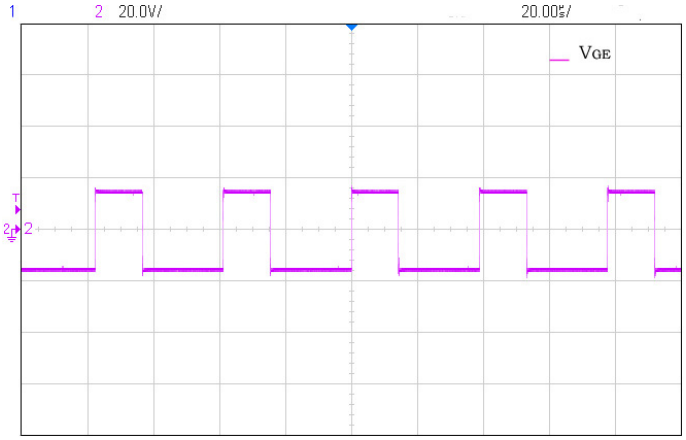

Figure 2.17 Gate drive: output voltage waveform

Figure 2.17 shows MIC 4425 driver output voltage waveform,which is changing in between +15 V and -15 V, to drive the IGBT.

CHAPTER 3

EVALUTION OF GATE DRIVE CIRCUIT FOR BUCK CONVERTER

Evaluation of gate drive circuit with short circuit protection is done by using buck converter. This chapter explains about design and hardware implementation of buck converter and evaluation of gate drive circuit under normal and fault conditions.

3.1 Buck Converter

The buck converter is a basic DC to DC converter, which converts electrical power provided from a source at a certain voltage to electrical power at a different DC voltage. The hardware implementation of buck converter is shown in Figure 3.1.

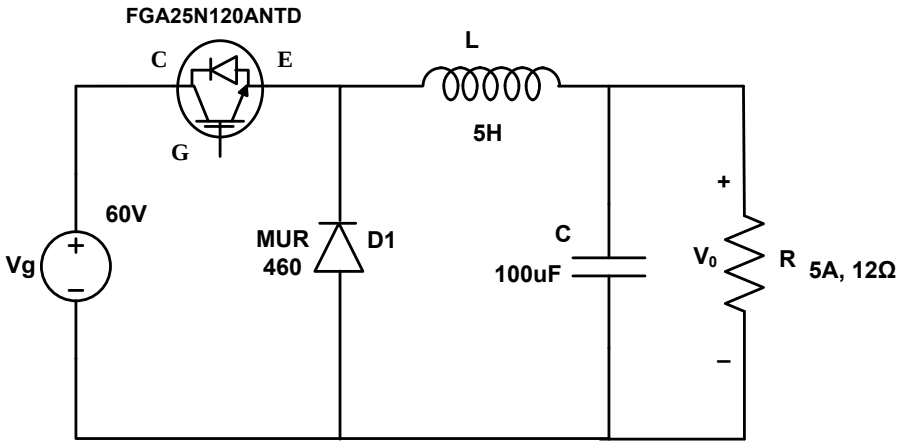

Figure 3.1 Buck converter

When the switch is on for a time duration DT_S, it conducts the inductor current, and diode becomes reverse biased. This results a positive voltage $V_L = (V_g - V_0)$ across the inductor. This voltage causes a linear increase in the inductor current i_L. When the switch is turned off for a time duration $(1 - D)\, T_S$, because of the inductive

energy storage, i_L continues to flows through the diode, and $V_L = V_o$ appears across the inductor until the switch is turned on again [3]. During switch on condition:

$$V_L = (V_g - V_0) \tag{3.1}$$

$$I_C = I_L - \frac{V_0}{R} \tag{3.2}$$

During switch off condition:

$$V_L = V_o \tag{3.3}$$

$$I_C = I_L - \frac{V_0}{R} \tag{3.4}$$

Voltage gain equation is given by,

$$V_o = DV_g \tag{3.5}$$

Ripple current of inductor and voltage ripple equations are,

$$\Delta i = \frac{V_g V_o}{L} DT_S \tag{3.6}$$

$$\Delta v_0 = \frac{\Delta i_L}{8 f_S C} \tag{3.7}$$

Specifications of the buck converter as follows:

$V_g = 60\,V$

$L = 5\,mH$

$P_0 = 300\,W$

$I_0 = 5\,A$

3.2 Evaluation results

Hardware implementation of buck converter is shown in figure 3.2.

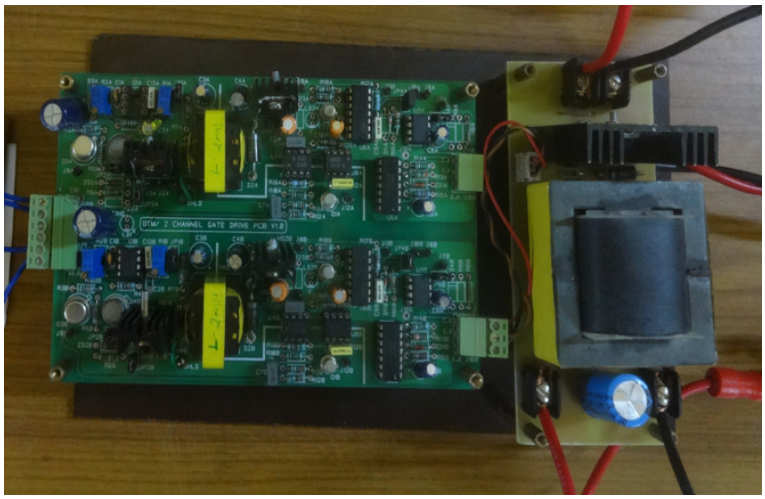

Figure 3.2 Hardware implementation of buck converter

The gate drive circuit is tested with IGBT FG25AN20ATD using buck converter. Figure 3.3 and 3.4 shows gate-emitter, collector-emitter voltages and switch current waveforms under 12 Ω resistive load.

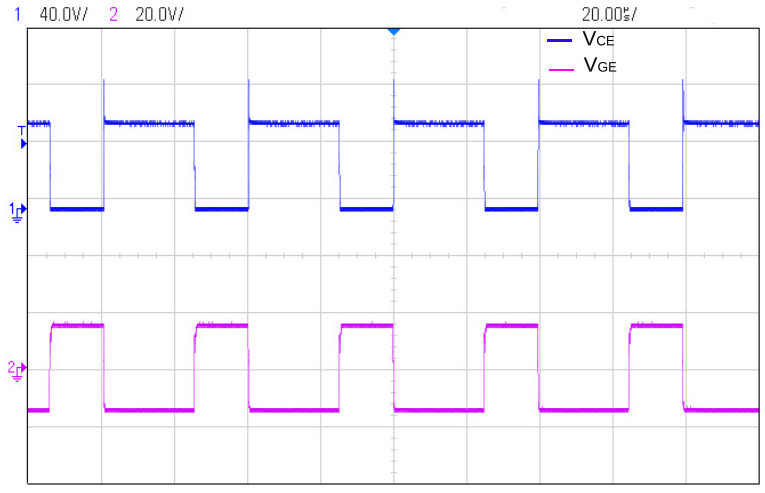

Figure 3.3 Buck converter:collector-emitter and gate-emitter voltage waveforms

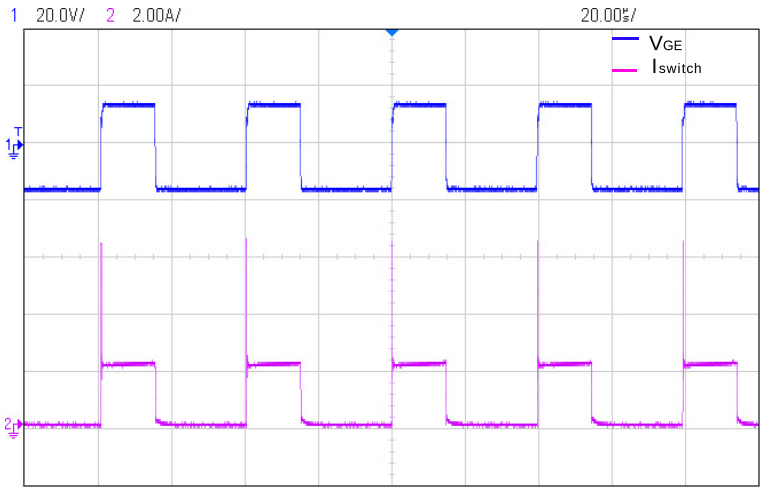

Figure 3.4 Buck converter:gate-emitter voltage and switch current waveforms

The DC bus voltage is set to 60 V, supplying 2 A R.M.S output current, at 25 kHz switching frequency with duty ratio of 0.4.

The turn on and turn off switching characteristics along with switching losses are shown in Figure 3.5 and 3.6.

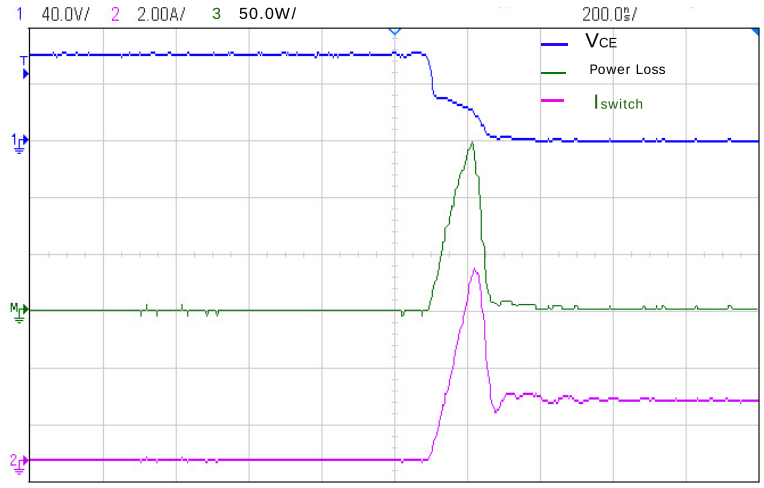

Figure 3.5 Buck converter:turn on characteristics of IGBT

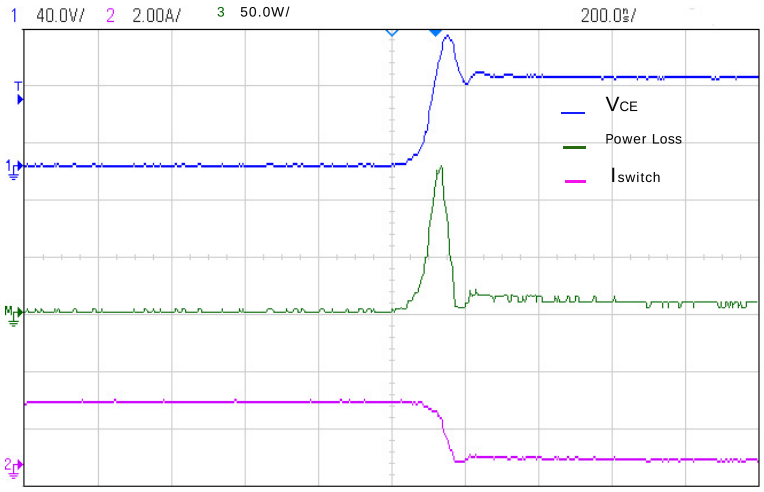

Figure 3.6 Buck converter:turn off characteristics of IGBT

IGBT turns on within 635 ns and the initial current spike is upto 6.3 A. This extra current is due to the free wheel diode reverse recovery. As shown in the figure 3.6 the current fall time consist of sharp fall within 120 ns and following a current tail of about 280 ns. The turn on delay time T_{don} is 104 ns and rise time T_r is 38 ns at 60 V supply voltage. During turn off the peak reverse voltage is 90.5 V. The turn off delay time T_{don} is 138 ns, current fall time T_r is 66 ns and storage time is 274 ns at 60 V supply voltage. During switch on conditions switching loss mainly occurs in the time of 200 ns with peak power of 150 watts. During switch off conditions switching loss mainly occurs in the time of 215 ns with peak power of 115 watts.

The gate drive circuit was tested with IGBT operating into short circuit condition. The experimental set up that was used to verify the performance of the gate drive circuit against short circuit protection is shown in Figure 3.7. In between the DC supply and buck converter or inverter, one capacitor bank is used because this capacitor bank will provide instant large peak current under short circuit conditions.

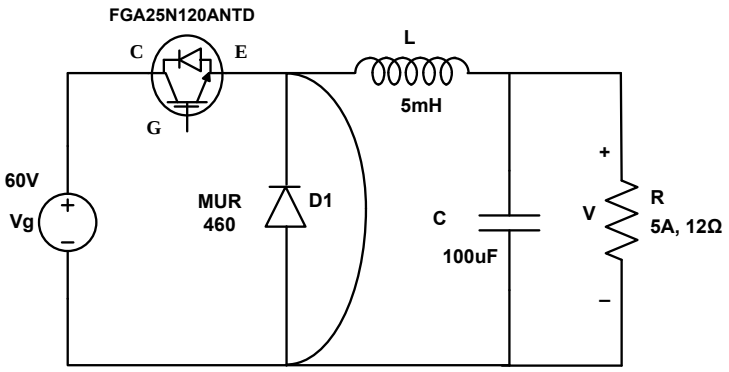

Figure 3.7 Buck converter: short circuit test diagram

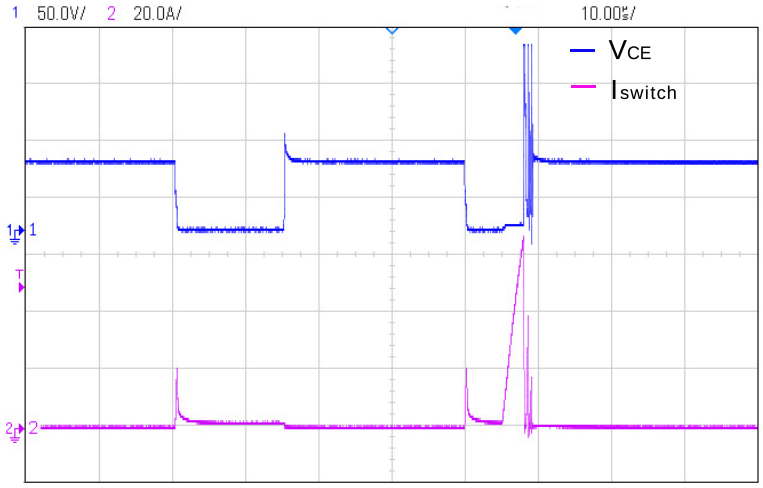

Figure 3.8 Buck converter:IGBT collector - emitter and collector current waveforms under short circuit at 60 V

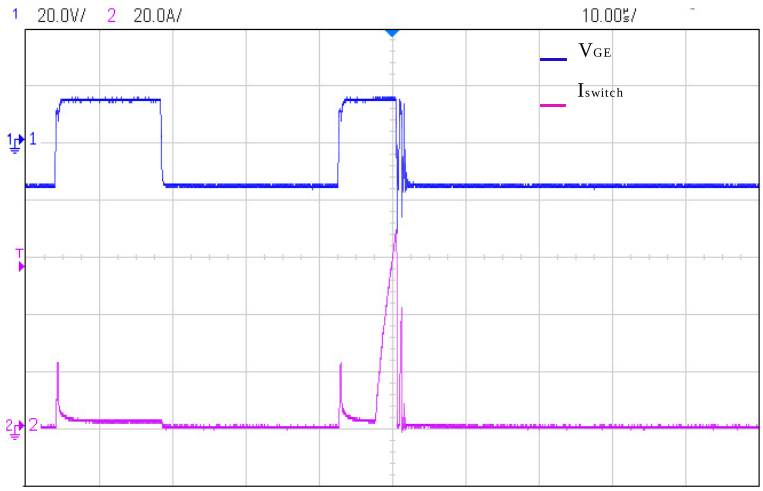

Figure 3.9 Buck converter:IGBT gate - emitter and collector current waveforms under short circuit at 60 V

The gate drive protection circuit is tested against short circuit condition by shorting the diode terminals at 60 V supply voltage as shown in Figure 3.8 and 3.9. At short circuit condition the current peaked up to 65 A which is less than the pulse current of IGBT 90 A, switch $V_{CE,sat}$ increased to greater than 6.2 V and gating pulses are tripped off after blanking time 2.8 μs.

CHAPTER 4

EVALUTION OF GATE DRIVE CIRCUIT FOR INVERTER

Evaluation of gate drive circuit with short circuit protection is done by using inverter. This chapter explains about design and hardware implementation of inverter and evaluation of gate drive circuit under normal and fault conditions.

4.1 Inverter

Inverter transfer power from a DC source to an AC load. The output voltage is controlled by switching the devices of the inverter in an appropriate sequence. Both switches on one leg can not be on at the same time, otherwise a short circuit would exist across the DC source, it will destroy the switches of the converter. The voltage rating of the inverter depends on the PWM techniques that are used to turn on and off the semiconductor switches. With SPWM technique the required DC Bus voltage for output Line-Line voltage of 400 V (RMS) is

$$m_a.V_{DC} = \frac{V_L.2.\sqrt{2}}{\sqrt{3}} \tag{4.1}$$

For the values of $m_a = 0.9$, the required DC bus voltage is 654 V. Switch used in inverter applications has to block minimum of 1.5 times of DC bus voltage.

Current drawn depends on the load connected to the inverter. For output power 1KVA , $V_L = 400\,V$, R.M.S current rating of Inverter is I = 2.5 A. Based on the blocking voltage, passing current and switching frequency, switch used in inverter is selected as IGBT F25N120ATD with 1200 V, 25 A ratings.

Figure 3.3 shows the three phase inverter, each leg consists of two switches. The DC supply is connected to the collectors of the all the top switches, and the D.C ground is

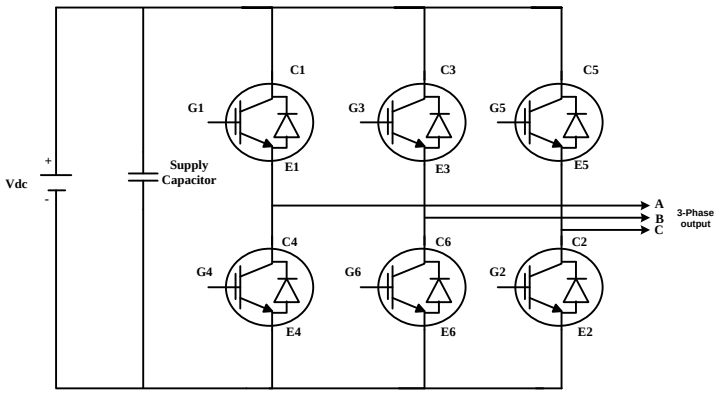

Figure 4.1 Inverter

connected to the emitters of the all the bottom switches. The gates of the all the switches are driven by individual gate drive circuits. During the operation of the inverter, due to the stray inductance of the DC bus bar, at turn off over voltage spikes are generated. If this voltage spikes exceed the rating of the switch, it can be destroyed. therefore to minimize the stray inductance of DC busbar, insulated and sandwich type busbar type construction is provided. Each switch is mounted on the finned aluminum heat sink. To get good temperature distribution thermally conductive silicon paste is applied to the contact surfaces, and all mounting bolts securing the switches were tightened to ensure a good thermal contact to the mounting surface of the heat sink. The top and bottom D.C busbar layers are the positive and ground of DC supply respectively. In each leg, the mid point of the emitter of the top switch and collector of the bottom switch as the output busbar connection. The DC bus capacitors are positioned vertically on the top layer. One on state voltage sensing diode, pair of the zener diodes and 10K resistor is used for the gate protection of IGBT. To reduce the effects of EMI generated by the switching of the IGBTs, the length of the leads carrying the gate drive signals should be as short as possible, and both gate and emitter wires are has to twist, to reduce the lead inductance. The DC bus tracks and output tracks are wider to handle high currents and voltages. All power and communication links are to the gate drive and inverter are connected via connectors, therefore allowing easy connection and disconnection [4].

The control circuit TMS320F28335 micro controller produces the sinusoidal PWM signals for the three phases using the inbuilt hardware PWM modules. 0.1 μF snubber capacitor is used across each leg to suppress the over voltages. DC bus capacitors 470 μF, 450 V are connected in series and parallel to achieve 700 μF capacitance. The

amplitude modulation ratio(m_a) is set to 0.9 in order to produce approximately the 400 V R.M.S rated output line to line voltage at the rated fundamental frequency of 50 Hz. Hardware implementation of three phase 1 KVA inverter is shown in the figure 4.2.

4.2 Evaluation results

Figure 4.2 Hardware implementation of three phase 1 KVA inverter

To ensure gate drive circuit capability, initially gate drive circuit is tested in single phase inverter operation. Control signals for single phase inverter switches, are generated by using TL 494 PWM IC.

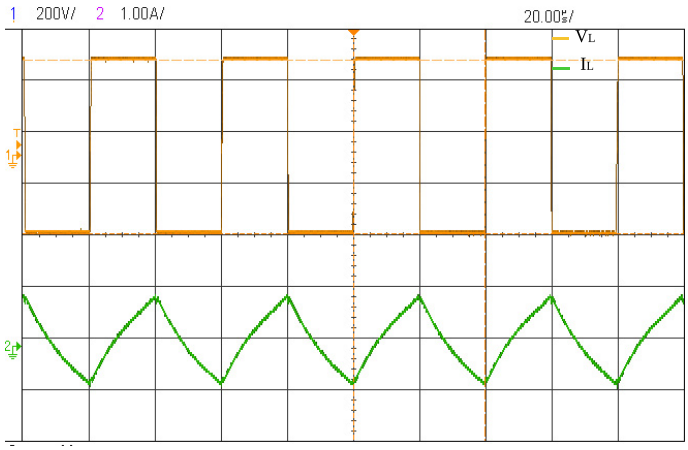

Figure 4.3 Single phase inverter with RL load at 300 V: Load voltage and current waveforms

Figure 4.3 shows the measured load output voltage and current waveforms of the inverter at 320 V DC supply with R-L load of 50 Ω and 1mH at 25 kHz switching frequency with square wave operation, to ensure that control and gate drive circuits were capable of controlling the three phase inverter with SPWM switching strategy to get the required current and voltage levels.

Evaluation of gate drive circuit is carried out using three phase inverter under resistive load. SPWM switching strategy is used to drive the switches.

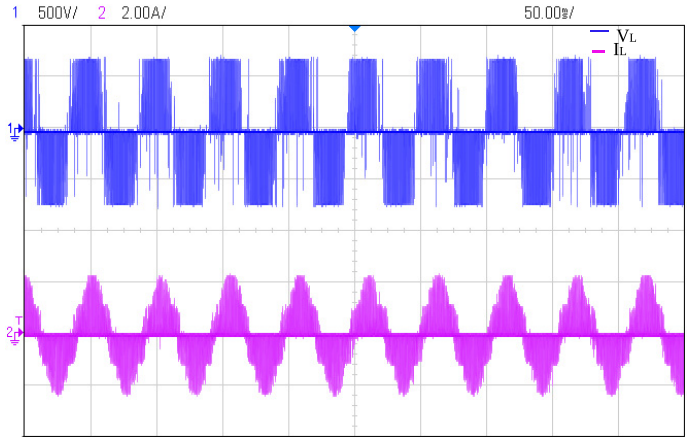

Figure 4.4 Three phase inverter with resistive load at 700 V DC: Load voltage and current waveforms

Figure 4.4 shows the measured output voltage across load and current through the load. Inverter is loaded up to 300 watts at 700 V DC supply.

Evaluation gate drive circuit is carried out using three phase inverter with an induction motor under no load.

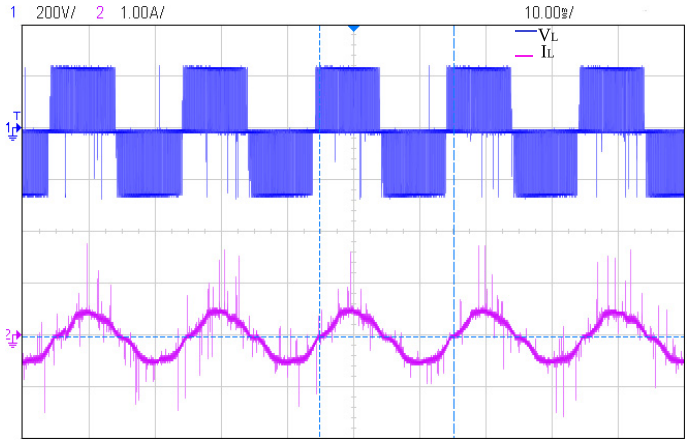

Figure 4.5 Three phase inverter with induction motor at 200 V DC: Load voltage and current waveforms

Figure 4.5 shows the output voltage and current waveform of the three phase inverter with SPWM controlling pulses at 200 V DC supply with induction motor. The fundamental frequency and switching frequency are set at 50 Hz and 10 kHz in the micro controller. The current waveform is very close to sinusoidal shape and peak of 1 A. Short circuit condition was created in one leg of the inverter circuit, by applying continuously on and off signal, with switching frequency 25 kHz to the top switch, and the constant 15 V positive gate-emitter voltage to the bottom switch, at 100 V and 200 V DC supply as shown in figure 4.6.

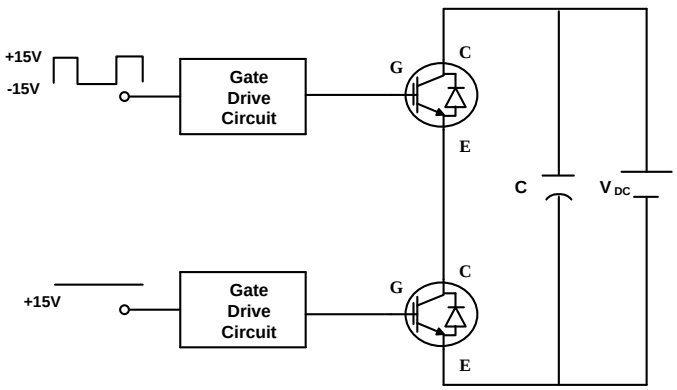

Figure 4.6 Inverter: short circuit testing diagram

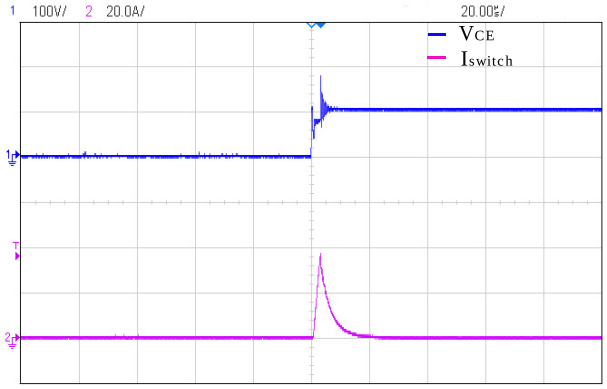

Figure 4.7 Inverter: IGBT collector - emitter and collector current waveforms under short circuit at 100 V

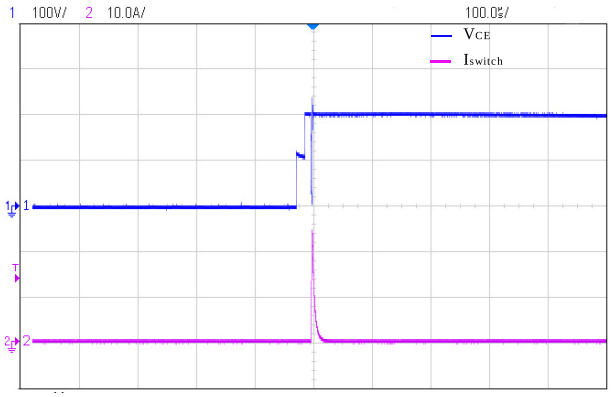

Figure 4.8 Inverter: IGBT collector - emitter and collector current waveforms under short circuit at 200 V

Figures 4.7 and 4.8 shows tthat, under short circuit conditions, voltage across switch increased to beyond 6.2 V, the gate drive reacts rapidly after 2.8 μs of the blanking time,the gate-emitter voltage decreased from +15 V to -15 V and turns off the IGBT completely.

CHAPTER 5

CONCLUSIONS

The gate drive circuits are very critical to the reliability and efficiency of an IGBT inverter system. An IGBT gate drive with short circuit protection is developed. Gate drive circuit generates isolated +15 V and -15 V for switching the IGBT. The maximum current capacity of the gate driver circuit is 3 A, which is enough to drive the IGBT. Short circuit protection is done based on collector-emitter voltage sensing method and it provides the safe turn off of a switching device under short circuit conditions. Precise detection of the over current can be done without an additional current sensor. Experimental tests were carried out to evaluate the performance of the gate drive circuit and switching characteristics of IGBT using buck converter. In the short circuit test conducted on buck converter under loaded condition, a ringing was observed which lasted for 2.8 μs, because the short circuiting was done using a mechanical switch. The inverter design incorporated a laminated sandwich busbar structure. The advantage of this mechanical construction is that over voltages are reduced by reducing the stray inductance. The demonstration of inverter in single phase operation was done using a RL load. Three gate drive circuits were built for three phase inverter, to evaluate gate drive circuit performance. Experimental tests were carried out to evaluate the performance of the gate drive and three phase inverter using a resistive load first and then an induction motor under no load. The results shows that the inverter output currents are approximately sinusoidal. The short circuit test was done on the inverter board under no load condition. Here, the gate drive circuit pulses to the inverter board were tripped off after 2.8 μs.

5.1 SCOPE FOR FUTURE WORK

When an induction motor under no load was operated using the inverter at DC bus bar voltage level of 200 V, a nuisance tripping of the gate drive circuit was observed. This is due to the common mode noise injected by the switching devices. An improvisation in the PCB layout has to be done to reduce nuisance tripping.

APPENDIX A

Design Of Flyback Converter

This chapter explains about design of the flyback converter. Design specifications of flyback converter as follows. $V_g = 15 \pm 10\,\text{V}$

$V_o = 18\,\text{V}$

$P_o = 5\,\text{watts}$

$f_s = 25\,\text{kHz}$

$\eta = 0.7$

$D_{Max} = 0.5$

By using flyback converter output voltage equation,

$$n = \frac{V_o}{V_g}\frac{(1-D)}{D} \tag{A.1}$$

$n \cong 2$

For fixed value of $n = 2$

$D_{min} = 0.375$

The DC component current is given by

$$I_{dc} = \frac{P_o}{\eta V_{gMax} D_{Min}} \tag{A.2}$$

$I_{dc} = 1.16\,A$

Assume the ripple current Δi is 10% of I_{dc}

then Δi=0.116 A

The R.M.S value of primary current I_1 is given by

$$I_1 rms = I_{dc}\sqrt{D}\sqrt{1 + \frac{1}{3}(\frac{\Delta i}{2})^2} \tag{A.3}$$

$I_1 rms = 0.86\,A$

The R.M.S value of secondary current I_2 is given by

$$I_2rms = \frac{1}{n} I_{dc} \sqrt{(1-D)} \sqrt{1 + \frac{1}{3}(\frac{\Delta i}{2})^2} \tag{A.4}$$

$I_2rms = 0.46\,A$

The primary inductance is given by

$$L_p = \frac{V_g D T_s}{\Delta i} \tag{A.5}$$

$L_p = 2.13\,mH$

Now transformer window area product is given by

$$A_e A_w = \frac{L_p \Delta i (I_1 rms + n I_2 rms)}{B_m J K_w} \tag{A.6}$$

$A_e A_w = 2013\,mm^4$

The selected core is E 25/13/7 with $A_e = 52.5\,mm^2$ and $A_w = 87\,mm^2$

The number of primary turns given by

$$N_{1Min} = \frac{V_g D T_s}{\Delta B A_e} Turns \tag{A.7}$$

$N_1 = 23.53 \cong 24$

Turns The number of secondary turns given by

$$N_2 = n N_1 Turns \tag{A.8}$$

$N_2 = 48$

Turns The wire size for primary and secondary given by

$$A_{w1} = \frac{I_1}{J} \tag{A.9}$$

$$A_{w2} = \frac{I_2}{J} \tag{A.10}$$

$A_{w1} = 0.284\,mm^2$ and $A_{w2} = 0.184\,mm^2$

The desired wire size from the wire tables are, for primary winding SWG 25 and for secondary winding SWG 28.

The schematics of gate drive circuit are shown in the figures A1 and A2.

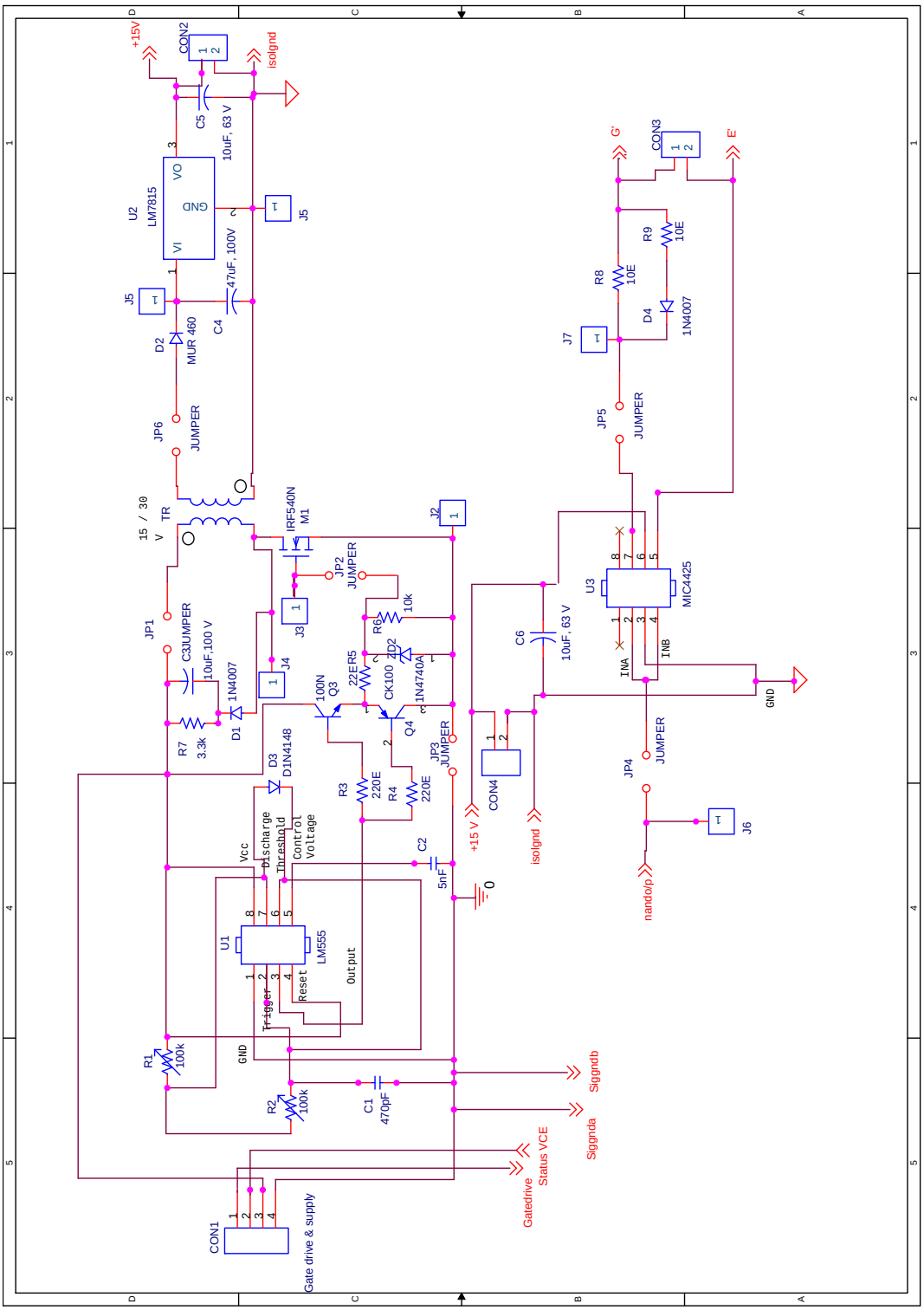

Figure A.1 Schematic of flyback converter

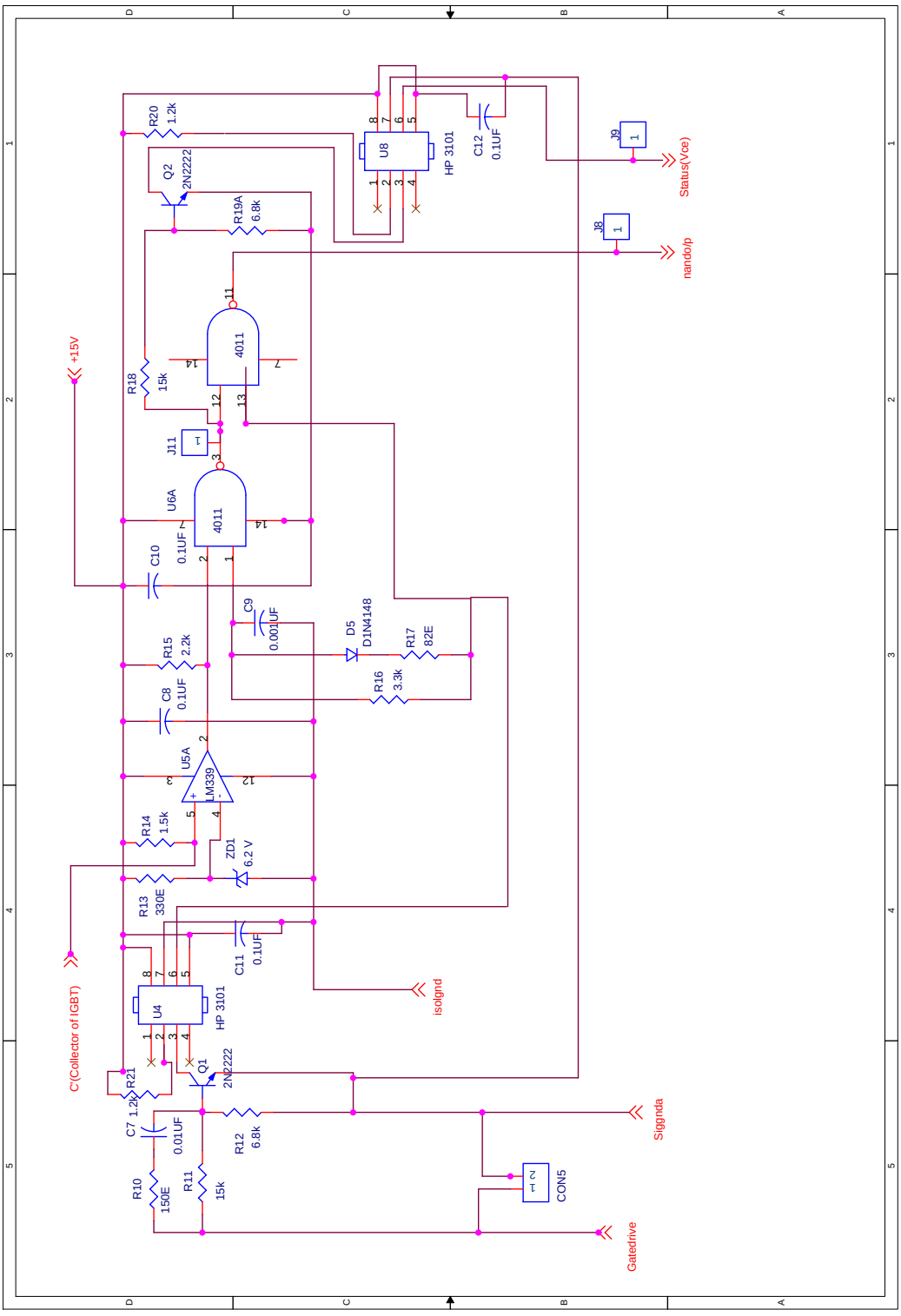

Figure A.2 Schematic of protection circuit

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