STEADY STATE SOLUTION AND NOISE ANALYSIS OF RING AMPLIFIER BASED SWITCHED CAPACITOR CIRCUITS

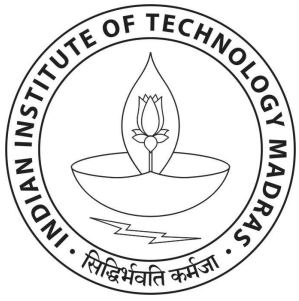
A Project Report

submitted by

SASHANK K

in partial fulfilment of the requirements
for the award of the degree of

BACHELOR OF TECHNOLOGY



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THESIS CERTIFICATE

This is to certify that the thesis titled **STEADY STATE SOLUTION AND NOISE ANALYSIS OF RING AMPLIFIER BASED SWITCHED CAPACITOR CIRCUITS**, submitted by **Sashank K**, to the Indian Institute of Technology, Madras, for the award of the degree of **Bachelor of Technology**, is a bona fide record of the research work done by him under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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ABSTRACT

KEYWORDS: Ring amplifier; Offset voltage; Stabilization mechanism; Overshoot; Dead-zone; Progressive reduction; Settling; Design procedure; Noise; Inter-reciprocity in LPTV systems; OTA

This report studies the steady state solution of a ring amplifier based switched capacitor circuit, analysing its structure and steady state mechanism in detail. An already available first order model is extended to include effects of slewing and parasitic capacitances. Based on the detailed analysis, a design procedure is formulated to help fix the transistor dimensions in the circuit.

The noise of the ring amplifier is analysed by using inter-reciprocity in LPTV networks with sampled outputs. The variation of noise with different parameters is studied. A frequency domain noise analysis of OTA based switched capacitor circuits is done, and the two noise analyses are compared.

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CHAPTER 1

INTRODUCTION

As stated in (Fiorenza *et al.*, 2006), designing traditional switched capacitor circuits (using op-amps and OTAs) has become an increasingly demanding task in scaled CMOS technologies. Lower supply voltages implies lower signal swing. Lower output resistances in scaled circuits leads to lower DC gains for traditional operational amplifiers. (Hershberg *et al.*, 2012) states that technology scaling is designed to favour the world of high-speed digital design, but not the traditional op-amp, which is fundamentally ill-suited to scaling. A truly scalable amplifier takes the features of scaled CMOS which favour digital design, and uses them to its advantage.

One attempt made in this regard was the CBSC, that is, comparator based switched capacitor circuit (Fiorenza *et al.*, 2006), which has the potential for significant power reduction when compared to traditional op-amp based circuits. Also, CBSC designs are more amenable to design in scaled environments and are free from feedback and stability concerns.

Another alternative, the ring amplifier or RAMP or ring-amp (Hershberg *et al.*, 2012), is the focus of this discussion. It embodies all the essential elements of scalability. It amplifies with nearly rail-to-rail swing, charges large capacitors efficiently by slew-based charging, scales well according to process trends and can be built with only a few transistors, capacitors and voltage-controlled switches.

The organization of this report is as follows:

- Chapter 2 introduces the structure of the ring amplifier, explains ring-amplification in detail using a first-order model presented by (Hershberg *et al.*, 2012). It then goes on to extend the first-order model to include effects of slewing and parasitic capacitances, and illustrates the same using suitable examples using a LEVEL 1 MOSFET model.
- Chapter 3 introduces some parasitic capacitance and delay models. It combines these with some of the constraints derived in Chapter 2 and provides a set of

guidelines for designing a ring amplifier (choosing transistor lengths and widths). It goes on to illustrate these guidelines with suitable examples using 0.18 μm LEVEL 49 models.

- Chapter 4 introduces some techniques for "time-domain" noise analysis in LPTV systems provided by (Pavan and Rajan, 2014). It then applies these techniques to the ring amplifier based switched capacitor circuits and an approximate model is developed to explain the noise in a ring-amplifier circuit. The variation of noise with different circuit parameters is explored and the trends are verified by running simulations using a LEVEL 1 model.

- Chapter 5 analyses the noise of traditional OTA based switched capacitor circuits using traditional "frequency-domain" techniques, which cannot easily be applied to ring amplifiers. It then goes on to state some similarities and differences in the noise performance of the ring amplifier based switched capacitor circuit and traditional op-amp based switched capacitor circuit.

CHAPTER 2

Structure and Functioning of Ring Amplifier

2.1 Structure

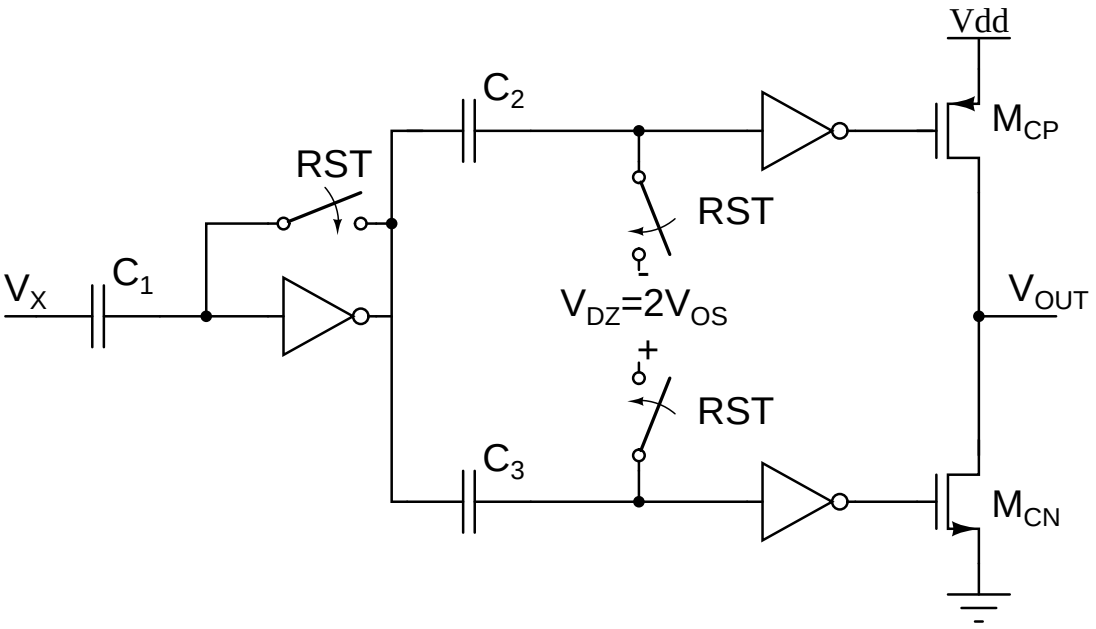


Figure 2.1: Ring amplifier

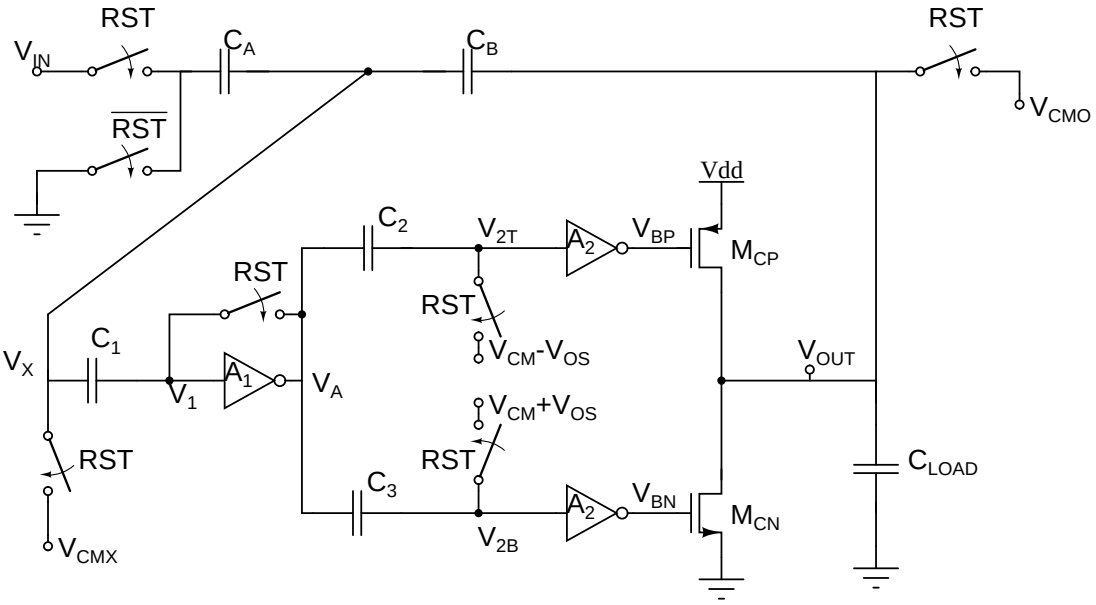


Figure 2.2: Ring amplifier with switched capacitor feedback

A simple structure of a ring-amplifier described in (Hershberg *et al.*, 2012) is first considered to explain the fundamentals of ring-amplification. Alternate structures have been developed for the ring amplifier like the ones mentioned in (Lim and Flynn, 2015) and (Lim and Flynn, 2014).

As shown in figures (2.1) and (2.2), a ring amplifier (abbreviated as ring-amp) is a ring oscillator split into two different paths and having different offset voltages embedded in each path. This creates a "dead-zone" region of no conduction both by M_{CN} and M_{CP} transistors. For sufficiently large values of dead-zone, the ring-amp slews, settles (rings) and locks itself into the dead-zone region. This is illustrated in figures (2.3) and (2.4). The large capacitor C_1 is used to cancel the voltage difference between V_{CMX} and the trip-point of the first stage inverter A_1. That is, a sufficiently large capacitor ensures that the voltage difference between the nodes V_X and V_1 during $\overline{RST}$ is the same as the difference during RST. Sources of offset after A_1 will however not be removed by the large capacitance C_1. The offset voltage V_{OS} is embedded using capacitors C_1 and C_2.

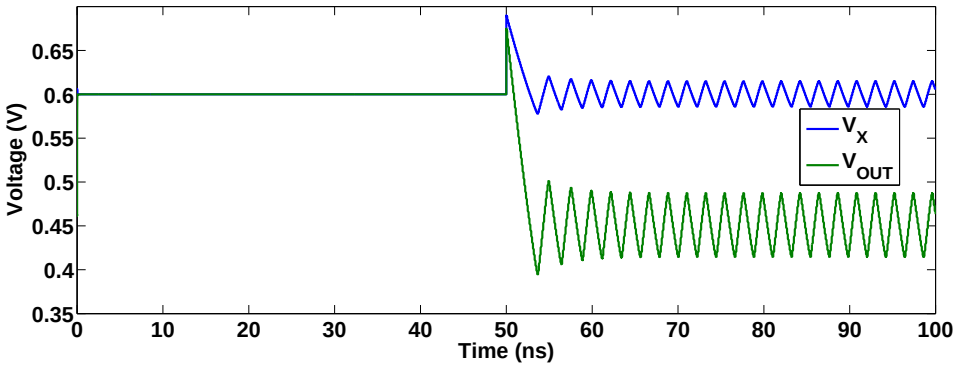


Figure 2.3: Ring amplifier behaves like a ring oscillator for V_{OS} = 0

It is apparent that when the ring-amp settles and locks itself to its steady state value, the node V_X will be within one input-referred offset voltage more or less than V_{CMX}. Denoting error in the node voltage V_X by ϵ_{V_X}, the following inequalities hold true,

$$\begin{aligned} V_{CMX} - \frac{V_{OS}}{A_1} < V_X < V_{CMX} + \frac{V_{OS}}{A_1} \\ |\epsilon_{V_X}| < \frac{V_{OS}}{A_1} \end{aligned} \tag{2.1}$$

where A_1 is the steady-state gain of the first stage inverter.

Also, it is obvious that if the circuit settles to steady state, its output value without

considering the error is

$$V_{OUT} = V_{CMO} + \frac{C_A}{C_B} V_{IN} \tag{2.2}$$

2.2 Ring Amplification

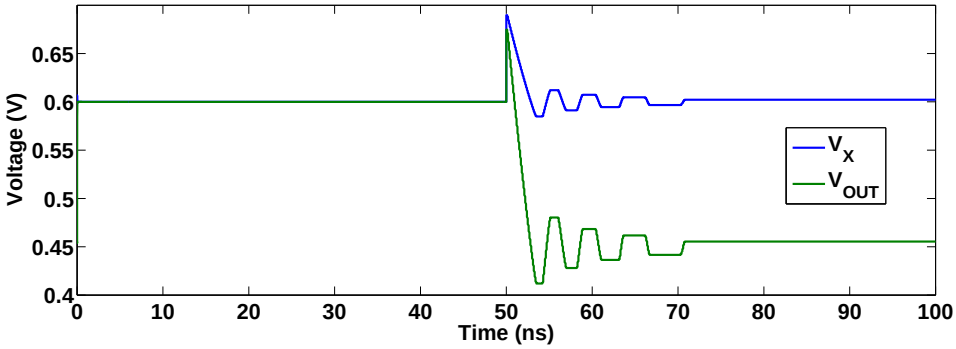


Figure 2.4: V_X, V_{OUT} v/s time for V_{OS} = 150 mV

Though the ring-amp has a very simple structure, analysis of its steady state is quite daunting. The basic theory provided in (Hershberg *et al.*, 2012) is first presented and elaborated upon. The theory is presented in the paper using a first-order model. In this report, this theory is extended to include effects like slewing and parasitic capacitances. For simplicity, the voltages V_{CMX}, V_{CM}, V_{CMO} in figure (2.2) and the trip-points of all inverters are assumed to be $\frac{V_{DD}}{2}$; and the capacitances C_1, C_2 and C_3 are assumed to be infinite capacitances. The following work is done for the case of negative input voltage V_{IN}. It can be similarly extended to positive input voltages also.

(Hershberg *et al.*, 2012) divides the ring amplification in $\overline{RST}$ into the following 3 phases:

- Initial Ramping (from **50 ns to 52.77 ns** in figure (2.4))
- Stabilization (from **52.77 ns to 70.84 ns** in figure (2.4))
- Steady State (from **70.84 ns to 100 ns** in figure (2.4))

2.2.1 Initial Ramping

Just as the $\overline{RST}$ phase starts, the voltage on the left plate of C_A changes from V_{IN}, the input voltage to 0. Consequently, there is a change in the voltage V_X, V_1 and V_{OUT},

given by

$$\begin{aligned}
\Delta V_X = \Delta V_1 &= -\frac{C_A \Delta V_{IN}}{C_A + \dfrac{C_B C_{LOAD}}{C_B + C_{LOAD}}} \\
&= -\frac{C_A (C_B + C_{LOAD}) \Delta V_{IN}}{C_A C_B + C_A C_{LOAD} + C_B C_{LOAD}} \\
\Delta V_{OUT} &= \frac{C_B \Delta V_X}{C_B + C_{LOAD}} \\
&= -\frac{C_A C_B \Delta V_{IN}}{C_A C_B + C_A C_{LOAD} + C_B C_{LOAD}}
\end{aligned} \tag{2.3}$$

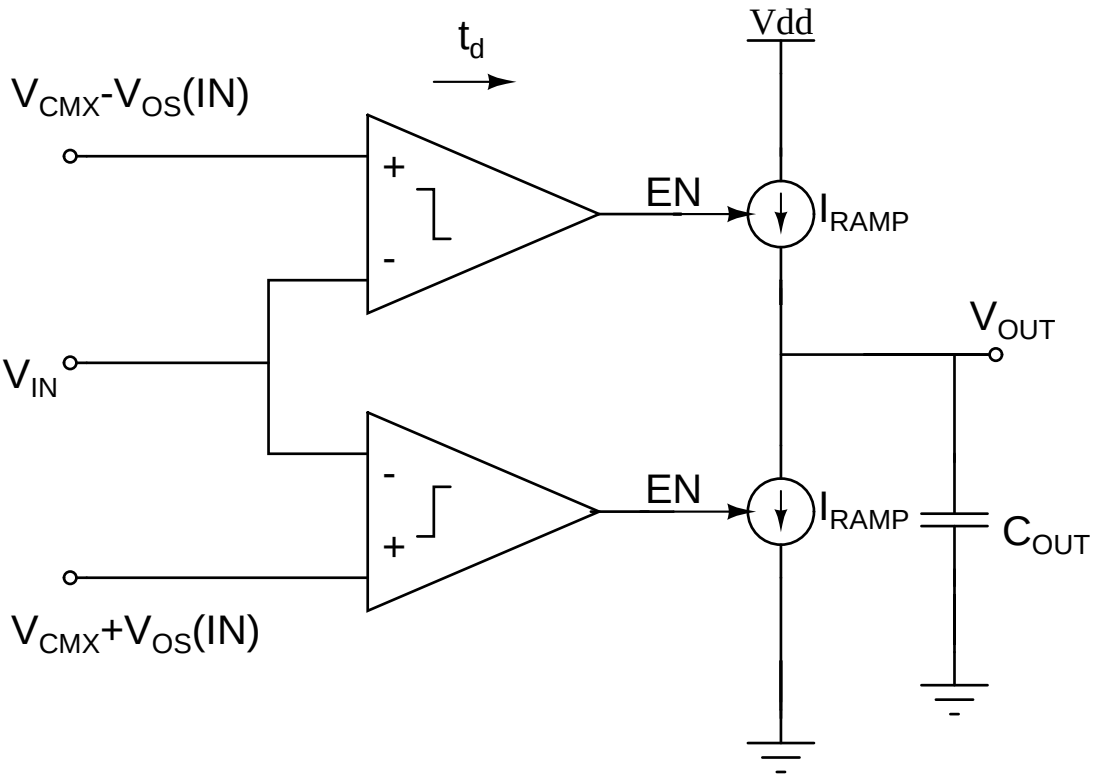


Figure 2.5: Ring amplifier in ramping phase

For the case of negative input voltage considered above, V_{OUT}, V_X and V_1 increase to $V_{OUT}+\Delta V_{OUT}, V_X+\Delta V_X$ and $V_1+\Delta V_1$ as soon as $\overline{RST}$ starts. After a small delay (due to parasitic capacitances), V_A goes very close to ground voltage, and $V_{2B} = V_A + V_{OS}$. Thus, $V_{BN} \approx V_{DD}$, and the transistor M_{CN} is maximally biased.

Now, V_{OUT} starts ramping down towards its steady state value of $\frac{V_{DD}}{2} + \frac{C_A}{C_B} V_{IN}$, as given by equation (2.2). Similarly, V_X and V_1 start ramping down towards $\frac{V_{DD}}{2}$. In this phase, the ring amplifier behaves like a pair of bi-directional continuous time comparators, as shown in figure (2.5). This ramping phase is supposed to end as soon V_X

reaches one of the comparator thresholds. (In case of negative inputs, this threshold is $V_X + \frac{V_{OS}}{A_1}$). However, due to the parasitic capacitances in the circuit, there is a propagation delay (t_d) from the node V_X to the node V_{OUT} of the circuit. Thus, there is an overshoot of V_X and hence V_1 and V_{OUT} beyond the comparator threshold. Denoting the ramp rate of the output node by r_0, the overshoot of V_{OUT} is given by,

$$\Delta V_{OUT,overshoot} = r_0 t_d \tag{2.4}$$

where, $r_0 = \frac{I_{OUT}}{C_{OUT}}$. I_{OUT} is calculated for a maximally biased M_{CN} with an output voltage equal to its steady state value of $\frac{V_{DD}}{2} + \frac{C_A}{C_B}V_{IN}$. As the gate of M_{CN} is maximally biased with V_{DD} and V_{OUT} is clearly less than V_{DD} (for the case of negative input considered here), it is obvious that M_{CN} is in the triode region of operation. The following are the expressions for I_{OUT} and C_{OUT}.

$$\begin{aligned} I_{OUT} &= \mu_n C_{OX}\frac{W}{L}\left((V_{DD} - V_{TN})V_{OUT} - \frac{V_{OUT}^2}{2}\right) \\ C_{OUT} &= C_{LOAD} + \frac{C_A C_B}{C_A + C_B} \end{aligned} \tag{2.5}$$

It is more useful (as will be seen later) to find out the input referred overshoot with respect to the mid-rail voltage, that is the overshoot of V_X with respect to $\frac{V_{DD}}{2}$. This is denoted by $v_{\text{overshoot},0}$.

$$v_{\text{overshoot},0} = r_0 t_d \frac{C_B}{C_A + C_B} - \frac{V_{OS}}{A_1} \tag{2.6}$$

2.2.2 Stabilization phase

After the initial ramping is done, the circuit oscillates/rings around its steady state value. If there is no offset voltage, the circuit keeps ringing infinitely with amplitude $v_{\text{overshoot},0}$ given by equation (2.6). An increased offset voltage means a higher chance of settling. The circuit settles if its final, steady state V_X satisfies the inequality (2.1).

A fundamental requirement for the circuit to settle is the progressive reduction in the gate overdrive voltages of transistors M_{CN} and M_{CP}. In the initial ramping phase, the gate was maximally biased and the output current was given by equation (2.5). This led to an overshoot of V_X beyond the comparator threshold $\left(\frac{V_{DD}}{2} + \frac{V_{OS}}{A_1}\right)$. If the V_X

overshoots the other threshold $\left(\frac{V_{DD}}{2} - \frac{V_{OS}}{A_1}\right)$, the circuit doesn't settle in that ring. If the gate overdrive in the next ring doesn't decrease and continues to remain V_{DD}, the rate of change of V_{OUT}, V_X and V_1 remain the same. From equation (2.6) and (2.4), it is apparent that the overshoot with respect to mid-rail voltage also continues to remain the same. Thus, the circuit will never settle if there is no progressive reduction of overdrive voltage. This is illustrated in figures (2.6) and (2.7). The first order model of the steady state solution is presented before the condition for progressive reduction of overdrive voltage is revisited.

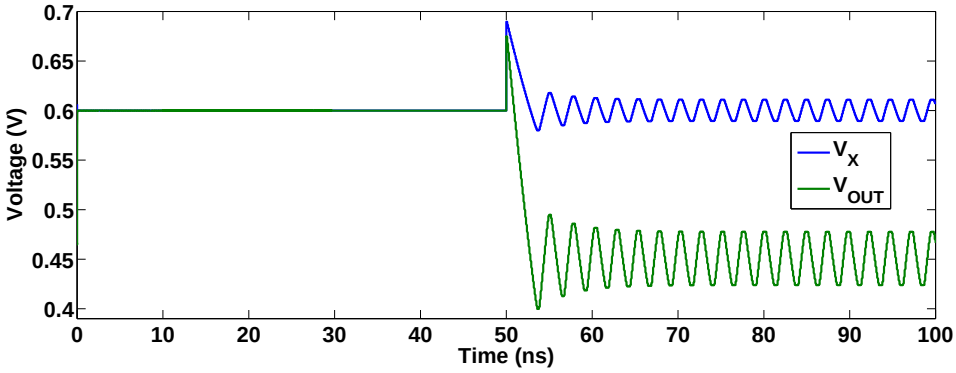


Figure 2.6: V_X, V_{OUT} v/s time for V_{OS} = 50 mV. The circuit doesn't settle

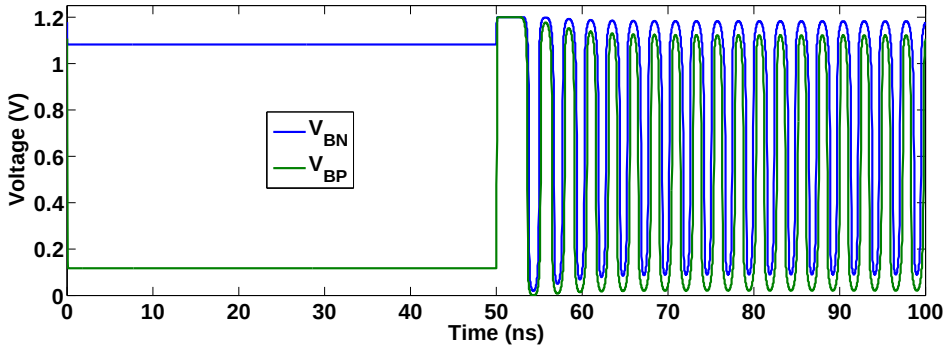


Figure 2.7: V_{BN}, V_{BP} v/s time for V_{OS} = 50 mV. The circuit doesn't settle as there is no progressive reduction in overdrive voltage.

2.3 First order model of steady state solution

2.3.1 Some Notations

Some notations which will be used in this section are introduced.

- $v_{\text{overshoot},i}$ is the amount of input referred overshoot (with respect to mid-rail voltage) when the NMOS transistor M_{CN} is active for the i^{th} time during the ringing phase.

- $v'_{\text{overshoot},i}$ is the amount of input referred overshoot with respect to mid-rail voltage) when the PMOS transistor M_{CP} is active for the i^{th} time during the ringing phase.

- r_i is the rate at which the the output node voltage V_{OUT} falls when the NMOS transistor M_{CN} is active for the i^{th} time during the ringing phase.

- r'_i is the rate at which the the output node voltage V_{OUT} falls when the PMOS transistor M_{CP} is active for the i^{th} time during the ringing phase.

- $t_{dz,i}$ is the time for which the circuit remains in dead-zone after the NMOS transistor was active for the i^{th} time. That is, it is the time for which the node voltage V_X stays at $\frac{V_{DD}}{2} - v_{\text{overshoot},i}$.

- $t'_{dz,i}$ is the time for which the circuit remains in dead-zone after the PMOS transistor was active for the i^{th} time. That is, it is the time for which the node voltage V_X stays at $\frac{V_{DD}}{2} + v_{\text{overshoot},i}$.

- $t_{cr,i}$ is the time taken by the circuit to cross from one dead-zone to another. This is the crossing in which NMOS transistor M_{CN} is active for the i^{th} time. In other words, $t_{cr,i}$ is the time taken for V_X to go from $v'_{\text{overshoot},i-1}$ to $v_{\text{overshoot},i}$. $t_{cr,0}$ is defined as the time taken by node V_X to cross from its initial threshold crossing of $\frac{V_{DD}}{2} + \frac{V_{OS}}{A_1}$ to $v_{\text{overshoot},0}$.

- $t'_{cr,i}$ is the time taken by the circuit to cross from one dead-zone to another. This is the crossing in which PMOS transistor M_{CP} is active for the i^{th} time. In other words, $t'_{cr,i}$ is the time taken for V_X to go from $v_{\text{overshoot},i}$ to $v'_{\text{overshoot},i}$.

- The index i in the above mentioned notation runs from 0.

The magnitude of the first input referred overshoot (on the negative side of mid-rail voltage) with respect to mid-rail voltage was evaluated in equation (2.6). Now, the circuit remains in dead-zone for $t_{dz,i}$. Next, the first input referred overshoot (with

respect to mid-rail) on the positive side of mid-rail voltage is computed.

$$v'_{overshoot,0} = r'_0 t_d \frac{C_B}{C_A + C_B} - \frac{V_{OS}}{A_1} \tag{2.7}$$

The rate r'_0 is calculated in the following manner using incremental analysis. The incremental voltage at the gate of inverter A_1 is the overshoot voltage calculated in equation (2.6). Now, the incremental voltage at the gate of inverter A_2, v_{2T} is given by

$$\begin{aligned} v_{2T} &= v_{overshoot,0} A_1 \\ &= \left(r_0 t_d \frac{C_B}{C_A + C_B} - \frac{V_{OS}}{A_1} \right) A_1 \end{aligned} \tag{2.8}$$

The incremental voltage at the gate of inverter M_{CP}, v_{BP} is given by

$$\begin{aligned} v_{BP} &= v_{2T} A_2 \\ &= \left(r_0 t_d \frac{C_B}{C_A + C_B} - \frac{V_{OS}}{A_1} \right) A_1 A_2 \end{aligned} \tag{2.9}$$

The rate is given by

$$\begin{aligned} r'_0 &= \left(r_0 t_d \frac{C_B}{C_A + C_B} - \frac{V_{OS}}{A_1} \right) A_1 A_2 k_p \\ k_p &= \frac{g_{m,M_{CP}}}{C_L + \dfrac{C_A C_B}{C_A + C_B}} \end{aligned}$$

By similar arguments, a pair of difference equations for r_i and r'_i is constructed.

$$\begin{aligned} r_i &= \left(r'_{i-1} t_d \frac{C_B}{C_A + C_B} - \frac{V_{OS}}{A_1} \right) A_1 A_2 k_n \\ k_n &= \frac{g_{m,M_{CN}}}{C_L + \dfrac{C_A C_B}{C_A + C_B}} \\ r'_i &= \left(r_i t_d \frac{C_B}{C_A + C_B} - \frac{V_{OS}}{A_1} \right) A_1 A_2 k_p \\ k_p &= \frac{g_{m,M_{CP}}}{C_L + \dfrac{C_A C_B}{C_A + C_B}} \end{aligned} \tag{2.10}$$

By solving above difference equations,

$$r_i = ((A_1A_2t_d)^2k_pk_n\psi^2)^i\left(r_0 + \frac{V_{OS}A_2k_n(1+k_pt_dA_1A_2\psi)}{1-(A_1A_2t_d)^2k_pk_n\psi^2}\right) - \frac{V_{OS}A_2k_n(1+k_pt_dA_1A_2\psi)}{1-(A_1A_2t_d)^2k_pk_n\psi^2} \tag{2.11}$$

where, ψ is the feedback factor and is given by

$$\psi = \frac{C_B}{C_A + C_B} \tag{2.12}$$

Similarly for r_i', the rate of change of V_{OUT} when the PMOS transistor M_{CP} is active, is given by

$$r_i' = ((A_1A_2t_d)^2k_pk_n\psi^2)^i\left(r_0' + \frac{V_{OS}A_2k_n(1+k_pt_dA_1A_2\psi)}{1-(A_1A_2t_d)^2k_pk_n\psi^2}\right) - \frac{V_{OS}A_2k_n(1+k_pt_dA_1A_2\psi)}{1-(A_1A_2t_d)^2k_pk_n\psi^2} \tag{2.13}$$

Now, for the circuit to settle to steady state, the overshoot with respect to the mid-rail must be less than $\frac{V_{OS}}{A_1}$.

If the NMOS transistor M_{CN} is active during the last ring, the following condition must hold for the circuit to settle.

$$\begin{aligned} r_it_d\psi - \frac{V_{OS}}{A_1} &< \frac{V_{OS}}{A_1} \\ r_i &< \frac{2V_{OS}}{A_1t_d} \times \left(1 + \frac{C_A}{C_B}\right) \end{aligned} \tag{2.14}$$

If the PMOS transistor M_{CP} is active during the last ring, the condition changes to the following.

$$\begin{aligned} r_i't_d\psi - \frac{V_{OS}}{A_1} &< \frac{V_{OS}}{A_1} \\ r_i' &< \frac{2V_{OS}}{A_1t_d} \times \left(1 + \frac{C_A}{C_B}\right) \end{aligned} \tag{2.15}$$

In the above expressions, A_1 should actually be replaced by $\tilde{A}_1$, the instantaneous gain of the first stage inverter and is few times smaller than the actual steady state saturation gain due to the effects of slewing which will be considered in the next section. The inverter A_1 is in the high-gain region (of the inverter characteristics) where both the PMOS ans NMOS transistors are in saturation region.

As observed later in figure (2.8), for most of the time , $V_{BN} > V_{DD} - V_{TP}$ and $V_{BP} < V_{TN}$. That is, for most part of the clock cycle, the second stage inverter is in the "low-gain region". That is, one of the PMOS or NMOS is in saturation and the other is in triode. Also, as discussed in detail in section 3.1.1 on delays and parasitic capacitances, the delay of stage 2 inverter is much less than the delay of stage 1 inverter. Hence, the slewing effects of second stage inverter can be neglected.

As stated in the previous paragraph, for most of the time $V_{DD} - V_{TP} < V_{BN} < V_{DD}$. The output voltage V_{OUT} of the circuit is $V_{DD} + \frac{C_A}{C_B} V_{IN}$. In case of negative input voltages being discussed here, $V_{OUT} < \frac{V_{DD}}{2}$. Hence, for most of the ramping and stabilization phases, the transistor M_{CN} is in triode region. This has been used in deriving the above rate expressions.

Similarly, for most of the time $0 < V_{BP} < V_{TN}$. The output voltage V_{OUT} of the circuit is $V_{DD} + \frac{C_A}{C_B} V_{IN}$. In case of small negative input voltages (such that $V_{OUT} > V_{BP} + V_{TP}$), for most of the ramping and stabilization phases, the transistor M_{CP} is in triode region. For higher negative inputs, the calculations above can be modified appropriately using $g_{m,M_{CP}}$ as the saturation transconductance.

Next, the expressions for time for each dead-zone crossing $t_{dz,i}$, $t'_{dz,i}$ and the time taken from one dead-zone crossing to the other $t_{cr,i}$, $t'_{cr,i}$ are computed. t_d, the inherent delay in the "comparator" is the reason for the overshoot from $\frac{V_{DD}}{2} \pm \frac{V_{OS}}{A_1}$. From the definitions of $t_{cr,i}$ and $t'_{cr,i}$ above, the above two quantities are written in terms of $v'_{overshoot,i}$ and $v_{overshoot,i}$.

$$
\begin{aligned}
t_{cr,i} &= t_d \frac{\frac{V_{OS}}{A_1} + v_{overshoot,i}}{v'_{overshoot,i-1} + v_{overshoot,i}} \\
t'_{cr,i} &= t_d \frac{\frac{V_{OS}}{A_1} + v'_{overshoot,i}}{v_{overshoot,i} + v'_{overshoot,i}}
\end{aligned}
\tag{2.16}
$$

For the circuit to cross the i^{th} dead-zone after a transition phase where the NMOS was active, the node V_A must go from $\frac{V_{DD}}{2} - V_{OS}$ to $\frac{V_{DD}}{2} + V_{OS}$. The incremental current through the drain of A_1 is $g_{m1} v_{overshoot,i}$. The capacitor is $2C'_1$. Therefore, by approximating that the node voltage V_A charges/discharges by a constant current which is g_m times the overshoot, the following expressions for $t_{dz,i}$ and $t'_{dz,i}$ are obtained.

Using a linear rate approximation, $t_{dz,i}$ is given as

$$t_{dz,i} = \frac{4V_{OS}C'}{g_{m1}v_{overshoot,i}} \tag{2.17}$$

Similarly,

$$t'_{dz,i} = \frac{4V_{OS}C'}{g_{m1}v'_{overshoot,i}} \tag{2.18}$$

2.4 Including slewing effects

The gain term A_1 referred to in the previous section is not the actual steady state gain, but is actually few times less than the actual value. This reduction in gain is due to slewing. The presence of the parasitic capacitance is the main reason for slewing.

When there is an overshoot of $v_{overshoot,i}$ below $\frac{V_{DD}}{2}$ at the node voltage V_X, the node voltage V_A doesn't shoot up by $A_1 v_{overshoot,i}$. Node voltage V_X remains at $\frac{V_{DD}}{2} - v_{overshoot,i}$ for a time $t_{dz,i}$. This is equivalent to a step incremental voltage of $v_{overshoot,i}$ applied at node V_X for time $t_{dz,i}$.

$$g_{m1}v_{overshoot,i} = g_{ds1}v_A + 2C'\frac{dv_A}{dt} \tag{2.19}$$

It is known that the steady state gain of stage 1 inverter A_1 is $\frac{g_{m1}}{g_{ds1}}$. Solving the differential equation (2.19),

$$v_A = A_1(1 - e^{-\frac{t_{dz,i}g_{ds,1}}{2C'}})v_{overshoot,i} \tag{2.20}$$

Therefore, the reduced gain $\tilde{A_1}$ is given by

$$\tilde{A_1} = A_1(1 - e^{-\frac{t_{dz,i}g_{ds,1}}{2C'}}) \tag{2.21}$$

It is apparent that the equations for instantaneous gain (2.21) and the equation for dead-zone time (2.17) seem to have been derived similarly. Both are approximate expressions, which work approximately as illustrated by several simulations, and provide considerable insight. Finding exact expressions would be a very tedious task which gives no insight, as the two quantities are highly co-dependent. A detailed explanation of the co-dependence is provided below.

There is a small time delay at the second stage inverter, which has been neglected for convenience. Thus, the actual time at which circuit enters dead-zone is a small time delay (t_{d2}) after the time at which V_A becomes $\frac{V_{DD}}{2} - V_{OS}$. Similarly, the time at which the circuit leaves dead-zone is a small time delay after the time at which V_A becomes $\frac{V_{DD}}{2} + V_{OS}$. At the time at which the circuit enters dead-zone, $V_A > \frac{V_{DD}}{2} - V_{OS}$, but need not be equal to $\frac{V_{DD}}{2}$ as assumed in the above calculation. Also, the voltage V_A continues to rise, though to a smaller extent, even after the circuit leaves dead-zone as the sign of the incremental voltage is still same.

That is, the node voltage V_X becomes $\frac{V_{DD}}{2}$ at time $\frac{t_{dz,i}}{2} - t_{d2}$. The time for which circuit remains in dead-zone after V_X reaches $\frac{V_{DD}}{2}$ is not $\frac{t_{dz,i}}{2}$, but $\frac{t_{dz,i}}{2} + t_{d2}$ after taking into account the small delay of the second stage inverter. Thus, the actual expression for $\tilde{A_1}$ would look like

$$\tilde{A_1} = A_1 \left(1 - e^{-\frac{\left(\frac{t_{dz,i}}{2} + t_{d2} + t_{dnz}\right) g_{ds,1}}{2C'}} \right) \tag{2.22}$$

where t_{dnz} is the factor to account for the time during which circuit leaves dead-zone, but V_A continues to rise. The equation (2.21) provides a reasonably accurate approximation of equation (2.22), as verified by several simulations.

2.5 Conditions for progressive reduction in overdrive voltage

For a V_{OS} of 150 mV, the circuit settles within $\frac{T_S}{2}$, as already seen in figure (2.4). This happens due to the progressive reduction in gate overdrive voltages V_{BN} and V_{BP}. This is illustrated in figure (2.8).

As seen before, the first overshoot of V_X (on the negative side of $\frac{V_{DD}}{2}$ with respect to mid-rail voltage is given by

$$v_{\text{overshoot},0} = r_0 t_d \frac{C_B}{C_A + C_B} - \frac{V_{OS}}{A_1} \tag{2.23}$$

The incremental voltage v_{2T} was calculated in equation (2.8). The node voltage V_{2T} is

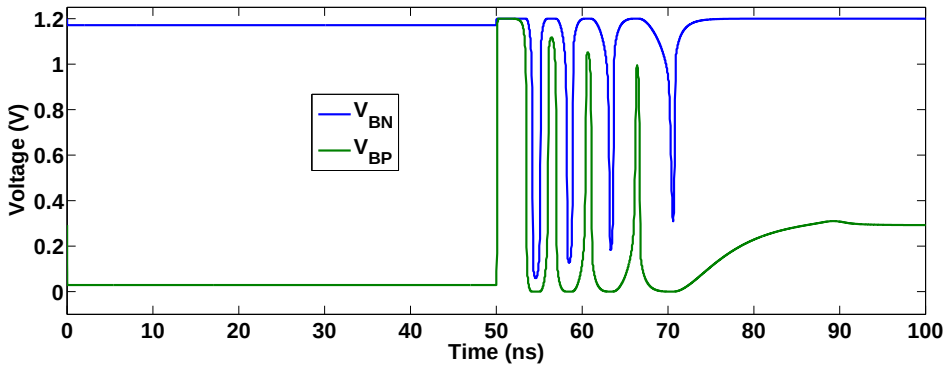


Figure 2.8: Progressive reduction in overdrive voltages

given by

$$V_{2T} = \frac{V_{DD}}{2} + \tilde{A}_1 v_{\text{overshoot},0} - V_{OS}$$

Hence, the voltage V_{BP} is given by

$$V_{BP} = f(V_{2T}) = f\left(\frac{V_{DD}}{2} + \tilde{A}_1 v_{\text{overshoot},1} - V_{OS}\right) \tag{2.24}$$

where, f is the inverter's large signal transfer function.

Now, condition for the ring amplifier to settle is derived. As mentioned in section (2.2.2), for the ring amplifier to settle, the overdrive voltages V_{BP} and V_{BN} must lower progressively from the rail voltages. Therefore, V_{BP} needs to go significantly above ground, so that the gate overdrive voltage of the M_{CP} transistor goes below V_{DD}. The condition thus required is,

$$\begin{aligned} &\frac{V_{DD}}{2} + \tilde{A}_1 v_{\text{overshoot}} - V_{OS} < V_{DD} - V_{TP} \\ &\tilde{A}_1 v_{\text{overshoot},1} < \frac{V_{DD}}{2} - V_{TP} + V_{OS} \end{aligned} \tag{2.25}$$

Substituting the expression for instantaneous gain obtained in equation (2.21),

$$A_1(1 - e^{-\frac{t_{dz,i} g_{ds,1}}{2C'}}) v_{\text{overshoot},0} < V_{DD} - V_{TP} + V_{OS} \tag{2.26}$$

The set of equations for the second overshoot of V_X (on the positive side of $\frac{V_{DD}}{2}$ with

respect to mid-rail voltage is derived below

$$
\begin{aligned}
&v'_{\text{overshoot},0} = r'_0 t_d \frac{C_B}{C_A + C_B} - \frac{V_{OS}}{A_1} \\
&V_A = \frac{V_{DD}}{2} - \tilde{A}_1 v'_{\text{overshoot},0} \\
&\tilde{A}_1 = A_1(1 - e^{-\frac{t'_{dz,0} g_{ds,1}}{2C'}}) \\
&V_{2B} = \frac{V_{DD}}{2} - \tilde{A}_1 v'_{\text{overshoot},0} + V_{OS} \\
&V_{BN} = f(V_{2B}) = f\left(\frac{V_{DD}}{2} - \tilde{A}_1 v'_{\text{overshoot},0} + V_{OS}\right) \\
&\frac{V_{DD}}{2} - \tilde{A}_1 v'_{\text{overshoot},0} + V_{OS} > V_{TN} \\
&\tilde{A}_1 v'_{\text{overshoot},0} < \frac{V_{DD}}{2} - V_{TN} + V_{OS} \\
&A_1(1 - e^{-\frac{t'_{dz,i} g_{ds,1}}{2C'}}) v_{\text{overshoot},0} < V_{DD} - V_{TN} + V_{OS}
\end{aligned}
\tag{2.27}
$$

2.6 Approximate number of rings in the circuit

From the (2.11) and (2.13), the equations of rate of change of V_{OUT} when the NMOS or PMOS is active for the i^{th} time; and (2.14) and (2.15), the conditions which the rates have to satisfy for the circuit to enter dead-zone, the following expression for number of rings is derived.

$$
\begin{aligned}
n_1 &= \frac{1}{\ln((A_1 A_2 t_d \psi)^2 k_p k_n)} \ln\left(\frac{\frac{2V_{OS}}{A_1 t_d} + \frac{V_{OS} A_2 k_n (1 + k_p t_d A_1 A_2 \psi)}{1 - ((A_1 A_2 t_d \psi)^2 k_p k_n)}}{r_0 + \frac{V_{OS} A_2 k_n (1 + k_p t_d A_1 A_2 \psi)}{1 - ((A_1 A_2 t_d \psi)^2 k_p k_n)}}\right) \\
n_2 &= \frac{1}{\ln((A_1 A_2 t_d \psi)^2 k_p k_n)} \ln\left(\frac{\frac{V_{OS}}{A_1 t_d} + \frac{2V_{OS}}{A_1^2 A_2 k_p \psi t_d^2} + \frac{V_{OS} A_2 k_n (1 + k_p t_d A_1 A_2 \psi)}{1 - ((A_1 A_2 t_d \psi)^2 k_p k_n)}}{r_0 + \frac{V_{OS} A_2 k_n (1 + k_p t_d A_1 A_2 \psi)}{1 - ((A_1 A_2 t_d \psi)^2 k_p k_n)}}\right) \\
N &= \min(2n_1, 2n_2 - 1)
\end{aligned}
\tag{2.28}
$$

The equation for n_1 gives half the number of rings if the NMOS is active during the last ring. The equation for n_2 gives half the number of rings if in the last ring, PMOS is active. The required number of rings is the minimum of the two. In the above expressions, if the steady state gain A_1 is used, the number of rings will be much higher than the actual number of rings. The number of rings may also turn out to be infinite

(which would imply the circuit doesn't settle). Using the instantaneous gain $\tilde{A_1}$ at the end of the first overshoot (equation (2.21)) gives a lower bound on the number of rings. Using the instantaneous gain at the end of first overshoot and approximating the gain A_2 as a constant by appropriate piece-wise linear approximations of inverter characteristics in low-gain region gives a reasonably insightful expression of the number of rings.

2.6.1 Variation of number of rings with V_{OS}

From equation (2.28), it is inferred that while keeping all other parameters constant and varying only V_{OS}, the number of rings as a function of V_{OS} is of the form

$$N = \frac{\ln\left(\frac{\alpha V_{OS}}{r_0 + \beta V_{OS}}\right)}{\ln\gamma} \tag{2.29}$$

That is, for circuits which settle, the number of rings reduces with V_{OS} in the manner

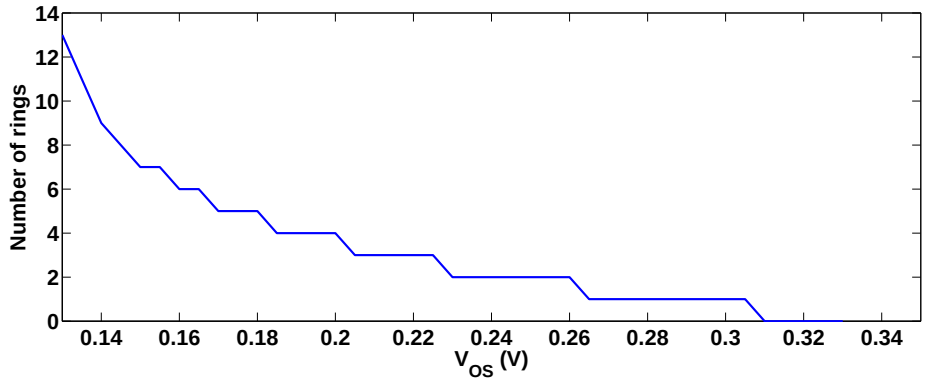


Figure 2.9: Number of rings vs V_{OS}

observed in figure (2.9) (since $\gamma = (A_1 A_2 t_d \psi)^2 k_p k_n < 1$ for circuits which settle). The plot in figure (2.9) shows the variation of number of rings versus V_{OS} for a LEVEL 1 model with the following parameters.

$$V_{DD} = 1.2\ \text{V}$$

$$C_A = 1.5\ \text{pF}$$

$$C_B = 1\ \text{pF}$$

$$C_{LOAD} = 0.2\ \text{pF}$$

For all inverters,

$$\frac{W}{L} \text{ of NMOS} = \frac{7.2}{2.4}$$
$$\frac{W}{L} \text{ of PMOS} = \frac{21.6}{2.4}$$

For M_{CN},

$$\frac{W}{L} = \frac{3.2}{3.2}$$

For M_{CP}

$$\frac{W}{L} = \frac{9.6}{3.2}$$

All dimensions are in μm.

Some plots of V_X, V_{OUT} versus time (in the amplification phase) are shown for different offset voltages to illustrate the point of decreasing number of rings with V_{OS}.

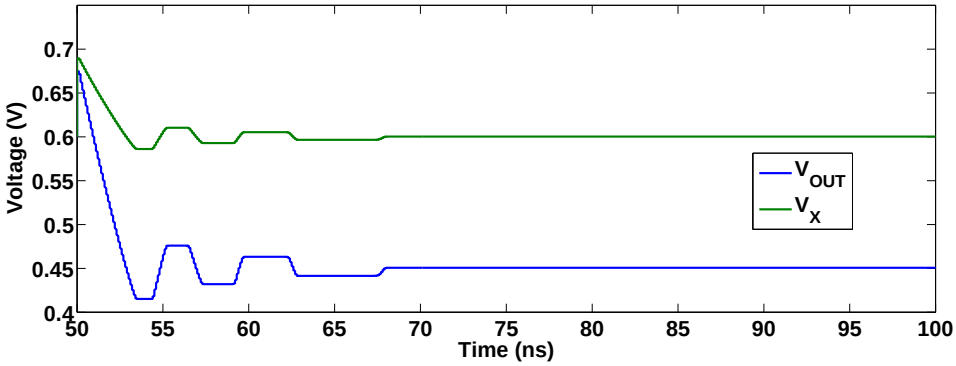


Figure 2.10: V_X, V_{OUT} v/s time for V_{OS} = 175 mV

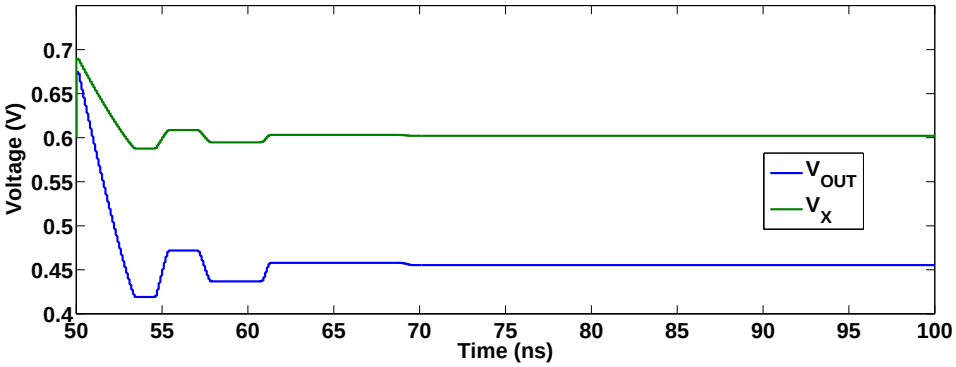


Figure 2.11: V_X, V_{OUT} v/s time for V_{OS} = 200 mV

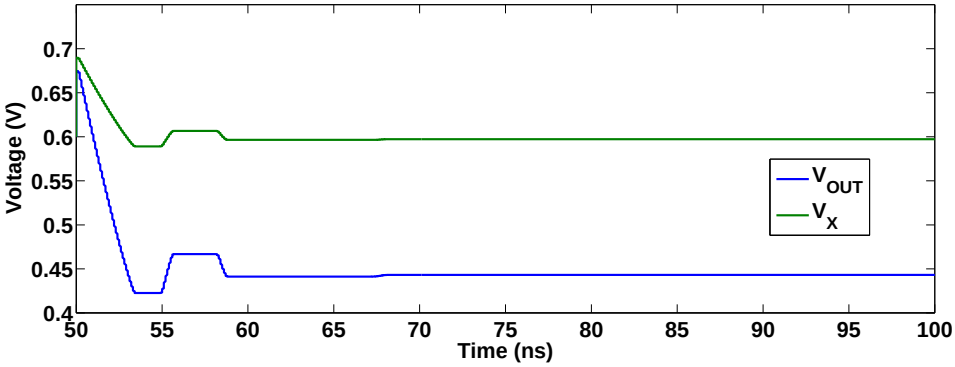


Figure 2.12: V_X, V_{OUT} v/s time for V_{OS} = 225 mV

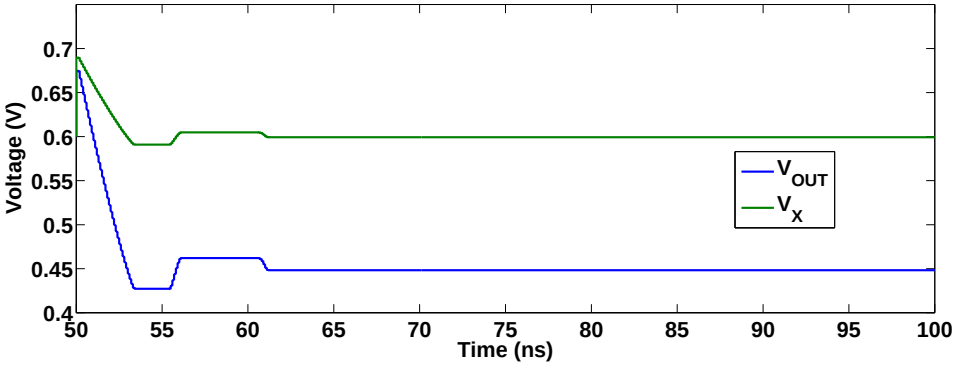


Figure 2.13: V_X, V_{OUT} v/s time for V_{OS} = 250 mV

2.6.2 Variation with C_{OUT}

From equation (2.28), the expression for number of rings in terms of C_{OUT} is dominated by the term in the denominator $\ln\left(\frac{(A_1A_2t_d)^2\psi^2 g_{m,M_{CN}} g_{m,M_{CP}}}{C_{OUT}^2}\right)$. Also there is a complicated dependence on C_{OUT} in the numerator of the form

$$\ln\left(\frac{\alpha+\frac{\beta}{C_{OUT}^2}+\frac{\gamma}{C_{OUT}}}{r_0+\frac{\delta}{C_{OUT}^2}+\frac{\gamma}{C_{OUT}}}\right)$$

The plot in figure (2.14) shows the variation of number of rings versus C_{LOAD} (which is directly related to C_{OUT}) for a LEVEL 1 model with the following parameters.

$$V_{DD} = 1.2\text{ V}$$

$$C_A = 1.5\text{ pF}$$

$$C_B = 1\text{ pF}$$

$$V_{OS} = 0.15\text{ V}$$

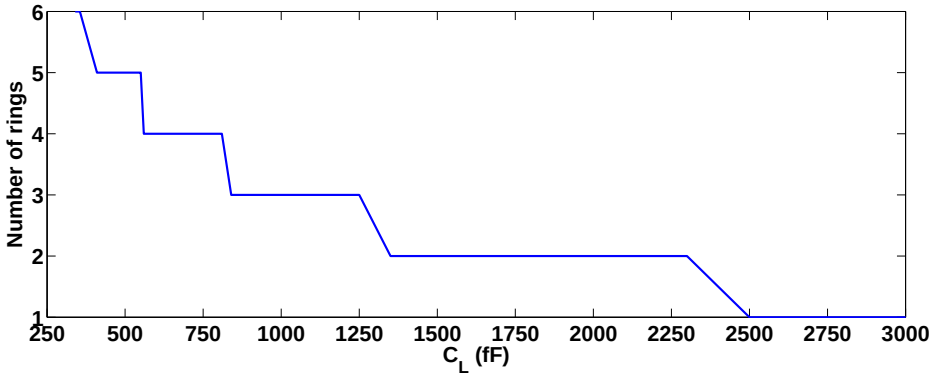


Figure 2.14: Number of rings vs C_{LOAD}

CHAPTER 3

Design of Ring Amplifier

Before stating the procedure to design lengths and widths of transistors in a ring amplifier, some preliminaries are stated. These preliminaries are useful in rationalizing the tweaking (in lengths and widths) required for a design which settles.

3.1 Preliminaries

3.1.1 Parasitic capacitances and delays

First, an approximate model for the various parasitic capacitances is given.

Each parasitic capacitance is modelled as proportional to the width of the transistor.

For the inverter A_1,

$$\begin{aligned} &\text{Gate capacitance} = C_{A_1,G}W_1 \\ &\text{Drain capacitance} = C_{A_1,D}W_1 \\ &\text{Output resistor} = \frac{b_1}{W_1} \end{aligned} \tag{3.1}$$

Both $C_{A_1,G}$ and $C_{A_1,D}$ have few components proportional to the length L_1 of the transistor. W_1 is the sum of widths of the NMOS and PMOS transistor making up the inverter. And $b_1 = \dfrac{2L_1}{\lambda\mu C_{OX}\frac{W}{L}\left(\frac{V_{DD}}{2} - V_T\right)^2}$, as the first stage inverter is in the "high-gain" region where both NMOS and PMOS are in saturation. Also, it is observed from simulation that $C_{A_1,D}$ is significantly less than $C_{A_1,G}$. That is, the drain capacitance is significantly less than the gate capacitance.

Similarly for inverter A_2,

$$\begin{aligned} &\text{Gate capacitance} = C_{A_2,G}W_2 \\ &\text{Drain capacitance} = C_{A_2,D}W_2 \\ &\text{Output resistor} = \frac{b_2}{W_2} \end{aligned} \tag{3.2}$$

As second stage inverter is mostly in low-gain region (1 transistor in saturation and other in triode), the output resistor is significantly less than that of first stage. That is, b_2 is significantly less than b_1.

For the M_{CN} and M_{CP} respectively,

$$\begin{aligned} \text{NMOS Gate capacitance} &= C_N W_N \\ \text{PMOS Gate capacitance} &= C_P W_P \end{aligned} \tag{3.3}$$

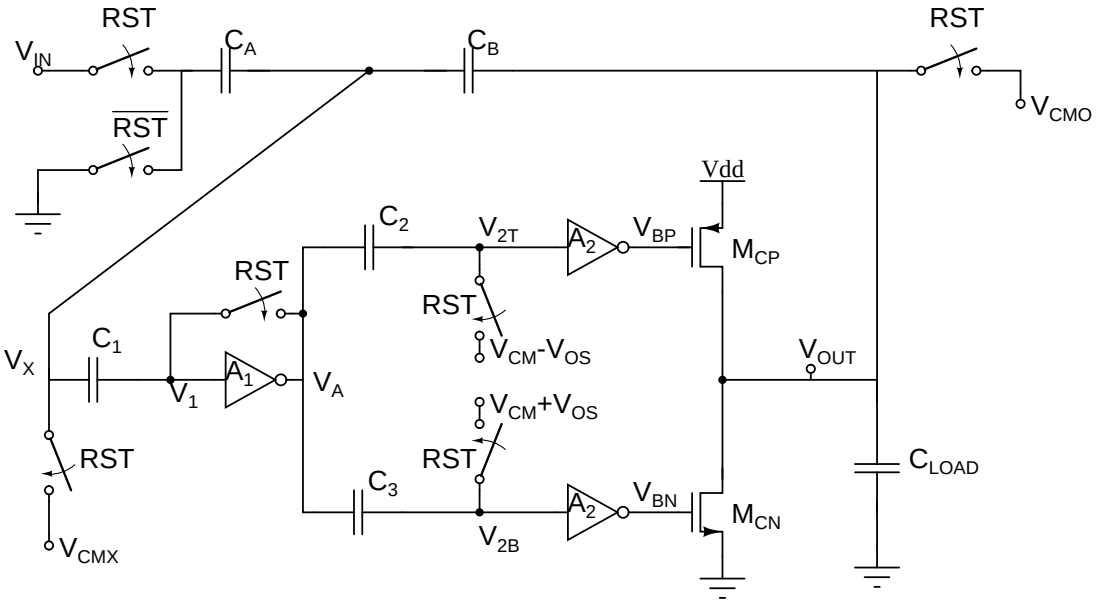
Now, the delays of the stages of inverters are computed. Delay of first stage is denoted by t_{d,A_1}, of the second stage is denoted by t_{d,A_2}.

$$\begin{aligned} t_{d,A_1} &\sim C_{OUT,A_1} r_{OUT,A_1} \\ C_{OUT,1} &= C_{A_1,D} W_1 + C_{A_2,G} W_2 \\ t_{d,A_1} &\sim b_1 C_{A_1,D} + b_1 C_{A_2,G} \frac{W_2}{W_1} \\ t_{d,A_2} &\sim C_{OUT,A_2} r_{OUT,A_2} \\ C_{OUT,2} &= C_{A_2,D} W_2 + C_N W_N \\ t_{d,A_2} &\sim b_2 C_{A_2,D} + b_2 C_N \frac{W_N}{W_2} \end{aligned} \tag{3.4}$$

In the case when PMOS transistor is active, the last expression of equation (3.4) becomes

$$t_{d,A_2} \sim b_2 C_{A_2,D} + b_2 C_P \frac{W_P}{W_2} \tag{3.5}$$

3.1.2 Steady state solution



The results derived in the previous chapter about progressive reduction in overdrive voltage are restated.

The rate at which V_{OUT} falls during the overshoot period after the initial ramping phase is given by

$$r_0 = \mu_n C_{OX} \frac{W}{L} \frac{(V_{DD} - V_{TN})}{C_{OUT}} \left(\frac{V_{DD}}{2} + \frac{C_A}{C_B} V_{IN} \right) \tag{3.6}$$

The set of equations for the first overshoot of V_X on the negative side of $\frac{V_{DD}}{2}$ with respect to mid-rail voltage is stated below

$$\begin{aligned}
v_{\text{overshoot},0} &= r_0 t_d \frac{C_B}{C_A + C_B} - \frac{V_{OS}}{A_1} \\
V_A &= \frac{V_{DD}}{2} + \tilde{A}_1 v_{\text{overshoot},0} \\
\tilde{A}_1 &= A_1 (1 - e^{-\frac{t_{dz,0} g_{ds,1}}{C_{OUT,A_1}}}) \\
V_{2T} &= \frac{V_{DD}}{2} + \tilde{A}_1 v_{\text{overshoot},0} - V_{OS} \\
V_{BP} &= f(V_{2T}) = f\left(\frac{V_{DD}}{2} + \tilde{A}_1 v_{\text{overshoot},0} - V_{OS} \right)
\end{aligned} \tag{3.7}$$

Now, using all the above equations together, a condition for the ring-amplifier to settle is derived. For the ring amplifier to settle, the overdrive voltages V_{BP} and V_{BN} must lower progressively from the rail voltages. Therefore, in the above case, V_{BP} must

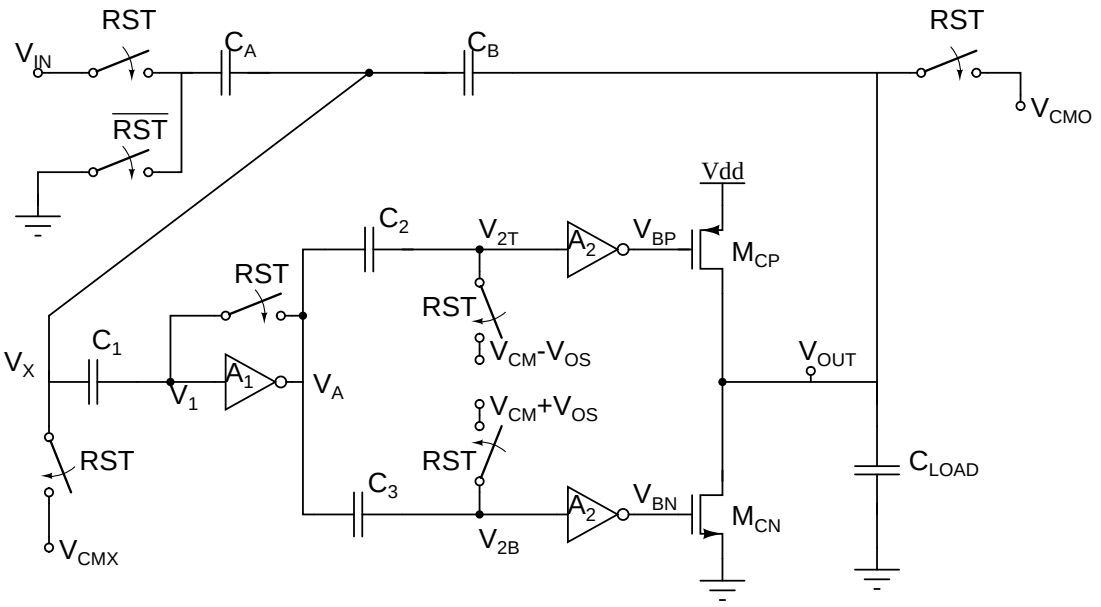
significantly above ground. That is, the gate overdrive voltage of the M_{CP} transistor must go below V_{DD}. The condition required for this is

$$\begin{aligned}
&\frac{V_{DD}}{2} + \tilde{A}_1 v_{\text{overshoot},0} - V_{OS} < V_{DD} - V_{TP} \\
&\tilde{A}_1 v_{\text{overshoot},0} < \frac{V_{DD}}{2} - V_{TP} + V_{OS} \\
&A_1(1 - e^{-\frac{t_{dz,i} g_{ds,1}}{C_{OUT,A_1}}}) v_{\text{overshoot},0} < V_{DD} - V_{TP} + V_{OS}
\end{aligned} \tag{3.8}$$

The set of equations for the first overshoot of V_X on the positive side of $\frac{V_{DD}}{2}$ with respect to mid-rail voltage is stated below

$$\begin{aligned}
&v'_{\text{overshoot},0} = r'_0 t_d \frac{C_B}{C_A + C_B} - \frac{V_{OS}}{A_1} \\
&V_A = \frac{V_{DD}}{2} - \tilde{A}_1 v'_{\text{overshoot},0} \\
&\tilde{A}_1 = A_1(1 - e^{-\frac{t'_{dz,0} g_{ds,1}}{C_{OUT,A_1}}}) \\
&V_{2B} = \frac{V_{DD}}{2} - \tilde{A}_1 v'_{\text{overshoot},0} + V_{OS} \\
&V_{BN} = f(V_{2B}) = f\left(\frac{V_{DD}}{2} - \tilde{A}_1 v'_{\text{overshoot},0} + V_{OS}\right) \\
&\frac{V_{DD}}{2} - \tilde{A}_1 v'_{\text{overshoot},0} + V_{OS} > V_{TN} \\
&\tilde{A}_1 v'_{\text{overshoot},0} < \frac{V_{DD}}{2} - V_{TN} + V_{OS} \\
&A_1(1 - e^{-\frac{t'_{dz,i} g_{ds,1}}{C_{OUT,A_1}}}) v_{\text{overshoot},0} < V_{DD} - V_{TN} + V_{OS}
\end{aligned} \tag{3.9}$$

3.2 Requirements for design



- The most important requirement for designing a ring amplifier which settles, is the progressive reduction of gate overdrive voltage of final stage transistors from the maximum possible V_{DD} to a voltage when they get cut-off. This requirement is given through equation (3.8) derived above.

$$\begin{aligned} A_1(1-e^{-\frac{t_{dz,i}g_{ds,1}}{C_{OUT,A_1}}})v'_{\text{overshoot},0} &< V_{DD}-V_{TN}+V_{OS} \\ A_1(1-e^{-\frac{t_{dz,i}g_{ds,1}}{C_{OUT,A_1}}})v_{\text{overshoot},0} &< V_{DD}-V_{TP}+V_{OS} \end{aligned} \tag{3.10}$$

- Next, it is observed from equation (3.7) that the overshoot voltage from mid-rail is proportional to delay in the circuit. The smaller the overshoot voltage, the higher the chances of settling in half clock-cycle $\left(\frac{T_S}{2}\right)$. So, it is desired to minimize the delay of the circuit. The delay of the circuit is the sum of delays of two stages derived above in equation (3.4). Also, it was mentioned before that the output resistance of the first stage inverter (in high gain region) is much higher than the second stage one. The 2 output capacitances are generally of the same order. So, the delay in first stage (t_{d,A_1}) is generally significantly higher than the delay in second stage inverter (t_{d,A_2}). So, it is important to minimize t_{d,A_1} in order to minimize the circuit delay.

- Also, from equation (3.7), it is noticed that the overshoot voltage is proportional to the rate at which the output node and hence the node V_X fall. So, it is important

to minimize the rate.

- The minimizations of delay and rate must be done for the first 2 overshoots. This requires some optimization.

3.3 A qualitative design procedure

Keeping in mind the above requirements, the following design procedure to make a ring-amp settle for a particular value of V_{OS}, is formulated. In this discussion, lengths and widths are chosen to make the ring amplifier settle for a fixed value of C_A, C_B, C_{LOAD} and V_{OS}. (The ring amplifier can be made to settle by increasing any of the parameters mentioned above).

- Minimum $\frac{W}{L}$ ratio means the rate of change voltage V_{OUT} is also minimum, as seen by equation (3.6). The width of the NMOS transistor M_{CN} is fixed at W_{min}, the minimum width allowed by the process. The length is also fixed at W_{min} so that $\frac{W}{L} = 1$. Now, the width and length of the PMOS transistor are also fixed at (W_{min}). Though the rate of change of voltage when PMOS and NMOS are active is asymmetric, smallest possible $\frac{W}{L}$ are ensured, thus rate of change of output voltage is as low as possible. If symmetry is desired, the length of the NMOS can be further increased, or the width of the PMOS can be increased. The former option of increasing length of NMOS is preferred so as to maintain similar delay times when NMOS and PMOS are active.

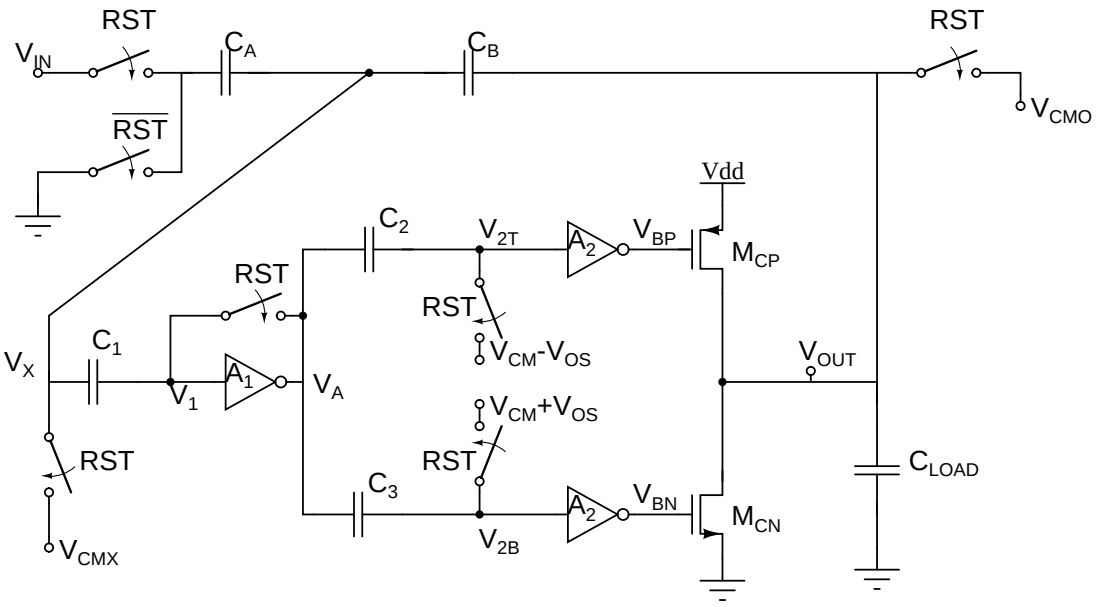
- Next, the lengths and widths of the transistors in the 2 inverters are determined. First, all transistor lengths in both stages are fixed at minimum (L_{min}) and widths of all NMOS transistors are fixed at W_{min}. Next, the PMOS width is fixed such that the trip point of the inverter is $\frac{V_{DD}}{2}$. (For TSMC 0.18 μm process used in the following examples, a good initial estimate would be L=180 nm for all transistors, W=270 nm for NMOS and W=1.08 μm for PMOS.) On fixing the minimum possible dimensions such that trip point is mid-rail voltage, the ring amplifier fails to settle in most cases. This is because the delay (and hence, the overshoot) given by equation (3.4) for the above dimensions, is too large to satisfy the condition for progressive reduction in overdrive voltage (3.8).

- The widths of transistors in first stage inverter and the length of the NMOS transistor of the final stage, i.e. M_{CN} are the parameters which can be tweaked. As seen from equation (3.4), increasing W_1 (width of transistors in stage 1 inverter) leads to smaller delay for stage 1 inverter. A good initial estimate would be $\sim$ 2-3 W_{min} for the NMOS transistor of first stage inverter, and $\sim$ 4 times the width of NMOS transistor for PMOS transistor. Now, as the transistor doesn't follow a simple square law model, equal ratios of $\frac{W_n}{W_p}$ in 2 different inverters doesn't ensure equal trip point for the two inverters. So after fixing the width of stage 1 transistors, the width of stage 2 transistors must also be changed so that they have same trip point (preferably $\frac{V_{DD}}{2}$). **This is a must**, as many calculations were done assuming a trip point of $\frac{V_{DD}}{2}$ for all inverters. An explanation for this necessity is that different trip point introduces an offset after the first stage inverter, which is not cancelled by C_1 as seen in section 2.1 on the structure of ring amplifiers.

- Further increase in length of M_{CN} leads to an decrease in rate and an increase in delay, as the C_N constant in equation (3.3) is length dependent. However, the first factor is more dominant, and hence increasing length increases the chance of settling.

- All the tweaking must be done for a small magnitude of input. If the circuit settles for a small input, it will certainly settle for larger inputs. Also, it must be done for a small value of offset voltage (V_{OS}). If the circuit settles for a small V_{OS} value, it will certainly settle for larger V_{OS} values, as illustrated in section (2.6.1).

3.4 Some examples to illustrate these rules



All examples are illustrated for the following case (in TSMC 0.18 μm technology, for a clock period of 200 ns). Only the amplifying phase of the clock cycle is shown in the graphs.

$$V_{DD} = 1.8\text{V}$$

$$C_A = 2\text{pF}$$

$$C_B = 1\text{pF}$$

$$C_L = 2\text{pF}$$

$$V_{OS} = 100\text{mV}$$

$$V_{IN} = -50\text{mV}$$

3.4.1 Example 1

All dimensions (in nm) were chosen keeping the first 2 points of the Design procedure.

For inverter A_1

$$\frac{W}{L} = \frac{1080}{180} \text{ for PMOS}$$
$$\frac{W}{L} = \frac{270}{180} \text{ for NMOS}$$

For the 2 inverters A_2

$$\frac{W}{L} = \frac{1080}{180} \text{ for PMOS}$$
$$\frac{W}{L} = \frac{270}{180} \text{ for NMOS}$$

For final stage

$$\frac{W}{L} = \frac{270}{270} \text{ for PMOS}$$
$$\frac{W}{L} = \frac{270}{540} \text{ for NMOS}$$

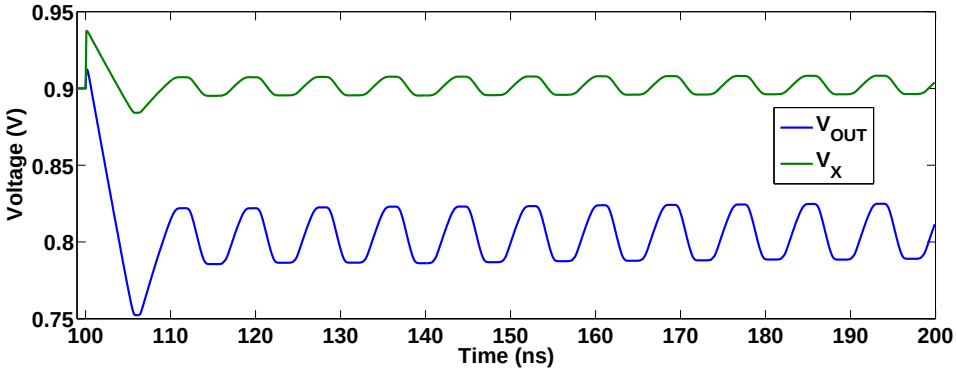


Figure 3.1: Plot of V_X and V_{OUT} vs time for Example 1

It is observed from figure (3.1) that the circuit doesn't settle.

3.4.2 Example 2

Now, the widths of transistors of stage 1 inverter are increased as mentioned in rule 3. The ratio of $\frac{W_p}{W_n}$ is same as before.

For inverter A_1

$$\frac{W}{L} = \frac{2000}{180} \text{ for PMOS}$$
$$\frac{W}{L} = \frac{500}{180} \text{ for NMOS}$$

For the 2 inverters A_2

$$\frac{W}{L} = \frac{1080}{180} \text{ for PMOS}$$
$$\frac{W}{L} = \frac{270}{180} \text{ for NMOS}$$

For final stage

$$\frac{W}{L} = \frac{270}{270} \text{ for PMOS}$$
$$\frac{W}{L} = \frac{270}{540} \text{ for NMOS}$$

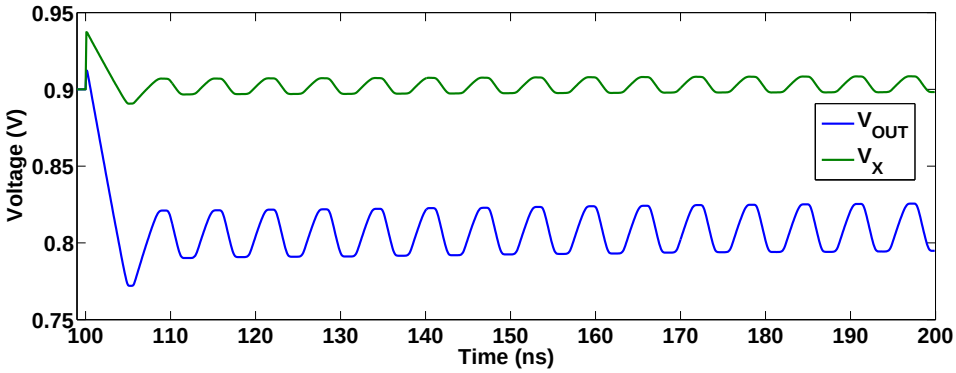


Figure 3.2: Plot of V_X and V_{OUT} vs time for Example 2

We observe from figure (3.2) that the circuit doesn't settle despite the V_X value reaching 898.5 mV. The offset voltage is 100 mV. The steady state gain $A_1 = 36$. So, the circuit must settle whenever $\frac{V_{DD}}{2} - \frac{V_{OS}}{A_1} < V_X < \frac{V_{DD}}{2} + \frac{V_{OS}}{A_1}$. In this case, circuit must settle whenever 897.23 mV < V_X < 902.77 mV. This doesn't happen, as the change in width of transistors in A_1 has made the trip point of A_1 (897.93 mV) different from that of A_2 (870.21 mV). This is why it was stated that **maintaining same trip point is a must**.

3.4.3 Example 3

Now, the width of the PMOS transistors of stage 2 inverters is increased to push the trip point of the stage 2 inverter towards the trip point of stage 1 inverter.

For inverter A_1

$$\frac{W}{L} = \frac{2000}{180} \text{ for PMOS}$$
$$\frac{W}{L} = \frac{500}{180} \text{ for NMOS}$$

For the 2 inverters A_2

$$\frac{W}{L} = \frac{1350}{180} \text{ for PMOS}$$
$$\frac{W}{L} = \frac{270}{180} \text{ for NMOS}$$

For final stage

$$\frac{W}{L} = \frac{270}{270} \text{ for PMOS}$$
$$\frac{W}{L} = \frac{270}{540} \text{ for NMOS}$$

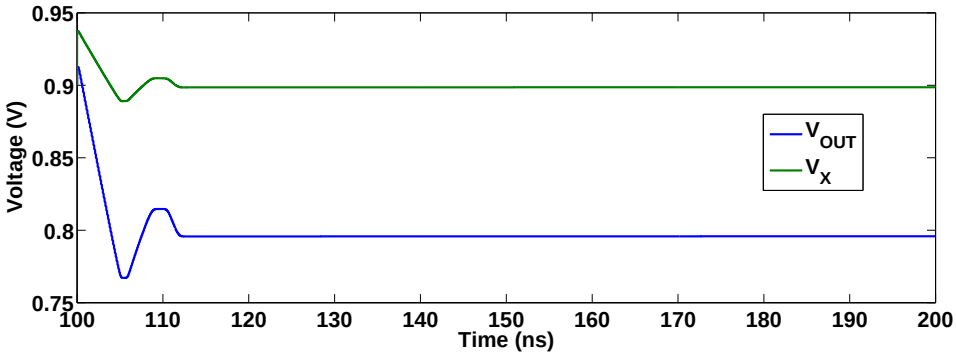


Figure 3.3: Plot of V_X and V_{OUT} vs time for Example 3

Now, it is observed that the circuit settles in 2 rings.

3.4.4 Example 4

Now, the length of the NMOS transistor (M_{CN}) is decreased. This increases the rate of drop of V_{OUT}, and causes asymmetry with respect to rate of voltage change.

For inverter A_1

$$\frac{W}{L} = \frac{2000}{180} \text{ for PMOS}$$
$$\frac{W}{L} = \frac{500}{180} \text{ for NMOS}$$

For the 2 inverters A_2

$$\frac{W}{L} = \frac{1350}{180} \text{ for PMOS}$$
$$\frac{W}{L} = \frac{270}{180} \text{ for NMOS}$$

For final stage

$$\frac{W}{L} = \frac{270}{270} \text{ for PMOS}$$
$$\frac{W}{L} = \frac{270}{270} \text{ for NMOS}$$

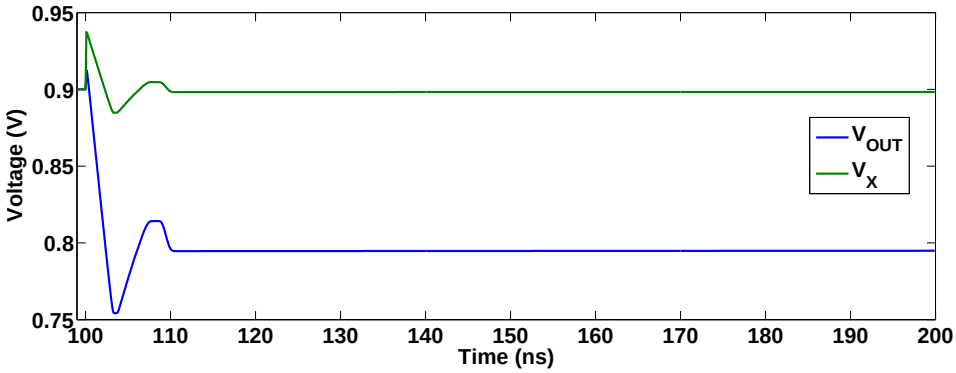


Figure 3.4: Plot of V_X and V_{OUT} vs time for Example 4

Again, the circuit settles. However, the 2 rising and falling rates of V_X and V_{OUT} change with respect to previous case, which is highlighted by the difference in dead-zone times.

3.4.5 Example 5

In example 3, it was noticed that circuit settled in just 2 rings. This means that further reduction in width may also lead to settling of output. Such a reduction is attempted and widths of PMOS transistors in second stage inverter are appropriately changed to maintain same trip point for all inverters.

For inverter A_1

$$\frac{W}{L} = \frac{1800}{180} \text{ for PMOS}$$
$$\frac{W}{L} = \frac{450}{180} \text{ for NMOS}$$

For the 2 inverters A_2

$$\frac{W}{L} = \frac{1300}{180} \text{ for PMOS}$$
$$\frac{W}{L} = \frac{270}{180} \text{ for NMOS}$$

For final stage

$$\frac{W}{L} = \frac{270}{270} \text{ for PMOS}$$
$$\frac{W}{L} = \frac{270}{540} \text{ for NMOS}$$

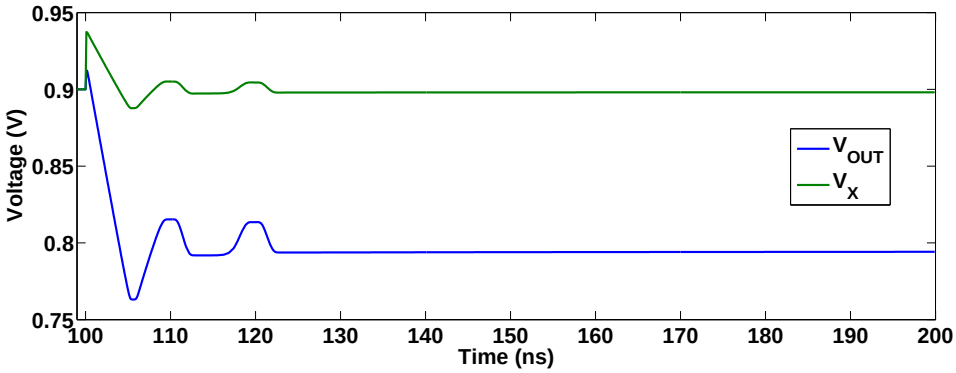


Figure 3.5: Plot of V_X and V_{OUT} vs time for Example 5

Now, the circuit settles in 4 rings. This increase in number of rings is as expected.

CHAPTER 4

Analysis of noise in ring amplifiers

4.1 Introduction

Looking at the "operating point" waveforms of different nodes in a ring amplifier based switched capacitor circuit in figures (2.8) and (2.4), it is obvious that the transconductance values and the output resistance values of different devices are not constant throughout the the clock-cycle like traditional OTA-based switched capacitor circuits. Due to the continuous changes in regions of operation of the circuit, all the g_m and g_{ds} (or r_O) values vary with time. This variation is periodic as the system is a LPTV system.

It is difficult to apply traditional frequency domain techniques for noise analysis of ring amplifier based switched capacitor circuits. Moreover, one is not interested in noise at all time instants in circuits which perform switched amplification. The only time point of interest is the time at which the output is sampled. In such a case, it is convenient to use the time-domain technique given by (Pavan and Rajan, 2014). For the specific case of ring-amplifiers, due to the complex nature of variation of the g_m and g_{ds} with time, a proper analysis would involve solving multiple differential equations and involved algebra. Approximating g_m and g_{ds} by suitable piece-wise constants simplifies the algebra to a large extent and provides some insights on dependence of the noise on different parameters of the ring amplifier circuit.

The concepts of inter-reciprocity and adjoint networks are extended to LPTV networks and used for the time-domain analysis. The fundamental reason why this is possible is the following.

For an LPTV network with an input $x(t)$, if the output of this network $y(t)$ is sampled at f_S, an equivalent LTI filter can be found. That is, if the LTI filter is excited by the same input $x(t)$ and the output is sampled at f_S, the output sequence is same as the the sequence of the LPTV network. The proof of this is provided in the appendix.

For constructing the adjoint network of an LPTV system,

- Linear elements (resistance R, capacitance C and inductance L) of the network $\mathcal{N}$ remain R, C and L in the adjoint network $\hat{\mathcal{N}}$.
- Periodic switches are time reversed. That is a switch which is one in a time interval T in $\mathcal{N}$ is on in the time interval $\overline{T}$ in $\hat{\mathcal{N}}$.
- All controlled sources transform in a similar way as the LTI networks but with an additional time reversal.

Now, to find the $h_{eq}(t)$, impulse response of an LTI filter equivalent to the LPTV network with sampled output, an impulse is applied at the output port of $\hat{\mathcal{N}}$ at the time instant $T_S - t_o$, where t_o is the time of observation of output. The output waveform is observed at the different input ports ($\hat{v_1}(t)$, $\hat{v_2}(t)$, ... $\hat{v_N}(t)$). Now, the equivalent LTI filter impulse responses from different input ports of $\mathcal{N}$ to the output port are given by

$$\begin{aligned} h_{1,eq}(t) &= \hat{v_1}(t + T_s - t_o) \\ &.... \\ h_{N,eq}(t) &= \hat{v_1}(t + T_s - t_o) \end{aligned} \tag{4.1}$$

If the autocorrelation function of the noise process at the l^{th} input is $R_{n,l}(\tau)$, the autocorrelation function of the output noise is given by

$$R_l(\tau) = R_{n,l}(\tau) * h_{l,eq}(\tau) * h_{l,eq}(-\tau) \tag{4.2}$$

where $*$ denotes the convolution operation. The output power spectral density is the Fourier transform of $R_l(mT_S)$, where T_S is the sampling period of the circuit.

If $h_{l,eq}(t)$ in the above equation (4.2) is time limited to $\frac{T_S}{2}$ (implying the convolution is time-limited to T_S), and $R_{n,l}(\tau)$ is delta-correlated, $R_l(mT_S)$ evaluates to

$$\begin{aligned} R_l[0] &= R_{s,n,l} \int_0^{T_S} h_{l,eq}^2(t)dt \\ R_l[mT_S] &= 0 \quad \forall m \neq 0 \end{aligned} \tag{4.3}$$

where $R_{s,n,l}$ is the strength of the correlation impulse.

Using Parseval's theorem, the integrated mean squared noise in such a case is given

by

$$\frac{1}{2\pi}\int_0^{\pi}\left(R_{s,n,l}\int_0^{T_S} h_{l,eq}^2(t)dt\right)d\omega \tag{4.4}$$

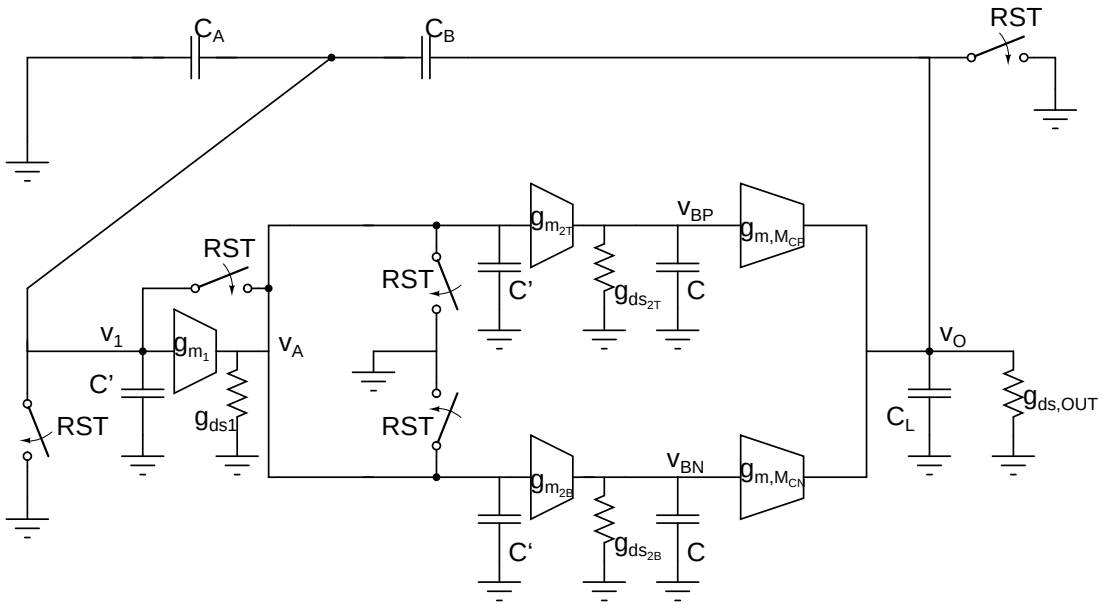


Figure 4.1: Incremental network

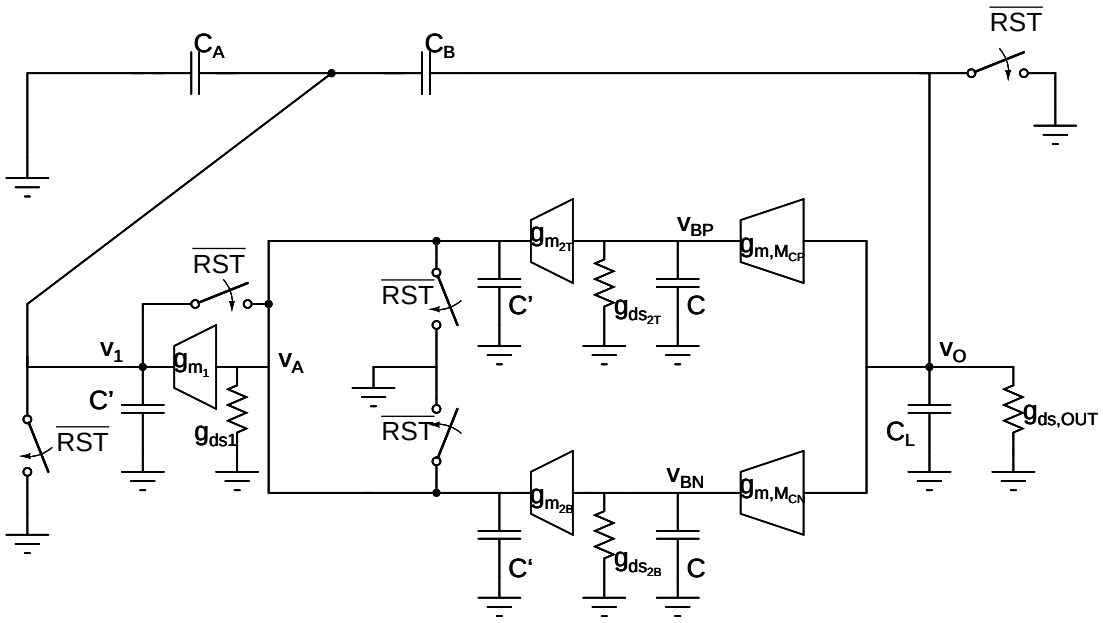


Figure 4.2: Adjoint incremental network

4.2 Estimation of $h(t)$ in the stabilization region of the circuit

The incremental equivalent of the circuit is shown in figure (4.1). Its adjoint is constructed and depicted in figure (4.2).

Before moving on to evaluate the impulse response $h(t)$, few approximations and consequent results are stated. These approximations are justified by simulation results.

- The first stage inverter A_1 is in the "high-gain region" (where both NMOS and PMOS are in saturation) throughout the sampling phase RST and for all of the amplification phase $\overline{RST}$ except the initial ramping phase, where it is in the "low-gain" region with only one of the two transistors in saturation. However, for convenience, the autocorrelation of the noise process at the drain of the inverter is assumed to be $\frac{8kTg_{m1}}{3}\delta(t)$, where g_{m1} is the transconductance in saturation region. That is, the noise is assumed to be white.

$$\begin{aligned} R_{n,A_1} &= \frac{8kTg_{m1}}{3}\delta(t) \\ g_{m1} &= \mu_n C_{OX}\frac{W}{L}\left(\frac{V_{DD}}{2} - V_{TN}\right) + \mu_p C_{OX}\frac{W}{L}\left(\frac{V_{DD}}{2} - V_{TP}\right) \end{aligned} \tag{4.5}$$

- The upper second stage inverter A_{2T} has an output voltage, V_{BP} close to 0 throughout the clock cycle except for small time intervals during amplification phase ($\overline{RST}$), as seen in figure (2.8). Similarly, the lower second stage inverter A_{2B} has an output voltage, V_{BN} close to V_{DD} throughout the clock cycle except for small time intervals during amplification phase ($\overline{RST}$), as seen in figure (2.8). For convenience, the autocorrelation of noise process at drains of A_2 inverters are assumed as 0 throughout. Thus, there is no contribution to noise from the transistors in second stage inverters.

- By similar argument, there is no contribution to noise from the transistors M_{CP} and M_{CN} as they remain in cut-off region for the entire clock cycle except time of ramping and crossing from one dead-zone to another, and hence have an autocorrelation of 0.

All that remains to be done is to find the $h(t)$ from the drain of inverter A_1 to the output.

In the adjoint network, an impulse current $\delta(t + T_s - t_o)$ is injected at the output node, and the corresponding response is computed. The v_A computed corresponds to the $v_o(t - T_S + t_o)$ observed when an impulsive current $\delta(t)$ is injected at the node V_A of the original incremental network. In this case, time of observation of output t_o is T_S, that is, the output is sampled at the end of the clock cycle.

An impulsive current is injected into the output node of the adjoint network at time 0, that is $\delta(t)$ current is injected. Now, the corresponding step increase in v_o is computed.

$$\begin{aligned}(C_L + C_B)\frac{dv_o}{dt} - C_B\frac{dv_1}{dt} &= \delta(t)\\ (C_A + C_B)\frac{dv_1}{dt} - C_B\frac{dv_o}{dt} &= 0\end{aligned} \tag{4.6}$$

Integrating both sides of the above equation from time $t = 0$ to an infinitesimal $t = \delta t$,

$$\begin{aligned}(C_L + C_B)\Delta v_o - C_B\Delta v_1 &= 1\\ (C_A + C_B)\Delta v_1 - C_B\Delta v_o &= 0\end{aligned} \tag{4.7}$$

Thus,

$$\Delta v_o = \frac{C_A + C_B}{C_AC_B + C_AC_L + C_BC_L} \tag{4.8}$$

Now, the calculation of $h(t)$ is done piecewise. The region of transition between two dead-zones and the region in the dead-zone are considered separately. From incremental analysis of the adjoint incremental circuit in figure (4.2), the following differential equations are obtained,

$$\begin{aligned}v_{BN}(t) &= \frac{-g_{m,M_{CN}}(T_s - t)v_o(t)}{g_{ds,2}(T_s - t)}\\ v_{BP}(t) &= \frac{-g_{m,M_{CP}}(T_s - t)v_o(t)}{g_{ds,2T}(T_s - t)}\\ -g_{m,2}(T_s - t)v_{BN}(t) - g_{m,2T}(T_s - t)v_{BP}(t) &= 2C'\frac{dv_A}{dt} + v_Ag_{ds,1}(T_s - t)\\ \left(\frac{C_L + C_B}{C_B} - \frac{C_B}{C_A + C_B}\right)\frac{dv_o(t)}{dt} &= -\frac{g_{m1}(T_s - t)v_A(t)}{C_A + C_B} - \frac{v_og_{ds,out}(T_s - t)}{C_B}\end{aligned} \tag{4.9}$$

It can be noted above that the parasitic capacitance C at the nodes v_{BP} and v_{BN} have not been considered. As stated in the previous chapter, the delay at this node is much less than the delay at node v_A. Thus, v_{BN} can be considered as $g_{m,M_{CN/CP}}$ times $r_{o,2} = \dfrac{1}{g_{ds,2}}$

times v_o. Also, the $g_{ds,out}$ term is neglected compared to other terms in the last line of equation (4.9)

The following notations are used in this chapter

- $t_{en,k}$ is the time at which the circuit enters the k^{th} dead-zone.
- $t_{ex,k}$ is the time at which the circuit exits the k^{th} dead-zone.
- $t_{cr,k}$ is the time taken in crossing from one dead-zone to another, that is, $t_{ex,k}$ to $t_{en,k+1}$. That is,

$$t_{cr,k} = t_{en,k+1} - t_{ex,k} \tag{4.10}$$

- $t_{dzo,k}$ is the time spent in the k^{th} dead-zone, i.e., the time taken between $t_{en,k}$ to $t_{ex,k}$. That is,

$$t_{dzo,k} = t_{ex,k} - t_{en,k} \tag{4.11}$$

It may be noted that the notation for time spent in dead-zone is a bit different from the notation used in the previous two chapters.

After injecting an impulsive current at $t = 0$, the time-reversed g_m, g_{ds} values are used in the adjoint network. In the "operating point" of the circuit which settles after N rings, the circuit enters its final dead-zone at $t = t_{en,N+1}$. That is, the circuit is settled after $t = t_{en,N+1}$. So, from $t = t_{en,N+1}$ to $t = T_S$, $g_{m,M_{CN}} = 0$, $g_{m,M_{CP}} = 0$ as the final stage transistors are cut-off. This means, in the adjoint network from $g_{m,M_{CN}} = 0$, $g_{m,M_{CP}} = 0$ from $t = 0$ to $t = T_S - t_{en,N+1}$. From the differential equation (4.9), it can be inferred that the node voltages do not change after $t = 0^+$ to $t = T_S - t_{en,N+1}$.

4.2.1 Calculation of $h(t)$ in the time-reversed transition regions

Now, $h(t)$ (or $v_A(t)$) is calculated in the time-reversed k^{th} crossing/transition region, that is, the time between $T_S - t_{en,k+1}$ to $T_S - t_{ex,k}$ using the differential equations set-up above. The solution will involve decoupling of the 2 differential equations in v_A and v_o and result in a second order differential equation. Here, a transition region where NMOS is active, is assumed. The other transition region where PMOS is active also has a similar formulation (with only $g_{m,M_{CN}}$ being replaced by $g_{m,M_{CP}}$).

When either M_{CN} or M_{CP} is active, its overdrive voltage increases from 0 to a maximum. This is not a step increase, and a small time interval elapses during this increase. Accounting for this change in calculations makes the algebra very involved. Thus, a constant maximum overdrive is assumed for a simple approximation. Assuming a constant maximum overdrive for the entire duration of $t_{cr,k}$ will obviously lead to errors. Thus, this constant overdrive approximation is done only for a fraction of $t_{cr,k}$, the time taken to cross from one dead-zone to another. This fraction is chosen empirically and hence is a source of error. This approximation works to reasonable accuracy as the rate of change of V_{BN} or V_{BP} is much lower at voltages close to maximum overdrive and much faster at lower overdrives. One approximate way to do the constant estimation is to assume maximum overdrive for the time taken to go from κ times the maximum overdrive to the maximum overdrive and then again come down to κ times the maximum overdrive. Choosing the value of κ is again empirical and may lead to errors. This constant approximation is a must for simple expressions, as will be seen from the following differential equations.

The resulting second order differential equation in v_A and v_o both take the same form

$$\begin{aligned}\delta\frac{d^2v_A}{dt^2}+\frac{\delta g_{ds1}}{2C'}\frac{dv_A}{dt}+\frac{A_2g_{m1}g_{m,M_{CN}}}{2C'(C_A+C_B)}v_A=0\\ \delta\frac{d^2v_o}{dt^2}+\frac{\delta g_{ds1}}{2C'}\frac{dv_o}{dt}+\frac{A_2g_{m1}g_{m,M_{CN}}}{2C'(C_A+C_B)}v_o=0\end{aligned} \tag{4.12}$$

where $\delta=\dfrac{C_L+C_B}{C_B}-\dfrac{C_B}{C_A+C_B}$.

Solving the above differential equation using initial conditions derived from (4.8),

$$\begin{aligned}&v_A(t)=e^{-\alpha(t-(T_s-t_{en,k+1}))}\left(k_1\sin(\beta(t-(T_s-t_{en,k+1}))+k_2\cos(\beta(t-(T_s-t_{en,k+1}))\right)\\ &\alpha=\frac{g_{ds1}}{4C'}\\ &\beta=\sqrt{\frac{g_{m1}g_{m,M_{CN}}A_2}{2\delta(C_A+C_B)C'}}\\ &k_1=\frac{v_A'(T_s-t_{en,k+1})+\alpha v_A(T_s-t_{en,k+1})}{\beta}\\ &k_2=v_A(T_s-t_{en,k+1})\end{aligned} \tag{4.13}$$

$$
\begin{aligned}
v_o(t) &= e^{-\alpha(t-(T_s-t_{en,k+1}))}\left(l_1\sin(\beta(t-(T_s-t_{en,k+1}))+l_2\cos(\beta(t-(T_s-t_{en,k+1}))\right)\\
\alpha &= \frac{g_{ds1}}{4C'}\\
\beta &= \sqrt{\frac{g_{m1}g_{m,M_{CN}}A_2}{2\delta(C_A+C_B)C'}}\\
l_1 &= \frac{v_o'(T_s-t_{en,k+1})+\alpha v_o(T_s-t_{en,k+1})}{\beta}\\
l_2 &= v_o(T_s-t_{en,k+1})
\end{aligned}
\tag{4.14}
$$

where $\delta = \dfrac{C_L+C_B}{C_B} - \dfrac{C_B}{C_A+C_B}$.

As will be seen sometime later in equation (4.17), at the beginning of every dead-zone (time reversed), v_A decays considerably towards 0. Thus, at the beginning of every dead-zone (time-reversed), $v_A \approx 0$. That is $v_A(T_S - t_{en,k}) \approx 0$. Using this approximation,

$$
\begin{aligned}
v_A(t) &= e^{-\alpha(t-(T_s-t_{en,k+1}))}\left(k_1\sin(\beta(t-(T_s-t_{en,k+1}))\right)\\
v_o(t) &= e^{-\alpha(t-(T_s-t_{en,k+1}))}\left(l_2\cos(\beta(t-(T_s-t_{en,k+1}))\right)\\
\alpha &= \frac{g_{ds1}}{4C'}\\
\beta &= \sqrt{\frac{g_{m1}g_{m,M_{CN}}A_2}{2\delta(C_A+C_B)C'}}\\
k_1 &= \frac{v_A'(T_s-t_{en,k+1})+\alpha v_A(T_s-t_{en,k+1})}{\beta}\\
&= \frac{\dfrac{A_2 g_{m,M_{CN}} v_o(T_s-t_{en,k+1})}{2C'} - \alpha v_A(T_s-t_{en,k+1}) + \alpha v_A(T_s-t_{en,k+1})}{\beta}\\
&= \frac{A_2 g_{m,M_{CN}} v_o(T_S-t_{en,k+1})}{2\beta C'}\\
l_2 &= v_o(T_s-t_{en,k+1})
\end{aligned}
\tag{4.15}
$$

Now, the integral of v_A^2 (in the k^{th} crossing region), which is a contributor to the output

noise PSD, as proved in equation (4.3), is given by

$$\int_{T_S-t_{en,k+1}}^{T_S-t_{ex,k}} v_A^2(t) = \frac{k_1^2}{2}\Bigg(\frac{1-e^{-2\alpha(t_{cr,k})}}{2\alpha} - \frac{e^{-2\alpha t_{cr,k}}}{2(\alpha^2+\beta^2)}(\beta\sin(2\beta t_{cr,k}) - \alpha\cos(2\beta t_{cr,k}) + \alpha)\Bigg) \tag{4.16}$$

4.2.2 Calculation of $h(t)$ in the time-reversed dead-zones

Now, $h(t)$ (or $v_A(t)$) is calculated in the k^{th} dead-zone region, i.e., the time between $T_S - t_{ex,k}$ to $T_S - t_{en,k}$ using the differential equations set-up above in (4.9). Here, both NMOS(M_{CN}) and PMOS(M_{CP}) are cut-off.

$$\begin{aligned} v_A(t) &= v_A(T_s - t_{ex,k})e^{\frac{-g_{ds}(t-(T_s-t_{ex,k}))}{2C'}} \\ v_o(t) &= v_o(T_s - t_{ex,k}) - \frac{A_1C'v_A(T_s-t_{ex,k})}{\delta(C_A+C_B)} + \frac{A_1C'v_A(T_s-t_{ex,k})e^{-\frac{g_{ds,1}(t-(T_S-t_{ex,k}))}{2C'}}}{\delta(C_A+C_B)} \\ v_o(t) &\approx -\frac{A_1C'v_A(T_s-t_{ex,k})}{\delta(C_A+C_B)}\left(1-e^{-\frac{g_{ds,1}(t-(T_S-t_{ex,k}))}{2C'}}\right) \end{aligned} \tag{4.17}$$

where $\delta = \dfrac{C_L+C_B}{C_B} - \dfrac{C_B}{C_A+C_B}$.

The approximation made in the above equation is justified as follows

$$\begin{aligned} &\frac{A_1C'v_A(T_s-t_{ex,k})}{\delta(C_A+C_B)} \\ &= \frac{A_1A_2g_{m,M_{CN/CP}}v_o(T_s-t_{ex,k+1})}{2\beta\delta(C_A+C_B)} \end{aligned} \tag{4.18}$$

For typical g_m and capacitance values,

$$\frac{A_1A_2g_{m,M_{CN/CP}}v_o(T_s-t_{ex,k+1})}{2\beta\delta(C_A+C_B)} >> e^{-\alpha(t_{cr,k})}v_o(T_s-t_{ex,k+1})\cos(\beta(t_{cr,k}) \tag{4.19}$$

Now, the integral of v_A^2 (in the k^{th} dead-zone region), which is a contributor to the output noise PSD, as proved in equation (4.3)

$$\begin{aligned} &\int_{T_S-t_{en,k}}^{T_S-t_{ex,k}} v_A^2(t) \\ &= \frac{v_A^2(T_s-t_{ex,k})(C')}{g_{ds,1}}\left(1-e^{-\frac{g_{ds,1}t_{dzo,k}}{C'}}\right) \end{aligned} \tag{4.20}$$

Now, integrals over all the dead-zone regions are summed to find the integral of $v_A^2(t)$ in the dead-zone region.

As there are N rings, the last entry to the time-reversed dead-zone is at $T_S - t_{en,N+1}$. Thus,

$$\begin{aligned} v_A(T_S - t_{en,N+1}) &= 0 \\ v_{00} = v_o(T_S - t_{en,N+1}) &= \frac{C_A + C_B}{C_A C_B + C_A C_L + C_B C_L} \end{aligned} \tag{4.21}$$

From equation (4.15),

$$\begin{aligned} v_A(T_S - t_{ex,N}) &= k_1 e^{-\alpha t_{cr,N}} \sin(\beta t_{cr,k}) \\ &= \sqrt{\frac{A_2 g_{m,M_{CN/CP}} \delta(C_A + C_B)}{2C' g_{m1}}} v_{00} e^{-\alpha t_{cr,N}} \sin(\beta t_{cr,k}) \end{aligned} \tag{4.22}$$

Substituting equation (4.22) in (4.17),

$$v_o(T_S - t_{en,N}) = \frac{-2A_1 C' \gamma_N v_A(T_S - t_{ex,N})}{\delta(C_A + C_B)} \tag{4.23}$$

where,

$$\gamma_N = 1 - e^{\frac{-g_{ds,1} t_{dzo,N}}{2C'}} \tag{4.24}$$

Now, the expression for $v_A(T_s - t_{ex,k})$ is evaluated using the equations (4.17) and (4.15),

$$v_A(T_s - t_{ex,k}) = -A_1 \gamma_{k+1} e^{-\alpha t_{cr,k}} \sin(\beta t_{cr,k}) \sqrt{\frac{2A_2 g_{m,M_{CN/CP}} C'}{g_{m1} \delta(C_A + C_B)}} v_A(T_s - t_{ex,k+1}) \tag{4.25}$$

$$\gamma_k = 1 - e^{\frac{-g_{ds,1} t_{dzo,k}}{2C'}} \tag{4.26}$$

The $g_{m,M_{CN/CP}}$ in the above formula denotes g_m of either NMOS M_{CN} or PMOS M_{CP} depending on which is active.

Now, the integral v_A^2 in the dead-zone is given by,

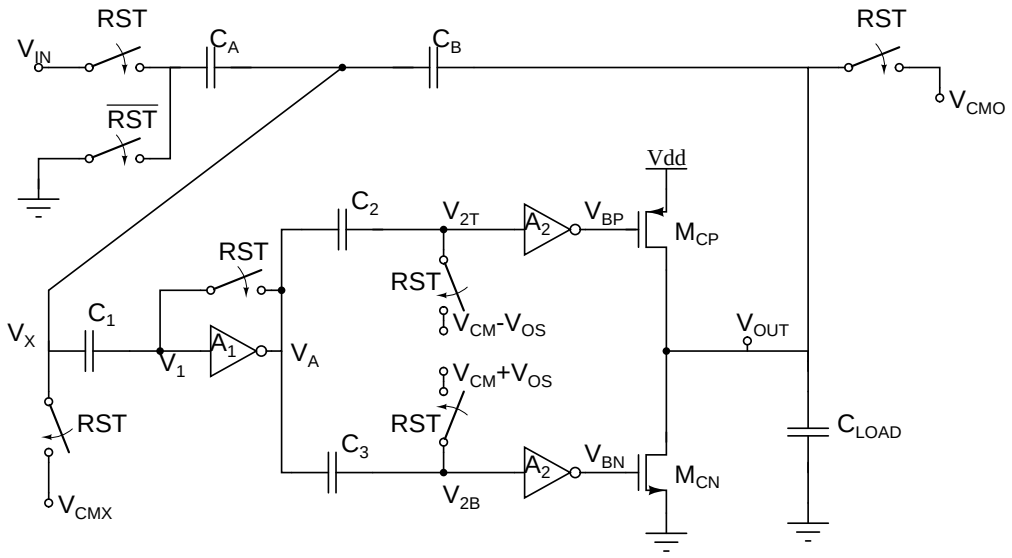
$$\int_{t_{dz}} v_A^2 = \sum_{k=1}^{N} v_A^2(T_s - t_{ex,k}) \frac{C'}{g_{ds,1}} (1 - e^{\frac{-g_{ds,1} t_{dzo,k}}{C'}}) \tag{4.27}$$

From equations (4.3), (4.4) and (4.5), the integrated mean squared noise is given by

$$\frac{4kT}{3g_{m1}}\left(\int_{t_{dz}} v_A^2(t)dt + \int_{t_{cr}} v_A^2(t)dt\right) \tag{4.28}$$

It is to be noted that the contribution from v_A in the initial ramping phase has been neglected. This is very tedious to calculate as making constant g_m approximations in this region are not feasible. However, this contribution to $\int v_A^2(t)dt$ is negligible compared to other contributions.

4.3 Simulation and analytic for variation of integrated mean squared noise with V_{OS}



From the equations derived in the previous section, it is observed that the mean squared output noise mainly depends on the following factors

- As the number of times the circuit rings increases, the integrated mean squared noise increases.
- For a particular number of rings, as the time taken for each ring of the circuit increases, the integrated mean squared noise also increases.
- Also, it is known that as V_{OS} increases for a given number of rings, the over-shoot with respect to mid-rail voltage also decreases. The equation for rate when

NMOS is active (derived in (2.11)) is given by,

$$r_i = ((A_1A_2t_d)^2k_pk_n\psi^2)^i\left(r_0 + \frac{V_{OS}A_2k_n(1+k_pt_dA_1A_2\psi)}{1-(A_1A_2t_d)^2k_pk_n\psi^2}\right) - \frac{V_{OS}A_2k_n(1+k_pt_dA_1A_2\psi)}{1-(A_1A_2t_d)^2k_pk_n\psi^2} \tag{4.29}$$

The overshoot v_i, on the negative side, with respect to mid-rail, is given by

$$v_{overshoot,i} = r_it_d\frac{C_B}{C_A+C_B} - \frac{V_{OS}}{A_1} \tag{4.30}$$

As V_{OS} increases, r_i decreases, since the coefficient of V_{OS} in the above equation (4.29) for rate is $((A_1A_2t_d)^2k_pk_n)^i - 1$ and for stable circuits which settle, $((A_1A_2t_d)^2k_pk_n)^i < 1$. Also, it is noticed from (4.30) that as V_{OS} increases, overshoot with respect to mid-rail decreases.

Now,

$$\begin{aligned} V_A &= \frac{V_{DD}}{2} + A_1v_{overshoot,i} \\ V_{2T} &= V_A - V_{OS} \\ V_{CP} &= f(V_{2T}) \end{aligned} \tag{4.31}$$

where f is the inverter characteristic transfer function. In the inverter characteristic transfer function (of figure 4.3), gain $\left(\frac{dv_o}{dv_i}\right)$ of an output voltage close to rails is much lower than that of output voltage close to mid-rail, where gain is maximum. As $v_{overshoot,i}$ decreases, V_A and hence V_{2T} decrease. This brings V_{2T} closer to mid-rail, and hence V_{CP} also closer to mid-rail. Thus, for lower overshoot values, V_{CP} is closer to mid-rail and hence A_2 is much higher for smaller $v_{overshoot,i}$. Thus, as V_{OS} increases, $v_{overshoot,i}$ decreases, hence increasing A_2. Higher A_2 from equations (4.22) and (4.25) implies higher noise. However, from equation (4.13), β also becomes higher with increase in A_2. As there is a sinusoidal dependence on β, as seen from equation (4.22) and (4.25), there may be some irregularities with higher β.

In the ring amplifier circuit, a constant load capacitance C_L, a constant C_A, C_B (hence, a constant gain) and a constant input voltage (V_{IN}) are maintained. Only the offset voltage V_{OS} embedded at the output of the first stage inverter is varied.

The following are the plots of integrated mean squared noise versus V_{OS} and number

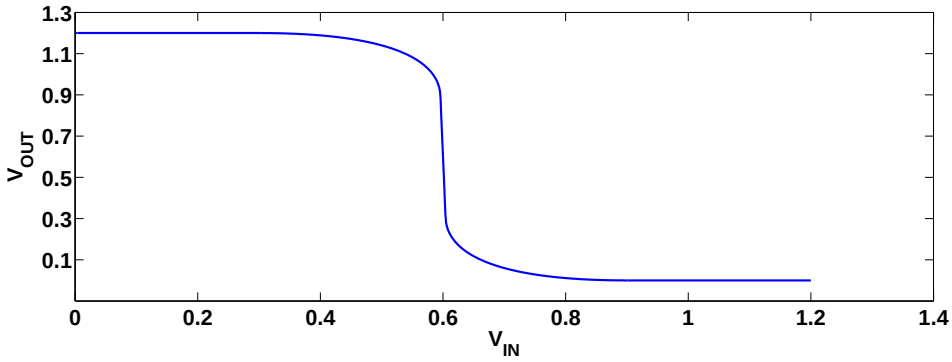


Figure 4.3: Inverter characteristics

of rings (N) versus V_{OS}. In this case, For all inverters,

$$\frac{W}{L} \text{ of NMOS} = \frac{7.2}{2.4}$$
$$\frac{W}{L} \text{ of PMOS} = \frac{21.6}{2.4}$$

For M_{CN},

$$\frac{W}{L} = \frac{3.2}{3.2}$$

For M_{CP}

$$\frac{W}{L} = \frac{9.6}{3.2}$$

All dimensions are in μm.

$$C_A = 1.5\text{pF}$$
$$C_B = 1\text{pF}$$
$$C_L = 0.2\text{pF}$$
$$V_{IN} = -0.1\text{V}$$

V_{OS} was varied from 180 mV to 310 mV, in steps of 5 mV. A pss and pnoise analysis was run for each of these cases using the guidelines in (Murmann, 2012). The resulting output noise and the number of rings are plotted against the offset voltage. The general trend from this plot looks like the mean squared noise decreases with increase in V_{OS} and hence the decrease in number of rings. However, on zooming in on the region with smaller number of rings, it is noticed that there is not a uniform decrease. For some k

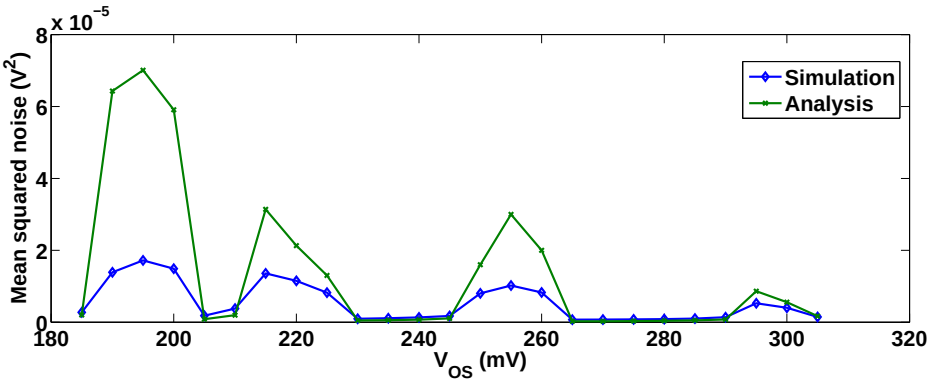


Figure 4.4: Integrated mean squared noise v/s V_{OS}

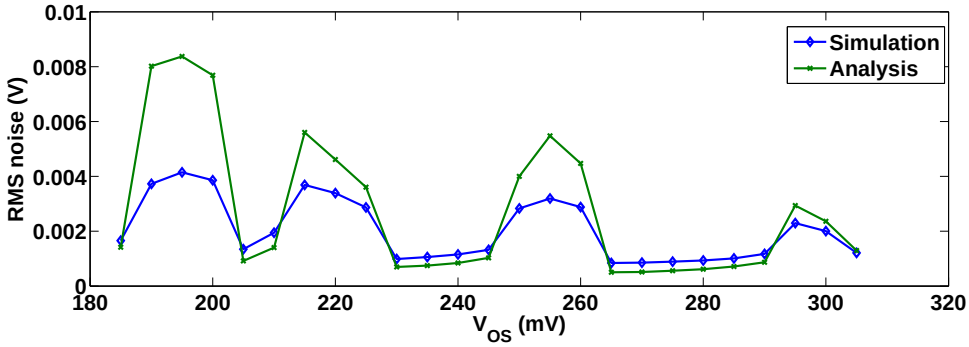


Figure 4.5: Root mean squared noise v/s V_{OS}

number of rings in the output, the noise increases with an increase in V_{OS}. This shows the dependence on the time taken for each ring and on the increase in A_2 with V_{OS}. For the same number of rings, the time taken for each ring increases with an increase in V_{OS}. Also, A_2 increases with increase in V_{OS}. Therefore, the integrated mean squared noise for a given number of rings is higher when the offset voltage V_{OS} is higher. However, as there is a sinusoidal dependence on β, as seen from equations (4.22) and (4.25), there may be some irregularities in trends with higher β.

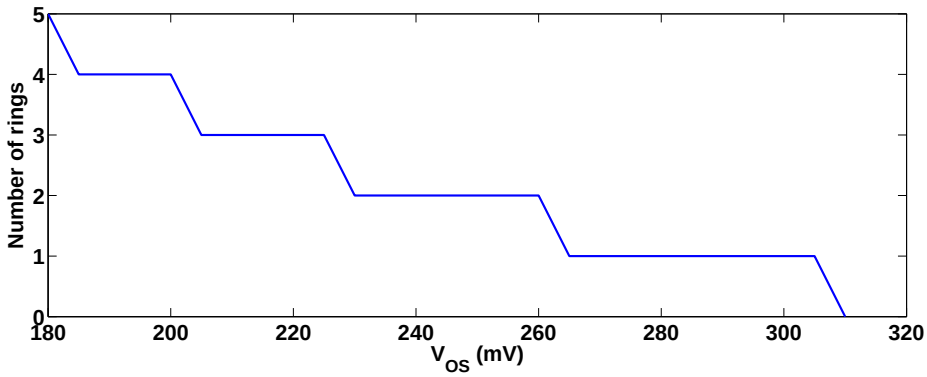
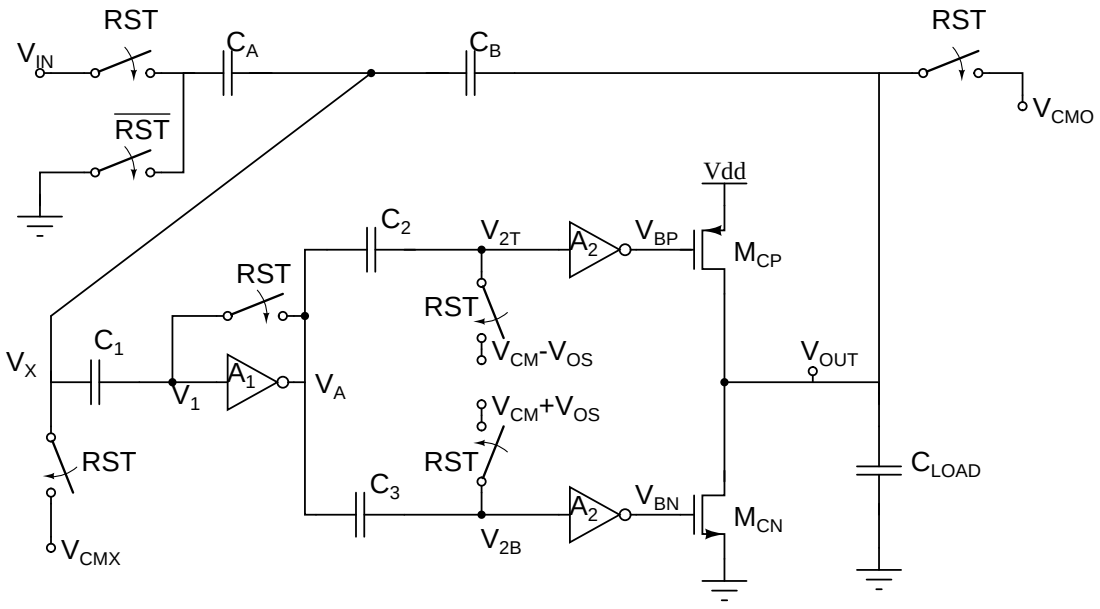


Figure 4.6: Number of rings v/s V_{OS}

4.4 Simulation and analytic for variation of integrated mean squared noise with C_{LOAD}



As in the previous section, it is observed that the mean squared noise mainly depends on the following factors

- As the number of times the circuit rings increases, the integrated mean squared noise increases.
- For a particular number of rings, as the time taken for each ring of the circuit increases, the integrated mean squared noise also increases.
- Also, it is seen that as C_{LOAD} increases for a given number of rings, the overshoot with respect to mid-rail voltage also decreases. The differential equations

(derived in (2.10)) governing the rate are given by,

$$\begin{aligned} r_i &= \left(r'_{i-1} t_d \frac{C_B}{C_A + C_B} - \frac{V_{OS}}{A_1} \right) A_1 A_2 k_n \\ k_n &= \frac{g_{m,M_{CN}}}{C_L + \dfrac{C_A C_B}{C_A + C_B}} \\ r'_i &= \left(r_i t_d \frac{C_B}{C_A + C_B} - \frac{V_{OS}}{A_1} \right) A_1 A_2 k_p \\ k_p &= \frac{g_{m,M_{CP}}}{C_L + \dfrac{C_A C_B}{C_A + C_B}} \end{aligned} \tag{4.32}$$

The overshoot, on the negative side, with respect to mid-rail v_i is given by

$$v_{overshoot,i} = r_i t_d \frac{C_B}{C_A + C_B} - \frac{V_{OS}}{A_1} \tag{4.33}$$

As C_{LOAD} increases, it is seen from the above set of equations that, k_n, k_p also decrease, therefore, r_i decreases. Now, as r_i decreases, from equation (4.33), it is noticed that $v_{overshoot,i}$ also decreases.

Now,

$$\begin{aligned} V_A &= \frac{V_{DD}}{2} + A_1 v_i \\ V_{2T} &= V_A - V_{OS} \\ V_{CP} &= f(V_{2T}) \end{aligned}$$

where f is the inverter characteristic transfer function. Now, in the inverter characteristic transfer function, gain $\left(\frac{dv_o}{dv_i}\right)$ of an output voltage close to rails is much lower than that of output voltage close to mid-rail, where gain is maximum. As $v_{overshoot,i}$ decreases, V_A and hence V_{2T} decreases. This brings V_{2T} closer to mid-rail, and hence V_{CP} also closer to mid-rail. Thus, for lower overshoot values, V_{CP} is closer to mid-rail and hence A_2 is much higher for smaller $v_{overshoot,i}$. Thus, as C_{LOAD} increases, $v_{overshoot,i}$ decreases, hence increasing A_2. Higher A_2 from equations (4.22) and (4.25) implies higher noise. The variation of inverter gain is illustrated by the inverter characteristics plotted in the figure (4.3).

However, from equation (4.13), β_i also becomes higher with increase in A_2. As there is a sinusoidal dependence on β_i, as seen from equation (4.22) and (4.25), there

may be some irregularities with higher β_i.

In the ring amplifier circuit, a constant offset voltage V_{OS}, a constant C_A, C_B (hence, a constant gain) and a constant input voltage (V_{IN}) are maintained. Only the load capacitance C_{LOAD} is varied.

The following are the plots of integrated mean squared noise versus C_{LOAD} and number of rings (N) versus C_{LOAD}. In this case, For all inverters,

$$\frac{W}{L} \text{ of NMOS} = \frac{7.2}{2.4}$$
$$\frac{W}{L} \text{ of PMOS} = \frac{21.6}{2.4}$$

For M_{CN},

$$\frac{W}{L} = \frac{3.2}{3.2}$$

For M_{CP}

$$\frac{W}{L} = \frac{9.6}{3.2}$$

All dimensions are in μm.

$$C_A = 1.5\text{pF}$$
$$C_B = 1\text{pF}$$
$$V_{OS} = 0.15\text{V}$$
$$V_{IN} = -0.1\text{V}$$

Also, C_{LOAD} was varied from 300 fF to 3 pF, in appropriate steps. A pss and pnoise analysis was run for each of these cases using the guidelines in (Murmann, 2012). The resulting output noise and the number of rings are plotted against the load capacitance.

The general trend from this plot looks like the mean squared noise decreases with increase in C_{LOAD} and the consequent decrease in number of rings. However, on zooming in on the region with smaller number of rings, it is noticed that there is not a uniform decrease. This shows the dependence on the following factors:

- The time taken for each ring. For a given number of rings, this time increases with increase in C_{LOAD}. Increased ringing time leads to increase in noise. However,

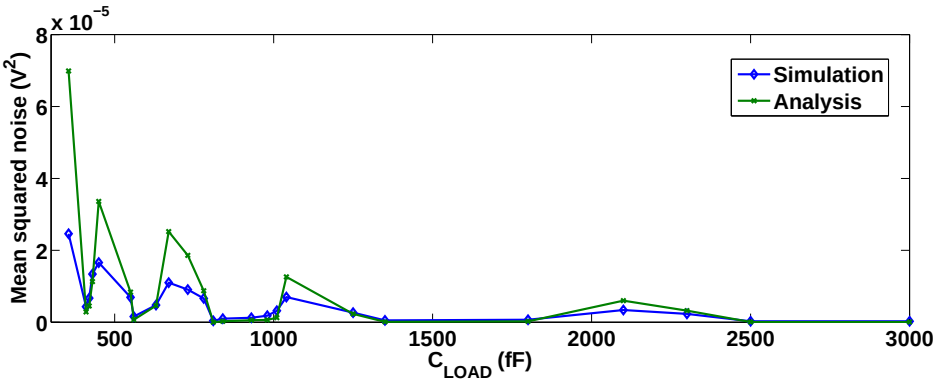


Figure 4.7: Integrated mean squared noise v/s C_{LOAD}

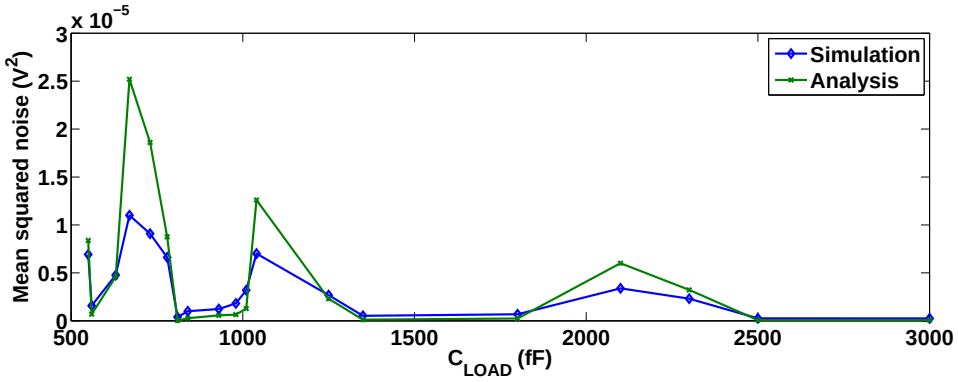


Figure 4.8: Integrated mean squared noise v/s C_{LOAD}, zoomed in

this is offset by a decrease in noise due to increase in C_{LOAD} itself. Increased C_{LOAD} means decreased initial rise in voltage v_{00} as given by equation (4.21). Decreased v_{00} leads to decreased noise as given by (4.22).

- Also, the increase in A_2 as explained at the start of the section.

- Similarly, as the overshoot $v_{overshoot,i}$ or $v'_{overshoot,i}$ decreases with increase in C_{LOAD}, there is a consequent decrease in the maximum gate overdrive voltage at the final stage. The incremental change in overdrive voltage is given by

$$\begin{aligned} v_{BN} &= A_1 A_2 v_i \\ v_{BP} &= A_1 A_2 v'_i \end{aligned} \tag{4.34}$$

  Decrease in overdrive voltage leads to decrease in $g_{m,M_{CN/CP}}$ if the final stage transistors are in saturation.

These are the reasons an increase followed by a decrease in noise for a given number of rings N, is observed.

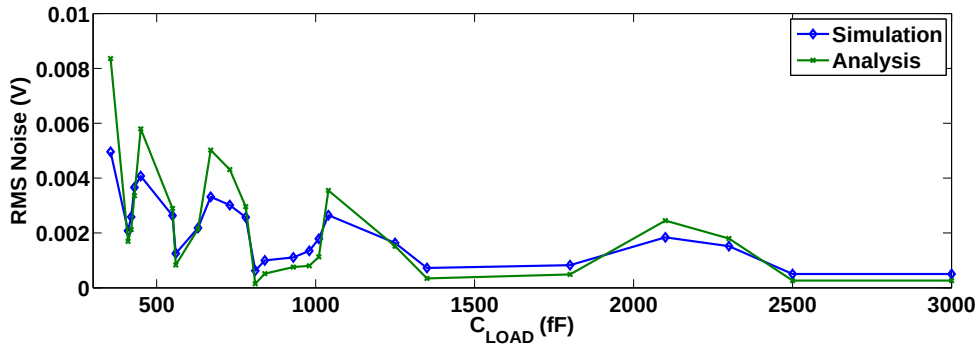


Figure 4.9: Root mean squared noise v/s C_{LOAD}

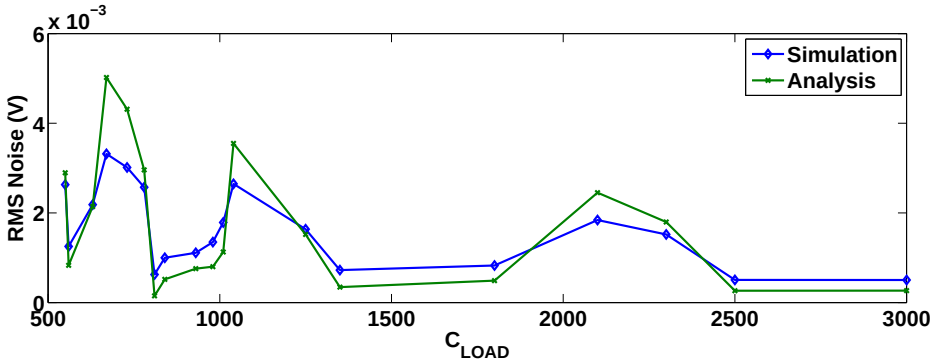


Figure 4.10: Root mean squared noise v/s C_{LOAD}, zoomed in

However, as there is a sinusoidal dependence on β_i, as seen from equations (4.22) and (4.25), there may be some irregularities in trends with higher β_i.

4.5 Possible sources of deviation

- As there is a sinusoidal dependence on β_i, as seen from equation (4.22) and (4.25), any small error in the estimation of β_i may lead to more significant errors in the estimation of $h(t)$. Also, if this error comes up in the estimation of the last (N^{th}) time-reversed ring, there will be an accumulation of error as we estimate the time-reversed rings $N-1$, ..., 1.

- Assuming constant (maximum) gate overdrive for the last stage NMOS/PMOS means estimated noise is higher than actual noise.

- Also, the approximation that $v_A(T_S - t_{en,k}) \approx 0$ while simplifying the expressions to a certain extent, may lead to deviation from simulation.

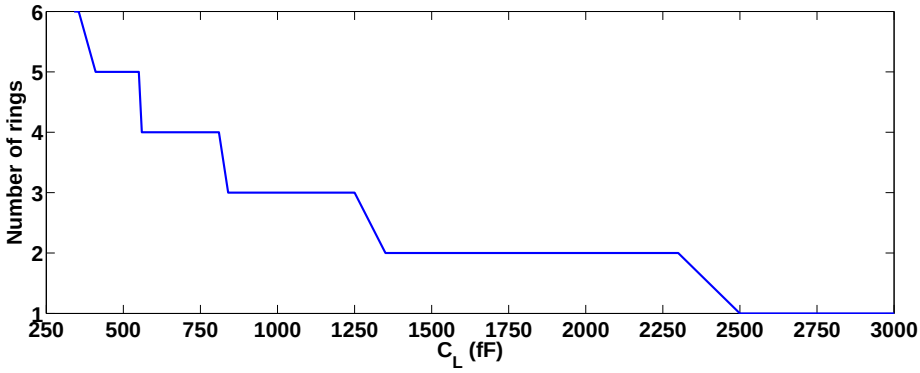


Figure 4.11: Number of rings v/s C_{LOAD}

CHAPTER 5

Analysis of noise in traditional OTA based switched capacitor circuits

In this chapter, the noise in traditional OTA based switched capacitor circuits is analysed. The g_m g_{ds} values are constant in this circuit, as opposed to the ring amplifier circuit. Thus, noise analysis by traditional frequency method is much simpler in this case. This point is illustrated in this chapter and some similarities and differences between the noise in 2 circuits are noted. The traditional OTA-based switched capacitor amplifier is shown in figure (5.1)

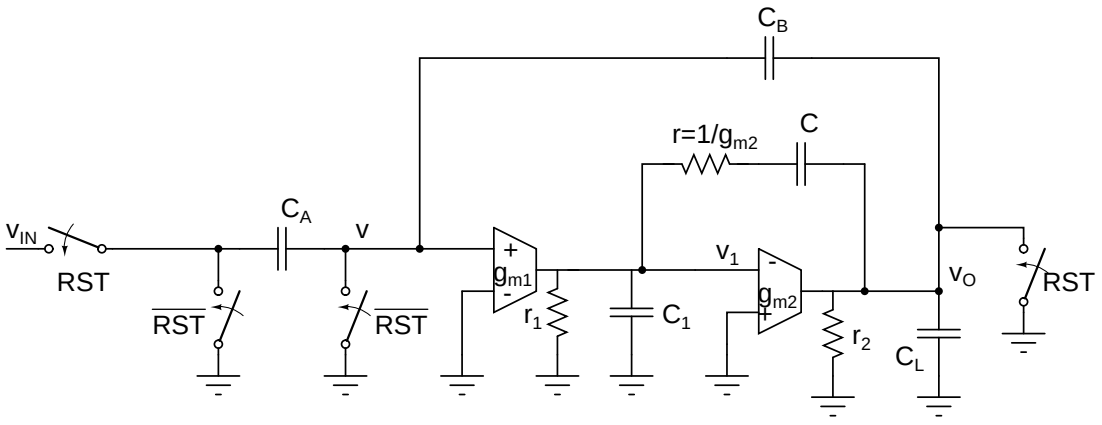


Figure 5.1: OTA based switched capacitor circuit

5.1 Noise calculation in OTA based switched capacitor circuits

The values used for simulation in this circuit are:

$$\begin{aligned} C_A &= 3\text{pF} \\ C_B &= 1\text{pF} \\ C_L &= 0.2\text{pF} \\ C_1 &= 10\text{fF} \\ r_1 &= r_2 = \infty \\ g_{m1} &= g_{m2} = 100\mu\text{S} \end{aligned} \tag{5.1}$$

The noise transfer functions from the 2 transconductance and from the zero-cancelling resistor to the output node are computed. The two output resistance values are assumed to be ∞ during our calculations. The transfer function from g_{m1} is $H_1(s)$, from g_{m2} is $H_2(s)$ and from the zero-cancelling resistor is $H_3(s)$.

5.1.1 Simulation and analytic noise due to g_{m1} for variation of integrated mean squared noise with C

$$\begin{aligned} v_1\left(sC_1 + \frac{g_{m2}sC}{g_{m2}+sC}\right) - v_o\left(\frac{g_{m2}sC}{g_{m2}+sC} + \frac{g_{m1}C_B}{C_A+C_B}\right) &= I(s) \\ v_o\left(s(C_A||C_B + C_L) + \frac{sCg_{m2}}{sC+g_{m2}}\right) - v_1\left(\frac{sCg_{m2}}{sC+g_{m2}} - g_{m2}\right) &= 0 \end{aligned}$$

Solving the above equations,

$$H_1(s) = \frac{g_{m2}^2}{s^3CC_1(C_L + C_A||C_B) + s^2(g_{m2}C_1(C_L + C_A||C_B + C) + g_{m2}C(C_L + C_A||C_B)) + sg_{m2}^2C + \frac{g_{m2}^2g_{m1}C_B}{C_A+C_B}} \tag{5.2}$$

The output noise spectral density is given by

$$S_{vO}(f) = |H(f)|^2 \times \frac{8kTg_{m1}}{3} \tag{5.3}$$

Capacitance C (pF)	Simulated mean squared noise (V^2)	Analytic mean squared noise (V^2)
0.01	1.23×10^{-6}	1.26×10^{-6}
0.02	5.95×10^{-7}	6.02×10^{-7}
0.05	2.29×10^{-7}	2.31×10^{-7}
0.1	1.13×10^{-7}	1.13×10^{-7}
0.25	4.45×10^{-8}	4.45×10^{-8}
0.5	2.22×10^{-8}	2.22×10^{-8}
0.75	1.48×10^{-8}	1.48×10^{-8}
1	1.11×10^{-8}	1.11×10^{-8}
5	2.23×10^{-9}	2.21×10^{-9}
10	1.36×10^{-9}	1.11×10^{-9}

Table 5.1: Noise due to first stage transconductance

Using appropriate contour integration and evaluating mean squared noise using the above transfer function, the output noise comes to be

$$\frac{\frac{2kTg_{m2}}{3}\left(\frac{CC_1+(C_L+C_A||C_B)(C+C_1)}{C}\right)}{\frac{C_B}{C_A+C_B}\left(g_{m2}(CC_1+(C_L+C_A||C_B)(C+C_1))-g_{m1}\frac{C_B}{C_A+C_B}C_1(C_L+C_A||C_B)\right)} \tag{5.4}$$

Table (5.1) shows analytic noise and simulated noise values (due to the first stage

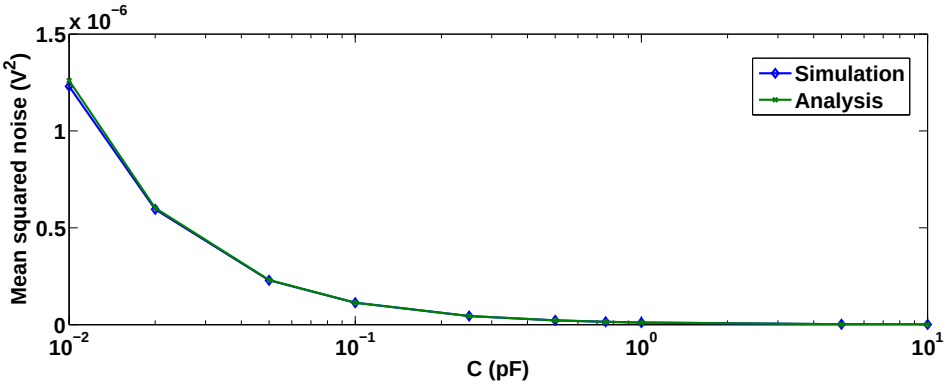


Figure 5.2: Mean squared noise v/s C

transconductance) as the Miller capacitance C is varied. As will be seen later, the first stage contributes the maximum noise to the circuit (till C becomes very large). Equation (5.4) gives the exact expression for the noise only in cases where the circuit settles to its steady state within the half the sampling period $\frac{T_S}{2}$. In cases where this doesn't happen, there is a deviation of analytic noise from simulated noise. (This is noticed in the case where C=10 pF. In this case, circuit doesn't settle to steady state within half the time period.) In such cases, the "time-domain" approach of computing noise (which was used in the previous chapter) can be used. However, when the circuit doesn't settle to

its desired steady state, there is an error in the output. So, it is sufficient to calculate noise for cases where there is settling within the half time period.

5.1.2 Simulation and analytic noise due to g_{m2} for variation of integrated mean squared noise with C

$$\begin{aligned} v_1\left(sC_1+\frac{g_{m2}sC}{g_{m2}+sC}\right)-v_o\left(\frac{g_{m2}sC}{g_{m2}+sC}+\frac{g_{m1}C_B}{C_A+C_B}\right)=0 \\ v_o\left(s(C_A||C_B+C_L)+\frac{sCg_{m2}}{sC+g_{m2}}\right)-v_1\left(\frac{sCg_{m2}}{sC+g_{m2}}-g_{m2}\right)=I(s) \end{aligned} \tag{5.5}$$

Solving the above equations,

$$H_2(s)=\frac{s(C+C_1)g_{m2}+s^2CC_1}{s^3CC_1(C_L+C_A||C_B)+s^2(g_{m2}C_1(C_L+C_A||C_B+C)+g_{m2}C(C_L+C_A||C_B))+sg_{m2}^2C+\frac{g_{m2}^2g_{m1}C_B}{C_A+C_B}} \tag{5.6}$$

The output noise spectral density is

$$S_{vO}(f)=|H(f)|^2\times\frac{8kTg_{m2}}{3} \tag{5.7}$$

Using appropriate contour integration and evaluating mean squared noise using the above transfer function, the output noise comes to be

$$\begin{aligned} &\frac{\frac{2kTg_{m2}}{3}\left(\frac{(C+C_1)^2}{C}\right)}{g_{m2}(CC_1+(C_L+C_A||C_B)(C+C_1))-g_{m1}\frac{C_B}{C_A+C_B}C_1(C_L+C_A||C_B)} \\ &+\frac{\frac{2kTg_{m2}^2}{3}\frac{CC_1}{C_A||C_B+C_L}}{g_{m2}(CC_1+(C_L+C_A||C_B)(C+C_1))-g_{m1}\frac{C_B}{C_A+C_B}C_1(C_L+C_A||C_B)} \\ &\approx\frac{\frac{2kTg_{m2}}{3}\left(\frac{(C+C_1)^2}{C}\right)}{g_{m2}(CC_1+(C_L+C_A||C_B)(C+C_1))-g_{m1}\frac{C_B}{C_A+C_B}C_1(C_L+C_A||C_B)} \end{aligned} \tag{5.8}$$

Table (5.2) shows analytic noise and simulated noise values (due to the second stage transconductance) as the Miller capacitance C is varied.

Capacitance C (pF)	Simulated mean squared noise (V^2)	Analytic mean squared noise (V^2)
0.01	6.44×10^{-9}	6.60×10^{-9}
0.02	4.61×10^{-9}	4.72×10^{-9}
0.05	3.56×10^{-9}	3.63×10^{-9}
0.1	3.21×10^{-9}	3.27×10^{-9}
0.25	3.00×10^{-9}	3.08×10^{-9}
0.5	2.93×10^{-9}	2.98×10^{-9}
0.75	2.91×10^{-9}	2.97×10^{-9}
1	2.89×10^{-9}	2.95×10^{-9}
5	2.87×10^{-9}	2.91×10^{-9}
10	2.85×10^{-9}	2.91×10^{-9}

Table 5.2: Noise due to second stage transconductance

5.1.3 Simulation and analytic noise due to the zero-cancelling resistor for variation of integrated mean squared noise with C

By proceeding along similar lines, the noise transfer function from the zero-cancelling resistor ($H_3(s)$) is,

$$H_3(s) = \frac{sCg_{m2} + s^2CC_1}{s^3CC_1(C_L + C_A||C_B) + s^2(g_{m2}C_1(C_L + C_A||C_B + C) + g_{m2}C(C_L + C_A||C_B)) + sg_{m2}^2C + \frac{g_{m2}^2 g_{m1} C_B}{C_A + C_B}} \tag{5.9}$$

The output noise spectral density is

$$S_{vO}(f) = |H(f)|^2 \times 4kTg_{m2} \tag{5.10}$$

Using appropriate contour integration and evaluating mean squared noise using the above transfer function, the output noise comes to be

$$\begin{aligned} &\frac{kTg_{m2}C}{g_{m2}(CC_1 + (C_L + C_A||C_B)(C + C_1)) - g_{m1}\frac{C_B}{C_A + C_B}C_1(C_L + C_A||C_B)} \\ &+ \frac{kTg_{m2}^2\frac{CC_1}{C_A||C_B + C_L}}{g_{m2}(CC_1 + (C_L + C_A||C_B)(C + C_1)) - g_{m1}\frac{C_B}{C_A + C_B}C_1(C_L + C_A||C_B)} \\ &\approx \frac{kTg_{m2}C}{g_{m2}(CC_1 + (C_L + C_A||C_B)(C + C_1)) - g_{m1}\frac{C_B}{C_A + C_B}C_1(C_L + C_A||C_B)} \end{aligned} \tag{5.11}$$

Capacitance C (pF)	Simulated mean squared noise (V^2)	Analytic mean squared noise (V^2)
0.01	2.41×10^{-9}	2.51×10^{-9}
0.02	3.08×10^{-9}	3.18×10^{-9}
0.05	3.71×10^{-9}	3.80×10^{-9}
0.1	3.97×10^{-9}	4.06×10^{-9}
0.25	4.16×10^{-9}	4.27×10^{-9}
0.5	4.22×10^{-9}	4.30×10^{-9}
0.75	4.24×10^{-9}	4.33×10^{-9}
1	4.26×10^{-9}	4.33×10^{-9}
5	4.28×10^{-9}	4.33×10^{-9}
10	4.28×10^{-9}	4.33×10^{-9}

Table 5.3: Noise due to zero-cancelling resistor

Table (5.3) shows analytic noise and simulated noise values (due to the second stage transconductance) as the Miller capacitance C is varied.

5.2 Comparison with noise of ring amplifier

As the Miller capacitance C increases in the OTA based switched capacitor circuit of figure (5.1), the quality factor reduces. That is, there is less ringing in the circuit. For less ringing, the noise contribution due to the first stage OTA g_{m1} goes down. In the OTA based circuit, there is an additional noise contribution from the zero-cancelling resistor and the second stage OTA g_{m2}.

The number of rings in the ring amplifier based switched capacitor circuits can roughly be treated as an equivalent of the quality factor. The general trend of the integrated mean squared noise decreases with decrease in number of rings. Thus, the general trend of the integrated mean squared noise decreases with increasing V_{OS} and C_{LOAD}. In case of ring-amp based switched capacitor circuits, only the first inverter contributes to noise, other transistors don't. Also, as stated in the previous chapter, decrease in integrated mean squared noise is not uniform as in the case of traditional OTA based switched capacitor circuits. Also, the steady state solution or the "operating point" depends on the input in the ring-amp circuit. Therefore, noise also varies with input in the ring-amp based switched capacitor circuits.

CHAPTER 6

Conclusion and Future Scope

In this work, an existing model for the steady state solution of a ring amplifier was studied in detail and was extended to include the effects of slewing and parasitic capacitances. The effect of different parameters like offset voltage and capacitances on the number of rings (during settling) was studied and the trends were verified by simulation. Based on the model developed and some constraints mentioned in (Hershberg *et al.*, 2012), a design procedure was formulated to help fix the transistor dimensions for a ring amplifier circuit which settles.

"Time-domain" techniques mentioned in (Pavan and Rajan, 2014) were used to analyse the noise in ring amplifier circuits. Various simplifying assumptions were made to explain the trends in noise variation with offset voltage and capacitances. The resulting model, though matches with simulation as far as the trends are concerned, gives only a rough (few 10s of percent error) point by point match for the integrated mean squared noise values. The model can be further improved and better approximations may be used to develop more accurate expressions without loss of intuition. An improvement may lead to prediction of the exact parameter values which minimize noise.

APPENDIX A

LPTV Networks with Sampled Outputs

The results of the (Pavan and Rajan, 2014) were used for the time-domain method of noise analysis in the ring-amplifier circuit. The proofs and other details of the (Pavan and Rajan, 2014) are explained in this appendix.

A linear periodic time varying (LPTV) network, with an input $x(t)$ is considered. It is shown that if the output of this network $y(t)$ is sampled at f_S, an equivalent LTI filter can be found. That is, if the LTI filter is excited by the same input $x(t)$ and the output is sampled at f_S, the output sequence is same as the the sequence of the LPTV network. Also, inter-reciprocity is extended to LPTV systems and used to find equivalent LTI filters from multiple inputs.

A impulse is applied at the input of a system at time $t-\tau$ and the output is observed at time t, where τ is the time difference between the observation of output and application of the input impulse. The impulse response of such a system is $h(t,\tau)$. When a complex exponential $x(t) = e^{j\omega t}$ is applied to such a system,

$$\begin{aligned} y(t) &= \int_{-\infty}^{\infty} x(t-\tau)h(t,\tau)d\tau = e^{j\omega t}h(t,\tau)d\tau \\ &= H(j\omega,t)e^{j\omega t} \end{aligned} \tag{A.1}$$

In a LPTV system with period T_S, $h(t) = h(t+T_S)$ and $H(j\omega,t) = H(j\omega,t+T_S)$. Thus, the "transfer function" can be written as a Fourier series

$$H(j\omega,t) = \sum_{k=-\infty}^{k=\infty} H_k(j\omega)e^{(j\omega_S t)} \tag{A.2}$$

where $\omega_S = \dfrac{2\pi}{T_S}$

The sequence obtained by exciting an LPTV system with $e^{j\omega t}$ and sampling the

output at T_S with an offset of t_o ($< T_S$), is considered

$$\begin{aligned} y[m, t_o] &= y(mT_S + t_o) \\ &\left[\sum_{k=-\infty}^{k=\infty} H_k(j\omega) e^{(j\omega_S t_o)}\right] e^{j\omega(mT_S+t_o)} \\ &= H_{eq}(j\omega) e^{j\omega(mT_S+t_o)} \end{aligned} \tag{A.3}$$

Thus, the output samples of an LPTV system are same as the output samples of an LTI system with transfer function $H_{eq}(j\omega)$ excited by the exponential $e^{j\omega t}$. As any arbitrary signal $x(t)$ can be written as a sum of complex exponentials through Fourier Transforms, by virtue of linearity the above property must hold for any input signal.

If an input is applied to a LPTV system at $t = t_i$ and output is sampled at offset of t_o, resulting sequence is $h(mT_S + t_o, mT_S + t_o - t_i)$, and the equivalent LTI sequence is $h_{eq}(mT_S + t_o - t_i)$. To find $h_{eq}(t)$, an impulse is applied to the system at $t_i = t_o - \Delta t$, and output sequence is recorded. This yields $h_{eq}(mT_S + \Delta t)$. Δt is swept from 0 to T_S in sufficiently fine steps, and $h_{eq}(mT_S + \Delta t)$ is obtained for all values of Δt. Thus, $h_{eq}(t)$ is found.

Inter-reciprocity can be extended to LPTV systems. Inter-reciprocity in LPTV networks implies the following. The sequence obtained by periodically sampling the output at the output port of $\mathcal{N}$ at a timing offset t_o, in response to a input impulse $\delta(t - t_i)$ applied to input port is identical to the sequence that would be obtained by applying the input impulse to the output port of $\hat{\mathcal{N}}$ at time $T_S - t_o$, and sampling the output (at the input port of $\hat{\mathcal{N}}$) at a timing offset $T_S - t_i$. This result is proved using Zak transforms in the (Pavan and Rajan, 2014). The adjoint network is then constructed as follows:

- Linear elements (resistance R, capacitance C and inductance L) of the network $\mathcal{N}$ remain R, C and L in the adjoint network $\hat{\mathcal{N}}$.
- Periodic switches are time reversed. That is a switch which is one in a time interval T in $\mathcal{N}$ is on in the time interval $\overline{T}$ in $\hat{\mathcal{N}}$.
- All controlled sources transform in a similar way as the LTI networks but with an additional time reversal.

Now, the adjoint network is used to compute $h_{eq}(t)$ in a more efficient manner. A

network $\mathcal{N}$ whose output is sampled at offset t_o and its adjoint $\hat{\mathcal{N}}$ are considered. $h_{eq}(mT_S + \Delta t)$ from input to output port of $\mathcal{N}$, is the sequence obtained by sampling the output at an offset of t_o when an impulse is applied at $t_o - \Delta t$. By LPTV inter-reciprocity stated above, it is noted that exactly the same sequence is obtained when an impulse is applied at time $T_S - t_o$ at the output port of the adjoint $\hat{\mathcal{N}}$ and sampling is done at the input port of the adjoint $\hat{\mathcal{N}}$ at timing offset of $T_S - t_o + \Delta t$. Sweeping the time of input impulse application at input port of $\mathcal{N}$ for a constant output observation offset of t_o at the output port of $\mathcal{N}$ is equivalent to keeping the input application at the output port of $\hat{\mathcal{N}}$ constant at $T_s - t_o$ and sweeping the timing offset of output observation at input port of $\hat{\mathcal{N}}$. Hence, $h_{eq}(t - (T_S - t_o))$ is obtained. $h_{eq}(t)$ is only a time-shifted version of the same.

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