Programmable Gain Amplifier (PGA)

and

Loop Filter Design for CTDSM with ELD ≥ 1

A Project Report

submitted by

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in partial fulfilment of the requirements

for the award of the degree of

DEPARTMENT OF ELECTRICAL ENGINEERING

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June 24, 2016

THESIS CERTIFICATE

This is to certify that the thesis titled Programmable Gain Amplifier for Digital Hearing Aid and Loop Filter Design for CTDSM with ELD ≥ 1, submitted by Aravind Nagulu, to the Indian Institute of Technology Madras, for the award of the degree of Master of Technology, is a bonafide record of the work done by her under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree.

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ABSTRACT

The motivation is to design high performance blocks for the frontend of a hearing aid. The frontend blocks include, the programmable gain amplifier (PGA), decimation filter, low dropout regulator (LDO), and ring oscillator. The present work focuses on the design the PGA similar to Kunal Karanjakar's work [1]. PGA is used to amplify the input signal to a sufficiently large output signal, recognized by the $\Delta\Sigma$ analog-to-digital converter (ADC). The gain range is from 0 dB to 40 dB with a resolution of 0.5 dB. Its input referred noise is 2 μV_{rms} with a total harmonic distortion (THD) of -80 dB in a bandwidth of 100 Hz - 10 kHz. To achieve this low input noise at a low power consumption, a pMOS + nMOS transistor differential input pair is used in the PGA. Capacitor is chosen as the gain element for the PGA to reduce the input referred noise.

The most interesting class of data converters is Delta-Sigma ($\Delta\Sigma$) modulators (DSM), which are oversampled noised shaped analog-to-digital converters (ADC). They are implemented either as continuous time (CTDSM) or discrete time (DTDSM) modulators. There are several advantages of implementing the modulator loop-filter with continuous time circuitry such as inherent anti-aliasing property, lower power consumption, higher maximum speed in a given technology. The bandwidth over which a given resolution can be achieved in a DSM is limited by the sampling frequency. For a CTDSM this sampling frequency is limited by the excess loop delay (ELD), which is one of the major concerns in high speed continuous time (CT) $\Delta\Sigma$ modulators. Conventional techniques address the problem of ELD by compensating the modulator only upto half clock cycle delay, which limits the sampling rate. By adding a fast loop around the sample and hold we can compensate the CTDSM with ELD ≥ 1 [5]. In this work, our focus is to port the design of CTDSM with ELD ≥ 1 [4], from UMC 180 nm to SCL 180 nm process.

TABLE OF CONTENTS

LIST OF FIGURES

ABBREVIATIONS

PGA	Programmable Gain Amplifier
CMFB	Common Mode Feedback
THD	Total Harmonic Distortion
ADC	Analog to Digital Converter
SQNR	Signal to Quantization Noise Ratio
LSB	Least Significant Bit
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MSA	Maximum Stable Amplitude
OBG	Out of Band Gain
OSR	Oversampling Ratio
OPAMP	Operational Amplifier
SNR	Signal to Noise and Ratio
PSD	Power Spectral Density

CHAPTER 1

INTRODUCTION

Hearing impairment in humans affects the ability to understand speech, and to localize the surrounding sound sources. Hearing aids are used to improve the hearing ability of a person. All the hearing aids, whether analog or digital, are designed to increase the strength of the sound reaching the ear-drum so that the hearing impaired person can understand speech better.

1.1 Digital Hearing Aid

Digital hearing aids are similar to the analog hearing aids except that they convert the amplified analog signal to digital, process it digitally, and convert the digital signal back to analog. The digitized signal is processed by a digital signal processor (DSP). Some of the important DSP functions are [2]:

- Increasing or decreasing levels of sounds in different frequency ranges
- Reducing background noise by certain noise reduction algorithms
- Varying the gain of the programmable gain amplifier
- Providing directional sound focus

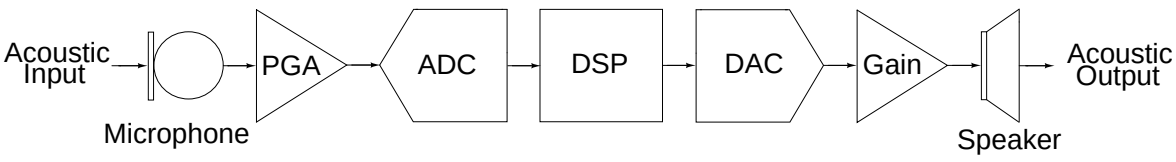


Figure 1.1: Block diagram of Digital Hearing Aid

The major power is consumed by the DSP. For more advanced DSP requirements in the future, the DSP power levels can go further up. So, the power consumed by other blocks has to be reduced. The frontend is composed of the blocks coming before the

DSP, and the backend is composed of the blocks following the DSP. The backend can consume a significant amount of power. The frontend consumes minimum amount of power in the complete chain. The PGA should provide variable gain at low power. The power thus saved can be allocated to the DSP for its advanced functions. In this work, the design of the frontend block, Programmable Gain Amplifier for the digital hearing aid is discussed.

CHAPTER 2

Programmable Gain Amplifier

2.1 Introduction

The PGA is used to amplify the output of the microphone to a sufficiently large value, avoiding overloading of the $\Delta\Sigma$ ADC. The PGA amplifies an input signal in a particular range to an output signal of a fixed amplitude. This output signal amplitude is the maximum stable amplitude (MSA) of the $\Delta\Sigma$ ADC. Thus for the particular input signal range, the ADC operates at its peak SNR. This increases the dynamic range of the frontend. In our case, the input signal range is from 4.5 $\text{mV}_{peak-peak}$ to 450 $\text{mV}_{peak-peak}$, for which the PGA gain varies from 40 dB to 0 dB, giving a constant output amplitude of 450 $\text{mV}_{peak-peak}$. For an input amplitude less than 4.5 $\text{mV}_{peak-peak}$ and greater than 450 $\text{mV}_{peak-peak}$, the transfer characteristic is linear with a constant gain of 40 dB and 0 dB, respectively. Fig. 2.1 shows the transfer characteristics of the PGA. Table 2.1 shows the design specifications of the PGA.

Table 2.1: Design Specifications of the PGA

Input referred noise	2 μV_{rms}
Bandwidth	100 Hz - 10 kHz
THD	-80 dB
Gain Range	0 dB - 40 dB
Gain Step	0.5 dB
Process	65 nm UMC CMOS

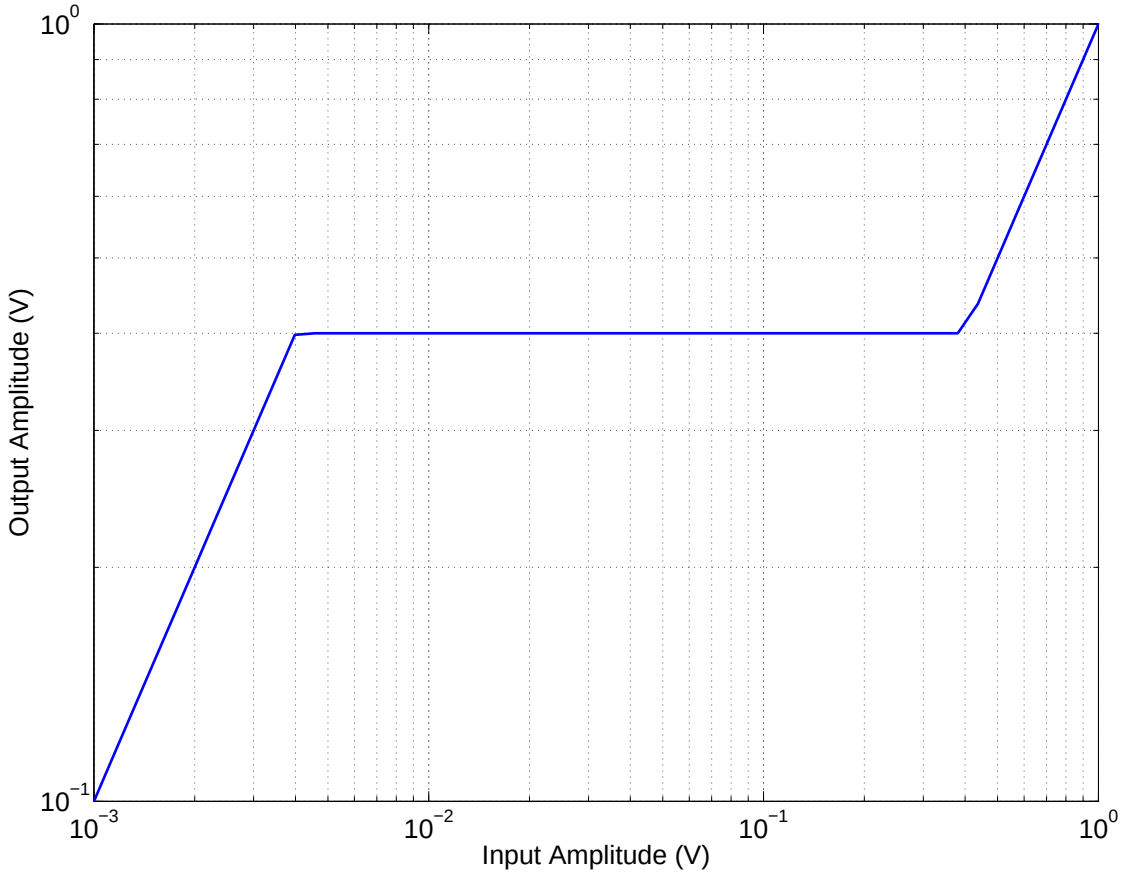


Figure 2.1: PGA Transfer Characteristics [1]

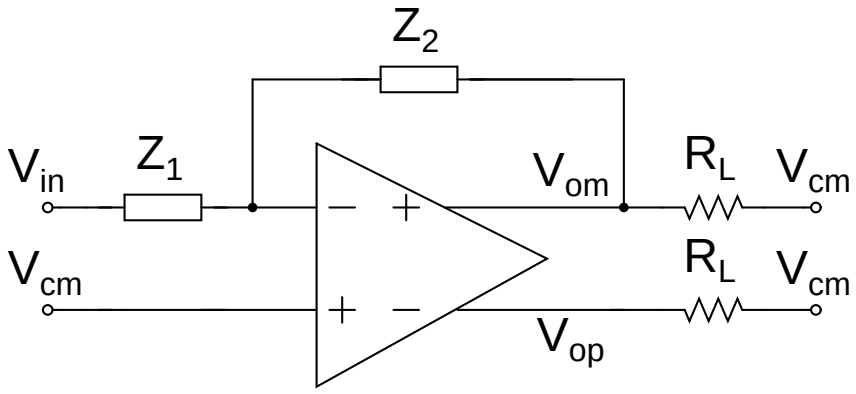


Figure 2.2: Single-ended Feedback PGA Architecture

2.2 PGA Design

The microphone output is single-ended, while the ADC input is differential. The input impedance of the ADC is $R_L = 120\,k\Omega$. The PGA must convert the single-ended input to a differential output. A differential feedback architecture over a single ended feedback architecture to avoid the noise contribution from the output stage CMFB circuit by the

virtue of differential feedback [1]. The differential feedback PGA architecture is shown in Fig. 2.3. The PGA outputs are

$$V_{op} = \frac{Z_2}{2Z_1} Vi, V_{om} = -\frac{Z_2}{2Z_1} Vi \tag{2.1}$$

$$A = \frac{V_{op} - V_{om}}{V_i} = \frac{Z_2}{Z_1} \tag{2.2}$$

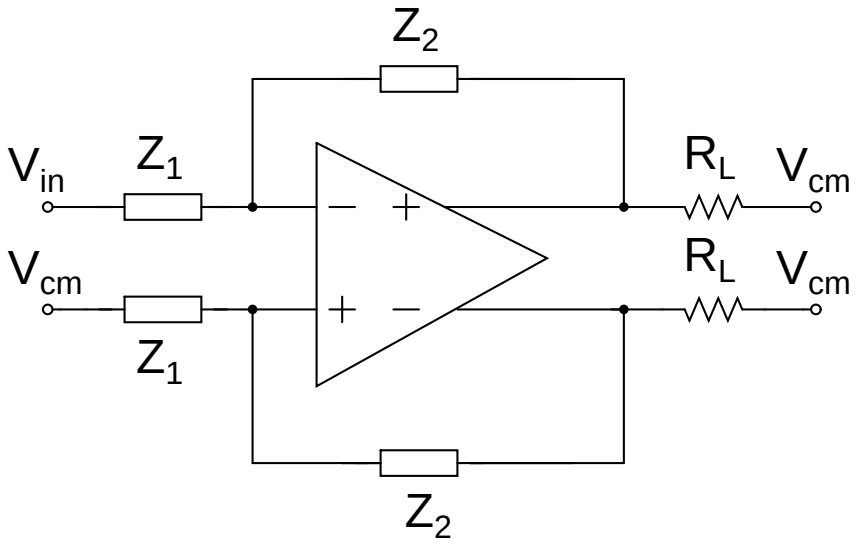


Figure 2.3: Differential Feedback PGA Architecture

2.2.1 Choice of the Gain Element

2.2.2 Differential resistive feedback PGA

Fig. 2.4 shows the differential resistive feedback PGA. The minimum value of resistor R1 is decided based on the loading of the microphone. In our case, the minimum impedance the microphone can drive is 17 kΩ [1]. The input impedance of the PGA is

$$Z_{in} = \frac{2R_1(R_1 + R_2)}{2R_1 + R_2} = \frac{2R_1(1 + A)}{(2 + A)} \tag{2.3}$$

If $Z_{in,min}$ of 20 kΩ [1] is used then for a gain of 40 dB, using (2.6) results in R_1 =

10 kΩ, R_2 = 1 MΩ. The input referred integrated noise voltage of the PGA is

$$V^2_{nres,in} = (8kTR_1 + 8kTR_2(\frac{R_1}{R_2})^2 + S_{n,opa}(1 + \frac{R_1}{R_2})^2).BW \tag{2.4}$$

For $V_{n,in}$ = 2 μV_{rms} we get $V_{n,opa}$ = 1 μV_{rms}. A feedback capacitor C_{feed} should be placed to compensate the pole due to parasitic capacitance C_p and achieve a good phase margin.

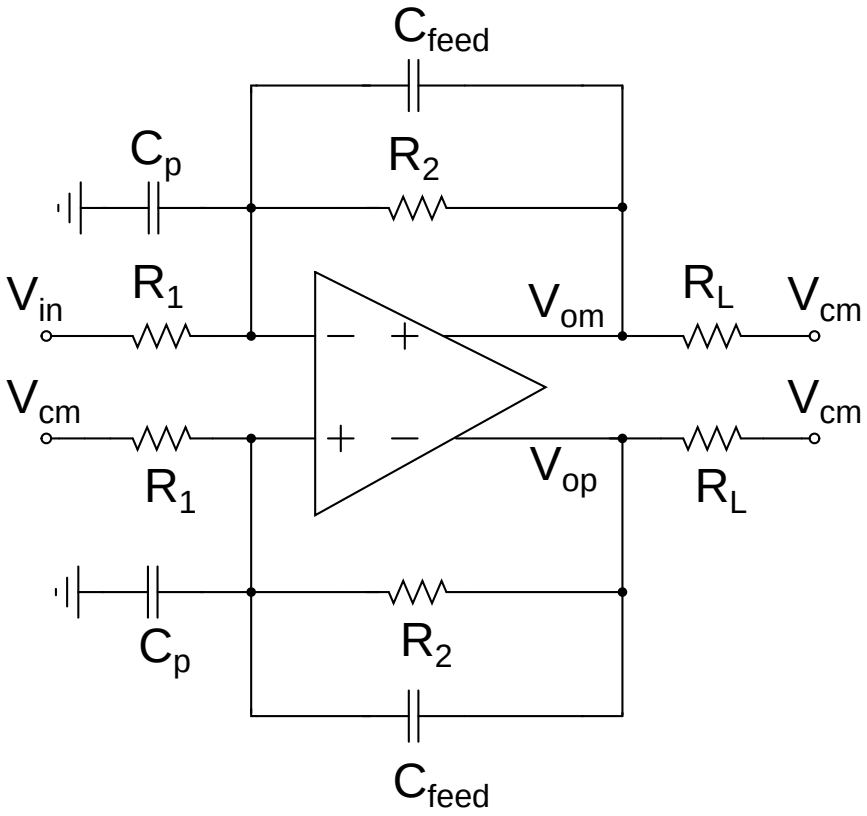


Figure 2.4: Differential resistive feedback PGA

2.2.3 Differential capacitive feedback PGA

Figure 2.5 shows the differential capacitive feedback PGA. The maximum value of capacitance C_1 is constrained by its area occupied on the chip. So C_1 of 20 pF was chosen. The input impedance of the PGA is approximately $1/(\pi f C_1)$. The minimum value of the input impedance is 160 kΩ at a frequency of 100 kHz for a capacitance, C_1 of 20 pF. The input referred integrated noise of the PGA is:

$$V_{ncap,in}^2 = S_{n,opa}(\frac{C_1 + C_2 + C_p}{C_1})^2.BW \tag{2.5}$$

For a parasitic capacitance, C_p of 5 pF and $V_{n,in}$ = 2 μV_{rms} we get $V_{n,opa}$ = 1.6 μV_{rms}. Hence a differential capacitive feedback architecture was used due to relaxed to noise considerations.

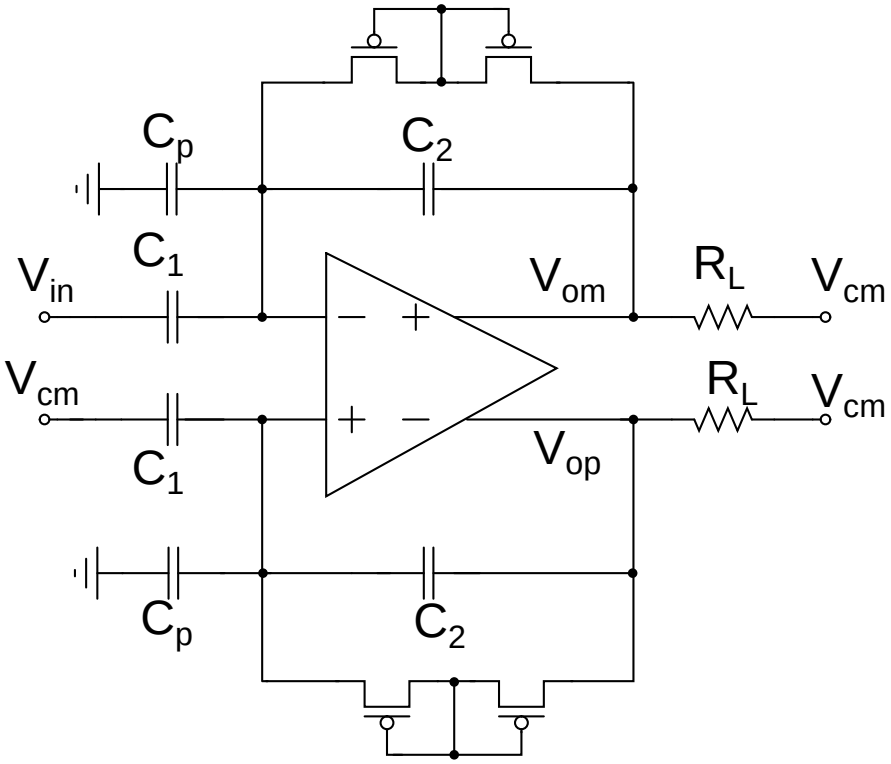


Figure 2.5: Differential capacitive feedback PGA

DC negative feedback around the amplifier is ensured by having a pseudo resistor (MOS transistor with zero gate-source voltage) parallel to the feedback capacitor C_2 as shown in the Figure 2.5.

2.2.4 Op-Amp Architechture

Distortion reduces with increasing the loop gain. For a PGA gain of 40 dB, the loop gain around the op-amp becomes minimum, which increases the distortion. So, a high dc gain of 100 dB is obtained using a three stage op-amp. The input referred voltage

noise spectral density of the op-amp with the pMOS input pair and an nMOS load is:

$$S_{n1}(f) = \frac{16kT}{3g_{mp}}(1 + \frac{g_{mn}}{g_{mp}}) + \frac{1}{C_{ox}f}(\frac{k_p}{W_pL_p} + \frac{k_n}{W_nL_n}\frac{g_{mn}^2}{g_{mp}^2}) \tag{2.6}$$

where g_{mp}, g_{mn} are the transconductances; W_p, W_n are the widths; and L_p, L_n are the lengths of the pMOS and the nMOS, respectively. The pMOS input pair is contributing transconductance, while the nMOS load is contributing only noise. To reduce the input referred noise, a large input transconductance is required. This could be obtained by increasing the current through the input pMOS transistor. But since the need is to design low power PGA, this option is ruled out. Instead, it is decided to give input to both the pMOS and nMOS differential pair [1]. The input transconductance becomes (g_{mp} + g_{mn}). The input referred voltage noise spectral density of the op-amp with both the pMOS and nMOS input pair is:

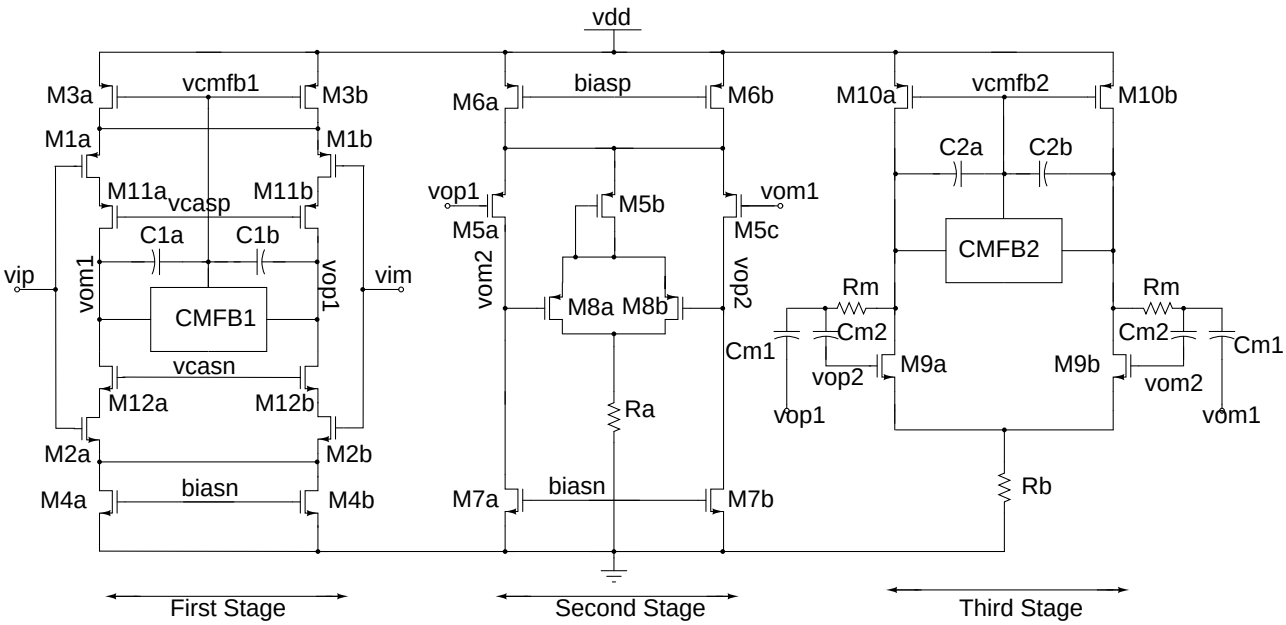
$$S_{n2}(f) = \frac{16kT}{3(g_{mp} + g_{mn})} + \frac{1}{C_{ox}f}(\frac{k_p}{W_pL_p}\frac{g_{mp}^2}{(g_{mp} + g_{mn})^2} + \frac{k_n}{W_nL_n}\frac{g_{mn}^2}{(g_{mp} + g_{mn})^2}) \tag{2.7}$$

Comparing (2.6) and (2.7), results in S_{n1}(f) > S_{n2}(f). Thus, a lower input referred noise can be achieved without increasing the power.

Fig.2.6 shows the circuit diagram of the op-amp while Fig.2.7 shows its CMFB circuit diagram. The opamp used in this work is designed by taking opamp in [1] as reference. The transistors M1a-M1b and M2a-M2b form the input pMOS pair and the nMOS pair, respectively. High V_T devices are used as input transistors to reduce the gate leakage current, flowing through the DC bias resistor. Their widths and lengths are kept large to reduce flicker noise. The bias voltages biasn and biasp are derived from a current mirror based biasing circuit. The first stage CMFB circuit in Fig. 2.7 ensures that its output has the same common mode as the input. Miller capacitors C1a and C1b are used to compensate this CMFB loop. The current in each of the input pairs is 4 μA to get an input referred noise of 1.6 μV_{rms}.

Transistors M5-M8 form the second stage. Transistors M5b and M8a-M8b form the CMFB circuit for this stage. If the common mode voltage at the nodes vop2 and vom2

decreases, it will decrease the current in M8a-M8b, and hence decreases the current in M5b. This increases the current through M5a-M5c as the total current through M6a-M6b is constant, eventually increasing the common mode voltage at the nodes vop2 and vom2. The drain voltage of M7 is decided by the gate voltages of M8a,b. At ff MOS corner, where the threshold voltage (V_T) decreases, the V_{GS} of M8a,b will reduce causing an increase in the g_{ds} of M7a,b, thus degrading the second stage gain. So, a resistance of 50 kΩ is kept in series with the source of M8a,b. This resistance carries a voltage drop of 50 mV to provide sufficient V_{DS} for M7a,b.



M1a,b	(2/0.5)600	M5a,c	(1/1)8	M8a,b	(0.5/0.5)1	M12a,b	(0.5/1)120	Cm2	1 pF
M2a,b	(1.5/1)1200	M5b	(1/1)16	M9a,b	(0.5/0.5)15	C1a,b	500 fF	Rm	14.7 kΩ
M3a,b	(1/1)192	M6a,b	(2/3)24	M10a,b	(2/3)6	C2a,b	500 fF	Ra	50 kΩ
M4a,b	(3/3)40	M7a,b	(3/3)1	M11a,b	(0.5/1)40	Cm1	350 fF	Rb	3.33 kΩ

Figure 2.6: Circuit Diagram of the Op-Amp [1]

Since the input and the output common mode voltages are same, the swing at the op-amp output will be limited by the threshold voltage (V_T) of M9a,b. Apart from providing gain, the second stage also shifts the common mode input of the second stage to a value lower than the third stage output common mode. This is to ensure a signal swing of 200 mV_{peak} over the common mode at the output of the third stage keeping M9a, M9b always in the saturation region. Transistors M14-M16, and the resistor Rcm form the CMFB for the third stage. This CMFB ensures that the output common mode voltage is at vcm. Since it is a two stage CMFB, it is compensated by adding Miller

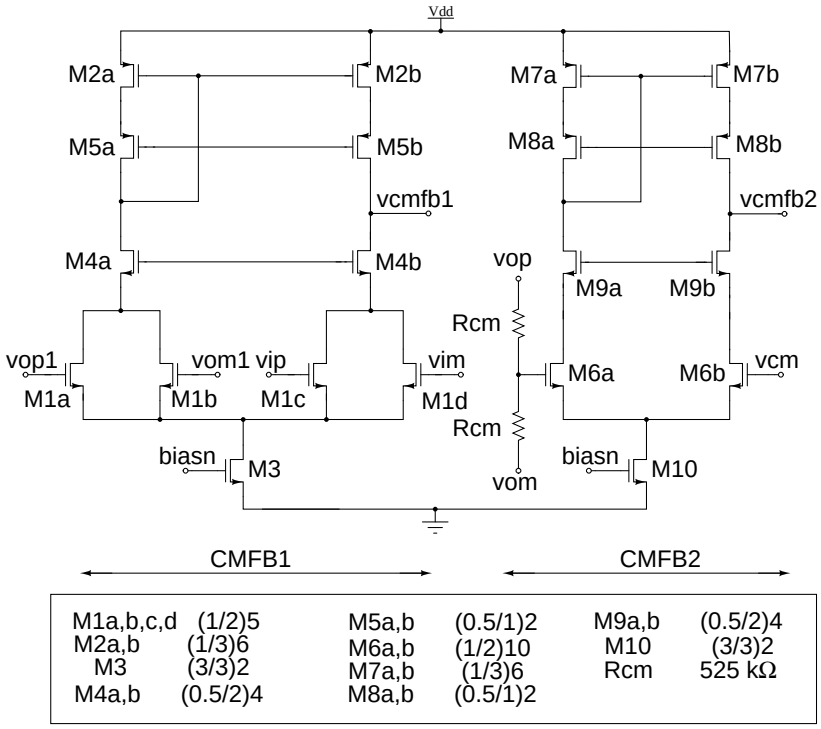


Figure 2.7: CMFB of the Op-Amp [1]

capacitors C2a and C2b. Nested Miller compensation [3] employing capacitors Cm1, Cm2 and a zero-cancelling resistor R_m is used for stabilizing the op-amp. The current in the third stage is fixed to 5.25 μA to get a phase margin of 69° for a PGA gain of 0 dB.

Table 2.2 shows the op-amp characteristics. Fig.2.8 shows the magnitude and the phase response of the loop gain for a PGA gain of 0 dB at different corners. Fig.2.9 and Fig.2.10 show the magnitude and phase response of first and second common mode feedback loop respectively. Fig.2.11 show the common mode step response of the op-amp for a PGA gain of 0 dB and a step of 200 mV at the PGA input node V_i. Fig.2.12 show the differential mode step response of the op-amp for a PGA gain of 0 dB and a step of 200 $mV_{peak-peak}$ at the PGA input node V_i.

Table 2.2: Op-Amp characteristics

Input referred noise	1.33 μV_{rms}
DC Loop Gain	93 dB
Unity loop gain frequency	2.21 MHz
Phase Margin	64.26°
Power consumption	29 μW

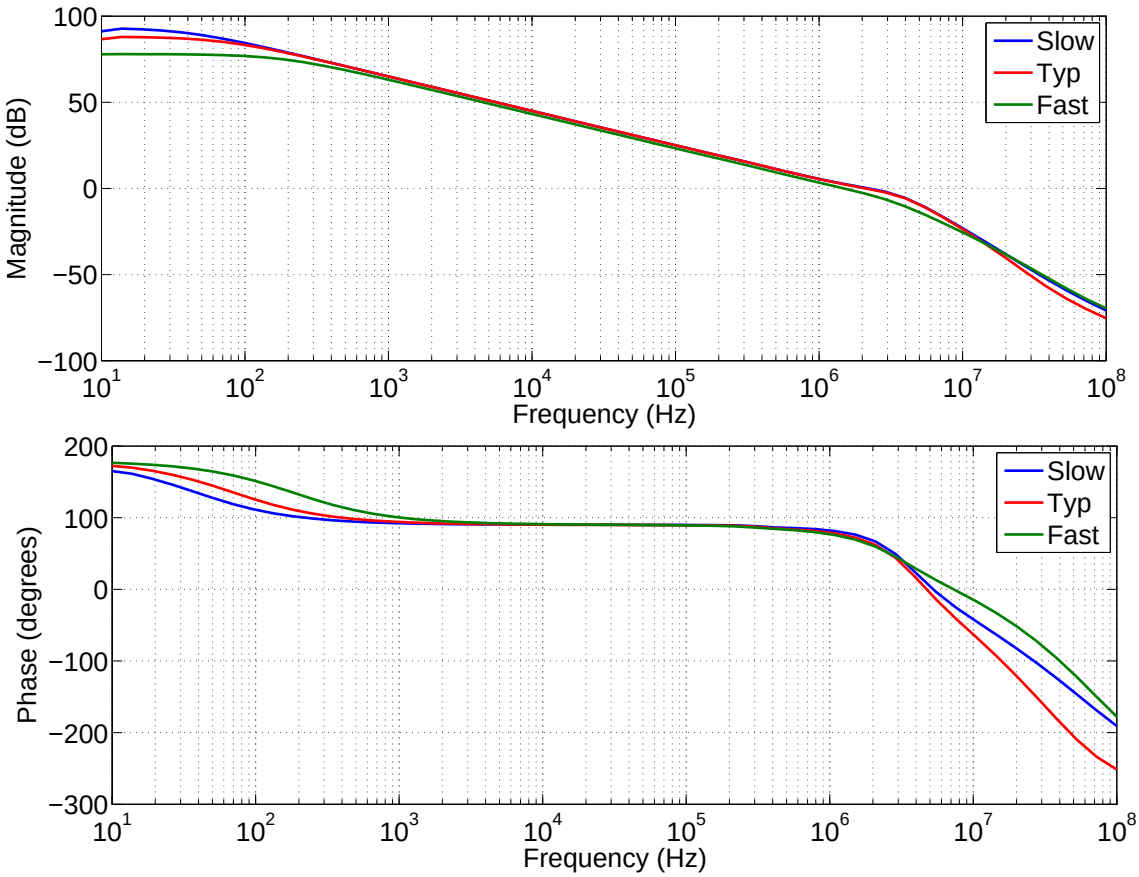


Figure 2.8: Magnitude and Phase response of the loop gain

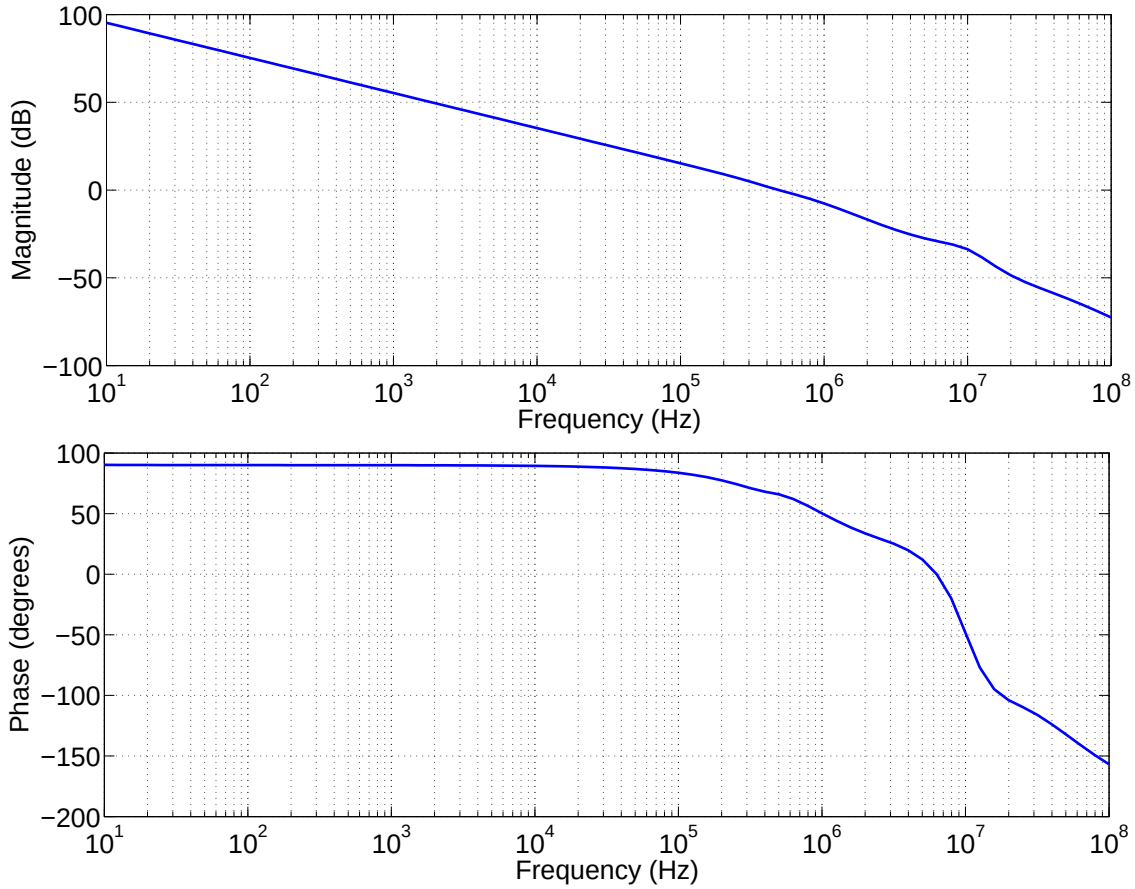


Figure 2.9: Magnitude and Phase response of the CMFB1 loop gain

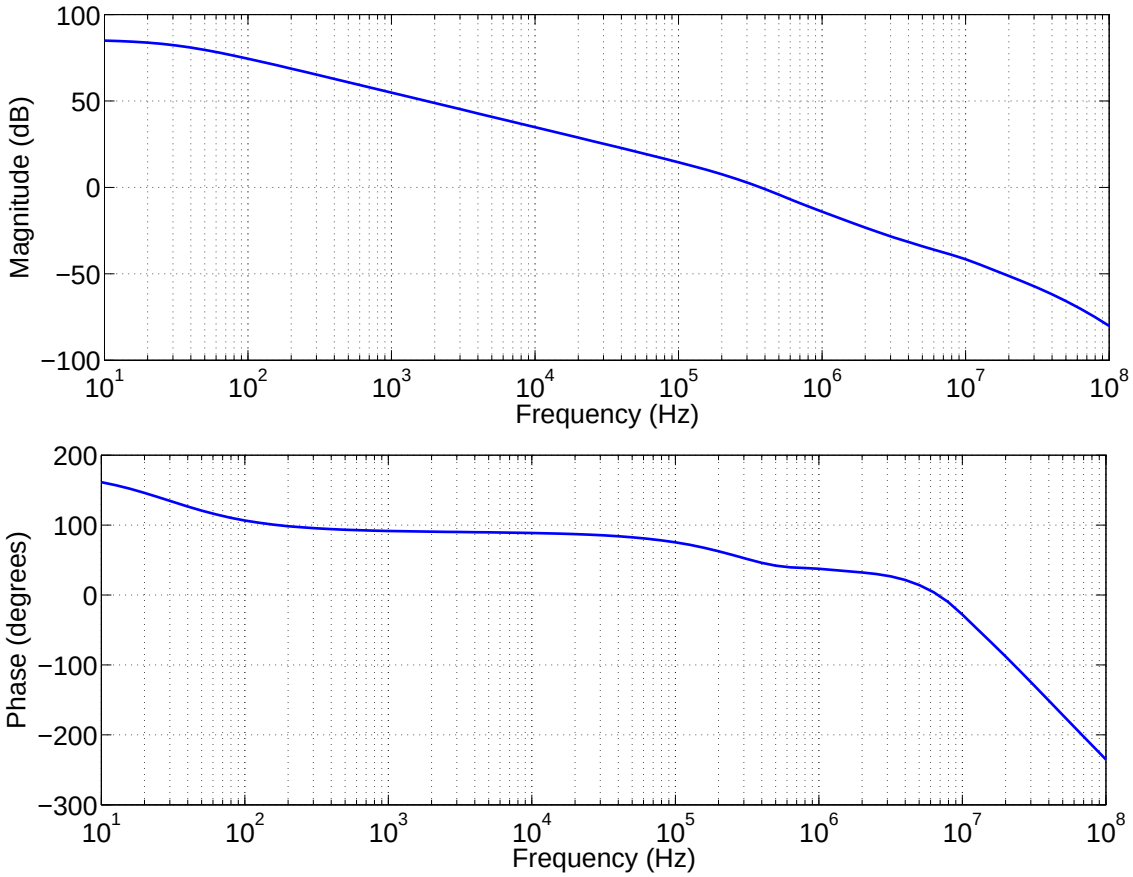


Figure 2.10: Magnitude and Phase response of the CMFB2 loop gain

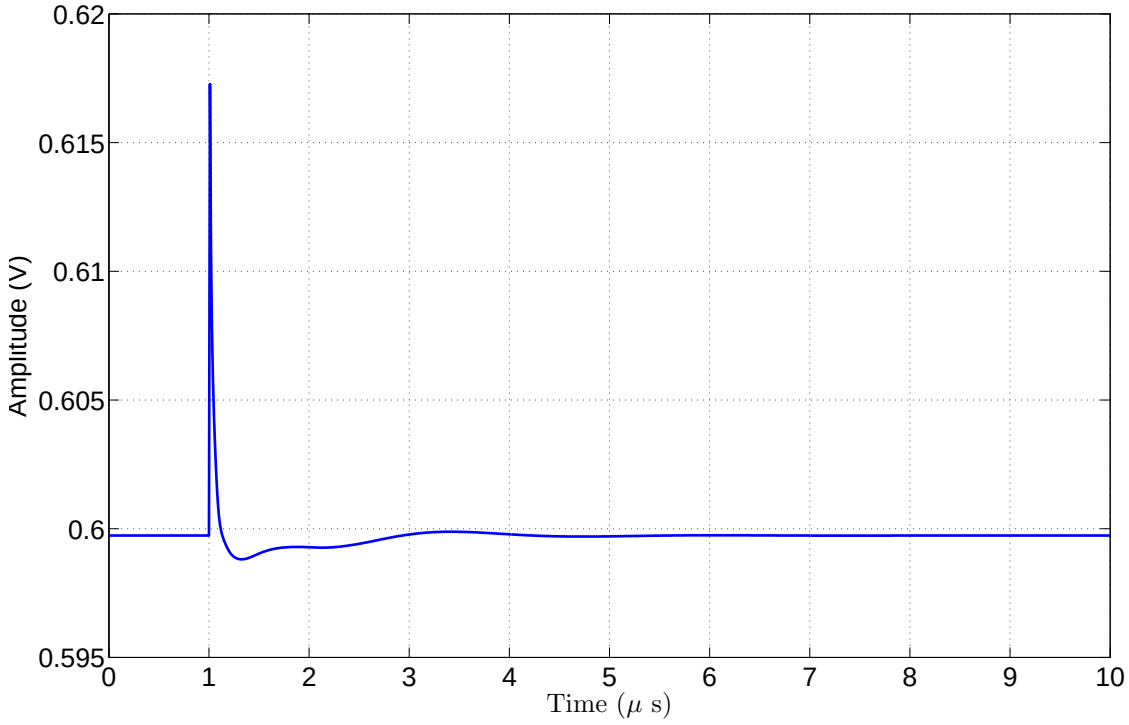


Figure 2.11: Common mode step response of the PGA in 0 dB gain configuration for a input step of 200 mV

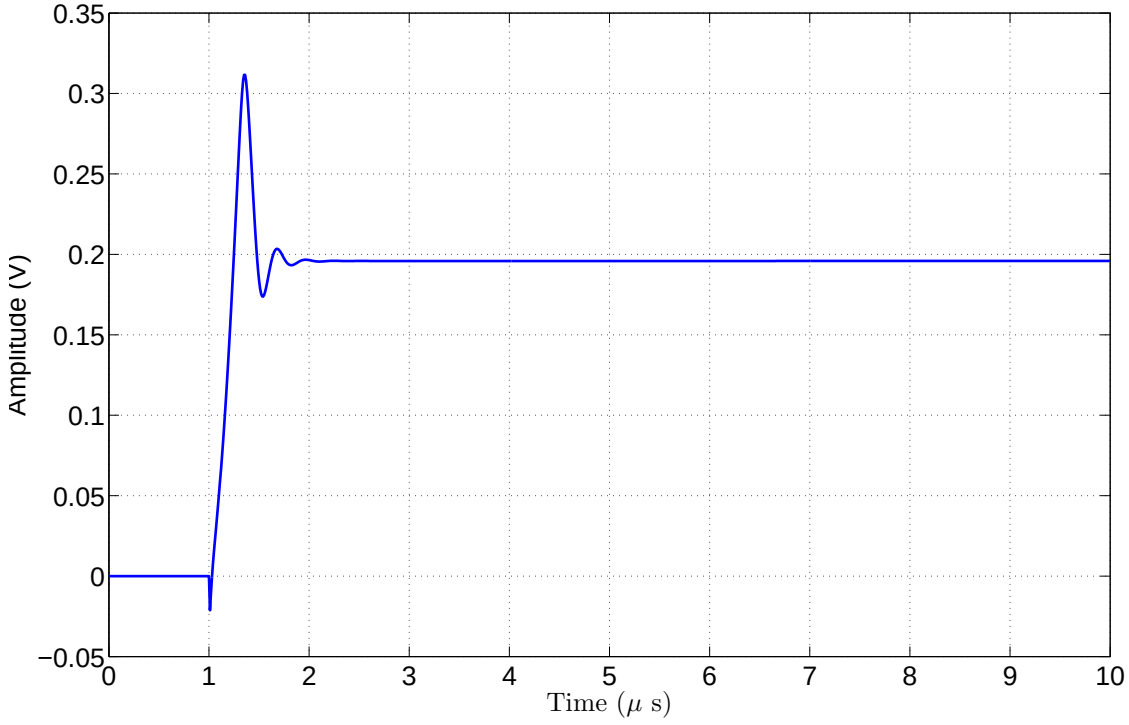


Figure 2.12: Differential mode step response of the PGA in 0 dB gain configuration for a input step of 200 $\text{mV}_{peak-peak}$

2.2.5 Programming linear-in-dB gain steps

The PGA gain varies from 0 dB to 40 dB in steps of 0.5 dB. For this linear-in-dB gain step, changing the input capacitor exponentially results in non-uniform capacitor values. We want to obtain linear-in-dB gain steps with linear changes in the capacitor values. Consider a gain decrement of 0.5 dB from an initial gain G_0 to a gain G.

$$G_0 = \frac{C_{20}}{C_{10}}; G = \frac{C_{20}}{C_1} \tag{2.8}$$

$$\frac{G}{G_0} = 10^{\frac{-0.5}{20}} = e^{\frac{-ln(10)}{40}} \tag{2.9}$$

$$e^x = \frac{1 + \frac{x}{2}}{1 - \frac{x}{2}} \tag{2.10}$$

Using the above approximation for a small x, we get

$$C_1 = C_{10}\frac{1 + \frac{ln(10)}{80}}{1 - \frac{ln(10)}{80}} \tag{2.11}$$

The 80 gain steps needed by the PGA are obtained by incrementing capacitor C_1 from 2 pF to 20 pF in 40 steps and C_2 in two steps, 0.2 pF and 2 pF. Table 2.3 shows values of capacitors for different values of gain from 0 dB to 20 dB. Gain from 20 dB to 40 dB are obtained by decrementing the capacitor C_2 to 0.2 pF.

Table 2.3: C_1 and C_2 for different gains

C_1 (pF)	C_2 (pF)	Increment capacitor (fF)	Gain Interval (dB)
2 - 2.825	2	137.5	0 - 3
3.025 - 4.225	2	200	3.5 - 6.5
4.525 - 6.325	2	300	7 - 10
6.773 - 9.46	2	448.5	10.5 - 13.5
10.13 - 14.16	2	671.5	14 - 17
15.13 - 20	2	973.5	17.5 - 20

2.3 Input Capacitor C_1 in the PGA

Fig.2.13 shows the input capacitor (C_1) bank and Fig.2.15 shows the subsection of the input capacitor (C_1) bank. Terminal T1 is connected to the input source and T2 is connected to the input terminal of the op-amp. The capacitor bank is divided in six branches. Each branch is again divided into 7 branches to obtain 40 gain steps with minimum gain step of 0.5 dB. All switches are implemented as transmission gates using both nMOS and pMOS transistors. The first capacitor in first branch corresponds to C_0 which is 2 pF and the incremental capacitor adds in parallel to C_0 by increasing the input capacitor therefore increasing the PGA gain. The first branch can be programmed for a gain range of 0 dB to 3 dB, the second branch can be programmed for a gain range of 3.5 dB to 6.5 dB, the third branch can be programmed for a gain range of 7 dB to 10 dB, the fourth branch can be programmed for a gain range of 10.5 dB to 13.5 dB, the fifth branch can be programmed for a gain range of 14 dB to 17 dB, the sixth branch can be programmed for a gain range of 17.5 dB to 20 dB. For further higher gains from 20.5 dB to 40 dB, the feedback capacitor is set to 0.2 pF and start running the values of C_1 from 2 pF to 20 pF. In the later sections of the thesis input capacitor in Fig. 2.13 will be represented using the symbol shown in Fig 2.14.

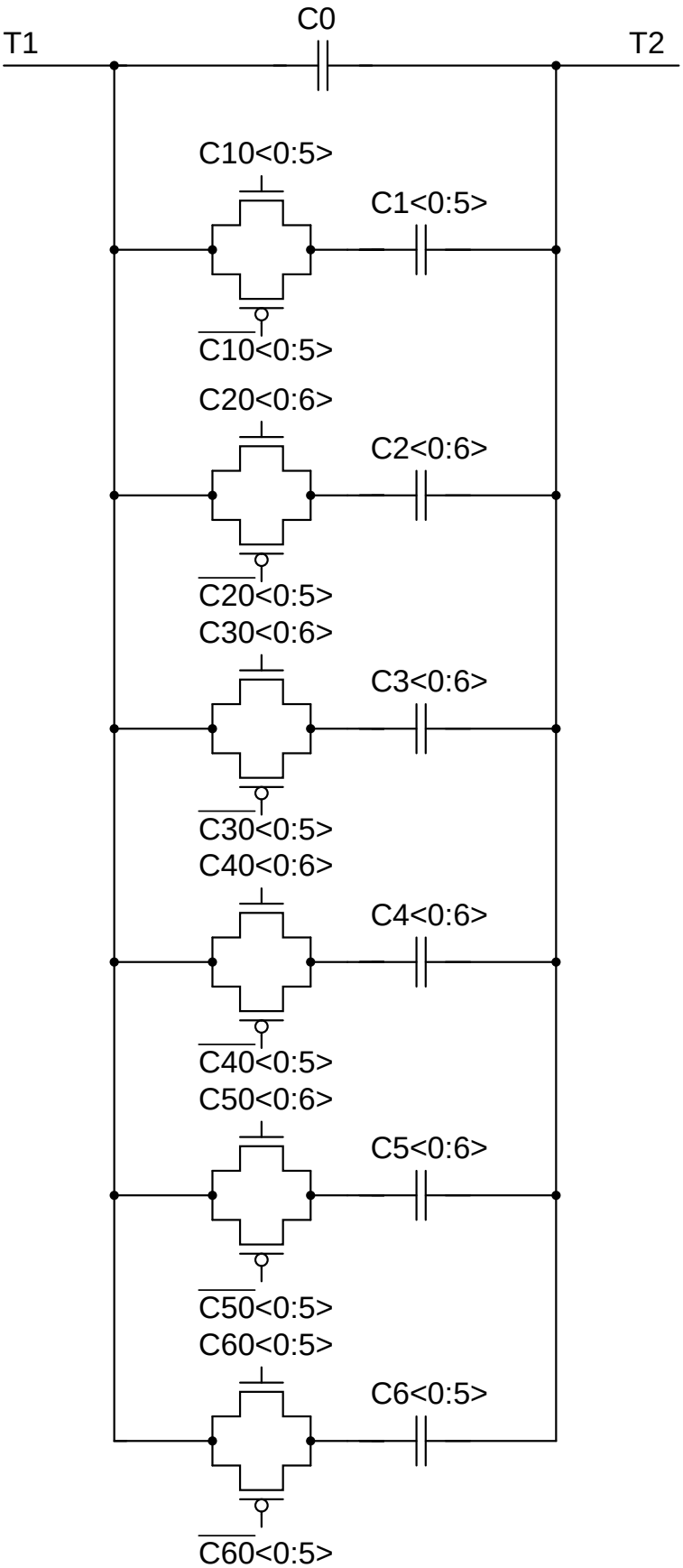


Figure 2.13: Input Capacitor C_1

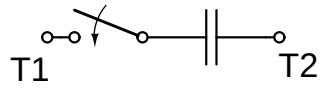


Figure 2.14: Symbol for input capacitor C_1

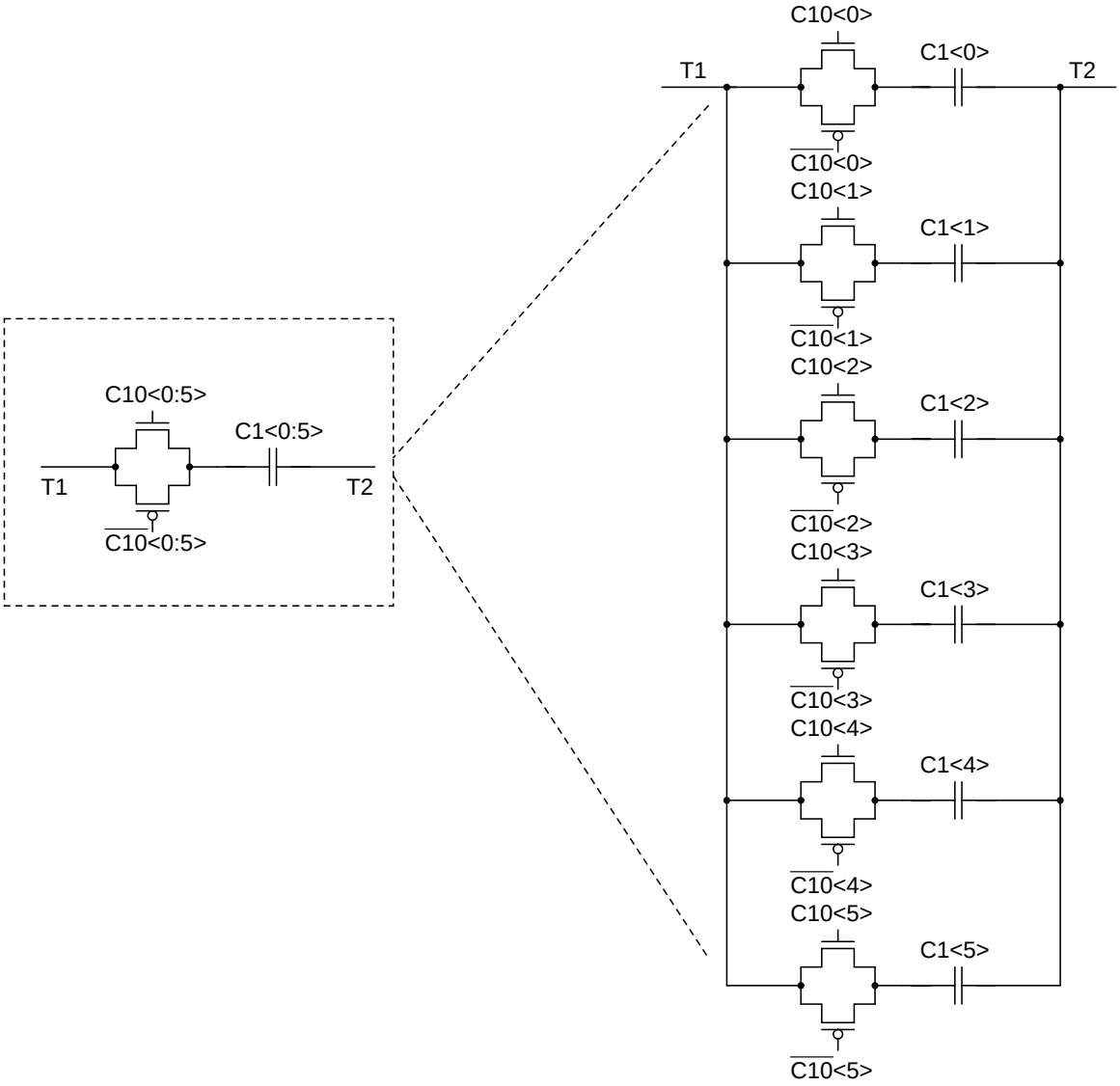


Figure 2.15: Section of Input Capacitor C_1

2.3.1 Switches in the Capacitor banks

Fig. 2.16 and Fig.2.17 shows two possibilities of connecting the switches in the capacitor bank. If we connect the switches as shown in the Fig. 2.17 the non-linearity from the switches will be very less because of less swing on the switches, but the leakage current from the switches will be flowing through the DC bias resistor and the DC bias point will be disturbed. To avoid the biasing issue switches are connected at the input source as shown in Fig. 2.16. However, non-linearity of the switches is not a problem because of the high series impedance of the capacitance at audio frequency.

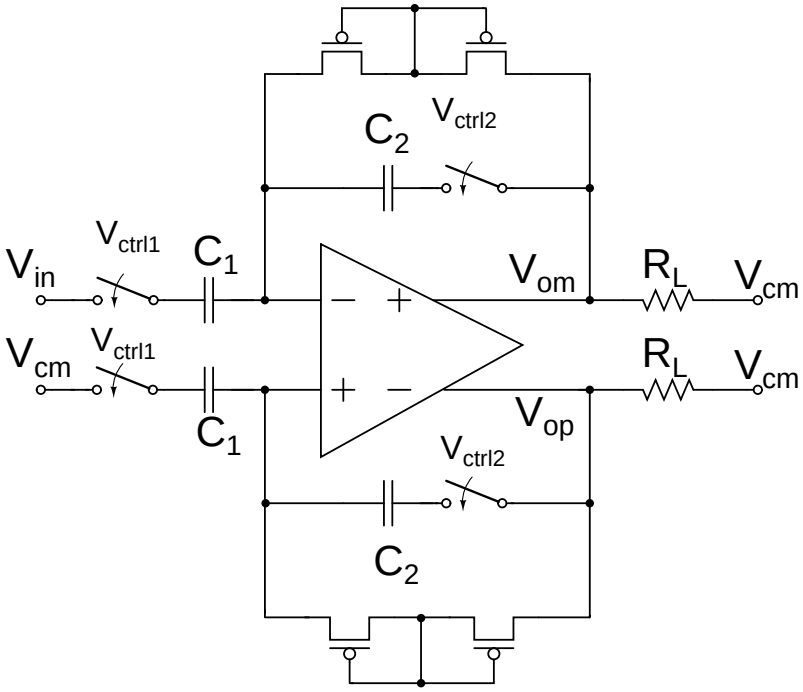


Figure 2.16: Switches connected at the input and output of the PGA

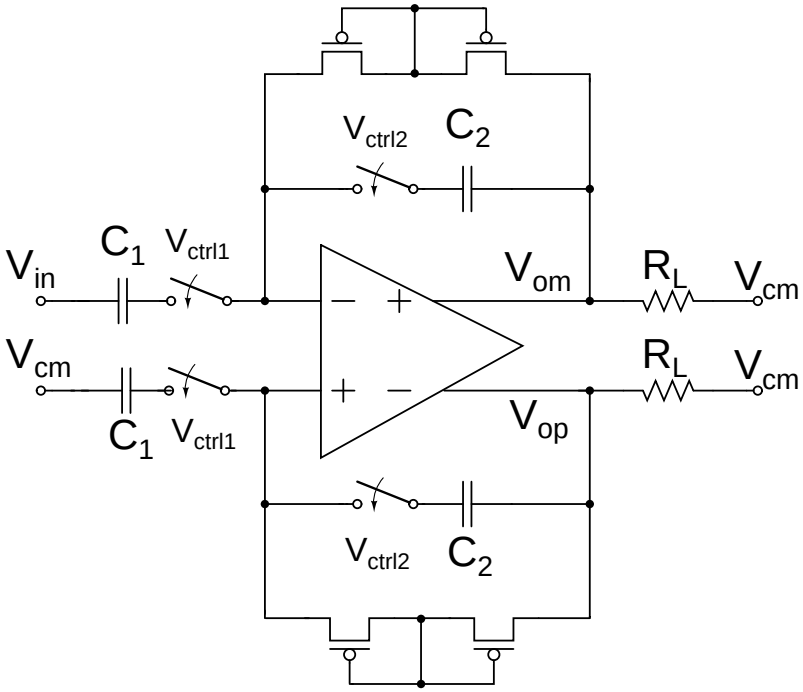


Figure 2.17: Switches connected at the virtual ground nodes of the PGA

2.4 Monotonicity of the PGA gain

Monotonicity in the PGA gain needs to be ensured. At every step an extra capacitance is added to the input capacitor increasing the gain of the PGA. Hence monotonicity is assured for gain range 0 dB - 20 dB and 20.5 dB - 40 dB. For monotonicity the gain G_1 from capacitor combination C_1 of 20 pF and C_2 of 2 pF, should be less than the gain G_2 from the capacitor combination C_1 of 2.137 pF and C_2 of 0.2 pF.

$$G_2 > G_1; G_1 = \frac{C_{10}}{C_{20}}; G_2 = \frac{C_{11}}{C_{21}} \tag{2.12}$$

$$C_{10} = 20pF; C_{20} = 2pF; C_{11} = 2.1375pF; C_{21} = 0.2pF \tag{2.13}$$

$$Hence, G_2 = 20.5dB; G_1 = 20dB \tag{2.14}$$

Since the gains G_2 and G_1 are ratio of metal to metal capacitors, the absolute values of the gains will be virtually the same. The additional 0.5 dB will account for any variations due to unsymmetrical layout. The gain variation of the PGA at the discontinuous points though montecarlo simulation is also negligible. Hence the monotonicity is

ensured.

2.5 Complete PGA architecture

The hearing aid requirement is to accept two different inputs, one from the microphone, and other from the telecoil [1]. Using the switches at the input source of the PGA, the user can switch between the two inputs. At a time, only one of the inputs will be amplified by the PGA. To maintain the differential nature of the circuit, switch is connected at the other input of the PGA (V_{cm}). The distortion introduced by the switches will be very small because of the high impedance capacitance in series with the switches. Fig 2.18 shows the complete PGA architecture.

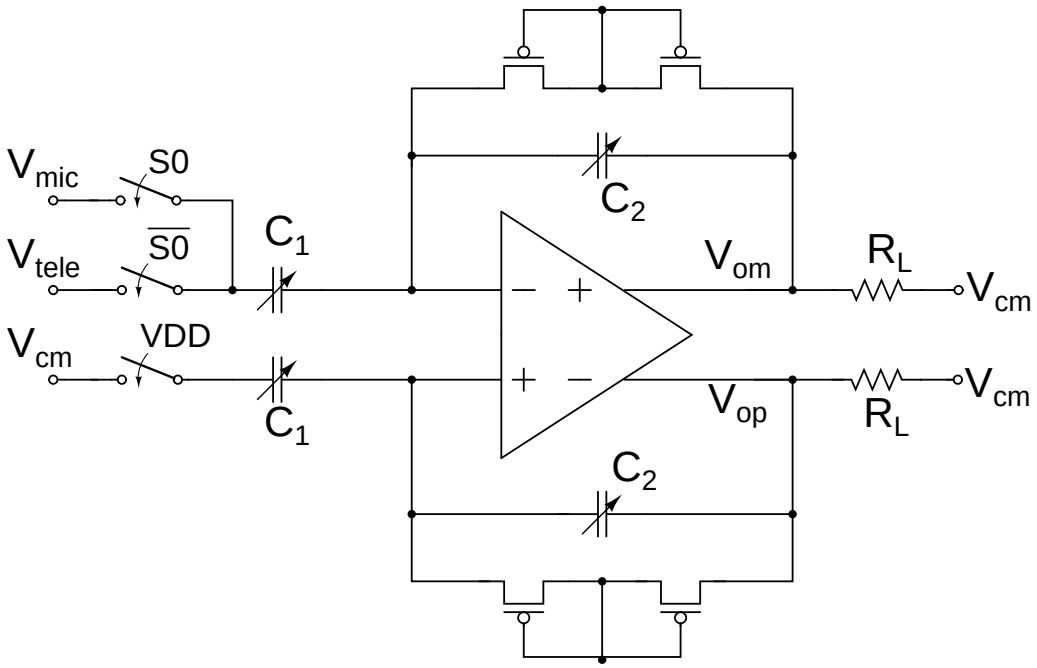


Figure 2.18: Complete PGA Architecture

2.6 Simulation Results

The PGA is simulated for measuring its distortion and noise performance in the 10 kHz bandwidth for various gain settings. The input is given to the V_{mic} node, while the V_{tele} node is at V_{cm}. Table 2.4 shows the simulated results. Fig 2.19 shows the power

spectral density (PSD) of the PGA output for the gain of 0 dB for an input amplitude of 450 $mV_{peak-peak}$ and a frequency of 1.25 kHz.

Table 2.4: THD and input noise in 10 kHz bandwidth

Input Amplitude (mV)	Gain (dB)	THD (dB)	Input referred noise (μV_{rms})
225	0	-80.5	10.2
160	2.95	-87.0	7.44
113	5.93	-88	5.58
80	9.2	-90	4.13
56	12.3	-91	3.19
40	15.8	-92	2.7
24	19.7	-94	2.21
24	20.5	-83	8.9
16	23	-83.8	7.5
11	25.9	-83.5	5.6
8	29.5	-83	4.1
5	32.8	-83.7	3.15
3.5	36.7	-82.6	2.2
2.3	40.1	-82.8	1.9

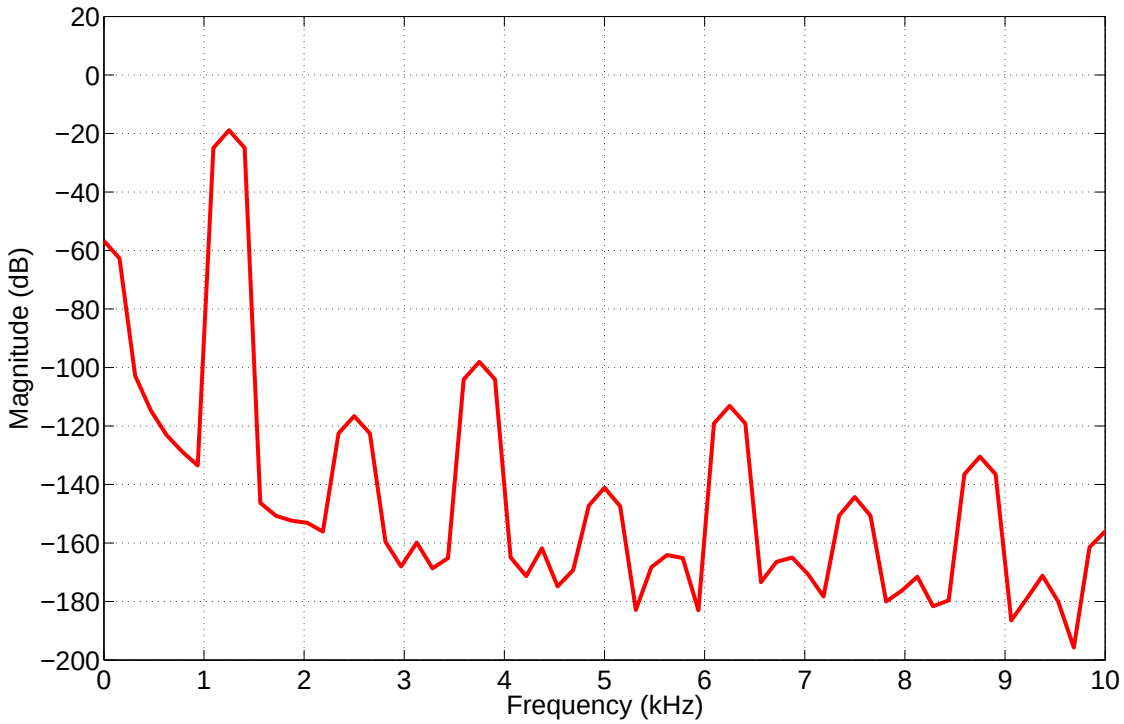


Figure 2.19: PSD of the PGA output for 450 mVp input

2.7 Layout

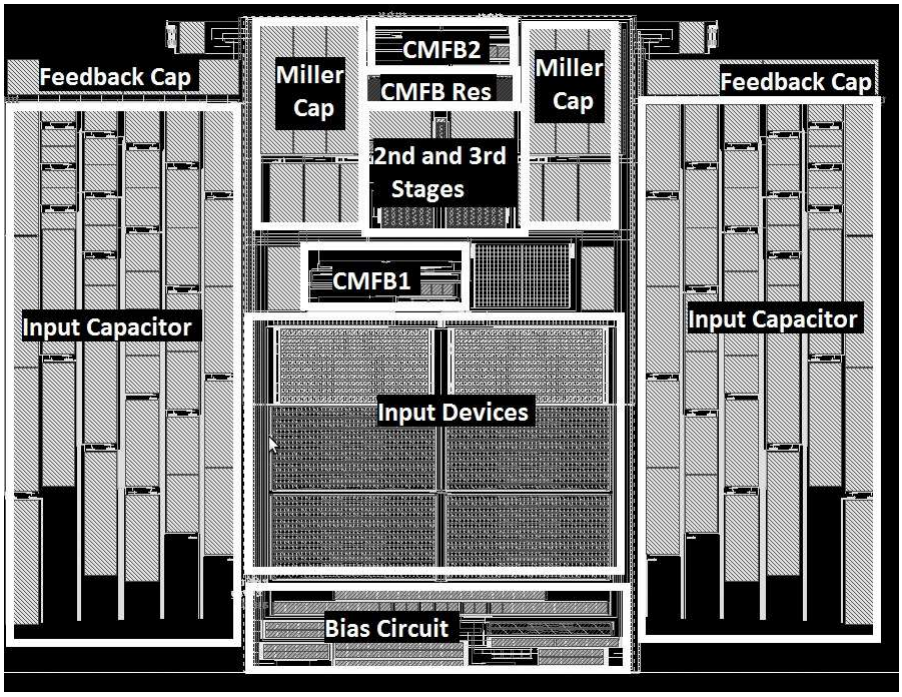


Figure 2.20: Layout Screenshot

2.8 Testbench and Simulations

The variables c0, sum1 and sum2 saved in the cadence state are the gain control variables. Table: 2.5 shows how to program PGA to different gains. When c0 value is 1 the PGA gain varies from 20 dB to 40 dB. The gain variation of the PGA after layout extraction for different values of code is shown in Figure 2.21. Figure 2.22 shows the gain step of the PGA after layout extraction for different values of code. The PGA is monotonic because the gain step is always above 0 dB line.

Table 2.5: Programming PGA Gain

c0*	sum1*	sum2*	PGA Gain	Code
0	0 - 5	0	0.085 - 2.54	0 - 5
0	0 - 6	1	2.96 - 5.93	6 - 12
0	0 - 6	2	6.34 - 9.36	13 - 19
0	0 - 6	3	9.77 - 12.81	20 - 26
0	0 - 6	4	13.23 - 16.28	27 - 33
0	0 - 5	5	17.27 - 19.68	34 - 39
1	0 - 5	0	20.59 - 23.04	40 - 45
1	0 - 6	1	23.46 - 26.11	46 - 51
1	0 - 6	2	26.8 - 29.87	52 - 58
1	0 - 6	3	30.28 - 33.32	59 - 65
1	0 - 6	4	33.73 - 36.79	66 - 72
1	0 - 5	5	37.78 - 40.1	73 - 79

* - only integer values

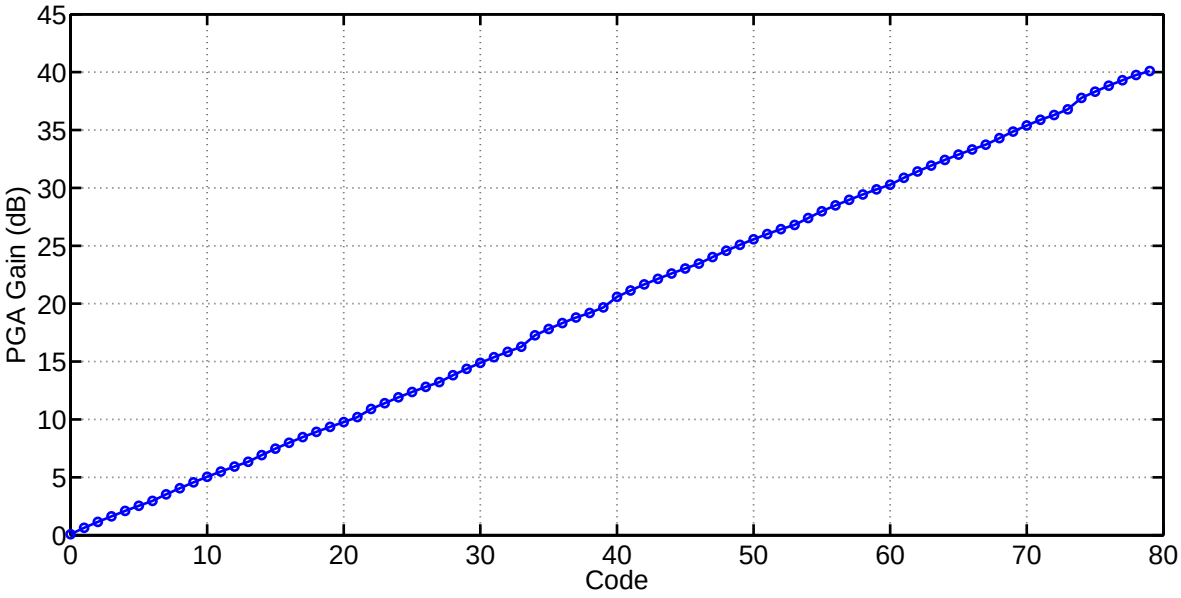


Figure 2.21: PGA gain for different values of code

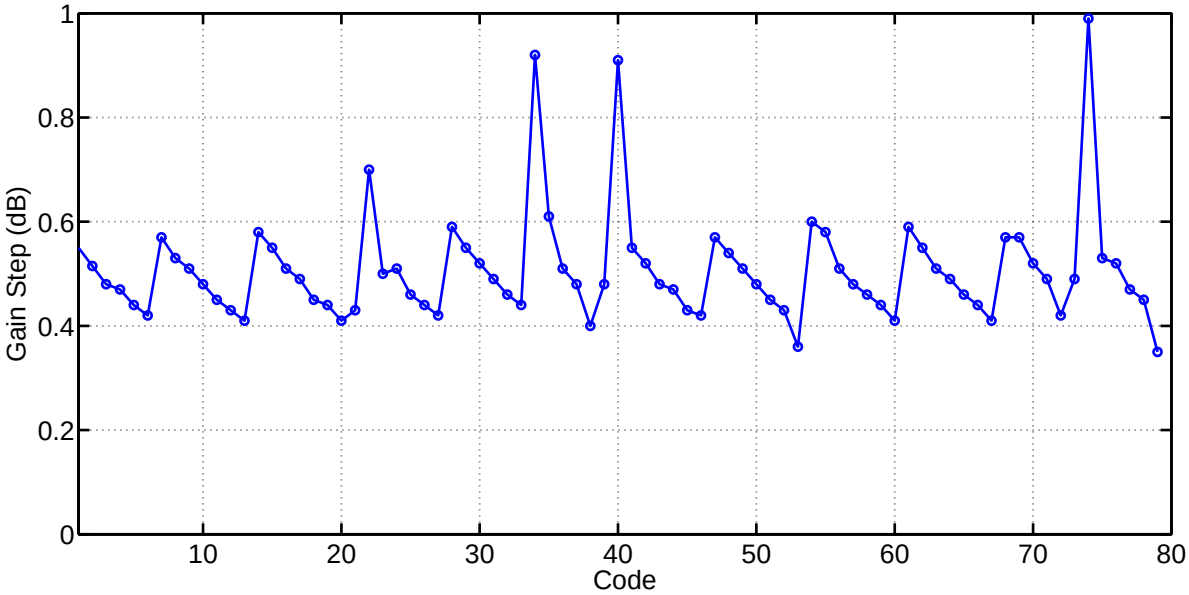


Figure 2.22: PGA gain step for different values of code

CHAPTER 3

CTDSM - Compensating excess loop delay of more than one clock cycle

3.1 Introduction

The following chapter explains the limitations of classical compensation techniques and will be talking about the compensation technique for CTDM with ELD ≥ 1 [5]. In the continuous time loop filter realized from a discrete time loop filter using d2c command in the Matlab, it is assumed that the delay between the sampling instant of the loop filter output and the generation of the new output is zero. However, in real circuits, this delay, known as excess loop delay (ELD), is non-zero due to the finite speed of transistors. The ELD usually consists of delays introduced by the regeneration time of the latch in the quantizer (including the dynamic element matching (DEM) logic if necessary), switching time of the DAC, and due to parasitic poles in the loop filter.

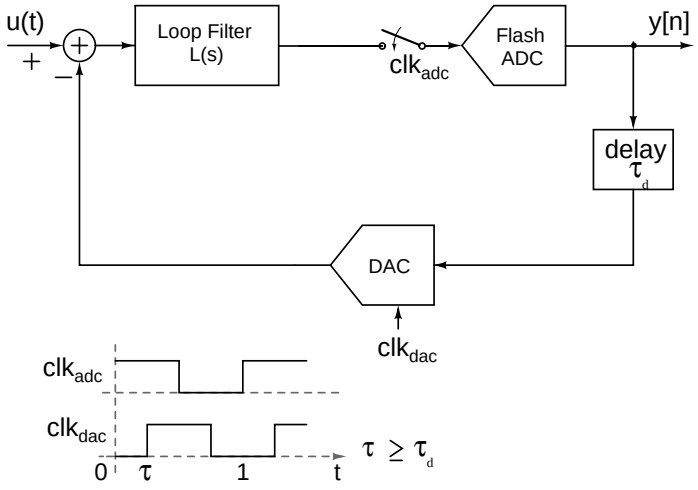


Figure 3.1: Block Diagram of CTDSM with ELD [4]

Fig. 3.1 shows the block diagram of a standard single-loop CTDSM. Because of the delay τ_d in the loop shown in Fig. 3.1, the DAC will have to be clocked at a time $\tau >$

τ_d delayed from the sampling instant of the ADC.

Fig. 3.2 shows three possible rectangular DAC pulses. For NRZ and RZ pulse case, the entire delay τ_d has to be compensated by some ELD compensation technique. However, if a HRZ DAC pulse is used, then half the clock cycle delay can be absorbed by the explicit half clock delay of the DAC pulse.

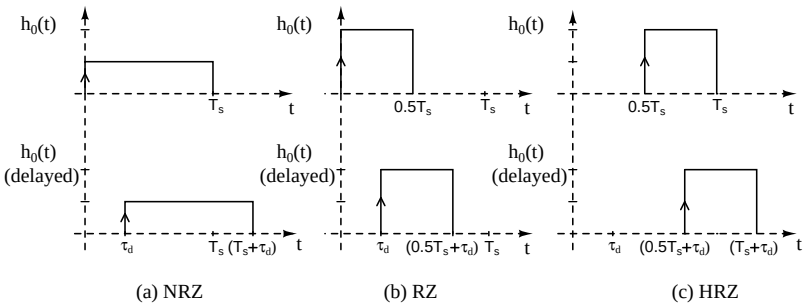


Figure 3.2: Impulse responses of the rectangular NRZ, RZ and HRZ DAC pulses for, (a) Top row: no delay, (b) bottom row: a delay of τ_d [4]

3.2 Compensating ELD using a differentiating path in the loop filter

In this technique above problem is removed by using an analog direct path from the output of the DAC. Fig. 3.3 shows this technique. Due to ELD the second sample of NTF becomes zero, the direct path k_0 provides the second sample. The remaining coefficients k_{1-n} adjusted such that the NTF is restored. Gain coefficient k_0 is realized using a differentiator following the first integrator in the loop filter. The differentiator is realized by passing output of the first integrator to virtual node of the summing opamp using a capacitor. The drawback of this technique is that the loop delay includes the delay of the main DAC and the loop filter. For a NRZ DAC pulse with ELD of τ_d the coefficients of the loop filter will be modified as follows [6]:

$$k_n = K_n \tag{3.1}$$

$$k_{n-1} = K_{n-1} + K_n\tau \tag{3.2}$$

$$k_{n-2} = K_{n-2} + K_{n-1}\tau + K_{n-2}\frac{\tau^2}{2!} \tag{3.3}$$

$$k_1 = K_1 + K_2\tau + K_3\frac{\tau^2}{2!}.... + K_N\frac{\tau^{N-1}}{(N-1)!} \tag{3.4}$$

$$k_0 = K_1\tau + K_2\frac{\tau^2}{2!} + K_3\frac{\tau^3}{3!}... + K_N\frac{\tau^N}{N!} \tag{3.5}$$

where k_{0-N} are the coefficients of the modulator with ELD of τ_d and K_{1-N} are the coefficients of modulator without ELD.

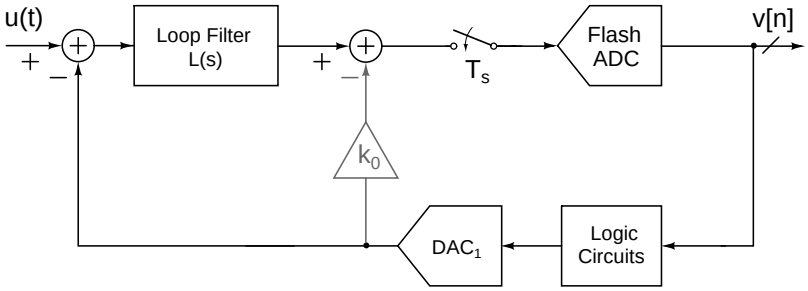


Figure 3.3: Block diagram of CTDSM with ELD compensation that is obtained by bypassing loop filter [4]

3.3 Fundamental limitations of classical compensation techniques

The method described in the last section is effective only if the quantizer delay is less than one clock cycle. To understand this, Fig. 3.3 is modified by moving the sampler before summation as shown in Fig. 3.4. Here, the feedback path DAC is shown as an NRZ DAC pulse which is followed by a delay block. The sampled impulse response at the output of the loop filter L(s), the direct path k_0, the resulting NTF impulse response and the NTF magnitude response are shown in Fig. 3.5 for different values of ELD. A fourth order modulator with an Out of Band Gain (OBG) of two and a sampling rate of 1 Hz is used as a prototype.

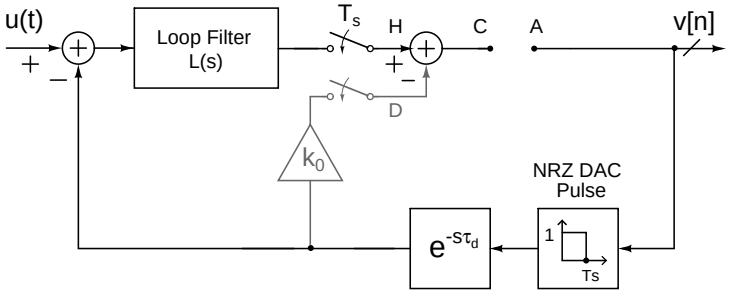


Figure 3.4: Fig. 3.3 modified to show the sampled outputs of L(s) and direct path separately. The loop broken at the input of flash ADC [4]

The top row of Fig. 3.5 corresponds to the delay free case. In this case, the contribution of the direct path is zero to make the sampled impulse response at C equal to the ideal value in Fig. 3.4. The second row corresponds to a half period delay. The second and subsequent samples of the output of the loop filter L(s) are reduced compared to the delay free case. Compensation is achieved by adding an appropriately scaled contribution from the direct path and adjusting coefficients in the loop filter L(s) to make the sampled impulse response at C in Fig. 3.4 the same as in the delay free case. The resulting NTF (Fig. 3.5 (2c)) is exactly the same as in the ideal case (Fig. 3.5(1c)). As ELD increases, the second sample decreases further, and the contribution required from the direct path increases.

The third row corresponds to an ELD of one and a half clock cycles. The second sample of the output of the loop filter L(s) is zero. In this case however, the contribution of the direct path is also zero and the second sample cannot be restored to its ideal value regardless of the choice of k_0 . Therefore, the second sample of the impulse response at C in Fig. 3.4 is zero. This results in an NTF whose second sample is always zero (Fig. 3.5 (3c)). Good lowpass NTFs cannot be realized with stable minimum phase transfer functions having a zero valued second sample in their impulse responses [4]. An example of the magnitude response of a stable NTF optimized for noise suppression at low frequencies, with second NTF sample being zero is shown in Fig. 3.5 (3d). Compared to the ideal case (Fig. 3.5 (1d)), the quantization noise suppression is worse and there is a greater peaking, indicating that conventional compensation techniques are

not effective for ELD exceeding a clock cycle.

The only way to obtain a non zero second sample in the impulse response from A to C in Fig. 3.4 is to have an additional feedback path which does not depend on the quantizer [4]. The delay of this path has to be less than a clock cycle.

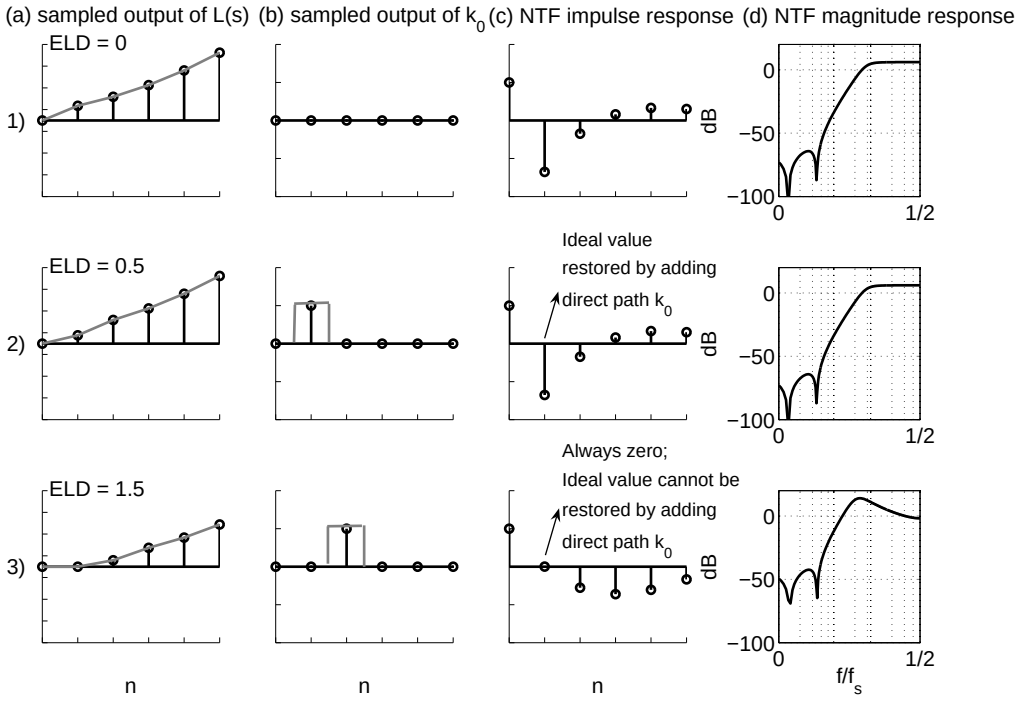


Figure 3.5: Limitation of conventional ELD compensation with $\tau_d > 1$; Each row shows the discrete time equivalent impulse response of the loop filter L(s) and the direct path k_0 (with the continuous time waveforms in gray) and the NTF impulse response that results from the combination. For clarity, columns (a), (b), and (c) are shown to different scales. [4]

3.4 Compensation technique for ELD > 1

Fig. 3.6 shows the modulator of Fig. 3.3 with an additional feedback loop around the sampler. A zero-order-hold converts the discrete-time signal into a continuous-time signal. In practice, the zero-order-hold is realized using a separate sample and-hold circuit (S/H). Since the new loop requires only a S/H, its delay is much smaller than that of the quantizer and the digital logic, and can be designed to have a delay less than a clock cycle from A to C. As before, the loop is broken at the point marked X and the discrete time impulse response from A to C is adjusted to be that of the ideal loop filter.

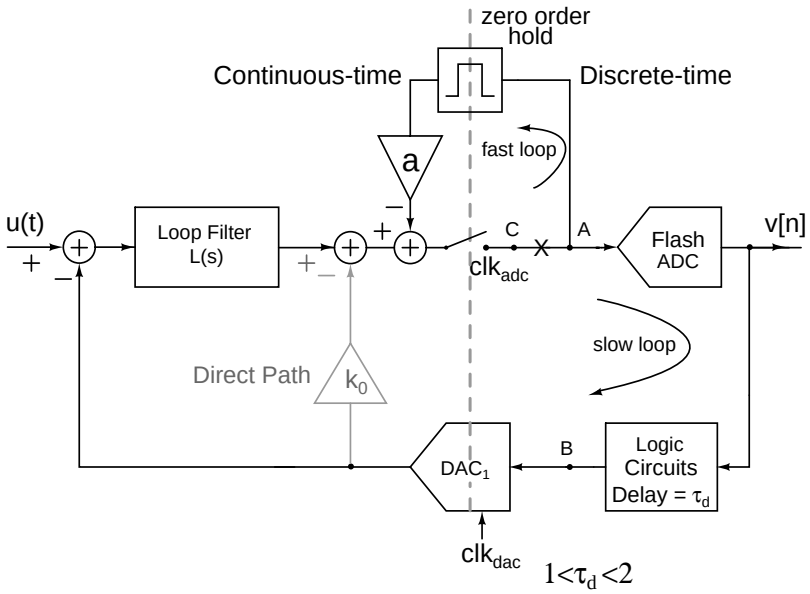


Figure 3.6: Block diagram of a $\Delta\Sigma$ ADC with ELD compensation obtained by bypassing the flash ADC using an S/H [4]

Here, the second sample of the original loop filter impulse response from A to C is obtained by adjusting the coefficient a in the fast loop. After getting the second sample accurately from the fast loop, coefficients are adjusted to match the rest of the samples to their ideal values [4].

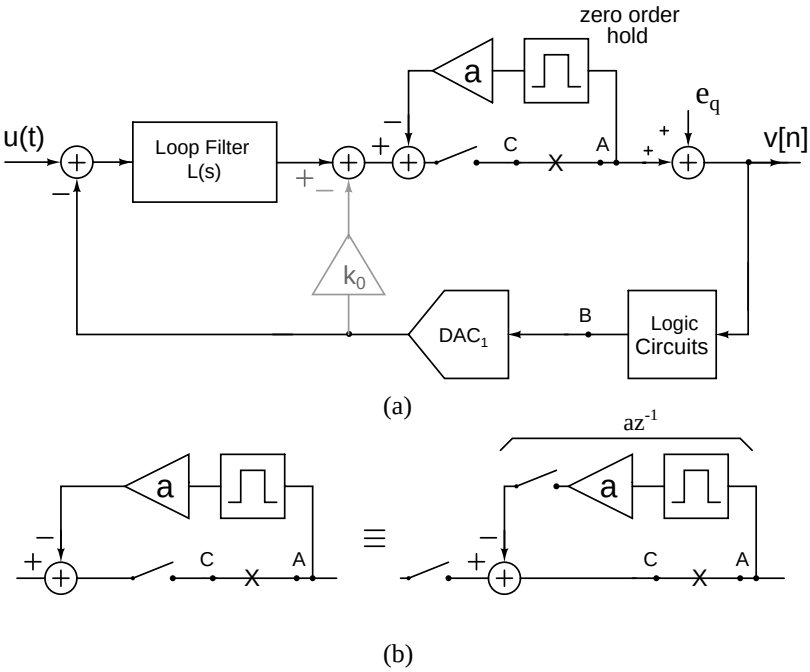


Figure 3.7: (a) Proposed $\Delta\Sigma$ modulator with additive quantization noise eq and (b) calculating the transfer function of the fast loop [4].

Fig. 3.7(a) shows the proposed structure with additive quantization error e_q. The

transfer function before the quantizer consists of the sampled outputs of L(s) and k_0 cascaded with the fast loop. From Fig. 3.7(b) it is seen that the transfer function of the fast loop is $1/(1 + az^{-1})$. The transfer function from the quantization error e_q to the output V is then calculated as follows [4]:

$$\frac{V(z)}{E_q(z)} = \frac{1 + az^{-1}}{1 + az^{-1} + (k_0 + L_d(z))z^{-2}} \tag{3.6}$$

Where L_d(z) corresponds to the sampled output of L(s). As mentioned in the previous section, the denominator is adjusted to be the same as that in the ideal NTF. Therefore,

$$NTF = (1 + az^{-1})NTF_{ideal}(z) \tag{3.7}$$

An additional zero appears in the noise transfer function, reducing the in-band signal to quantization noise ratio SQNR to some extent.

CHAPTER 4

Fourth Order Loop Filter

4.1 Architecture

A fourth order loop filter with optimized zeros (for an OSR of 25) is used for the current design, same as the modulator in [4]. Loop filter architecture was chosen to be cascade of integrator with feedforward summation (CIFF) as shown in Fig. 4.1(a). The main advantage of CIFF over cascade of integrator with distributive feedback (CIFB) is that the signal component at the integrator outputs is a lot smaller. This increases the linearity of the loop filter. Secondly, a 4-bit quantizer is used in the present implementation. A

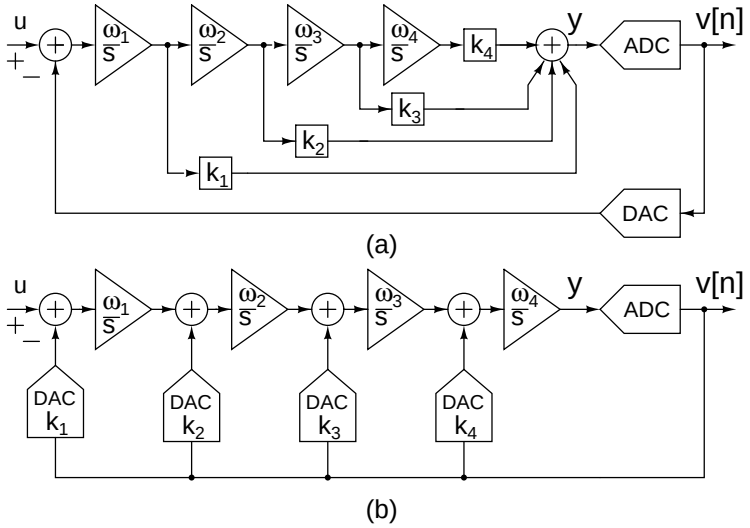


Figure 4.1: Lowpass fourth order CTDSM (a) CIFF and (b) CIFB topology [4]

CIFB loop filter would need four such DACs compared to a single DAC in case of CIFF. Hence, using a CIFF loop-filter results in a smaller area. Also due to multiple feedback in the CIFB, load on the quantizer is higher. This increases the power dissipation of quantizer [4].

4.2 Active-RC vs G_m-C integrators [4]

The basic circuit blocks in a CT loop-filter are the CT integrators. Many kinds of CT integrators are available but the most commonly used ones are active-RC integrators and G_m-C integrators (see Fig. 4.1). The comparison between active-RC integrators and G_m-C is as follows:

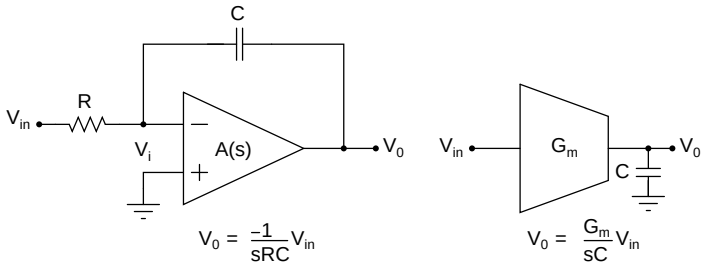


Figure 4.2: a) Active-RC and (b) G_m-C integrators [4]

- Active-RC integrators are closed loop applications of the opamps, whereas G_m-C integrators have transconductors in open loop.
- Because of this, active-RC integrators have high linearity, which allows a larger signal swing.
- G_m-C integrators can work at higher speeds than active-RC integrators due to their open-loop architecture.
- In a loop filter with active-RC integrators, the virtual ground termination provided by the first opamp will also greatly improve the linearity of the feedback DAC whose outputs are connected to the inputs of the opamp.

Because of the above reasons, active-RC integrators are used in CT $\Delta\Sigma$ modulator in [4].

4.3 Discrete-time (DT) loop filter and its continuous-time (CT) equivalent

4.3.1 Discrete-time loop filter

A fourth order modulator with optimized zeros and an OSR of 25 is used for the current design. The NTF that is to be realized is derived from the $\Delta\Sigma$ Toolbox in MATLAB and is given by:

$$NTF_{ideal}(z) = \frac{(z^2 - 1.998z + 1)(z^2 - 1.988z + 1)}{(z^2 - 1.204z + 0.3771)(z^2 - 1.43z + 0.6585)} \tag{4.1}$$

From the NTF_{ideal} , the loop filter response $L_{ideal}(z)$ can be determined by:

$$L_{ideal}(z) = \frac{1 - NTF_{ideal}(z)}{NTF_{ideal}(z)} \tag{4.2}$$

With the ELD compensation technique described in the previous chapter the NTF realized will be [5]:

$$NTF(z) = (1 + az^{-1})NTF_{ideal}(z) \tag{4.3}$$

The modulator with the NTF given in Eq. 4.3, was simulated in MATLAB. The peak SNR obtained is 96 dB.

4.3.2 Continuous-time loop filter realization

If we want to realize the above discrete-time loop filter response in a CT modulator with an NRZ DAC, the sampled value of the pulse response of the CT loop filter should be the same as the impulse response of the DT loop filter. In our case, since the second

sample of the NTF is obtained from the parallel path, the sampled response at the output of the CT loop filter must corresponds to :

$$L(z) = L_{ideal}(z) - az^{-1} \tag{4.4}$$

response at the output of the CT loop filter must corresponds to : The two systems

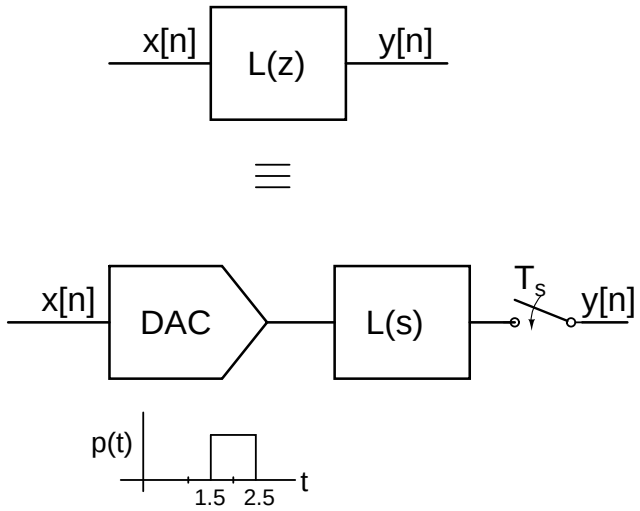


Figure 4.3: Equivalence of CT and DT loop filters [4]

shown in Fig. 4.3 are identical if:

$$Z^{-1}L(z) = L^{-1}(P(s)L(s))|_{t=nT_s} \tag{4.5}$$

where P (s) represents the pulse response of the DAC. This transformation of the DT response to the CT response is called as the impulse invariance transform. Using MATLAB, for a CT modulator with an NRZ DAC, one can drive the CT loop filter response including ELD compensation as:

$$H(s) = \frac{0.9695(s + 1.758)(s + 0.2436)(s^2 + 0.2311s + 0.095)}{(s^2 + 0.001823)(s^2 + 0.01171)} \tag{4.6}$$

This forms the prototype CT loop filter for our design. The prototype loop filter response in Eq. 4.6 when driven by an NRZ DAC with a delay (ELD) of 1.5 clock cycles sampled at the output, corresponds to Eq. 4.4. A fourth order CT loop filter in CIFF architecture can be realized using a cascade of four integrators. The optimization zeros

of the NTF are realized using the feedback factors β_1 and β_2. Direct path is added from the modulator input to the loop filter output to reduce the swing at the output of third and fourth integrators [4]. We use a sampling frequency f_s of 800 MHz. So, we have to frequency scale our prototype loop filter by replacing s by s/f_s in Eq. 4.6. In other words, H(s/f_s) gives the loop filter response to be operated at a sampling rate of f_s. Nodes are scaled such that that all nodes have a peak-to-peak differential swing of approximately 700 mV_{ppd} , except for the summing amplifier which has a peak-to-peak differential swing of 3 V_{ppd} . Node scaling ensures that the outputs of the opamps do not saturate for input voltages within the quantizer range.

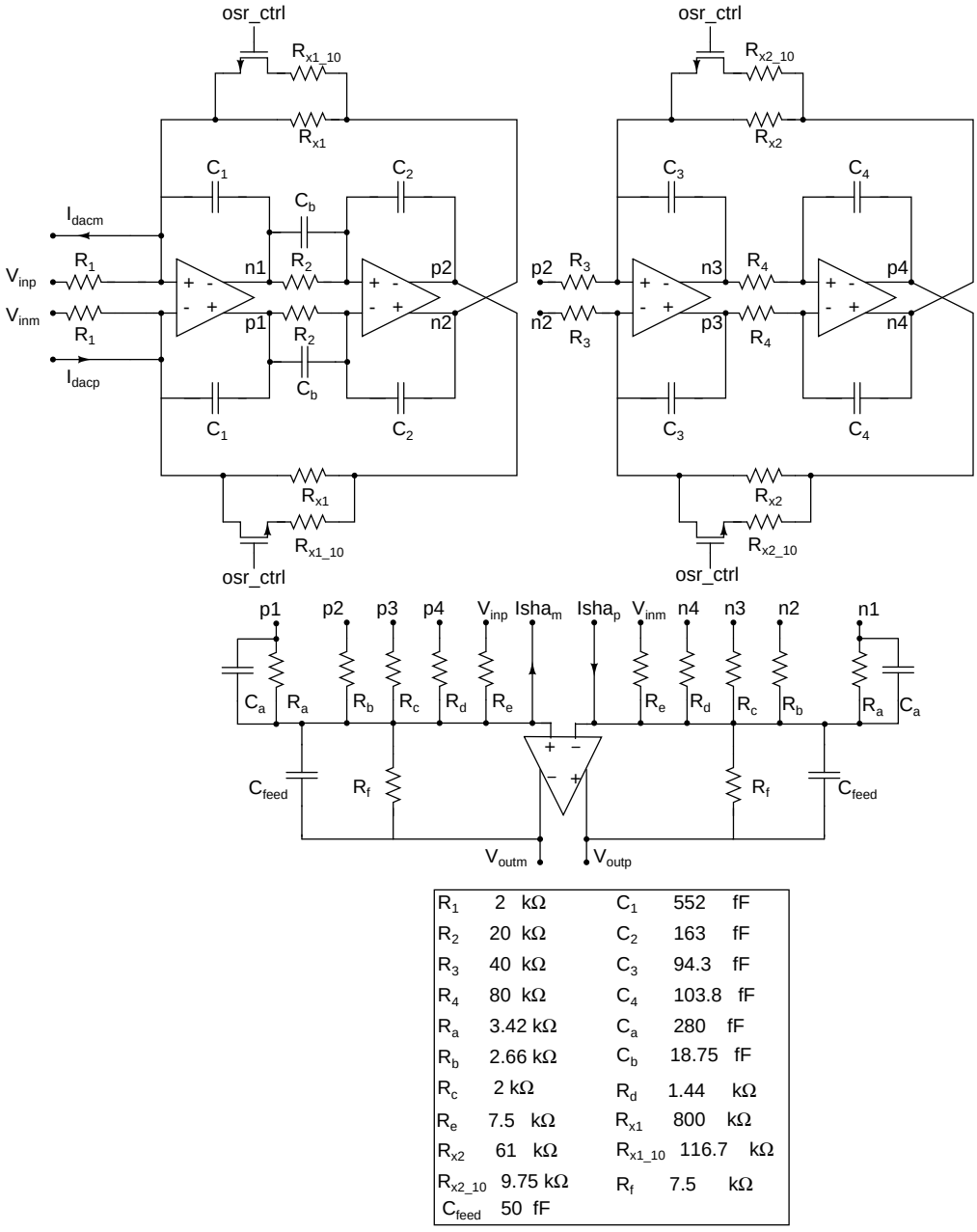
4.3.3 Loop filter component specifications

The loop-filter is a fourth order filter implemented using active-RC integrators shown in Fig. 4.4. The loop-filter is a cascade of integrators with feedforward summation. The output current of the DAC, $I_{dacp,n}$ feeds the input of the first integrator. The NTF determines the integrator time constants (RC). The factors which determine the absolute values of R and C are:

- input referred noise of the system
- node voltage swings

The input resistor R_1 is the major contributor to the input referred noise. Therefore, noise specifications determine R_1. The noise from the succeeding integrators is negligible because while referring back to the input, the noise from the later stages will be divided by the preceding integrator gain. Therefore their impedance levels are increased to minimize power dissipation. The parasitic capacitance limit the extent to which impedance level can be increased [4]. R or C values in individual stages are then adjusted for node scaling while preserving the transfer function.

The resistors and capacitors have process variations and the RC product varies by around 70% over the corners. This variation was overcome by having a four bit capacitor banks. Appropriate capacitor values are selected depending on the corner. The



R_1	2 kΩ	C_1	552 fF
R_2	20 kΩ	C_2	163 fF
R_3	40 kΩ	C_3	94.3 fF
R_4	80 kΩ	C_4	103.8 fF
R_a	3.42 kΩ	C_a	280 fF
R_b	2.66 kΩ	C_b	18.75 fF
R_c	2 kΩ	R_d	1.44 kΩ
R_e	7.5 kΩ	R_{x1}	800 kΩ
R_{x2}	61 kΩ	R_{x1_10}	116.7 kΩ
R_{x2_10}	9.75 kΩ	R_f	7.5 kΩ
C_{feed}	50 fF		

Figure 4.4: Loop Filter Block Diagram [4]

bank of capacitors reduces the maximum RC variation to around 7%.

By increasing the frequency of the optimized zeros, $\Delta\Sigma$ modulator can be operated with a higher bandwidth (lower OSR). The osr_{ctrl} signal in Fig. 4.4 controls the OSR of the modulator by increasing the frequency of optimized zeros by placing resistors $R_{x110,210}$ in parallel with $R_{x1,2}$.

- If osr-ctrl = 0, then OSR =25
- If osr-ctrl = 1, then OSR =10

The feed-in-capacitor C_a in Fig. 4.4 is used to provide a direct path k_0 across the

loop filter. k_0 is given by $R_f C_a$ /$R_1 C_1$ (with ideal opamps). C_b is used to bypass the delay introduced by the feedback capacitor C_{feed} at higher frequency.

A direct path is added from the modulator input to the loop filter output through R_e. The benefit of using the direct path is the reduction in the swing at the output of the third and the fourth integrators, which in turn helps in improving the feedback factor of the summing amplifier. The direct path does not compromise the antialiasing property. The degradation in the alias rejection around f_s is given by [4]:

$$\frac{L_{00}}{L_0} = \frac{2\pi C_1 R_1 R_a}{R_e} \tag{4.7}$$

Where, L_{00} and L_0 denote the transfer function from the DSM input to the quantizer input for no direct path and with direct path respectively (from $V_{inp,m}$ to $V_{outp,m}$ in Fig. 4.5).

4.3.4 First Opamp

The first opamp is the most critical opamp in the design of the loop-filter. The noise of the first opamp reflects directly at the input. The first opamp also the contributes to the distortion. A two stage opamp is required to provide the desired gain while driving the resistive load.

Two stage Miller compensated architectures provide high DC gain and high output swings. But the drawback is that they require a large amount of power for getting a particular bandwidth. Instead, one can use feedforward compensated architectures which give the same bandwidth at much lower power but at the cost of output swing. Since we can scale down the output swings such that the opamps do not saturate, while preserving the loop-filter transfer function, feedforward architecture was the choice for this design.

Because of the multibit quantizer used in this design, the maximum current that has to be provided by this opamp at any time is 1/(num of level) times less than that in a single bit architecture. So opamp slewing and distortion requirements are relaxed in a multibit architecture compared to a single bit CT $\Delta\Sigma$ modulator [4].

4.3.5 Feedforward Compensated Op-Amp

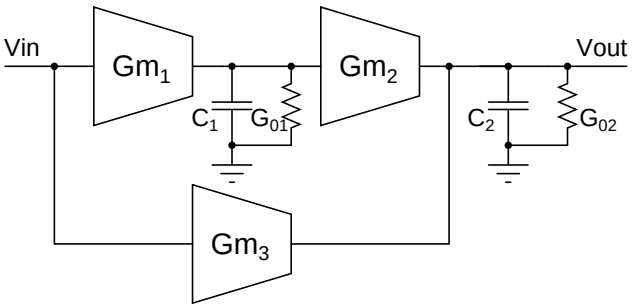


Figure 4.5: Feedforward Architecture [4]

Figure 4.5 shows the block diagram of a feedforward compensated opamp. We can write the transfer function of the opamp as:

$$H(s) = \frac{Gm_1Gm_2 + Gm_3G_{o1} + sC_1Gm_3}{(sC_1 + G_{o1})(sC_2 + G_{o2}))} \tag{4.8}$$

The transfer function has two poles and a zero. The DC Gain of the opamp is:

$$A_{DC} = \frac{Gm_1Gm_2 + Gm_3G_{o1}}{G_{o1}G_{o2}} \tag{4.9}$$

If the zero is at a much lower frequency than the Unity Gain Frequency (UGF) of the opamp, then we get a first order (20 dB/dec) roll off at the UGF. We also get the high DC gain of a two stage opamp.

Fig. 4.6 shows the circuit diagram of the opamp used in the first integrator. The main contributor to the total noise is the first stage of the opamp. Flicker noise is not a serious issue in this design because the bandwidth of interest is assumed to be 1MHz to 16 MHz [4]. Yet, to reduce the flicker noise, the nMOS load transistors in first stage are chosen to have a length of 1 μm. The total input referred thermal noise voltage spectral density of the opamp can be roughly written as:

$$S_n(f) = \frac{16kT}{3Gm_p}[1 + \frac{Gm_n}{Gm_p}] \tag{4.10}$$

where Gm_p and Gm_n are the transconductances of the transistors $\text{M}_{p1,2}$ and $\text{M}_{n1,2}$ respectively. Thus, to reduce the input referred noise, we need to have a large Gm_p

and a small Gm_n. The second stage is designed such that it carries enough current to achieve the desired bandwidth. It should have enough current to supply the integrating capacitor, and the load resistors (the input resistor of second integrator, the input resistor of the summing amplifier used to realize the coefficient k_1, and the common mode sensing resistor). Transistors $M_{n7,8}$ are a scaled version of $M_{n5,6}$, used in the first stage common mode feedback circuit. $M_{p6,7}$ form the feedforward stage (Gm_3 in Fig.4.5)

4.3.6 CMFB Circuit

The feedforward opamp has two stages of common mode feedback. The first stage CMFB loop consists of the transistors M_{p3}, $M_{n5,6}$, $M_{p4,5}$ and $M_{p1,2}$. If the common mode level of vom1 and vop1 increases, the currents in $M_{n5,6}$ will increase which in turn will increase the current in M_{p3}. Since the total tail current is constant, this will result in an decrease in the currents in $M_{p1,2}$, thus bringing down the common mode output level of the first stage.

The second stage CMFB has the common mode sensing resistors R_{cm} and the feedback loop ensures that the dc common mode level is fixed to Vcmref. Since the CMFB loop has two stages, we need to compensate it by adding a miller capacitance C_{comp1} to stabilize the loop.

Table 4.1: Performance summary of the first opamp in the loop-filter

DC Gain	79 dB
Unity-gain Frequency	2.28 GHz
Phase Margin	65.8°
Input reffered noise	25 μV_{rms}
Power (1.8V)	6.21 mW

Figure 4.6: First Opamp

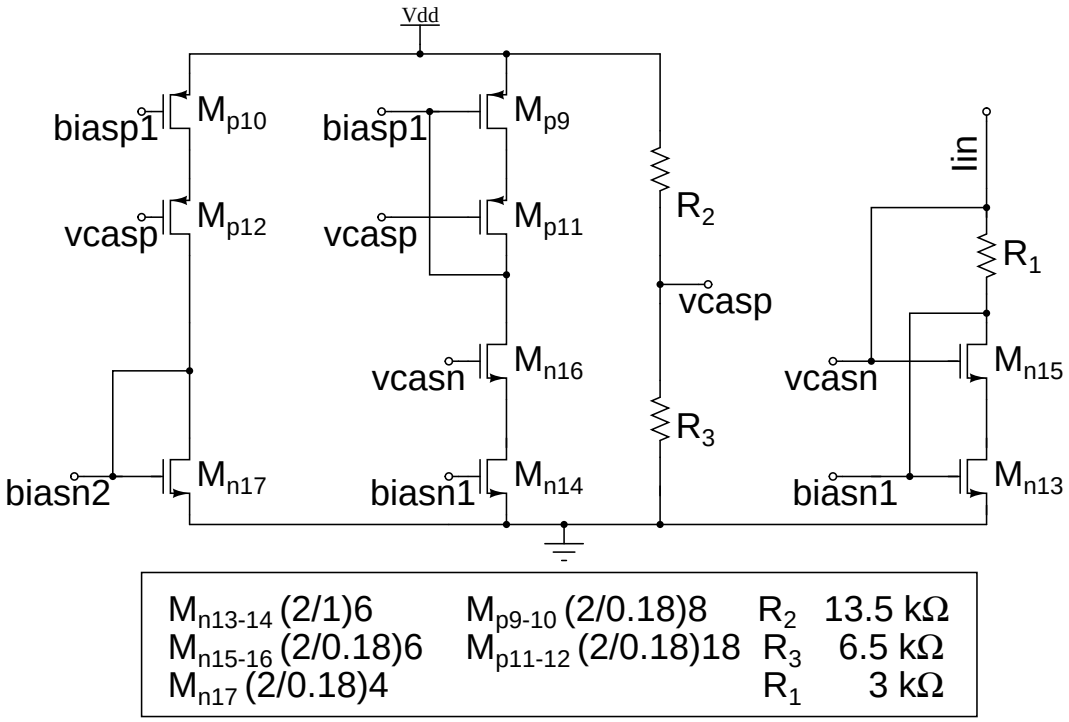


Figure 4.7: First Opamp Bias Circuit

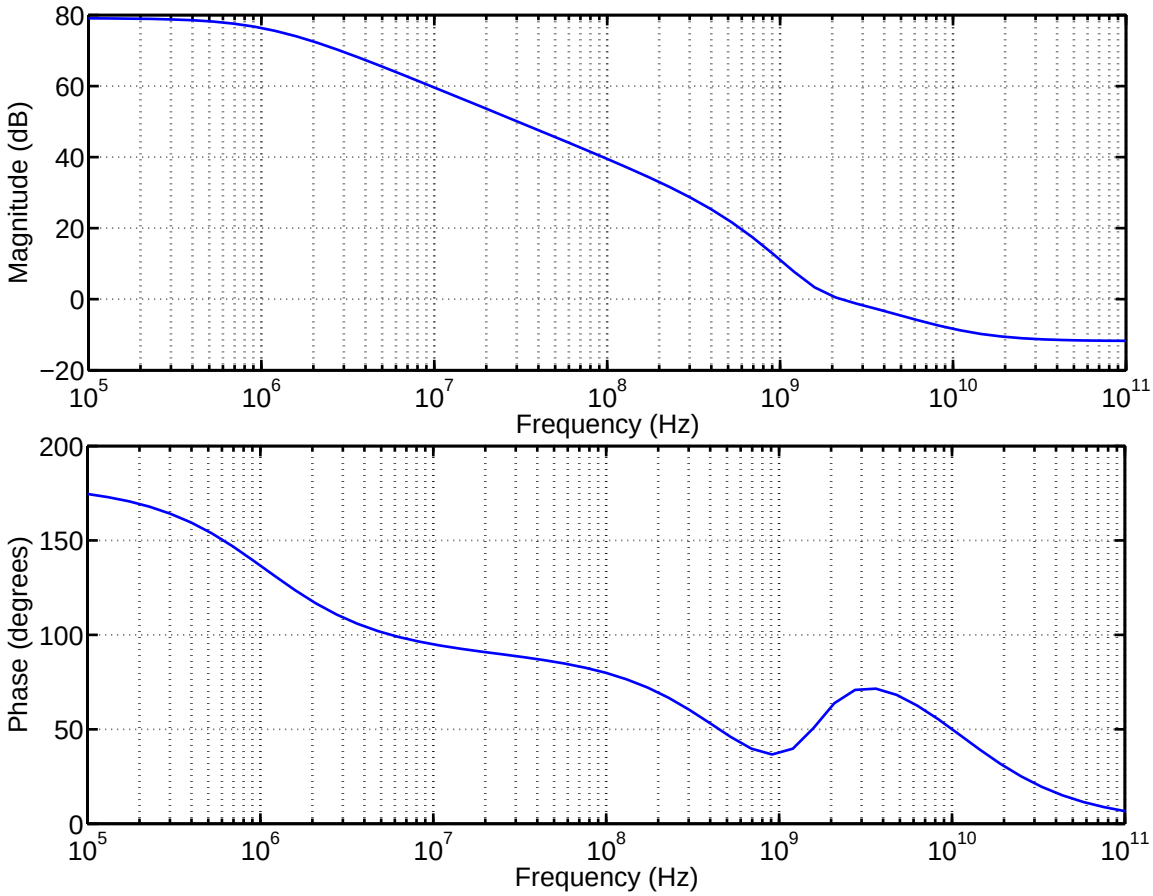


Figure 4.8: Magnitude and Phase response of the First Opamp

4.4 Other Integrating Opamps

The noise and nonlinearities of other opamps get divided by the gain of their respective preceding stages. So the other integrating opamps have relaxed constraints on DC gain, input referred noise, unity gain frequency and slew rate specifications. The only constraint is that the opamp has to supply enough current for its loads [4]. The current consumed by these opamps is less as the nonlinearity and bandwidth constraints are relaxed. Note that opamp1 needs to be fastest among all the four opamps used in the integrators, as it forms the fastest path (through k_1) of the loop filter. The other integrating opamps are just the scaled version of the first opamp.

4.5 Summing Opamp

The summing opamp has a huge capacitive load due to the 4-bit flash ADC. Also the feedback factor of the summing opamp is very small, as all the resistors realizing the feedforward coefficients of the loop filter are connected in parallel at its virtual ground node. Hence, the summing opamp has to satisfy very tight specifications on the UGF (to reduce delay), and the output swing. The bandwidth of the summing amplifier has to be greater than f_s to ensure that the pulse response of the summing amplifier settles within one clock period. The swing at the output of the opamp is $3\,V_{peak-peak,d}$. So the headroom for the output stage is only $300\,mV_{peak-peak}$. So we cannot use the feedforward architecture that was used for the integrating opamps. Another option is to use the miller compensated two stage opamp. The miller opamp solves the swing problem, but it takes a lot of power to get the desired UGF. With this motivation an architecture that combines the feedforward compensation which realizes a higher UGF for a given power consumption and a common source amplifier second stage which provides a high output swing is used in [4].

The swing limitation of the feedforward opamp architecture in Fig. 4.4 is due to the presence of Gm3 directly between the input and output nodes. Gm_3 has to be a differential pair with a tail current source in order for the opamp to have commonmode

(CM) rejection. Therefore the only option to obtain large output swing is to split the feedforward stage into two stages as shown in Fig. 4.9. Gm'$_3$ is a differential pair with high CM rejection and Gm$_3$ is a common source amplifier with high output swing. It has to be ensure that the pole at the output of Gm'$_3$ is at a sufficiently high frequency.

The transfer function is given by [4]:

$$H(s) = \frac{\frac{Gm_1G_2}{Go_1Go_2}(1+\frac{sC_3}{Go_3}) + \frac{Gm_2Gm'_3}{Go_2Go_3}(1+\frac{sCo_1}{Go_1})}{(1+\frac{sC_1}{Go_1})(1+\frac{sC_2}{Go_2})(1+\frac{sC_3}{Go_3})} \tag{4.11}$$

G0$_3$ is equal to Gm'$_3$/5, to get a gain of five from this stage. Gm'$_3$ is chosen large enough such that the non-dominant pole Go$_3$/C$_3$ is much higher than the closed loop unity gain frequency. So then for all the frequencies less than f$_s$ the feed forward path can be approximated to a first order path. So, we can neglect the this pole and Eq. 4.10 can be modified as below:

$$H(s) = \frac{\frac{Gm_1G_2}{Go_1Go_2} + \frac{Gm_2Gm'_3}{Go_2Go_3}(1+\frac{sCo_1}{Go_1})}{(1+\frac{sC_1}{Go_1})(1+\frac{sC_2}{Go_2})} \tag{4.12}$$

This opamp has 2 poles and zero. Recalling that the zero in the standard feedforward architecture is at -Gm$_1$Gm$_2$/C$_1$Gm$_3$. The zero has been brought to a lower frequency. Which can be assumed as the effective feedforward Gm is increased by as factor Gm'$_3$/Go$_3$. So now, the open loop unity gain frequency is Gm$_3$Gm'$_3$/C$_2$Go$_3$.

Circuit details of this feedforward opamp is shown in Fig. 4.9 and Fig. 4.10. In the conventional feedforward opamp, output swing is limited by the threshold voltage of nMOS because the input and the output of the opamp have the same common mode voltage. But in this architecture, the second stage input common mode voltage is independent of the output common mode voltage. For a higher output swing the output stage has to be a common source amplifier with its input biased at one V$_{gs}$ above the ground. For this, Gm'$_3$ is ac coupled to Gm$_3$ through the capacitor C$_b$. Gm'$_3$ is implemented with the nMOS input pair and diode connected nMOS loads to have a gain of β = 5. An nMOS load is used instead of a pMOS load to have smaller parasitics. CMFB

of second stage is provided by sensing the common mode voltage through Rcm and feeding back the current through Mp11,12. CMFB through current feedback eliminates the tail current transistors in the second stage, and results in a larger swing.

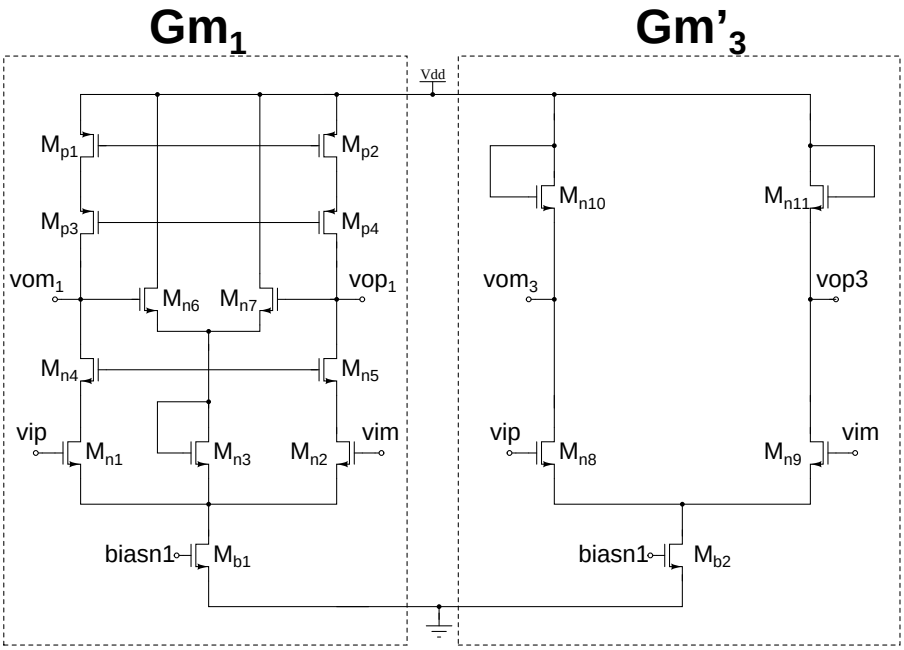
A feedback capacitor C_{feed} of 50 fF is added parallel to the feedback resistance of the summing opamp as shown in the Fig.4.4. This zero helps in cancellation of the pole created due to gate capacitance of the summing opamp and increase the phase margin of the loop.

As shown in Fig.4.4 capacitance C_b is added parallel to resistance R_2 to introduce a zero and cancel the effect of the pole due to C_{feed} and R_f for the paths from 2^{nd}, 3^{rd} and 4^{th} integrators. The value of capacitor C_a is increased to cancel the effect of the pole in first integrator path.

Table 4.2 summarizes the summing opamp characteristics.

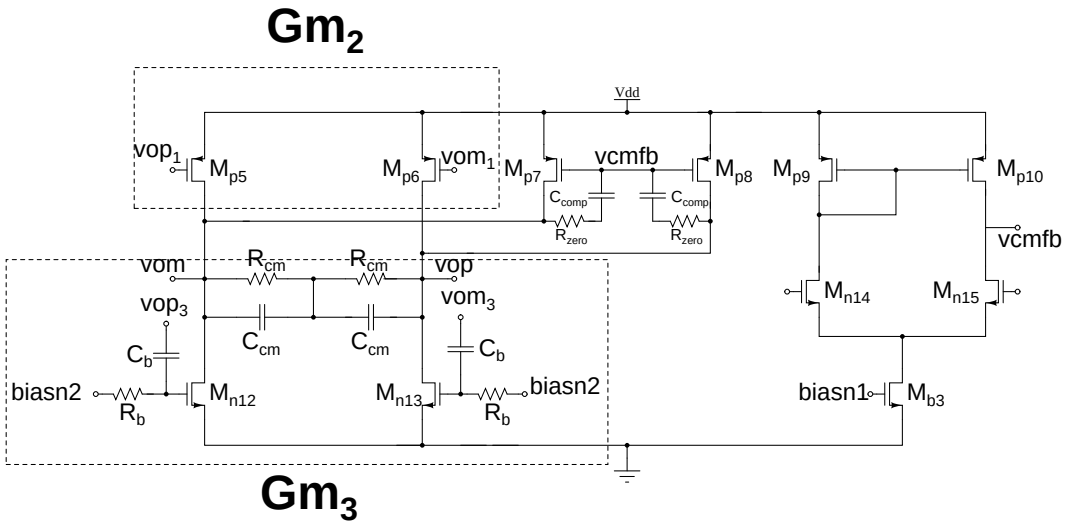
Table 4.2: Performance summary of the first opamp in the loop-filter

DC Gain	61 dB
Unity-gain Frequency	3.6 GHz
Phase Margin	56°
Power (1.8V)	10.62 mW



M_{n1-5} (2/0.18)10	M_{n10-11} (2/0.18)4	M_{b2} (2/0.18)40
M_{n6-7} (2/0.18)2	M_{p1-4} (2/0.18)16	
M_{n8-9} (2/0.18)40	M_{b1} (2/0.18)24	

Figure 4.9: Summing Opamp [4]



M_{n12-13} (2/0.18)60	M_{p7-8} (2/0.18)12	R_b 1 MΩ	C_b 200 fF
M_{n14-15} (2/0.18)2	M_{p9-10} (2/0.18)1	R_{zero} 500 Ω	C_{zero} 125 fF
M_{p5-6} (2/0.18)20	R_{cm} 50 kΩ	C_{cm} 30 fF	

Figure 4.10: Summing Opamp [4]

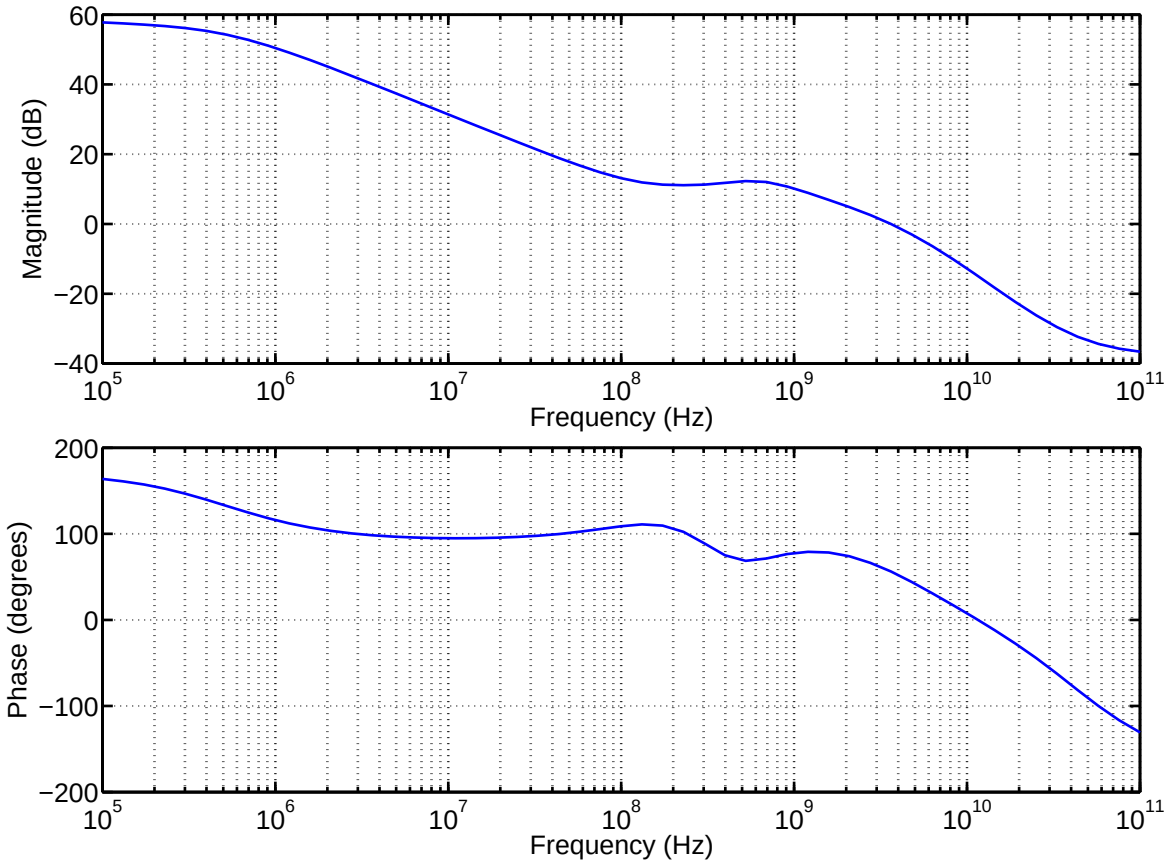


Figure 4.11: Magnitude and Phase response of the Summing Opamp

CHAPTER 5

High speed parallel feedback path components

5.1 Architecture

We have seen in Chapter 3 that a fast loop excluding the quantizer is required to compensate for quantizer delay of more than one clock cycle. Fig.5.1 (a) shows the block diagram of this fast loop, were a zero-order hold is cascaded with the gain stage. The gain coefficient a is the magnitude of the second sample of the NTF impulse response. The zero-order hold is realized using a S/H as shown in Fig.5.1(b). The gain stage is realized using a Gm cell whose output is connected to the virtual node of the summing opamp as shown in Fig.5.1(c) [4]. Transconductance of the Gm cell has to be a/R, for realizing the second sample of value a. In the following sections, we will discuss the circuit level details of the S/H and the Gm cell.

5.2 Sample Hold

An open-loop architecture was chosen because of its ability to operate at higher speeds. The simplest open-loop S/H is constructed from an nMOS switch and holding capacitor. The nonlinearity of the S/H does not contribute to the ADC nonlinearity because of the high gain of the preceding loop filter.

Fig. 5.2 shows one half of the pseudo differential S/H circuit. The S/H is formed using a cascade of two track and hold stages operated by alternate clock phases ϕ and $\phi 1$. Source followers formed using transistors M1 and M2 act as input buffer for the two track and hold stages.

A capacitive attenuator with C_1 and $C_2$is used at the input to reduce the signal swing (C_1 /(C_1 +C_2)) requirement of the buffers. The reduction in the input signal swing is

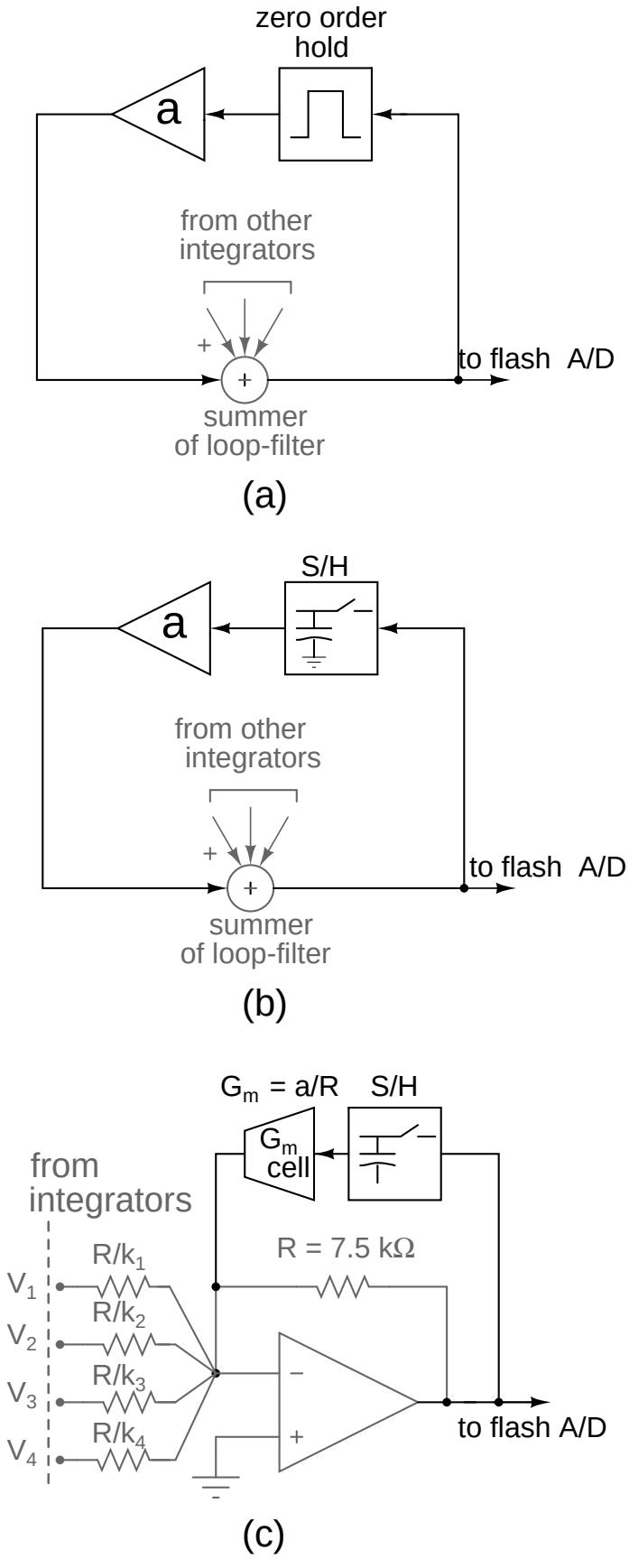


Figure 5.1: (a) Fast loop ELD compensation (see Fig. 3.16) (b) S/H as zero-order hold. (c) Gm cell as gain stage. (Single ended equivalent) [4]

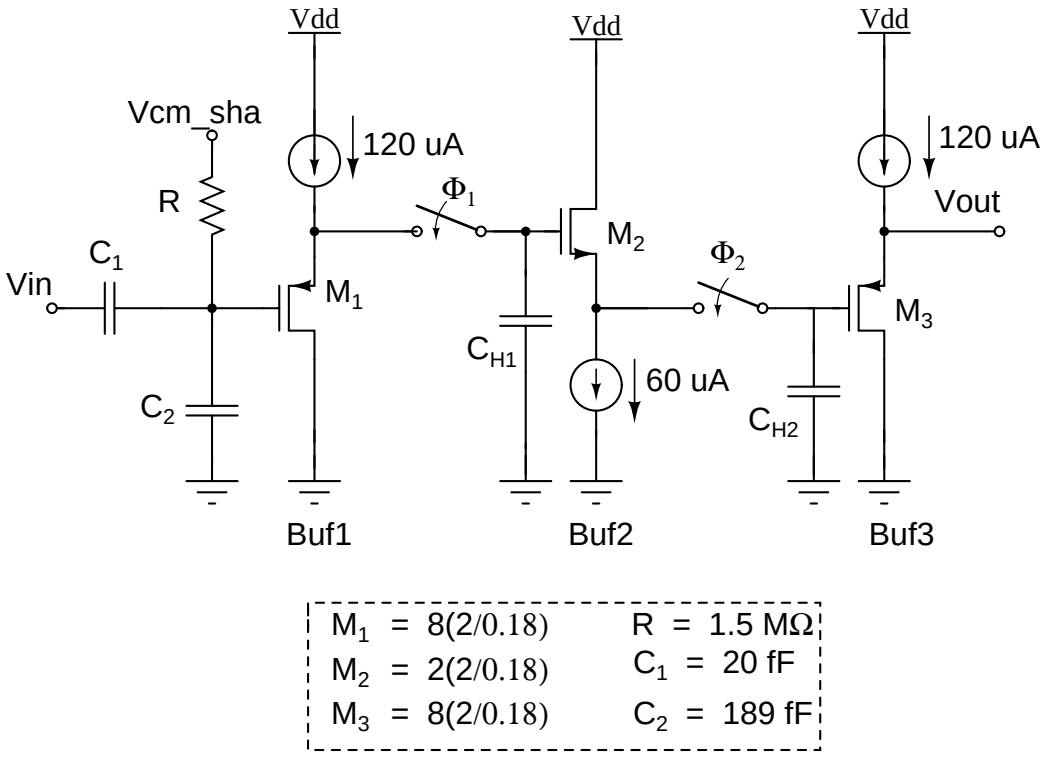


Figure 5.2: S/H circuit (One half of the pseudo differential structure)

compensated by providing a correspondingly higher gain in the Gm cell. A source follower M3 serves as the output buffer to drive the Gm cell. The parasitic capacitances at the gates of M2 and M3 are sufficiently large and therefore, C_{H1} and C_{H2} are not explicitly realized. Resistor R is used to provide the DC bias point to the gate of M1 . The voltage $V_{cm,sha}$ is derived from the constant g_m bias circuit (discussed in later section). The output of the attenuator is buffered by source follower M1 before being fed into the first sampler having C_{H1}. The input buffer is needed so that the previous stage sees a constant load. The source follower M_1 isolates the input from switching activity of the sampler. $M_{1,3}$ have their body and source terminals are tied together to avoid distortion and attenuation due to body effect.

In order to reduce nonlinearity, the sampling switch is implemented as a constant gate-overdrive switch as shown in Fig. 5.3. Here the capacitor C_3 is charged to the voltage Vdd during the hold phase (ϕ_1 being high). During the track phase (ϕ_1 being high), the bottom plate of C_3 is connected to the input signal whereas the top plate is connected to the gate of M1 through M4 . Thus the gate-to-source voltage of M1 during tracking mode is constant.

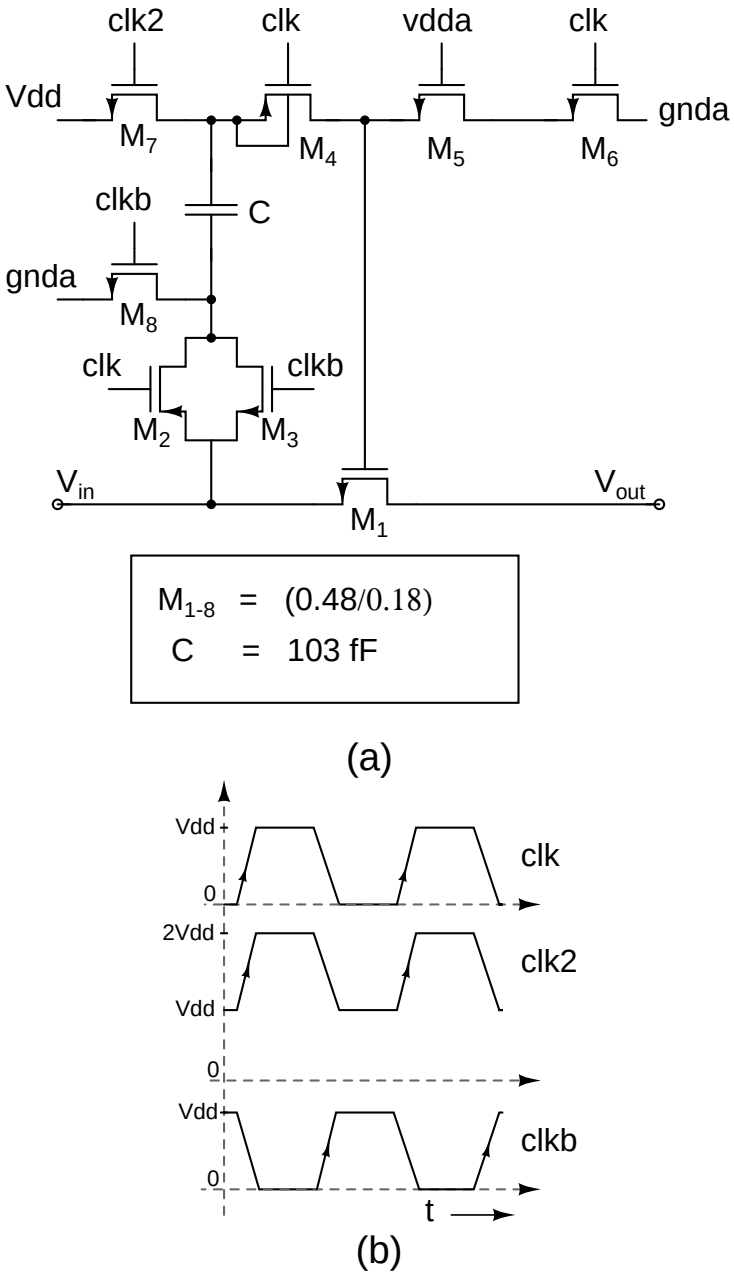


Figure 5.3: (a) Bootstrapped switch. (b) Clock waveforms for the bootstrapped switch [4]

A charge pump is used to generate 2Vdd and Vdd for ϕ_2 . Fig. 5.4 shows the schematic of the charge pump. When the ϕ_1 is high, bottom plate of C_4 is connected to gnda, through M1 and top plate is charged to Vdd through M5 , which is acting as current source. When ϕ_1 goes low, the bottom plate of C_4 sees a jump of Vdd and hence top plate of C_4 also jumps by Vdd to 2Vdd. So ϕ_2 toggles between 2Vdd and Vdd following the ϕ_1 signal [4].

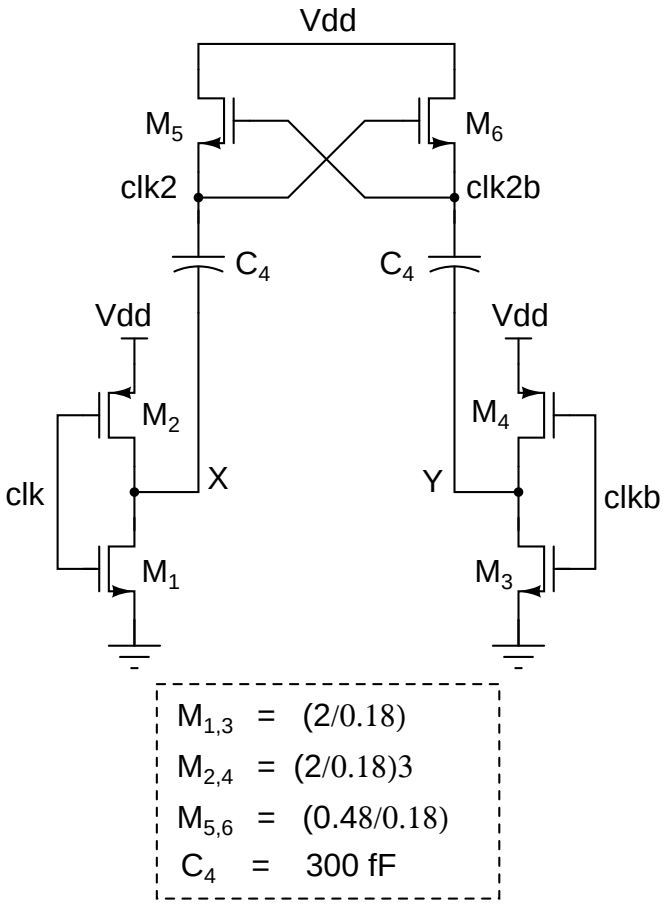


Figure 5.4: Charge pump to generate clock with levels 2Vdd and Vdd [4]

5.3 G_m cell

The circuit schematic of the Gm cell used after the S/H is shown Fig. 5.5. The output of the S/H is ac coupled to its input through the capacitor C. To realize the coefficient a, the transconductance Gm has to be:

$$Gm = \frac{a}{R_f}\frac{C_1 + C_2}{C_1} \tag{5.1}$$

where a is the second sample of the ideal NTF impuse response. R_f is the feedback resistor around the summing opamp used in the loop filter. The output of this Gm cell is fed back to the virtual node of the summing opamp to from the fast loop of the modulator.

The Gm cell is biased using a fixed Gm , so that the Gm of transconductor can track 1/R across all process corners and the second sample value remains unchanged across all process corners. The circuit diagram is shown in Fig. 5.6 [7].

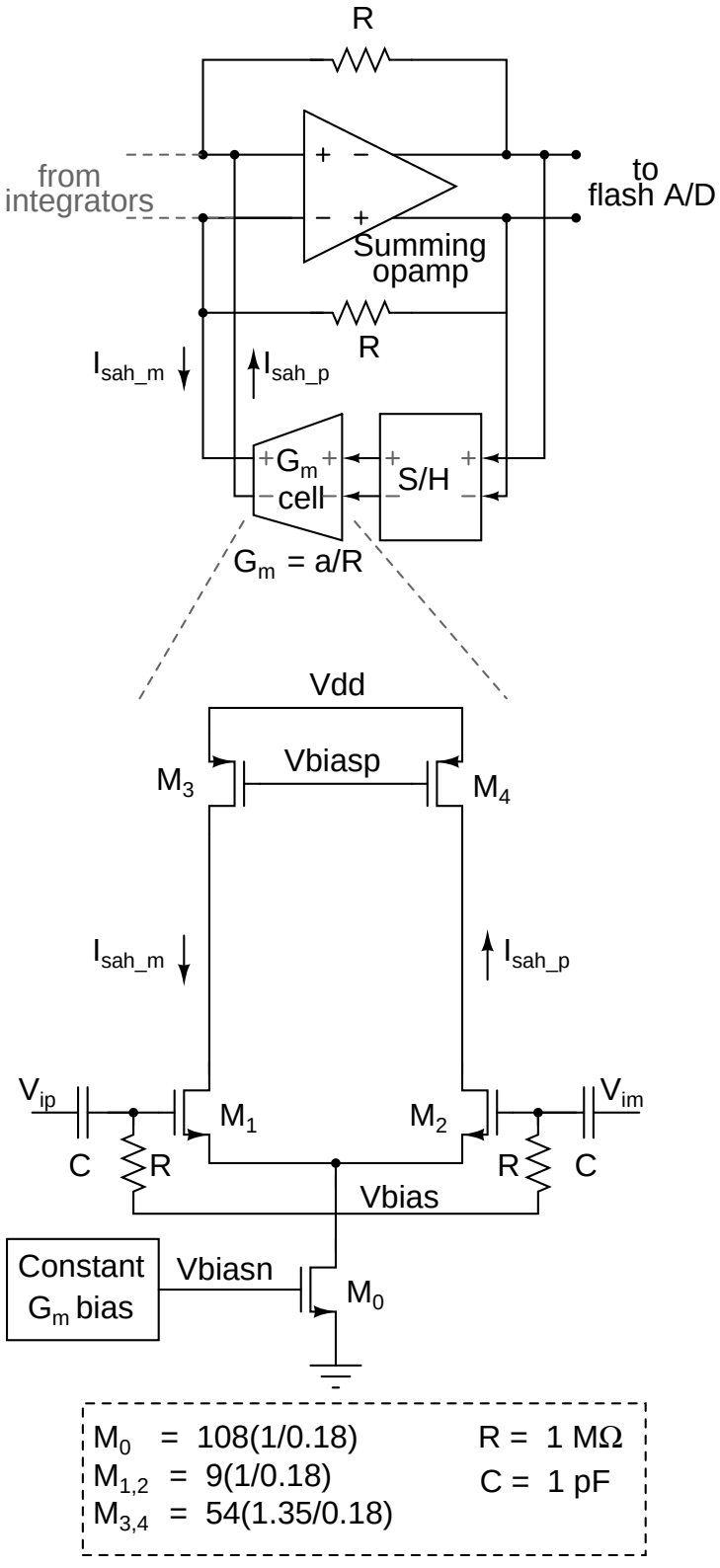


Figure 5.5: G_m cell [4]

The devices whose transconductance needs to be fixed are M1 and M2 . In steady state, the feedback in the circuit ensures that the currents in M9 and M10 are equal.

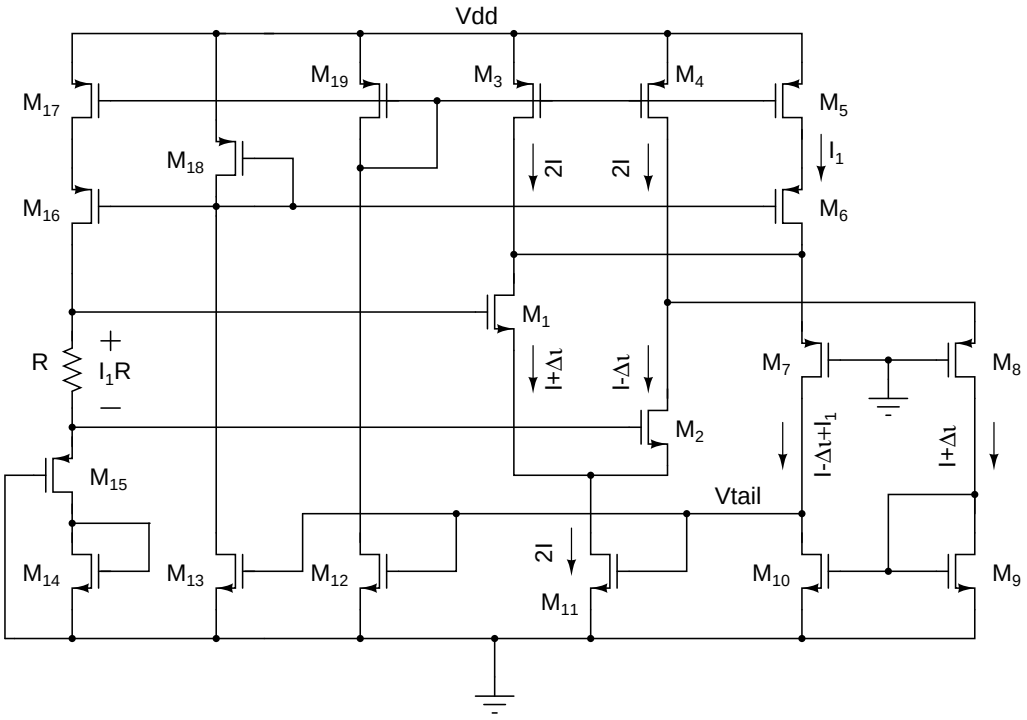


Figure 5.6: Fixed-G$_m$ bias circuit [7]

This gives:

$$I - \Delta I + I_1 = I + \Delta I \tag{5.2}$$

$$2\Delta I = I_1 \tag{5.3}$$

The differential current due to a small incremental voltage I_1R is given by the relation:

$$2\Delta I = Gm_{M_1} I_1 R \tag{5.4}$$

$$Gm_{M_1} = \frac{1}{R} \tag{5.5}$$

The resistance R is the replica of the feedback resistor around the summing opamp of the loop filter. This design is robust in various aspects namely: It is not dependent on the MOSFET square law, It is independent of supply voltage and temperature variations and it is not affected by the output impedance of the transistors and back-gate effect. The design details of the fixed transconductance bias used in this design is shown in Fig. 5.7

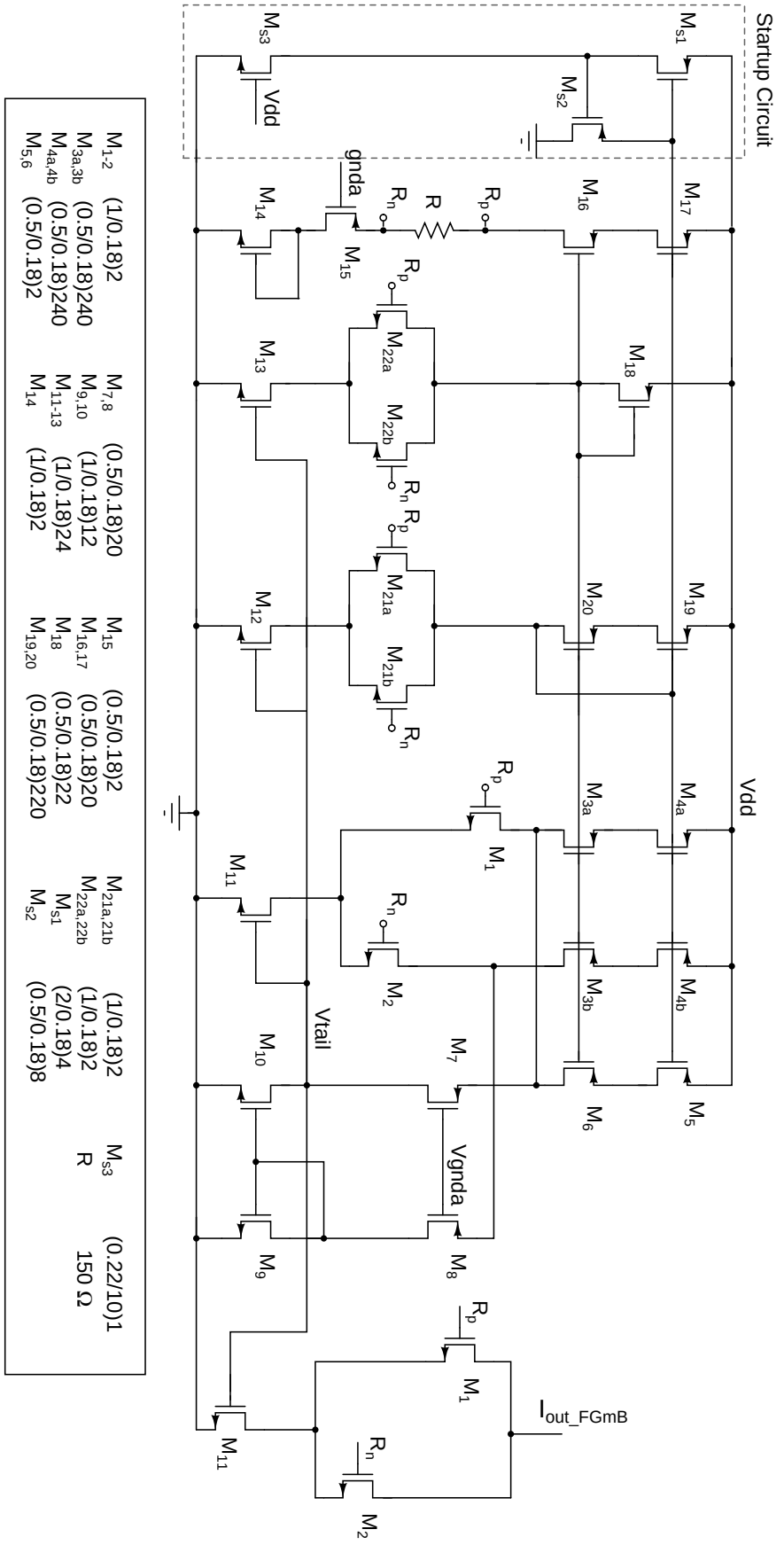


Figure 5.7: Fixed-Gm bias circuit used in this work

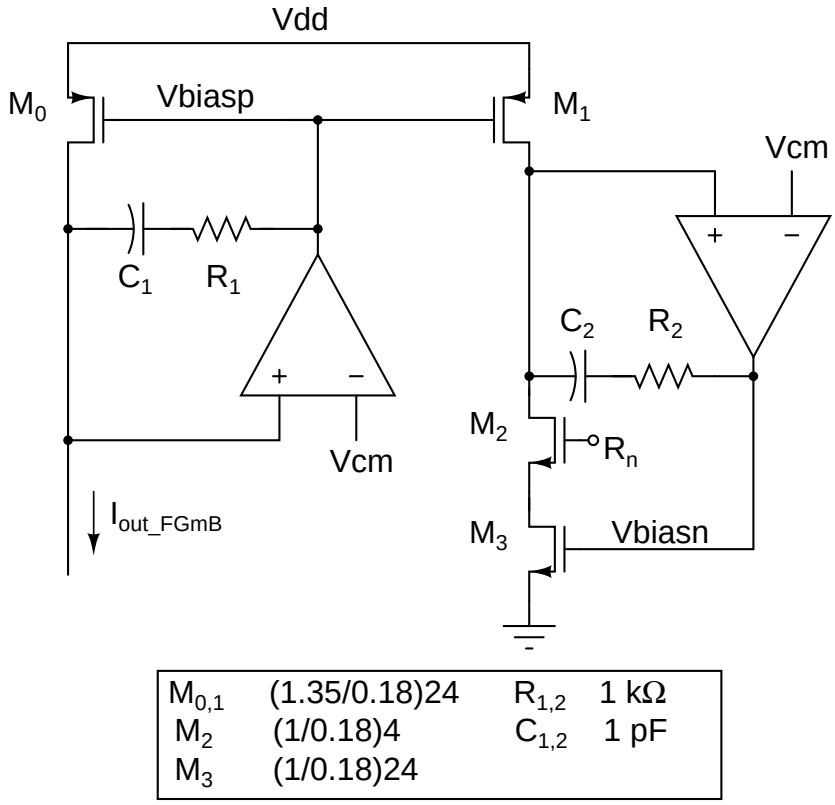


Figure 5.8: Biasing circuit for the G_m cell shown in Fig. 5.5 (The output from Fig. 5.7 is the input to this circuit) [4]

The circuit in Fig. 5.8 accepts the current from the constant Gm bias generator (Fig. 5.7) and provide the bias voltage Vbiasn to the Gm cell in Fig. 5.5. It consists of a pMOS current mirror $M_{0,1}$ followed by an nMOS stack $M_{2,3}$ which are the replicas of $M_{1,2}$ and M_0 respectively in Fig. 5.5. Opamps are used to force equal VDS across transistors in a mirror realize accurate current mirroring [4]. Single stage opamps consisting of a differential pair and a current mirror are used in Fig. 5.8.

CHAPTER 6

Quantizer

6.1 4-bit Flash ADC

6.1.1 Introduction

As discussed in chapter 3, in continuous time delta sigma modulator the delay introduced by the quantizer (ADC, DAC and logic circuit) is a very crucial. So in this design a 4-bit flash ADC was designed to reduce the delay introduced by the quantizer [4]. A n-bit flash ADC the full scale of the ADC is divided into (2^n-1) level and the input is compared with these levels using (2^n-1) comparators. The output of these comparators will be a string of 1's followed by 0's which is also known as thermometric code. According to the necessity this thermometric code will be converted into binary using digital logic. In the schematic the full scale reference levels V_{refp} and V_{refm} are generated using ideal voltage sources in the schematic, the full scale reference level generation circuit has not been designed. The block diagram of the 4-bit flash ADC is shown in the Figure. 6.1.

The references levels for the comparators are generated using a resistive ladder between the full scale voltages.

6.1.2 CML Latch

The drawbacks of using normal CMOS comparators in high frequency operation were discussed in [4]. So CML latch as shown in Figure 6.2 was used in this design. When LC is high, M_2 is ON and M_3 is OFF. The differential gain from input to output is $gm_{M4}R$. So the output of the latch linearly tracks the input as this is called tracking

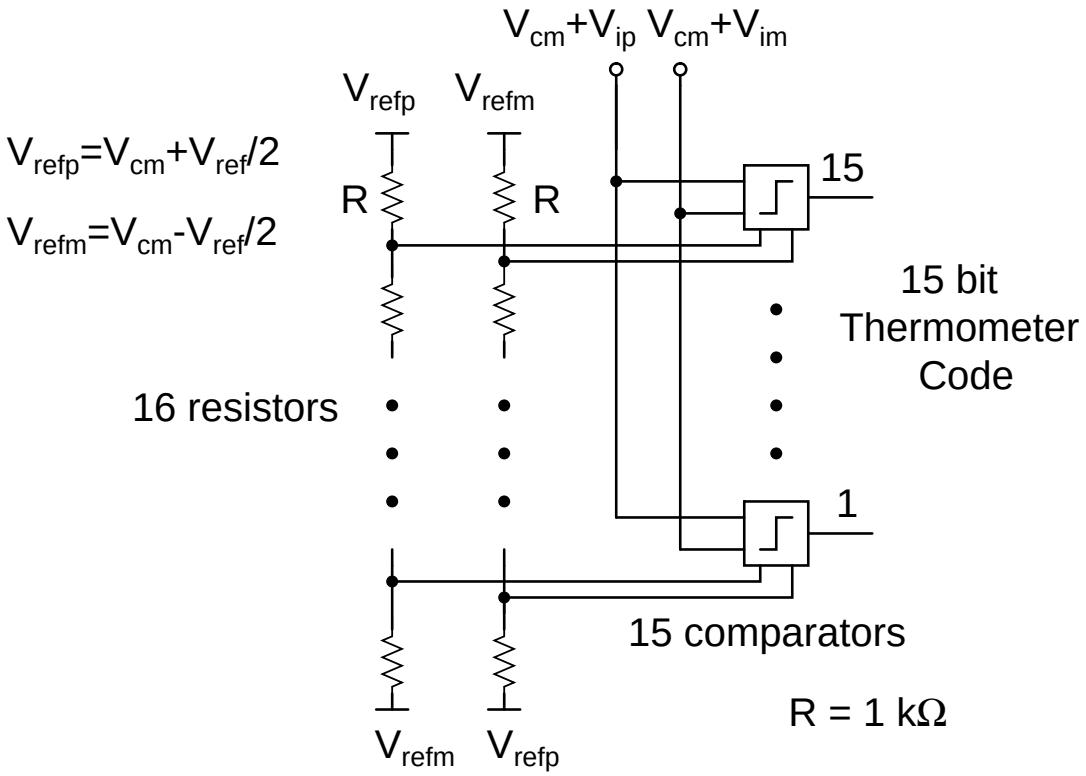


Figure 6.1: Block diagram of 4-bit flash ADC [4]

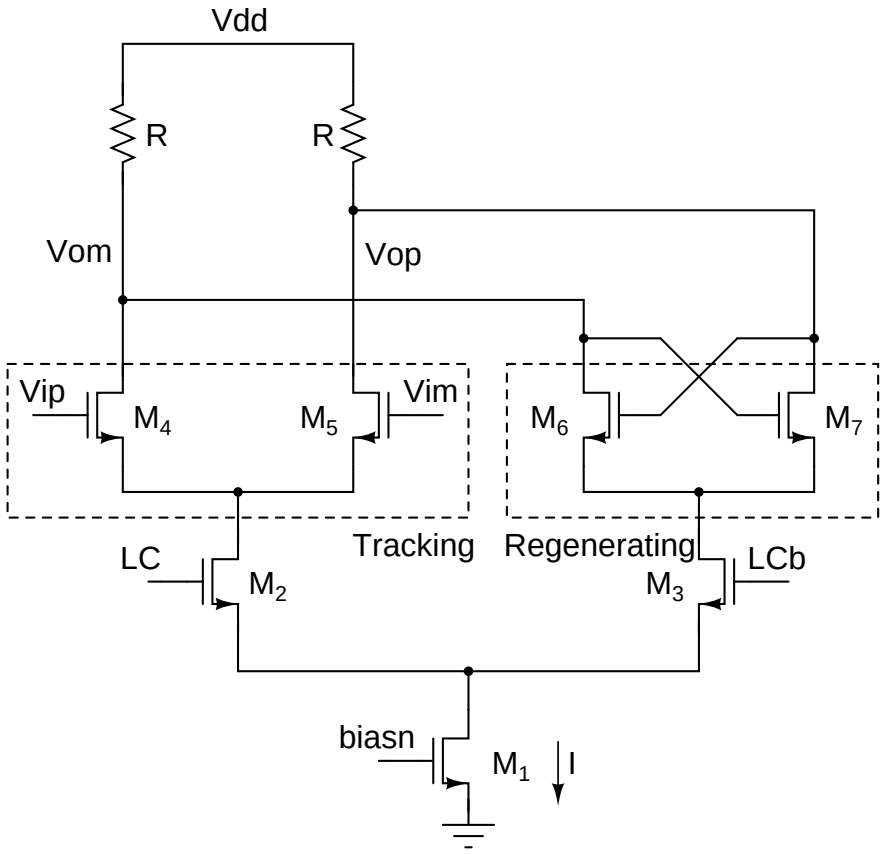


Figure 6.2: CML Latch [4]

phase of the latch. When LC is low, M_2 is turned OFF and the output is latched by the regenerative pair (M_6 and M_7) because of their positive feedback and this phase is called regenerating phase. This regenerative pair continues to provide gain during this phase, the minimum cross-coupled gain to hold the state is $gm_{M6-7}R > 1$. The falling edge of LC is the sampling instant of this CML latch. The common mode gain from input to output during the tracking phase is very less, so this CML is insensitive to common mode noise [4].

6.1.3 Comparator Architecture

Figure 6.3(a) and (b) show the block diagram of the comparator used and the corresponding clock waveforms respectively. The comparator works as follows:

The inputs V_{ip} and V_{im} are connected through two capacitors C_c, which are periodically charged to the voltages (V_{refp} - V_{cm}) and (V_{refm} - V_{cm}) respectively through the capacitors C_b. The two capacitors C_b are charged to (V_{refp} - V_{cm}) and (V_{refm} - V_{cm}) using the single ended references V_{refp}, V_{refm} and V_{cm} when LE is high. LE and LC are non-overlapping clocks and are operating ar frequency of fs/4 to allow a high time for the capacitors to charge, which shows a significant improvement in the performance of the reference subtracter [4]. So the differential input seen by the Latch1 is ((V_{ip} - V_{im}) - (V_{refp} - V_{refm})). The references V_{refp} and V_{refm} are connected to the levels from the resistive ladder.

The input reference subtracter is cascaded with 3 CML latches for providing enough regenerative gain and avoid metastability problem [4]. The latches in the comparator are followed by a buffer to drive the DAC and the digital logic, and to isolate the DAC from the ripples produced from the latch3 during switching. When LCL is high, latch1 will be tracking the input. During this time latch2 will be regenerating the previous sample and latch3 will be tracking the ouput of latch2, as shown in the Figure 6.3(b). The output of the latch1 is reset at the end of its regenerative phase, so that the input will be tracked from the start of the next track phase. The regenerative output of latch1

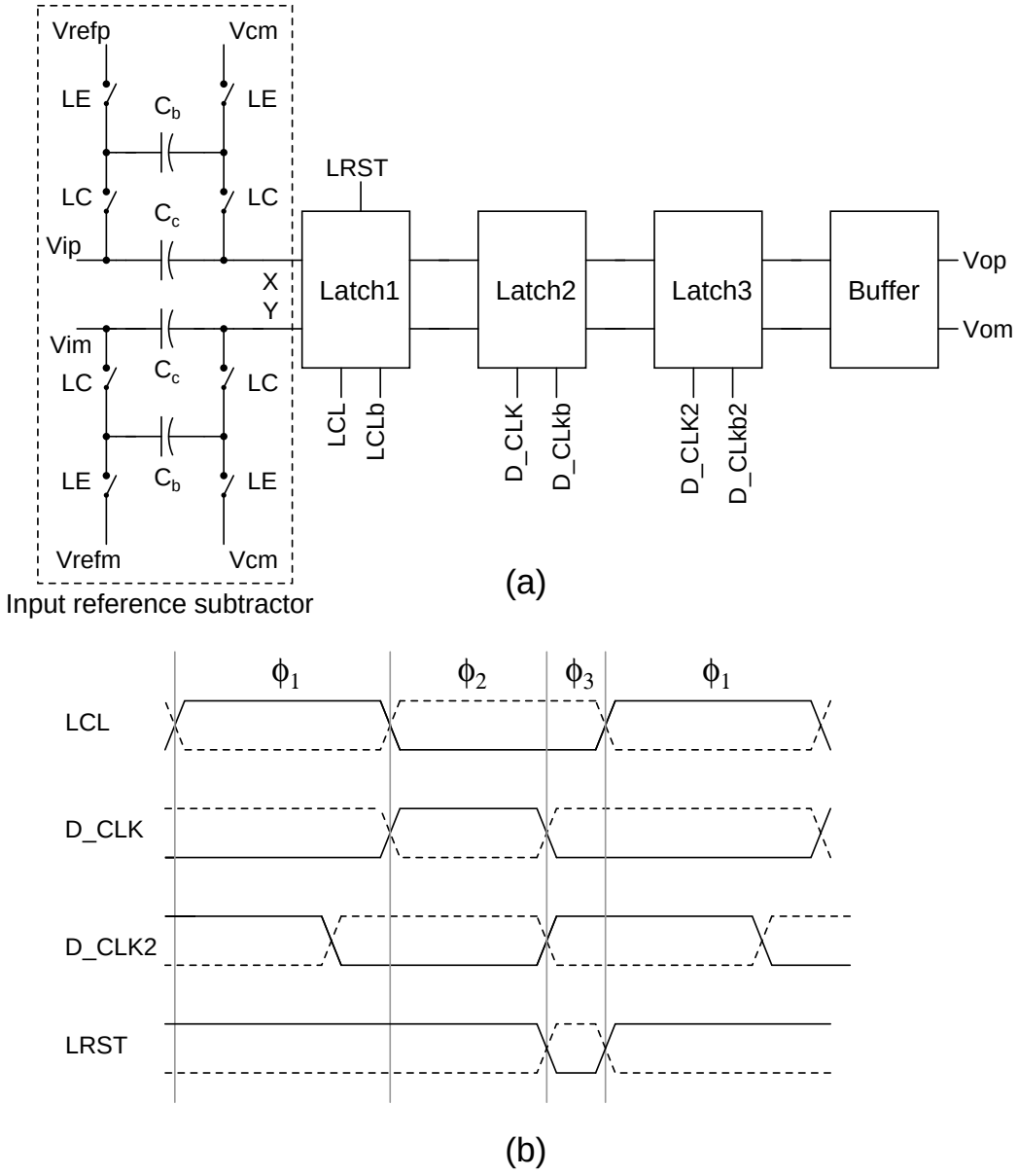


Figure 6.3: (a)Comparator block diagram (b) Clock waveforms,[4]

will be sampled by latch2 before the reset phase of latch1 as shown in Figure 6.3(b) The clock generation circuit has not been designed and ideal clocks are being used in the schematic of the Quantizer.

6.1.4 Buffer

Due to the finite output impedance of the current sources in the latches, the tail node parasitic capacitance along with the dip in the output voltage when the current switches from one arm to the other cause a lot of ripple in the output voltage [4]. An output buffer, shown in Fig. 6.4, is used to clean up this ripple.

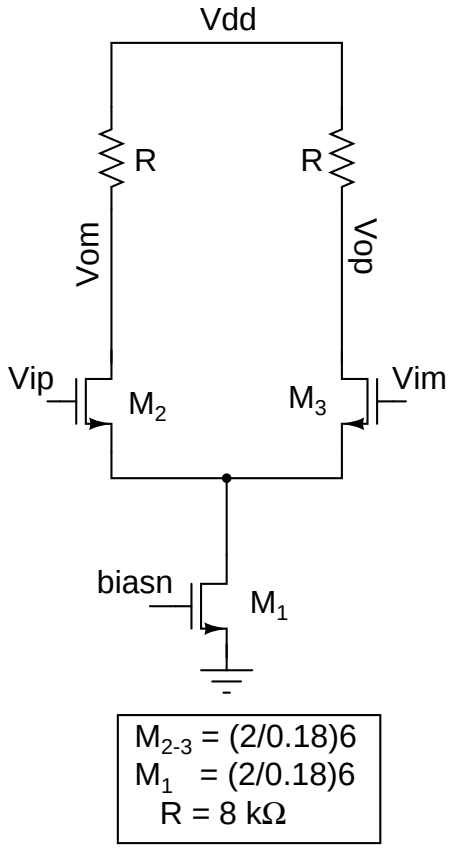


Figure 6.4: Buffer[4]

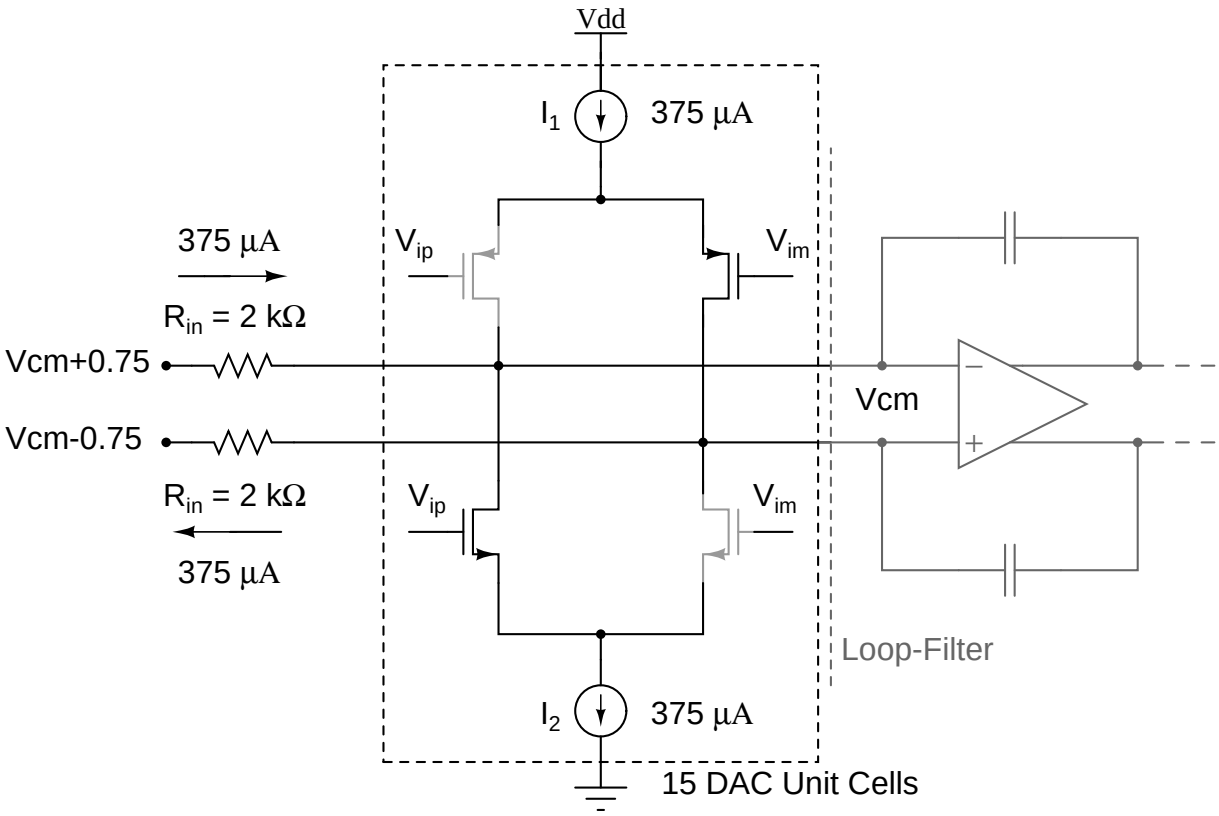
6.2 4-Bit DAC

6.2.1 Complementary Switching Architecture

A current steering DAC with complementary switching was designed [4]. Complementary switching architecture is shown in Figure. 6.5. The input referred noise and the current consumption are less in complementary steering architecture than one-sided switching architecture. The advantages of the complementary architecture are discussed in [4].

6.2.2 Unit DAC Cell

The unit DAC cell with the architecture that of [4] is implemented. The circuit diagram of the unit DAC cell is shown in Figure 6.6. When clk is high inv_{1-2} writes the information about the input D and Db into the latch (inv_5 and inv_6 connected back-to-back).



Unit DAC cell current = 375/16 = 23.44 µA (for 15 cell)

IDAC maximum = 15/16*(375 µA) = 351.5 µA

Figure 6.5: Circuit diagram of complementary current steering DAC feeding to loop filter input [4]

The latch is a positive feed back circuit and stores the information about the input for complete cycle. The clock used in DAC cell are CMOS and the $\text{inv}_{1,2}$ converts the CML input from ADC to CMOS level. M_{n1-2} and M_{p1-2} are nMOS and pMOS switches respectively, used to steer the current in one of the two paths. The current sources used in the schematic are ideal, resistance dependent reference current generating circuit is not designed. The outputs om and op are connected to the virtual nodes of the first integrating opamp.

6.2.3 Simulation Results

Figure 6.7 shows the spectrum of the output voltage for a differential input of 3 $V_{peak-peak}$. SNR obtained is 23.89 dB.

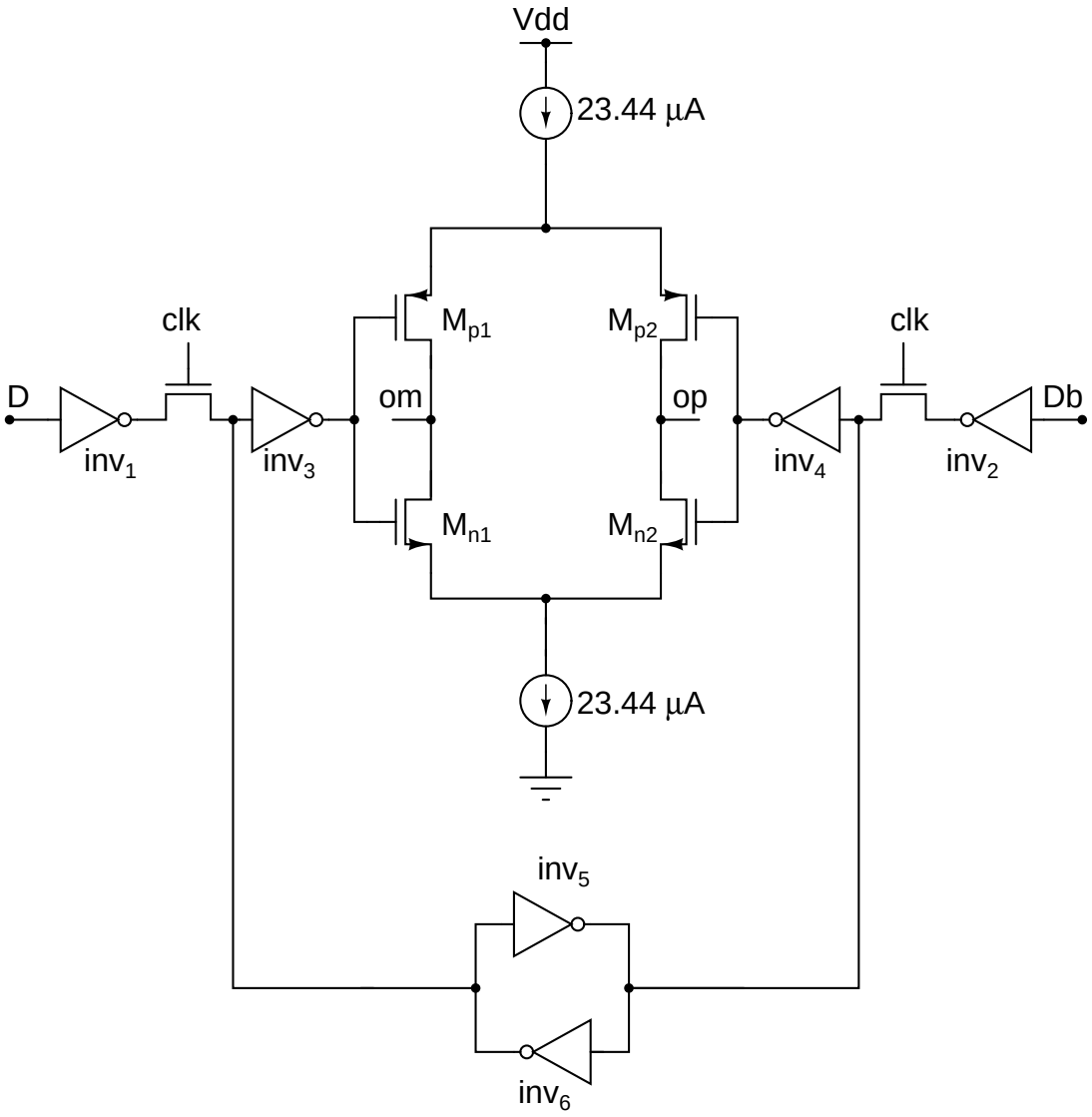


Figure 6.6: DAC unit-cell [4]

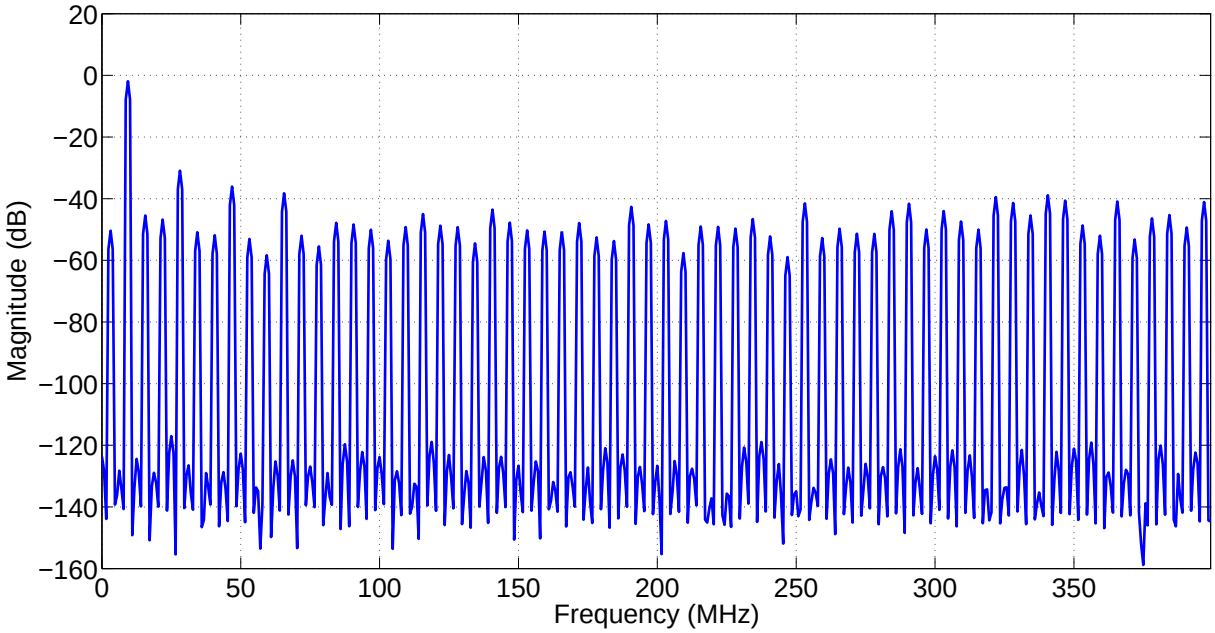


Figure 6.7: Output spectrum of the quantizer for a 3 $V_{peak-peak}$ input

CHAPTER 7

Circuit Level Simulation Results

7.1 Transistor level simulation at the schematic level

Fig. 7.1 shows the PSD at the output of the modulator with the verilog blocks in the loop filter (Integrator Opamps, Summing Opamp and fast loop) replaced by its transistor level schematic with ideal quantizer. (0.18 μm SCL CMOS models are used). Obtained SNR at an input equal to MSA is 93 dB. There was 3 dB variation in this SNR across various process corners. Table 7.1 shows the summary of the simulated performance.

The Fig. 7.2 shows the behaviour of the modulator for the variation in ELD.

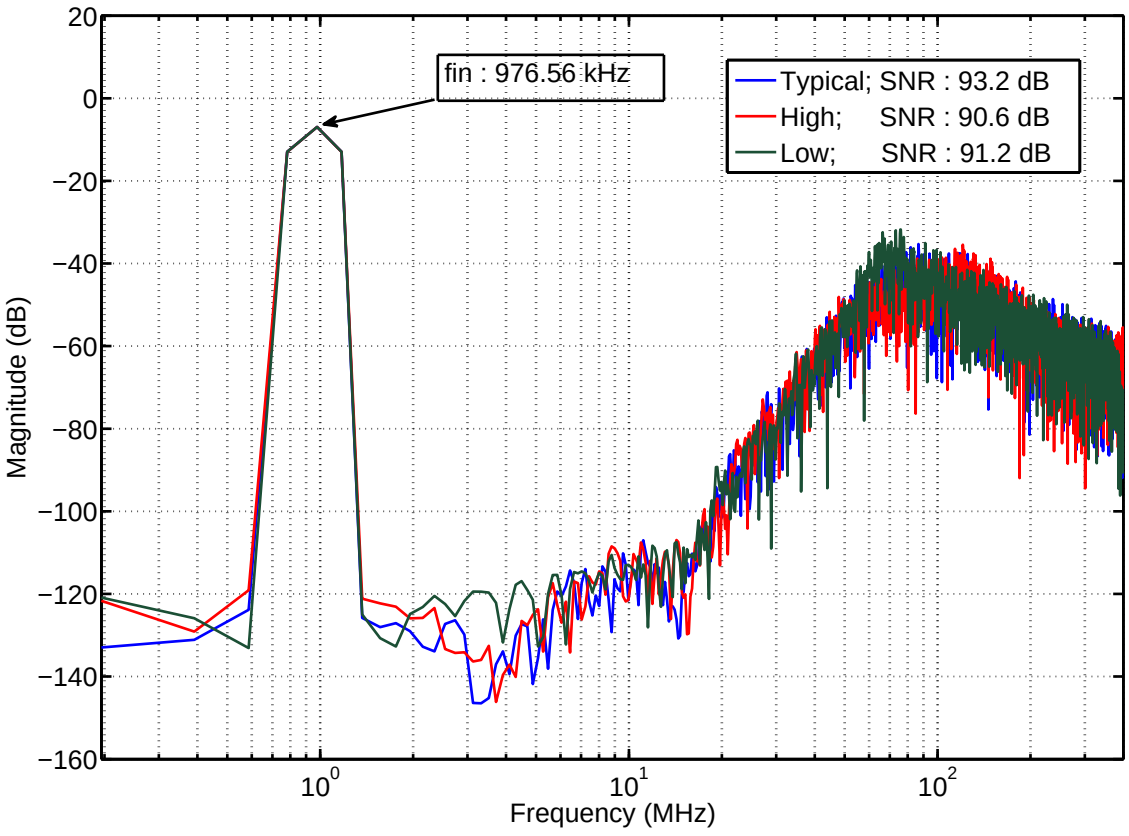


Figure 7.1: PSD of the modulator: Transistor level circuit

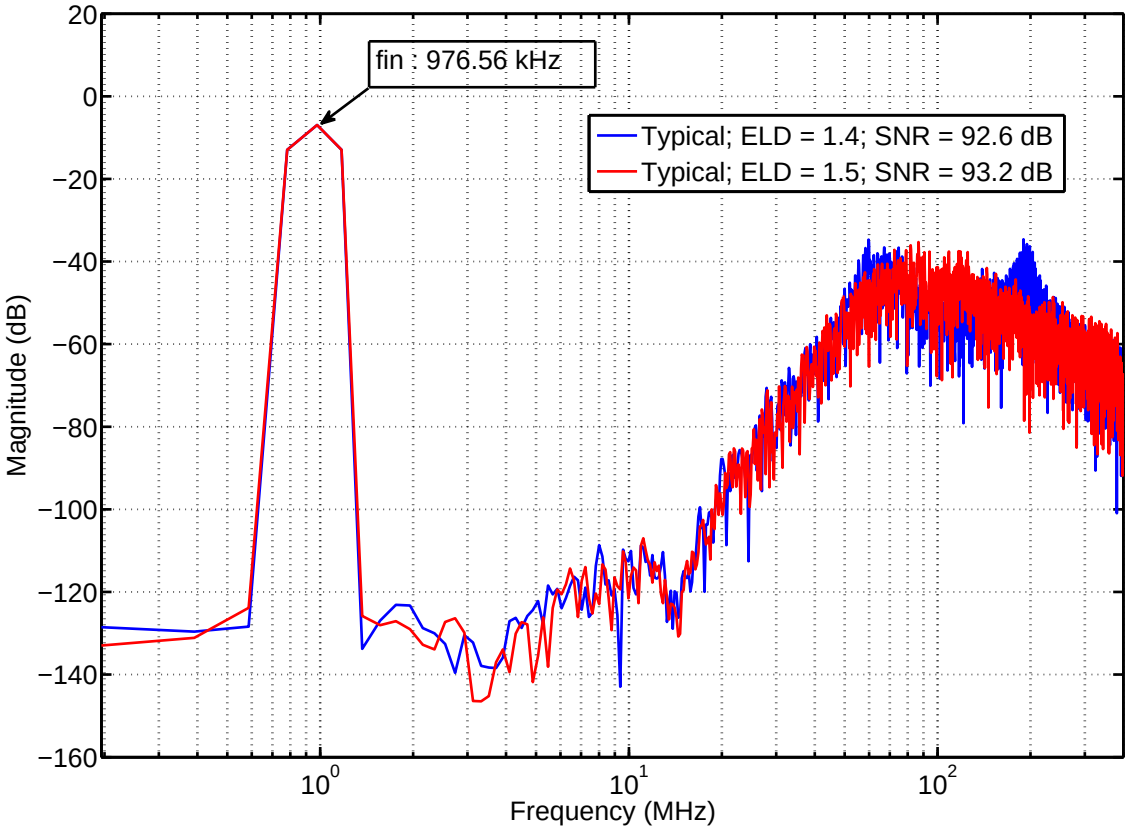


Figure 7.2: PSD of the modulator for ELD variation

7.2 Summary of the Simulation Results

Table 7.1: Simulation Results

Resistor	Capacitance	Temp (°C)	SNDR (dB)
typ	typ	27	93.2
max	max	0	90.6
low	low	80	91.2

7.3 Summary of the Simulation Results

Table 7.2: Simulation Results

Block	Power(V = 1.8) mW
1^{st} Opamp	6.21
2^{nd}, 3^{rd} & 4^{th} Opamp	1.98 (each)
Summing Opamp	10.62
Fast Loop (S/H & G_m cell)	5.2

The worse case quantization noise in transistor level simulations was -93 dB. Thermal noiose of the modulator is -84 dB. So total noise (thermal noise + quantization noise) is -83.2 dB.

7.3.1 Final Results

Table 7.3: Summary of the Loop Filter performance with ideal quantizer

Sampling Frequency	800 MHz
Input Bandwidth	16 MHz
MSA	0.73
SQNR	90 dB
Inband Thermal Noise	-84 dB
Peak SNR	81 dB
Power	28 mW
Process	180 nm SCL CMOS

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