Mixer Design, Ground Bounce effects and Power Amplifier design

A Project Report submitted by

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In partial fulfillment of the requirements for the award of the degree of

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CERTIFICATE

This is to certify that the project titled **Mixer Design, Ground Bounce effects and Power Amplifier design**, submitted by **Dinesh Katam (EE11B016),** to the Indian Institute of Technology, Madras, for the award of the degree of Bachelor of Technology in Electrical Engineering, is a bonafide record of the project work done by him in the Department of Electrical Engineering, IIT Madras. The contents of this report, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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Place: Chennai
Date: 10.06.2015

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I take this opportunity to express my sincere gratitude towards my project guide, Dr. S. Aniruddhan, for the freedom and support he gave me during the course of the project. I am extremely grateful to him for agreeing to take me on as his student. His guidance and deep knowledge in the field have been indispensable.

CONTENTS

INTRODUCTION

This project was done in three phases. In the initial phase, design of active and passive mixer was done. Mixers translate modulated carriers from one frequency to another by multiplying the input by a square wave (a sum of odd harmonics). In addition to generating sum and difference components, mixer will also generate unwanted spurs at multiples of the LO and Carrier frequencies. Mixers also add noise, IMD products and LO leakage to the output spectrum. The design was aimed at reducing these unwanted effects.

In the next phase, I worked with Abhishek Kumar, PhD. Scholar under Dr. S. Aniruddhan. The work focused on reducing the ground bounce effects due to bond wires specifically in Power Amplifier design. The aim of the work was to deliver as much power as possible from the PA with efficient operating point of the transistors. The use of series resonance with an extra bond wire, substantially reduces ground-bounce effects in narrowband RF front-ends. Instability check, impedance balancing is also done.

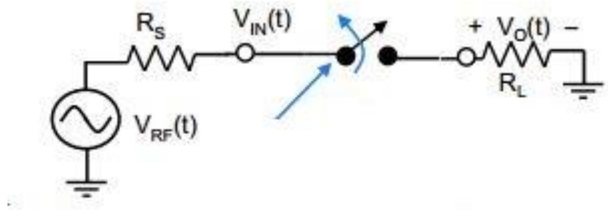
In the final phase, a single-ended dual band Power amplifier is designed. An RF Power Amplifier is usually the final active block of any electronic system that is transmitting RF Power. Its main task is to increase the power level of signals at its input up to a predefined level. It is the most power hungry building block of RF transceivers and careful design has to be made for high efficiency. The primary advantage of a dual band PA is significant reduction in silicon area, without compromising on RF performance and power efficiency. Simulation results and plots are shown.

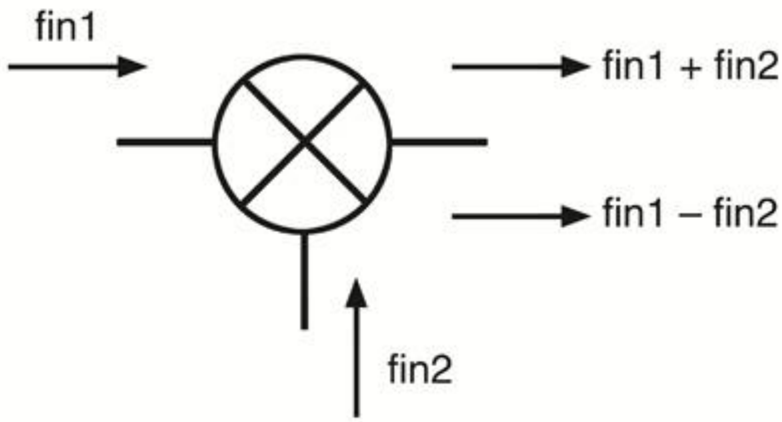
PHASE-1

Mixers

Passive Mixers:

A passive mixer implemented with switches is chosen for its low-power and high linearity performance.





The operation of a passive mixer can be understood if we view the MOSFET as a switch. The mosfet is on for 50% of the time. In effect, the RF is multiplied by LO, a square wave. Since the LO signal must switch the switches on and off, a large LO power is required.

$$Conversion\ gain\ = \frac{output\ power\ at\ f_{IF}}{RF\ available\ input\ power}$$

Passive mixers have the significant advantages:

1. They don't require a dc bias current
2. They don't dissipate standby power
3. They commutate the signal in the voltage domain.
4. Thus, they are well suited for applications requiring low flicker noise and low power consumption.

5. Passive mixer is very linear. The device is either "on" or "off" and does not impact the linearity too much. Since there is no transconductance stage (active mixer has transconductance stage), the linearity is very good.

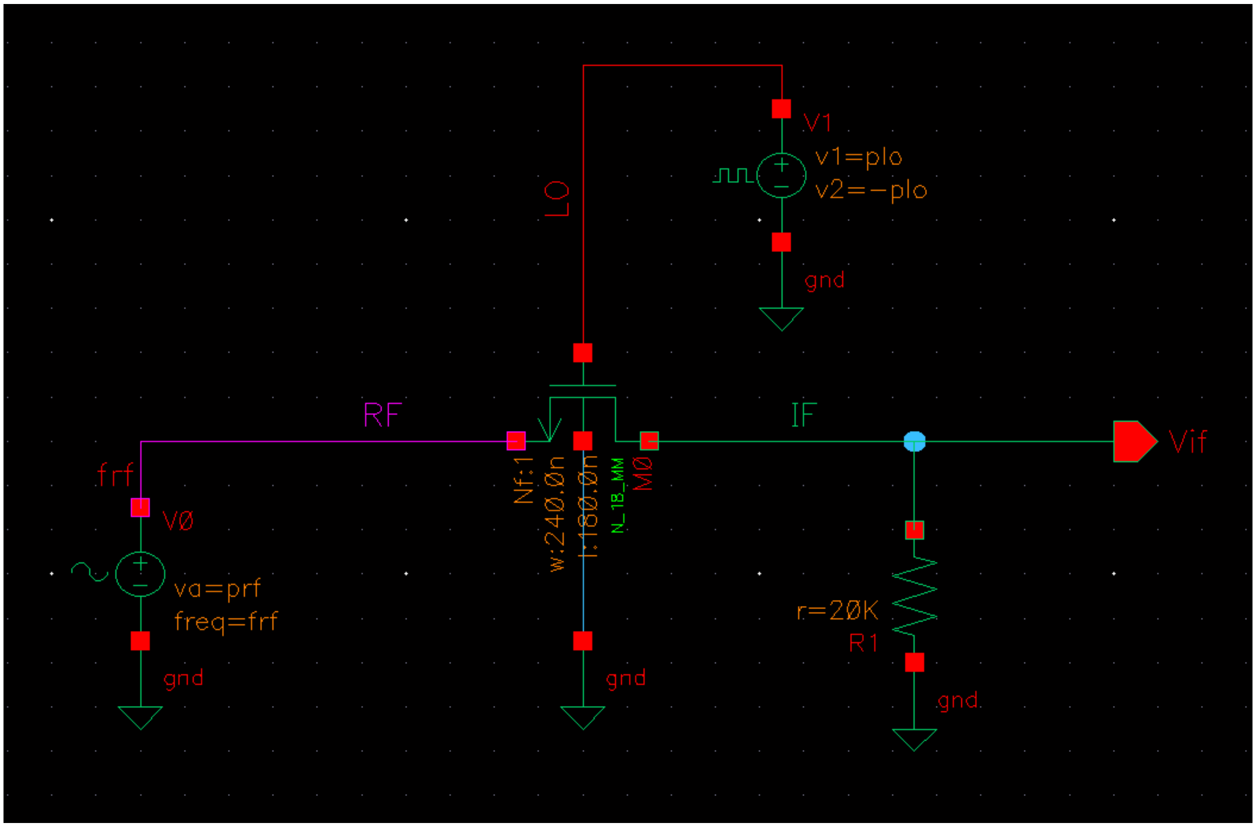
Disadvantages of passive mixer:

The downside is that the MOS mixer is passive, or lossy. There is no power gain in the device. At the same time, there are also drawbacks of high noise figure and high conversion loss.

Hence, usually we use an LNA before the passive mixer so that the overall noise figure gets better. Passive mixers are used when the signal is still healthy (less lossy) and linear mixer is required.

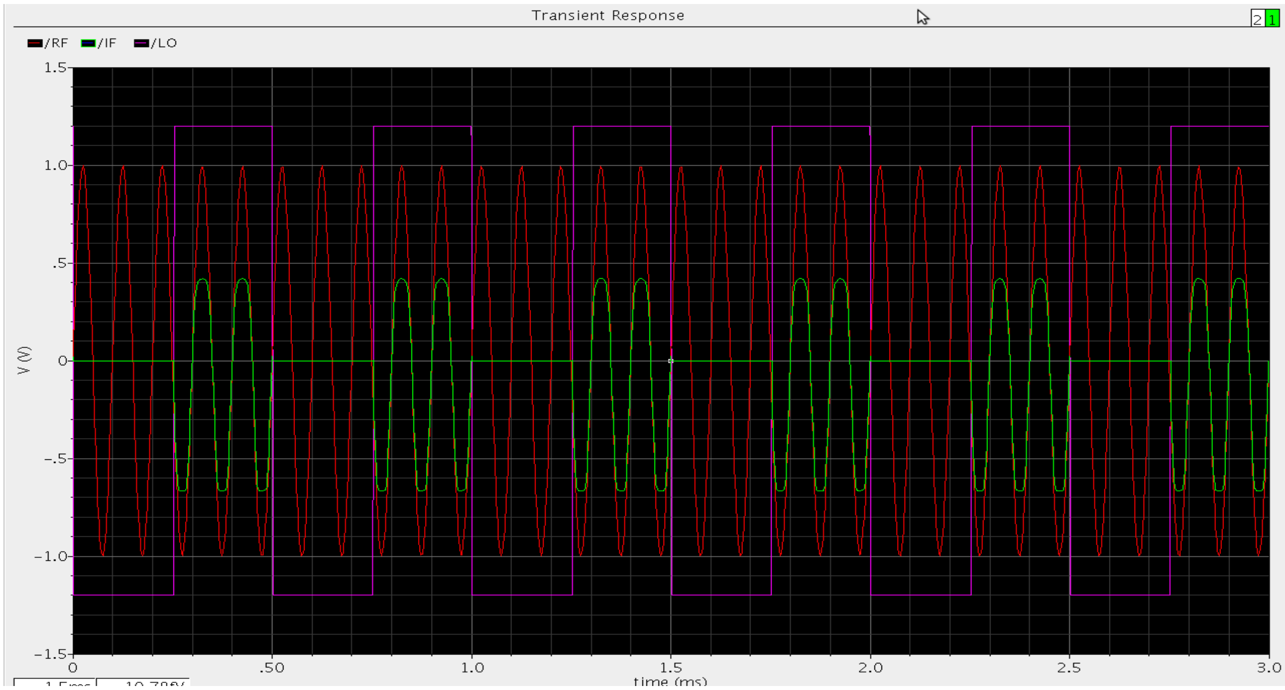
Simulation data:

Testbench Schematic (used 180nm process technology):

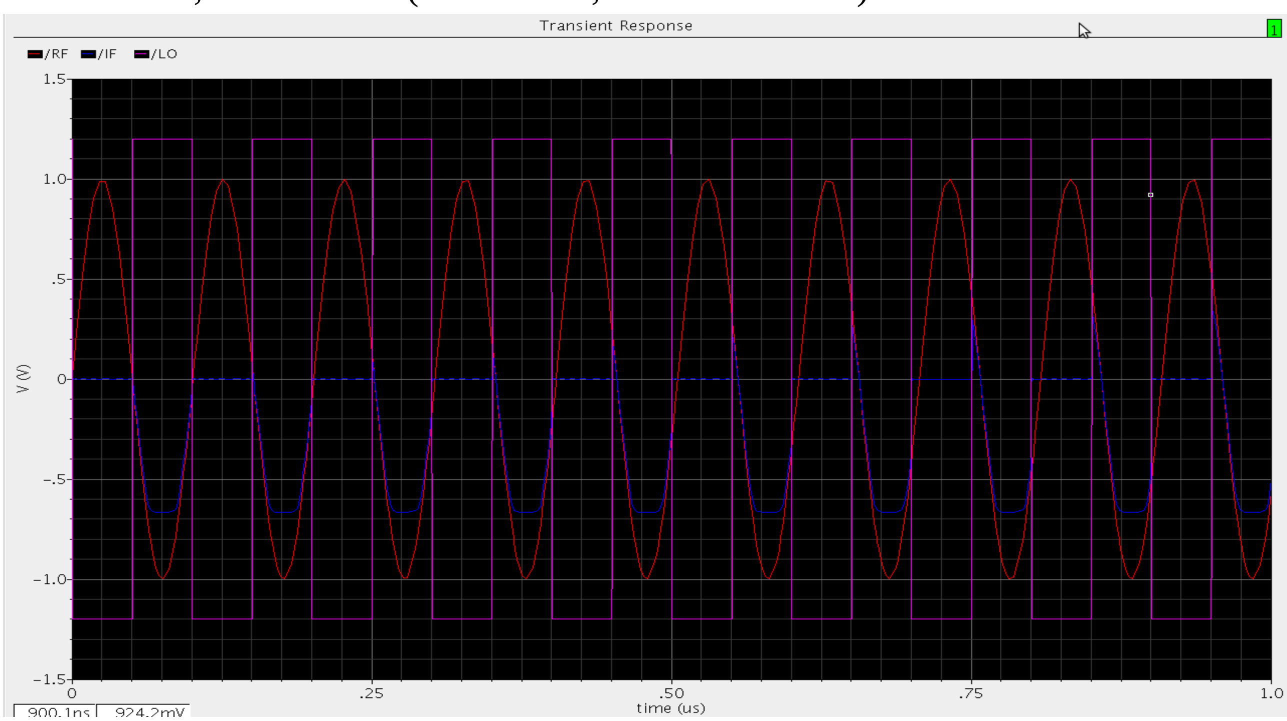


Transient analysis

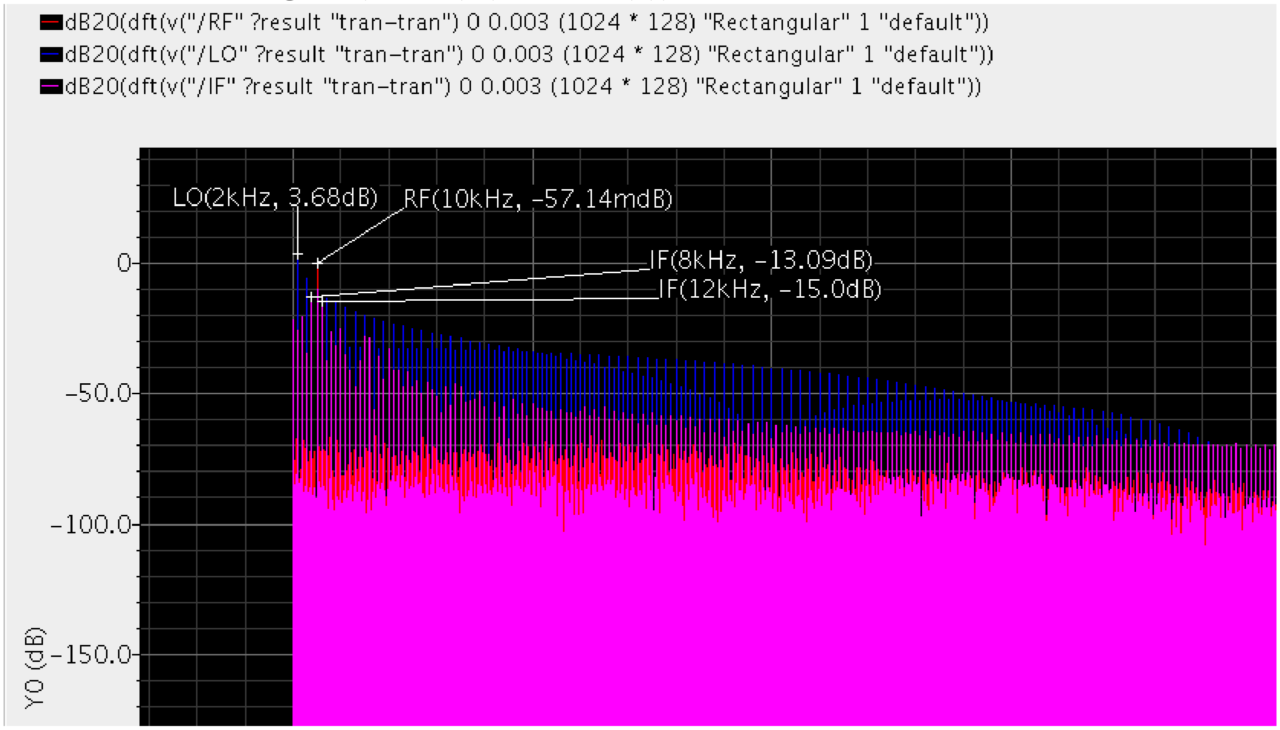
a) RF=10kHz , LO=2kHz (IF=8kHz and 12kHz)



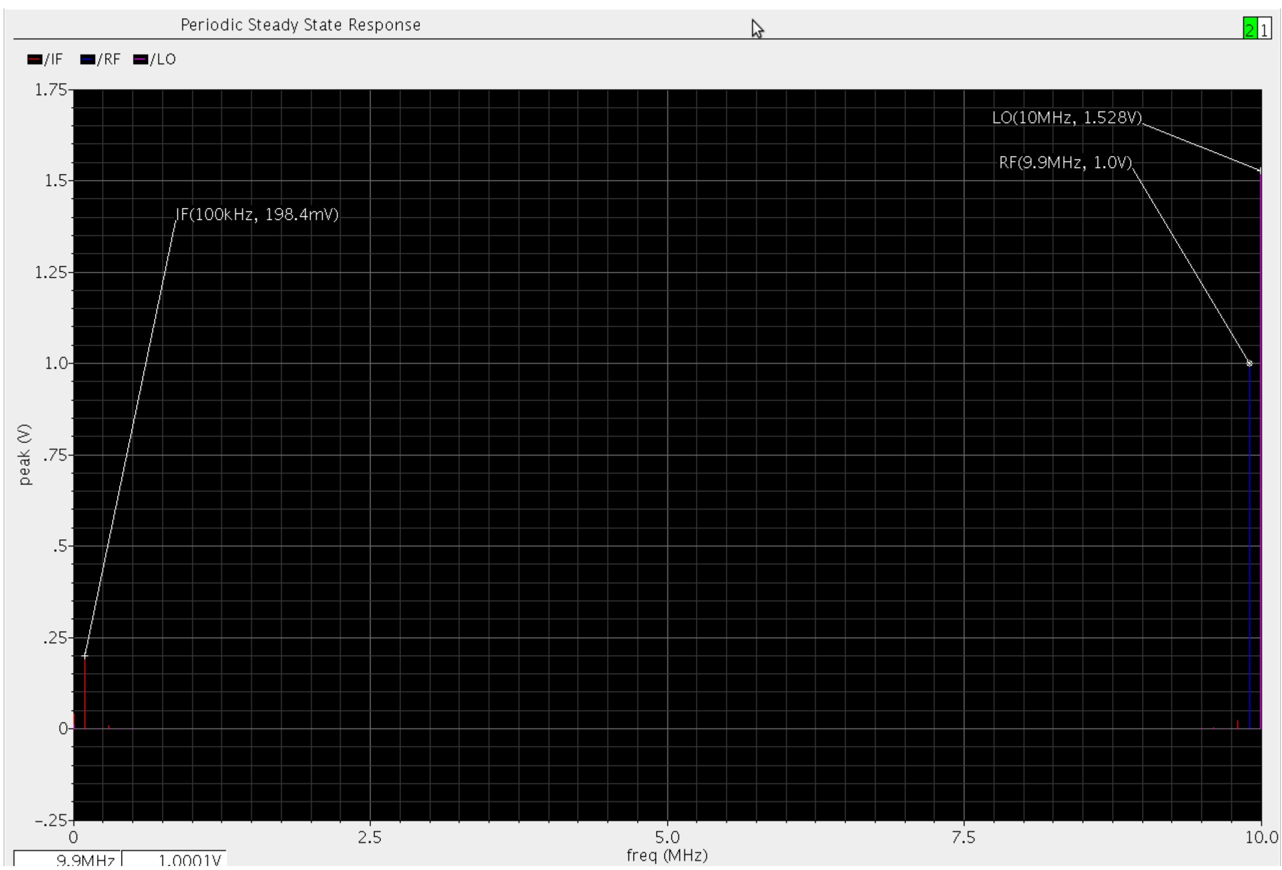
b) RF=9.9MHz, LO=10MHz (IF=100kHz, downconversion)



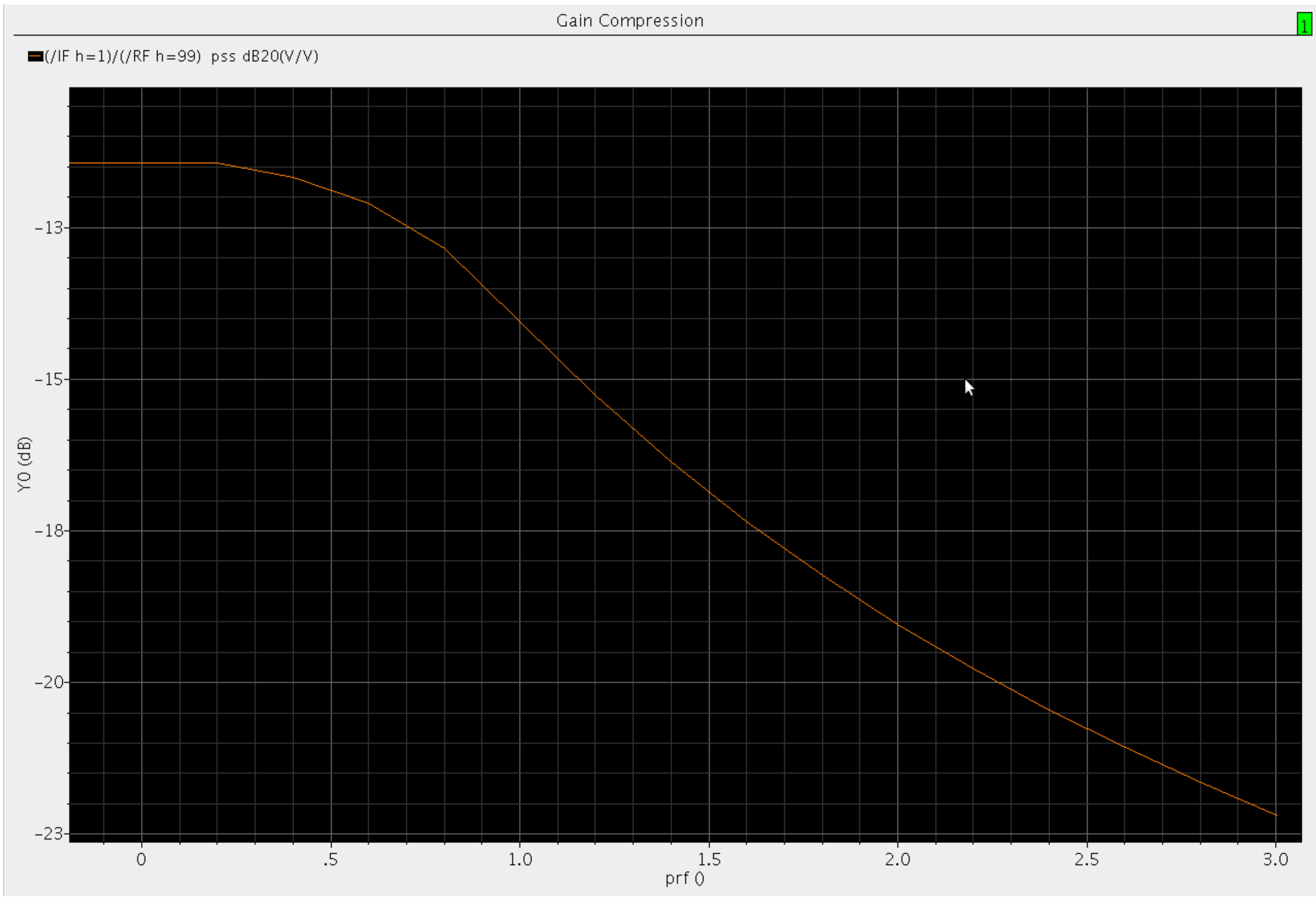
Conversion gain (-13dB) (for case (a)):



PSS sim showing frequency harmonics of IF for case (b)

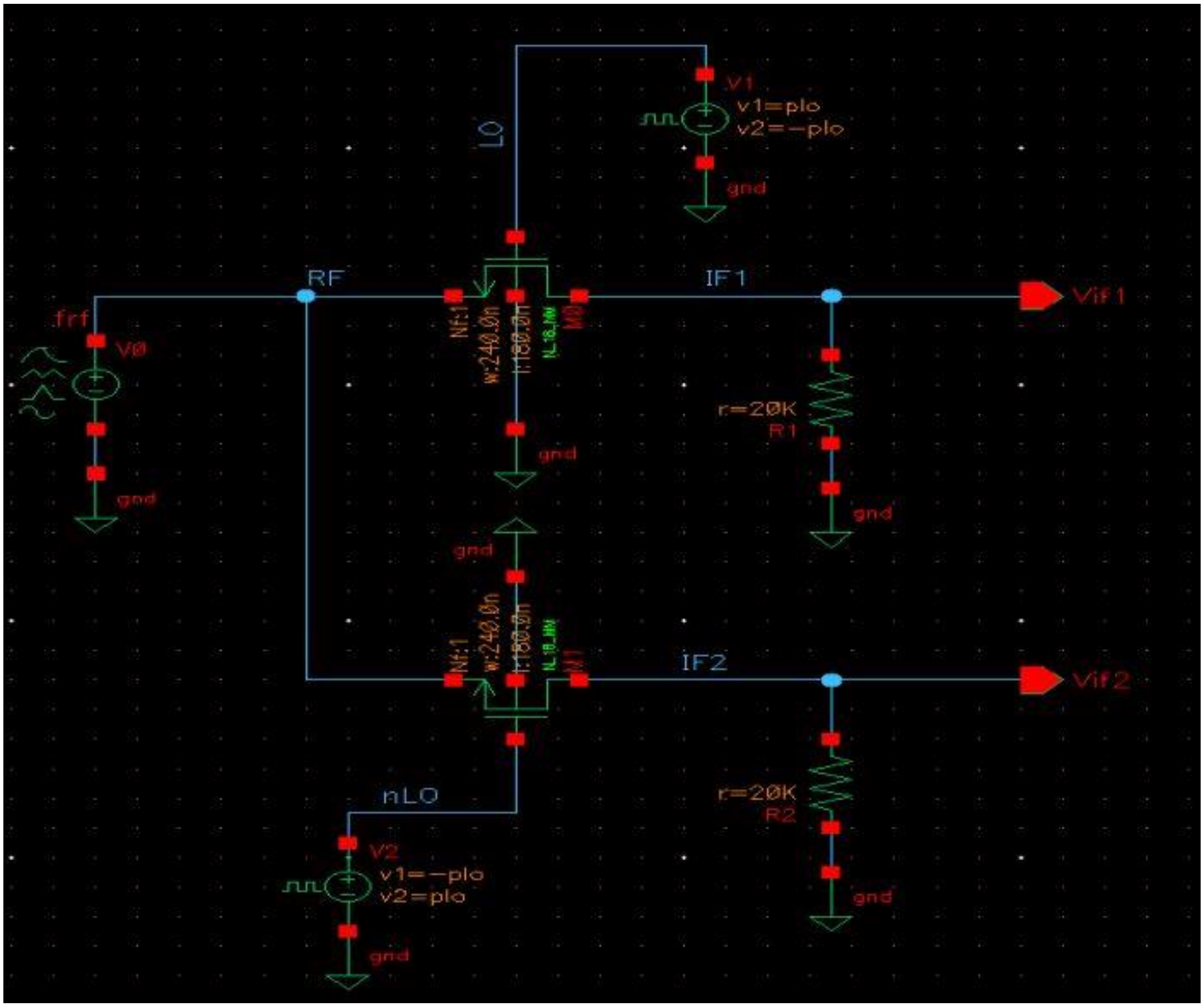


Gain compression plot:



Conversion gain vs input power

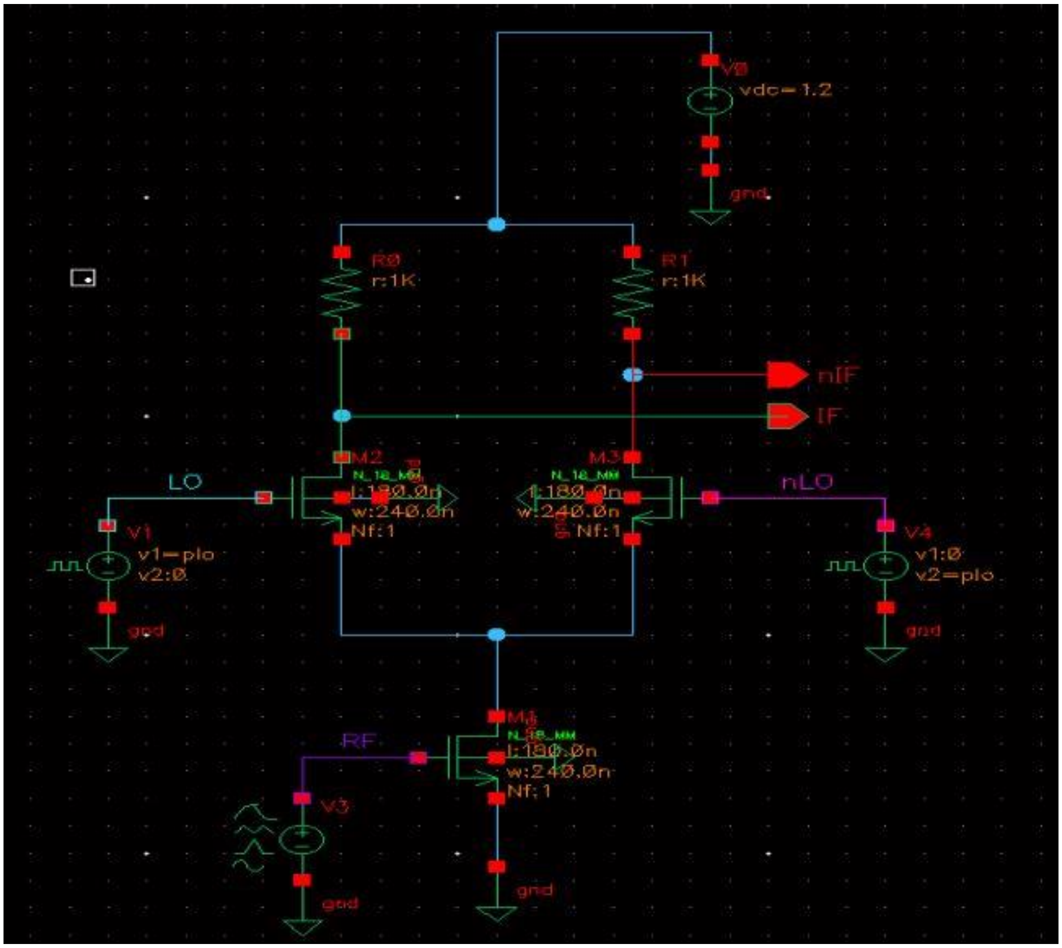
Single Balanced Passive Mixer:

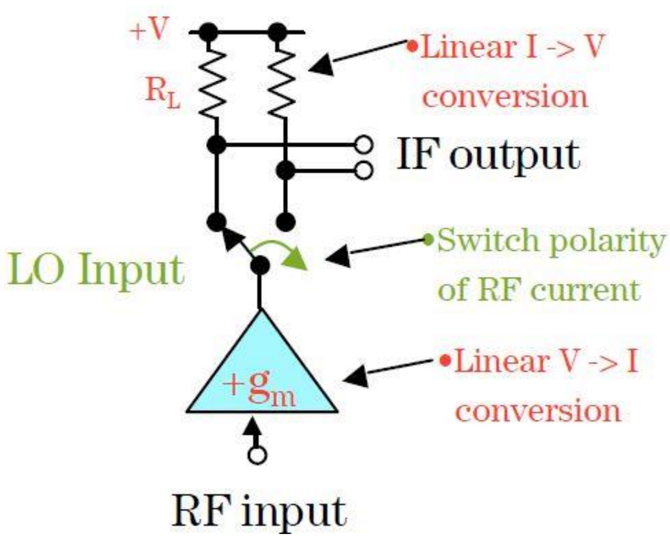


With a single-balanced passive mixer design, the resulted direct-conversion receiver achieves an ultralow flicker-noise corner with 6 dB more gain and much lower power and area consumption than the double-balanced mixer. It is interesting to note that the single-balanced passive mixer is able to achieve positive voltage conversion gain instead of loss.

ACTIVE MIXERS:

Single Balanced Active Mixer:

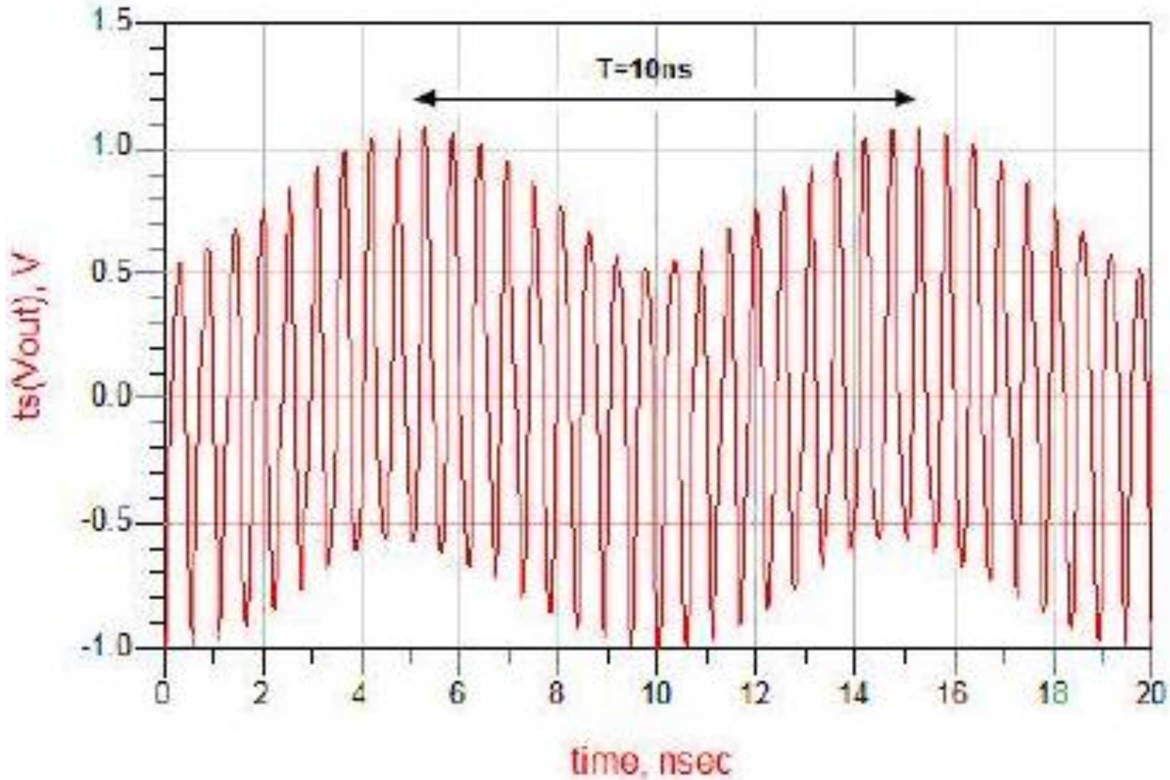




The RF feedthrough can be eliminated by using a differential IF output and polarity reversing LO switch. But, we can still get LO feedthrough if there is a DC current in the signal path. This is often the case since the output of the transconductance amplifier will have a DC current component. This current shows up as a differential output.

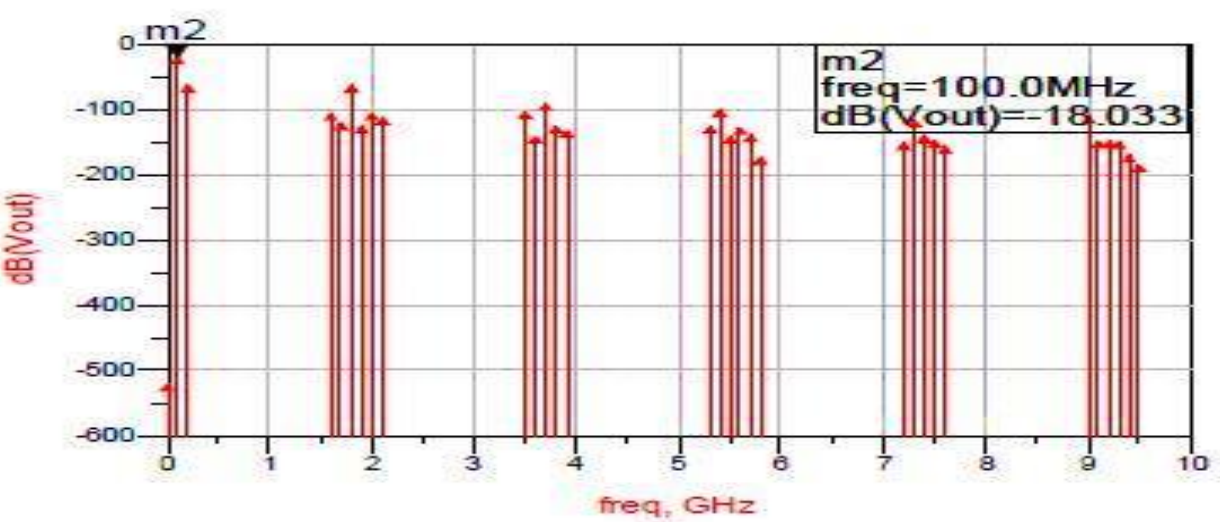
Simulation result:

Transient analysis:



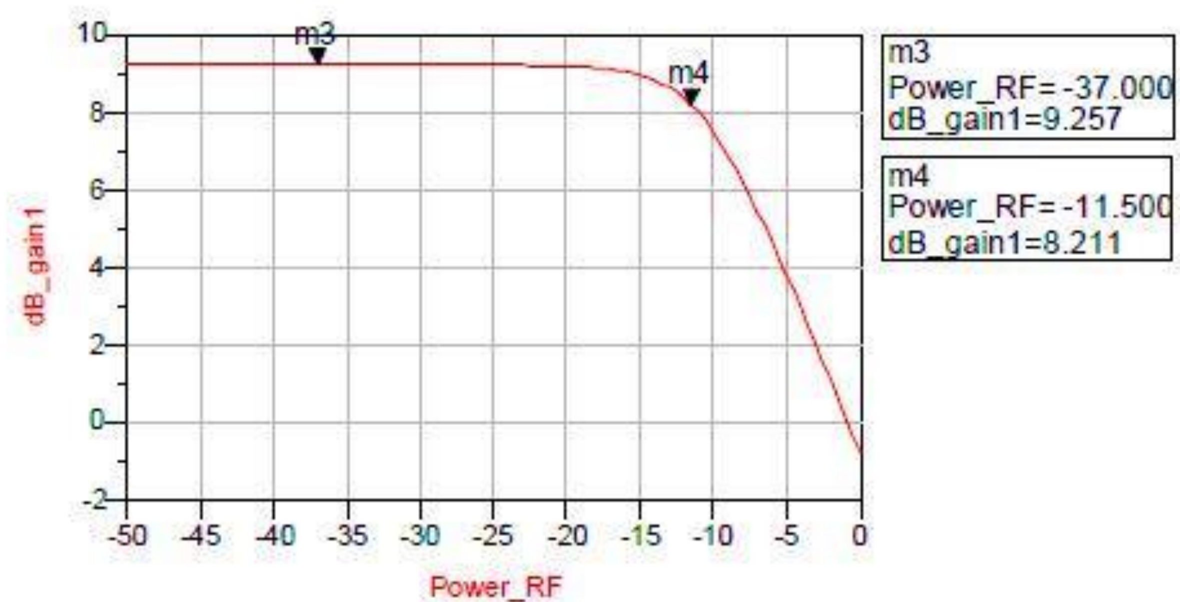
For

F_{RF}= 9.9GHz, F_{LO}= 10 GHz and F_{IF} is at 100MHz



As you can see, the output spectrum of the single-balanced switching mixer is much less cluttered than the nonlinear mixer spectrum. This was simulated with transient analysis. The LO was generated with a 1.2V pulse function and the duty cycle was set to 50%. The output is taken differentially as Vout = IF - nIF. Note the strong LO feedthrough component in the output. This is present because of the DC offset on the RF input which produces a differential LO voltage component in the output.

Gain conversion (1dB gain conversion point):

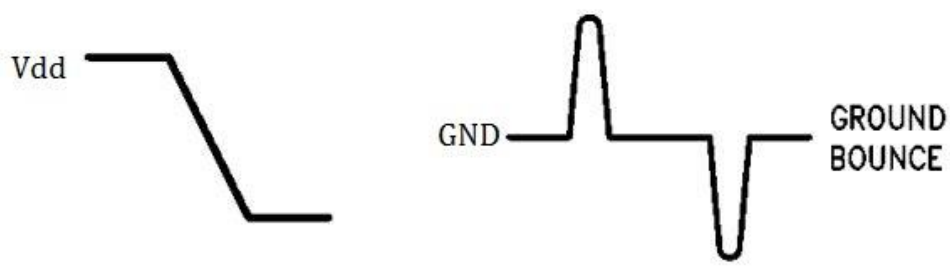


PHASE-2

Ground Bounce:

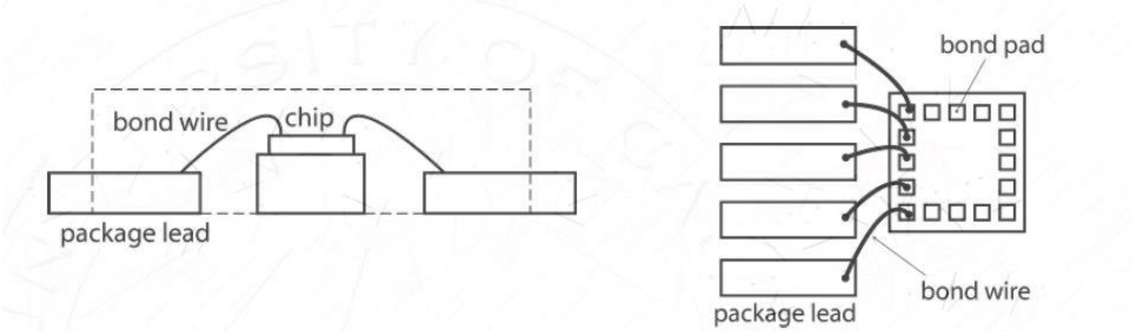
Ground bounce is a phenomenon where ground inside of a chip goes up and down relative to the ground on the PCB. This is mostly due to the lead inductance of the pins combined with high-speed changes in current on the ground pins. The more current on the ground pins, and the more that current changes, the more ground bounce there will be. Package pins, bonding wires, and on-chip IC interconnects all have parasitic inductances. The emitter/source inductance is a major problem as it limits the device swing, reducing the efficiency of the amplifier. It also is a big source of ground bounce that can lead to instability. When an inductor current experiences time-domain variation, a voltage fluctuation is generated across the inductor. This voltage is proportional to the inductance of the chip-package interface and the rate of change of the current. As a result, when the logic cells in a circuit are switched on and off, the voltage levels at the power distribution lines of the circuit fluctuate. At RF frequencies, the impedance offered by package parasitics in the form of bond wires and leads become comparable to the load and source impedances. Unless taken into account, it is very difficult for RF signals to cross the barrier between chip and board formed by these package parasitics.

$$V_{bounce} \propto L\frac{dI}{dt}$$



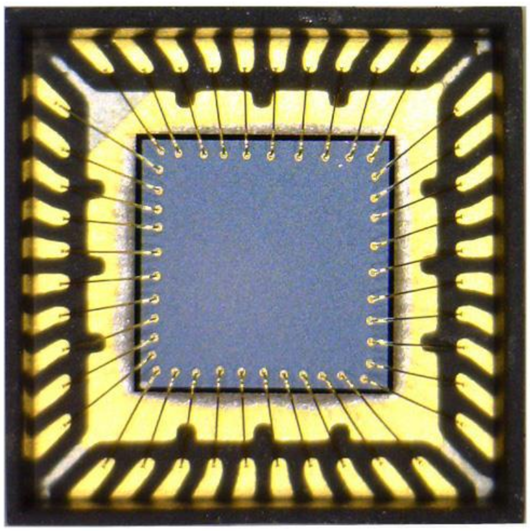
Minimizing ground-bounce and its effects:

1. Reducing the length of bondwires connecting to sensitive nodes.
2. Differential implementation of RF front-ends.
3. A large capacitor can be connected between power and ground inside the chip to supply transient currents.
4. Impedance balancing of the output stage to null the effects of ground-bounce due to other on-chip circuits.
5. The output stage ground is often separated to mitigate the coupling effect (adding/subtracting from the input signal).



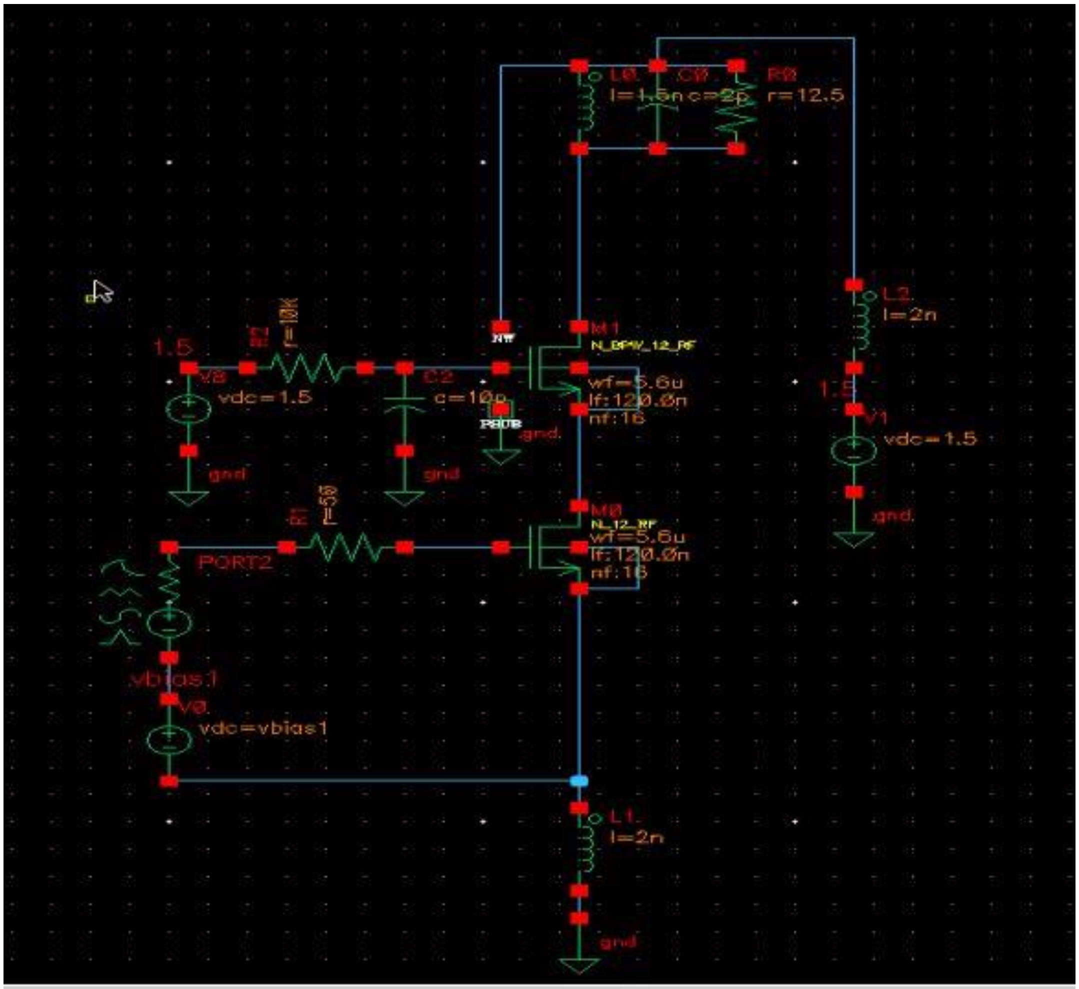
Use as many bondwires to reduce this inductance

<u>Bond wire:</u>



Bond wires are Interconnections between an IC or other semiconductor device and its packaging during semiconductor device fabrication. Although less common, wire bonding can be used to connect an IC to other electronics or to connect from one PCB to another.

Bond wire Implementation:



The bond wires, modelled as inductances are placed in the schematic as shown above. The 2nH inductance is connected near the ground and supply. The results are shown below:

1. Input referred P1dB= -4.89145dBm
2. Output referred P1dB= 12.0758dBm
3. Small signal gain= 13.07854dB

The capacitance at the gate of the cascode nMOS is changed and the following is observed:

Capacitance (pF)	**Input referred P1dB (dBm)**	**Output referred P1dB (dBm)**	**Small signal gain (dB)**
10	-4.89145	12.0758	13.07854
5	-3.33468	11.0063	12.00771
1	3.35386	6.76363	7.76402

Though the Input referred P1dB is improving for smaller caps, it is observed that Output referred P1dB and Small signal gain degrade.

<u>Comparison of specs with and without bond wire:</u>

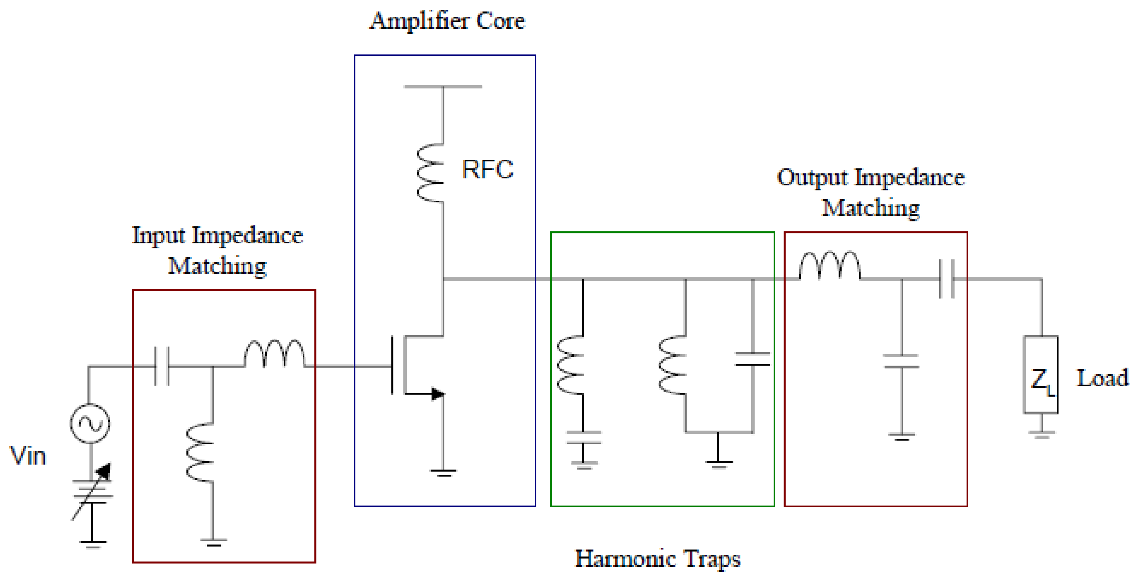
Spec	**Without Bond wire**	**With bond wire**
Input referred P1dB (dBm)	-4.858	-4.89145
Output referred P1dB (dBm)	12.9365	12.0758
Small signal gain (dB)	13.95	13.07854

The specs degrade slightly when the bond wire is placed. This is due to ground bounce effect and has to be reduced.

PHASE-3

RF Power Amplifier- Design and Layout

1. **Introduction:**



Basic PA topology

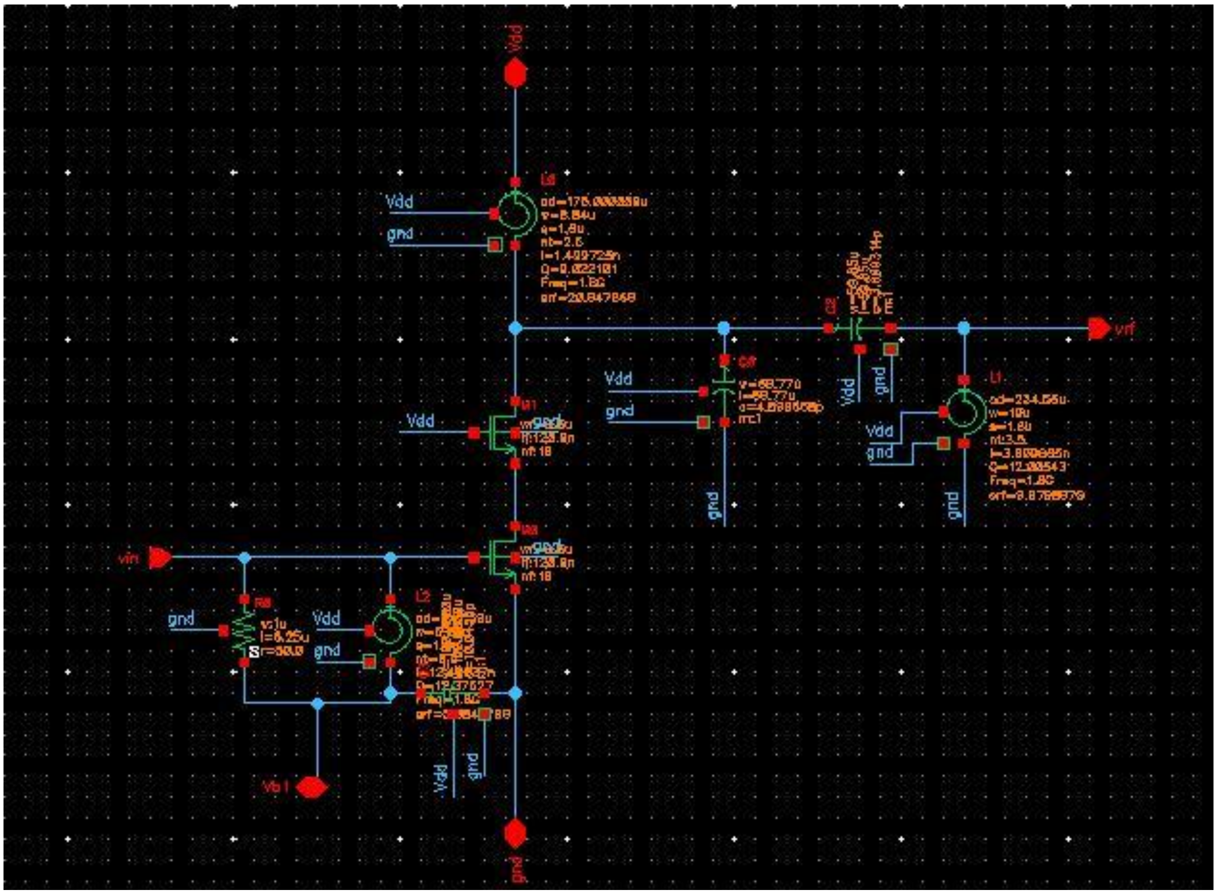
The power amplifier (PA) is a key element in transmitter systems, whose main task is to increase the power level of signals at its input up to a predefined level. PA's requirements are mainly related to the absolute achievable output power levels, in conjunction with highest efficiency and linearity performances. The power consumption of PA is the dominant component of total transmitter power consumption, making the PA efficiency crucial. The linear power amplifiers are optimized for maximum gain and linearity.

This work describes a **1.8-GHz** class-A power amplifier with 12.80dBm saturated output power, and 31.60% maximum Power Added Efficiency (PAE) is designed in the UMC 130-nm CMOS process. The OP1dB is 8.31dBm .At the 5dBm output, the required input power level is -11.57dBm and PA consumes 31.1134mA from **VDD=1V**. The PA is single-ended.

This work also describes: 1.8GHz class A PA with supply voltage VDD=3V, 0.9GHz class A PA with supply voltage VDD=1V and 0.9GHz class A PA with supply voltage VDD=3V. The performance parameters of the above PAs are compared and tabulated in this work.

2. **Circuit design:**

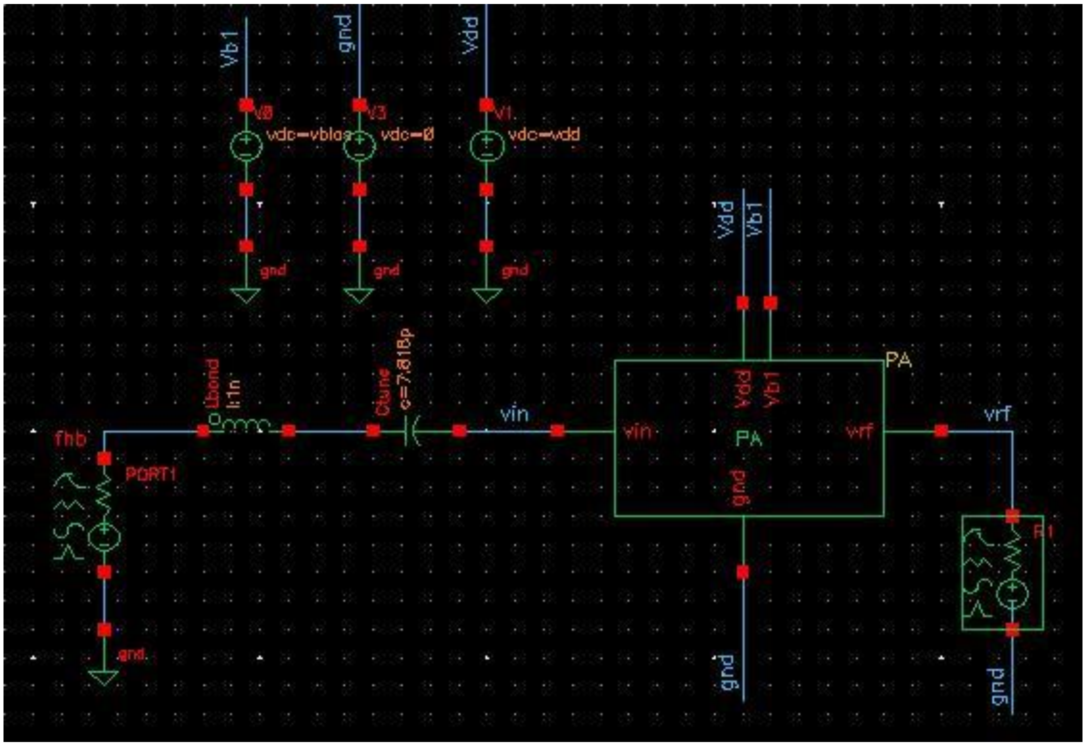
The figure below shows the circuit schematic of power amplifier. It is realised using NMOS transistor in common-source (CS) configuration, with the device biased in the saturation region of operation. The other transistor acts as a cascode device which relaxes the constraints on the maximum swing allowed at the drain node, which reduces the stress on the transistors.



An inductor between the power supply and drain node of the transistor acts as an RF choke, presenting a short circuit for DC and open circuit for the RF signal. It therefore supplies the bias current, while at the same time, allowing the drain node to swing around its quiescent value, equal to the supply voltage. The inductor value is chosen such that it tunes out unwanted harmonics.

The input and output are matching is done using resonant LC circuit. For a given output power, the voltage swing required at the output increases with increase in load impedance. The output impedance transformation is done in order to deliver the required power; the load impedance has to be down converted to a lower value to keep the voltage swings within the (reliability) limits.

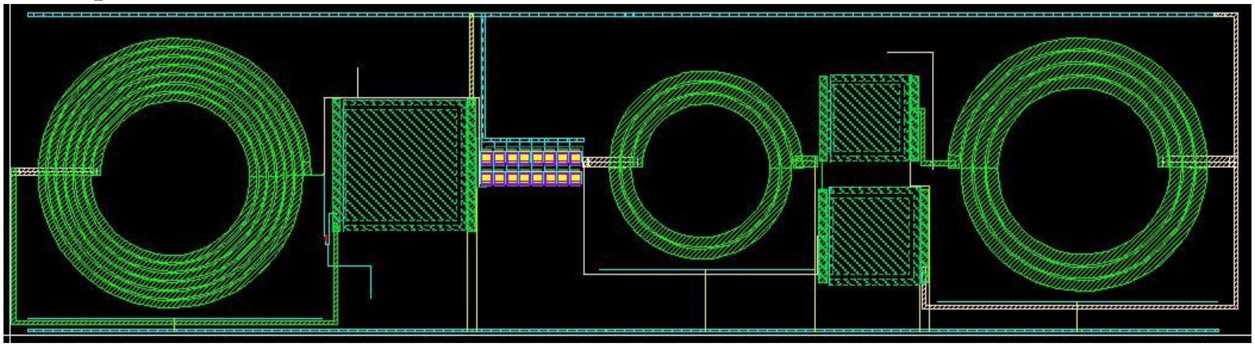
Here is the test bench (the 1nH inductor is the bond wire inductance which can be resonated out with a capacitance of value 7.818pF):



3. **Layout:**

The most important parameters considered in the layout are total area and routing.

Floor plan:



The total area is $0.32\ mm^2$.

The layout is DRC passed and LVS passed. RC extraction was done and the simulations were performed.

4. **Specifications/Performance:**

The most important parameters that define an RF Power Amplifier are:

- Output Power
- Gain
- Linearity
- Stability
- DC supply voltage
- Efficiency

Choosing the bias points of an RF Power Amplifier can determine the level of performance ultimately possible with that PA. By comparing PA bias approaches, can evaluate the tradeoffs for: Output Power, Efficiency, Linearity, or other parameters for different applications.

- The Power Class of the amplification determines the type of bias applied to an RF power transistor.
- The Power Amplifier's Efficiency is a measure of its ability to convert the DC power of the supply into the signal power delivered to the load.

- The definition of the efficiency can be represented in an equation form as:
  $\eta = \frac{Signal\ power\ delivered\ to\ the\ load}{DC\ power\ supplied}$ or $Power\ Added\ Efficiency = \frac{P_0 - P_{in}}{P_{DC}}$
- Power that is not converted to useful signal is dissipated as heat. Power Amplifiers that has low efficiency have high levels of heat dissipation, which could be a limiting factor in particular design.
- In addition to the class of operation, the overall efficiency of a Power Amplifier is affected by factors such as dielectric and conductor losses.

Class A PA is defined, as an amplifier that is biased so that the output current flows at all the time, and the input signal drive level is kept small enough to avoid driving the transistor in cut-off. Another way of stating this is to say that the conduction angle of the transistor is 360°, meaning that the transistor conducts for the full cycle of the input signal. That makes Class-A the most linear of all amplifier types, where linearity means simply how closely the output signal of the amplifier resembles the input signal.

5. <u>Simulation Results:</u>

The following simulations are done for each version of the PA:

- OP1dB and Gain
- Transient analysis
- Power consumption
- Efficiency
- IIP3
- ACPR
- AM-PM plots

A. <u>OP1dB and Gain:</u>

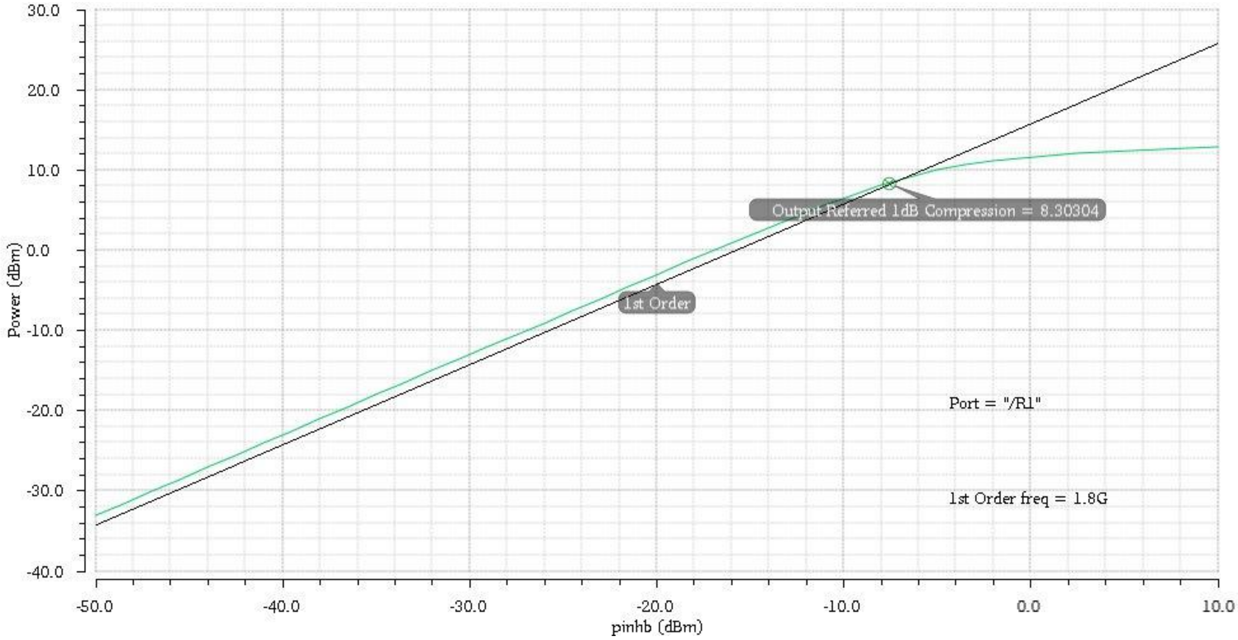
The input 1dB compression point is the input power at which the linear gain of the amplifier has compressed by 1 dB. The output referred 1-dB compression point (in dB) would then be given by the sum of the input referred 1-dB point (in dB) and the gain of the amplifier (in dB). This metric is often used measure of the linear power handling capability of the PA. When the output power does not further increase due to a higher input power, the PA is said to be saturated and it cannot deliver more power regardless of the input power to PA. The gain determines the amount of power that needs to be delivered to the load. PA's are required to boost the transmitted signal by providing a signal gain to the output of the preceding stage, usually a mixer.

We introduce the input RF power, P_{in}, driving the whole amplifier chain. By combining the input power, P_{in}, and the output power, P_{out} the Gain, G, can be defined as the ratio of the output power and the input power, usually expressed in dB. $G = 10log_{10}(\frac{P_{out}}{P_{in}})$

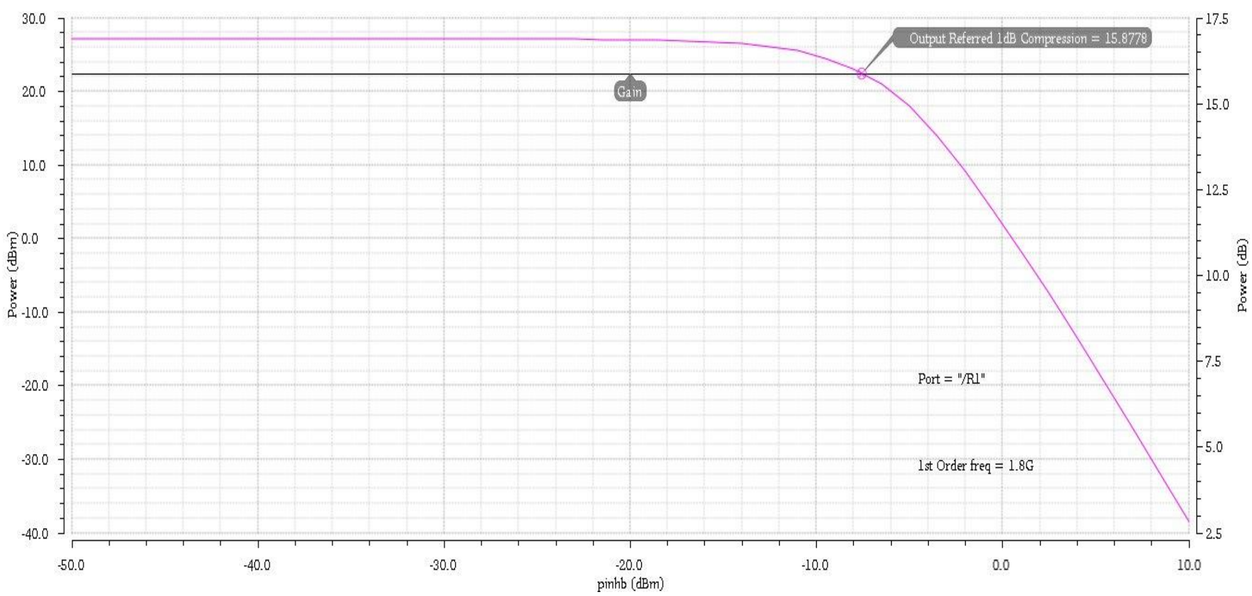
Here are the results of simulation:

	High Band(1.8GHz) Vdd=1V	High Band(1.8GHz) Vdd=3V	Low Band(0.9GHz) Vdd=1V	Low Band(0.9GHz) Vdd=3V
Gain(dB)	16.57	17.11	12.24	13.87
OP1dB(dBm)	8.303	8.23	7.86	9.16

Example Plots:



OP1dB High Band 1V PA



Gain High Band 1V PA

B. Power Consumption:

In a typical transmitter, the PA consumes the most amount of power from the supply/battery. For portable devices, it is essential that this parameter be kept to a minimum.

	High Band(1.8GHz) Vdd=1V	High Band(1.8GHz) Vdd=3V	Low Band(0.9GHz) Vdd=1V	Low Band(0.9GHz) Vdd=3V
Current drawn (mA)	31.11	8.65	31.11	8.65
Supply (V)	1	3	1	3
Power Consumed (mW)	31.11	25.95	31.11	25.95

C. Efficiency

An important measure of the PA is the efficiency as it directly affects the talk-time in handheld devices and has an impact on the electricity bill in base stations. One of the efficiency measures is the Drain Efficiency, which is defined as the ratio between the average output power at the fundamental, Pout, and the DC power consumption. When considering the input power, Pin, needed to drive the amplifier chain, we can define another efficiency metric called Power-Added Efficiency, PAE as the input power subtracted from the output power, which is then divided by the total DC power consumption.

	High Band(1.8GHz) Vdd=1V	High Band(1.8GHz) Vdd=3V	Low Band(0.9GHz) Vdd=1V	Low Band(0.9GHz) Vdd=3V
Drain Efficiency	61.24%	68.11%	56.28%	65.45%
PAE	31.60%	32.11%	33.32%	36.73%

**The efficiencies are quoted at maximum (saturated) output power*

	High Band(1.8GHz) Vdd=1V	High Band(1.8GHz) Vdd=3V	Low Band(0.9GHz) Vdd=1V	Low Band(0.9GHz) Vdd=3V
Drain Efficiency	10.16%	12.18%	10.16%	12.18%
PAE	10.03%	11.86%	10.05%	11.9%

***The efficiencies are quoted at 5dBm output power*

D. Linearity (Third-order intercept point and ACPR):

Several wireless communication standards employ modulation schemes with non-constant envelopes, which need to be amplified by PAs capable of linear amplification. To quantify the level of linearity, or rather, the level of non-linearity, several measures exist.

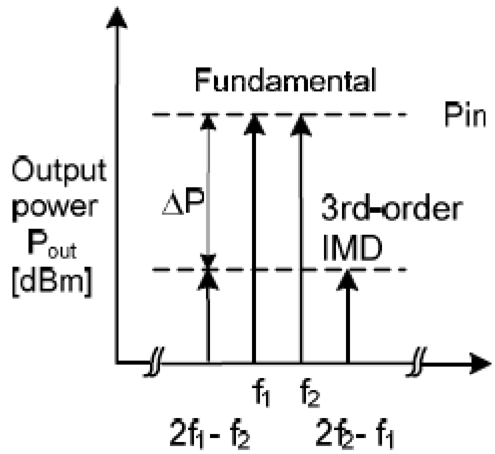
One of the sources of distortion in amplifiers is intermodulation, which appears when two closely located frequencies are transmitted through the PA at the same time. When two or more signals are input to an amplifier simultaneously, the second, third, and higher-order intermodulation components (IM) are caused by the sum and difference products of each of the fundamental input signals and their associated harmonics.

When two signals at frequencies f1 and f2 are input to any nonlinear amplifier, the following output components will result:

- Fundamental: f1, f2
- Second order: 2f1, 2f2, (f1+f2), (f1-f2)
- Third order: 3f1, 3f2, (2f1±f2), (2f2±f1)

The odd order intermodulation products (2f1-f2, 2f2-f1, 3f1-2f2, 3f2-2f1, etc) are close to the two fundamental tone frequencies f1 and f2.

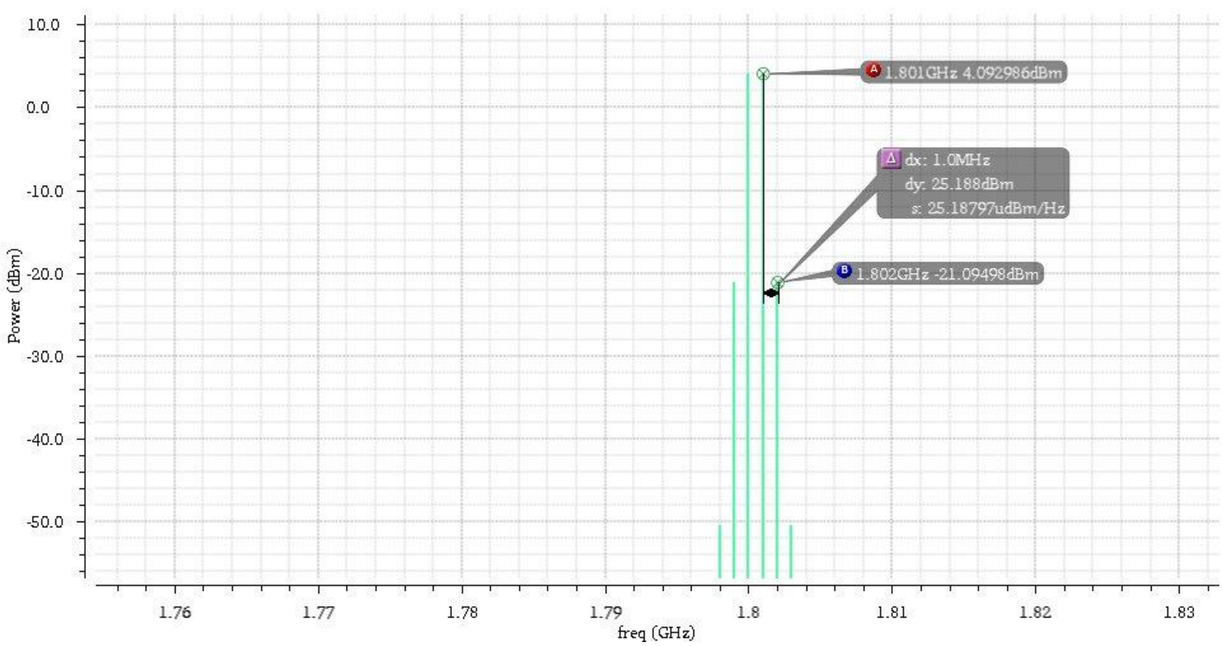
The nonlinearity of a Power Amplifier can be measured on the basis of generated spectra than on variations of the fundamental signal. The estimation of the amplitude change (in dB), of the intermodulation components (IM) versus fundamental level change, is equal to the order of nonlinearity.



$$IIP3_{dBm} = \frac{\Delta P}{2} + P_{in_{dBm}}$$

	High Band(1.8GHz) Vdd=1V	High Band(1.8GHz) Vdd=3V	Low Band(1.8GHz) Vdd=1V	Low Band(1.8GHz) Vdd=3V
IIP3 (dBm)	6.65	5.81	6.43	6.32

Plots:



IIP3 High Band 1V PA (Pin=-11.57dBm)

<u>ACPR:</u>

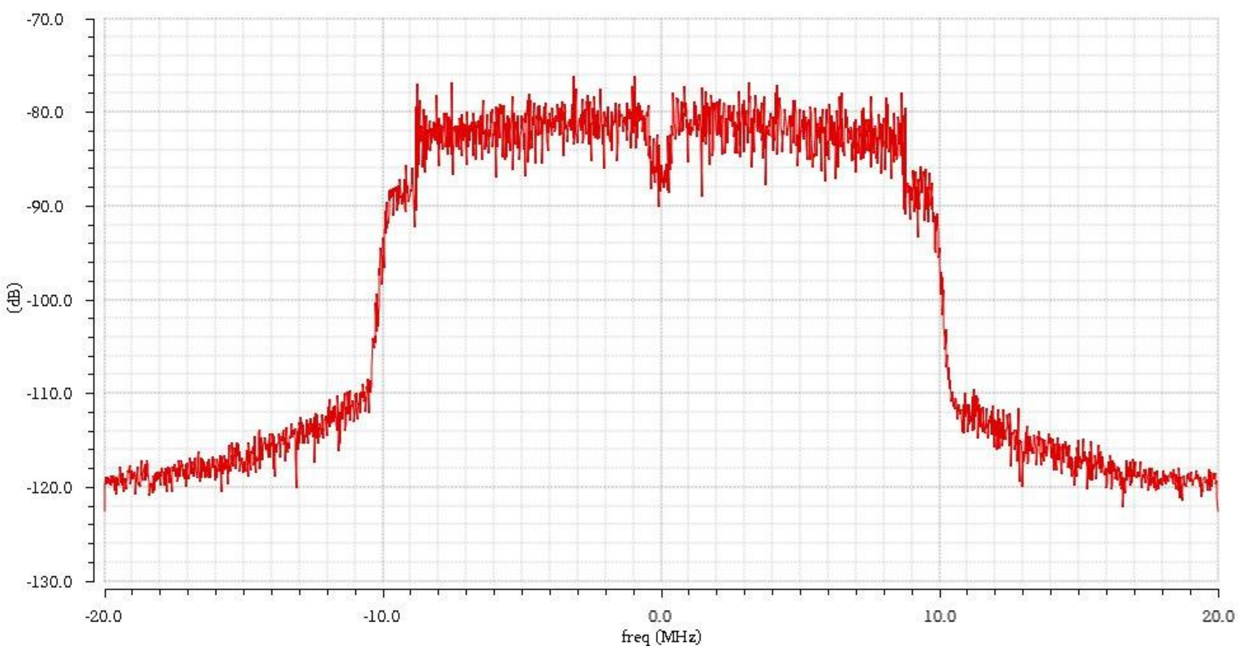
As the radio transmission has a frequency bandwidth (channel) allocated around the carrier, where the transmission may be conducted, any power falling outside these frequencies will disturb neighboring channels and the transmission therein.

The Adjacent Channel Power Ratio (ACPR) is defined as the ratio of power in a bandwidth away from the main signal to the power in a bandwidth within the main signal, where the bandwidths and acceptable ratios are determined by the standard being employed. The I and Q modulated input signal given is a QAM4 signal with a PAPR of 7.8 and 7.5 respectively.

The ACPR is measured at $P_{out} = 5dBm$

	High Band(1.8GHz) Vdd=1V	High Band(1.8GHz) Vdd=3V	Low Band(1.8GHz) Vdd=1V	Low Band(1.8GHz) Vdd=3V
ACPR(dBc)	-36.91	-37.14	-36.43	-37.21

Plots:



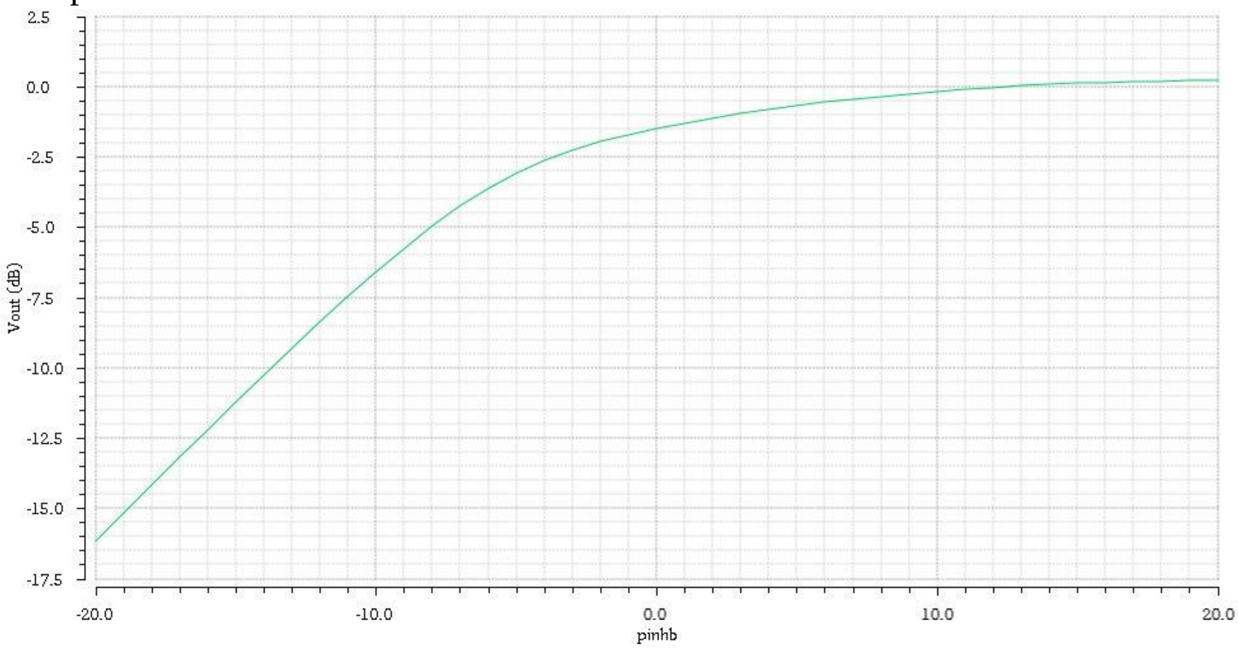
ACPR High Band 1V PA

AM-PM plots:

The nonlinear behavior of a PA is commonly tested via AM-AM and AM-PM conversions. They consist in the transformation of the input amplitude variations into variations of the output amplitude and phase, respectively.

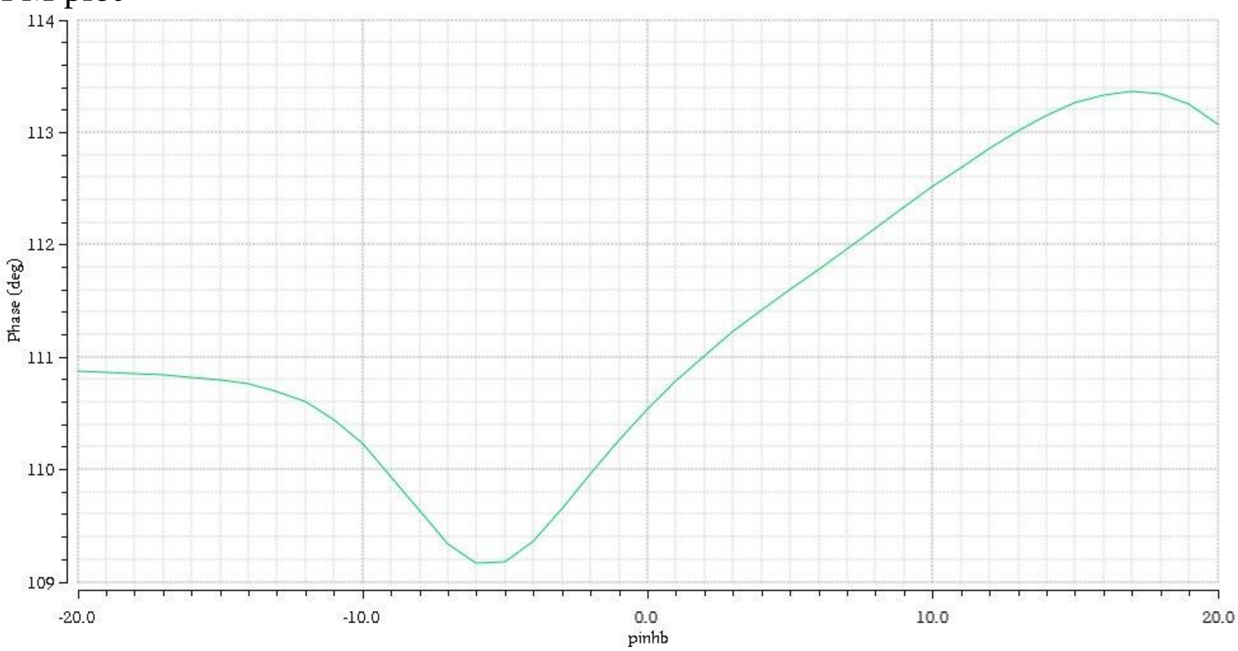
Plots:

AM plot



AM plot of High Band 1V PA

PM plot



PM plot of High Band 1V PA

CONCLUSION

Active and Passive mixer design is discussed in this work.

The effects of Ground bounce due to bond wires in RF systems is explained with the example of a Power amplifier (PA).

The design of the PA is also described in this work. The PA is class-A where the amplifier that is biased so that the output current flows at all the time, and the input signal drive level is kept small enough to avoid driving the transistor in cut-off. Another way of stating this is to say that the conduction angle of the transistor is 360°, meaning that the transistor conducts for the full cycle of the input signal.
A cascode device is used to reduce the stress on the transistors. That makes Class-A the most linear of all amplifier types. However, the efficiency-linearity trade-off is considered while designing the PA.
UMC130nm process technology is used to design the PA (High band, 1.8GHz) which with 1V supply, it transmits linear power up to 12.8dBm with 44% drain efficiency. The Low band (0.9GHz) PA is also designed with 1V and 3V supply. The low band and high band PAs can be combined with a shared inductor (RF Choke) which forms a dual band PA.

References:
RF Microelectronics, Razavi