DESIGN OF 12 BIT 500MSPS DIGITAL TO ANALOG CONVERTER

A Project Report

submitted by

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THESIS CERTIFICATE

This is to certify that the thesis titled **DESIGN OF 12 BIT 500MSPS DIGITAL TO ANALOG CONVERTER**, submitted by **G V S Vaishnavi**, to the Indian Institute of Technology, Madras, for the award of the dual degree of **Bachelor of Technology and Master of Technology**, is a bona fide record of the research work done by her under our supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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ABSTRACT

KEYWORDS: DAC ; High speed; 12 bit; 500MSPS; Current Steering; Resistive.

A 12 bit 500MSPS Digital to Analog Converter design is presented in this work. Different DAC architectures are explored and compared. A 6+6 segmented current steering DAC is designed in 65nm technology and its static and dynamic performance is characterized. The current steering DAC is observed to show an INL below 0.3LSB and an SFDR of 68dB close to Nyquist frequency for a sampling frequency of 500MHz. The dynamic performance of the DAC is observed to be limited by finite code dependent output impedance at high frequencies. Hence resistive DAC architectures are explored to improve dynamic performance of the DAC. A 3-way segmented DAC is designed with a segmentation of 6 thermometer, 3 binary weighted and 3 R-2R ladder DAC bits. With this configuration, with resistor mismatch, the DNL is calculated to be less than 0.1LSB and the INL is less than 0.4LSB. The SFDR of the resistive DAC is seen to be around 90dB till 100MHz and above 80dB till 150MHz..

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ABBREVIATIONS

DAC	Digital to Analog Converter
ADC	Analog to Digital Converter
DNL	Differential Non-linearity
INL	Integral Non-linearity
SFDR	Spurious free dynamic range
IM3	3rd order Intermodulation Distortion
UGB	Unity Gain Bandwidth
FFT	Fast Fourier Transform

CHAPTER 1

INTRODUCTION

The advent of high speed and low power analog and digital circuits calls for high performance data conversion circuits. As most naturally occurring signals are analog and as most processing today is done in the digital domain, there is a need for an ideal interface in terms of a digital to analog converter. Following Moore's law, as integrated circuits today are becoming smaller and smaller in size and much faster in terms of frequency of operation, the data conversion circuits in latest CMOS technologies targeting high frequency operation and low power consumption are becoming a widely researched area in the field of analog electronics.

In this thesis we describe the design of a high speed, high resolution digital to analog converter. Digital to analog conversion has been studied over the years using a number of different architectures. Linearity and spectral purity are among the major concerns in digital to analog converter performance. The trade-off in converter design is usually between bandwidth and the resolution of the converter. Higher bandwidth and higher resolution converter design is hence of great interest.

In high resolution DACs, segmented DACs are vastly studied to optimize for area and performance. Current steering segmented DACs are an attractive option for high speed applications as the current cell is always on and the current is steered to the required output of the DAC depending upon the input code, as will be seen in Chapter 4. But for high resolution designs, non-linearity due to code dependent output impedance becomes a limiting factor, leading us to explore other possible DAC architectures.

The next obvious choice for DAC design are the resistive ladder architectures. In this work we explore various types of resistive ladder architectures including segmented DACs with binary weighted, thermometer decoded and R-2R resistive ladder designs. A resistive DAC unlike its current steering counterpart needs a I-V amplifier to convert the DAC current into an appropriate output voltage. And this amplifier has strong re-

quirements of linearity and bandwidth.In this work we design a two stage feedforward amplifier with high gain and bandwidth to obtain I-V conversion of the DAC output.

The thesis is organized as follows:

Chapter 2 discusses the basics of Digital to Analog Converters and some design considerations.

Chapter 3 discusses the design of digital parts of the DAC,the decoder and latch.

Chapter 4 discusses the Current Steering DAC design and corresponding simulation results.

Chapter 5 discusses the Resistive DAC design and corresponding simulation results.

Chapter 6 compares the performance of the Current steering DAC with the Resistive DAC.

Chapter 7 presents the conclusions.

CHAPTER 2

Digital to Analog Converter Basics

2.1 Non-linearity in DACs

The linearity of a DAC can be characterized by both its static as well as dynamic performances. Static performance is taken at the steady state just before a clock transition, after all the transients settle down. Dynamic performance is characterized by the DAC's frequency response to single or multi tone inputs and accounts for transient behavior, glitches due to clock transitions, etc.

2.1.1 Static Non-Linearity- DNL/INL

Differential Non-Linearity

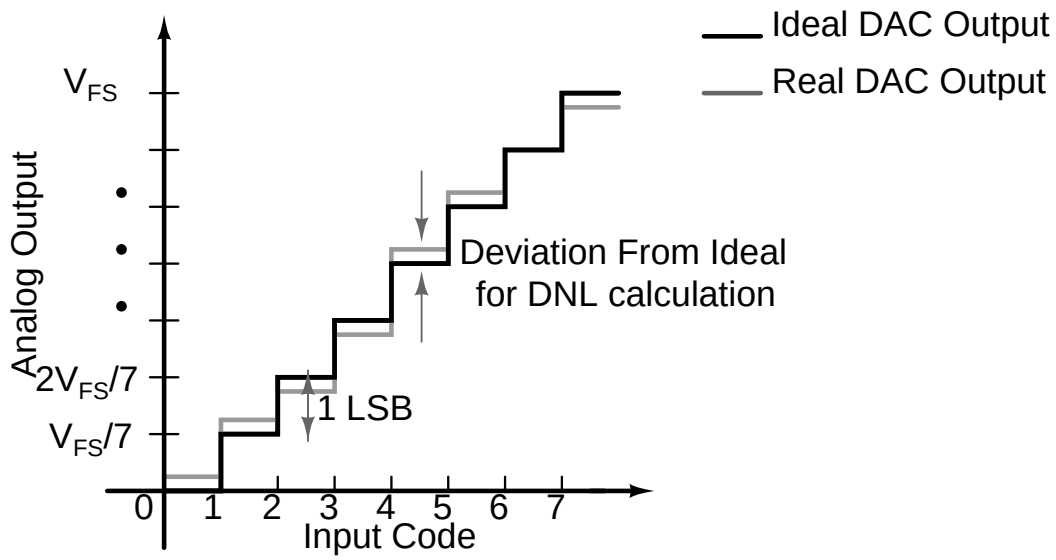

Figure 2.1: Differential Non-Linearity in a 3 bit DAC

DNL is a measure of deviation in the voltage output of two adjacent digital input values of a DAC.

$DNL = \frac{V(k)-V(k-1)-LSB}{LSB}$, where$V(k)$is the output voltage corresponding to the kth input digital code and LSB being the smallest possible value of the DAC output.

Integral Non-Linearity

INL is a running sum of the DNL of a DAC. It gives the deviation of the analog output from the ideal straight line. To compensate for gain and offset errors, the output waveform is fitted to a straight line using end point fit or best fit and then the INL calculated.

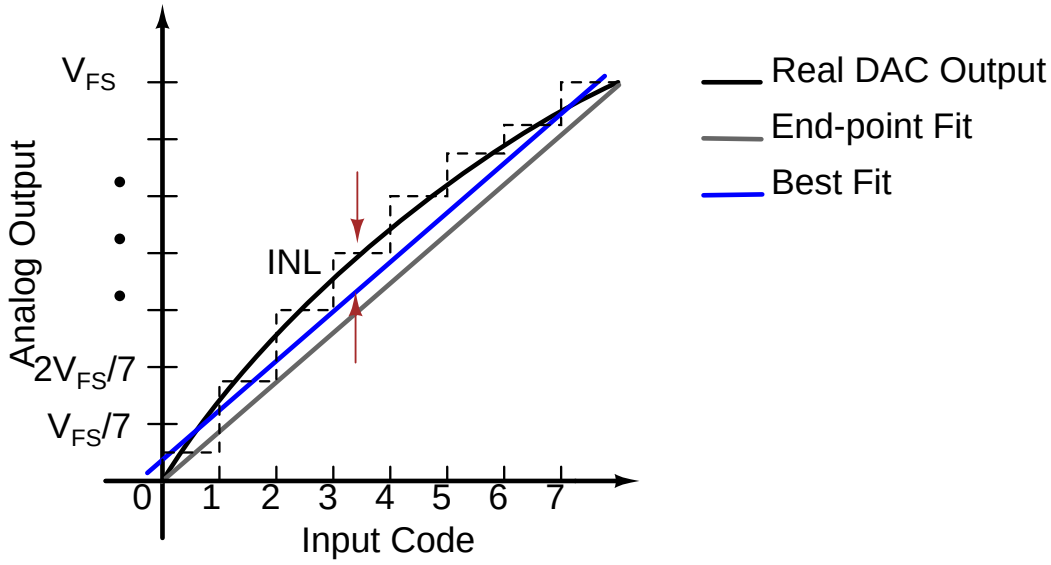

Figure 2.2: Integral Non-Linearity in a DAC

$INL(k) = \frac{\sum_{i=0}^{i=k-1} W_i - kLSB}{1LSB}$, where $W_i = V(i) - V(i-1)$

2.1.2 Dynamic Non-Linearities - SFDR, IM Distortion

The frequency spectrum of the DAC is analyzed to determine the dynamic performance.

Spurious Free Dynamic Range

SFDR is one of the measures of the dynamic performance of the DAC. When an input of a single frequency is given to an ADC which feeds the corresponding digital signal to the DAC, the output of the DAC, which is just a quantized version of the input sinusoid, should contain only the input tone $f_{in}$and tones at $nf_s \pm f_{in}$ due to sampling. Hence in

the signal band, only the f_{in}tone should be present. But in case of a real DAC, along with f_{in}, other spurious tones can be present between 0 and $f_s/2$. Hence the linearity of the DAC in terms of SFDR is given as the difference between the power of the input signal and the largest spur within the bandwidth of the DAC.

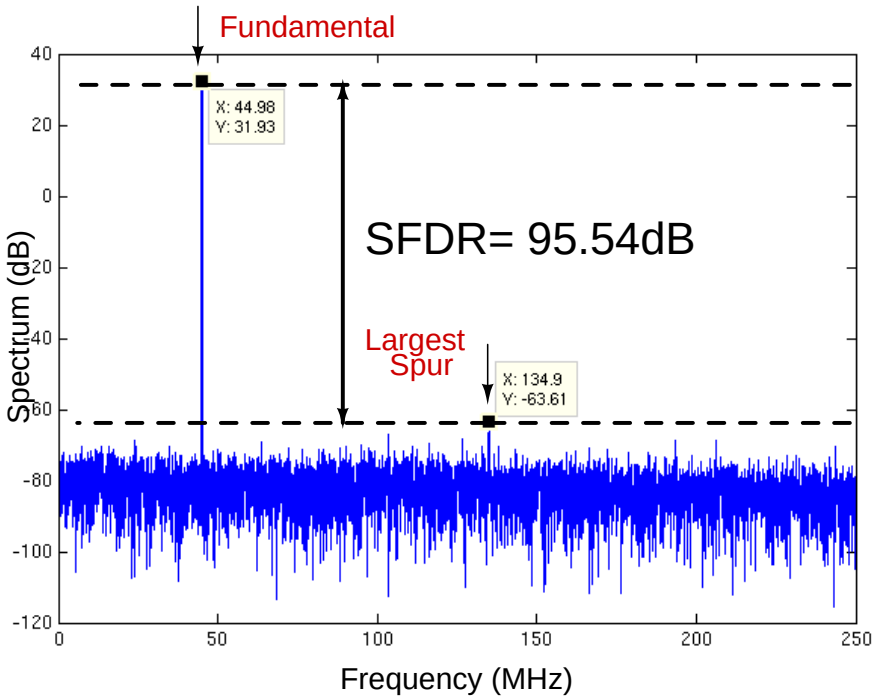

Figure 2.3: SFDR Example

Intermodulation Distortion

Another measure of linearity of the DAC is its ability to reject stray signals within the signal band. For this, a closely spaced two tone input (at frequencies f_1 and f_2) is fed to the DAC and the DAC spectrum is observed. For a perfectly linear system, the output spectrum should consist only of the two input tones. But for any real system, due to non-linearity, intermodulation frequencies are seen at $f_1 - f_2$, $f_2 - f_1$, $2f_1 - f_2$, $2f_2 - f_1$, and so on. The power of these intermodulation tones should be much smaller than the input fundamental tones in order to efficiently retrieve the required input frequency in the output.

For a fully differential DAC, as only odd order harmonics exist, a good figure of linearity is the third order intermodulation component, or IM3 which is the difference

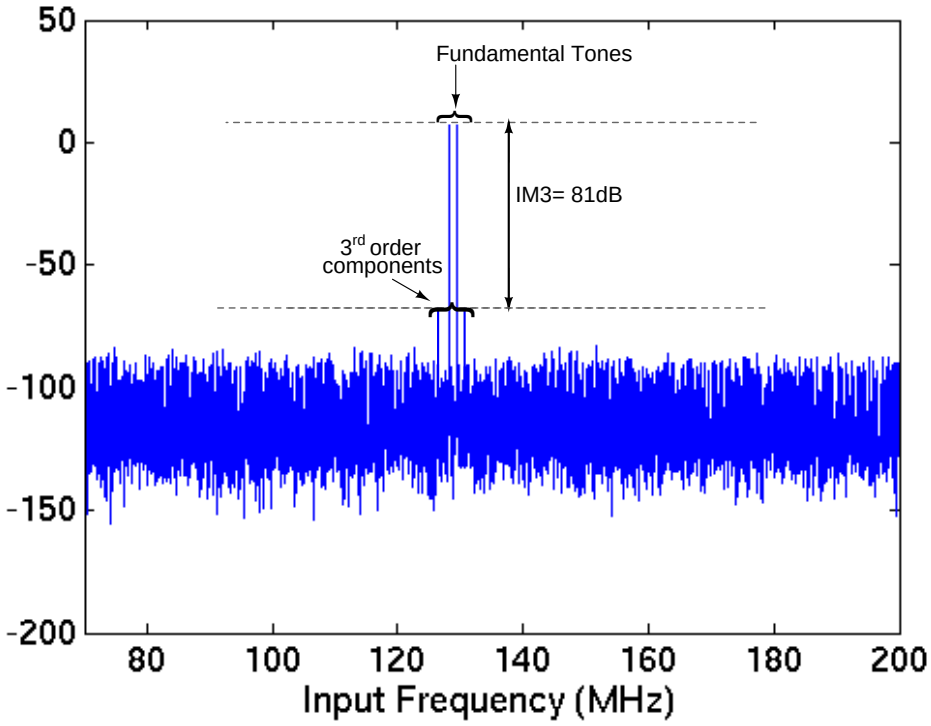

Figure 2.4: Intermodulation Distortion Example

in powers of the fundamental tones and the 3rd order intermodulation frequencies, that is between f_1 or f_2 and $2f_1 - f_2$ or $2f_2 - f_1$.

2.2 Types of Digital to Analog Converters

2.2.1 Binary Weighted DAC

In this DAC architecture, all current sources are binary weighted, that is, each subsequent current source is twice the previous current source. Hence an N bit DAC requires only N scaled current sources.

Worst case DNL is at major code transition, that is, the input digital code changes from 0111... to 1000...

Hence for an N bit binary weighted DAC, Maximum DNL is $\sqrt{2^N - 1}\sigma_I$,where σ_I is the standard deviation of a unit current source.

A binary weighted DAC does not need any separate decoder to generate the switch-

ing signals. The N input bits can directly function as switching signals for the N current branched in a binary weighted DAC.

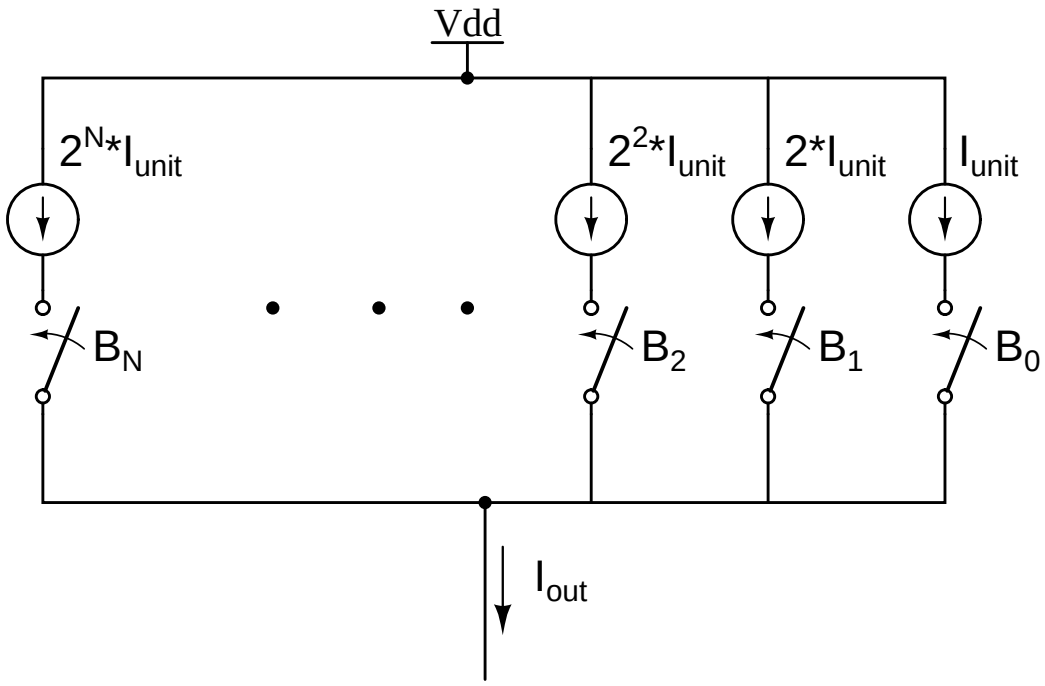

Figure 2.5: N bit Binary Weighted DAC

2.2.2 Thermometer DAC

In a thermometer coded DAC, all current sources are unit current sources and are of equal value. Hence for a N bit DAC, we need $2^N - 1$ current sources. In order to generate switching signals for a thermometer DAC, a N to $2^N - 1$ binary to thermometer decoder is required. For high resolution thermometer DACs this decoder area becomes very large and a tradeoff is considered between the decoder area and static non-linearity in segmented DACs to optimize the DAC area.

DNL for a Thermometer DAC is only σ_I as only one unit current source is switched on at every code transition.

INL for both binary weighted and thermometer DAC is the same since it depends only on the area of all the current sources. Maximum INL is at the last code of the DAC, that is at full scale, and is $\sqrt{2^{N-1}}\sigma_I$.

A segmented architecture of 6 thermometer MSB bits and 6 binary weighted LSB

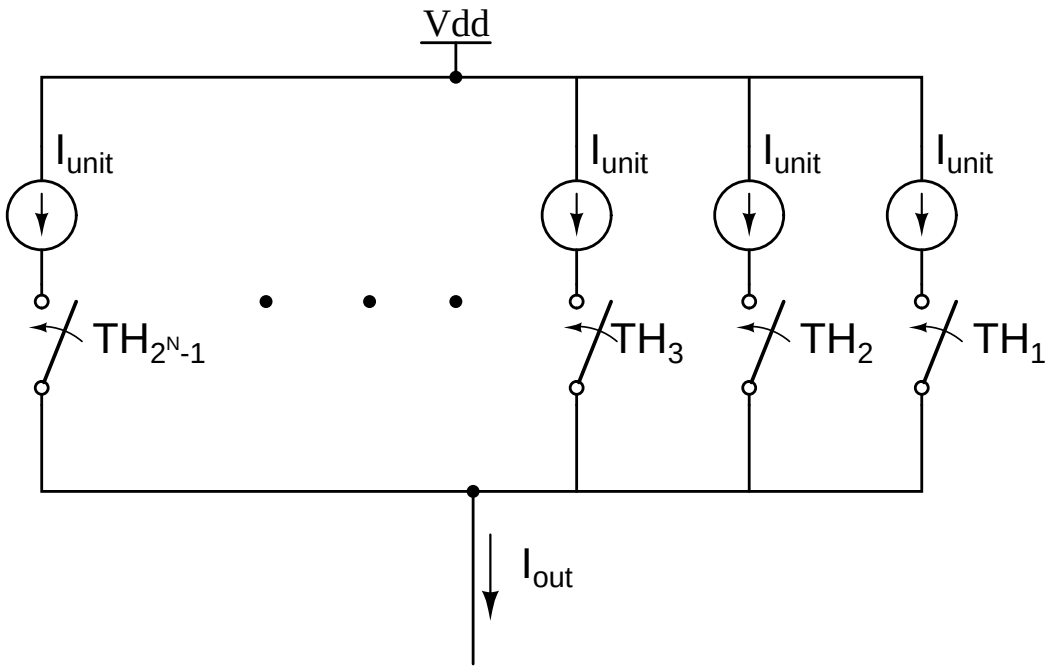

Figure 2.6: N bit Thermometer DAC

bits is considered to optimize between decoder area and desired static non-linearity.[1]

2.3 DAC Simulation Setup

2.3.1 Transient simulation duration

As our design is a 12 bit DAC, for any measurement becomes a good measure of the system only when all 4096 DAC codes are sampled in the DAC waveform. In our case, when we perform SFDR simulations, a transient of the DAC output is taken for a number of cycles in order to make sure that all the 4096 codes are sampled in the DAC output waveform. Exact time interval of simulation is estimated using a Matlab simulation that counts all the codes sampled in a DAC output signal for various frequencies in the signal band. For a transient signal of 34us all 4096 codes are observed to be sampled for all input frequencies within the signal band.

2.3.2 FFT considerations for SFDR and IM3

Spectral leakage is an important concept when FFTs of waveforms are taken to study the frequency performance of a system. DAC dynamic performance is measured in terms of the spurious free dynamic range and the intermodulation distortion. Both these require taking a Fourier transform of an appropriately sampled transient signal of the DAC output.

For an N point FFT, input frequency should be taken as follows

$$f_{in} = \frac{k}{N} * f_s \tag{2.1}$$

where f_s is the sampling frequency of the DAC. In the FFT, each bin width is $\frac{f_s}{N}$. If the input is not on a bin, that is $\frac{f_{in}}{f_s} \neq \frac{k}{N}$, the discrete Fourier series for a rectangular window will have non-zero coefficients at frequencies other than the fundamental at f_{in} and this is called spectral leakage. To avoid spectral leakage, the input frequency should be on a bin, that is, f_{in} should be of the form in equation 2.1, where k and N are co-prime numbers.

Hence for determining the SFDR and IM3 of the DAC output waveform, the input frequency is taken such that it lies on a bin for our sampling frequency of 500MHz, to ensure no spectral leakage is present.

2.3.3 Anti-image filter

The output waveform of a DAC can be seen as a sample and hold version of the input waveform in a ADC-DAC setup. Hence for a sampling frequency of f_s, the output spectrum of a DAC will contain the fundamental frequency f_{in}, and images at $nf_s \pm f_{in}$. In order to observe the spectrum beyond the sampling frequency, the DAC output waveform is usually sampled at a frequency higher than f_s. In our case, we sample the output waveform at $32f_s$ to plot the FFT. Hence to observe a clean spectrum within the signal band and avoid tones around the sampling frequency from folding back into the signal band, we use a low pass image rejection filter at the output of the DAC. An 8th order, 1.25GHz cutoff analog filter is implemented using a verilog block with

coefficients generated in Matlab, for this purpose.

2.3.4 Improving simulation speed : VerilogA modeling

Transient simulation for 35us for a 12 bit current steering DAC design with around 2000 transistors takes almost a day to simulate. This results in lot of time being taken just for the simulation before the analysis of the results. Hence other methods are explored to improve the speed of the simulation yet achieve good accuracy with respect to the original circuit.

All Digital blocks are replaced with their verilog equivalents taking into account the real delays and rise/fall times. It is seen than the simulation time reduces by more than half and also the SFDR values obtained differ by less than 1dB. The full transistor level simulation SFDR values are seen to be slightly higher than the values simulated using SFDR blocks.

Table 2.1: Fast Simulation and Full Simulation SFDR (dB) comparison

Frequency (MHz)	Fast simulation	Full Simulation
1.862	82.34	83.72
9.674	55.92	56.71
49.35	46.23	46.84
92.07	43.07	42.2

CHAPTER 3

Digital Part Design: Decoder & Latch

3.1 Binary to Thermometer Decoder

The switching signals for the binary weighted DAC can be given directly from the digital code. It requires no decoding. On the other hand, thermometer DAC needs a decoder before the input digital code can be fed in as switching signals. For an N bit thermometer DAC, there exist $2^N - 1$ unit current cells and the the N input bits need to be converted to these $2^N - 1$ switching signals. In our design, the 6 MSB bits are thermometer decoded. Hence we need a 6 to 63 binary to thermometer decoder to generate the corresponding thermometer DAC switching signals. For better matching and simplicity of the digital design, the 6 to 63 binary to thermometer decoder is implemented as an 8x8 matrix, row-column decoder and two 3 to 7 binary to thermometer decoders as described in [2].

The 3 to 7 binary to thermometer decoder is implemented as seen in the Figure 3.1. The decoder truth table is seen in Table 3.1. Subsequently, the row-column decoder is implemented as follows and the complementary select signals are generated as seen in Figure 3.2.

Table 3.1: 3 bit binary to thermometer decoder

Binary code	Thermometer code
000	0000000
001	0000001
010	0000011
011	0000111
100	0001111
101	0011111
110	0111111
111	1111111

The 6 MSB bits are thermometer decoded using the following decoding logic. The 6 input bits are first divided into two groups of 3 bits each (Upper MSB bits and Lower

MSB bits). Each of these UMSB and LMSB bits are thermometer decoded to 7 row lines and 7 column lines which drive a 63 cell array, which gives the switching signals to the 63 thermometer current cells.

3.2 Latch Design

The decoded switching signals coming from the 6-63 binary to thermometer decoder as well as the 6LSB bits from the input digital code, are taken as the switching signals for the complete DAC design. But in order to reduce effects of clock delay over the chip, the switching signals are first passed through a latch and then fed to the DAC circuit. But in order to successfully drive the DAC circuit, the latch should be extremely fast, that is, it should react well to the 500MHz sampling frequency, and be synchronized with the clock.

For this application, a C^2MOS latch, whose structure is shown in Figure 3.3, is designed to latch the switching signals. The signals at the output of the latch swing between VDD and GND.

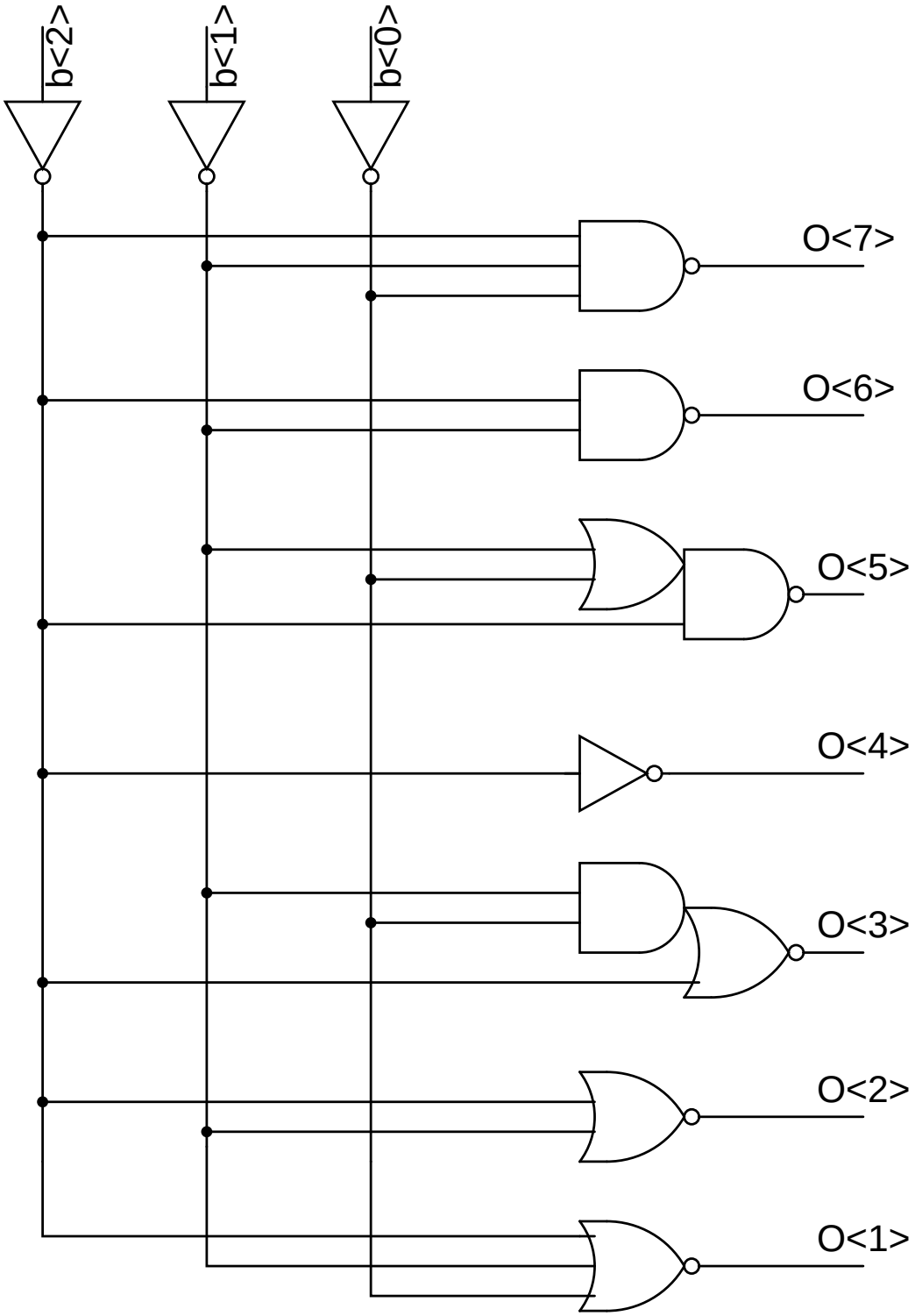

Figure 3.1: 3 to 7 Binary to Thermometer Decoder

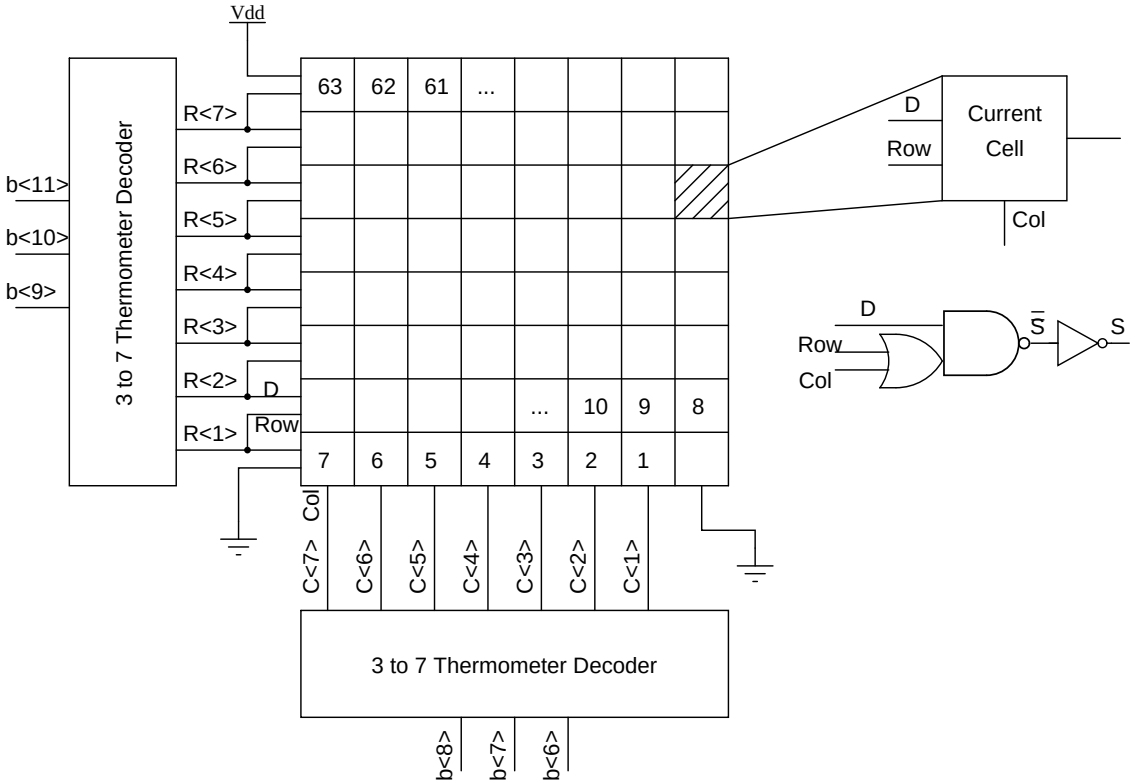

Figure 3.2: Row-Column Decoder

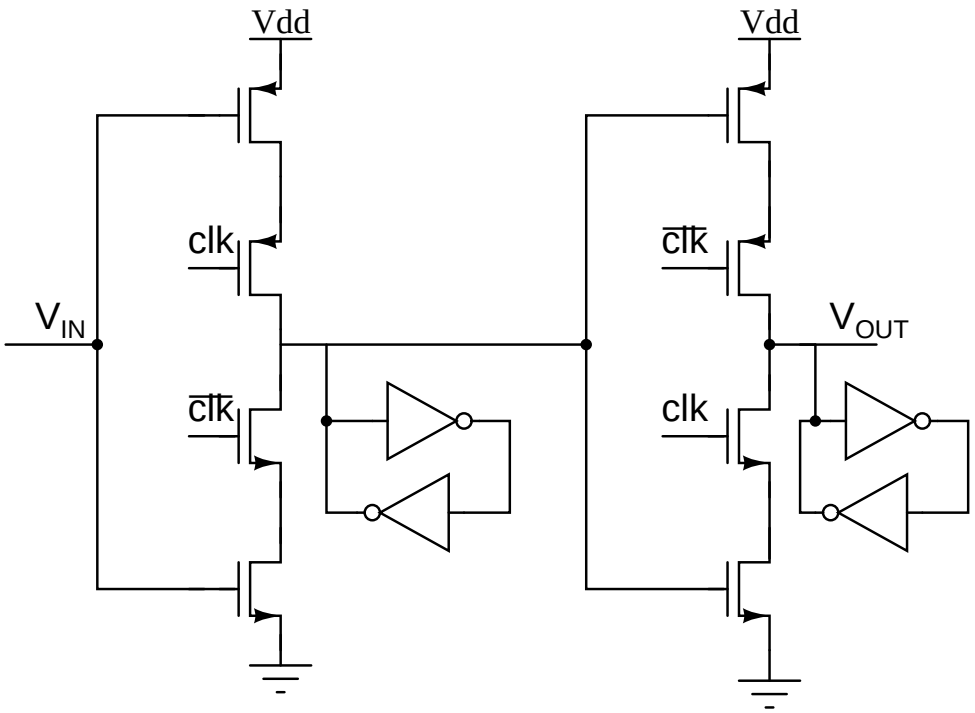

Figure 3.3: C^2MOS Latch

CHAPTER 4

Current Steering DAC Design

4.1 Motivation

Current steering DACs are a vastly studied architecture in DACs. This architecture has an inherent advantage in terms of speed as the current sources are always on and are merely switched from one side to the other. In a current steering DAC, the basic unit of current is a unit current cell, shown in Figure 4.1. M_1 and M_2 form the switch transistors and the switch signals are designed such than only one of the two transistors is on at any time. Hence this steered current flows directly into the load resistor. The complete DAC is made by integrating multiple copies of this current cell, scaled in a binary weighted or thermometer fashion according to the segmentation. DAC output voltage across the load resistor is obtained by appropriately steering the required current into the load on the basis of the input digital code. As our design is targeted at 500MSPS, a current steering DAC architecture is chosen to begin with. As described in section 2.2, a 6+6 Thermometer + Binary Weighted segmentation is selected and the afore mentioned decoder and latches designed, to be used in the DAC design.

4.2 Current Cell Design

4.2.1 Estimating Mismatch parameters

Mismatch equation:

$$WL_{min} = \frac{1}{2(\frac{\sigma_I}{I})^2}[A_\beta^2 + \frac{4A_{Vt}^2}{(V_{GS} - V_T)^2}] \tag{4.1}$$

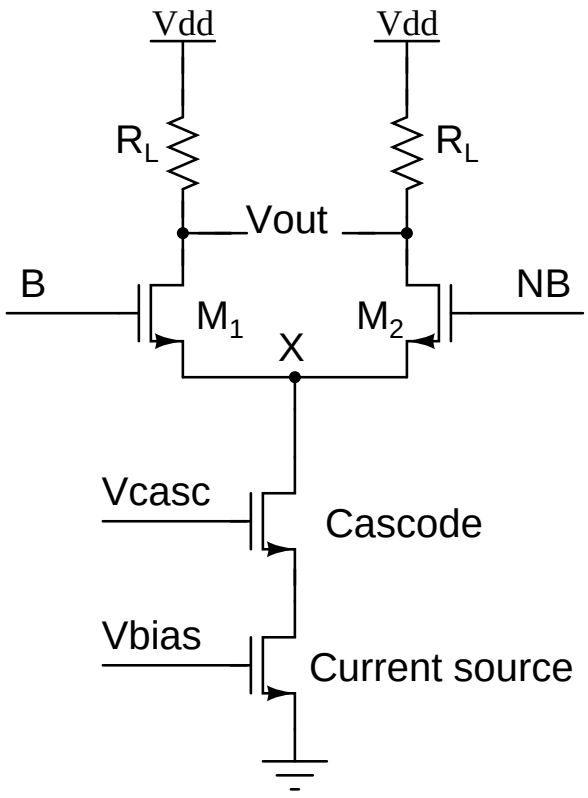

Figure 4.1: Unit current cell

Full scale current constraint:

$$I_{FS} = 2^N \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_T)^2 \tag{4.2}$$

The transistors in the unit current cell are sized according to the equations 4.1 and 4.2.Hence in order to calculate the size of the current source in the unit current cell, we need to know the mismatch parameter A_{Vt} and A_β. Both these parameters depend on the technology. In our case, the design is done in 65nm technology from STMicroelectronics. Hence from the ST65 library, nmos with low V_t and low power is used.

$$A_{Vt} = \frac{\sigma_{V_t}}{\sqrt{WL}} \tag{4.3}$$

Monte Carlo simulations are carried out for 100 runs each for various WL values. Further, $\sigma_{Vt}$is plotted with respect to $\frac{1}{\sqrt{WL}}$.Slope of this straight line gives the mismatch parameter A_{Vt}.

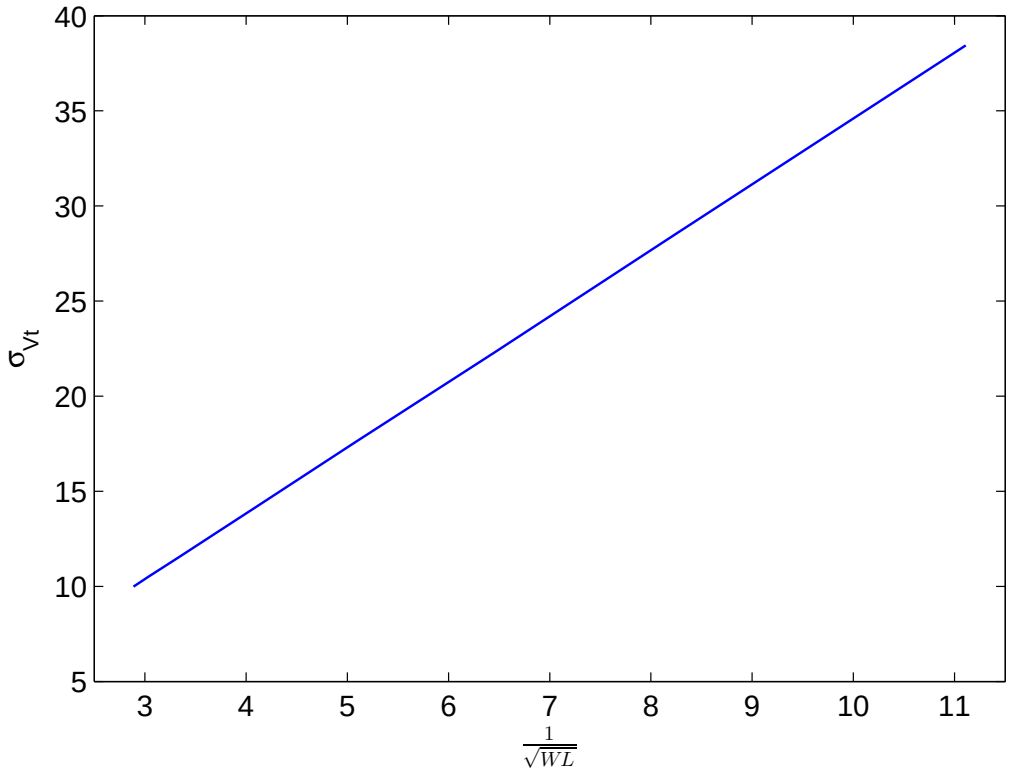

Figure 4.2: Mismatch Parameter estimation

From Figure 4.2, A_{V_t} is obtained as 3.6mV-um and A_β is taken as 0.01 from the transistor documentation.

4.2.2 Cell sizing

The current cell sizes are calculated using two equations, mismatch constraint using INL specifications and full scale current equation.[3]

Mismatch equation: $WL_{min} = \frac{1}{2(\frac{\sigma_I}{I})^2}[A_\beta^2 + \frac{4A_{Vt}^2}{(V_{GS}-V_T)^2}]$

Full scale current constraint: $I_{FS} = 2^N \frac{\mu_n C_{ox}}{2} \frac{W}{L}(V_{GS} - V_T)^2$

Mismatch and INL: $INL = \sqrt{2^{N-1}}\frac{\sigma_I}{I}$, INL specification = 1LSB

Segmentation: 6+6 Thermometer and Binary Weighted

Full scale current = 1mA

Now considering Output Voltage swing as 700mV, for a load resistor of 700Ω, leaves 500mV for the three transistors (switch transistor, cascode transistor and current source). Solving these two equations, taking $V_{gs} - V_{th}$ as 100mV, the size of the current source transistor is found to be 0.987(um)/6.068(um). For the Cascode transistor and Switch transistor, minimum Length is considered and Width found for $V_{gs} - V_{th}$ = 50mV and width adjusted to comply with minimum width requirements.

Cascode Transistor Size= 135(nm)/74.65(nm).

Switch Transistor Size= 135(nm)/74.65(nm).

In order not to push the switch transistors into triode, the switching voltage(B) is kept between 800mV and GND.

Transistors are placed in parallel to obtain higher current cells in the binary weighted and thermometer DACs. Figure 4.3 shows a complete block diagram of the current steering DAC. Here a 2X current cell is obtained by placing two copies of the unit current cell in parallel. Similarly higher current cells are obtained by placing the appropriate number of unit cells in parallel. The switching signals for the binary weighted DAC are fed in directly from the LSB bits through latches, whereas, the switching signals for the thermometer DAC are generated using the 6 to 63 binary to thermometer decoder as seen in Figure 4.3.

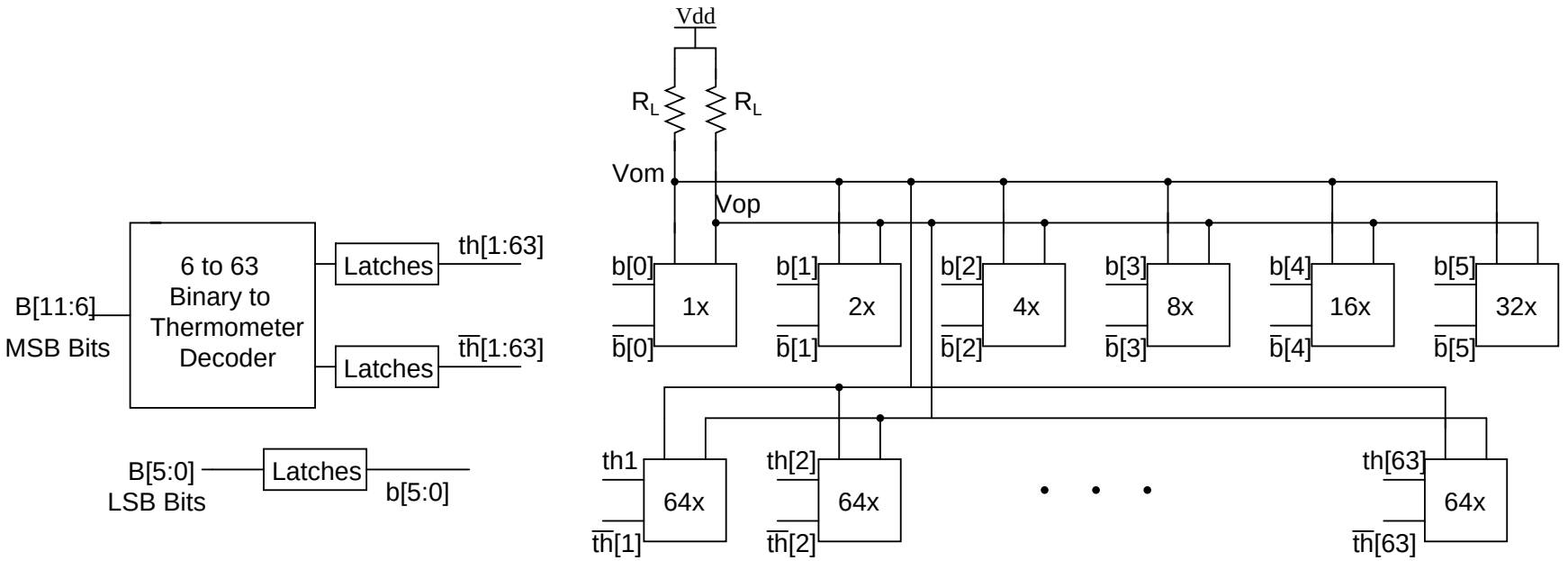

Figure 4.3: Current Steering DAC Block Diagram

4.3 Switching signals and tail node voltage

In a current steering DAC architecture, it is important that all the transistors are in saturation through out operation. This ensures that the output impedance is high and non-linearities are low. Depending upon the point of intersection of the complementary switching signals, the tail node voltage is defined. If the switching signals intersect in the lower half of the voltage range, there is a possibility of both the switch transistors to be momentarily off at the same time. This causes a sudden drop in the voltage of the tail node. This pushes the cascode and current source transistors into linear region momentarily causing transition non-linearities and subsequently causes a glitch in the output voltage. The delay in the switching signals is adjusted such that the switching transitions intersect in the upper half of the voltage transition and all both the transistors are not off at the same time. This reduces the glitch in output at clock transitions and improves the dynamic performance. When the transition voltage is V_{X2} or V_{X3} as seen in Figure 4.4 and 4.5 , the tail node voltage drops suddenly, when both the switch transistors are off. The switch signals are set such that they intersect at $V_{X1}$for the tail node voltage to be stable.

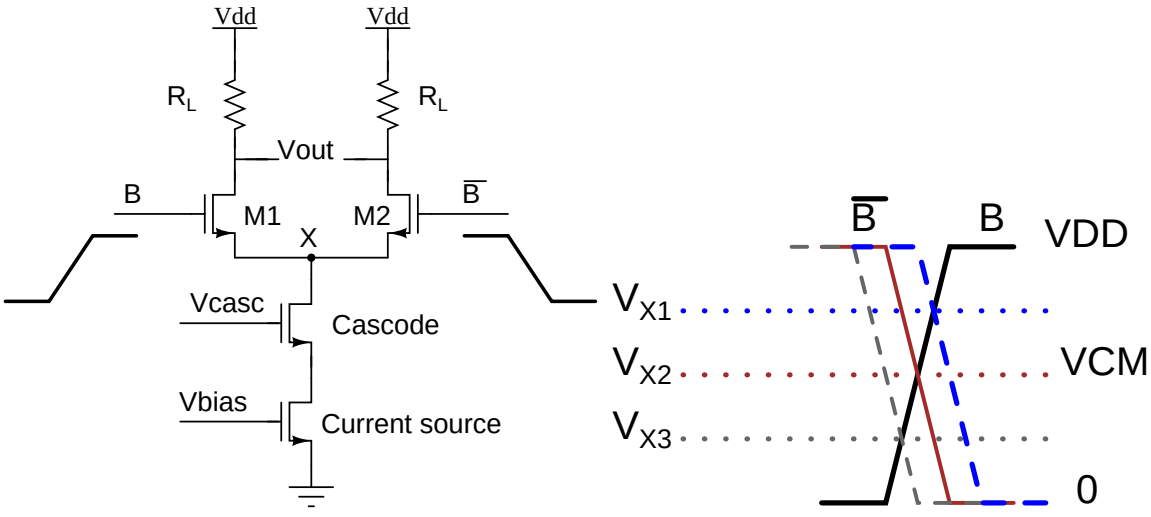

Figure 4.4: Current cell with switch signal transition

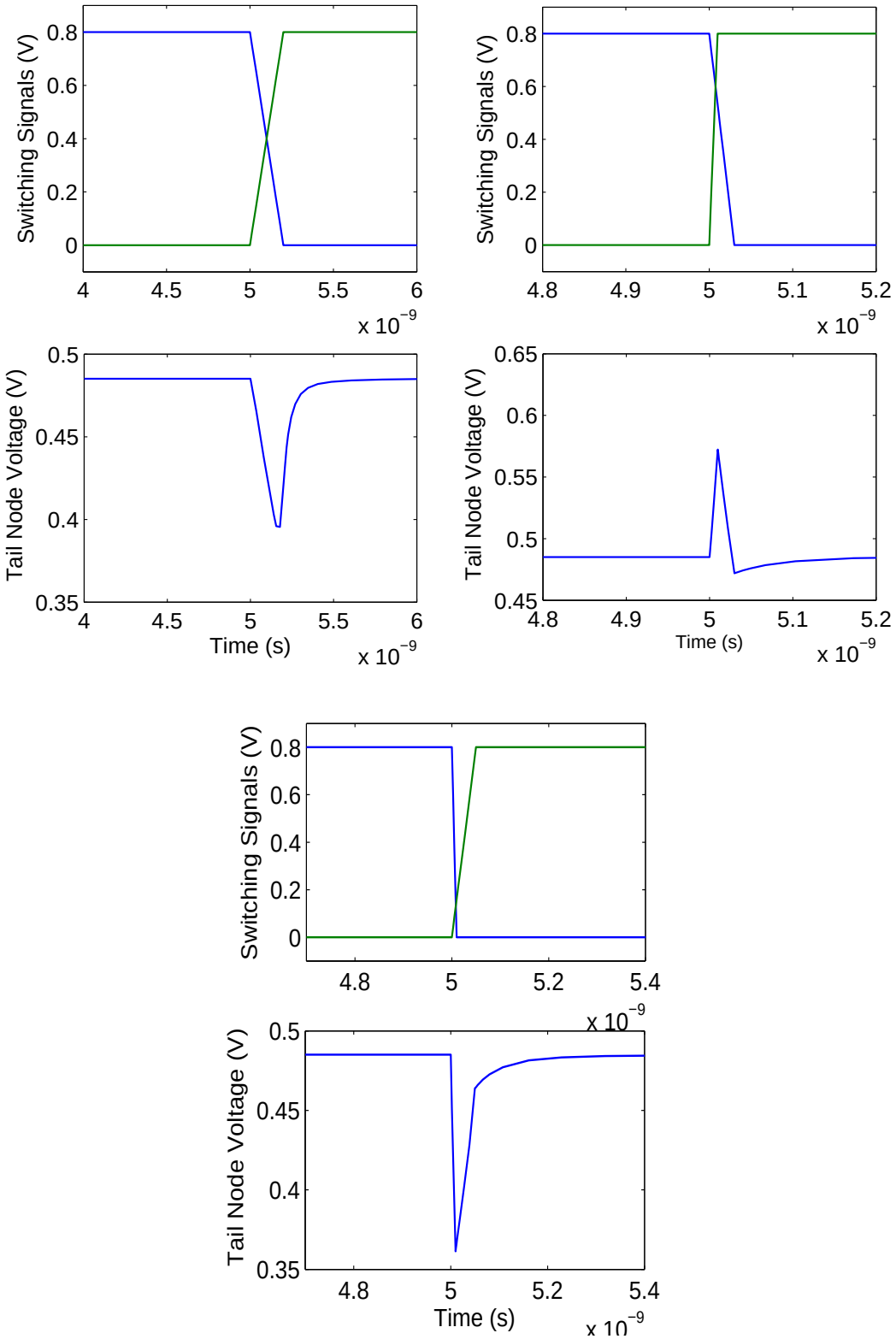

Figure 4.5: Tail node voltage variation with switch signal intersection

4.4 DAC non-linearity estimation

The spectrum of the DAC output for a load of 700Ω is observed to be limited by the third harmonic component. The static behavior of the DAC with frequency in the signal band is described in this section. The steady state value of the DAC output, before every clock transition is considered and the non-linearity estimated using curve fitting. The DAC output obtained for a ramp input plotted with respect to the input code is fitted to a curve of the form $ax + bx^3$, b being the third order coefficient. The input codes 1:4096 are scaled to correspond to 0 to 1.4V for easier correlation to a linear plot of slope 1.

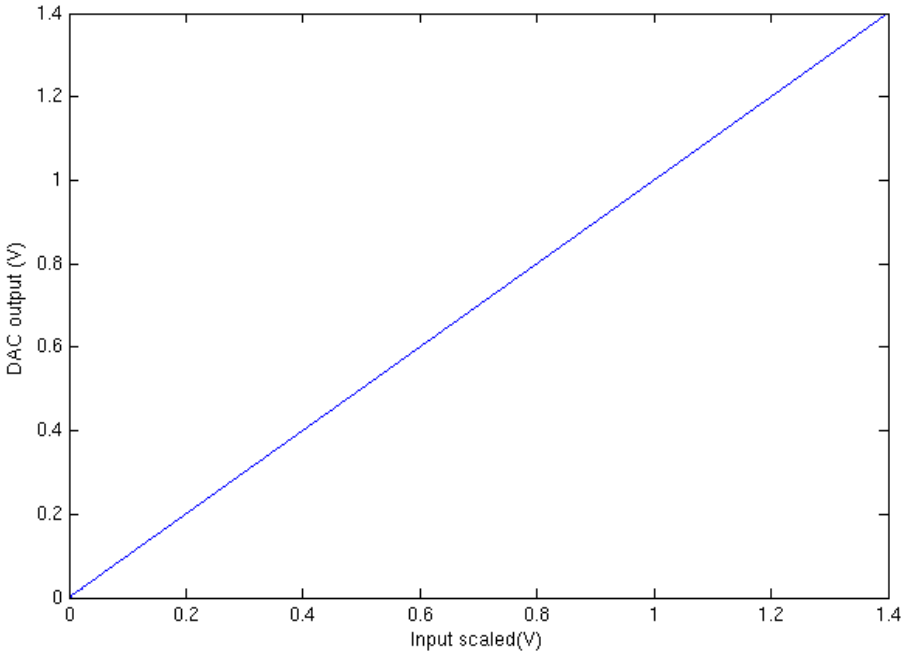

Figure 4.6: DAC output versus input code for a ramp input

The coefficients are obtained as $a = 0.999766$ and $b = -0.000050527$. Using this the distortion expected due to third order non-linearity can be estimated.

When an input of $Acoswt$ is given , the output of the DAC expected would be

$$(aA + \frac{3bA^3}{4})coswt + \frac{bA^3}{4}cos3wt$$

Hence if A is taken as 0.7 in this case, the difference between the fundamental tone and the 3rd order component in dB is 104.16dB. But at high frequencies, SFDR

is observed to fall rapidly suggesting degradation due to finite code dependent output impedance as will be seen later in section 4.5.

Hence to accurately estimate third order component at high frequencies, a sin wave input is given and the DAC output again fitted (compared to the ideal DAC output) to a third order polynomial as above to determine the third order distortion component with high frequencies. It is observed that gradually with increase in input frequency the coefficient of the third order component increases and the third order component limits the SFDR greatly at high frequencies.

Using the above expression, the difference between the fundamental tone and third harmonic component in dB is calculated as

$20log(aA) - 20log(\frac{bA^3}{4})$, where A is the amplitude of the sinusoid, 700mV in this case.

The estimated SFDR using this method is plotted against the input frequency and compared with that of the real DAC obtained, in Figure 4.7. At a frequency of fin=158.264MHz, $a = 1.0084$ and $b = -0.03$ (very large compared to -0.00005 in the ramp case). As frequency increases this third order coefficient b increases further.

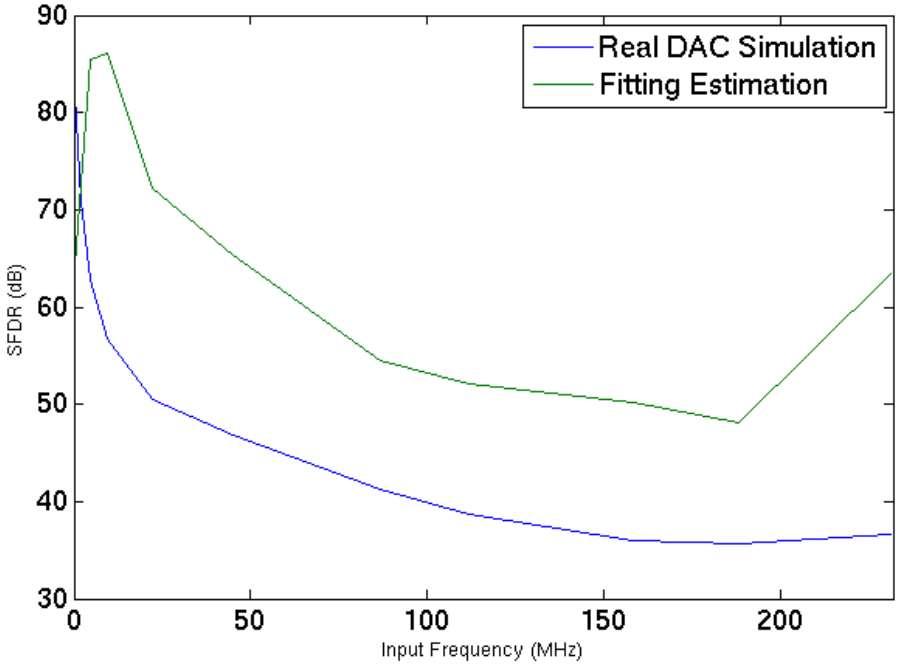

Figure 4.7: Third order component estimation and SFDR

The third order coefficient is observed to become larger with frequency and this is reflected in the SFDR simulations of the DAC suggesting a degradation in static behavior at high frequencies due to finite code dependent output impedance. Degradation of real DAC SFDR with respect to the estimate can be attributed to dynamic behavior and quad switching is tried to improve this, which will be discussed in section 4.6. The static performance of the DAC is improved by reducing the output load but at the cost of output voltage swing.

4.5 Finite Output Impedance

In a current steering DAC, at any point of time, if m current sources are steered to one output terminal, $2^N - m$ current sources are steered to the other output terminal. Due to this, the number of output conductances of the current cells connected to the output nodes varies with the input code. This makes the effective output impedance code dependent and results in non-linearity when the output impedance of the current cell becomes comparable to the load resistance. At higher frequencies the switching capacitance starts introducing non linearity in DAC output, as the output impedance is different when the switch is on and when the switch is off.

At low frequencies, the output impedance is the resistive impedance looking in through the output node. At high frequencies, the drain capacitance of the switch transistors also comes into picture. In order to have minimal effect of this capacitance, the sizes of the switch transistors are kept small at (0.135um/0.075um).

Output Impedance at DC

In a cascoded architecture as in case of our DAC cell, the output impedance is given as $R_{out} = R_{source} * g_{m,casc} R_{casc} * g_{m,1} R_1$, where R_{source} is the drain source impedance of the Current source transistor, $R_{casc}$is the D-S impedance of the cascode transistor and $R_1$is the D-S impedance of the switch transistor. $g_{m,casc}$and $g_{m,1}$are the transconductances of the cascode and switch transistors respectively.

In our DAC design, for a unit current cell with the load resistor of 700Ω, Iu-

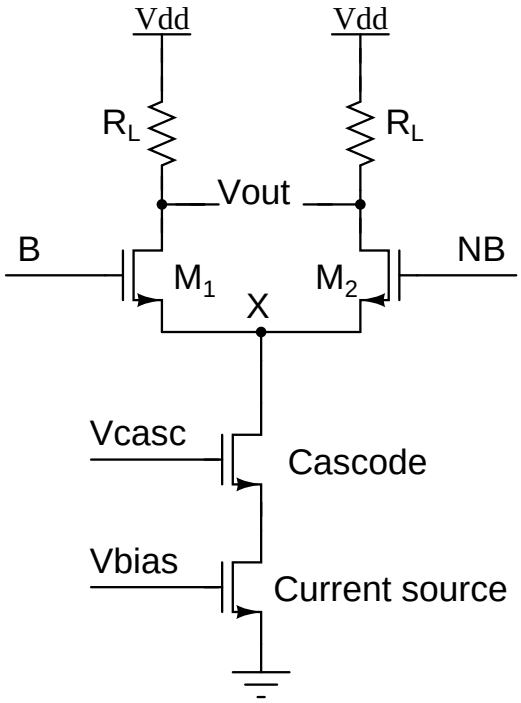

Figure 4.8: Unit Current Cell

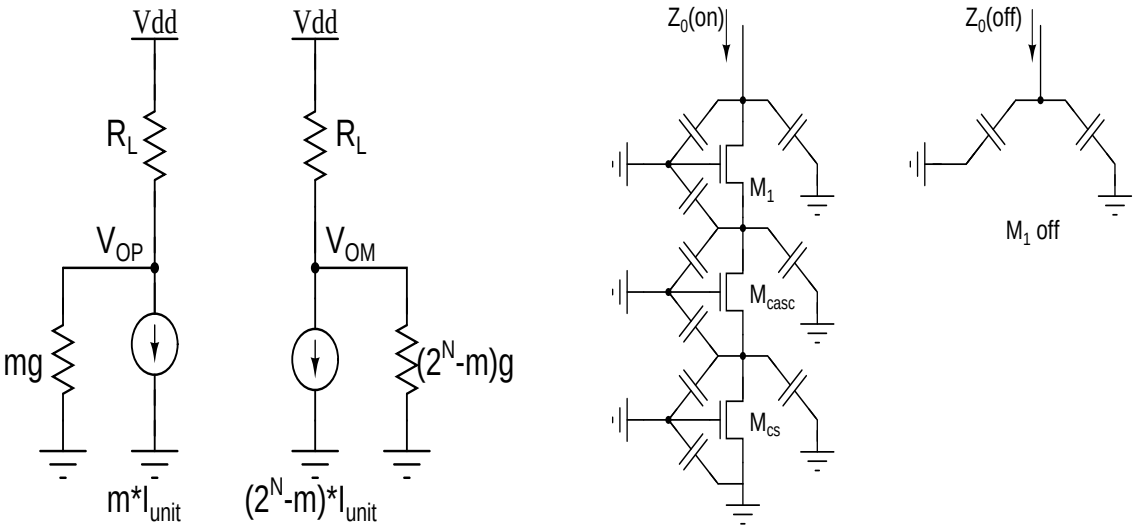

Figure 4.9: Code dependent output impedance

nit=1mA/4096, these values are obtained as

$R_{source} = 5.724M\Omega; g_{m,casc} = 5.153uS; R_{casc} = 3.267M\Omega; g_{m,1} = 5.712uS; R_1 = 3.165M\Omega$

Hence using the above expression, R_{out} is obtained as $1.742G\Omega$

It is seen that R_{out} of a unit current cell is nearly $2.5 * 10^6$ times the Load resistor.

From Figure 4.9[4], ideally when the finite current source impedance is not present,

$$V_{out} = V_{om} - V_{op} = I_{unit} R_L (2^N - m)$$

But due to the presence of the finite output impedance, now V_{op} and V_{om} change and V_{out} becomes

$$V_{out} = V_{om} - V_{op} = \frac{V_{DD} - R_L[(2^N - m)I_{unit}]}{1 + gR_L(2^N - m)} - \frac{V_{DD} - mR_L I_{unit}}{1 + mgR_L}$$

So it can be observed that to get Vout as close to 1 as possible, gR_L should be $\ll 1$. We can define a resistance ratio R_{ratio} as $\frac{R_{CS}}{R_L}$, where $R_{CS}$is the output impedance of the unit current source which is $1/g$ here. Hence for finite output impedance to have little effect on the linearity of the DAC, $R_{ratio} \gg 1$. In our case, $R_{ratio} = 1.742G/700 = 2.5 * 10^6$ which is >>1 and output impedance in the worst case when all the current sources are steered to one side is $1.742G\Omega/4096 = 0.425M\Omega$ and hence the output impedance including the load resistor becomes $698.85\Omega \approx 700\Omega$ at DC.

But as frequency increases, the output impedances of the transistors also vary with frequency and a large degradation is seen in the effective output impedance. Hence the effect of code dependence of output impedance becomes larger at higher frequencies and the SFDR is seen to degrade drastically at frequencies close to Nyquist, 250MHz is our case.

All the current cells are switched to one side to simulate for the worst case output impedance variation with frequency when all the R_{ds} come in parallel with the load resistor. S parameter analysis is run across V_{test} on the circuit,shown in Figure 4.10, and

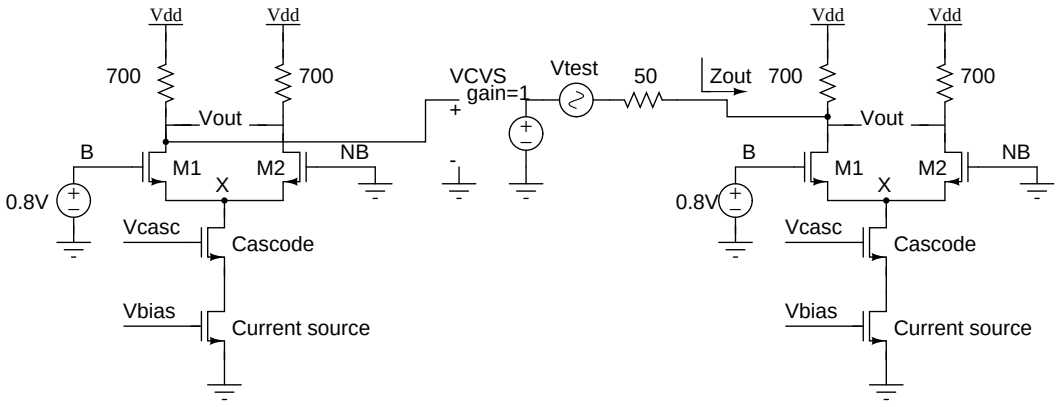

Figure 4.10: Testbench for Output Impedance measurement

the output impedance looking into the current cell plotted with the frequency. Since 4096 current cells are connected to the output nodes, there is a large parasitic capacitance at the output nodes. Hence at higher frequencies, the effect of these non-linearities becomes higher as the effective output impedance reduces with frequency.

Effect of load Resistance Upon reducing the load resistance, as the looking in output impedance of the switch transistors is comparatively larger, the degradation in effective output impedance due to code dependance reduces. This hence improves the linearity of the DAC. But reducing the load resistance to improve DAC linearity is at the cost of output voltage swing. The output voltage swing reduces with reduction in load resistance. As seen in Figures 4.14 and 4.15 , for a load resistor of 700Ω, the effective output impedance degrades from 700Ω to 405Ω for a single cascoded current cell, while for a 250Ω load, the degradation is from 250Ω to 233Ω, which is comparatively much less than the high load case.

The effect of load resistance can be observed in case of the DAC's static performance. The INL of the DAC is observed for both the loads 700Ω and 250Ω. A ramp input is applied and the DAC output waveform is sampled for every code to determine the INL. The differential output is plotted with respect to the input code. A best fit straight line is fitted to the DAC output so plotted to correct for offset and gain errors and INL calculated as

$$INL = \frac{\sum W - kLSB}{1LSB}$$

The DAC step size is 1.4(output swing)/4096. The DAC is designed for an INL of 1 LSB. Figure 4.11 shows the INL for a 700Ω load and it touches 1.25 LSB. On the other hand INL for 250Ω load is less than 0.3 LSB meeting the design requirements.

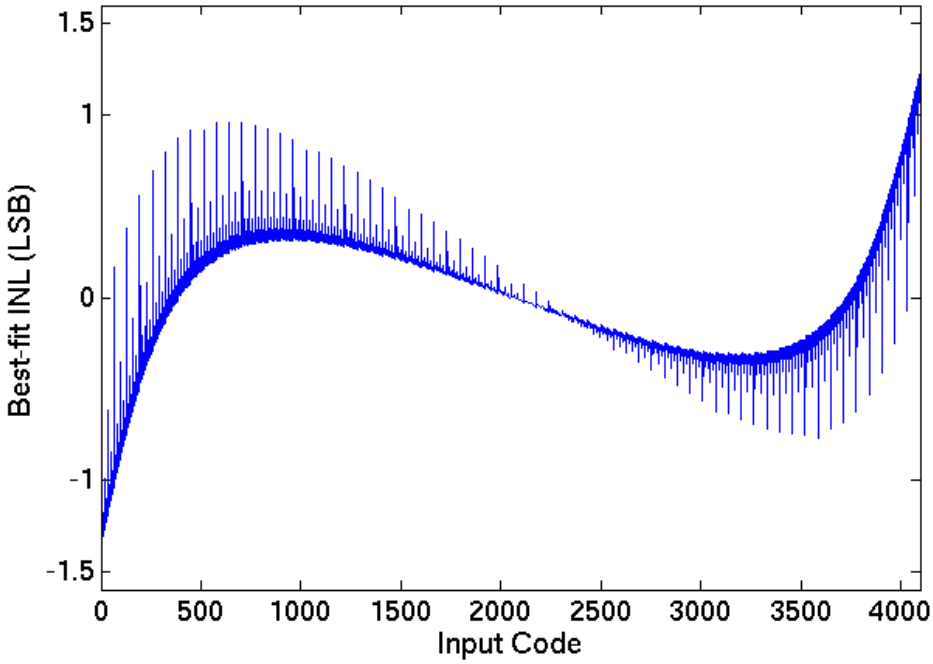

Figure 4.11: Best-fit INL for 700Ω load resistor

Cascoding current cell Cascoding a current cell improves the looking in drain impedance by $g_m r_{ds}$ times. A lower load resistor increases the headroom present for the switch and current source transistors. This can be utilized to double cascode the current cell as seen in Figure 4.13 . Figure 4.15 shows that the degradation in output impedance with frequency reduces on double cascoding. But as impedance degradation is still large, nonlinearity due to code dependent output impedance still dominates at high frequencies. Hence as seen in Figure 4.19, SFDR improvement is not significant.

4.6 Differential Quad Switching

In a conventional current steering DAC, most switches toggle at frequency much less than the clock frequency, depending on the switching signals. Due to this, if any nonlinearity associated with transition is present, the frequency of the spur will lie within

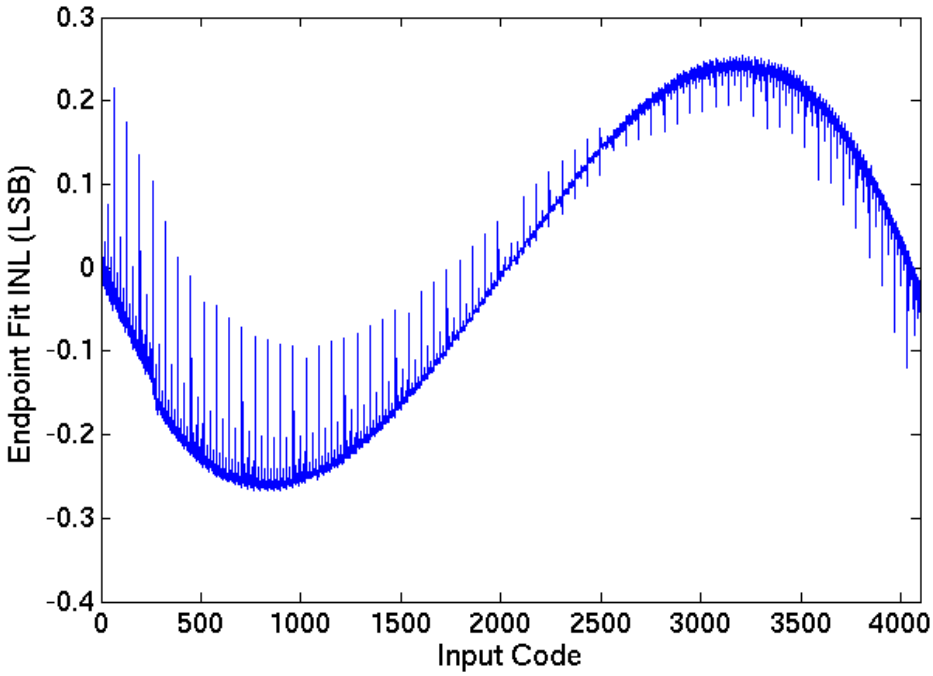

Figure 4.12: Best-fit INL for 250Ω load resistor

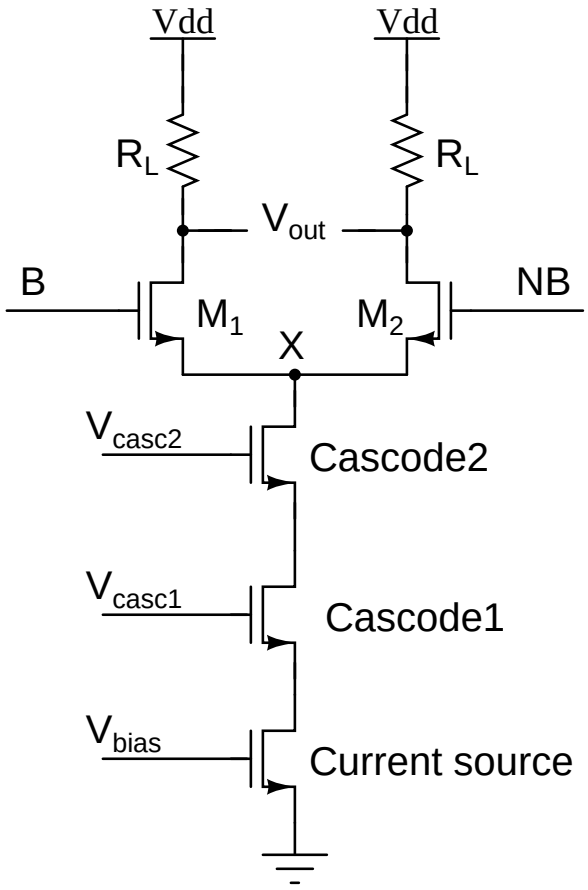

Figure 4.13: Double cascoded current cell

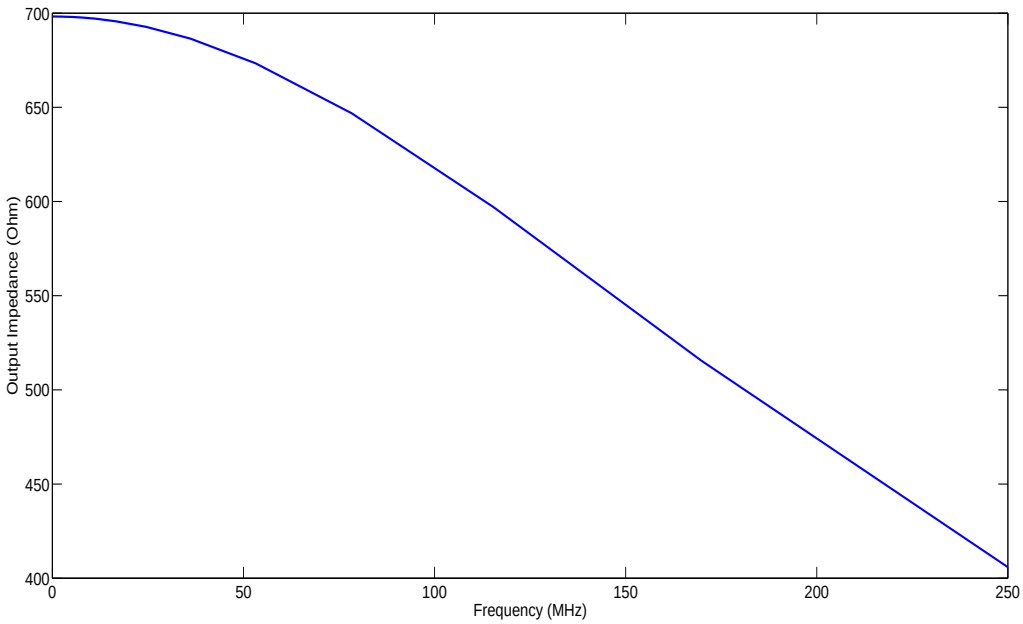

Figure 4.14: Output Impedance with frequency for a load resistor of 700Ω

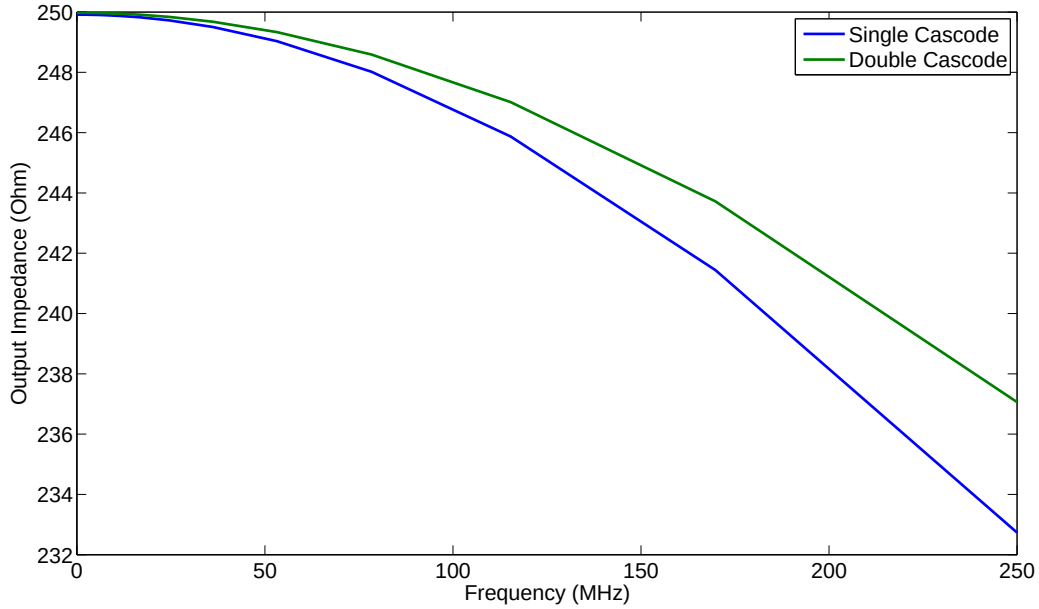

Figure 4.15: Output Impedance with frequency for a load resistor of 250Ω

the signal band. To isolate such behavior from the signal band, differential quad switching is introduced.

Differential Quad switching[5] is a method to improve the dynamic performance of a DAC. Instead of the conventional two switches used to steer current in a current cell, this method incorporates four switches, as shown in Figure 4.16, which switch according to a decoding logic such that, at any clock transition only one of the four switches is on. As one switch toggles at every clock transition, the non-linearity due to transitions will no longer be in the signal band but at the clock frequency, that is, double the signal band frequency.

But quad switching has twice the number of transistors connected to each output node in comparison with a conventional switch design. This introduces a large capacitance at the output node and hence degradation in the output impedance with frequency is observed as seen in Figure 4.16 and 4.17. This causes higher effect of non-linearity due to code dependent output impedance at frequencies close to Nyquist, suggesting that differential quad switching does not help improve frequency performance in our design.

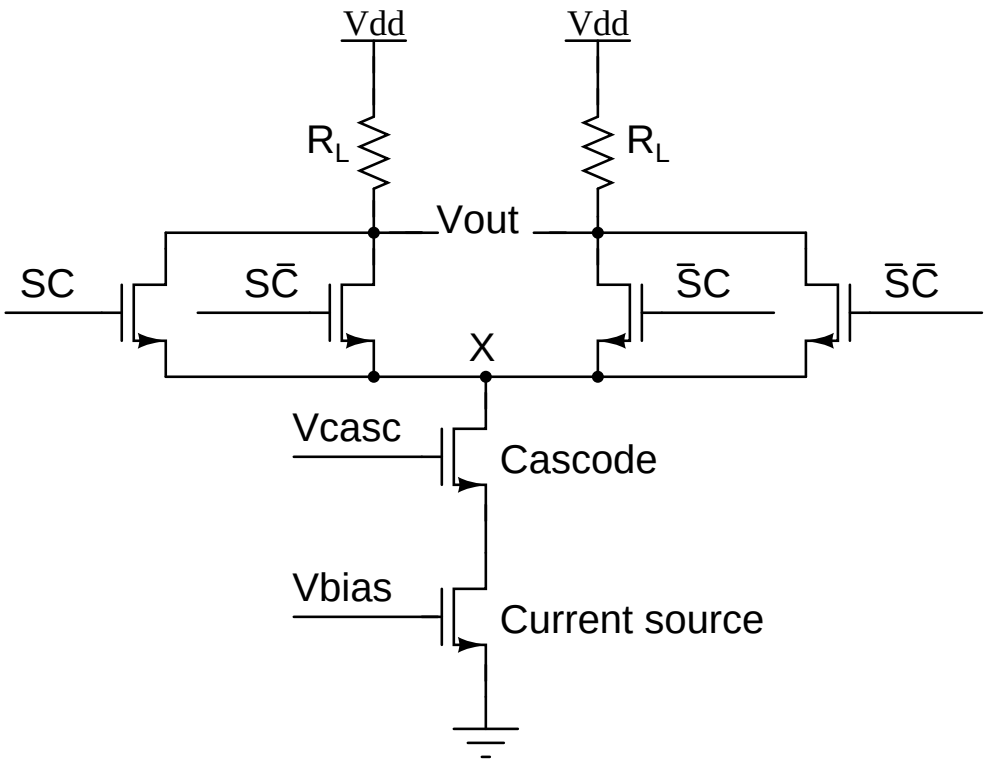

Figure 4.16: Current cell with differential quad switching

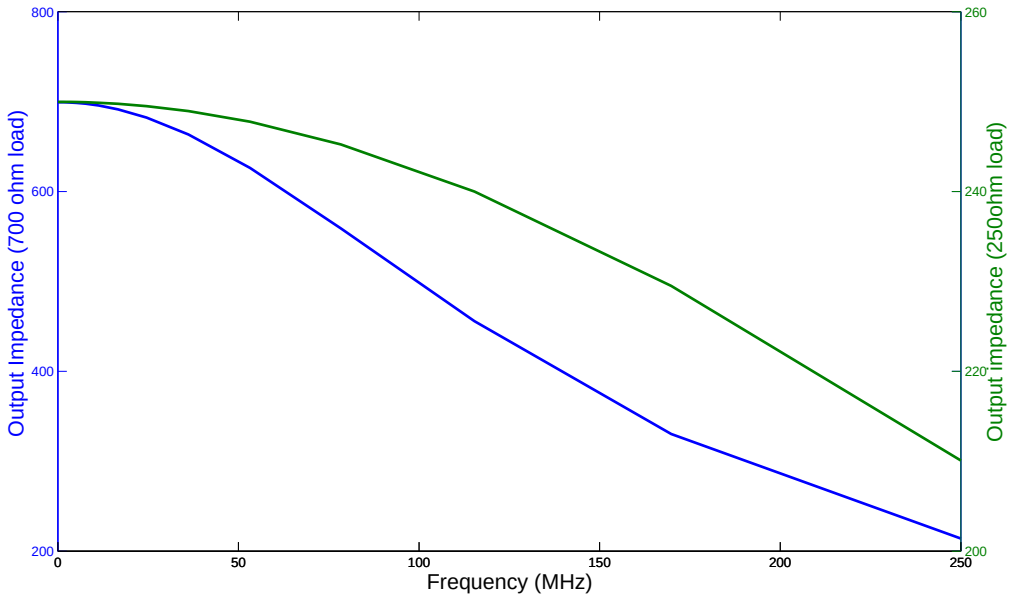

Figure 4.17: Output Impedance with frequency in a current cell with differential quad switching

4.7 SFDR Comparison

A 34us long transient simulation of the DAC output is done. The output signal transient signal is sampled at $32f_s$ and a 524288 point FFT is taken. The input frequencies are placed on bins to avoid spectral leakage, as discussed in section 2.3.2.

Figure 4.18 shows a comparison in the SFDR with different load resistors and single cascoding in current cell, in comparison with ideal DAC SFDR. As discussed in section 4.5, reducing the load resistor reduces the effect of non-linearities due to finite code dependent output impedance and subsequently, the SFDR of the DAC output improves. For a 250Ω load resistor, the SFDR start from close to 85dB at low frequencies and falls to less than 50dB close to Nyquist frequency.

In Figure 4.19, we can see the effect of double cascoding the current source. Double cascoding marginally improves the SFDR due to increase in output impedance. But degradation is still present due to code output impedance. Best case scenario in SFDR is observed for a load resistor of 50Ω with a double cascoded current source, at the cost of having only 100mV-PP swing at the output. In this case, the SFDR at Nyquist frequency is around 70dB, which is more than 30dB higher than the 700Ω load case.

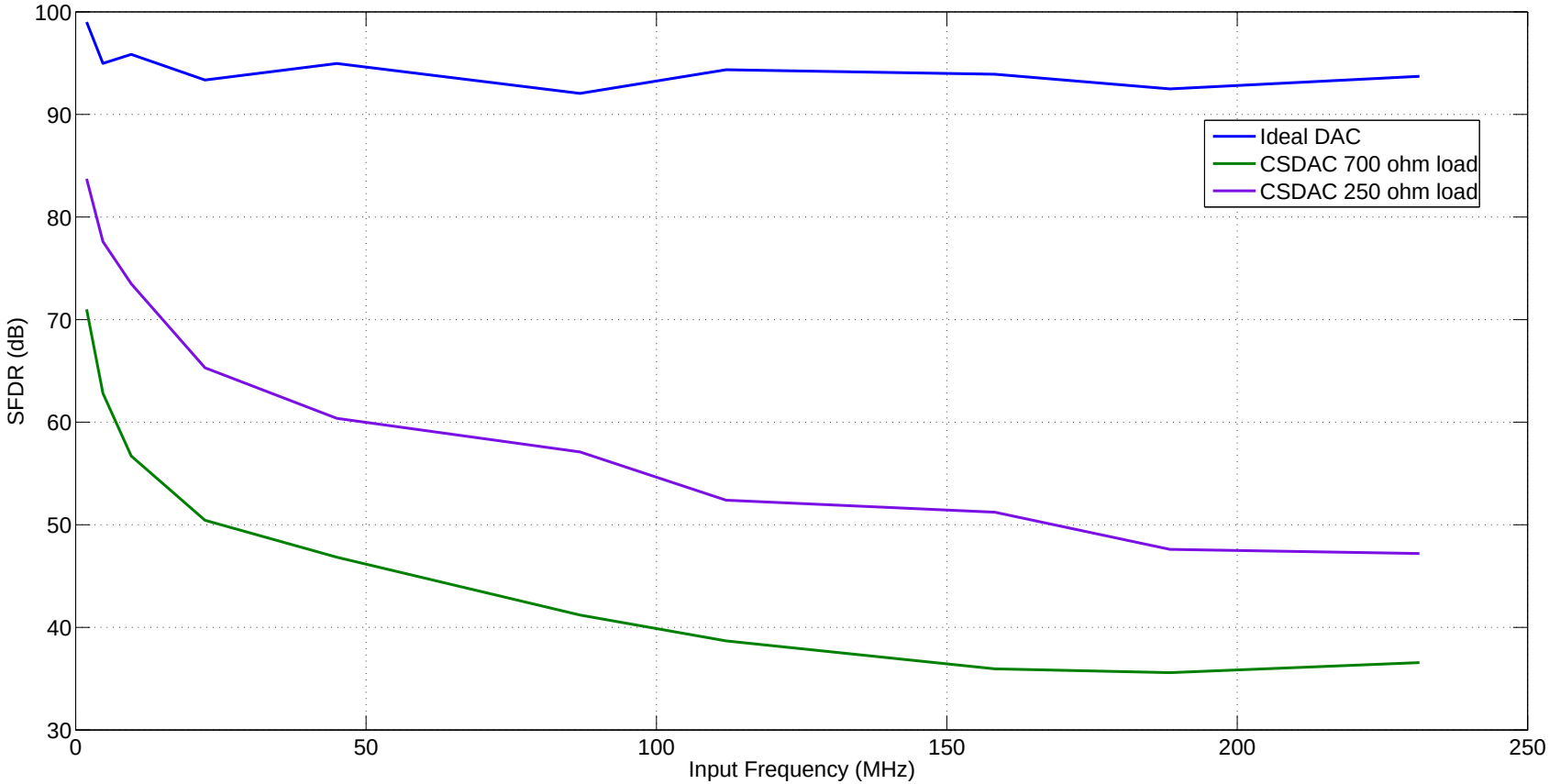

Figure 4.18: SFDR comparison with varying load resistors

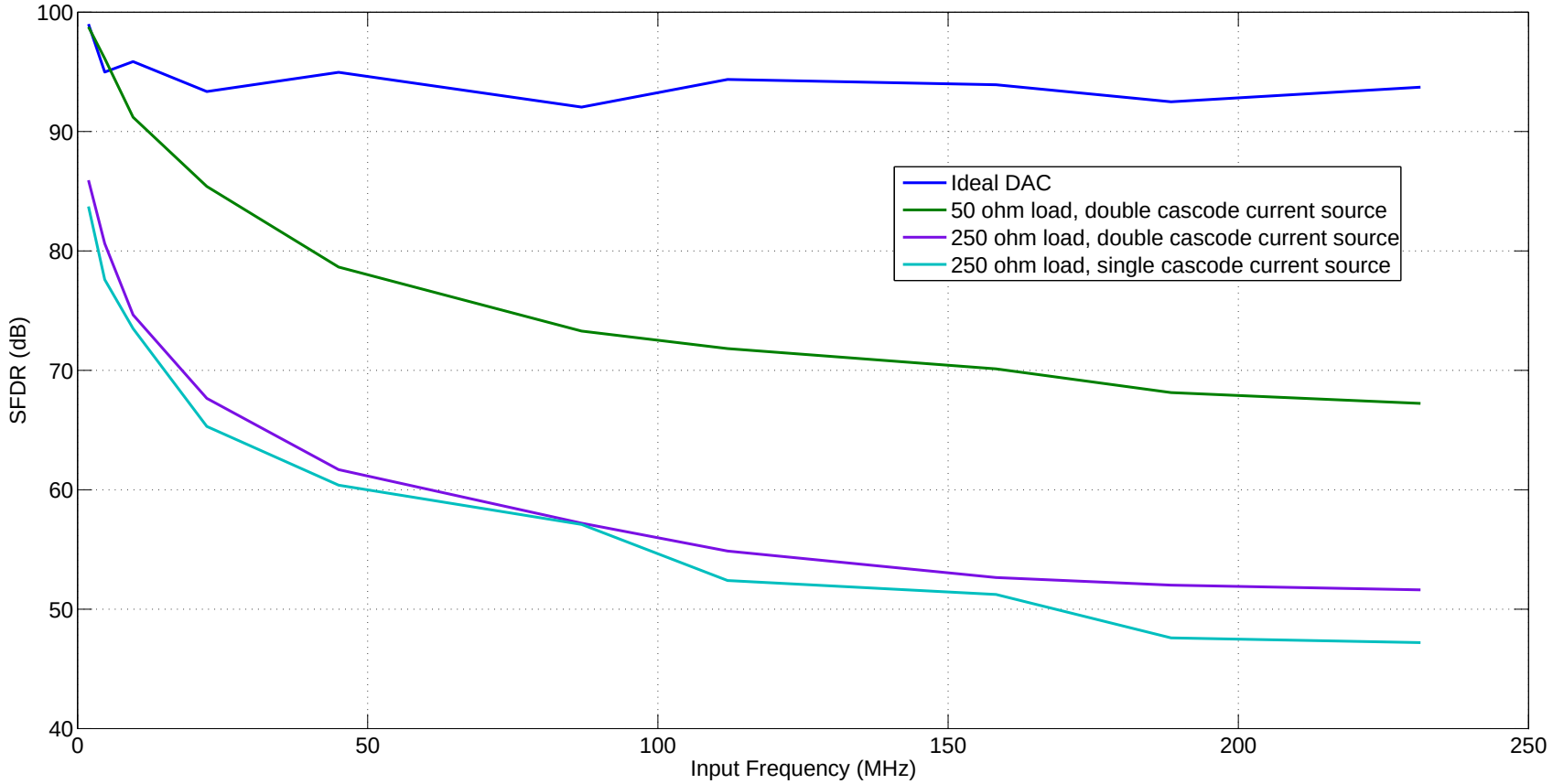

Figure 4.19: SFDR comparison with single and double cascoded current cells

CHAPTER 5

Resistive DAC Design

5.1 Motivation

The current steering DAC design for high speed applications in 65nm technology faces a bottle neck in terms of the non-linearity due to finite code dependent output impedance. The SFDR is observed to start at 90dB at frequencies less than 1MHz and gradually falls to 50dB close to Nyquist for a 500mVPP output swing. This calls for exploring other DAC architectures which can give better frequency performance at frequencies close to Nyquist. As resistive ladder architectures are better compared to current steering architectures in terms of not having the issue of code dependent output impedance, they are explored in this section and compared in terms of static and dynamic performances of the DACs.

5.2 Architecture

Continuing with the current steering DAC segmentation, the resistive DAC is initially implemented as a 6+6 Thermometer + Binary-weighted segmented architecture, shown in Figure 5.1.The same decoder and latches used in case of the current steering DAC are also used for the Resistive DAC. The decoder output is fed to the latches and subsequently fed to the DAC as switching signals, switching between 0 and VDD.

The differential DAC is implemented using two identical Resistor arrays connected to the positive and negative terminal of a differential op amp with complementary switching signals. Hence if m resistors are active on the negative side, $2^N - m$ are active on the positive side.

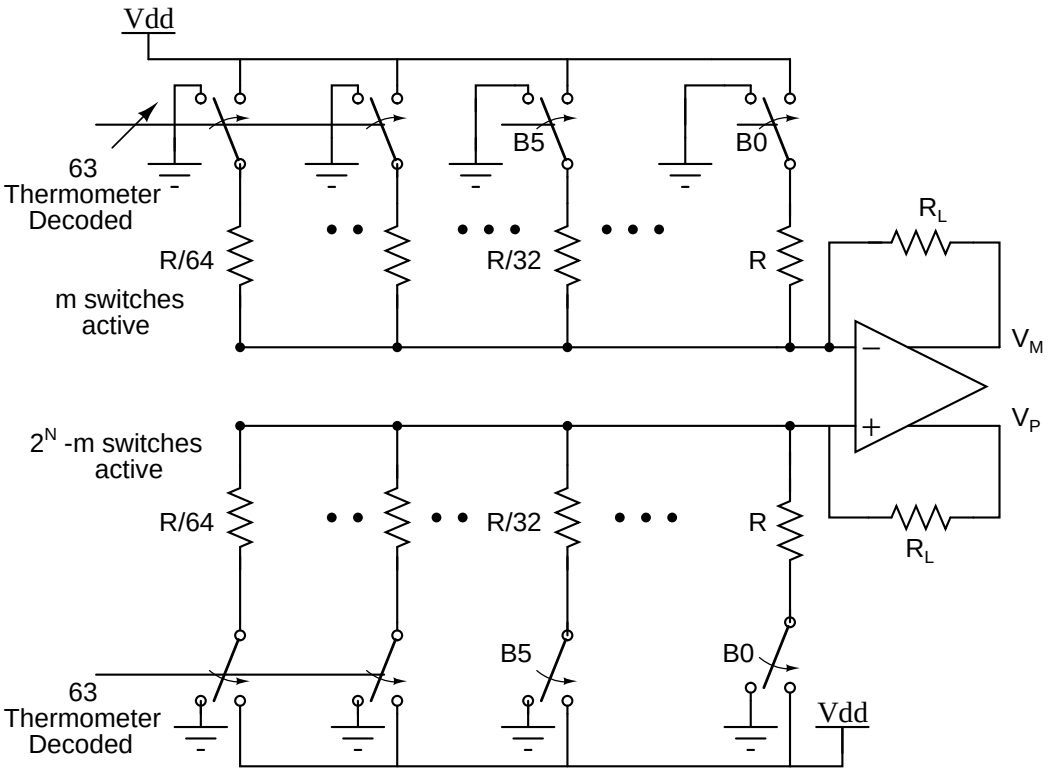

Figure 5.1: Fully Differential Resistive DAC

5.2.1 Switch On Resistance (Binary Weighted LSB DAC)

In case of resistive DAC, the on resistance of switches plays a very important role. As the switches come in series with the resistors in the ladder, finite on resistance of the switches defines the amount of current flowing in each leg of the resistive ladder and hence degrades the static performance of the DAC.

A MOS transistor in linear region can be used as a switch. Depending upon the switching voltage, the switches can be implemented by either a PMOS or an NMOS or both. When an NMOS is used as a switch, it gives a strong zero and a weak one. On the other hand a PMOS switch gives a strong one and a weak zero. Hence NMOS switches are used when a resistor is switched to zero and a PMOS switch is used when it is switched to VDD.

$$Ron = [\mu C_{ox} \frac{W}{L}(V_{GS} - V_{TH})]^{-1} \tag{5.1}$$

DC analysis of a minimum size NMOS transistor (135nm/60nm) gives an on resis-

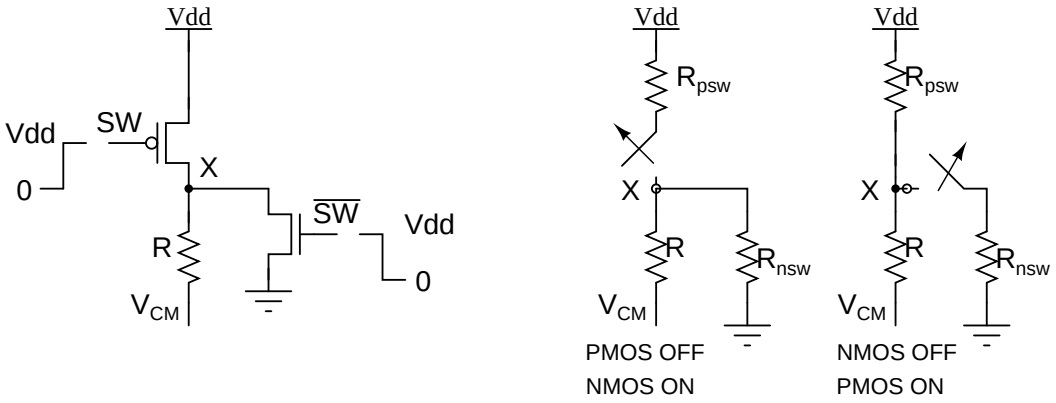

Figure 5.2: Switch On Resistance along with ladder resistor

tance of 2.256KΩ. R is taken as 50KΩ for a 50mA full scale current (to have small size of resitors). Corresponding to higher bits as the size of the resistors reduces, the on resistance of the switch becomes comparable to that of the binary weighted or thermometer DAC resistor and the voltage drop across the resistor no longer remains $V_{DD} - V_{CM}$ but gets divided like in a voltage divider. As seen in Figure 5.2, voltage at node X is defined by the resistance of the switch which is on. This causes the currents in the resistor ladder branches to be different from 2X,4X.. times I_{unit}, different from what is expected. This further introduces non-linearity in the system. Switch on resistance should be reduced to fix this issue.

According to equation 4.1, R_{on} can be reduced by increasing the size of the transistor. Hence the LSB switch sizes are made 4X the minimum size (NMOS-135nm/60nm, PMOS-3*135nm/60nm) and all subsequent MSB switches are sized correspondingly as 2X ,4X,8X,16X,32X and 64X the size of the LSB switch so that the voltage drop across the respective resistors is the same in all the cases, hence driving the expected amount of current.

In Figure 5.2, ideally voltage at node X supposed to swing between 0 and VDD (1.2V). But due to the finite on resistance of the switches, it goes between 35mV and 1.189V (LSB switch sizes are 4X the minimum PMOS and NMOS sizes).

When the size of the switches is increased further to 10X the minimum size of both NMOS and PMOS switches, this swing changes to 20mV and 1.955V. At 10X, MSB (largest switches) PMOS size is 260um/60nm and NMOS size is 86um/60nm corresponding to R/64 resistors.

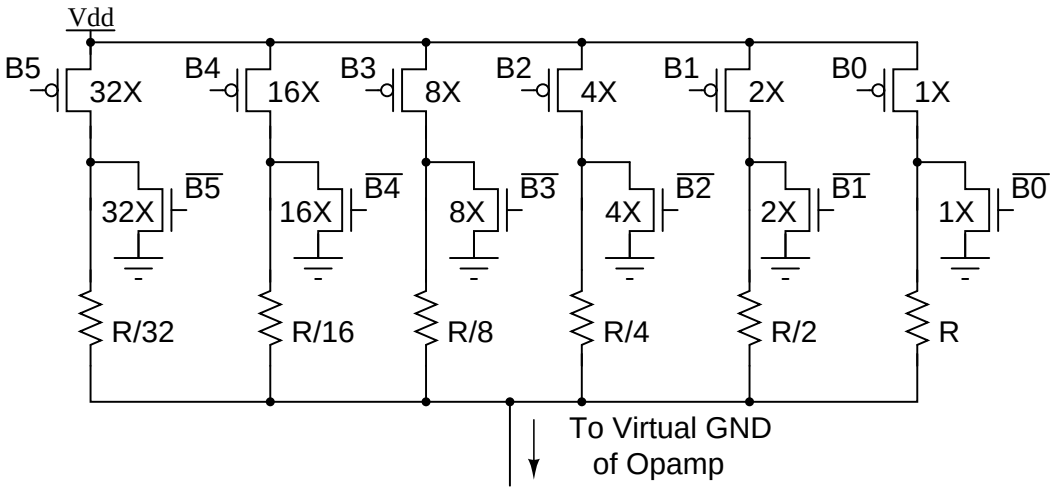

Figure 5.3: Binary weighted DAC with scaled switches

The transistors are sized such that the Ron of a PMOS-NMOS switch is equal for both the switches, that is PMOS size is 3 times the NMOS size as seen in Table 5.1.

Table 5.1: On resistance of switches

Switch Type	Switch Size	Ron(Ω)	Rload(Ω)	Voltage across resistor(V)
	Compared to min size			
nlvtlp	1X	2.256K	R	0.55
nlvtlp	4X	612.5	R	0.593
nlvtlp	10X	249.8	R	0.597
plvtlp	10X	257.7	R	0.597

Min size NMOS = 135nm/60nm; Min size PMOS = 3*Min size NMOS; R=50KΩ

Ideal voltage across resistor is 0.6V (VDD-Vcm). With 10X size switches we obtain a close value of 0.597V. Larger switches can be used to push this value even closer to 0.6 but the size of the switches become too large to implement on Silicon.

From Table 5.2 we can observe that scaling the switch sizes by the same factor by which the branch resistors are scaled down, the voltage drop across the resistor remains constant and hence keeping the currents clean multiples of the LSB branch current.

In case of binary weighted architecture for the 6 bit LSB DAC, due to presence of 6 different values of resistors, there is large mismatch issue. That is, there will be large glitches in the DAC output at major code transitions and this worsens the DAC dynamic performance. Also, in case of the fully binary weighted LSB DAC architecture, the LSB resistor becomes very large $\sim M\Omega$, for a full scale current of 1mA, becoming non-realistic to implement linearly on silicon. Hence to keep both, the full scale current

Table 5.2: Scaling of switches

Switch Size	Ron(Ω)	Rload(Ω)	Voltage across resistor(V)
Compared to LSB switch			
2X	125.9	R/2	0.597
4X	63.19	R/4	0.597
8X	31.66	R/8	0.597
16X	15.84	R/16	0.597
32X	7.92	R/32	0.597
64X	3.964	R/64	0.597

LSB switch size = 10X of Minimum size switches; R=50KΩ

as well as the LSB resistor realizable, an R-2R architecture is tried for the LSB DAC. The advantage with R-2R architecture is better matching since only two values of resistors are used. R-2R DAC architecture, acts as a successive voltage division circuit, allowing smaller size of resistors to be used for smaller full scale current. The design and behavior of the R-2R DAC is described in the next section.

5.2.2 R-2R LSB DAC

The LSB R-2R DAC can be implemented in two ways. One with the switches near the VDD/GND end and one with the switches at the virtual ground of the op amp end. It is observed that in the current mode, the resistors are switched between virtual grounds of two op amps and large spikes are seen in the output current due to charge injection, as seen in Figure 5.5.

Current mode R-2R DAC Figure 5.4 shows the structure of the current mode R-2R DAC.Every subsequent resistor branch contains half the current of the previous branch.

The total single ended output current in Figure 5.4 can be given as

$$I_{out} = V_{DD}(\frac{B_5}{2} + \frac{B_4}{4} + \frac{B_3}{8} + \frac{B_2}{16} + \frac{B_1}{32} + \frac{B_0}{64}) \tag{5.2}$$

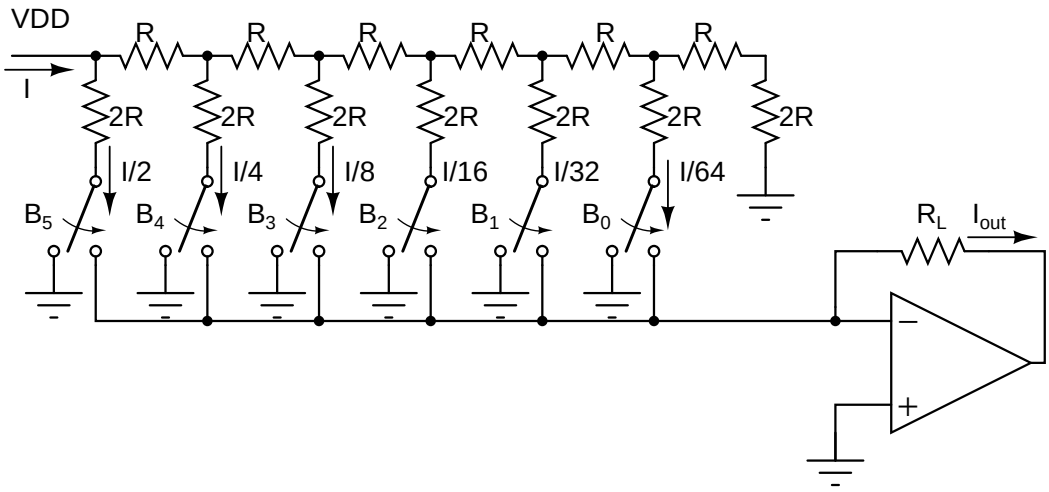

Figure 5.4: Current mode R-2R DAC

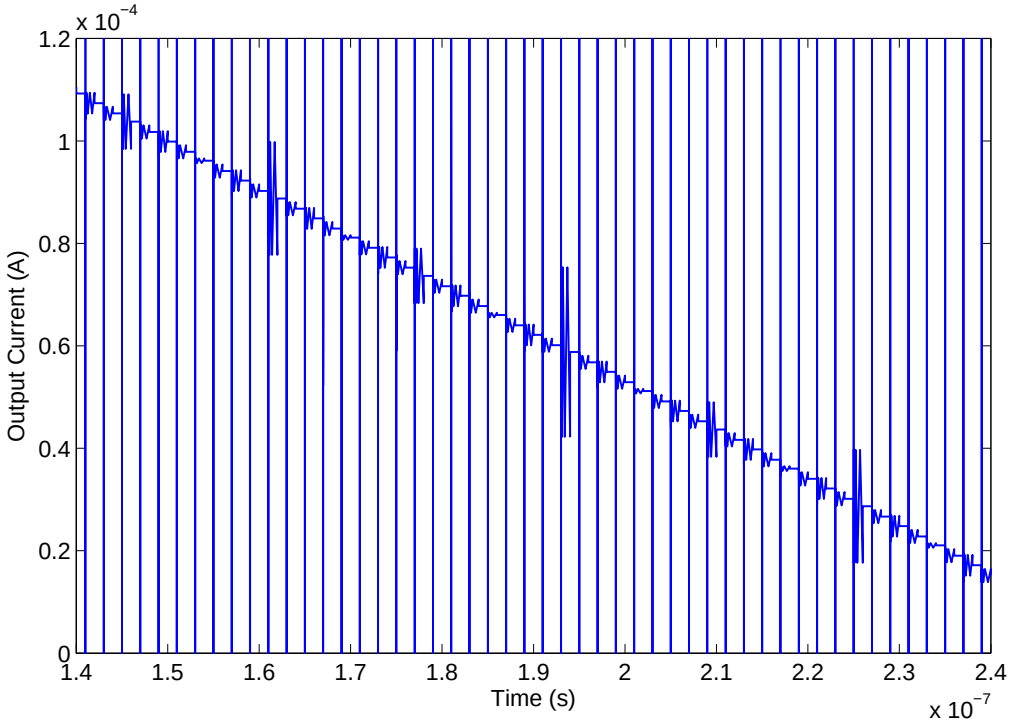

Figure 5.5: Output voltage waveform of Current mode DAC for ramp input

Charge Injection in Current mode R-2R DAC

In the 6 bit R-2R LSB DAC, implemented in current mode as seen in Figure 5.4, the switches are present on the virtual ground side instead of the VDD/GND side. In this configuration, the output DAC waveform is seen to have large spikes at every clock transition as seen in Figure 5.5. Possible reasons behind these glitches are clock feed through and charge injection.

Clock feed through: This is due to the parasitic capacitance between the gate and drain and gate and source of the transistors. Due to this the switching signal is coupled to the drain /source and hence causes spikes at the switching transitions. Upon replacing the PMOS and NMOS switches with a CMOS switch, with same sized PMOS and NMOS transistors, clock feedthrough should get canceled. But this was not observed and spikes were still present in case of the Current mode R-2R DAC. This suggests that charge injection is the cause and clock feedthrough is ruled out.

Charge Injection: In this phenomenon, the charge in the channel of the transistor, takes the path of least resistance to flow out. In case of the voltage mode DAC,Figure 5.7, the switches are present on the VDD/GND side and VDD/GND are the path for least resistance, hence all the charge flows towards VDD/GND and the current flowing through the op amp is not affected. But in case of the current mode DAC, the switches being on the virtual ground side of the resistive ladder, the charge in the channel of the transistor flows towards the op amp and reflects in the DAC output voltage as spikes. Since in charge injection, charge flows in the path of least resistance, this is verified by placing a small resistance between the switches and the virtual ground of the op amp. This reduces the spikes in the output waveform. Hence charge injection is observed to be present in this architecture.

Voltage mode R-2R DAC

The structure of a voltage mode R-2R DAC can be seen in Figure 5.7 and the output waveform in Figure 5.8.In this case the switches are towards the VDD/GND end and

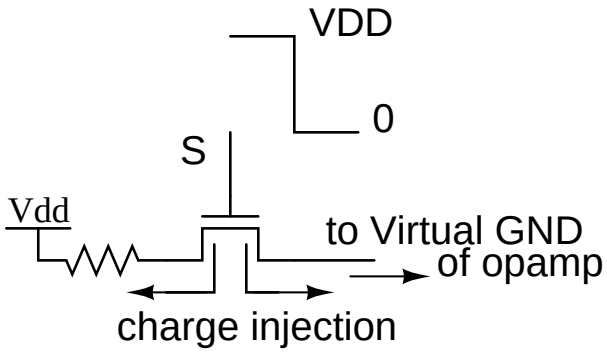

Figure 5.6: Charge Injection in MOS switches

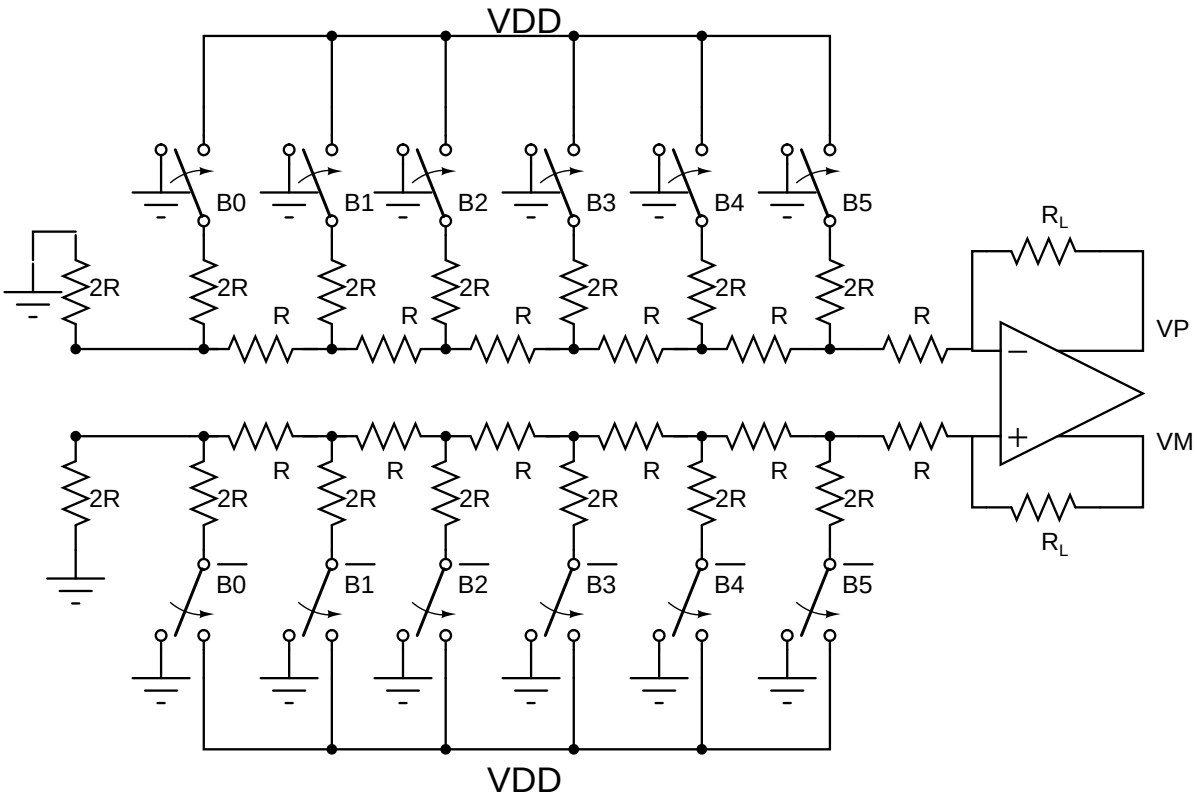

Figure 5.7: Voltage mode R-2R DAC

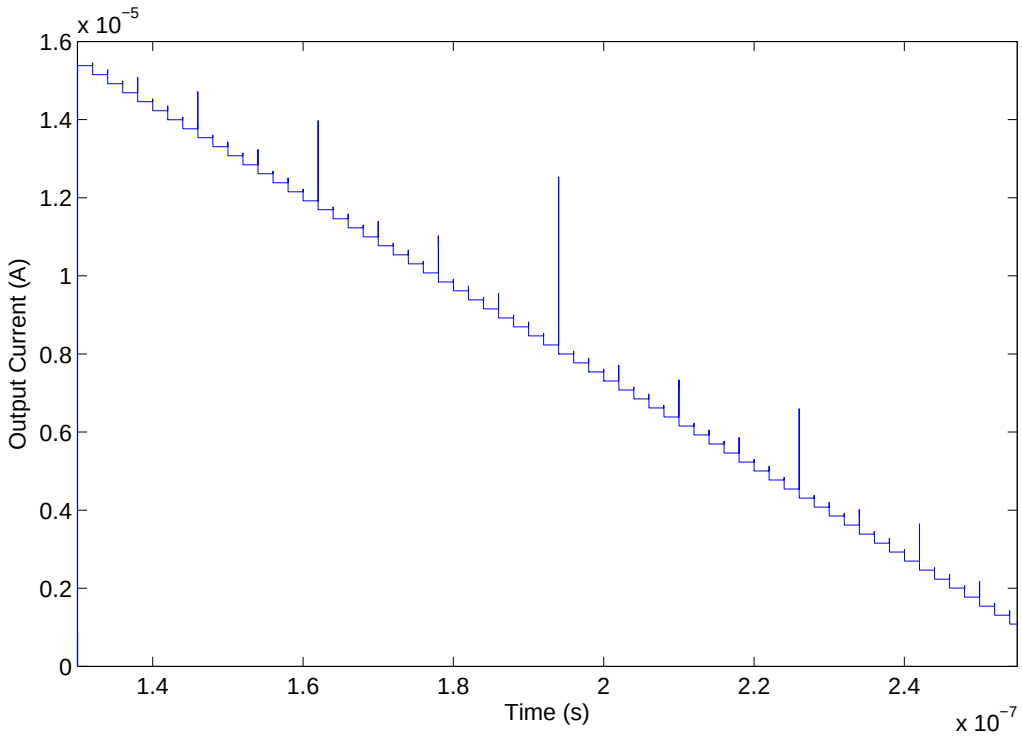

Figure 5.8: Output waveform of voltage mode R-2R DAC for ramp input

hence charge injection is not observed. With current mode R-2R configuration, the SFDR is 90dB at 1.892MHz and falls to close to 80dB close to Nyquist. But in case of voltage mode R-2R DAC, SFDR is better than current mode and close to binary weighted, but the drawbacks being large sizes of switches to reduce on resistance and non-linearity due to the switch on resistance. A different segmentation is described in the next section to tackle these issues.

5.2.3 3-way Segmented DAC

In order to reduce the effect of the switch size and positioning in case of the two R-2R DAC implementations as well as charge injection, the lower 6 bits are further segmented into 3+3 bits where the upper LSB bits are binary weighted and the lower 3 LSB bits are implemented as a R-2R DAC. The voltage mode of R-2R DAC is implemented and the output current waveform, Figure 5.10, for a ramp input is very close to ideal.

3-way segmented DAC output is observed to be much cleaner than the R-2R DAC outputs in Figures 5.5, 5.8 and 5.10.

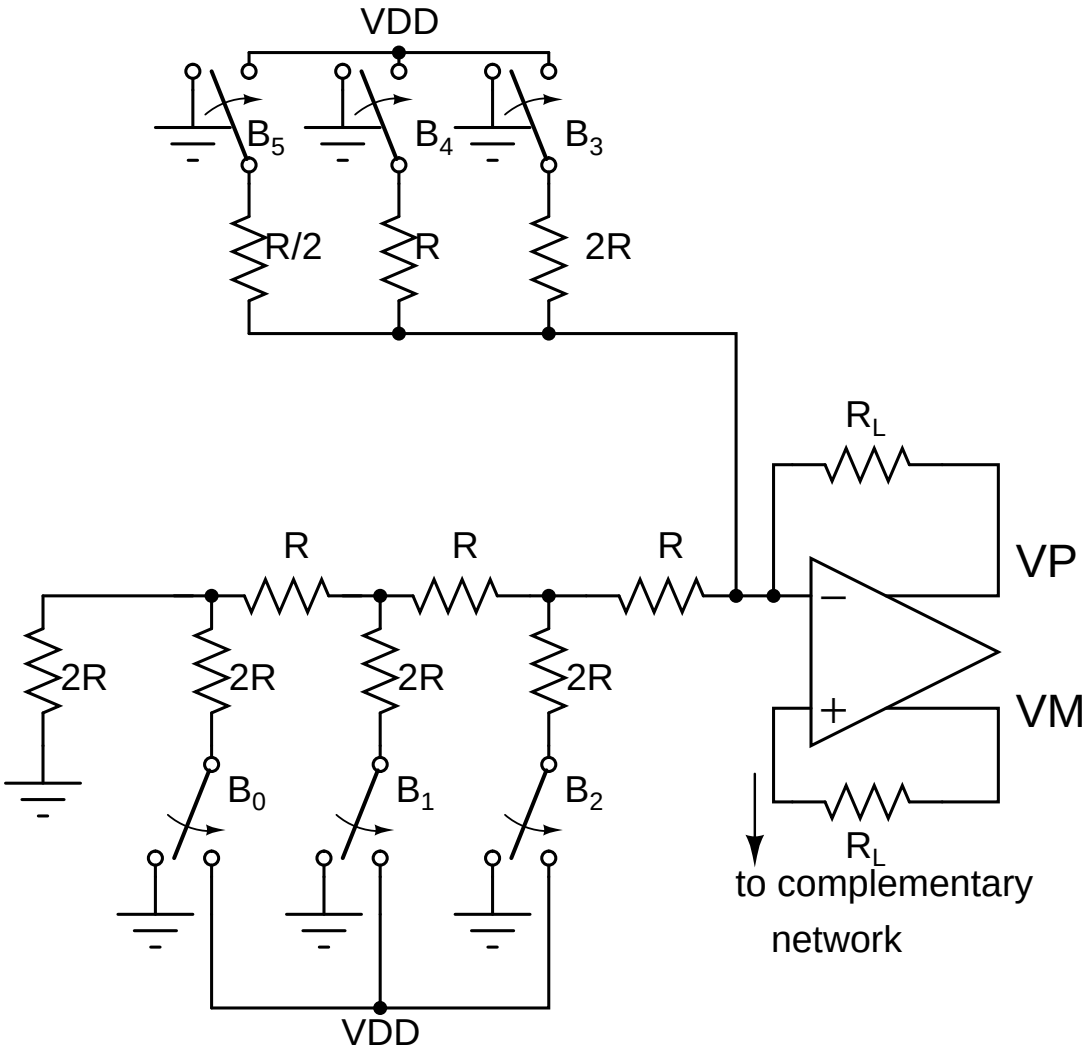

Figure 5.9: Segmented LSB DAC

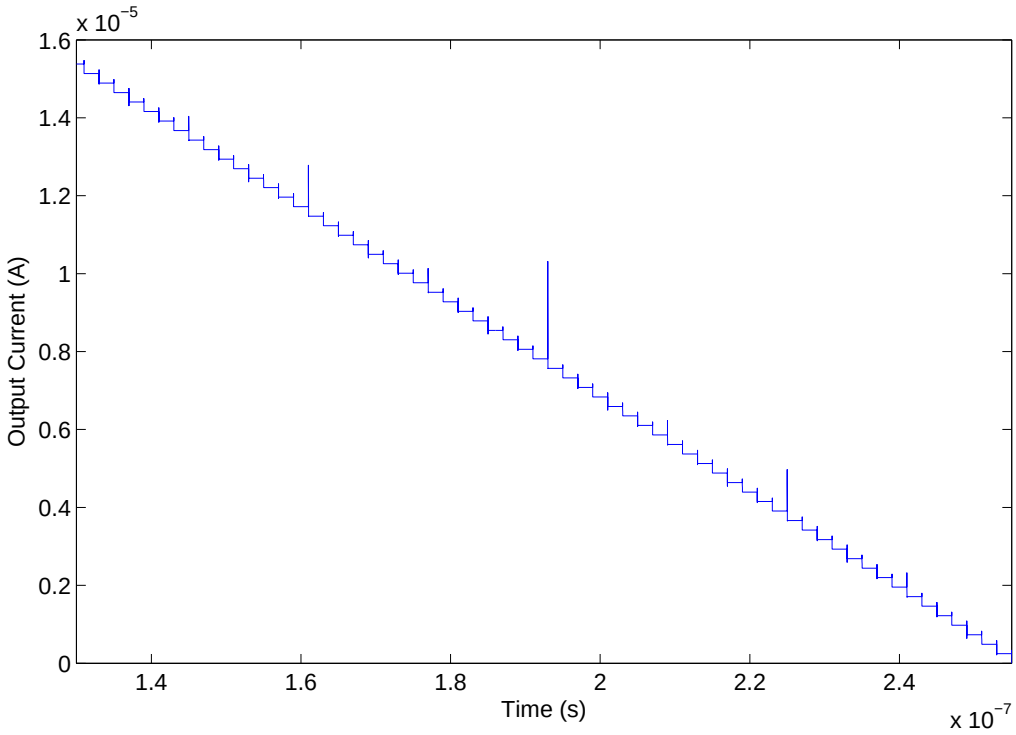

Figure 5.10: Output current in 3 way segmented LSB DAC

5.3 Resistive DAC with Ideal Op amp

The resistive DAC with 3-way segmentation is considered with the Ideal Op amp to compare with the current steering DAC.

The top 6 bits are thermometer decoded, next three bits are binary weighted and the bottom 3 bits are implemented as a voltage mode R-2R DAC. The 6-63 binary to thermometer decoder is used to decode the top 6 bits to be fed into the USB thermometer DAC. The 6 LSB bits are fed directly. All these switching signals are fed to latches and subsequently to the respective DAC switching transistors.

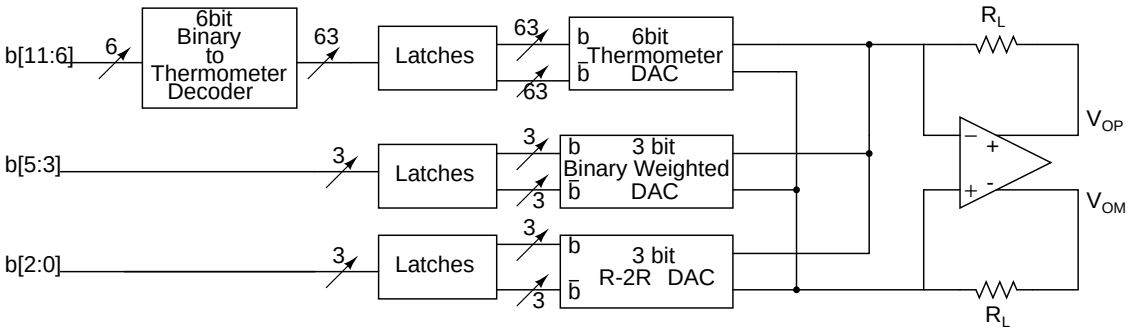

Figure 5.11: Resistive DAC Block Diagram

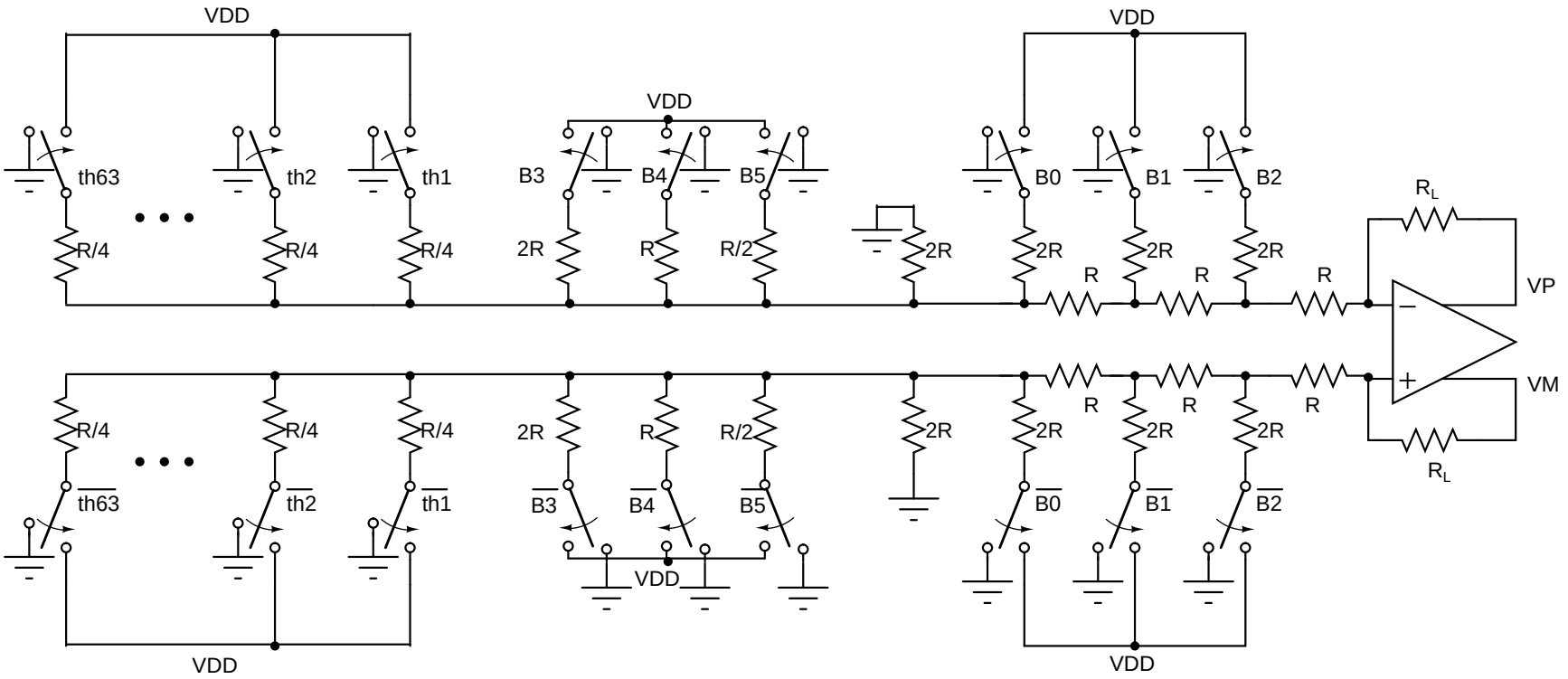

Figure 5.12: Full Resistive DAC structure

An ideal op amp of 10000 gain and infinite bandwidth is generated using a VerilogA block and used to simulate in this architecture.

Since the common mode of the switching nodes and the output nodes is V_{CM}, the virtual ground nodes also settle to V_{CM} as the gain of the op amp is very high.

The DAC performance is measured in terms of DNL, INL, SFDR and IM3, as will be seen in section 5.5. It is seen to be quite close to the Ideal behavior. The ideal op amp is then replaced by a real op amp targeting a high gain and high UGB. The op amp design for the resistive DAC is seen in the next section.

5.4 Op amp Design

For our design of the 12 bit resistive DAC, to have good static and dynamic performance, the op amp at the end of the resistor ladder needs to have high gain and high bandwidth. As the output of the DAC can be considered as a sample and hold version of a sin wave, it has the fundamental and all odd harmonics. And to successfully replicate this behavior at the op amp output, the op amp ideally needs to have infinite gain and infinite bandwidth. But as real systems are finite gain, finite bandwidth systems, the design of the op amp should target the maximum gain and bandwidth obtainable for a given architecture, with realistic power consumption.

For our design we consider a two stage feed forward compensated architecture which gives a high gain and high bandwidth.

Figure 5.13 shows a the macro model of the two stage feed forward compensated op amp designed for the resistive DAC. Transconductor G_{mF}constitutes the high speed feed forward path, while, transconductors G_{m1} and G_{m2} form the two stage high gain path.

The transfer function is given as $\frac{V_0(s)}{V_e(s)} = \frac{G_{mF}}{G_L+sC_L} + \frac{G_{m1}G_{m2}}{(G_{O1}+sC_1)(G_L+sC_L)}$

DC gain is due to that of two stages given by $A_o = \frac{G_{mF}}{G_L} + \frac{G_{m1}G_{m2}}{G_{o1}G_L}$

This system has two poles and one zero in the left half plane.

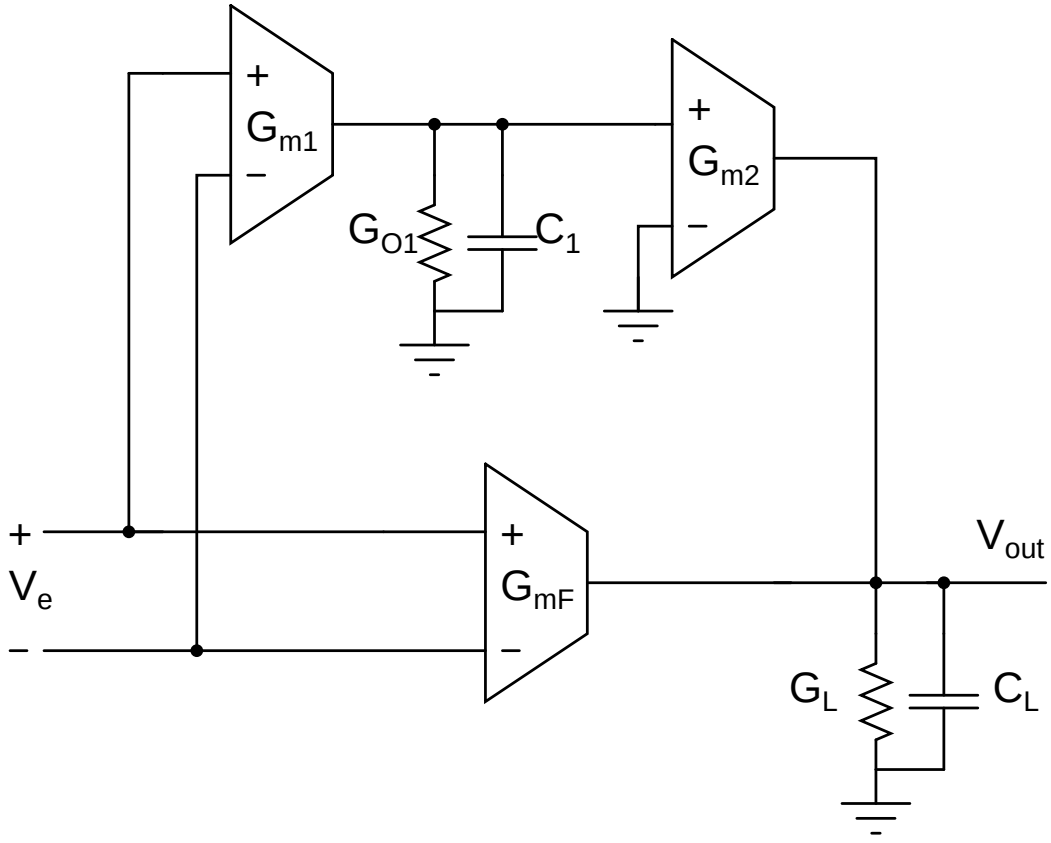

Figure 5.13: Two stage feed forward compensated op amp

$p_1 = \frac{G_L}{C_L}$, $p_2 = \frac{G_{O1}}{C_1}$, $z \simeq \frac{G_{m1}G_{m2}}{G_{mF}C_1}$,$\omega_0 = \frac{G_{mF}}{C_L}$

For the system to be stable, the net phase shift should be between $-90^0$and -180^0. Hence both the poles and the zero should come before the UGB, as the two poles add a phase shift of -180^0 and the zero adds $+90^0$, asymptotically reaching -90^0.The op amp is designed such that the zero comes in between the two poles, such that the system looks like a first order system at UGB. In our case, the op amp is placed in a resistive feedback loop and hence the load is only the parasitic capacitance of the output stage.

To obtain a high gain , the first stage is designed as a telescopic cascode architecture.Also, as the full scale current of the DAC is 1mA, hence the op amp output stage should be able sink 1mA of current at full scale with good linearity. Hence the transistors in the output stage are sized to carry a bias current of 2mA. But increasing the output stage current any further will reduce R_{ds} at the output node and introduce non-linearity. Hence the bias current is fixed at 2mA.

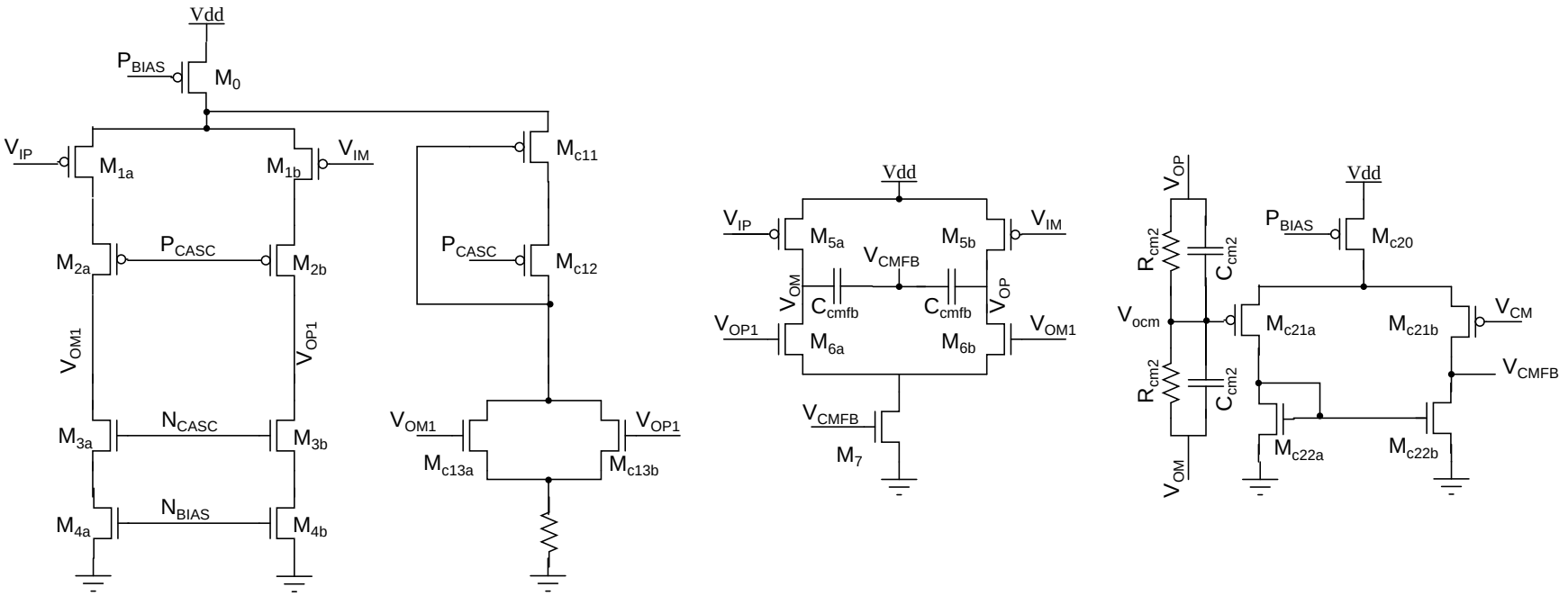

Figure 5.14: Two stage feed forward op amp schematic

Table 5.3: Opamp Transistor Sizes

$M_0 = 132u/0.2u$	$M_5 = 80u/0.12u$	$M_{c13} = 1.8u/0.06u$
$M_1 = 60u/0.12u$	$M_6 = 2(150u/0.24u)$	$M_{c20} = 1.6u/0.2u$
$M_2 = 60u/0.06u$	$M_7 = 100u/0.06u$	$M_{c21} = 3u/0.2u$
$M_3 = 15u/0.06u$	$M_{c11} = 12u/0.12u$	$M_{c22} = 2u/0.4u$
$M_4 = 1u/0.5u$	$M_{c12} = 12u/0.06u$	

The structure of the op amp can be seen in Figure 5.14. The first stage transconductance G_{m1} is formed by transistors M_{1a} and M_{1b}. PMOS transistors M_{2a} and M_{2b} act as cascode stage to increase the output impedance. NMOS transistors M_{4a} and M_{4a} form the current source and M_{3a}, M_{3b} form the cascode stage for the current source to increase output impedance and subsequently, the gain. A current mode feedback is used for the common mode feedback of the first stage. Transistors M_{c11} to M_{c13b} form the common mode feedback of the first stage. When the first stage common mode voltage increases, which implies that the current through M_1 is higher than the current in M_3, V_{GS} across M_{c13a} and M_{c13b} increases. Then the current through $M_{c11-c13b}$ increases. But since the sum of currents through M_1 and M_{c11} is constant, current through M_1 will reduce, reducing the common mode voltage at the first stage output. The current through M_{c11} is set to be one-fifth of the current through M_0.

In the output stage, transistors M_{6a} and M_{6b} form the second stage transconductance (G_{m2}). The feed forward stage constituted by transistors M_{5a} and M_{5b} reuses the current of the second stage to prove a high speed path. A resistive common mode detector and a single stage op amp form the common mode feedback circuit for the second stage. The input to the feedback amplifier becomes,$V_{ocm} = (V_{OP} + V_{OM})/2$. The single stage amplifier constituted by transistors $M_{c20} - M_{c22b}$, set the output common mode to V_{CM}.

As seen from the bode plot in Figure 5.15, the op amp UGB is close to 7.5GHz and has a DC gain of 56.6dB. The two poles are at 6.26MHz and 5.05GHz and the zero is at 3.21GHz. Power consumed by the op amp is 6.291mW. This op amp is integrated with the resistive DAC ladder and the performance characterized as seen in the following sections.

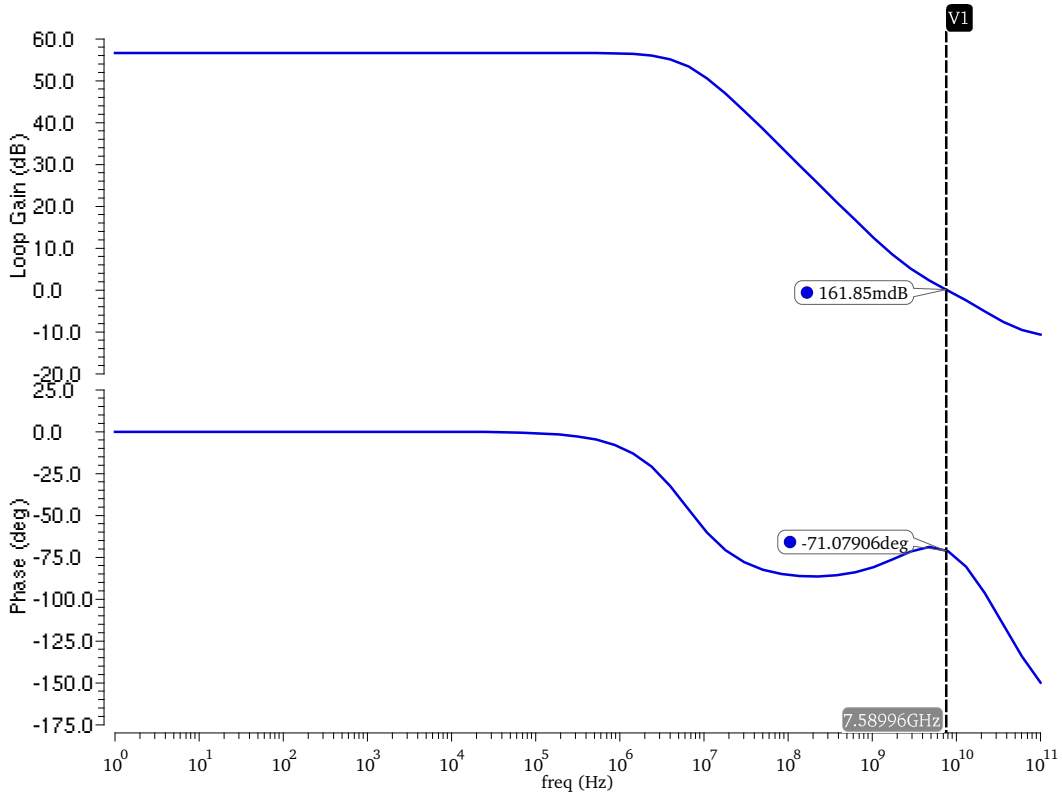

Figure 5.15: Op amp Loop Gain and Phase Bode plot

5.5 Simulation Results and Observations

The DNL and INL characterize the static behavior of a DAC. Hence to plot the DNL and INL, the steady state output values for every code are taken and the DNL and INL computed as described in section 2.1.

For an ideal DAC, in our case with ideal resistors and ideal op amp, the DNL and INL should be close to zero as there is no error in the output voltage. This can be observed in Figure 5.16, where the DNL and INL of an Ideal 6+6 thermometer + binary weighted segmented DAC is very close to zero.

The DNL and INL for the 6 bit thermometer + 6 bit R-2R DAC is plotted in Figure 5.17. As described in section 5.2.2, charge injection is present in a current mode R-2R DAC. But as DNL/INL are static performance measures, the DNL and INL are observed to be within specifications. The degradation due to charge injection reflects in SFDR degradation.

Figure 5.18 shows a comparison in SFDR between different resistive DAC architec-

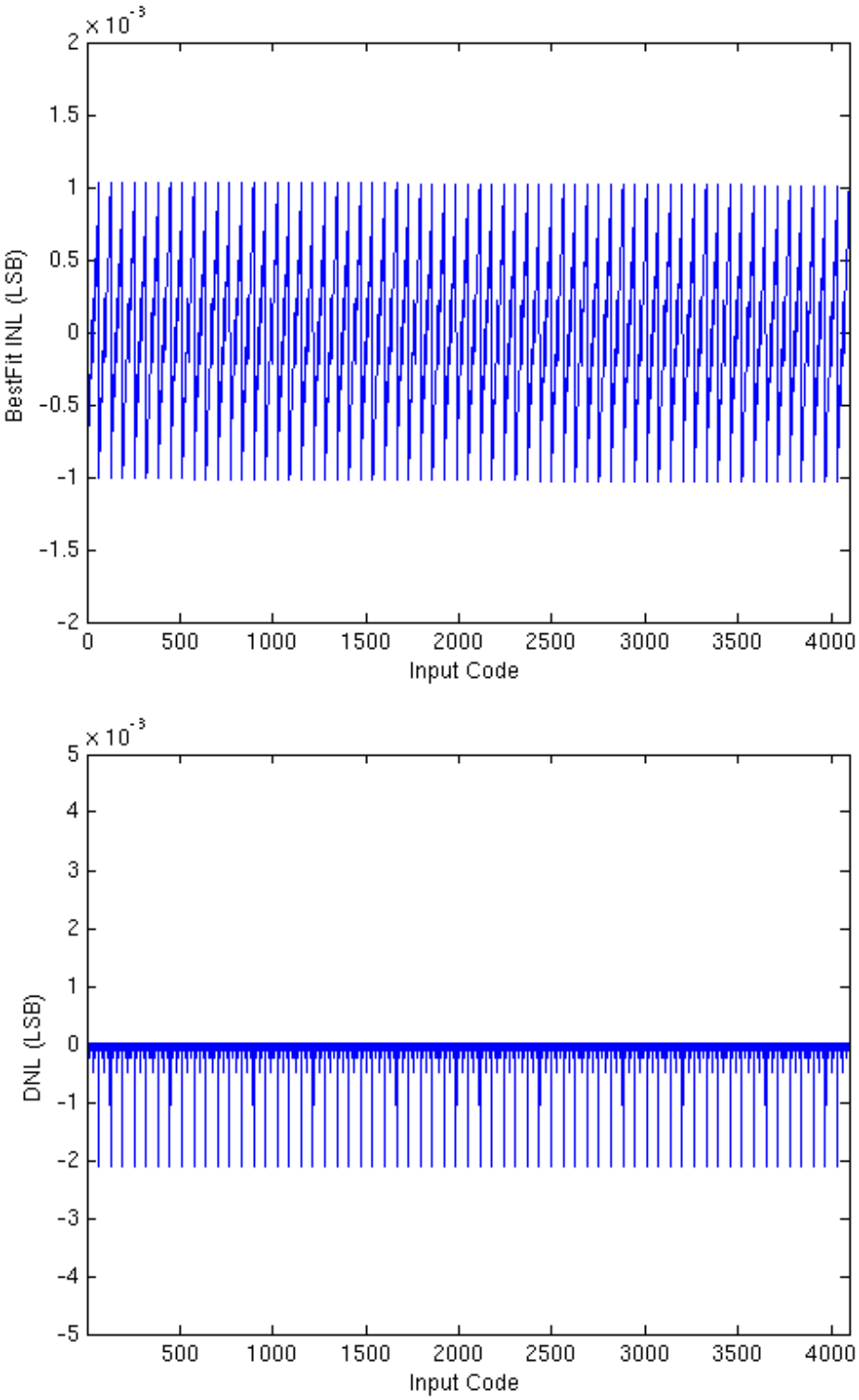

Figure 5.16: Best fit INL and DNL for Ideal DAC

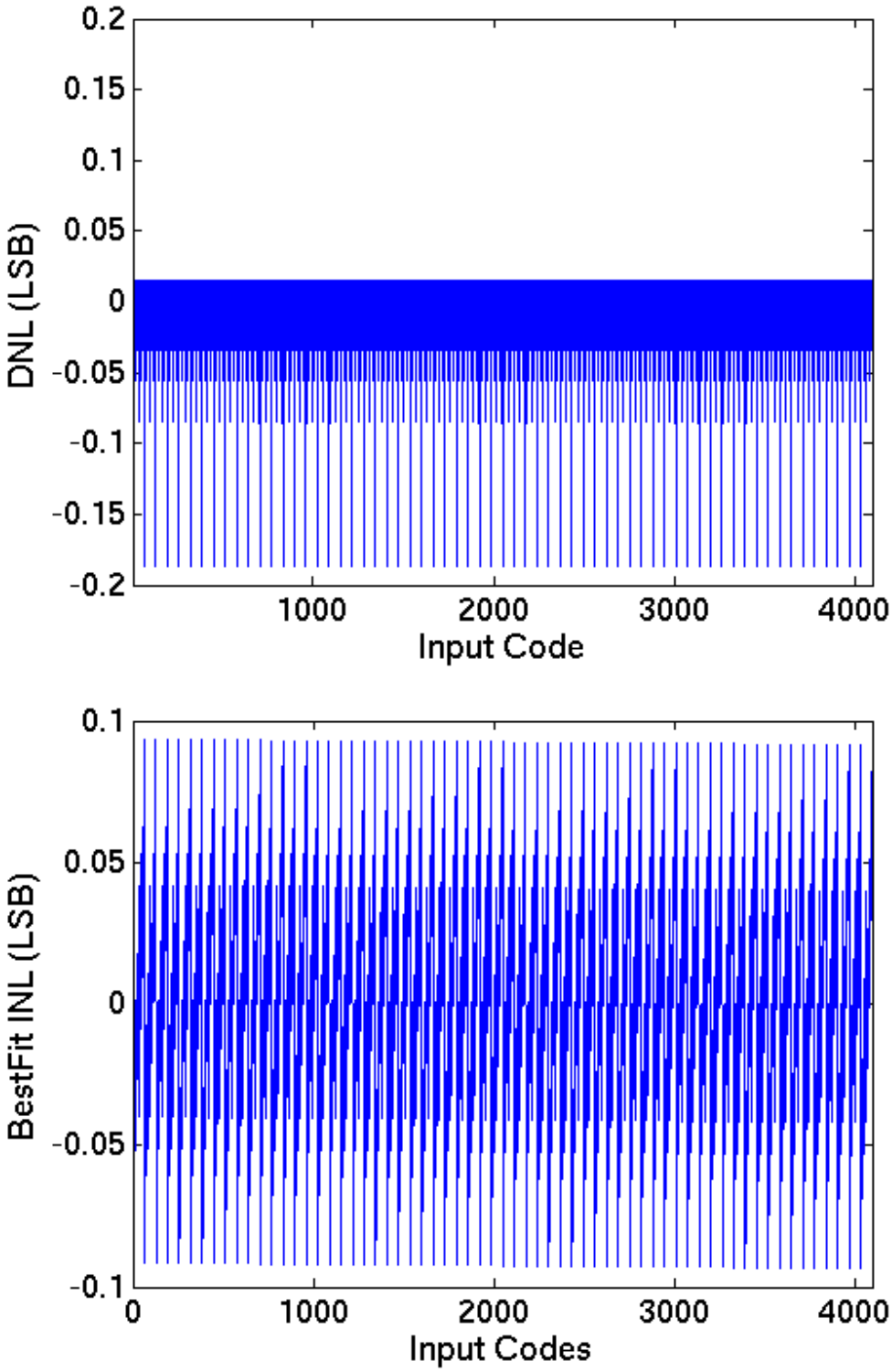

Figure 5.17: R-2R DAC DNL INL

tures with real resistors and Ideal opamp. These are compared with the Ideal resistive DAC SFDR. When the 6 LSB bits are implemented as a binary weighted DAC, SFDR is observed to be higher than a corresponding R-2R DAC implementation. Best case SFDR behavior is with the 3 way segmented DAC, in which the SFDR for real resistors and Ideal opamp implementation is above 90dB for most of the signal band.

Figure 5.19 shows a comparison in SFDR between resistive DAC implementations with Ideal opamp and the real opamp designed.

With the real opamp, and a feedback resistor of 50Ω, the SFDR is observed to be around 90dB till frequencies upto 100MHz and above 80dB for frequencies upto 150MHz.

SFDR degradation with real opamp at high frequencies: It is known that the g_{ds} of a transistor changes with V_{ds} across it. Since the full scale current of the DAC is 1mA, the feedforward stage of the opamp is biased at 2mA. Due to the large size of the transistors in the output stage, the r_{ds} seen from the output of the opamp is a few hundred ohms. With lower feedback resistor of 50Ω ,the SFDR is seen to improve to higher than 70dB at 220MHz as compared to 60dB for a 250Ω feedback resistor.

For a smaller swing at the output, the r_{ds} of the transistors is more linear and hence the SFDR improves. Upon placing a VCVS of gain 1, the VCVS provides all the current required by the DAC and the g_{ds} non-linearity does not reflect at the output. This is observed when the SFDR with the VCVS is seen to be above 90dB through out the bandwidth.

g_{ds} linearity can be improved by increasing the lengths of second stage transistors.But improvement in SFDR with this is marginal as the width of the transistors also correspondingly increases. g_{ds} non linearity is a strong function of the output swing. Cascoding the transistors in the second stage improves the absolute value of r_{ds} but at the cost of output swing, hence degrading the SFDR.

The SFDR is seen to degrade with frequency because of the finite gain, finite bandwidth property of the opamp. In the two stage feedforward architecture of the opamp implemented, the DC gain is DBMS and the UGB is close to 7.5GB. But as the frequency increases the gain of the opamp reduces. It is seen that at 250MHz, the gain of

the opamp reduces to 25dB. Hence the effect of gds non-linearity with swing is higher at higher frequencies,due to which the degradation of SFDR with frequency is observed.

Reducing the opamp UGB to 2GHz degrades the SFDR to 50dB at 220MHz as compared to 60dB with the 7.5GHz opamp for a feedback resistor of 250Ω. This suggests that the gain of the opamp at frequencies close to Nyquist frequency limits the SFDR and hence a higher gain and higher bandwidth opamp can be used to improve the performance of the DAC.

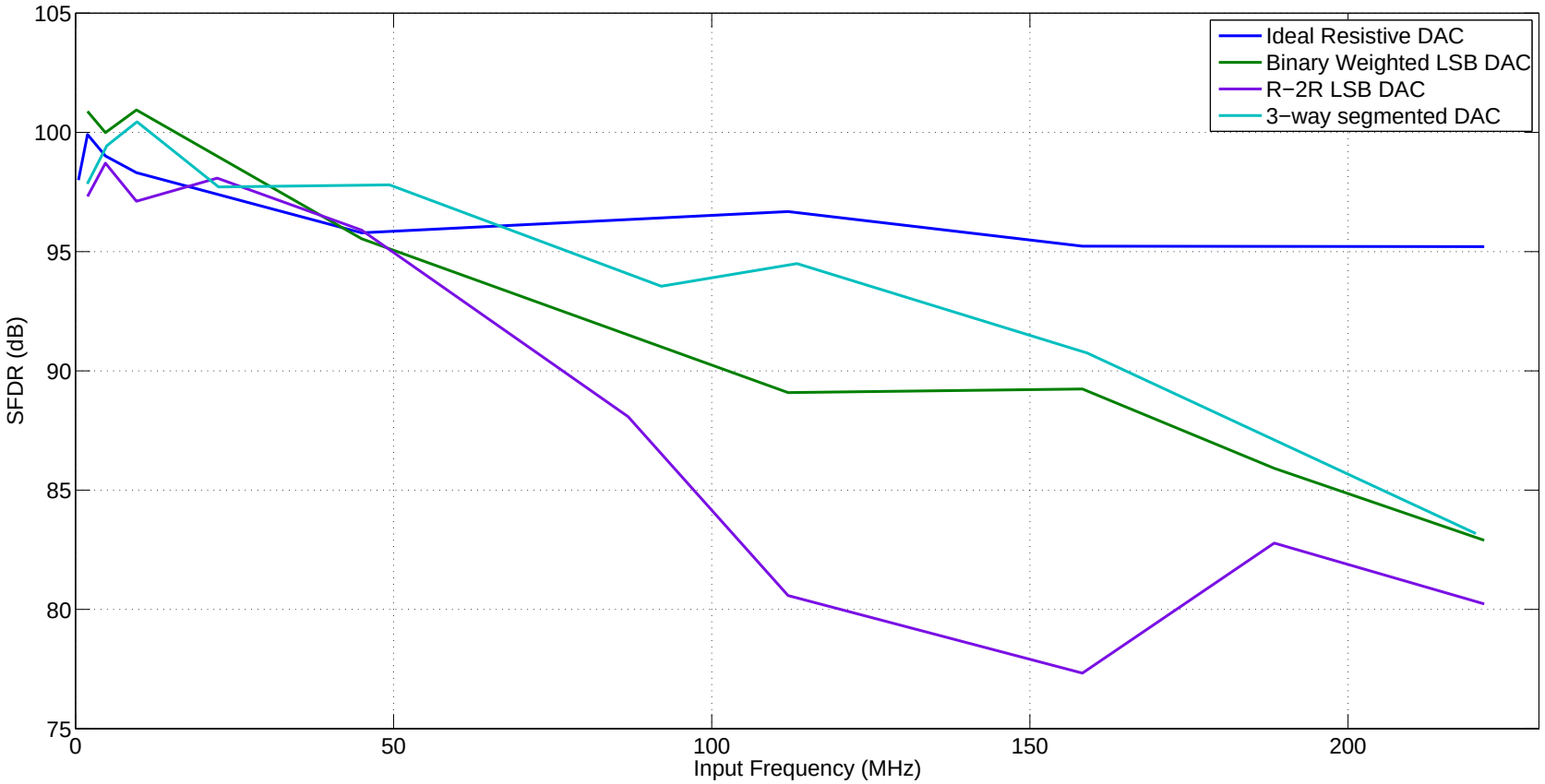

Figure 5.18: SFDR comparison for different resistive DAC architectures

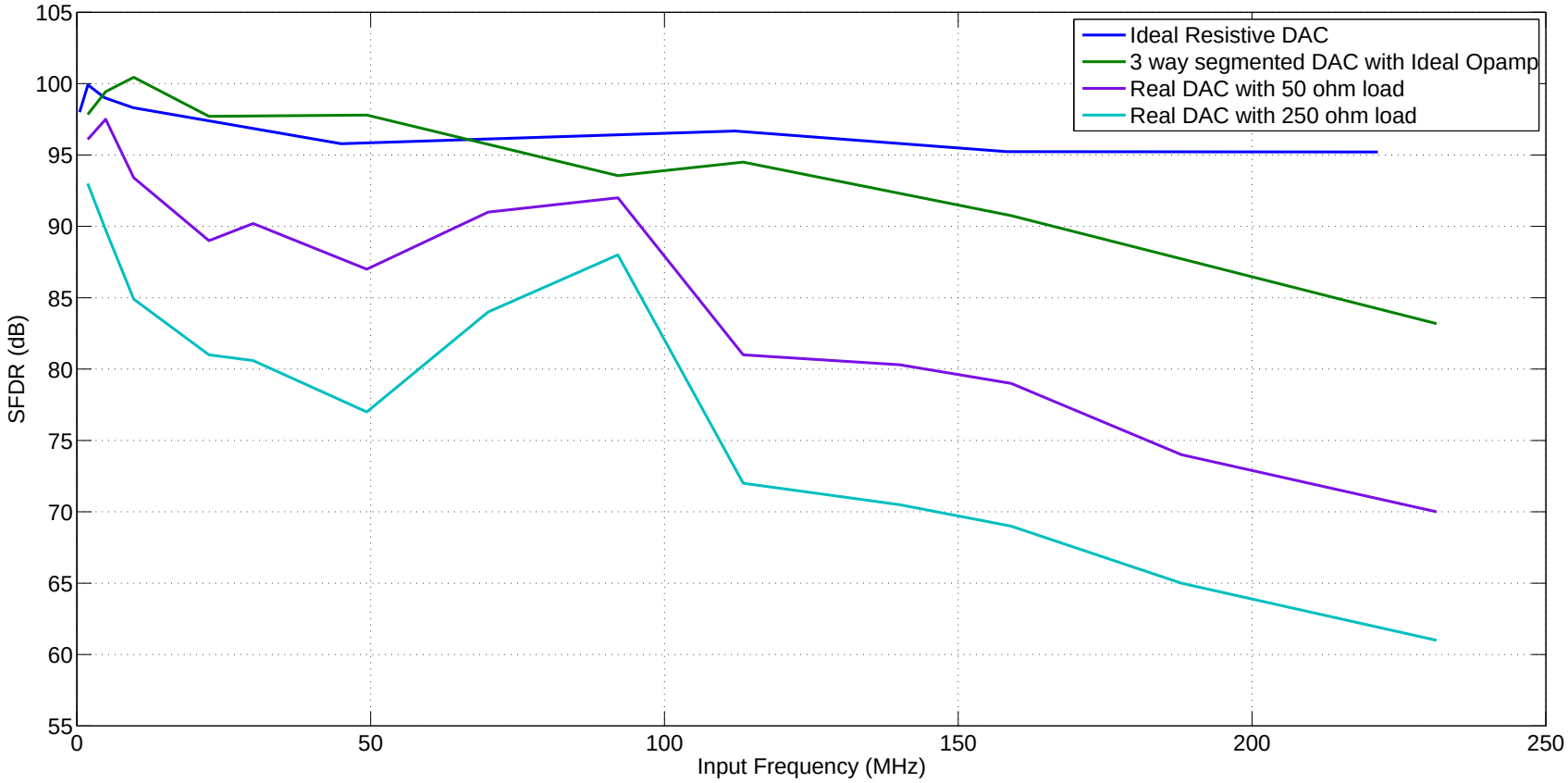

Figure 5.19: SFDR comparison for resistive DAC with ideal and real op amps

CHAPTER 6

Comparison : Current Steering DAC vs Resistive DAC

6.1 Dynamic Performance

In this section, both the DAC designs, current steering and resistive DAC designs are compared in terms of their static and dynamic performances. Figure 6.1 and 6.2 show a comparison in the SFDR of the output of the two DAC designs for load resistors of 50Ω and 250Ω respectively. These are also compared with the SFDR of an Ideal DAC. In both the cases it is observed that the overall spectral performance of the resistive DAC design is better than the current steering counterpart. The spurious free dynamic range with frequency is observed to be higher for smaller load resistors at the cost of output swing. In case of the resistive DAC, SFDR is seen to be around 90dB for input frequencies upto 100MHz and then gradually falls to 72dB at frequencies close to the Nyquist frequency. Whereas, in the current steering DAC, the SFDR starts above 90dB at low frequencies but rolls off fast to less than 70dB at higher frequencies.

Figure 6.3 shows a comparison of the intermodulation distortion due to third order distortion components in the output spectrum of the DAC. This is calculated as describes in section 2.1.2. Resistive DAC is again seen to have higher distortion tolerance compared to the current steering DAC.

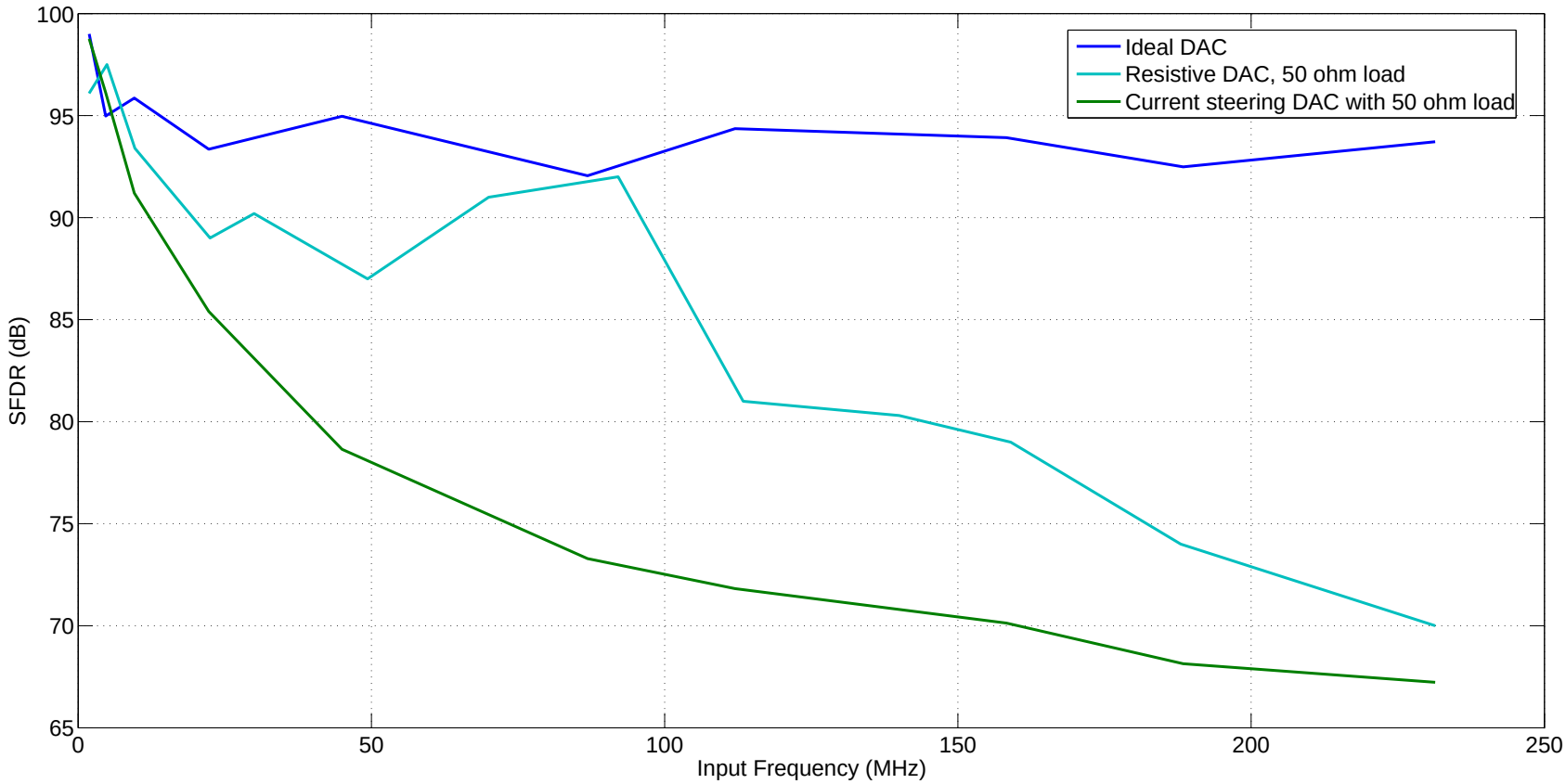

Figure 6.1: SFDR comparison for 50Ω load

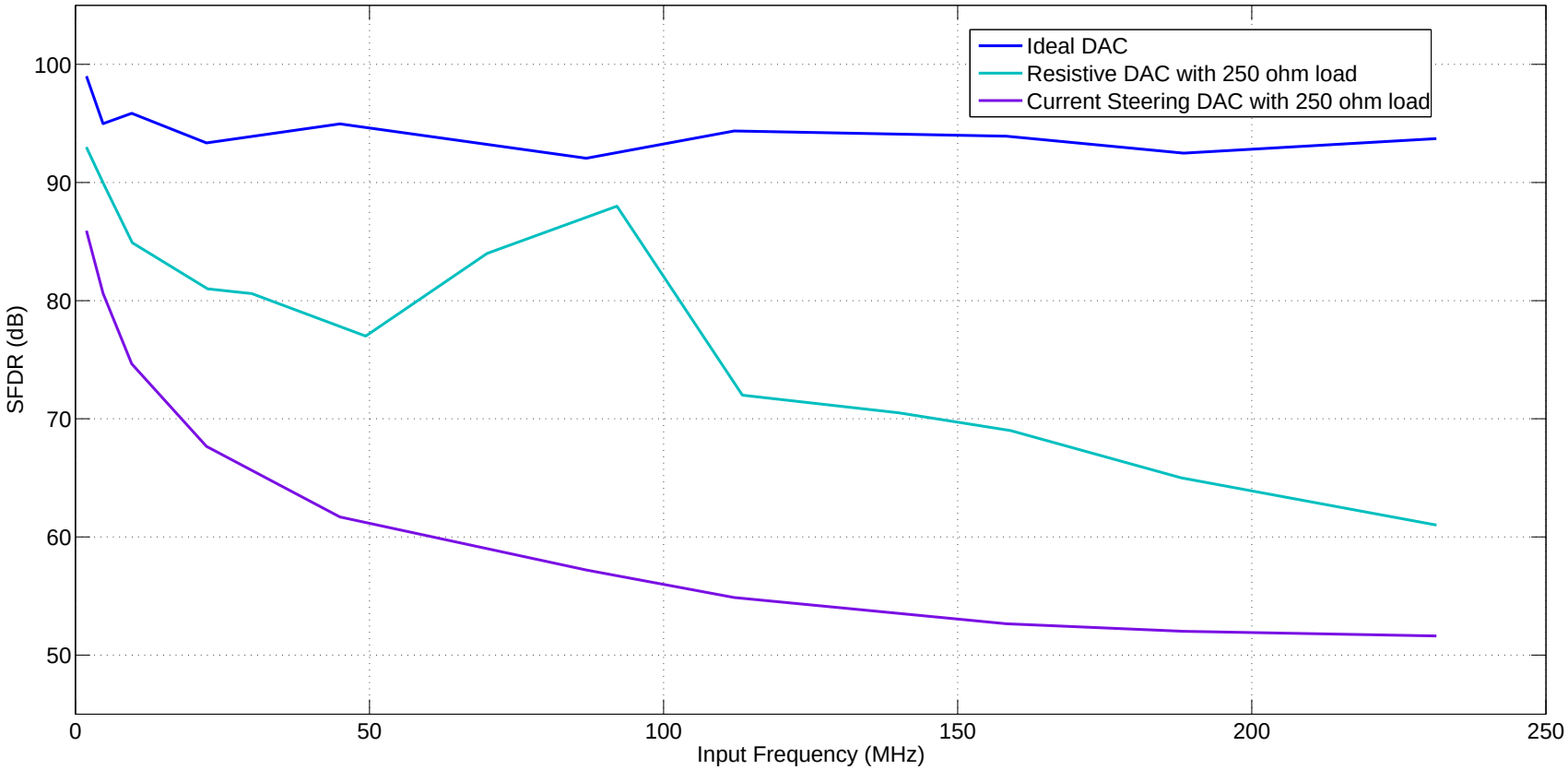

Figure 6.2: SFDR comparison for a 250Ω load

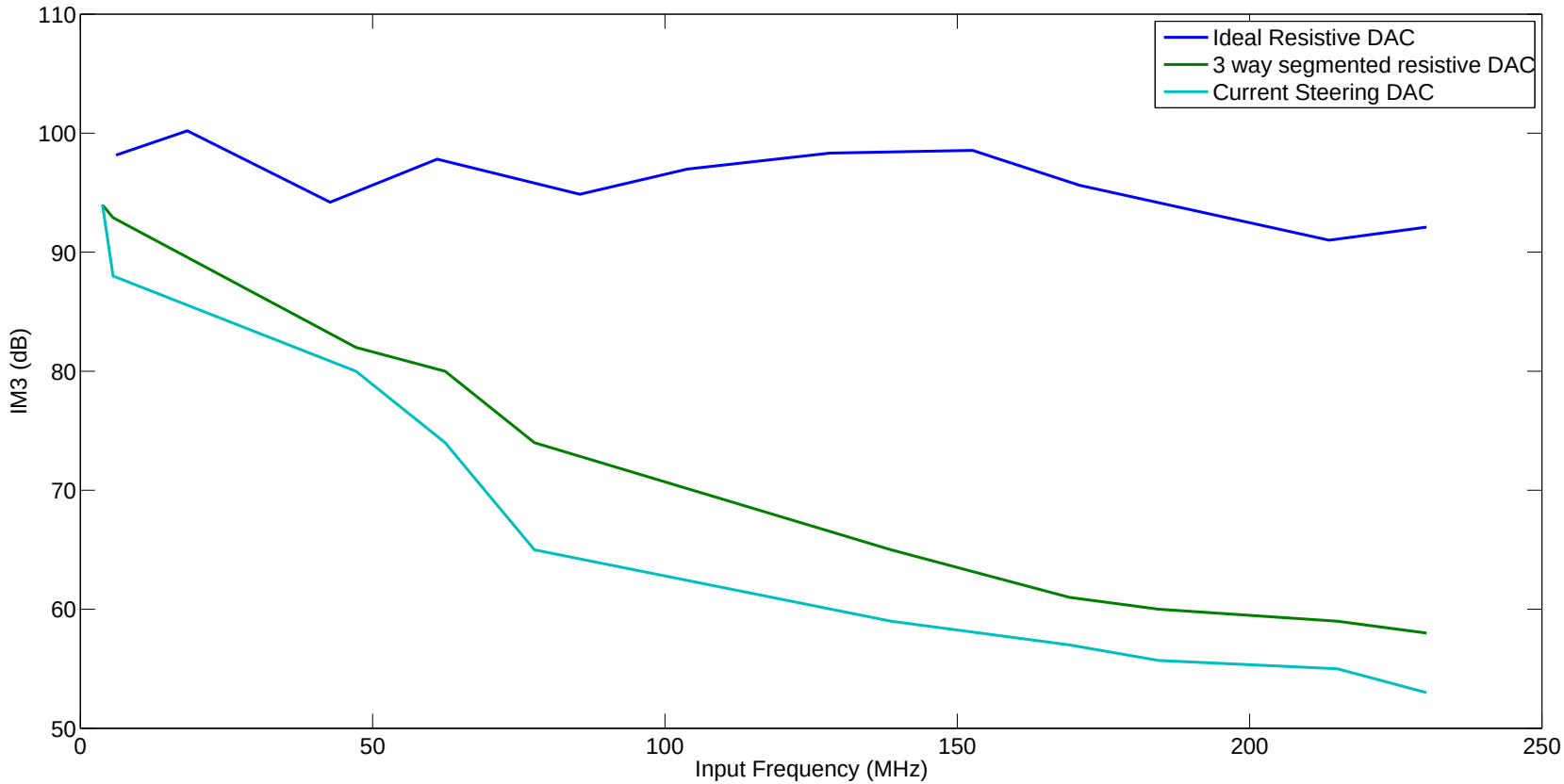

Figure 6.3: Intermodulation Distortion comparison

6.2 Resistor Mismatch - Monte Carlo Simulation

In order to see the effect of resistor mismatch on the DAC performance, Monte Carlo simulations are carried out in Matlab and the DNL and INL plotted for 2000 runs. P+ Unsilicided poly resistors from the ST65 library are considered for our design as they fall in our resistor range and have good temperature and mismatch behavior. In the resistor mismatch model documentation, the RPPO resistors have a standard deviation 12.786 and have a Gaussian distribution. Hence in the Matlab model, the resistors are taken as Normal random variables with the given standard deviation using the normrnd() function. The current through each branch are calculated with these resistors depending upon the input code and added to give the final output current.

A ramp input is given with all 4096 codes. DNL and endpoint INL are plotted for 2000 Monte Carlo runs of the ramp input. For 2000 runs, the INL is seen to be less than 0.4LSB and the DNL is observed to be less than 0.1LSB.

The SFDR (Figure 6.7) is also similarly plotted for by taking an FFT of the output current of the resistor ladder with resistive mismatch. The SFDR is observed to be above 85dB for more than 99% of runs out of the 100 Monte Carlo runs simulated.

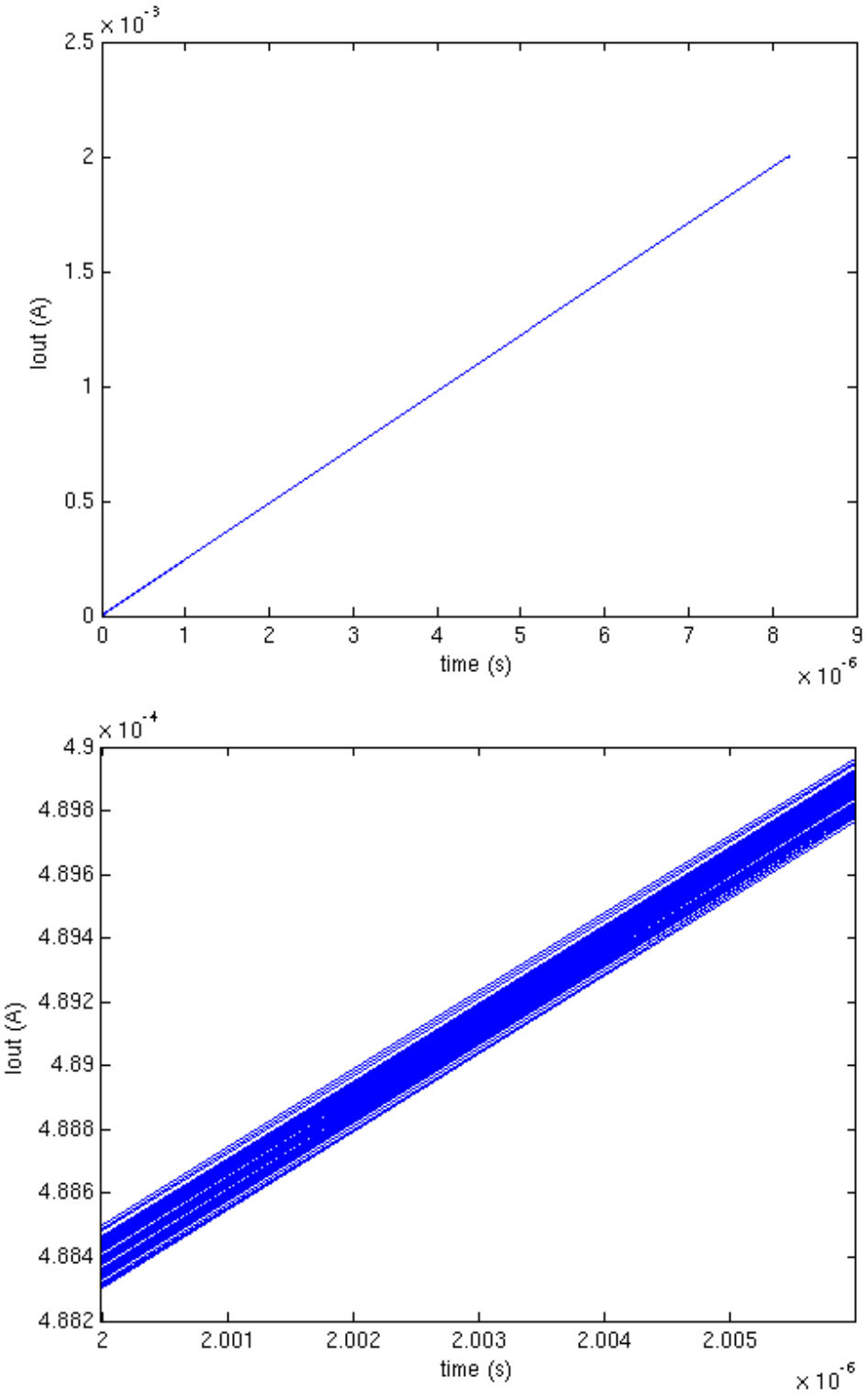

Figure 6.4: Output current with resistor mismatch (100runs MC)

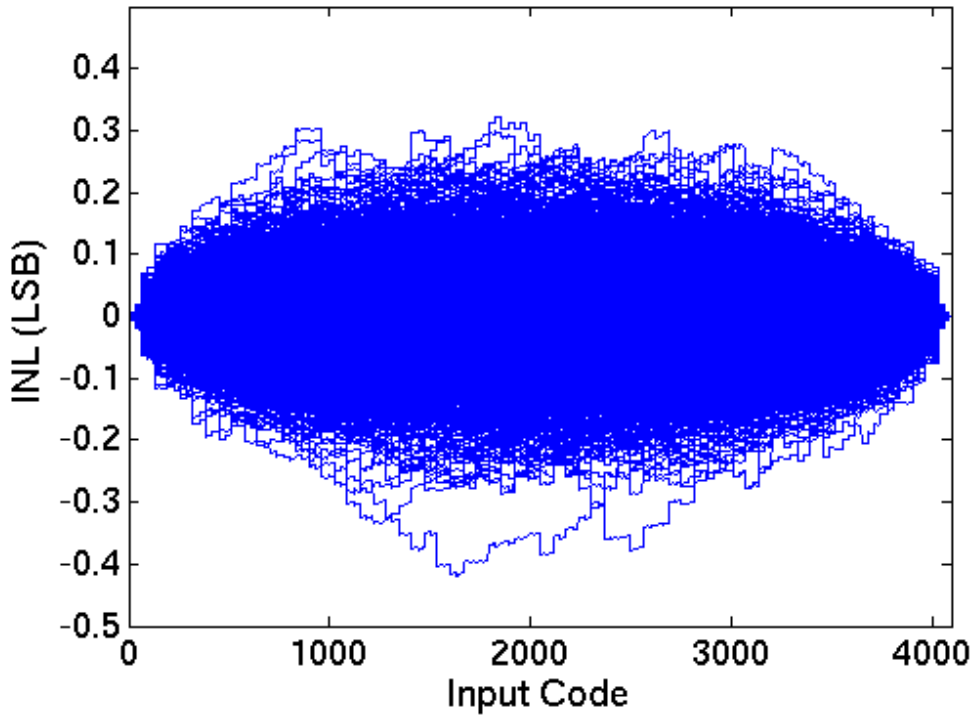

Figure 6.5: Endpoint INL for 2000 runs of Monte Carlo Simulation : Resistor Mismatch

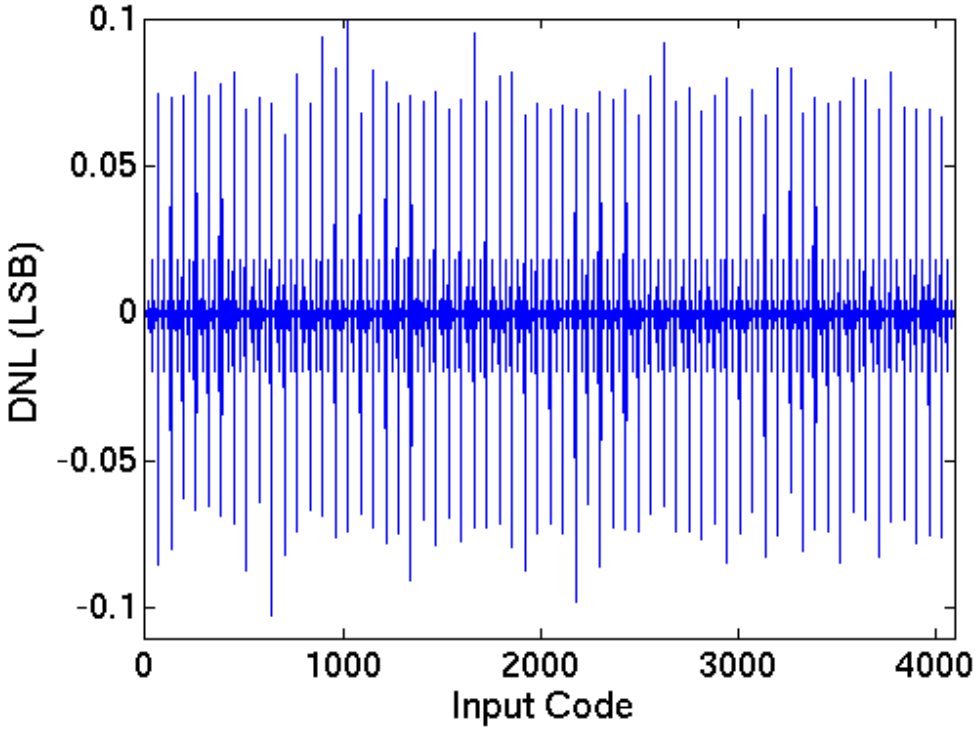

Figure 6.6: DNL for 2000 runs of Monte Carlo Simulation : Resistor Mismatch

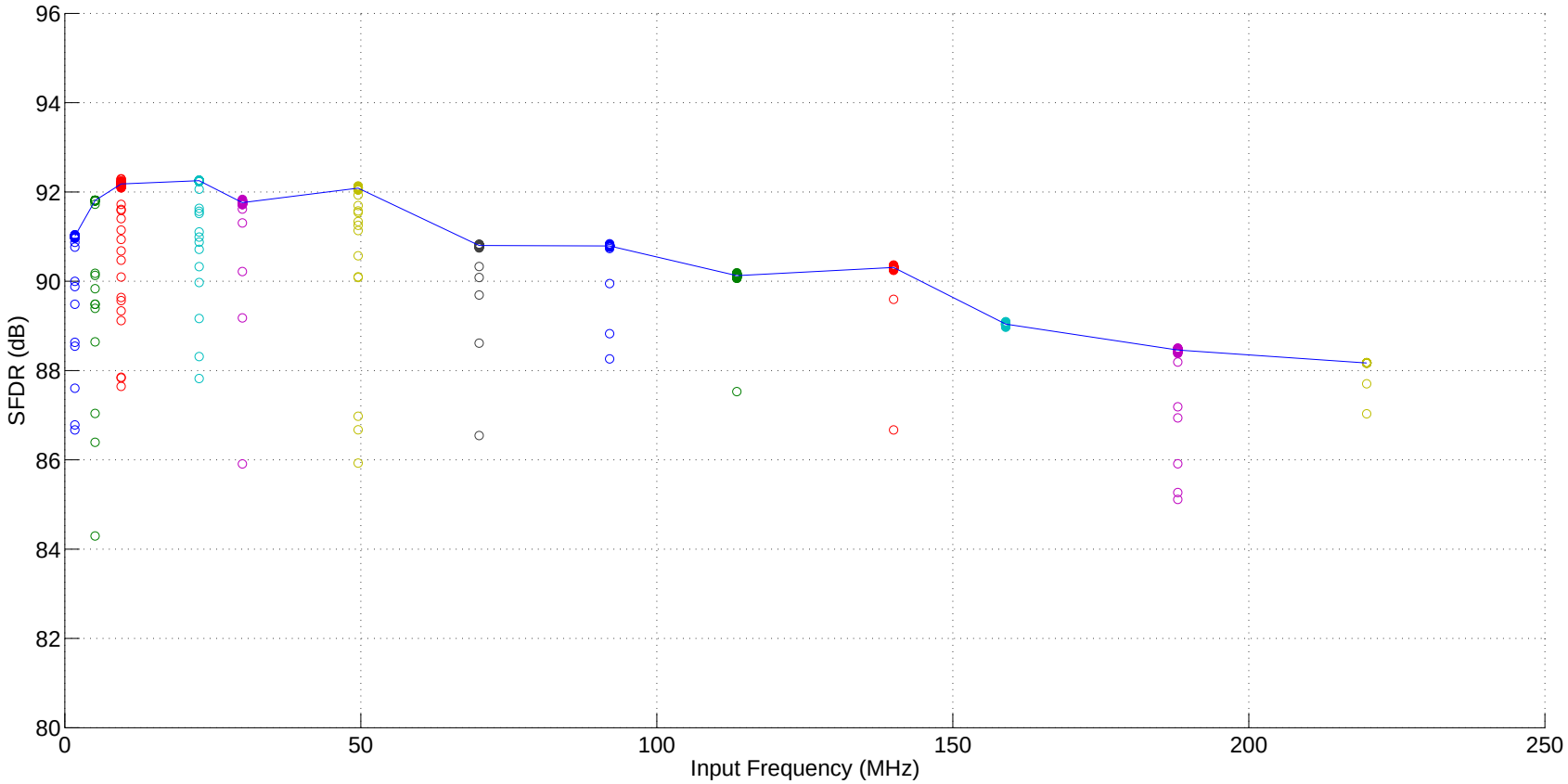

Figure 6.7: SFDR- Monte Carlo scatter plot

CHAPTER 7

CONCLUSIONS

12 bit 500MSPS digital to analog converter is designed in current steering and resistive ladder architectures in 65nm technology. Segmented architecture is considered to optimize for DAC area and performance. The current steering DAC is designed as a 6+6 thermometer + binary weighted segmented design. When characterized for frequency performance, this design is seen to have degradation in SFDR at high frequencies due to non-linearity from finite code dependent output impedance. With current steering DAC, the SFDR is seen to roll off from 90dB at low frequencies to 68dB close to Nyquist frequency. Hence resistive DAC architectures are explored for improved frequency performance. Different segmentations are tried including 6 thermometer+ 6 binary weighted, 6 thermometer + 6 R-2R and 3 way segmented architectures. The DAC designed with a 3 way segmented architecture, 6 thermometer, 3 binary weighted and 3 R-2R bits is seen to give the best frequency performance with ideal I-V opamp, which is subsequently replaced by a real opamp. The I-V opamp is designed as a two stage feedforward compensated architecture with a DC gain of DBMS and a UGB of 7.5GHz. 3 way segmented DAC with real opamp is observed to have a much better dynamic performance compared to the Current Steering counterpart.Monte Carlo analysis is done to account for resistive mismatch and a DNL of 0.1 LSB and an INL of less than 0.4 LSB is obtained. Monte Carlo simulation for SFDR showed a value higher than 85dB for more that 99% of the runs over the signal band. The SFDR with real opamp is around 90dB for frequencies till 100MHz and above 80dB for frequencies till 150MHz. At frequencies close to Nyquist, the SFDR drops to 70dB due to gain limitations from the opamp.Hence a higher gain, higher bandwidth opamp is needed to improve the frequency performance at higher frequencies.

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