3-PHASE 3-WIRE AND 3-PHASE 4-WIRE GRID TIED ACTIVE FRONT END VOLTAGE SOURCE RECTIFIER CONTROL

A Project Report

submitted by

MOHAMED ANSHAD PARI

in partial fulfilment of the requirements
for the award of the degree of

Master of Technology (Power Systems and Power Electronics)
and Bachelor of Technology
in
Electrical Engineering

DEPARTMENT OF ELECTRICAL ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY MADRAS.

MAY 2015

THESIS CERTIFICATE

This is to certify that the thesis titled **3-PHASE 3-WIRE AND 3-PHASE 4-WIRE GRID TIED ACTIVE FRONT END VOLTAGE SOURCE RECTIFIER CONTROL**, submitted by **MOHAMED ANSHAD PARI**, to the Indian Institute of Technology, Madras, for the award of the degree of **Dual-Degree (Bachelor of Technology & Master of Technology)**, is a bona fide record of the project work done by him under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

Dr. Kamalesh Hatua
(Project Guide)
Asst.Professor
Dept. of Electrical Engineering
IIT-Madras, 600 036

Place: Chennai

Date: 6th May 2015

ACKNOWLEDGEMENTS

It gives me great pleasure to express my sincere and heartfelt gratitude to Dr. Kamalesh Hatua for his excellent guidance, motivation and constant support throughout my project . I consider myself extremely fortunate to have had a chance to work under his supervision. I am grateful to him for instilling a passion in the domain of Power Electronics and Drives through his scholarly lectures on Machine Modelling and Power Electronic Control of Electric Machines. Working with him has enhanced my potential on a technical as well as on a personal level and has made the final year of my learning in IITM truly memorable amongst all the five years I had spent here.

I also thank Dr. Shanti Swarup for his valuable support as a mentor during my entire tenure as a student.

I thank Mr. Kothandaraman and Ms. Jayasudha for their help and advice in arranging the hardware setup.

I am truly wordless to express my gratitude to my fellow research scholar Jose Titus for being a pillar of support during my work. Discussions with him helped me to grasp the digital platform which made me a step ahead in my work and trouble shooting sessions with him who has an eagle eye, were worth an experience.

I deeply esteem my fellow students in the Laboratory, especially Parthasarathy and Vamshi Krishna for spending their invaluable time with me, in discussing about the project. I would also extend my thanks to Hridya, Deepthi, Pratap, Aloka, Shekhar, Saravanan, Rajendra, Guru and Poongothai for their support during my work.

This work could not have come to this stage without the support and encouragement from my family. My heartfelt thanks to all of them.

ABSTRACT

KEYWORDS: Active Front End Converter; Voltage Source Rectifier; Vector Control

The aim of the project is modeling and controlling of a 3-phase 3-wire and 3-phase 4-wire voltage source rectifier. These types of converters are generally classified as Active Front End Converter (FEC), since these are connected to front/utility side of the supply. The implemented converter can also be used as a replacement for a diode bridge rectifier for an induction motor drive. Active front end converter ensures bidirectional power flow between AC grid and DC bus. The front end converter maintains a fixed DC bus at all operating conditions. It draws sinusoidal current from the grid and have VAR compensation capability. In this project, vector control of FEC has been implemented in a synchronous reference frame, which is aligned with the a-phase grid voltage. Vector control ensures independent control of both active power and reactive power flow between AC grid and active front end rectifier.

Simulation studies are done for a 10 kVA 3-phase 3-wire and 3-phase 4-wire FEC using MATLAB/SIMULINK to verify the design of the power circuit and control algorithms. The control hardware is developed based on the TMS320F28335 DSP from Texas Instruments, which is indigenously developed in the laboratory. The system design and control software for 3-phase 3-wire and 3-phase 4-wire FEC are experimentally validated on a 10 kVA laboratory prototype. A simple algorithm in order to eliminate the lower order harmonics from the line current of FEC has been implemented.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

ABBREVIATIONS

AFEC	Active Front End Converter
FEC	Front End Converter
AC	Alternating Current
DC	Direct Current
VSI	Voltage Source Inverter
FOC	Field Oriented Control
PI	Proportional and Integral
IGBT	Insulated Gate Bipolar Transistor
UPS	Uninterpretable Power Supply
PWM	Pulse Width Modulation
PLL	Phase Locked Loop
KVL	Kirchhoff's voltage law
SPWM	Sinusoidal Pulse Width Modulation
SVPWM	Space Vector Pulse Width Modulation
THD	Total Harmonic Distortion
CCS	Code Composer Studio
ADC	Analog to Digital Converter
$\boldsymbol{I^2C}$	Inter Integrated Circuit
CAN	Controller Area Network
JTAG	Joint Test Action Group
DMA	Direct Memory Access
PIE	Peripheral Interrupt Expansion
OTP	One Time Programmable
SARAM	Single Access RAM
ROM	Read Only Memory
PD	Protection and Delay

NOTATION

V_{sa}, V_{sb}, V_{sc}	Instantaneous grid voltages in *abc* frame, V
V_m	peak value of the grid voltage
$V_{s\alpha}, V_{s\beta}$	Instantaneous grid voltages in $\alpha\beta$ frame, V
V_{sd}, V_{sq}, V_{s0}	Instantaneous grid voltages in *dq0* frame, V
I_{sa}, I_{sb}, I_{sc}	Instantaneous line currents in *abc* frame, A
$I_{s\alpha}, I_{s\beta}$	Instantaneous line currents in $\alpha\beta$ frame, A
I_{sd}, I_{sq}, I_{s0}	Instantaneous line currents in *dq0* frame, A
L_f	Line side inductance , mH
L_c	Common mode inductance , mH
R_f	Coil resistance associated with the line side inductor, Ω
C_{dc}	DC bus capacitance , μF
R_dC	Load resistance , Ω
$V_{ina}, V_{inb}, V_{inc}$	Instantaneous pole voltages of the inverter in *abc* frame, V
$V_{in\alpha}, V_{in\beta}$	Instantaneous pole voltages of the inverter in $\alpha\beta$ frame, V
V_{ind}, V_{inq}	Instantaneous pole voltages of the inverter in *dq* frame, V
ω	Grid frequency, rad/s
θ	Instantaneous angle of *a*-phase grid voltage, rad
V_{dc}	Instantaneous DC bus voltage, V
e_{ffd}, e_{ffq}	*d* and *q*-axis feed forward terms, V
K_p	Proportional gain of the PI controller
K_i	Integral gain of the PI controller
G	Gain of the inverter
I_{sd_n}, I_{sq_n}	*nth* harmonic component in the line currents in *dq* frame, A
I_n	Instantaneous neutral current, A

CHAPTER 1

INTRODUCTION

In the present scenario renewable energy has become major focus for the research. Among renewable sources Solar Power is efficient and environment friendly one. India has tremendous scope of generating solar energy. The geographical location of the country stands a benefit to this. Almost all parts of India receive 4-7 kWh of solar radiation per sq meters. To meet the surge demand of electricity, solar energy is the best form of energy needs of India and bridge the energy demand-supply gap.

In near future, solar energy must be used as the prime source of electricity. But one of the main challenge to supply solar power is its synchronization from all the distributed generation. Solar PV panels supplies power at different DC voltage levels. They are converted to 3-phase AC voltages and connected to the conventional 440 V grid. A 3-phase grid tied front end converter generally used for the DC to AC conversion. In this project both 10 kVA front end 3-phase 3-wire and 3-phase 4-wire grid tied inverter controller implemented and tested.

1.1 Back ground of the project

A Grid-Tied inverter is a power converter that converts DC current to AC current with an ability to synchronize with distribution Grid. Unlike in the transmission 3-phase 3-wire system, a 3-phase 4-wire system is necessary in the distribution side. A 3-phase 4-wire system requires additional controllers from a 3-phase 3-wire system. The inverter implemented in the laboratory has a 800 V DC bus and it is connected to a 440 V supply.

In the implemented system AC power from the grid will be converted to a DC voltage of 800 V, and this DC power will in turn fed into a resistance. The implemented converter is capable of bi-directional power flow. A two-level voltage

source inverter (VSI) is used as grid tied inverter. The implemented converter is essentially a current controlled voltage source. This type of converters are generally classified as Front End Converter (FEC), since these are connected to front/utility side of the supply. The implemented converter can also be used as a replacement for a diode bridge rectifier for a induction motor drive. In this way the regulation capability of the drive can be ensured with superior input current quality.

The ideal requirements of a FEC are as follows

- DC bus voltage control
- Sinusoidal input current with any given power factor
- Bi-directional power flow
- Good dynamic response

1.1.1 Vector Control for FEC

The principle of Vector Control or Field Oriented Control (FOC) was originally developed by F. Blaschke and K. Hasse in Germany by the late 1960s for control of induction machine. The basic idea of this scheme is to control the flux producing and torque producing components of the induction motor in an independent manner. In induction machine the outer loop controls the speed of the motor, while the inner loop controls the current vector, which are producing torque and flux. Because of this fact the speed control of induction machine can be easily achieved[1]. Similar control technique can be adopted for power flow control of FEC [2; 3].

In this method, 3-phase grid voltages and line currents are converted into an equivalent 2-axes reference frame, which is stationary in nature. They are further converted into a synchronous reference frame, which rotates with grid (synchronous) frequency. In synchronous reference frame, the components of current corresponding to active and reactive power are controlled in an independent (orthogonal coordinates) manner similar to the torque and flux producing components in a motor drive. It is important to note that in synchronous reference

frame voltage and current become DC quantity. Therefore it is easy to implement these controllers using conventional PI controllers.

Though the technique of vector control was developed at late 1960's, it could not be readily realized in practice as the method is computationally intensive. However, with the advancement in the digital processors, today implementation of vector control algorithm is simple.

1.2 Power Structure of the System

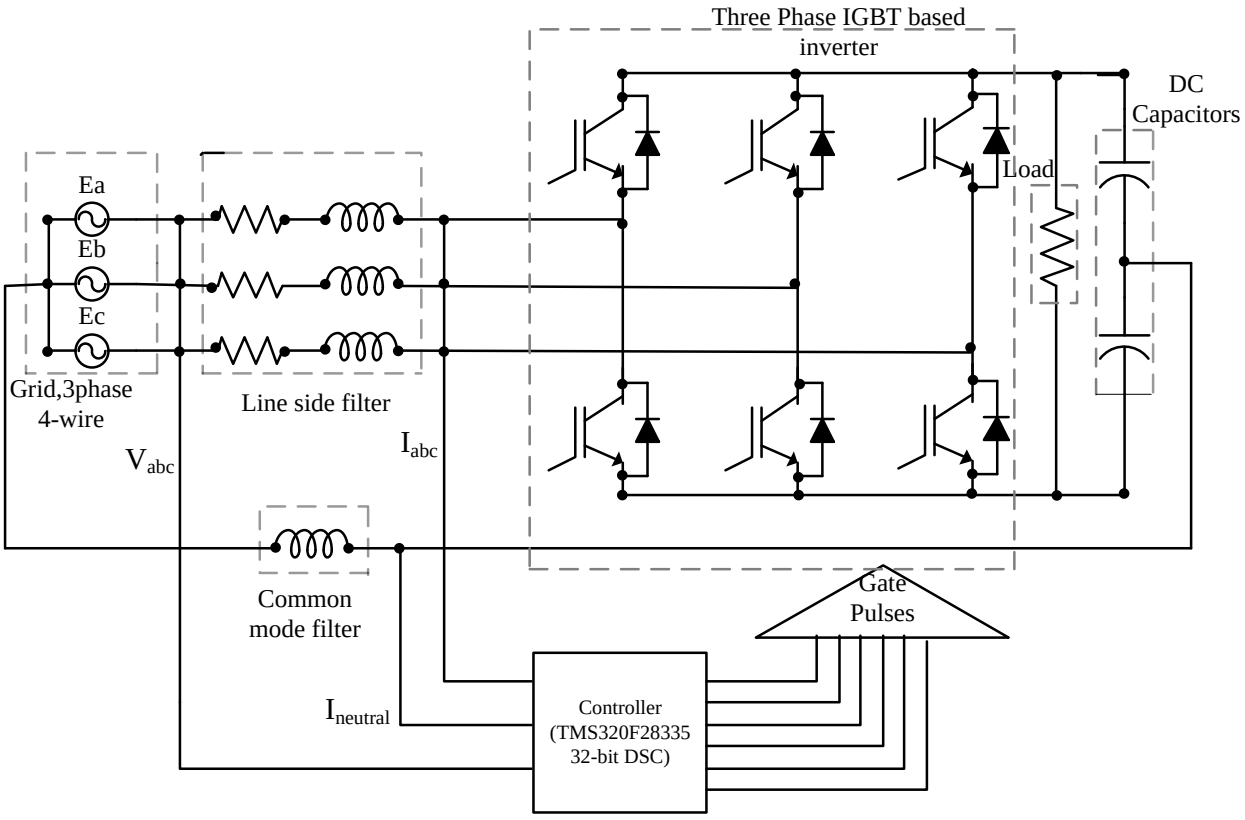


Fig. 1.1 Power structure of the system

The power structure of FEC consists of, a 3-phase 4-wire grid-tied inverter through line inductance, common mode filter, resistive load across DC bus and Digital Signal Controller(DSC). The power structure of FEC used is shown in Fig. 1.1. The controller is an indigenously developed 32-bit floating point Digital Signal Controller(DSC).

1.3 Goals of the Project Work

In this project two FEC configurations are implemented in a 10 kVA setup. The two configurations are 3-phase 3-wire and 3-phase 4-wire system. In applications where neutral wire connection to the inverter is of mandatory, there 3-phase 4-wire system is used. In general for motor drive applications, 3-phase 3-wire systems are used. In applications like battery charger, UPS and grid tied inverter 3-phase 4-wire inverter connection is mandatory [4; 5; 6]. For a 3-phase 4-wire system, the control techniques needs few modifications from the 3-phase 3-wire system.

1.3.1 Vector control of 3-phase 3-wire FEC and 3-phase 4-wire FEC

Achievements with the 3-phase 3-wire FEC and 3-phase 4-wire FEC, in this project are listed below.

Vector control: In synchronous reference frame independent control of both active and reactive power control is possible. Since in the synchronous reference frame all the quantities are DC, a simple PI controller will make steady state error zero.

Soft start-up: Soft start-up algorithm helps the output voltage build gradually, keeping the starting current low.

DC bus voltage regulation: DC bus will remain same voltage as reference voltage within the prescribed load.

Operation at desired power factor: Achieved both lagging and leading power factor operation of FEC.

Different PWM techniques: Both sinusoidal and space vector modulation schemes has been experimented.

Elimination of lower order harmonic components from the line current: Effective elimination of $5th$ and $7th$ harmonic components of line current without increasing bandwidth of the controllers has been done.

Elimination of zero sequence current: Eliminated zero sequence current, that is current that flowing through the neutral wire in a 3-phase 4-wire FEC with the help of a neutral current controller.

Neutral current distortions: Analyzed the effect on neutral current distortions with sinusoidal and space vector modulation schemes in a 3-phase 4-wire FEC.

1.4 Organisation of Thesis

Chapter 2 presents a detailed description on the theory of space phasors, detailed modeling and analysis of 3-phase 3-wire Front End converter and 3-phase 4-wire FEC with different modulation techniques. The chapter also describes the control strategy for the FEC and techniques for elimination of harmonics from the line current. Front End Converter (FEC) is presented along with the relevant equations.

Chapter 3 deals with the hardware organization for the implementation of FEC on a 10 kVA laboratory prototype. Some of the basic capabilities and features of the control platform, which is indigenously developed in the laboratory based on the TMS320F28335 Digital Signal Controller (DSC), from Texas Instruments, that are used in the control implementation. And the protection and delay card that acts as the interface between the controller and the inverter is discussed. It also describes the digital implementation FEC control system using per unitisation technique. The design of current controllers and voltage controllers used in the vector control scheme are presented.

Chapter 4 Discusses the results obtained from the simulation for the 10 kVA FEC (both 3-wire and 4-wire) as well as that from the actual hardware implementation on the 10 kVA FEC (both 3-wire and 4-wire).

Chapter 5 Presents the summary of the work done and the future scope for improving the work.

CHAPTER 2

Modeling, Analysis and Control of 3-phase 3-wire and 3-phase 4-wire Front End Converter

2.1 Introduction

In this chapter modeling and control technique for a 3-phase 3-wire and a 3-phase 4-wire front end converter(FEC) are discussed. The three phase voltages and line currents of a FEC are analyzed with complex space vectors and control techniques adopted for the FEC are implemented in a synchronous reference frame. Proposed control uses coordinate transformations which transforms voltages and currents of a three phase stationary system to a revolving two coordinate time invariant system which rotates at the grid frequency and synchronized with a-phase grid voltage.

Relevant equations for control are derived in rotating reference frame and the basic scheme for the control is presented. Deign methodology of a simple phase locked loop (PLL) adopted to determine the rotating voltage reference frame is discussed. Elimination of lower order harmonics ($5th$ and $7th$) from the line current of the FEC also described in this chapter.

2.2 Vector Control of FEC

The concept of vector control for a 3-phase 3-wire FEC is described in following section.

Figure 2.1, shows power architecture of a 3-phase 3-wire PWM rectifier which have a IGBT based two-level VSI, necessary filter inductor and DC bus capacitor. DC bus of the rectifier is formed by two identical series connected capacitors.

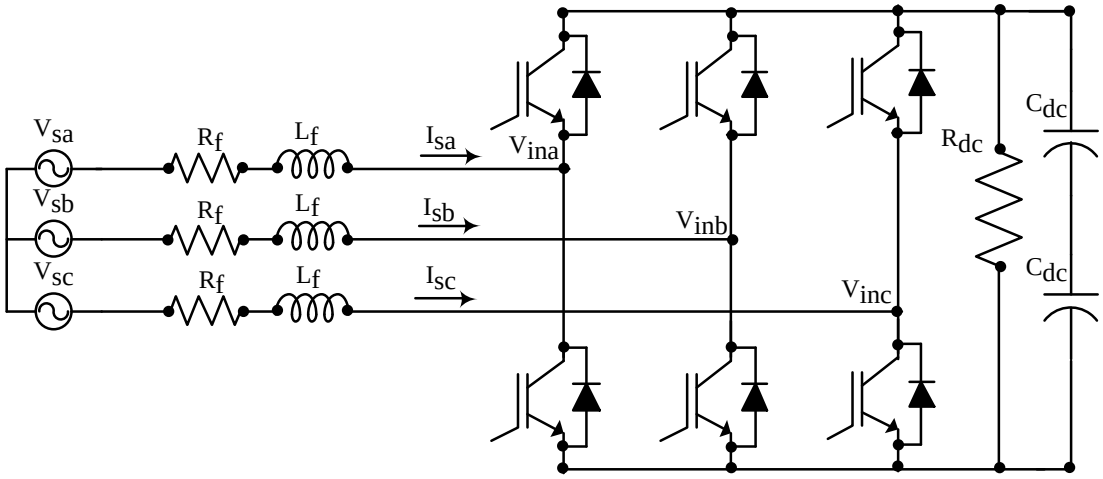


Fig. 2.1 3-phase 3-wire FEC

The three phase balanced grid voltages are given below

$$Vsa(t) = VmCos(wt) \tag{2.1}$$

$$Vsb(t) = VmCos(wt - 2\pi/3) \tag{2.2}$$

$$Vsc(t) = VmCos(wt + 2\pi/3) \tag{2.3}$$

Where V_{sa}, V_{sb} and V_{sc} are three phase voltages. Transforming equations (2.1)-(2.3) into α-β (stationary) reference frame [7].

$$\vec{V}_{3-\phi} = [V_{sa}(t) + V_{sb}(t)e^{j(2\pi/3)} + V_{sc}(t)e^{j(4\pi/3)}] \tag{2.4}$$

$$= V_{s\alpha} + jV_{s\beta} \tag{2.5}$$

where

$$V_{s\alpha} = V_{sa}(t) - \frac{1}{2}V_{sb}(t) - \frac{1}{2}V_{sc}(t) \tag{2.6}$$

$$= \frac{3}{2}V_m Cos(wt) \tag{2.7}$$

$$V_{s\beta} = \frac{\sqrt{3}}{2}[V_{sb}(t) - V_{sc}(t)] \tag{2.8}$$

$$= \frac{3}{2}V_m Sin(wt) \tag{2.9}$$

Thus the grid voltage can be written in space vector format as given in Eq.(2.12).

$$\vec{V_s} = V_{s\alpha} + jV_{s\beta} \tag{2.10}$$

$$= \frac{3}{2}V_m[Cos(wt) + jSin(wt)] \tag{2.11}$$

$$= \frac{3}{2}V_m e^{jwt} \tag{2.12}$$

The Eq.(2.12) explains that, the voltage space vector ($\vec{V_s}$) has a magnitude of $\frac{3}{2}V_m$ and it rotates with an angular speed of w with respect to a stationary reference frame in the anti-clockwise direction. Hence space vector ($\vec{V_s}$) makes an angle $wt = \theta$ at any given instant of time with respect to the α-axis. Therefore, it is able to choose a synchronous d-q reference frame which rotates with an angular speed of w in the anti-clockwise direction and making an angle $wt = \theta$ at any given instant of time with respect to the α-axis as shown in the figure 2.2. Here the synchronous reference frame is selected in such a way that grid voltage space vector ($\vec{V_s}$) is aligned along d-axis so that its component along q-axis is zero. Since grid voltage space vector ($\vec{V_s}$) and d-q axis rotating at same speed w as shown in figure 2.2, then these are seemed to be stationary with respect to each other thus grid voltage space vector appeared as DC quantity in d-q reference frame.

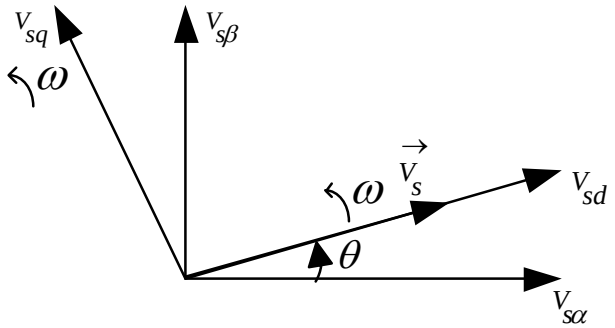


Fig. 2.2 α-β and d-q frames phasor representation

From the figure 2.2 derivation of the equation for $\vec{V_s}$ in d-q reference frame is

given below

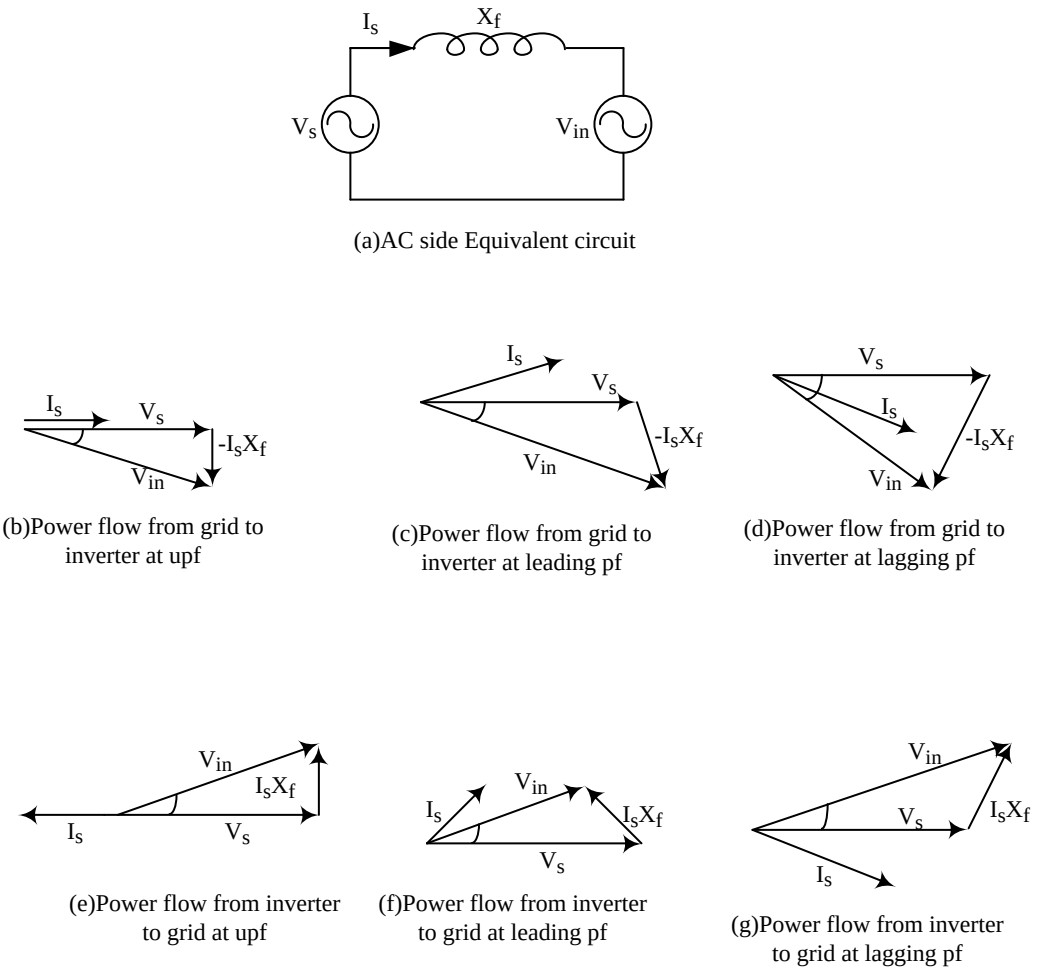
$$V_{sd} = V_{s\alpha}Cos\theta + V_{s\beta}Sin\theta \quad (2.13)$$

$$V_{sq} = V_{s\beta}Cos\theta - V_{s\alpha}Sin\theta \quad (2.14)$$

2.3 Ideal Operation of Front End Converter

The possible modes of operations of a FEC are shown using phasor diagrams in figure 2.3.

In the figure 2.3, V_s indicates grid voltage and V_{in} indicates per phase inverter



(a)AC side Equivalent circuit

(b)Power flow from grid to inverter at upf

(c)Power flow from grid to inverter at leading pf

(d)Power flow from grid to inverter at lagging pf

(e)Power flow from inverter to grid at upf

(f)Power flow from inverter to grid at leading pf

(g)Power flow from inverter to grid at lagging pf

Fig. 2.3 Equivalent circuit and phasor diagrams of the FEC

output voltage. It is known that active power flows from leading voltage to lagging voltage, and reactive power flows from higher magnitude of voltage to lower mag-

nitude of voltage. Therefore in FEC control, phase and magnitude of the inverter voltage is adjusted in such a way that desired reactive and real power flows into the inverter from the grid. If unity power factor current of magnitude I_s is desired to be drawn from the grid, then the inverter voltage can be obtained by vectorially adding grid voltage (V_s) and negating the reactive drop ($I_s X_f$) as shown in figure 2.3(b). In the similar way vector diagram for real power flow and reactive power flow at different possible operating conditions are shown in figures 2.3(b)-2.3(g).

2.4 Modeling of 3-phase 3-wire Front End Converter

In this section modeling of a 3-phase 3-wire FEC is discussed. As mentioned earlier, the modeling and controller design has carried out in the rotating *d-q* reference frame. The rotating reference frame is obtained from the grid voltage.

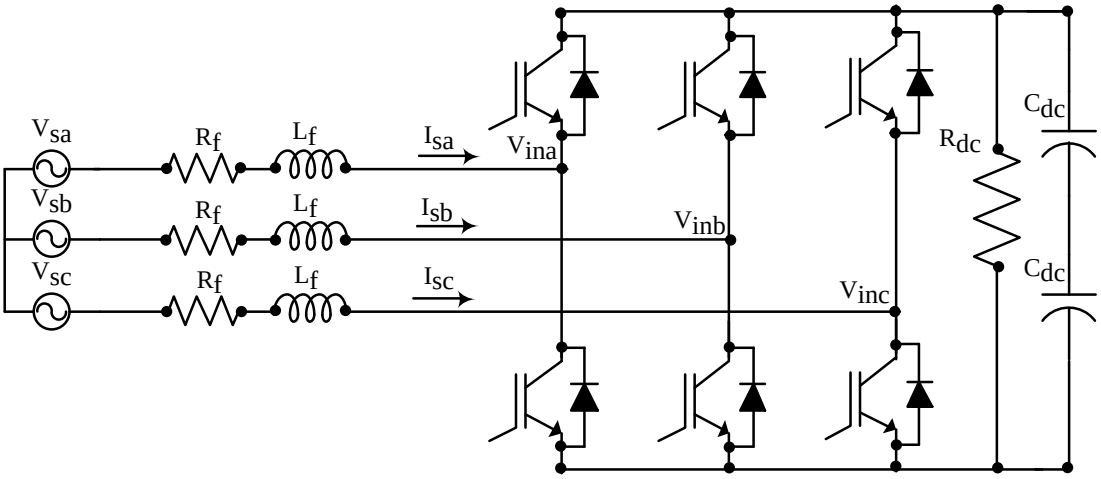


Fig. 2.4 3-phase 3-wire FEC circuit diagram

3-phase balanced grid voltages for the 3-phase 3-wire FEC are given below.

$$Vsa(t) = VmCos(wt) \tag{2.15}$$

$$Vsb(t) = VmCos(wt - 2\pi/3) \tag{2.16}$$

$$Vsc(t) = VmCos(wt + 2\pi/3) \tag{2.17}$$

Applying KVL to circuit 2.4, voltage equations for 3-phase 3-wire FEC can be obtained as given below.

$$Vsa = R_f I_{sa} + L_f \frac{dI_{sa}(t)}{dt} + V_{ina} \tag{2.18}$$

$$Vsb = R_f I_{sb} + L_f \frac{dI_{sb}(t)}{dt} + V_{inb} \tag{2.19}$$

$$Vsc = R_f I_{sc} + L_f \frac{dI_{sc}(t)}{dt} + V_{inc} \tag{2.20}$$

Eq.(2.21) can be obtained by transforming the equations (2.18), (2.19) and (2.20) into the α-β reference frame.

$$\vec{V}_s^{\alpha-\beta} = R_f \vec{I}_s^{\alpha-\beta} + L_f \frac{d\vec{I}_s^{\alpha-\beta}(t)}{dt} + \vec{V}_{in}^{\alpha-\beta} \tag{2.21}$$

In Eq.(2.21), $\vec{V}_s^{\alpha-\beta}$ is the grid voltage space vector in α-β reference frame, $\vec{I}_s^{\alpha-\beta}$ is the line current space vector in α-β reference frame and $\vec{V}_{in}^{\alpha-\beta}$ is the inverter pole voltage in α-β reference frame.
$\vec{V}_s^{d-q}$ is the grid voltage space phasor observed from rotating (d-q) reference frame. Therefore Eq.(2.21) can be rewritten as

$$\vec{V}_s^{d-q}(t)e^{j\theta} = R_f \vec{I}_s^{d-q} e^{j\theta} + L_f \frac{d(\vec{I}_s^{d-q}(t)e^{j\theta})}{dt} + \vec{V}_{in}^{d-q} e^{j\theta} \tag{2.22}$$

$$(V_{sd} + jV_{sq})e^{j\theta} = R_f(I_{sd} + jI_{sq})e^{j\theta} + L_f \frac{d(I_{sd} + jI_{sq})e^{j\theta}}{dt} + (V_{ind} + V_{inq})e^{j\theta} \tag{2.23}$$

$$\text{where } L_f \frac{d(I_{sd}+jI_{sq})e^{j\theta}}{dt} = L_f \frac{dI_{sd}}{dt} e^{j\theta} + j\omega L_f I_{sd} e^{j\theta} + jL_f \frac{dI_{sq}}{dt} e^{j\theta} - \omega L_f I_{sq} e^{j\theta} \tag{2.24}$$

It is important to note that equations (2.22) and (2.23) are still in the α-β reference frame.
Substituting equation Eq.(2.24) in equation Eq.(2.23), FEC equation in d-q reference frame can be obtained after multiplying Eq.(2.23) with $e^{-j\theta}$. The d-axis and q-axis components of FEC voltage equation in d-q reference frame can be obtained by multiplying Eq.(2.23) with $e^{-j\theta}$ and equating real and imaginary parts

as follows

$$V_{sd} = R_f I_{sd} + L_f \frac{dI_{sd}}{dt} - \omega L_f I_{sq} + V_{ind} \quad (2.25)$$

$$V_{sq} = R_f I_{sq} + L_f \frac{dI_{sq}}{dt} + \omega L_f I_{sd} + V_{inq} \quad (2.26)$$

Eq. (2.25) and Eq. (2.26) together explain the front end converter equation in d-q reference frame. Eq. (2.25) and Eq. (2.26) can be rewrite as given in Eq. (2.27) and Eq. (2.28) (since, $V_{sq} = 0$).

$$V_{ind} = -R_f I_{sd} - L_f \frac{dI_{sd}}{dt} + e_{ffd} \quad (2.27)$$

$$V_{inq} = -R_f I_{sq} - L_f \frac{dI_{sq}}{dt} + e_{ffq} \quad (2.28)$$

Where, $e_{ffd} = -V_{sd} - \omega L_f I_{sq}$ and $e_{ffq} = \omega L_f I_{sd}$ are the d-axis and q-axis feed forward terms respectively.

2.5 Control Strategy for FEC

As mentioned earlier, control of the FEC has been done in synchronous (d-q) reference frame. The objectives of the FEC control are as follows.

- Maintaining DC bus voltage at a fixed reference value
- Control of real power flow from the grid
- Control of reactive power flow from the grid

All the above criteria for the control can be achieved through conventional vector control techniques [8]. All the above vector controller loops are shown in figure 2.5. In figure 2.5, V_{dc} and V_{dc}^* are the actual and reference DC bus voltage respectively, I_{sd} and I_{sq} are the d and q-axis component of the line current vector in the d-q reference frame, I_{sd}^* and I_{sq}^* are the reference for d and q-axis component of the line current vector in the d-q reference frame, e_{ffd} and e_{ffq} are the feed forward terms in the d and q-axis respectively and V_{ind}^* and V_{inq}^* are the reference pole voltage of the inverter in the d-q reference frame.

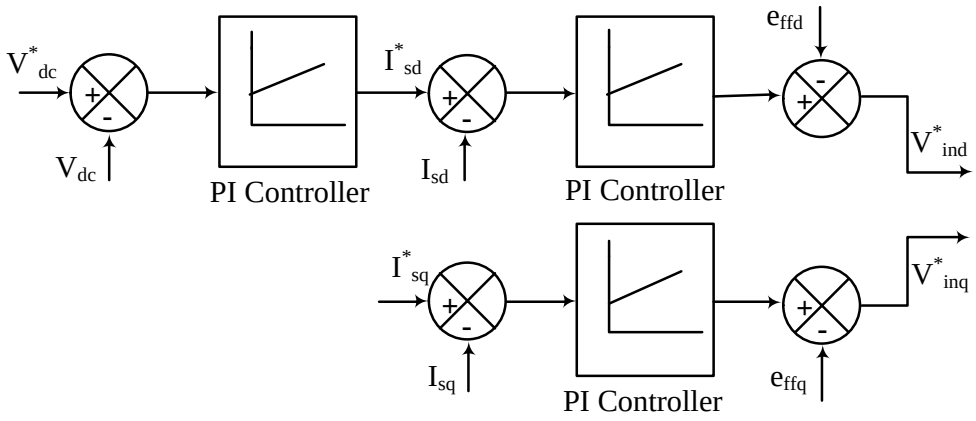


Fig. 2.5 Vector Controller Loops

The DC bus voltage regulation is possible through a PI controller, which takes the difference between actual DC bus voltage and reference DC value as the input. The output of the DC bus voltage controller will be the reference for I_{sd} controller. I_{sd} controller controls the real power flow from the grid, since I_{sd} is a measure of real power (P) as shown in Eq.(2.29). The reactive power flow control from the grid is possible through by controlling I_{sq}, since I_{sq} is a measure of reactive power (Q) as shown in Eq.(2.30). Feed forward terms e_{ffd} and e_{ffq} are added at the output of I_{sd} and I_{sq} controller respectively, in order to get the V^*_{ind} and V^*_{inq}. V^*_{ind} and V^*_{inq} will then used for the PWM generation.

$$P = \frac{2}{3}[V_{sd}I_{sd} + V_{sq}I_{sq}] = \frac{2}{3}V_{sd}I_{sd} \tag{2.29}$$

$$Q = \frac{2}{3}[V_{sq}I_{sd} - V_{sd}I_{sq}] = -\frac{2}{3}V_{sd}I_{sq} \tag{2.30}$$

The overall block diagram of a vector controlled 3-phase 3-wire FEC in *d-q* reference frame is shown in figure 2.6.The grid voltages and line currents are transformed into *d-q* reference frame from the stationary reference frame, and are used as feedback variables for the controller. The control calculations are performed in the *d-q* reference frame.

The vector controller has an outer DC voltage controller loop and two inner

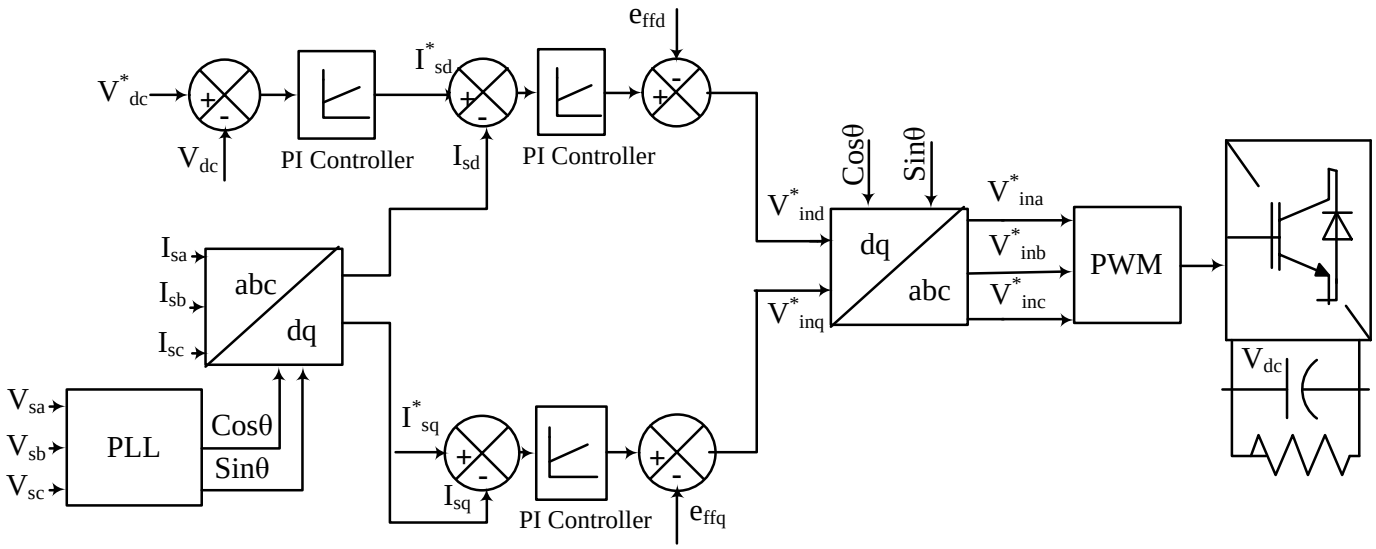


Fig. 2.6 Control structure of FEC in *d-q* reference frame

current controller loops. V^*_{ind} and V^*_{inq}, which are obtained after adding feed forward terms to the inner controller loops are transformed into stationary reference frame as V^*_{ina}, V^*_{inb} and V^*_{inc}. V^*_{ina}, V^*_{inb} and V^*_{inc} are the three phase modulating voltages in the stationary reference frame, which are used to generate PWM pulses. The generated pulses will go to the IGBT gate driver and required pole voltages will be generated at the inverter terminals.

The transformations from the stationary to *d-q* reference frame and *d-q* to stationary reference frame requires information about $Cos\theta$ and $Sin\theta$, where θ is angle made by *d*-axis with α-axis at any instant of time. The information about $Cos\theta$ and $Sin\theta$ can be obtained from a Phase Locked Loop (PLL). The structure of a PLL is explained in the following section.
The details about PI controller design, feed-forward terms and PWM generation are also explained in the subsequent sections.

2.5.1 Phase Locked Loop (PLL)

PLL plays a major role in the controller part as it will give position information of the utility grid voltage at any instant of time. These $Cos\theta$ and $Sin\theta$ will be used in the transformations of voltage and current between stationary reference

frame and synchronous reference frame[9]. The block diagram of PLL which is used in the project is shown in figure 2.7. The three phase balanced grid voltages

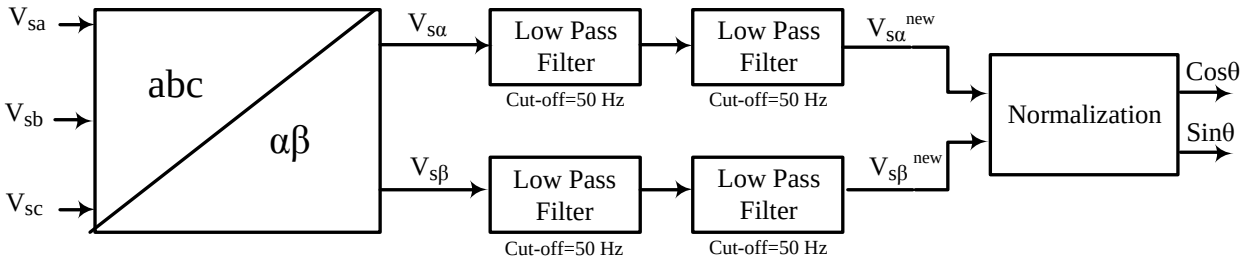


Fig. 2.7 PLL Block Diagram

are transformed into α-β reference frame. After that it will pas through two low pass filters of cut-off frequency equals to $50Hz$. By normalizing the output with appropriate values, $Sin\theta$ and $Cos\theta$ can be generated.

The three phase balanced grid voltages are given below, here the assumption is that grid frequency $w = 2\pi * 50rad/s$ is a constant.

$$\begin{aligned} Vsa(t) &= VmCos(wt) \\ Vsb(t) &= VmCos(wt - 2\pi/3) \\ Vsc(t) &= VmCos(wt + 2\pi/3) \end{aligned}$$

3-phase to α-β transformations yield

$$\begin{aligned} V_{s\alpha} &= V_{sa}(t) - \frac{1}{2}V_{sb}(t) - \frac{1}{2}V_{sc}(t) \\ &= \frac{3}{2}V_{sa}(t) \\ &= \frac{3}{2}V_m Cos(wt) \qquad (2.31) \\ V_{s\beta} &= \frac{\sqrt{3}}{2}[V_{sb}(t) - V_{sc}(t)] \\ &= \frac{3}{2}V_m Cos(wt - \pi/2) \\ &= \frac{3}{2}V_m Sin(wt) \qquad (2.32) \end{aligned}$$

Since each low pass filter will produce a gain of $\frac{1}{\sqrt{2}}$ and a phase shift of $\frac{-\pi}{4}$, the output of two cascaded low pass filters with the corresponding inputs $V_{s\alpha}$ and $V_{s\beta}$ will be

$$\begin{aligned}
[V_{s_\alpha}^{new} + jV_{s_\beta}^{new}] &= \frac{1}{2}[V_{s\alpha} + jV_{s\beta}]e^{-j\pi/2} \\
V_{s_\alpha}^{new} &= \frac{1}{2} * \frac{3}{2} * V_m Cos(wt - \pi/2) \\
&= \frac{1}{2} * \frac{3}{2} * V_m Sin(wt) \qquad (2.33) \\
V_{s_\beta}^{new} &= \frac{1}{2} * \frac{3}{2} * V_m Sin(wt - \pi/2) \\
&= [-1]\frac{1}{2} * \frac{3}{2} * V_m Cos(wt) \qquad (2.34) \\
& \qquad (2.35)
\end{aligned}$$

The normalization in order to get $Sin\theta$ and $Cos\theta$ is explained below

$$Cos\theta = \frac{-V_{s_\beta}^{new}}{\sqrt{(V_{s_\alpha}^{new})^2 + (V_{s_\beta}^{new})^2}} \qquad (2.36)$$

$$Sin\theta = \frac{V_{s_\alpha}^{new}}{\sqrt{(V_{s_\alpha}^{new})^2 + (V_{s_\beta}^{new})^2}} \qquad (2.37)$$

2.5.2 PI Controllers

Using the output of PLL, it is possible to convert grid voltages and line currents from a stationary reference frame to a synchronous reference frame, where all the quantities appeared as DC. Here, DC bus voltage controller will acts as outer loop controller and two current (I_{sd} and I_{sq}) controllers act as inner controller loops.

Real Power and Reactive Power Controller

In a FEC, real power control is possible by controlling the real part of current I_{sd} and reactive power control is done by controlling I_{sq}. The controller draws current from the grid based on the load requirement, while keeping the DC bus voltage at the reference. In the case of reactive power control, by varying I_{sq}^* variation

in reactive power flow from the grid is possible. As mentioned in section 2.5, the output of the real power controller and reactive power controller will be V^*_{ind} and V^*_{inq} respectively, which is the reference for modulating signal.

By referring to equation Eq. (2.25) and Eq. (2.26), rearranging the terms and removing feed forward terms from the equations,

$$V_{ind}(t) = -R_f I_{sd}(t) - L_f \frac{dI_{sd}(t)}{dt} \tag{2.38}$$

$$V_{inq}(t) = -R_f I_{sq}(t) - L_f \frac{dI_{sq}(t)}{dt} \tag{2.39}$$

Converting Eqs. (2.38) and (2.39) into frequency domain

$$V_{ind} = -R_f I_{sd} - sL_f I_{sd} \tag{2.40}$$

$$V_{inq} = -R_f I_{sq} - sL_f I_{sq} \tag{2.41}$$

Where I_{sd} and I_{sq} are the d-axis and q-axis component of current in the frequency domain respectively. While, V_{ind} and V_{inq} are the d-axis and q-axis inverter voltage in frequency domain respectively.

From the equations 2.40 and 2.41, the plant transfer functions for active and reactive power controllers are given as

$$\frac{I_{sd}}{V_{ind}} = \frac{-1}{R_f + sL_f} \tag{2.42}$$

$$\frac{I_{sq}}{V_{inq}} = \frac{-1}{R_f + sL_f} \tag{2.43}$$

From the above discussion, the derived controller block diagrams for active and reactive power controllers are shown in figures 2.8 and 2.9 respectively. Where, K_{pi} is the current controller gain and τ_{pi} is the current controller time constant.

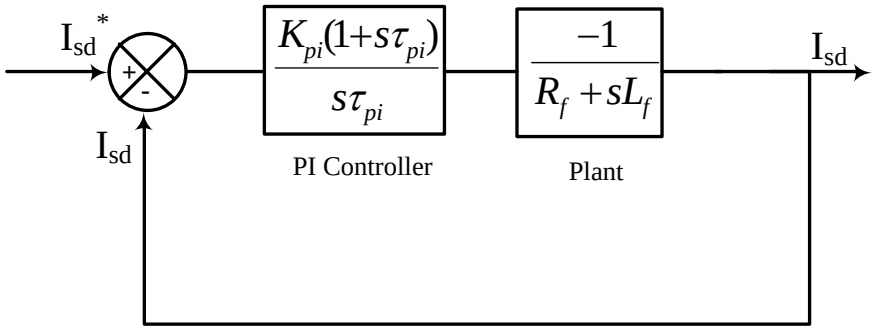


Fig. 2.8 Block diagram for I_{sd} controller

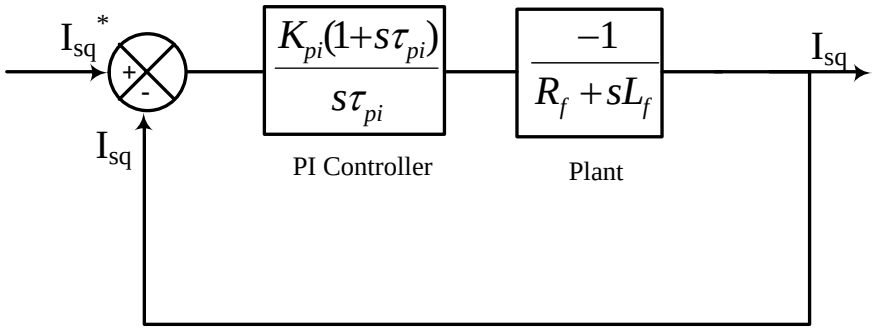


Fig. 2.9 Block diagram for I_{sq} controller

DC bus voltage controller

DC bus voltage controller is responsible for controlling the DC bus voltage at any prescribed load conditions. The plant for the DC voltage controller can be derived as follows.

The current through the DC load (DC current) is

$$I_{dc}(t) = C_{dc}\frac{dV_{dc}(t)}{dt} \tag{2.44}$$

Where, C_{dc} is the capacitance of DC bus capacitor, $I_{dc}(t)$ is the instantaneous DC current and $V_{dc}(t)$ is the instantaneous DC bus voltage. The above equation can

be converted into frequency domain as follows

$$I_{dc} = sC_{dc}V_{dc} \tag{2.45}$$

In the equation (2.45), I_{dc} represents the DC current in the frequency domain and V_{dc} represents the DC voltage in the frequency domain. The equation (2.45) can be rewritten as

$$V_{dc} = \frac{I_{dc}}{sC_{dc}} \tag{2.46}$$

But, here as explained above DC bus controller acts as outer loop and output of the controller will be the reference for inner real power controller. From the equation (2.46), it is able to obtain the DC bus controller Plant transfer function as $\frac{1}{sC_{dc}}$.

Here, the obtained transfer function is between DC bus voltage (V_{dc}) and DC current (I_{dc}). But in the case of a FEC controller, this controller acts as outer loop controller. So the DC voltage controller will generate the reference for I_{sd} controller. So there is a necessity of deriving transfer function of V_{dc} with respect to I_{sd}.

From the power balance equation following derivation is carried out.

$$\begin{aligned}
3\text{-}\phi power &= \sqrt{3} * V_{l-l} * I_{l-l} && (2.47)\\
&= V_{dc} * I_{dc} && (2.48)\\
&= \sqrt{3} * \sqrt{3} * V_{ph} * I_{ph} \\
&= 3 * \frac{V_{peak}}{\sqrt{2}} * \frac{I_{peak}}{\sqrt{2}} \\
&= \frac{3}{2} * V_{peak} * I_{peak} \\
&= \frac{3}{2}(\frac{2}{3}V_{sd})(\frac{2}{3}I_{sd}) && (2.49)
\end{aligned}$$

From Eq.(2.49), I_{dc} in terms of I_{sd} can be derived as

$$I_{dc} = \frac{2}{3} * \frac{V_{sd} I_{sd}}{V_{dc}} \tag{2.50}$$

$$I_{dc} = K * I_{sd} \tag{2.51}$$

Where $K = \frac{2}{3}\frac{V_{sd}}{V_{dc}}$, which is the constant relating between I_{dc} and I_{sd}. With the above information the controller block diagram for DC bus voltage controller is given in figure 2.10. Where, K_{dc} is the voltage controller gain and τ_{dc} is the voltage controller time constant.

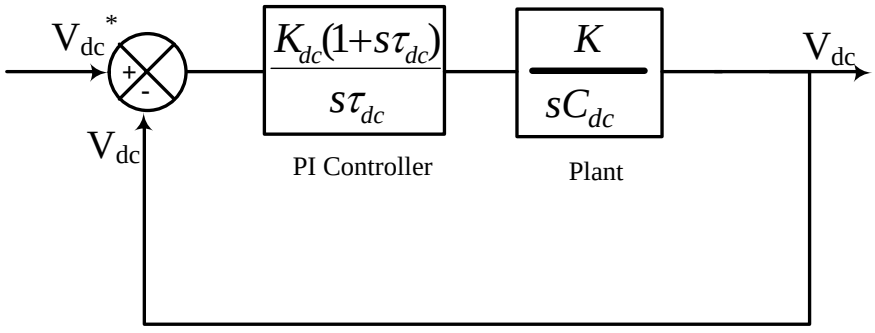


Fig. 2.10 Block diagram for V_{dc} controller

2.5.3 Feed-forward Terms and Inverter Gain

As observed in equations (2.25) and (2.26), there is cross coupling exists between d-axis and q-axis voltage. To ensure the decoupled control in d-q reference frame, feed forward terms e_{ffd} and e_{ffq} are subtracted from the outputs of I_{sd} and I_{sq} controllers respectively. The expressions for e_{ffd} and e_{ffq} are given below.

$$e_{ffd} = -V_{sd} - \omega L_f I_{sq} \tag{2.52}$$

$$e_{ffq} = \omega L_f I_{sd} \tag{2.53}$$

While designing the above mentioned controllers, inverter gain($G = \frac{V_{dc}}{2}$) has not been considered. The inverter gain can be incorporated after feed-forward terms are subtracted at the output of the controllers. To limit the starting inrush

current, the average pole voltage is required to be close to the supply voltage through out the start-up process. The average pole voltage of an inverter is determined by V_{sd}^* and V_{sq}^*. Even though in FEC, G is constant during steady state, it increases from the pre-charged value to the reference value during the starting. Hence, instead of holding G constant at its steady state value, it could be varied dynamically in order to reduce the starting current.

All the controllers with the relevant parameters is shown in figure 2.11

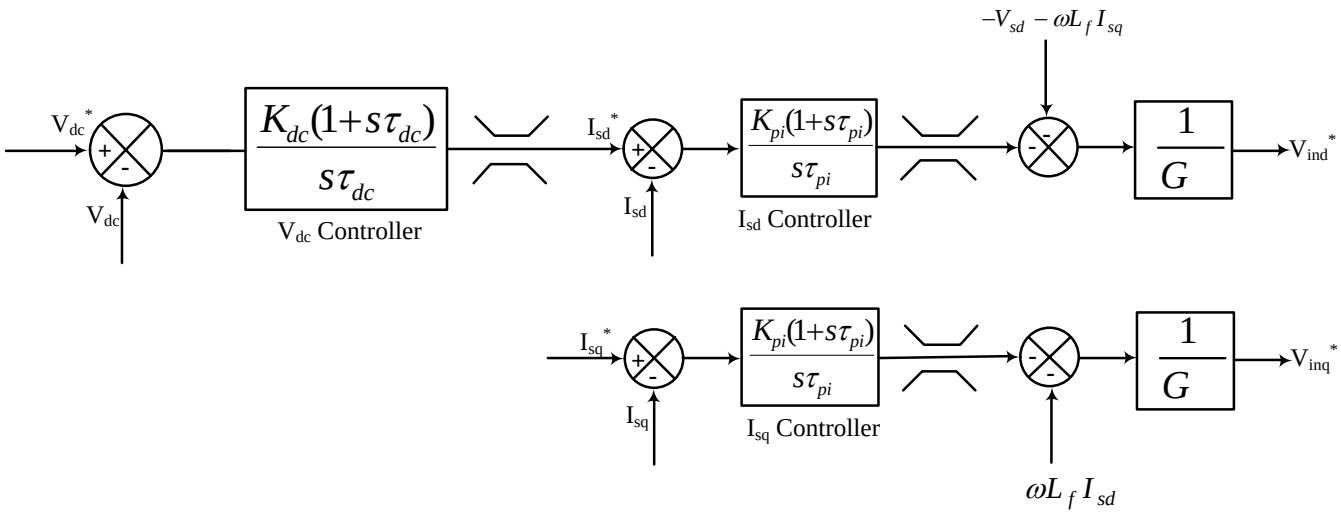


Fig. 2.11 Controller Structure

2.5.4 PWM generation

In order to get PWM pulses which goes to the IGBT gate, basically two modulation schemes have been used. They are sine-triangle PWM and space vector pulse width modulation (SVPWM). To obtain 3-phase balanced comparing signals, V_{ind}^* and V_{inq}^* are transformed into V_{ina}^*, V_{ina}^* and V_{inc}^* using $Cos\theta$ and $Sin\theta$

In the case of sinusoidal PWM (SPWM), the highest average phase voltage that can be applied is $\frac{V_{dc}}{2}$ and in the case of SVPWM is $\frac{V_{dc}}{\sqrt{2}}$. Hence in the case of SPWM, the comparing signals will go to the over modulation at the starting, but in the case of SVPWM this effect is not pronounced. In this project, the half of middle value of modulating waves at any instant is added to the original 3-phase modulating signals to generate reference signals equivalent to SVPWM [10]. The

generation of modulating signal equivalent to space vector from the sinusoidal reference signals is shown in figure 2.12.

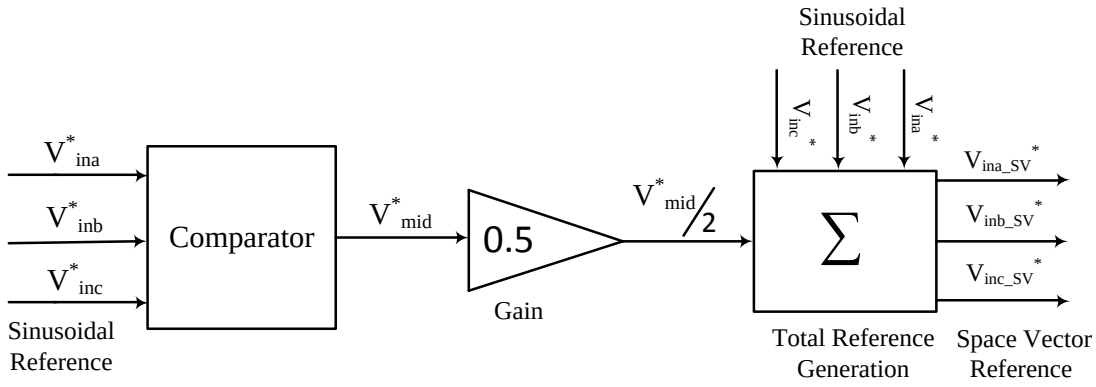


Fig. 2.12 Generation of SVPWM modulating signals from the SPWM modulating signals

The SVPWM adds zero sequence voltage to the three phase pole voltages. In 3-phase 4-wire system, because of this zero sequence voltage zero sequence current flows through the neutral wire. Also in back-to-back connected converters zero sequence current will circulate between the converters due to the presence of zero sequence voltage. Hence, SVPWM is not suitable for 3-phase 4-wire system and back-to-back converters.

2.6 Elimination of lower order harmonics from the line current of a 3-phase 3-wire FEC

In this section a simple control technique to eliminate the lower order harmonics present in the line current of 3-phase 3-wire FEC has been explained. Lower order harmonics are present in the grid current due to dead time in the IGBT module, low switching frequency and low filter inductance size. Moreover grid current controller only with the L-filter pollutes the line current with lower order harmonics and the grid current THD become worse in light load conditions. All the above reasons will allow a low impedance path for $5th$ harmonic current in the grid current which increases the line current THD [11].

The situation is not that much pronounced in the low voltage converters or high voltage/high currents converters. So there should be a different scheme apart from the conventional technique implemented in order to eliminate this lower order harmonics. The implemented technique has one loop parallel harmonic compensation structure, which is implemented parallel to the fundamental vector control loop. This type of implementation does not effect the dynamics of the original controller loop and also removes further hardware modifications.

2.6.1 Harmonic elimination technique

The basic control structure for nth harmonic elimination is shown in figure 2.13. The elimination control of each lower order harmonic is done in its own synchronous reference frame, where it behaves like a DC quantity. So PI controllers are sufficient to make each harmonic's d-axis component and q-axis component to zero.

The transformation from the stationary reference frame to the nth harmonic reference frame is only possible, if $Cosn\theta$ and $Sinn\theta$ are available. These quantities can be obtained from fundamental unit vectors $Cos\theta$ and $Sin\theta$ using trigonometric expansion formulas. Out put of the nth harmonic I_{sd_n} and I_{sq_n} controllers will be $V^*_{ind\_n}$ and $V^*_{inq\_n}$ respectively. $V^*_{ind\_n}$ and $V^*_{inq\_n}$ will then transform into stationary quantities $V^*_{ina\_n}$, $V^*_{inb\_n}$ and $V^*_{inc\_n}$. All these harmonic voltage references ($V^*_{ina\_n}$, $V^*_{inb\_n}$, $V^*_{inc\_n}$) are then added together with the fundamental reference voltages (V^*_{ina}, V^*_{inb}, V^*_{inc}) to generate the resultant voltage references ($V^*_{ina\_net}$, $V^*_{inb\_net}$, $V^*_{inc\_net}$) which are used to generate PWM pulses.

Each step by step procedure for elimination technique are explained in subsequent sections.

PLL for nth harmonic

As explained above, in order to transform the quantities from stationary reference frame to the nth harmonic rotating reference frame information about $Cosn\theta$ and $Sinn\theta$ are necessary. Information on $Cos\theta$ and $Sin\theta$ are obtained from funda-

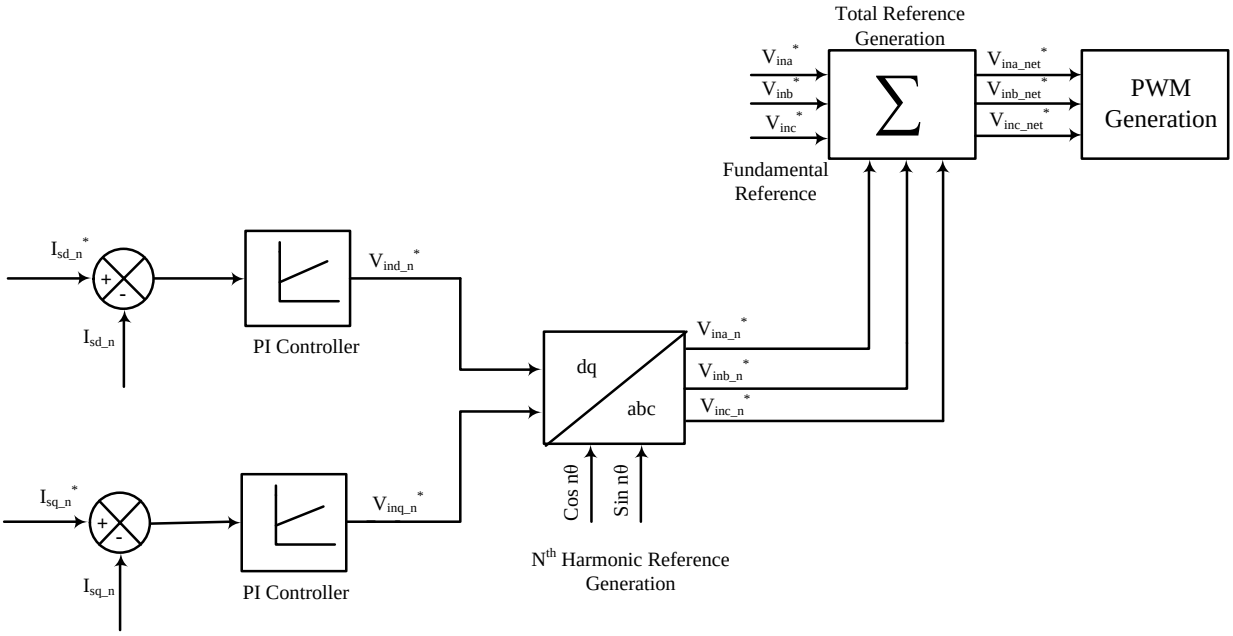


Fig. 2.13 Control structure for nth Harmonic elimination

mental PLL as explained in section 2.5.1. In this project $5th$ ($ie\ n = 5$) harmonic content is eliminated from the actual grid current. The derivation of $Cos5\theta$ and $Sin5\theta$ from the $Cos\theta$ and $Sin\theta$ are explained below.

$$\begin{aligned} Cos2\theta &= 2Cos^2\theta - 1 \\ Sin2\theta &= 2Sin\theta Cos\theta \\ Cos3\theta &= Cos2\theta Cos\theta - Sin2\theta Sin\theta \\ Sin3\theta &= Sin2\theta Cos\theta + Cos2\theta Sin\theta \\ Cos5\theta &= Cos3\theta Cos2\theta - Sin3\theta Sin2\theta \qquad (2.54) \\ Sin5\theta &= Sin3\theta Cos2\theta + Cos3\theta Sin2\theta \qquad (2.55) \end{aligned}$$

Harmonic Extraction Process

Since harmonic elimination controllers are implemented in nth harmonic reference frame, there is a need for harmonic current/voltage extraction from the actual current/voltage. This process of extraction is explained in figure 2.14.

The algorithm basically consists of two cascaded stages. In the first stage, ac-

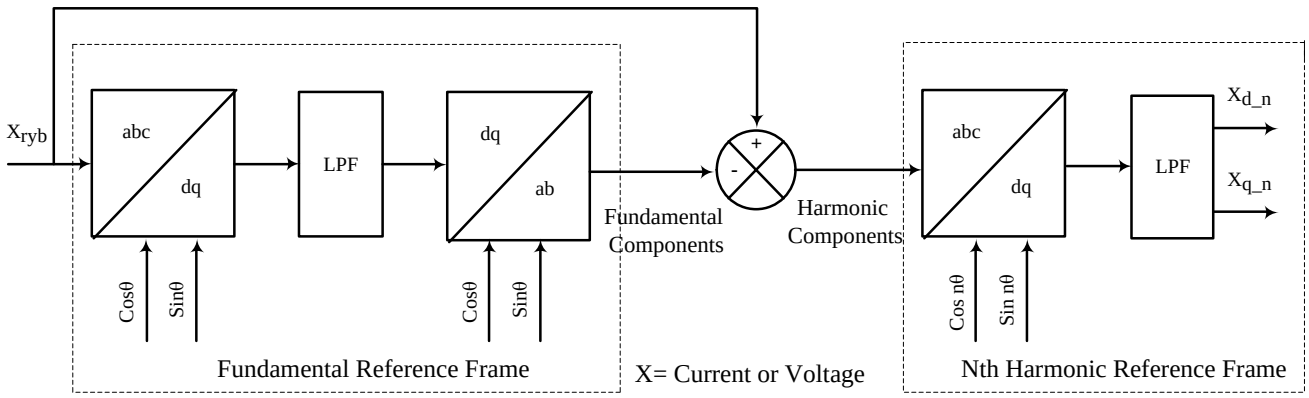


Fig. 2.14 Harmonic Extraction Algorithm

tual signal is transformed into fundamental reference frame using low pass filters. From the fundamental reference frame which will again convert back to stationary reference frame, but in this case the stationary signal only contains the fundamental component. Then this fundamental component is subtracted from the actual signal to get the only the harmonic components. Second stage involves the required *nth* harmonic extraction in the *nth* harmonic *d-q* reference frame using *nth* harmonic PLL and low pass filters. This algorithm ensures that the fundamental ripples are eliminated from the harmonic reference frame.

2.7 Three-phase Four-wire FEC

3-phase 4-wire FEC is necessary in the case of domestic applications and single phase load. For this supply neutral should be connected to converter which ensures earth fault protection.[12; 13]

The neutral connection mainly done in two ways. One is supply neutral wire could be connected to the mid-point of the DC bus and another option is to have an additional leg in the converter and to connect the supply neutral to the mid-point of this additional leg. [14; 15]. In this project supply neutral has been connected to the mid-point of the DC bus as shown in figure 2.15

So far controlling and modeling concerned, the basic structure of controller and modeling will remain same as in 3-phase 3-wire FEC. Additional modeling

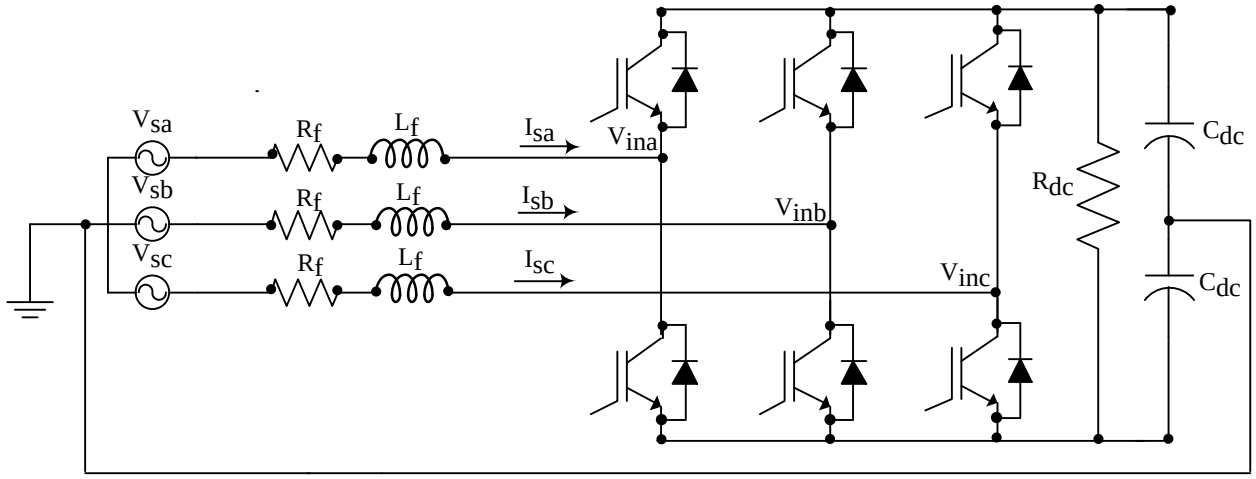


Fig. 2.15 3-phase 4-wire FEC

and control techniques should be implemented in 3-phase 4-wire FEC compared to 3-phase 3-wire FEC in order to take care of common mode current, which will flow through the neutral wire. The detailed modeling and controller design for 3-phase 4-wire FEC are explained in subsequent sections.

2.7.1 Modeling and control of 3-phase 4-wire FEC

The main challenge in modeling of 3-phase 4-wire FEC is taking care of common mode (zero sequence) current, which flows through the neutral wire. The converter in the figure 2.15 can be regarded as three independent single-phase half-bridge FEC (see figure 2.16(a)) sharing common DC bus [16].

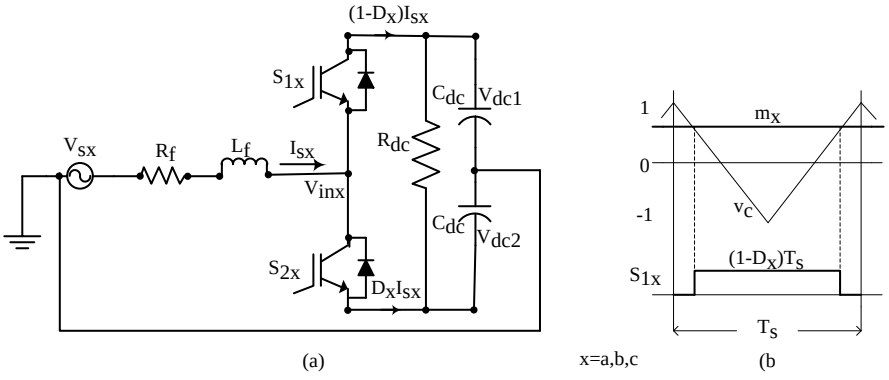


Fig. 2.16 xth phase half bridge FEC

In three phase four wire system instantaneous line current consists of a differential mode current and common mode current. In this case the xth phase current can be written as given below.

$$i_x = i_{xd} + i_{CM} \tag{2.56}$$

$$\text{where } i_{CM} = \frac{i_a + i_b + i_c}{3} \tag{2.57}$$

Where i_x is the instantaneous current at xth phase, i_{CM} is the common mode current and i_{xd} is the differential mode current.
The common mode current i_{CM} is same in three phases. The inductors offer inductance L_f for both common mode and differential mode currents, because there is no mutual coupling between the inductors.

Reasons for common mode current

From the circuit 2.16(a), it is clear that common mode current can flow through the neutral wire, if there is a mismatch in the voltages of two DC capacitors ($V_{dc1} \neq V_{dc2}$) at the steady state. This mismatch in voltage arises due to various reasons such as[17; 18]

- Small offsets in the input current measurement
- Offsets in the reference current and measured input voltage
- Small mismatch in the two DC capacitors C_{dc}
- Shunt resistance associated with C_{dc}
- Difference in initial voltage of two DC capacitors

Elimination of common mode current

In this project the elimination of zero sequence (common mode) component has been implemented with a PI controller. Since PI controllers can eliminate lower order harmonics from the system, it is sufficient for the elimination of zero sequence component. The additional neutral current controller along with the basic controller is shown in figure 2.17.

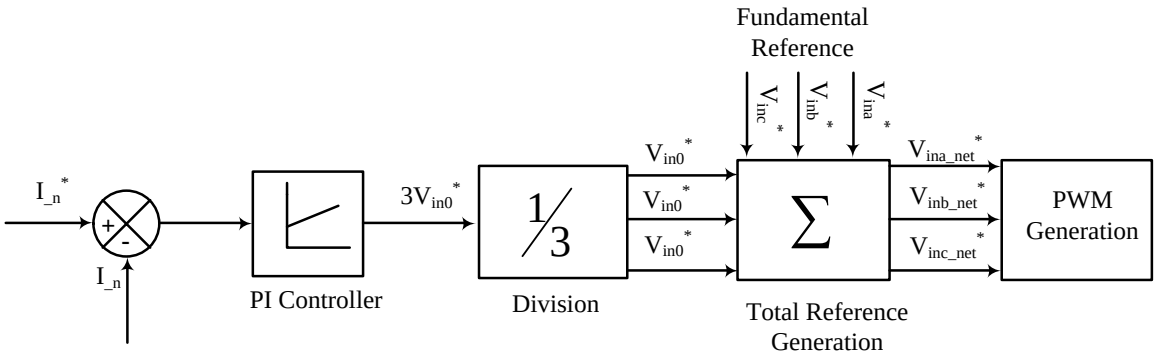


Fig. 2.17 Controller block diagram for 3-ϕ 4-wire FEC

The controller additionally making neutral current to zero using a PI controller along with the other basic controllers of the 3-phase 3-wire FEC. The reference for the PI controller is zero and the feed back should be sensed from neutral current. The output of the PI controller will be divided by three and then added to the each 3-phase reference, which generated using basic controller loops. The above controller make sure that there is no voltage difference between the two DC capacitors and thereby neutral current is zero.

The plant for the PI controller can be derived with the help of figure 2.18(a) and 2.18(b). Figure 2.18(a) shows the zero-axis electrical circuit of 3-phase 4-wire FEC, where V_{s0} is the zero sequence component present in the grid voltage, I_{s0} is the zero sequence component in the line current, $3I_{s0} = I_N$ is the current flows through neutral wire and $(V_{dc1} - V_{dc2})$ is the difference between the voltage of two DC capacitors C_{dc}.

Figure 2.18(b) shows the simplified circuit of the zero-axis circuit, where $R_f/3 = R_{eq}$ is the effective resistance in the zero-axis path and $L_f/3 = L_{eq}$ is the effective inductance in the zero-axis path. From Figure 2.18(b), the transfer function between common mode voltage V_{CM} and neutral current I_N can be derived as shown below.

$$\frac{V_{CM}}{I_N} = \frac{1}{R_{eq} + sL_{eq}} \tag{2.58}$$

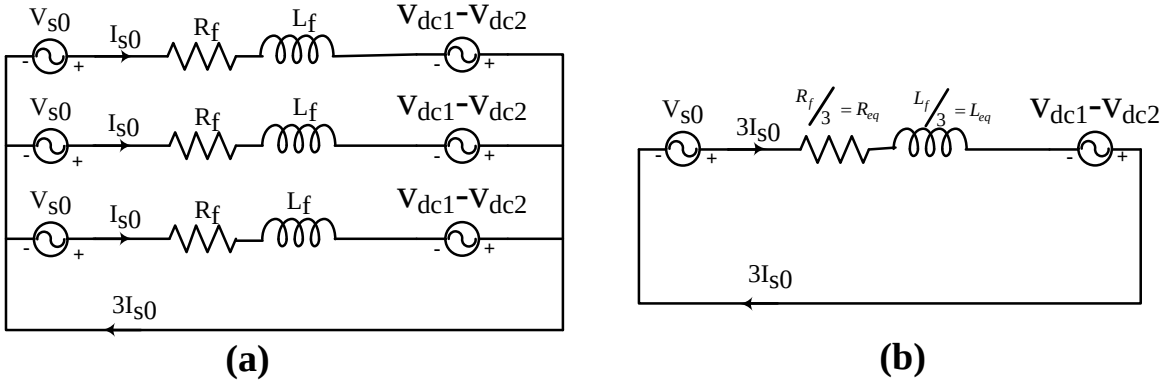


Fig. 2.18 (a)Zero-axis circuit of 3-phase 4-wire FEC(b)Equivalent zero-axis circuit of 3-ϕ 4-wire

With the above discussion the derived controller block diagram for neutral current controller is given in figure 2.19, where K_{pn} is the neutral current controller gain and τ_{pn} is the neutral current controller time constant.

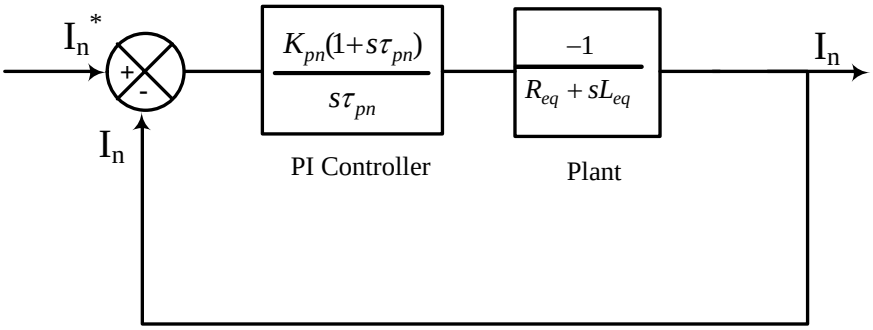


Fig. 2.19 (a)Neutral current controller for a 3-phase 4-wire FEC

2.7.2 Switching frequency distortions in line and neutral current

The switching frequency distortions in the line and neutral currents of a four wire FEC causes EMI, power loss and device stress [19; 20]. So over all distortions in the line currents and neutral currents must be reduced. The distortions in a two-level, 3-phase 4-wire FEC with sine-triangle PWM is shown in figure 2.20(a).

The instantaneous pole voltage v_{inx} shown in figure 2.20(a) can be divided into average value V_{inx} and a switching frequency ripple $\tilde{v}_{inx}$. The ripple voltage $\tilde{v}_{inx}$ causes ripple current $\tilde{i}_x$ in xth phase as shown in figure 2.20(a).

The ripple current $\tilde{i}_x$ at any phase x is zero both at the start and the end of switching cycle T_s. Figure 2.20(a) qualitatively shows the variations of line and neutral current ripples over the switching cycle T_s. From the figure 2.20(a), it can be interpreted that the distortions in the neutral current $\tilde{i}_N$ is much higher than line current ripples ($\tilde{i}_a$, $\tilde{i}_b$, $\tilde{i}_c$) as $\tilde{i}_N = -(\tilde{i}_a + \tilde{i}_b + \tilde{i}_c)$.

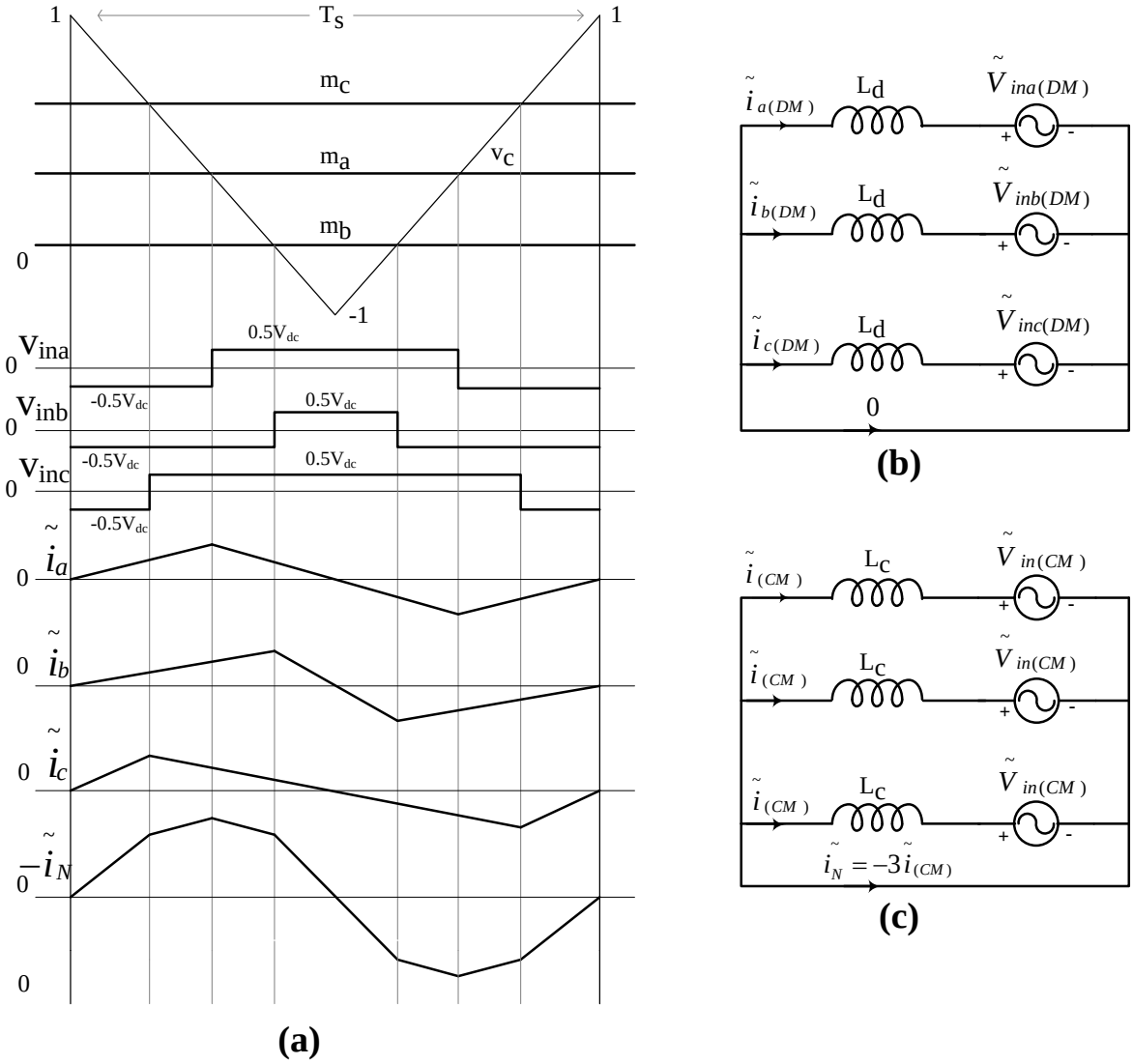


Fig. 2.20 (a)Line and neutral current distortions with SPWM(b)Differential mode ripple equivalent circuit(c)Common mode ripple equivalent circuit

Analysis of line and neutral current distortions

As discussed above difference in DC capacitors voltage causes common mode current through neutral. Besides this unbalance in the pole voltage causes switching frequency current in the neutral wire. The unbalance in the pole voltage , that is common mode component in the pole voltage is given in Eq.(2.59). Therefore switching ripple in xth phase can be written as a combination of differential mode switching ripple ($\tilde{V}_{inx(DM)}$) and common mode switching ripple ($\tilde{V}_{in(CM)}$)as given in Eq.(2.60).

$$\tilde{V}_{in(CM)} = \frac{\tilde{V}_{ina} + \tilde{V}_{inb} + \tilde{V}_{inc}}{3} \tag{2.59}$$

$$\tilde{V}_{inx} = \tilde{V}_{inx(DM)} + \tilde{V}_{in(CM)} \tag{2.60}$$

The ripple voltages $\tilde{V}_{inx(DM)}$ and $\tilde{V}_{in(CM)}$ causes ripple currents $\tilde{i}_{j(DM)}$ and $\tilde{i}_{(CM)}$ in the xth phase line. This is shown in figure 2.20(b) and 2.20(c) respectively. Where $\tilde{i}_{x(DM)}$ is the differential mode current in xth phase and $\tilde{i}_{(CM)}$ is the common mode current in the system. The expression for common mode current $\tilde{i}_{(CM)}$ is given in Eq.(2.61). Similar to pole voltage, ripple current in the xth phase can be written as a combination of differential mode switching ripple current ($\tilde{i}_{x(DM)}$) and common mode switching ripple current ($\tilde{i}_{(CM)}$) as given in Eq.(2.62). This common mode ripple current causes common mode switching distortion in the neutral wire as shown Eq.(2.63).

$$\tilde{i}_{(CM)} = \frac{\tilde{i}_a + \tilde{i}_b + \tilde{i}_c}{3} \tag{2.61}$$

$$\tilde{i}_x = \tilde{i}_{x(DM)} + \tilde{i}_{(CM)} \tag{2.62}$$

$$\tilde{i}_N = -3\tilde{i}_{(CM)} \tag{2.63}$$

Elimination of neutral current distortions

From the above discussion it is clear that neutral current distortions is happening because of unbalance in the pole voltage ripple ($\tilde{V}_{in(CM)}$). The ripple voltage $\tilde{V}_{inx(DM)}$ and ($\tilde{V}_{in(CM)}$) depend on a number of factors such as system frequency, switching frequency and PWM scheme. As basic controller for the 3-phase 4-wire

FEC is same as that of 3-phase 3-wire FEC, nothing can be done to eliminate $\tilde{V}_{in(CM)}$. So the only possibility is to reduce the neutral current distortions.

From the figure 2.20(c), it is clear that $\tilde{i}_{(CM)}$ not only depend on magnitude of the $\tilde{V}_{inv(CM)}$ but also the impedance offered by three common mode inductance. In the case of three single phase inductors inductance offered by L_f will be same for both common mode current and differential mode current, that is $L_c = L_d = L_f$.

Also from figure 2.20(b), it is clear that differential mode current in xth phase $\tilde{i}_{x(DM)}$, does not flows through the neutral wire. Thus the figure 2.20(b) represents the current in a 3-phase 3-wire FEC and figure 2.20(c) represents the additional common mode equivalent circuit in the case of a 3-phase 4-wire system. So the basic controller for both 3-phase 3-wire FEC and 3-phase 4-wire FEC will be same as long as there is no changes in the equivalent circuit shown in figure 2.20(b). Therefore an additional change in the equivalent circuit shown in figure 2.20(c) does not effect the main controller part.

So an additional modifications should be done in the figure 2.20(c) in order to reduce the common mode current distortions. One such possibility is to have an additional inductance (L_{cn}) in the neutral path as shown in figure 2.21, which will offer additional impedance for the common mode switching current and thereby reducing the switching distortions from the neutral wire. Thus without affecting the main controller reduction in neutral current distortions is possible.

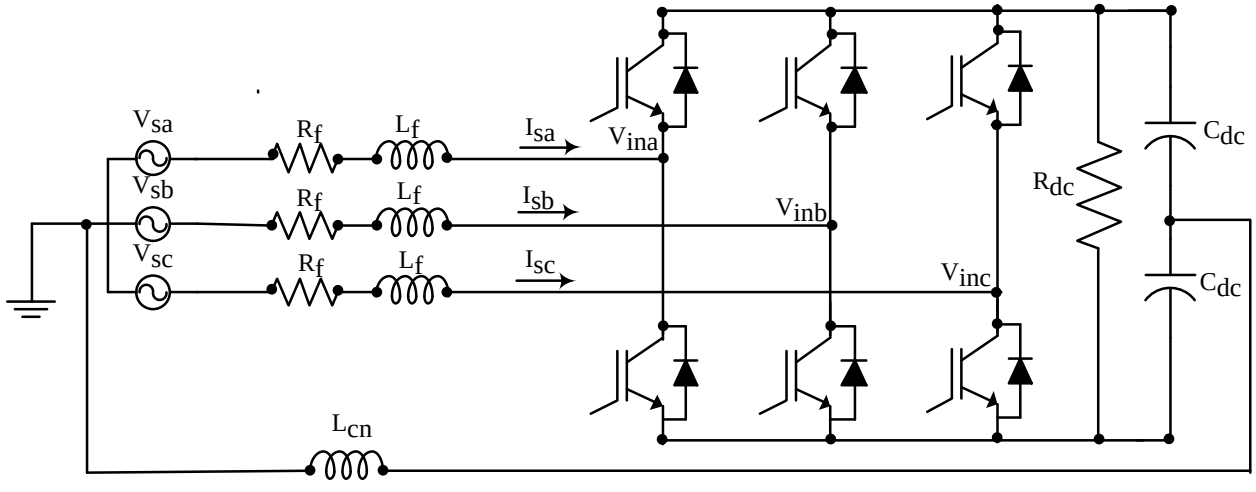


Fig. 2.21 3-phase 4-wire FEC with additional inductance (L_{cn}) in the neutral wire

2.8 Conclusion

This chapter discussed the concept of vector control and modeled FEC in synchronous reference frame. PLL has been used in the modeling and controller in order to synchronize with the grid.The complete derivation and block diagram of all the controllers are discussed. The difference in control strategy of 3-phase 3-wire FEC and 3-phase 4-wire FEC has been taken care off. Discussed the technique for elimination of lower order harmonics from the line current of a FEC with relevant equations.

CHAPTER 3

HARDWARE ORGANISATION AND CONTROL IMPLEMENTATION OF FEC

3.1 Introduction

In this chapter, the features about TMS320F28335, 32-bit floating point Digital Signal Controller from Texas Instruments and the brief overview about the hardware organization that help in implementing vector control of FEC will be explained. The additional circuitry developed for proper interfacing and protection will also be discussed. The chapter also explains about the controller design and implementation for the vector control of FEC. The design is done following a per unit system with defined base quantities.

3.2 Brief Overview of the TMS320F28335

TMS320F28335 has a 32-bit DSP core with modified Harvard architecture, and also includes a single precision IEEE754 floating point unit. It has both C/C++ engine, enabling users to develop to write system control software in a high level language. The memory bus architecture of TMS320F28335 contains a program read bus, a data read bus and a data write bus. This device has real-time JTAG, which supports real-time debugging along with the Code Composer Studio(CCS) from TI. The memory space contains independent sections of flash-memory, single access RAM (SRAM), onetime programmable memory (OTP) and boot ROM. The Boot ROM is factory-programmed memory space with boot-loading software. An XINTF zone is a region in the TMS320F28335 memory map that can be directly connected to the external interface. The device has an on-chip oscillator with a PLL for clock scaling. It also has 88 GPIO pins multiplexed with a variety of other peripherals like PWM [21] and ADC [22]. The controller also has standard

communications interface like I^2C and CAN. 96 external interrupts are supported [23], which are governed by the Peripheral Interrupt Expansion (PIE) unit.

In this project, a generic control platform based on TMS320F28335 Digital Signal Controller (DSC) which is developed in the lab has been used for the vector control of FEC

3.3 Current and Voltage Sensing

The feedbacks required for vector control of FEC are the phase voltages, line currents and the DC bus voltage. Current and voltage sensor cards based on Hall effect sensors are used to obtain these signals. Apart from providing feedbacks, these signals are also used for providing protection to the inverter against possible overcurrent and overvoltages. In this project, the LA100P sensor has been used for current sensing and the LV25P sensor for sensing the DC bus voltage. The burden resistors are selected so as to get an output voltage of 5V, corresponding to 100A for the current sensor and 1000V for the voltage sensor.

3.4 Three Phase Inverter Module

A three phase 2-level Voltage Source Inverter(VSI) from Semikron is used in this project for obtaining DC bus voltage from the grid source [24]. The inverter uses 1200V, 100A IGBT modules as the power switches with each module forming one leg of the inverter. The inverter has a front end diode bridge rectifier for energising the DC bus from an input three phase supply. A pre-charging circuit consisting of resistors in parallel with relays, is connected in series with each line to prevent large inrush currents into the capacitor during energising. The rectifier and the modules are mounted on the heat sink and connected to the DC bus capacitor by conducting sheets. Three Gate driver cards are mounted on the module for giving proper isolation and gate drive for the IGBT gate terminals.

Apart from the basic inverter module, a Protection and delay card has been used for proper interfacing and protection. This will be discussed in the following

subsection.

3.4.1 Protection and Delay Card

The function of the Protection and Delay(PD) card is to provide protection against faults and also to generate complementary signals with proper rising edge delay. The three top switch PWM signals from the DSP are level shifted and fed to the PD card. It generates the complementary signals with proper delay using RC circuits and logic gates. These are then given to the gate driver inputs of the inverter module. The outputs of the Hall sensors are also connected to the PD card where they are buffered and fed to high speed opamp comparators. The protection references to the comparators can be set using potentiometers. The output of the comparators indicate fault conditions and are fed to an RS latch using a wired AND logic. The PD card has provision to provide protection for six sensed currents and two DC bus voltages. Also the circuitry for generating delayed complementary signals can be completely disabled by setting the jumpers provided. In this case, the delay has to be generated in software using the deadband module and all the six PWMs can then be directly fed from the DSP. LEDs provided on board are used for fault annunciation. The PD card also has provisions to transmit and receive the PWMs in either differential or single ended fashion by setting appropriate jumpers. It also controls the relays of the pre-charging circuit thereby protecting the capacitors from large inrush currents.

3.5 Three Phase Line Side Filter and Common Mode Filter

The line side filters are used for the smoothing the line current from the switching ripples. In this project, three single-phase inductors are used as the line side filter. The ratings of single phase inductor are given in Table 3.1.

In the case of a 3-phase 4-wire FEC, a common mode filter is necessary in addition to the 3-phase line side filter, in order to reduce the switching frequency

Table 3.1 Ratings of a single phase inductor

Parameter	**Value**
Value	2.5mH
Maximum peak voltage	800V
Maximum peak current	35A
RMS current	15A
Fundamental current frequency	50Hz
Switching current frequency	5kHz

distortions in the line and neutral current. In this project an additional single phase inductor is used as the common mode filter, the ratings of common inductor are given in Table 3.2.

Table 3.2 Ratings of common mode inductor

Parameter	**Value**
Value	4mH
Maximum peak voltage	440V
Maximum peak current	10A
RMS current	7A
Fundamental current frequency	50Hz
Switching current frequency	5kHz

3.6 Soft Start-up for FEC

The various theoretical methods for the soft start-up of a FEC are discussed in chapter 2, such as different PWM scheme and dynamic variation of inverter gain. In this section the actions that needs to be taken care during the hardware implementation of both 3-phase 3-wire and 3-phase 4-wire FEC in order to ensure a soft start-up are discussed.

One of the critical precautions of a FEC is that the grid should not be short circuited at any time of the operation, even during the start-up also. All the procedures for soft start-up is explained after pre-charging the DC bus and before the controller starts. The procedure for pre-charging the DC bus with three phase diode bridge rectifier is explained before.
There is a modification in pre-charging of 3-phase 4-wire FEC from the 3-phase 3-wire FEC in order to avoid high starting current during the starting of pre-

charging. In the case of 3-phase 4-wire FEC, the neutral wire from the supply should not be connected to the mid point of the DC bus before pre-charging. That is there should a manual switch between the neutral point of the supply and mid point of the DC bus, and the switch should be closed only after DC bus get pre-charged.

The sequence for the soft start-up after pre-charging are explained below.

Step 1:

One of the precaution is that never use hardware delay for the complementary signals, which is generated by PD card and use only the software delay generated by deadband module of the DSP board. This is because in the hardware delay independent control of six PWM signals is not possible, that is top switch and bottom switch in a leg of the inverter can't be ON or OFF simultaneously, where this will be always complementary to each other. But in the case of software delay, top switch and bottom switch in a leg can be OFF simultaneously using the Trip zone module of the DSP.

So in the case of hardware delay, at the starting of FEC at least two among three of the top switches in the inverter will be ON even before the controllers generating the appropriate PWM pulses, which will cause short circuit in the grid at the starting and thereby high staring current. Since in the software delay, all the six switches can be kept OFF till the controllers generating the appropriate PWM pulses, so there is no short circuit in the grid at the starting thereby reduction in starting current.

Hence software delay should be used instead of hardware delay in order to avoid short circuit in the grid and thereby reduction in the starting current at the starting of a FEC.

Step 2:

Since the implemented PLL has two low pass filters, there is certain dynamics and settling time associated with the output of PLL. So the PLL output should be settled before the controller starts, in order to get the correct unit vectors from the starting itself. Because unit vectors without the appropriate values can cause high starting current.

So the DSP software code for the PLL must be settled before the controller starts. This can be done in open loop as the PLL does not require any feed back infor-

mation from the controller, it will take only the grid voltages as its input and it will output the position information of the grid voltage.

Step 3:

Once the PLL output is settled, then the controller can start. In this project, the starting of controller is done through a feed back signal from the PD card, where feed back signal is taken from the output of ON/OFF switch of the PD card. This feedback signal will go to one of the GPIO of the DSP board, and if the ON/OF switch is ON controller will start and if it is OFF the controller loop won't run. But in this case there could be problem with noise, which is picked up from the path between PD card and DSP board. Because of this noise, it can happen that even if the ON/OFF switch is not ON, the noise can make the ON/OFF switch output voltage equal to the voltage when its in ON position and vice verse. So there should be an input qualifier at the GPIO of the DSP, to determine whether it is a noise or actual signal in order to make sure that the controller starts only based on the ON/OFF switch position.

3.7 Hardware Setup

The vector control for the FEC are implemented on 10KVA laboratory type. Some of the photographs of the FEC setup and the various additional circuitry built for interfacing will be presented in this section.

Figure 3.1 shows the over all view of the FEC hardware set-up, it contains Semikron IGBT module, line side inductors, pre-charge circuit, PD card, digital oscilloscope, voltage and current sensors and the DC power supply for the PD card and sensors.

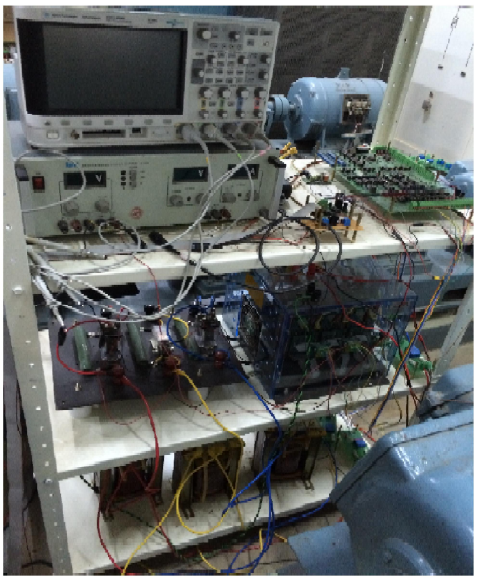


Fig. 3.1 Inverter and control hardware

Figure 3.2 shows the DSP board, which is used for the digital controller implementation of FEC. The DSP board has TMS320F28335 based DSC, an analog interface, Digital to Analog Converter(DAC), JTAG debugger and communication interfaces.

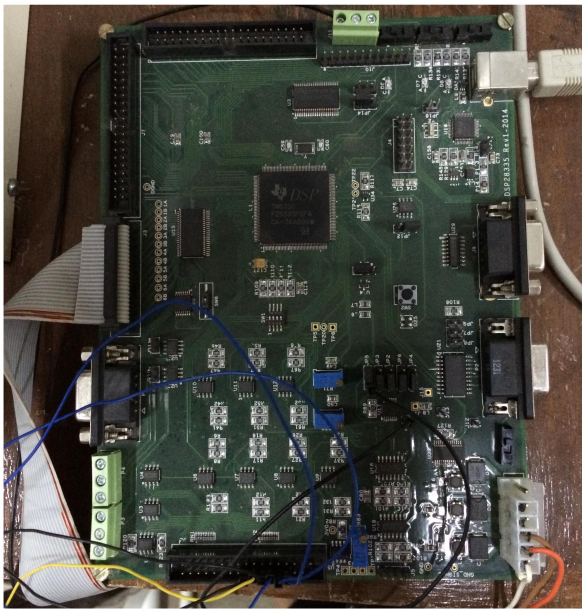


Fig. 3.2 The DSP board which is developed in the lab

The picture shown in left of the figure 3.3 is the pre-charge circuit, which used to charge the DC bus without high inrush current. The picture shown in right of the figure 3.3 is the PD card, which provide protection against faults and also to generate complementary signals with deadband.

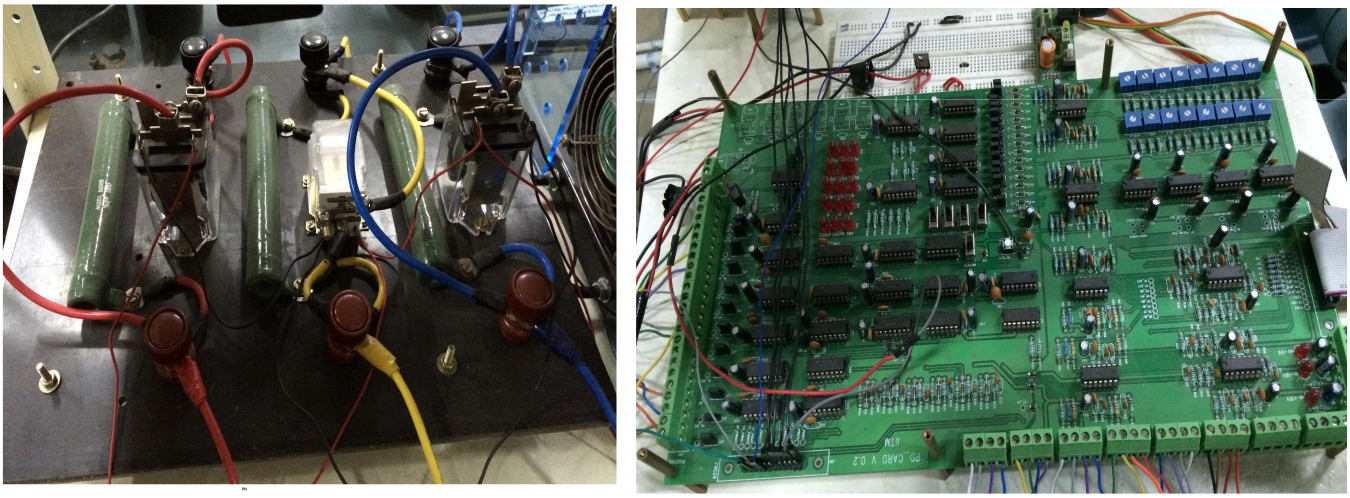


Fig. 3.3 Pre-charge Circuit (left) and PD card(right)

The picture shown in left of the figure 3.4 is the inductors used as the line side filters and picture shown in right of the figure 3.4 is the inductor used as the common mode filter.

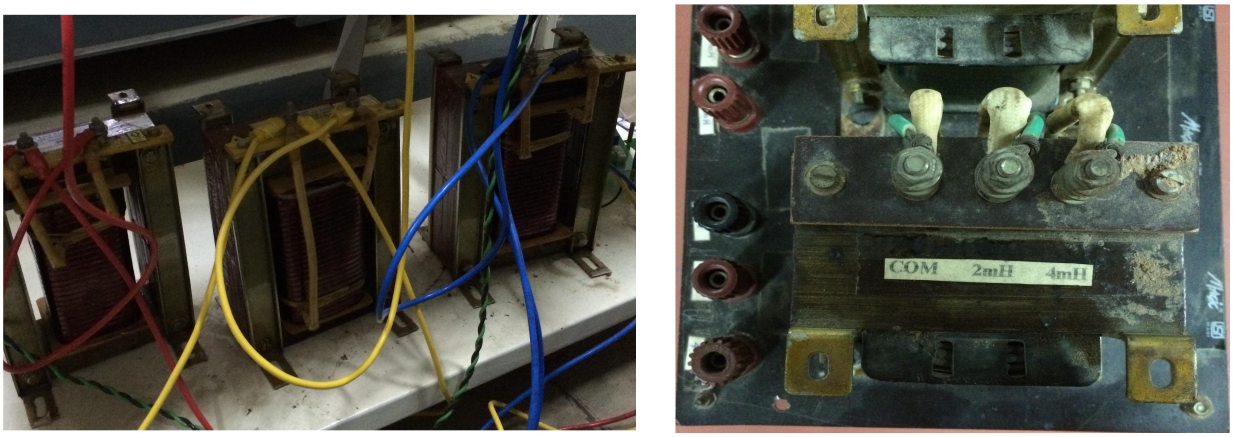


Fig. 3.4 Line side inductors (left) and Common mode inductor(right)

3.8 The Per Unit System

In this work, a Per Unit(pu) system has been followed for implementing the control algorithms. This makes the digital implementation easy as all quantities are

brought to the same range of values in pu. Thus the controller can use a common number format for performing the computations. For per unitisation of quantities, base values are required which are chosen as per convenience. Table 3.3 gives the base values chosen for the different quantities.

Table 3.3 PU base quantities

Voltage(V_b)	800 V
Current(I_b)	12.5A
Frequency(f_b)	50Hz

3.9 Design of Controllers

The vector control of 3-phase 3-wire FEC uses PI controller for controlling V_{dc}, I_{sd} and I_{sq}. In addition to the basic controllers, elimination of $5th$ harmonic component from the line current of FEC requires two additional controllers, they are I_{sd_5} and I_{sq_5}.
In the case of 3-phase 4-wire FEC, there should be an additional neutral current (I_n) controller apart from the basic controllers of 3-phase 3-wire FEC.

The PI controllers used in vector control are provided with output limiters and integrator antiwindup. Output limiters ensure that the currents and voltages of the FEC are within rated limits at all times. The integrator antiwindup disables the integral action when the output of the controller reaches its limit value. This helps in making the controller faster.
The notations that are used in each controller design are given below

Table 3.4 PI controller notations

K_p	Proportional gain
k_i	Integral gain
U_{max}	Max. output limit
U_{min}	Min. output limit

The controller parameters obtained for the 10 kVA 3-phase 3-wire and 3-phase 4-wire FEC are given in Table. designvalues.

Table 3.5 Controller parameters

Controller	$K_p(pu)$	$K_i(pu)$	$U_{max}(pu)$	$U_{min}(pu)$
V_{dc}	19.52	0.00125	0.6	-0.6
I_{sd}	0.1221	$4*10^{-5}$	1.225	-1.225
I_{sq}	0.1221	$4*10^{-5}$	0.175	-0.175
I_{sd_5}	0.0122	$4*10^{-5}$	0.1225	-0.1225
I_{sq_5}	0.0122	$4*10^{-5}$	0.0175	-0.0175
I_n	0.1221	$4*10^{-5}$	0.525	-0.525

3.10 Conclusion

This chapter outlined the features of the TMS320F28335 that are used in implementing the vector control algorithms. The additional hardware used for sensing the voltages and currents and interfacing between the various circuits are also discussed. The chapter also presented the controller design values for the vector control of FEC using per unitisation technique.

CHAPTER 4

RESULTS AND INFERENCES

4.1 Introduction

In this chapter the simulation and experimental results pertaining to this project will be discussed. The experimental and simulation results corresponding to PLL, 3-phase 3-wire FEC and 3-phase 4-wire FEC are included in this chapter.

4.2 Simulation Results

4.2.1 PLL Results

The three phase grid voltages are shown in figure 4.1, where a-phase voltage is leading b-phase voltage and c-phase voltage is leading a-phase voltage.

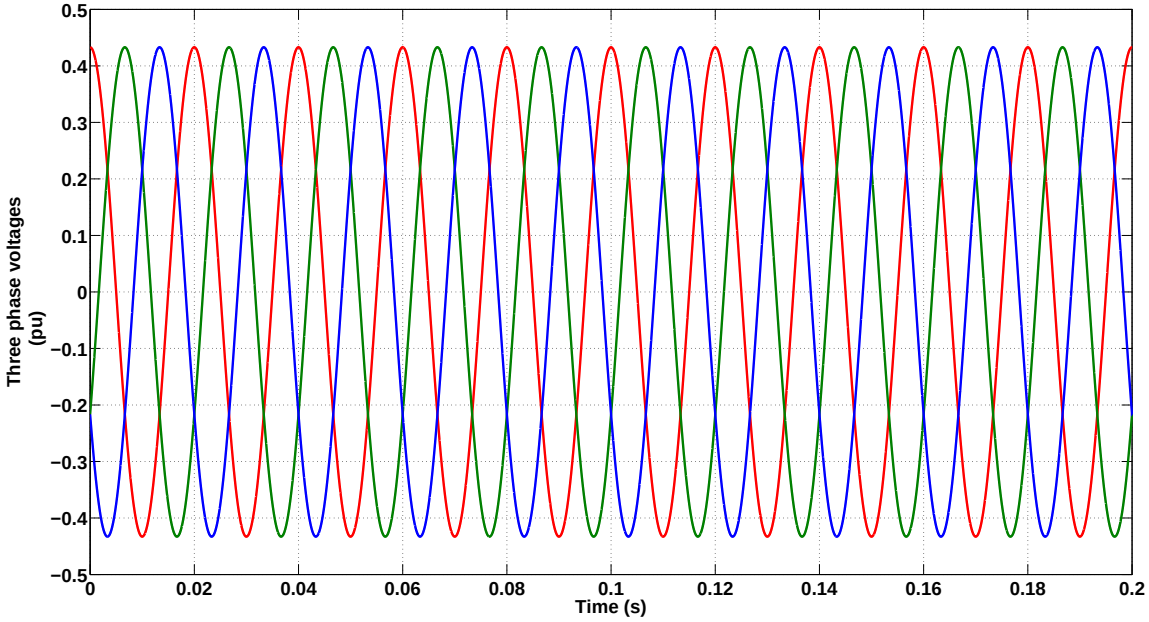


Fig. 4.1 *Simulation result*: a(red), b(green) and c(blue) phase voltages*(Scale: X-axis: 0.02 s/div, Y-axis: 0.2 pu/div or 160 V/div)*

As explained before, these three phase voltages V_{sa}, V_{sb}, V_{sc} are converted into $V_{s\alpha}$ and $V_{s\beta}$, which are given in figure 4.2.

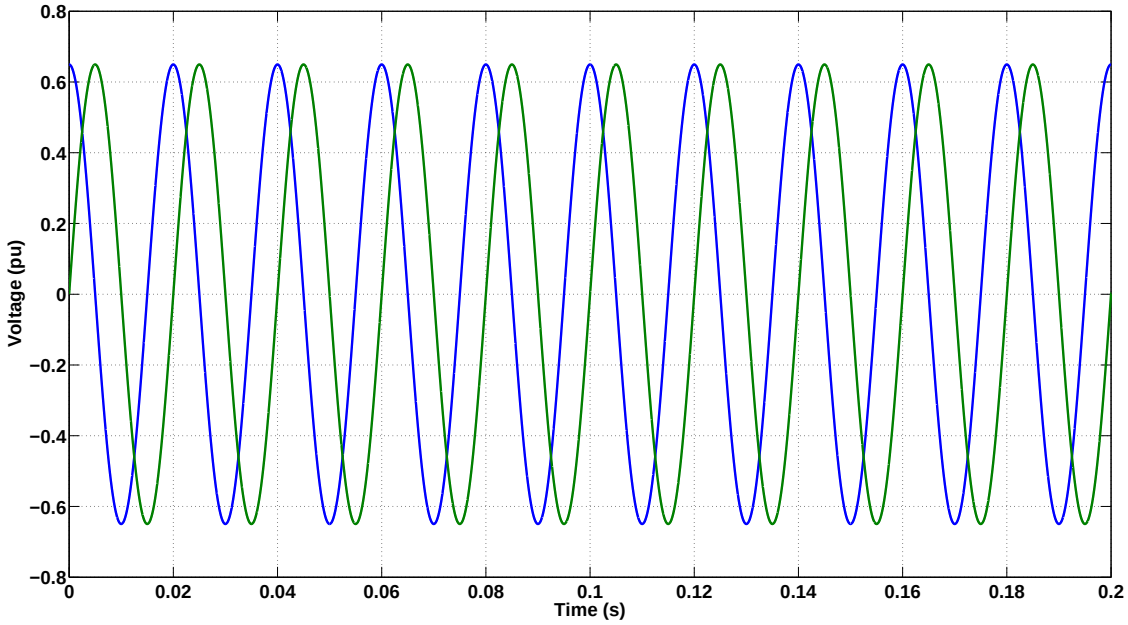


Fig. 4.2 *Simulation result*: $V_{s\alpha}$(blue) and $V_{s\beta}$(green)*(Scale: X-axis: 0.02 s/div, Y-axis: 0.2 pu/div) or 160 V/div*

The outputs of first low pass filter and second low pass filter with input as $V_{s\alpha}$ and $V_{s\beta}$ are given in figure 4.3 and 4.4 respectively. Here, the output magnitude is decreasing by $\sqrt{2}$ and a phase shift of 45° from the input as it passing through each low pass filters, also there is a finite settling time associated with each low pass filter as seen from figures 4.3 and 4.4.

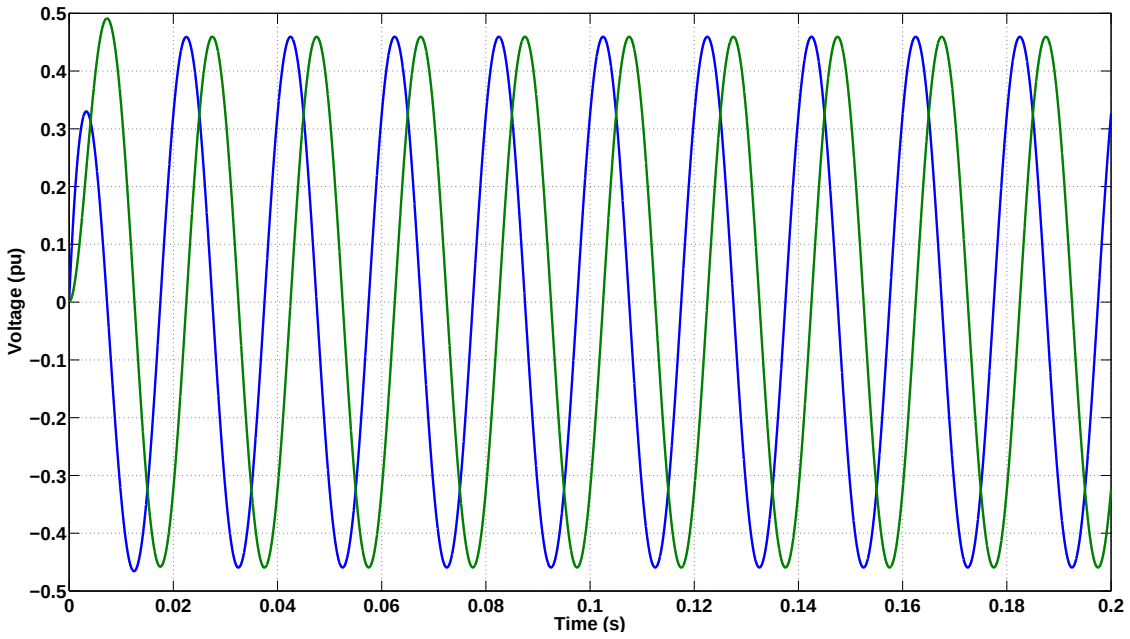


Fig. 4.3 *Simulation result*: $V_{s\alpha}$(blue) and $V_{s\beta}$(green) after passing through first low pass filter *(Scale: X-axis: 0.02 s/div, Y-axis: 0.1 pu/div or 80 V/div)*

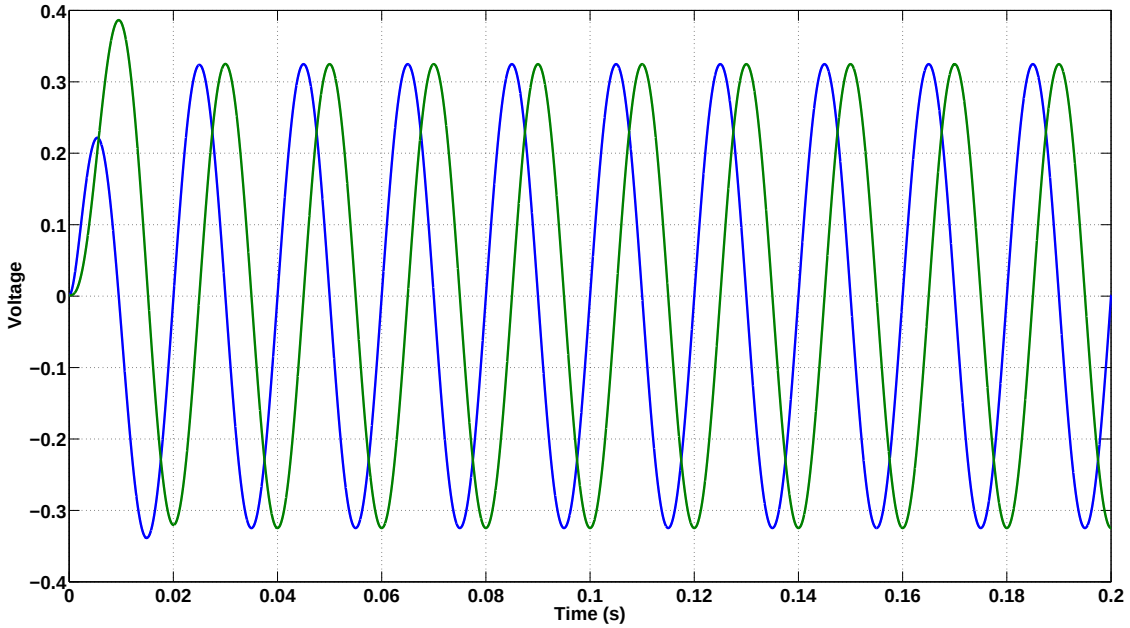


Fig. 4.4 *Simulation result*: $V_{s\alpha}$(blue) and $V_{s\beta}$(green) after passing through second low pass filter *(Scale: X-axis: 0.02 s/div, Y-axis: 0.1 pu/div or 80V/div)*

After normalizing the output of low pass filters, $Cos\theta$ and $Sin\theta$ can be obtained as shown in figure 4.6. The initial time for settling is due to the delay produced by low pass filters.

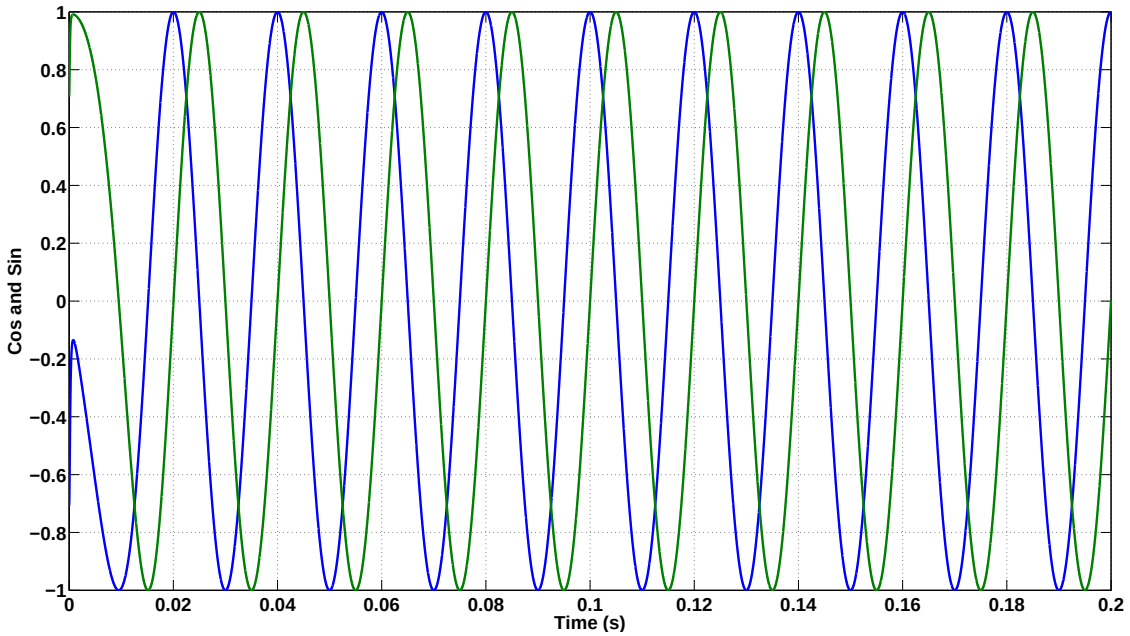


Fig. 4.5 *Simulation result*: $Cos\theta$(blue) and $Sin\theta$(green) *(Scale: X-axis: 0.02 s/div, Y-axis: 0.2 pu/div)*

In figure 4.7, it can be observed that the PLL output $Cos\theta$ and the grid voltage V_{sr} are in phase.

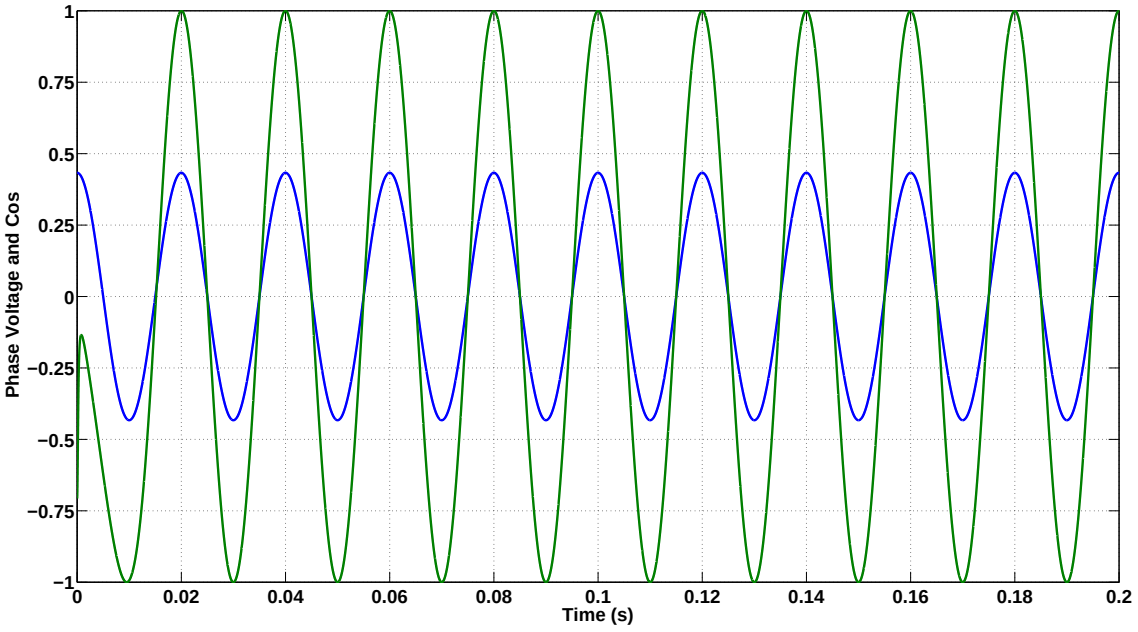


Fig. 4.6 *Simulation result*: $Cos\theta$(green) and V_{sr}(blue) *(Scale: X-axis: 0.02 s/div, Y-axis: 0.25 pu/div)*

4.2.2 3-phase 3-wire FEC results

The important wave forms of the 3-phase 3-wire FEC are given below.

The charging of DC bus from the initial pre-charged value (through diode bridge rectifier) to the voltage reference value (800V) is shown in figure 4.7. Here note that controller action starts after $0.1s$ of simulation.

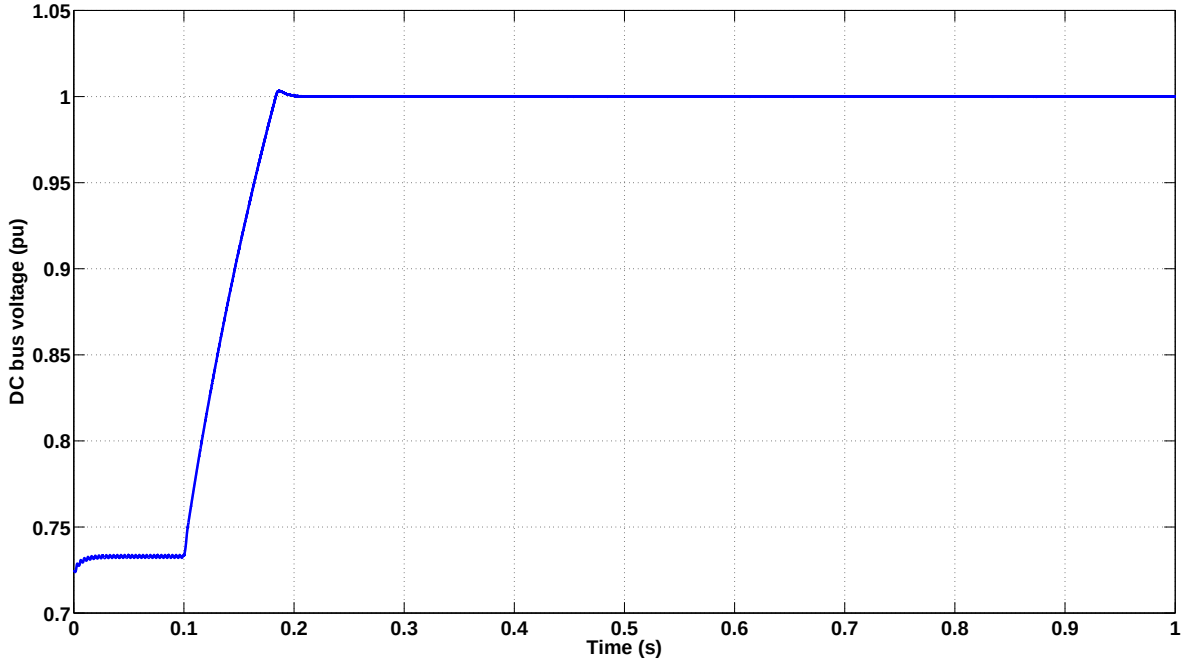


Fig. 4.7 *Simulation result*: DC bus charging from the initial pre-charged value to the reference voltage *(Scale: X-axis: 0.1 s/div, Y-axis: 0.05 pu/div or 40 V/div)*

The three phase line currents I_{sa}, I_{sb} and I_{sc} before staring controller, that is three phase currents through a three phase diode bridge rectifier is shown in figure 4.8.

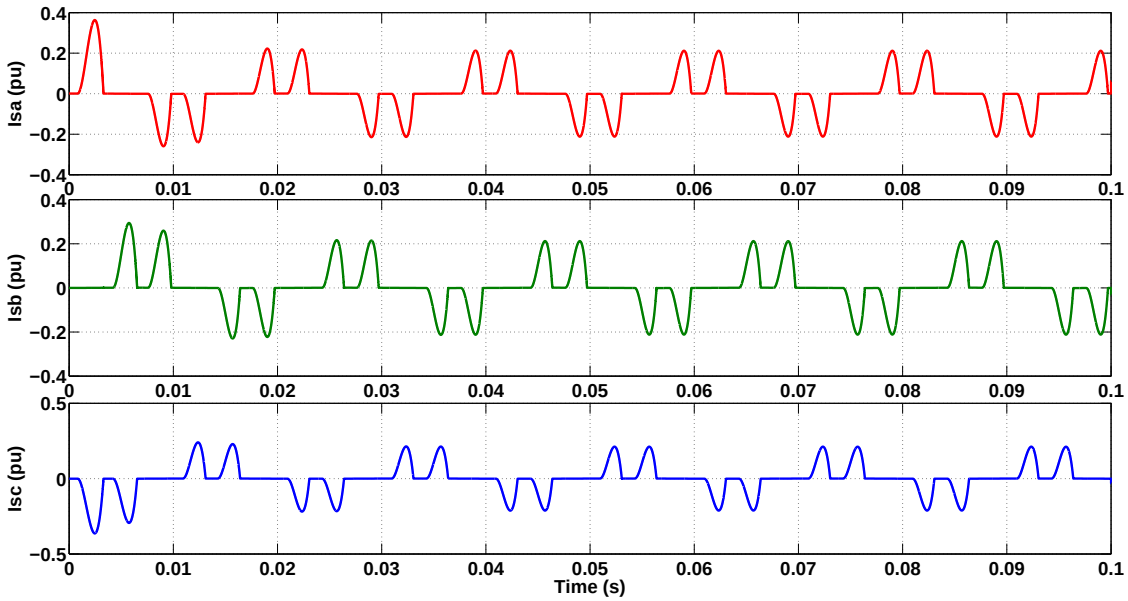


Fig. 4.8 *Simulation result*: Three phase line currents I_{sa}(blue), I_{sb}(green) and I_{sc}(red) through diode bridge rectifier *(Scale: X-axis: 0.01 s/div, Y-axis: 0.1 pu/div or 1.25 A/div)*

The three phase line currents I_{sa}, I_{sb} and I_{sc} at the starting of a 3-phase 3-wire FEC is shown in figure 4.9. Soft start-up for a 3-phase 3-wire FEC is achieved because of reduced starting inrush current.

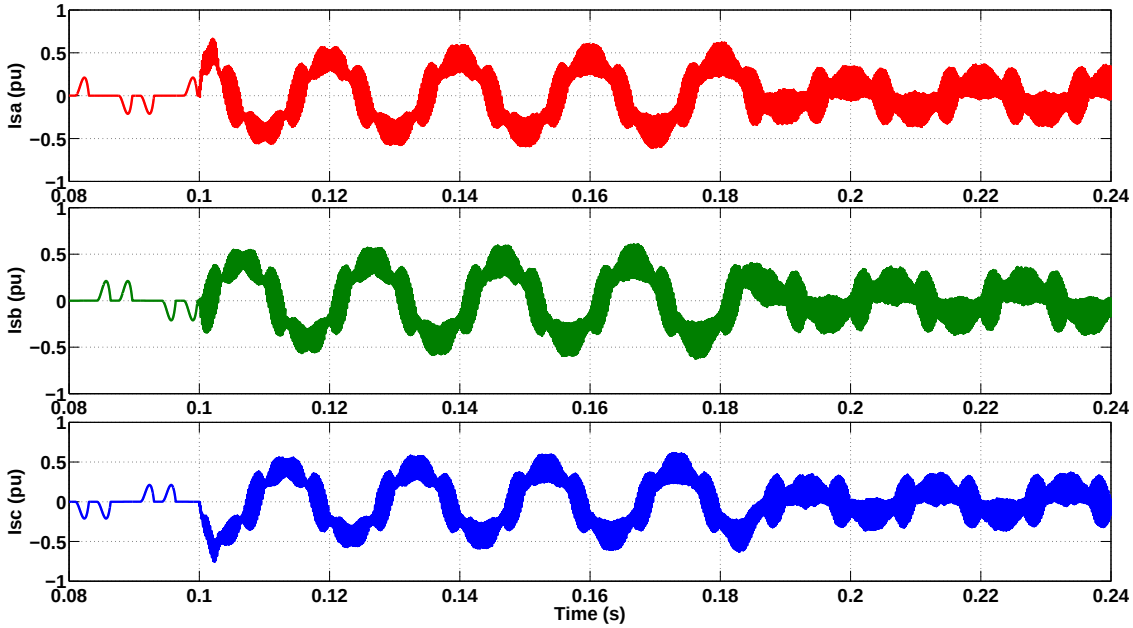


Fig. 4.9 *Simulation result*: Three phase line currents I_{sa}(blue), I_{sb}(green) and I_{sc}(red) at the starting of 3-phase 3-wire FEC *(Scale: X-axis: 0.02 s/div, Y-axis: 0.2 pu/div 2.5 A/div)*

The three phase line currents I_{sa}, I_{sb} and I_{sc} at the steady state of a 1 kVA 3-phase

3-wire FEC is shown in figure 4.10.

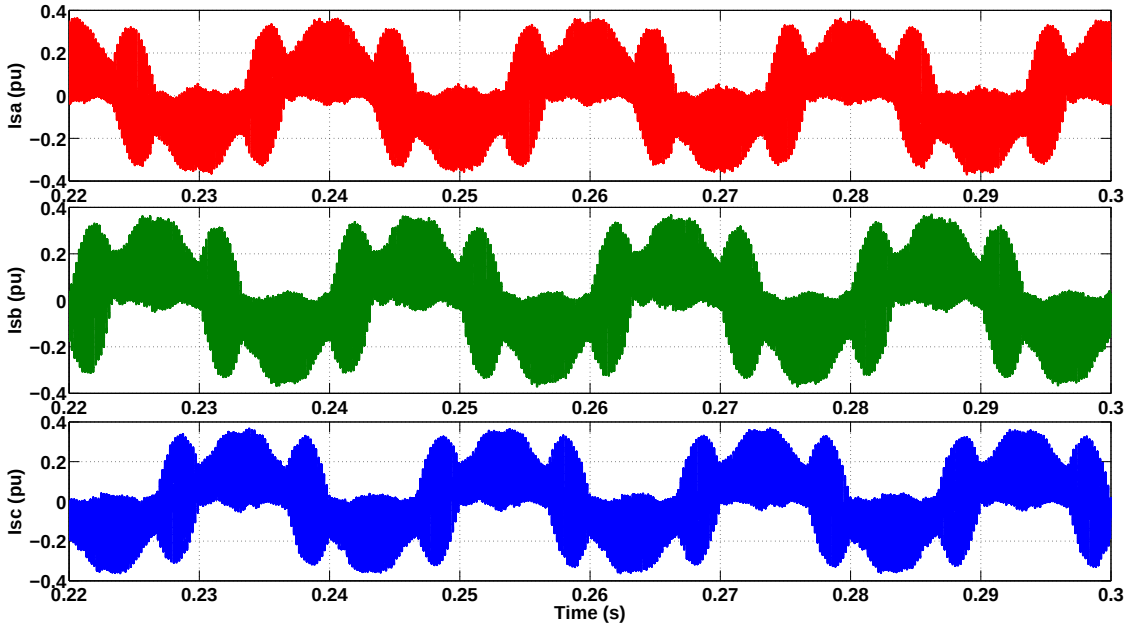


Fig. 4.10 *Simulation result*: Three phase line currents I_{sa}(blue), I_{sb}(green) and I_{sc}(red) at the steady state of 3-phase 3-wire FEC *(Scale: X-axis: 0.02 s/div, Y-axis: 0.2 pu/div or 2.5 A/div)*

The d-axis component of current I_{sd} following the reference I^*_{sd} is shown in figure 4.11. From figure 4.11, it can be observed that both I_{sd} and I^*_{sd} are DC in nature and contains switching frequency components.

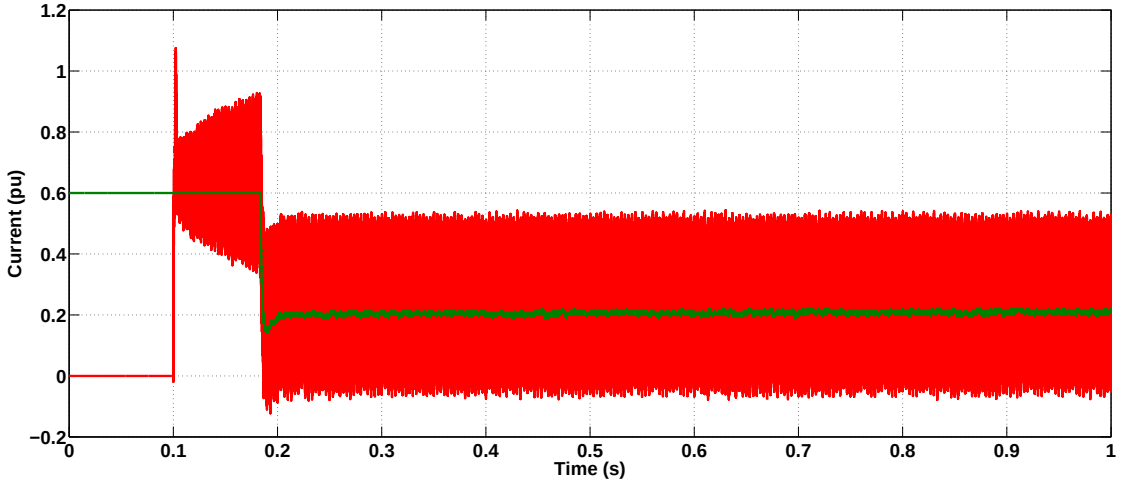


Fig. 4.11 *Simulation result*: I_{sd} (red) and I^*_{sd} (green) of a 3-phase 3-wire FEC *(Scale: X-axis: 0.1 s/div, Y-axis: 0.2 pu/div or 2.5 A/div)*

The q-axis component of current I_{sq} following the reference I^*_{sq} is shown in fig-

ure 4.12. From figure 4.12, it can be observed that both I_{sq} is DC in nature but contains switching frequency components while I^*_{sq} is DC in nature without any switching frequency components. Also in the figure 4.12 the grid delivers the power at unity power factor, since the reactive component of current is drawn from the grid is zero($I^*_{sq} = 0$)

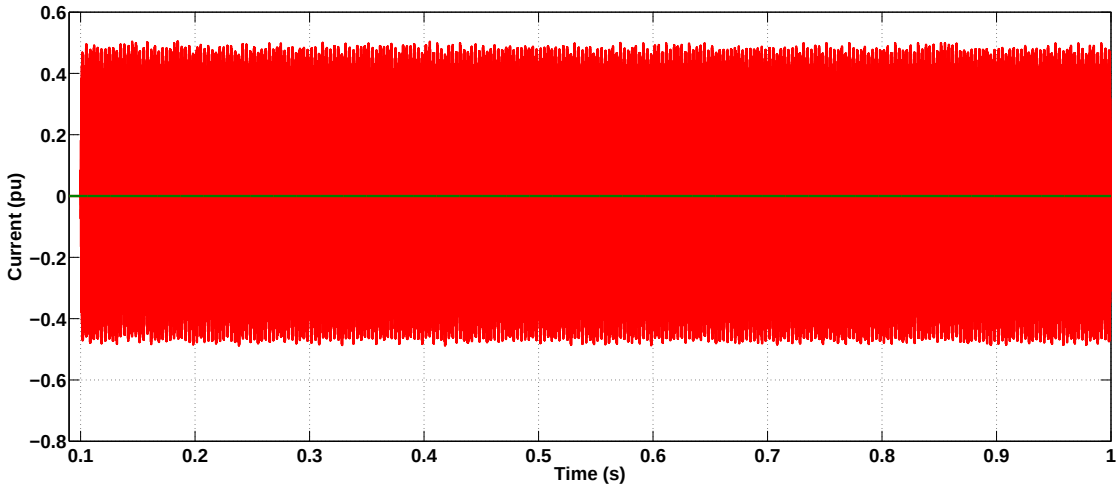


Fig. 4.12 *Simulation result*: I_{sq} (red) and I^*_{sq} (green) of a 3-phase 3-wire FEC *(Scale: X-axis: 0.1 s/div, Y-axis: 0.2 pu/div or 2.5 A/div)*

As explained in chapter 2, the reactive power flow from grid can be controlled through I_{sq} controller. That is by varying the I^*_{sq}, it is possible to draw power from the grid at different power factor. The real time variation in line current I_{sa} with respect to change in I^*_{sq} is shown in figure 4.13(a), where I^*_{sq} is increased from zero to $2pu$ and then decreased to zero and again decreased to $-2pu$. The change in the I^*_{sq} is shown in figure 4.13(b).

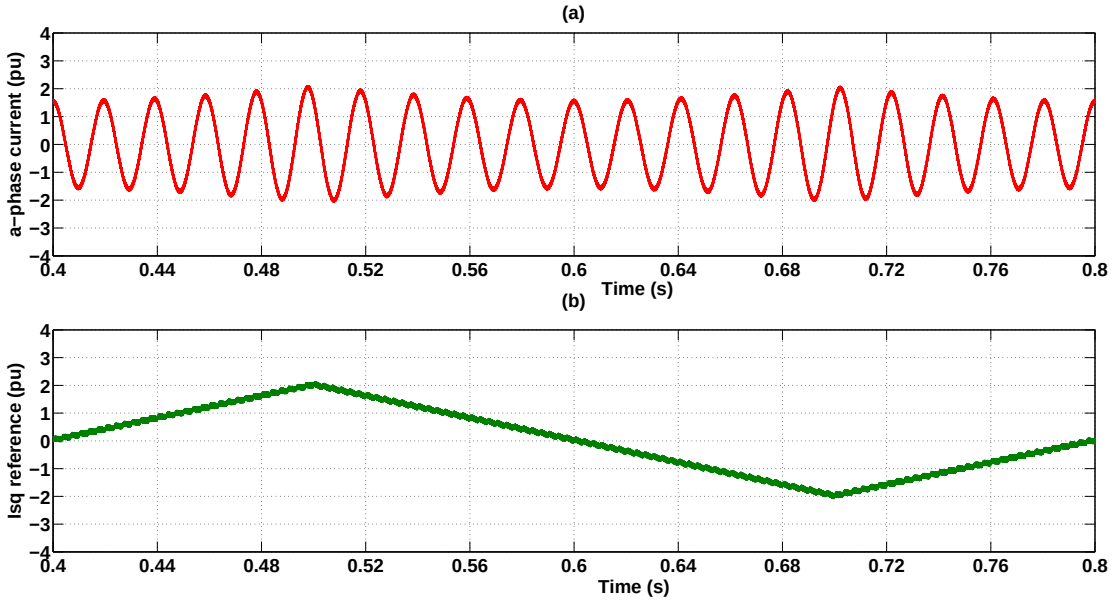


Fig. 4.13 *Simulation result*: The variation in line current I_{sa} (a) with respect to change in I^*_{sq} (b) -*Scale: X-axis: 0.04 s/div, Y-axis: 1 pu/div or 12.5 A/div*

The real time variation in the current I_{sq} with respect to change in I^*_{sq} is shown in figure 4.14, where I^*_{sq} is increased from zero to $2pu$ and then decreased to zero and again decreased to $-2pu$.

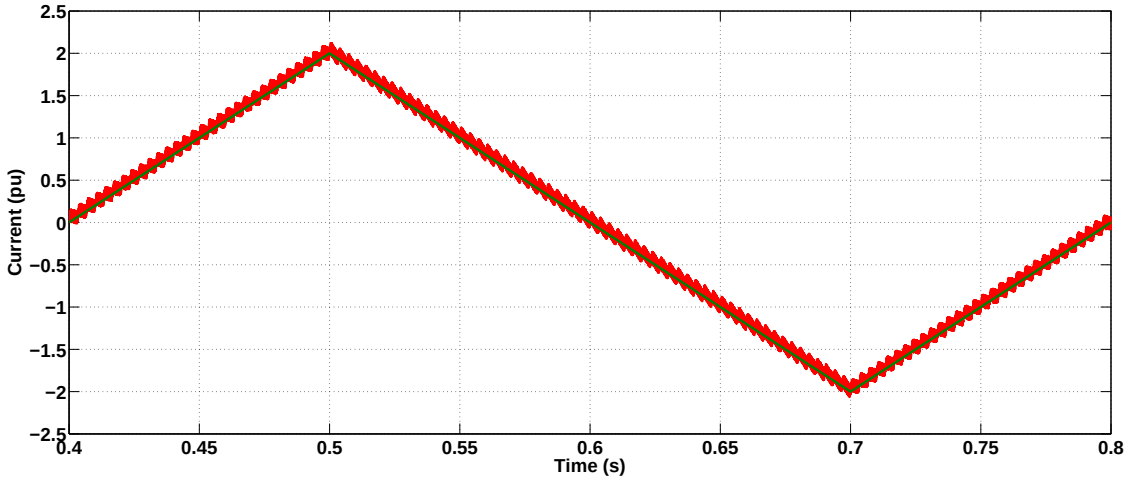


Fig. 4.14 *Simulation result*: Variation in I_{sq} (red) with respect to change in I^*_{sq} (green) of a 3-phase 3-wire FEC *(Scale: X-axis: 0.05 s/div, Y-axis: 0.5 pu/div or 6.25 A/div)*

The line current I_{sa} and phase voltage V_{sa} at $10kW$ (full load) load is shown in figure 4.15. Here the grid delivers power at unity power factor.

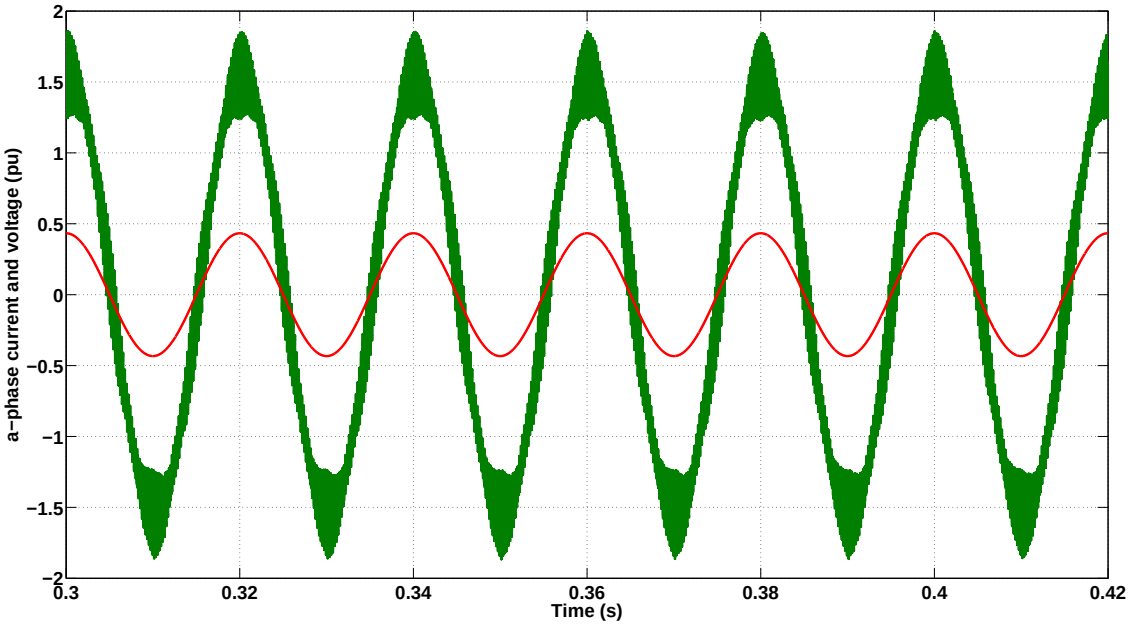


Fig. 4.15 *Simulation result*: Phase voltage V_{sa} (red -*Scale: X-axis: 0.02 s/div, Y-axis: 400 V/div*) and line current I_{sa} (green -*Scale: X-axis: 0.02 s/div, Y-axis: 6.25 A/div*) of a 3-phase 3-wire FEC at $10kW$ (full load) load

The line current I_{sa} and phase voltage V_{sa} at $I_{sq}^{*} = 2pu$ is shown in figure 4.16. Here the grid delivers power at leading power factor.

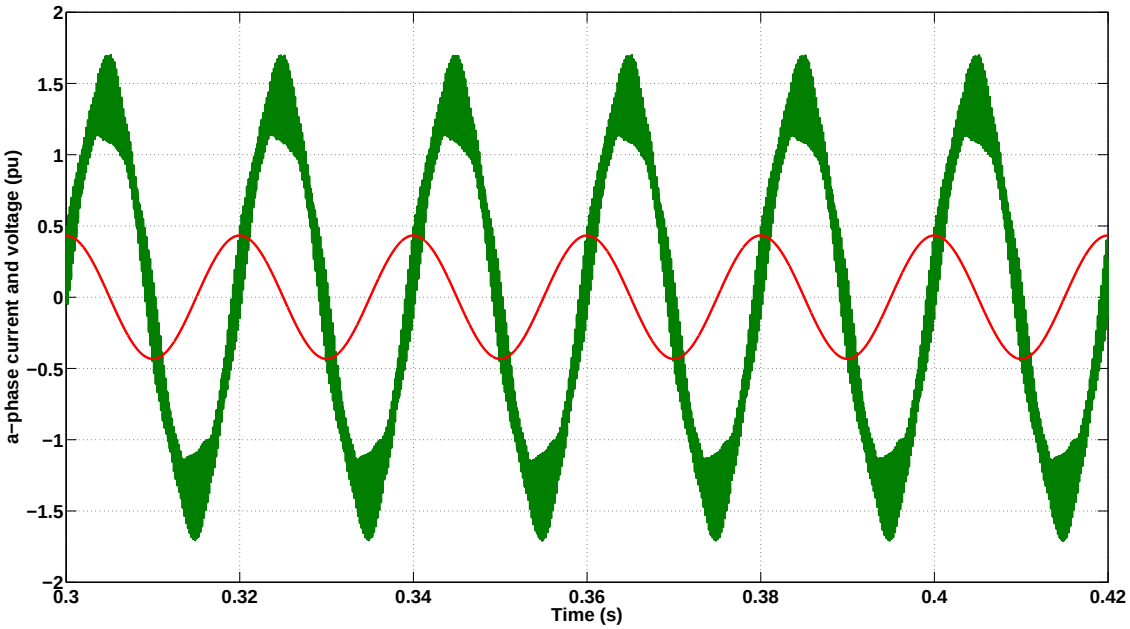


Fig. 4.16 *Simulation result*: Phase voltage V_{sa} (red -*Scale: X-axis: 0.02 s/div, Y-axis: 400 V/div*) and line current I_{sa} (green -*Scale: X-axis: 0.02 s/div, Y-axis: 6.25 A/div*) of a 3-phase 3-wire FEC at $I_{sq}^{*} = 2pu$

The line current I_{sa} and phase voltage V_{sa} at $I_{sq}^{*} = -2pu$ is shown in figure 4.17. Here the grid delivers power at lagging power factor.

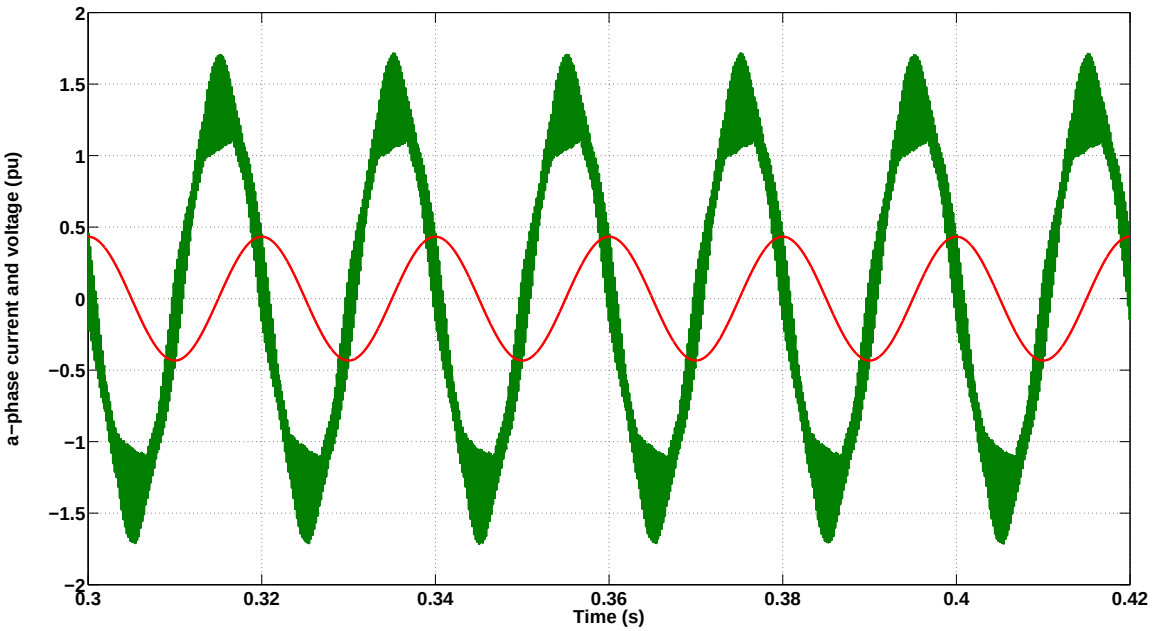


Fig. 4.17 *Simulation result*: Phase voltage V_{sa} (red -*Scale: X-axis: 0.02 s/div, Y-axis: 400 V/div*) and line current I_{sa} (green -*Scale: X-axis: 0.02 s/div, Y-axis: 6.25 A/div*) of a 3-phase 3-wire FEC at $I^*_{sq} = -2pu$

As explained before, the SPWM modulation technique will cause over modulation during the starting and thereby high inrush current compared to SVPWM technique. Figure 4.18(a) shows the a-phase current and figure 4.18(b) shows the a-phase modulating signal at the starting of 3-phase 3-wire FEC using SPWM modulation scheme. Figure 4.18(b) shows that a-phase modulating signal is going to the over modulation at the staring, and thereby high starting current as shown in figure 4.18(a).

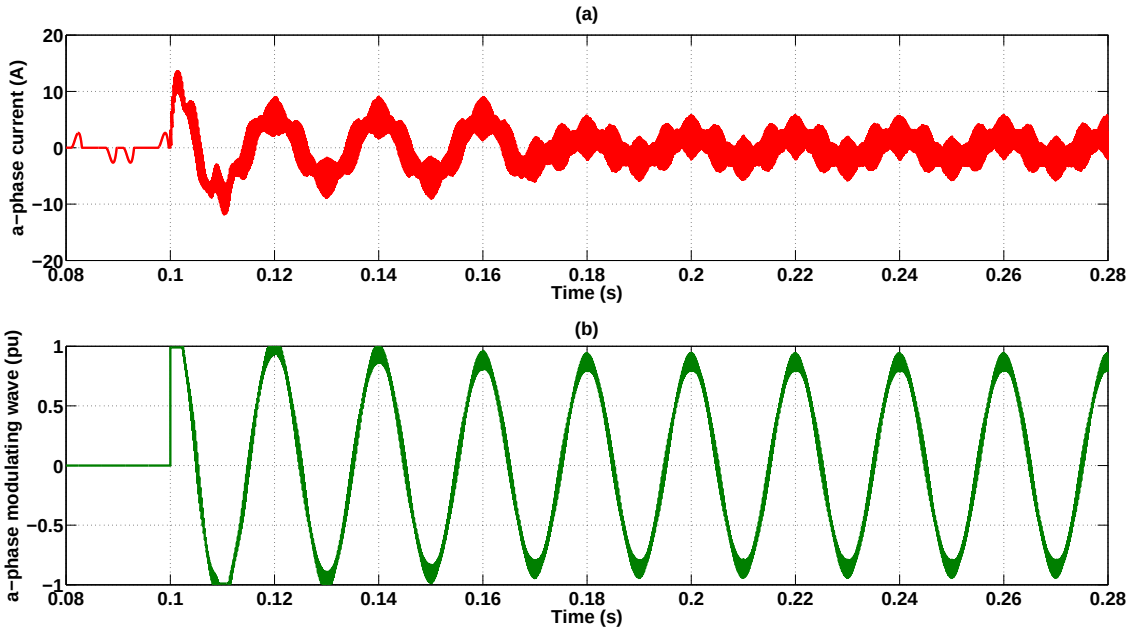


Fig. 4.18 *Simulation result*: Line current I_{sa} (red -*Scale: X-axis: 0.02 s/div, Y-axis: 10 A/div*) and a-phase modulating signal (green -*Scale: X-axis: 0.02 s/div, Y-axis: 0.5 pu/div*) at the starting of a 3-phase 3-wire FEC using SPWM scheme

Figure 4.19(a) shows the a-phase current and figure 4.19(b) shows the a-phase modulating signal at the starting of 3-phase 3-wire FEC using SVPWM modulation scheme. Figure 4.19(b) shows that a-phase modulating signal is not going to the over modulation at the staring, and thereby low starting current as shown in figure 4.19(a). By comparing figure 4.18(a) and figure 4.19(a), it can be concluded that string current of a FEC is less using SVPWM scheme compared to the use of SPWM modulation scheme.

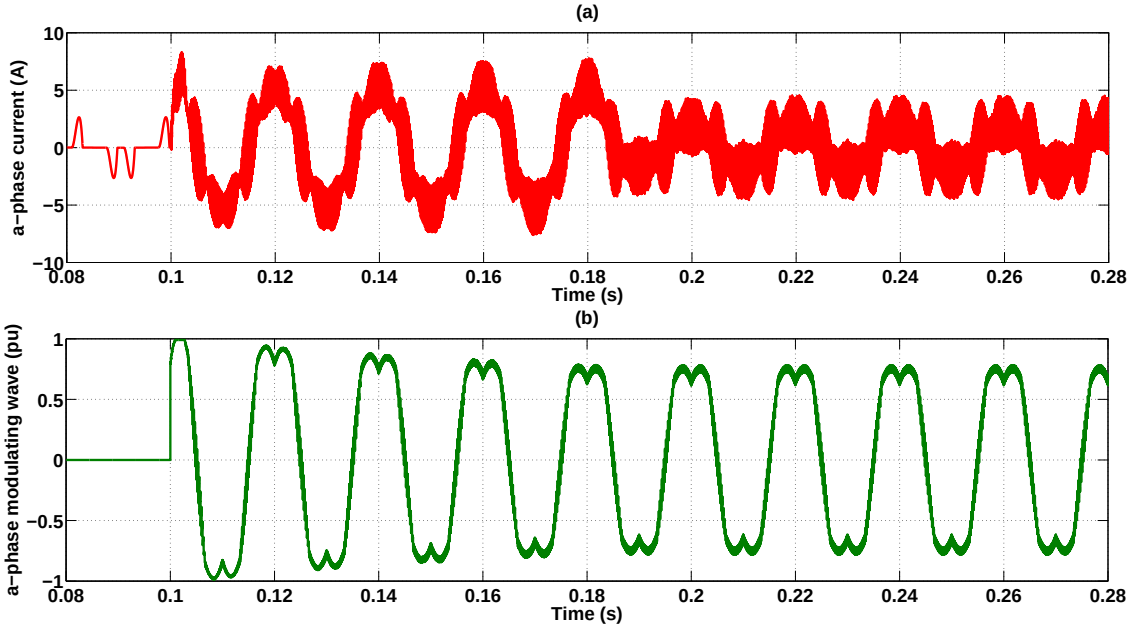


Fig. 4.19 *Simulation result*: Line current I_{sa} (red -*Scale: X-axis: 0.02 s/div, Y-axis: 5 A/div*) and *a*-phase modulating signal (green -*Scale: X-axis: 0.02 s/div, Y-axis: 0.5 pu/div*) at the starting of a 3-phase 3-wire FEC using SVPWM scheme

4.2.3 Elimination of lower order harmonic component from the line current of a 3-phase 3-wire FEC

The elimination of lower order harmonic component from the line current of a 3-phase 3-wire FEC is carried out with a 10kW DC load. The important results of elimination of $5th$ order harmonic components are given below.

The steady state line current I_{sa} without eliminating harmonic components is shown in figure 4.20

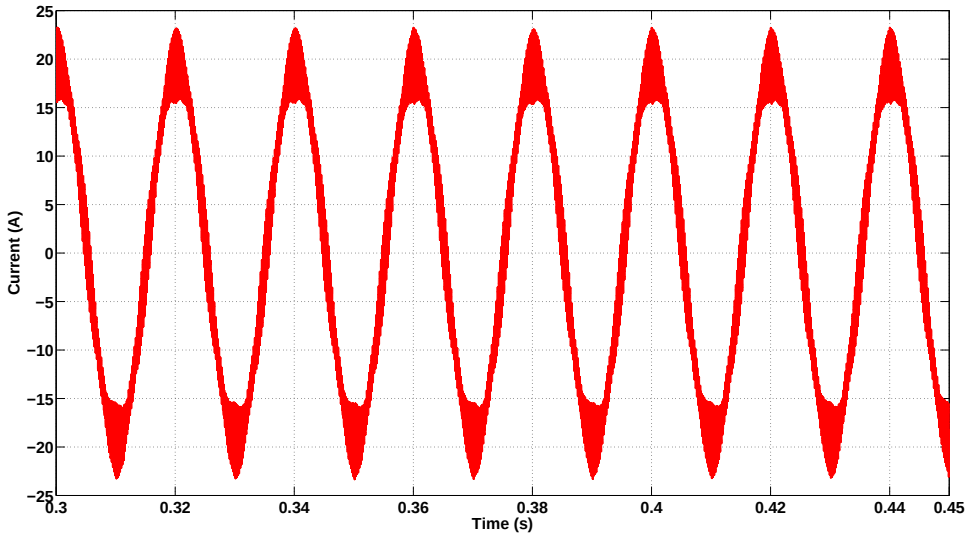


Fig. 4.20 *Simulation result*: The steady state line current I_{sa} *(Scale: X-axis: 0.02 s/div, Y-axis: 5 A/div)*

The harmonic spectrum of the steady state line current I_{sa} without eliminating harmonic components is shown in figure 4.21. The harmonic spectrum shows that there is a significant amount of $5th$ harmonic current present in the line current.

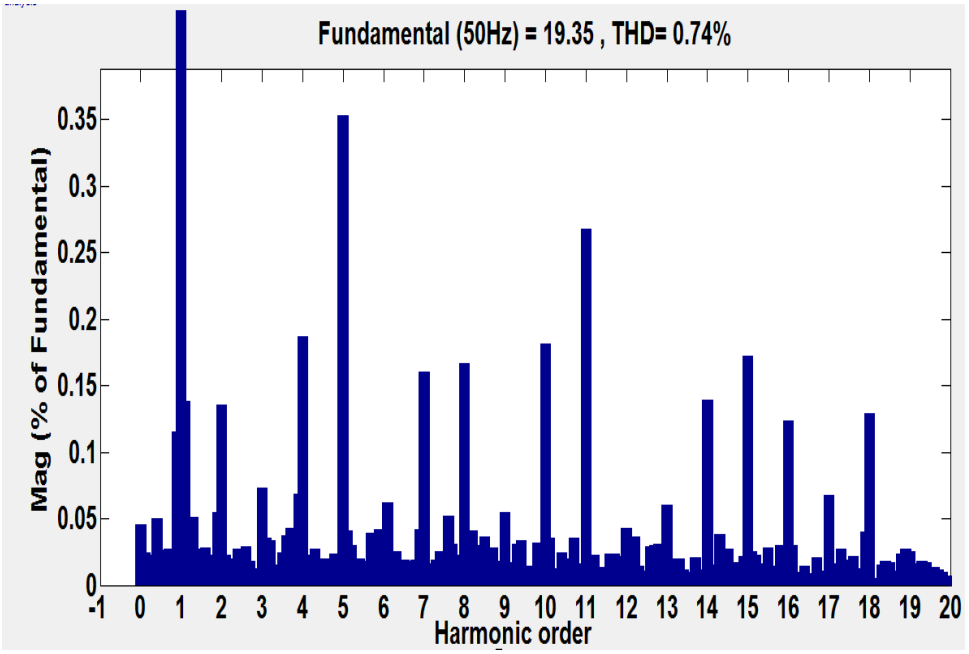


Fig. 4.21 *Simulation result*: The harmonic spectrum of line current I_{sa} without eliminating harmonic components

The steady state line current I_{sa} after eliminating $5th$harmonic component is shown in figure 4.22

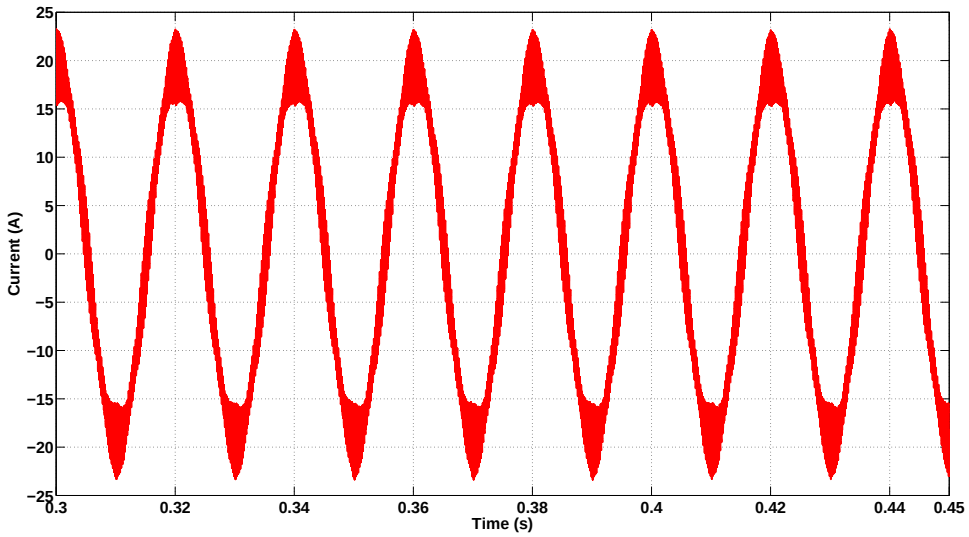


Fig. 4.22 *Simulation result*: The steady state line current I_{sa} after eliminating $5th$harmonic component *(Scale: X-axis: 0.02 s/div, Y-axis: 5 A/div)*

The harmonic spectrum of line current I_{sa} after eliminating $5th$ harmonic component is shown in figure 4.23. The $5th$ harmonic component is considerably reduced from the line current and thereby decrease in THD compared to current without eliminating harmonic components as shown in figure 4.23.

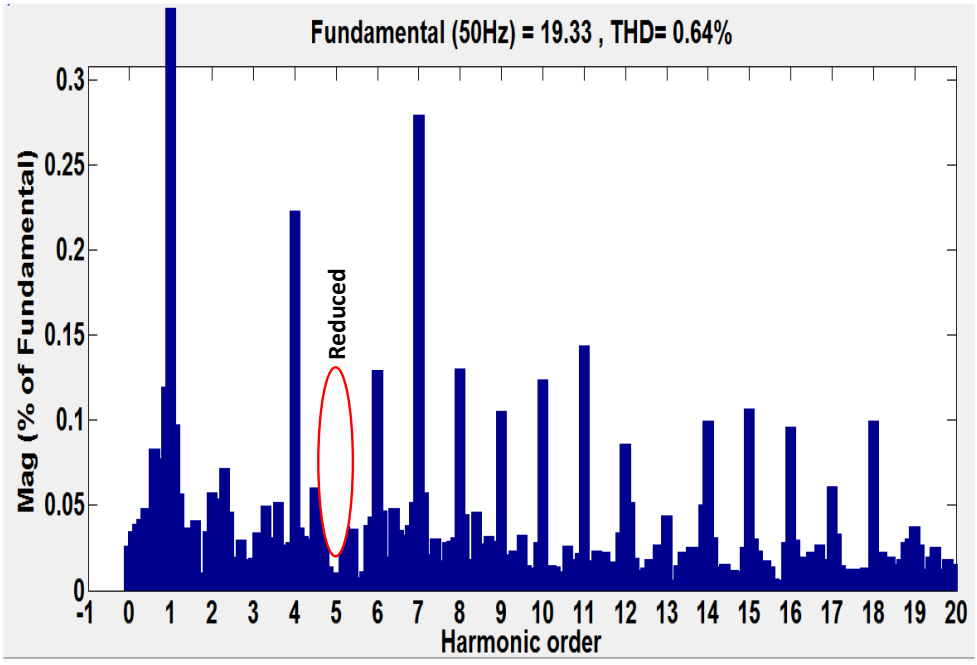


Fig. 4.23 *Simulation result*: The harmonic spectrum of line current I_{sa} after eliminating $5th$ harmonic component

The intermediate results during elimination process of $5th$ harmonic component are explained below.

The $5th$ harmonic PLL, that is $Cos5\theta$ and $Sin5\theta$ is shown in figure 4.24. The $5th$

harmonic PLL is derived from fundamental PLL using trigonometric expansions.

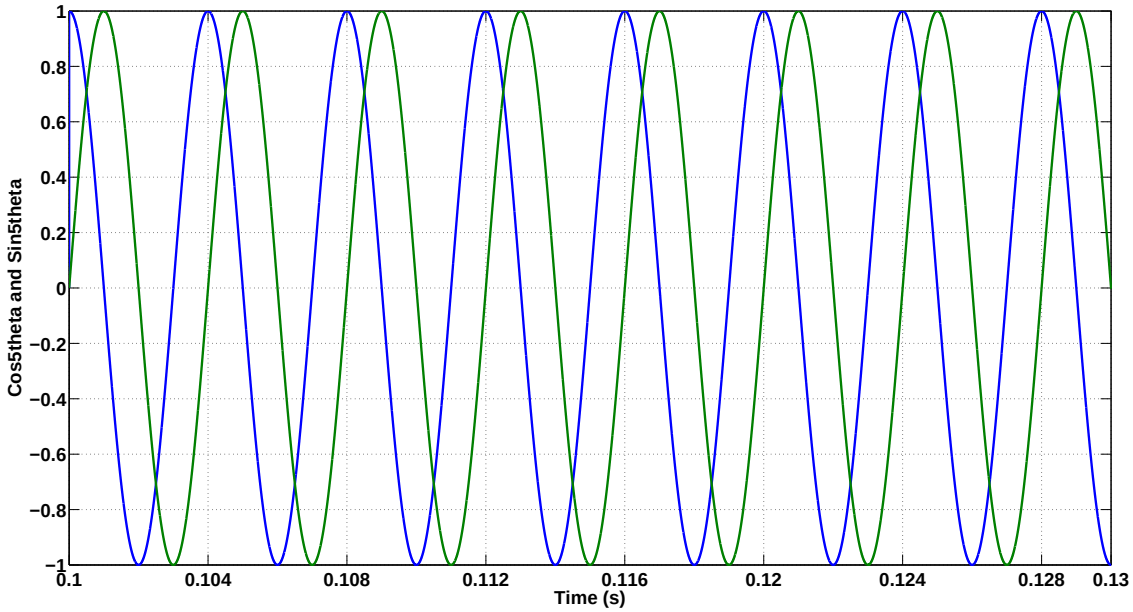


Fig. 4.24 *Simulation result*: $Cos5\theta$(blue) and $Sin5\theta$(green) *(Scale: X-axis: 0.004 s/div, Y-axis: 0.2 pu/div)*

The line current I_{sa} after extracting all the harmonic components using harmonic extraction technique is shown in figure 4.25, where it only contains the fundamental component of current.

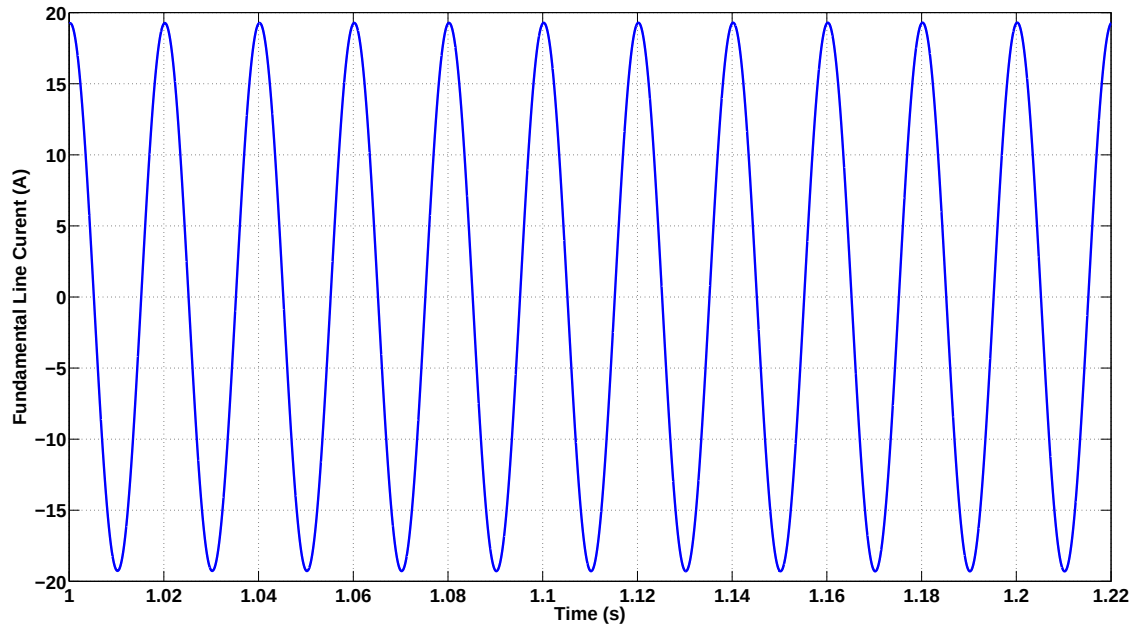


Fig. 4.25 *Simulation result*: Fundamental component of the line current I_{sa} *(Scale: X-axis: 0.02 s/div, Y-axis: 5 A/div)*

The harmonic components of line current I_{sa} after extracting the fundamental component is shown in figure 4.26, as explained above the harmonic components

contains a considerable amount of $5th$ harmonic.

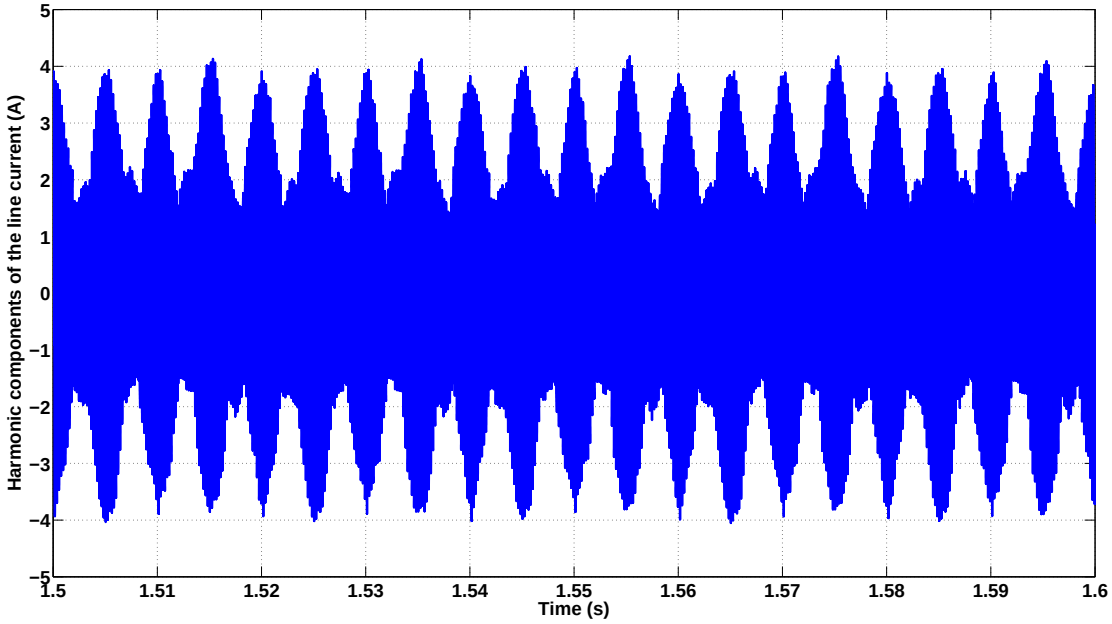


Fig. 4.26 *Simulation result*: Harmonic components of the line current I_{sa} *(Scale: X-axis: 0.01 s/div, Y-axis: 1 A/div)*

The reference ($I^*_{sd\_5}$) and feed back (I_{sd_5}) for the I_{sd_5} controller is shown in figure 4.27, where I_{sd_5} is the $5th$ harmonic d-axis component of the current vector in the $5th$ harmonic synchronous reference frame. The I_{sd_5} controller is used for the elimination of $5th$ harmonic d-axis component of the current vector from the line current.

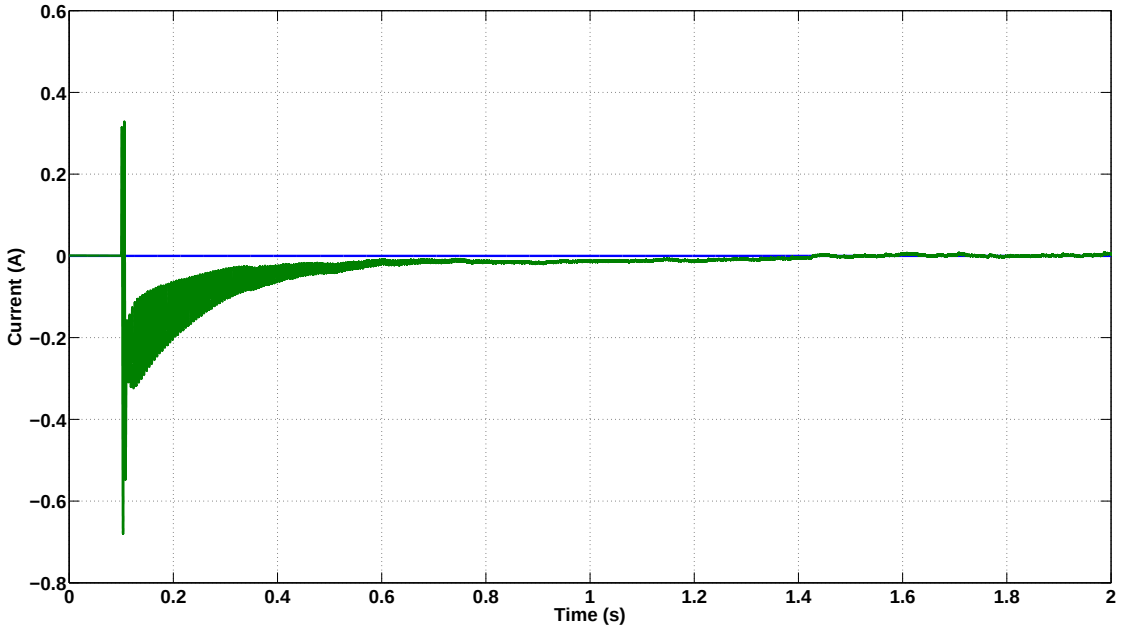


Fig. 4.27 *Simulation result*: $I^*_{sd\_5}$ (blue) and I_{sd_5} (green) *(Scale: X-axis: 0.2 s/div, Y-axis: 0.2 A/div)*

The reference ($I^*_{sq\_5}$) and feed back (I_{sq_5}) for the I_{sq_5} controller is shown in figure 4.28, where I_{sq_5} is the $5th$ harmonic q-axis component of the current vector in the $5th$ harmonic synchronous reference frame. The I_{sq_5} controller is used for the elimination of $5th$ harmonic q-axis component of the current vector from the line current.

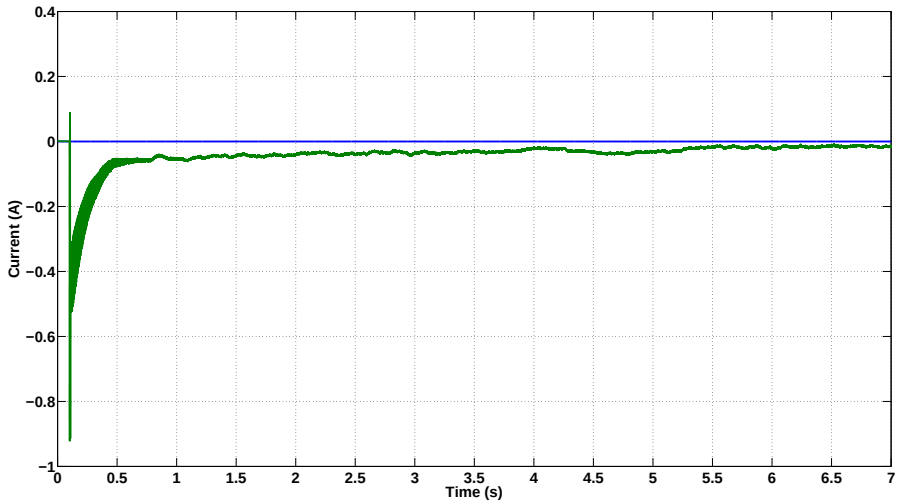


Fig. 4.28 *Simulation result*: $I^*_{sq\_5}$ (blue) and I_{sq_5} (green) *(Scale: X-axis: 0.5 s/div, Y-axis: 0.2 A/div)*

The three phase reference modulating signals corresponding to $5th$ harmonic is shown in figure 4.29. From figure 4.29, it can be observed that the modulating signals are at $5th$ harmonic frequency ($250Hz$). These modulating signals were further added with fundamental reference modulating signals.

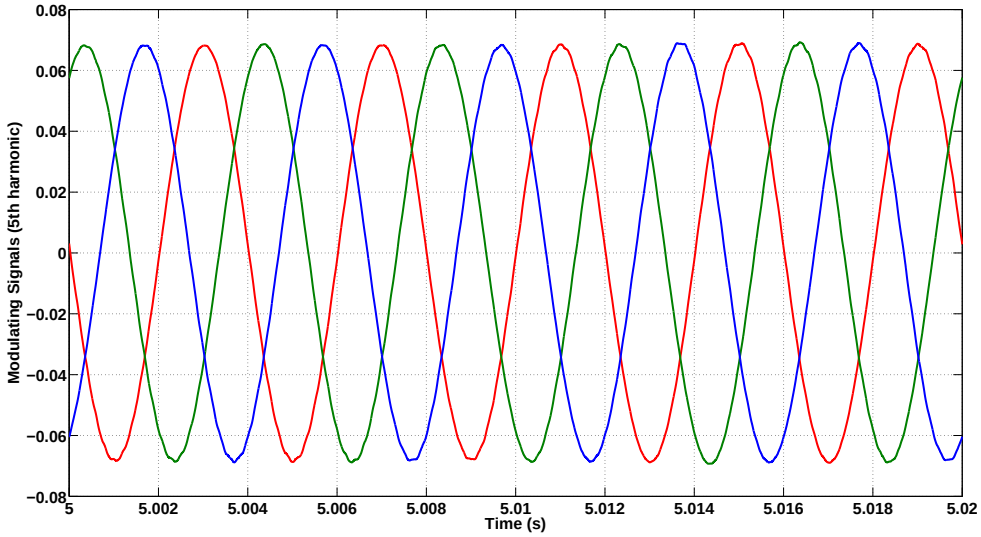


Fig. 4.29 *Simulation result*: Three phase reference modulating signals $V^*_{ina\_5}$ (red), $V^*_{inb\_5}$ (green), $V^*_{inc\_5}$ (blue) corresponding to $5th$ harmonic *(Scale: X-axis: 0.002 s/div, Y-axis: 0.02 pu/div)*

4.2.4 3-phase 4-wire FEC results

As explained in chapter2, the 3-phase 4-wire FEC is implemented with an additional common mode filter (L_c) in the neutral wire in order to reduce the switching harmonic distortions from the neutral current. In simulation, experiments have been carried out with and without common mode filter. The relevant wave forms of the 3-phase 4-wire FEC are given below.

The neutral current without neutral current (I_n) controller and without L_c using SPWM scheme is shown in figure 4.30(a). Figure 4.30(a) shows that there is lower order harmonics and huge amount of switching ripple current in the neutral wire. As explained before, the reason for lower order common mode harmonic current is unbalance in the voltages of DC capacitors, which is shown in figure 4.30(b). It is important to that in figure 4.30(b) even though there is mismatch in the voltage of two DC capacitors, addition of both voltage make the total DC bus voltage to $800V$, that is DC bus voltage control is perfectly working in the case of 3-phase 4-wire FEC even without neutral current controller.

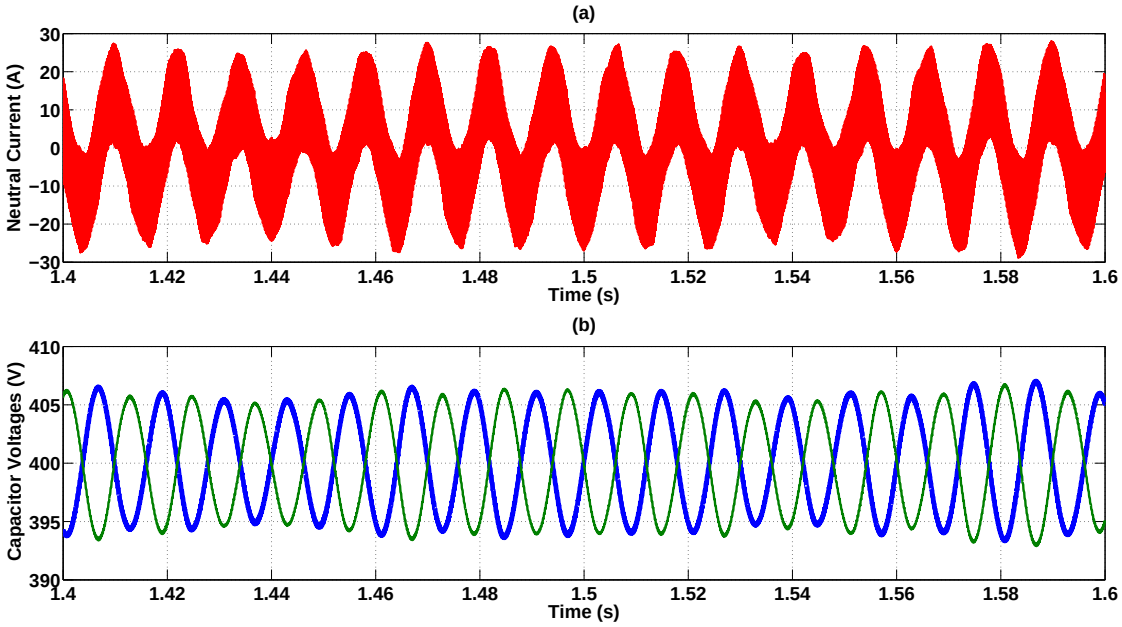


Fig. 4.30 *Simulation result*: (a)Neutral current (*(Scale: X-axis: 0.02 s/div, Y-axis: 10 A/div)*) (b) Two DC capacitor voltages (*(Scale: X-axis: 0.02 s/div, Y-axis: 5 V/div)*) without the L_c and without I_n controller using SPWM scheme

The neutral current with neutral current (I_n) controller and without L_c using SPWM scheme is shown in figure 4.31(a). Figure 4.31(a) shows that there is no

lower order harmonics and huge amount of switching ripple current in the neutral wire. From figure 4.31(b), it can be observed that there is no mismatch between the voltages of the two DC capacitors, that is I_n controller perfectly eliminated the neutral current and thereby the mismatch between capacitor voltages are also got eliminated.

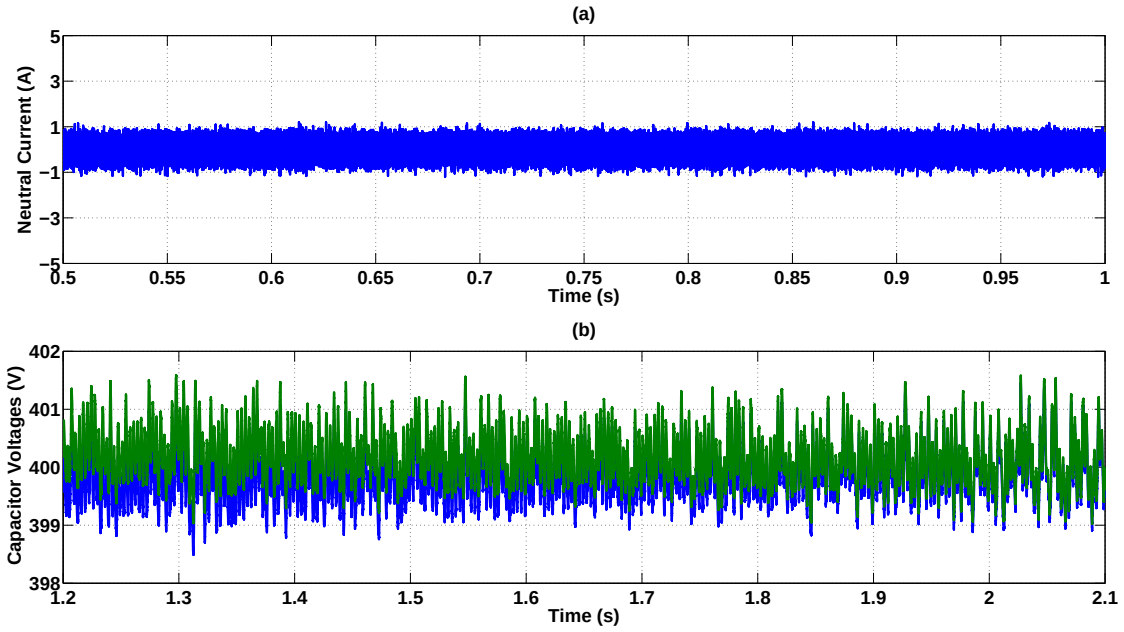


Fig. 4.31 *Simulation result*: (a)Neutral current (*(Scale: X-axis: 0.05 s/div, Y-axis: 2 A/div)*) (b) Two DC capacitor voltages (*(Scale: X-axis: 0.1 s/div, Y-axis: 1 V/div)*) without the L_c and with I_n controller using SPWM scheme

The neutral current without neutral current (I_n) controller and with L_c using SPWM scheme is shown in figure 4.32(a). Figure 4.32(a) shows that there is lower order harmonics and some amount of switching ripple current in the neutral wire. The switching ripple current reduced compare to figure 4.30(a) is because of the impedance offered by the common mode inductor. As explained before, the reason for lower order common mode harmonic current is unbalance in the voltages of DC capacitors, which is shown in figure 4.32(b). It is important to that in figure 4.32(b) even though there is mismatch in the voltage of two DC capacitors, addition of both voltage make the total DC bus voltage to $800V$. Also there is a decrease in the magnitude of the osculations of the capacitor voltages in the figure 4.32(b) compared to figure 4.30(b), this because of the presence of L_c.

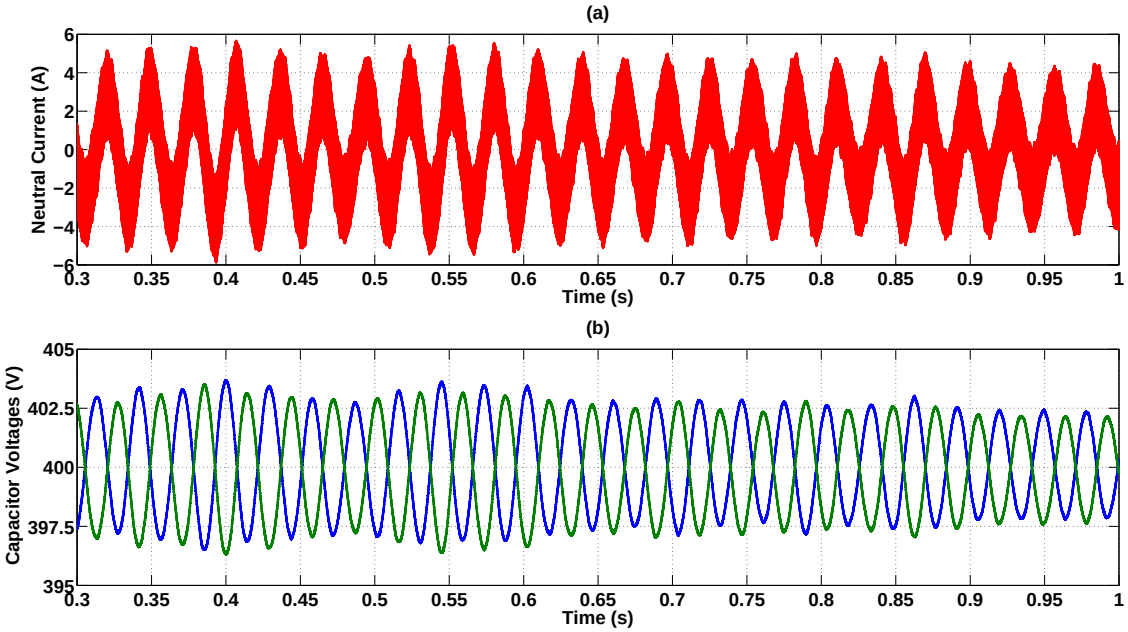


Fig. 4.32 *Simulation result*: (a)Neutral current (*(Scale: X-axis: 0.05 s/div, Y-axis: 2 A/div)*) (b) Two DC capacitor voltages (*(Scale: X-axis: 0.05 s/div, Y-axis: 2.5 V/div)*) with the L_c and without I_n controller using SPWM scheme

The neutral current with neutral current (I_n) controller and with L_c using SPWM scheme is shown in figure 4.33(a). Figure 4.33(a) shows that there is no lower order harmonics and less amount of switching ripple current in the neutral wire. From figure 4.33(b), it can be observed that there is no mismatch between the voltages of the two DC capacitors, that is I_n controller perfectly eliminated the neutral current and thereby the mismatch between capacitor voltages are also got eliminated. The amount of switching ripple voltage content in the DC bus capacitors shown in figure 4.33(b) is less compared to the figure shown in 4.31(b) because of the presence of L_c in the neutral wire.

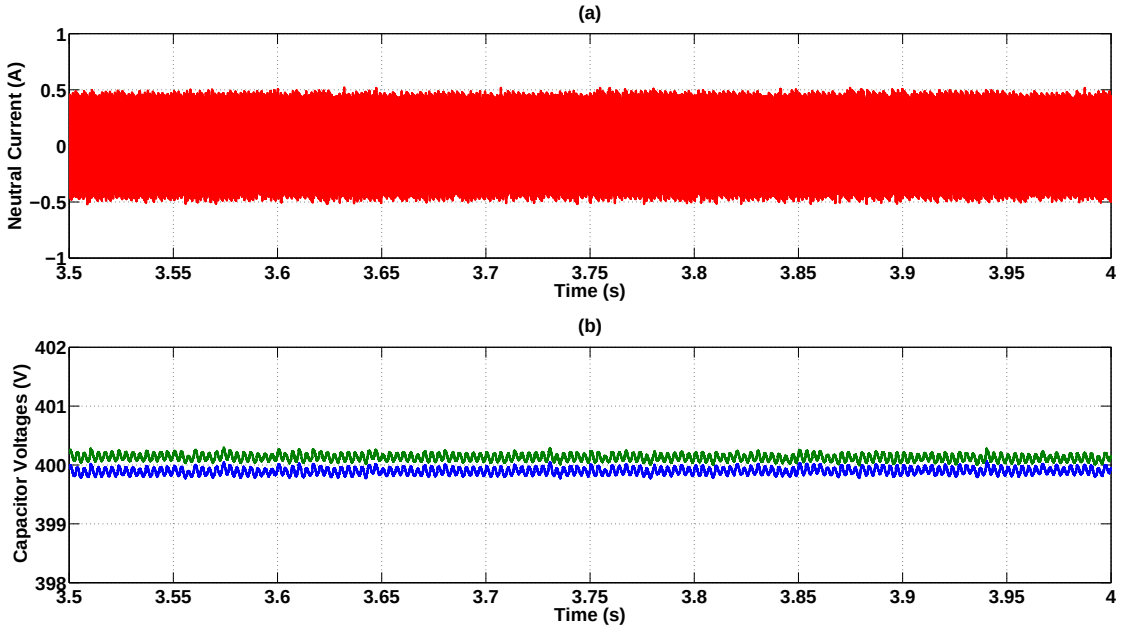


Fig. 4.33 *Simulation result*: (a)Neutral current (*(Scale: X-axis: 0.05 s/div, Y-axis: 0.5 A/div)*) (b) Two DC capacitor voltages (*(Scale: X-axis: 0.05 s/div, Y-axis: 1 V/div)*) with the L_c and with I_n controller using SPWM scheme

4.3 Hardware Results

4.3.1 PLL Results

The three phase balance grid voltages V_{sr}, V_{sy}, V_{sb} are converted into $V_{s\alpha}$ and $V_{s\beta}$, which is given in figure 4.34.

The outputs of first low pass filter and second low pass filter with input as $V_{s\alpha}$ and $V_{s\beta}$ are given in figure 4.35 and 4.36 respectively. Here, the output magnitude is decreasing by $\sqrt{2}$ and phase shift of 45° as it passing through each low pass filters.

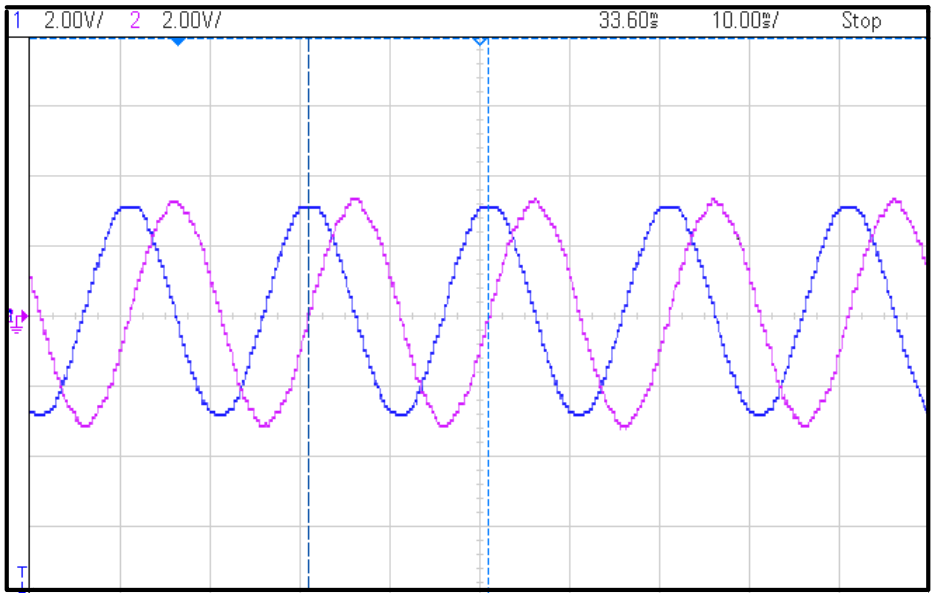


Fig. 4.34 *Hardware result*: $V_{s\alpha}$(blue) and $V_{s\beta}$(violet) *(Scale: X-axis: 0.01 s/div, Y-axis: 0.4 pu/div or 320 V/div)*

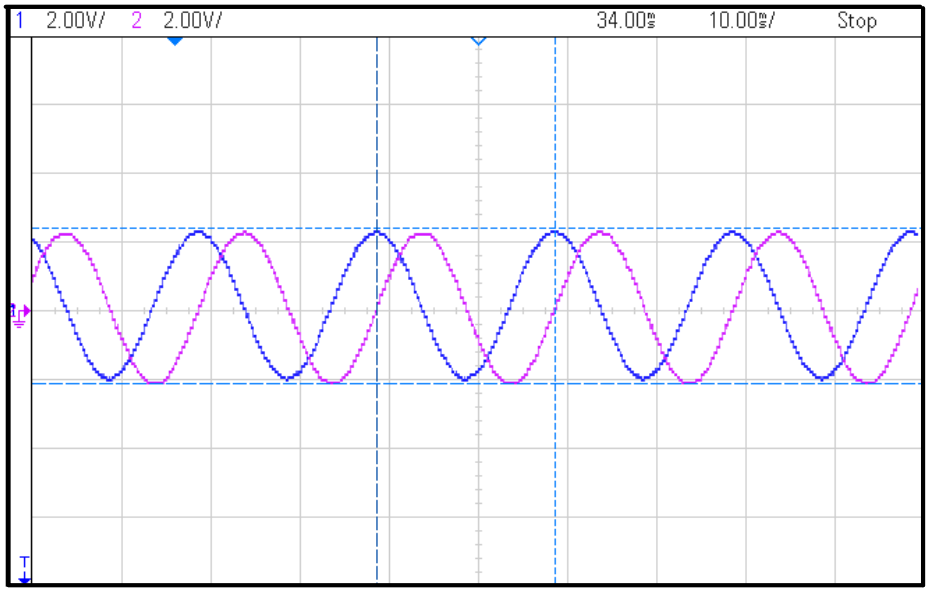


Fig. 4.35 *Hardware result*: $V_{s\alpha}$(blue) and $V_{s\beta}$(violet) after passing through first low pass filter *(Scale: X-axis: 0.01 s/div, Y-axis: 0.4 pu/div or 320 V/div)*

After normalizing the output of low pass filters, $Cos\theta$ and $Sin\theta$ can be obtained as shown in figure 4.37.

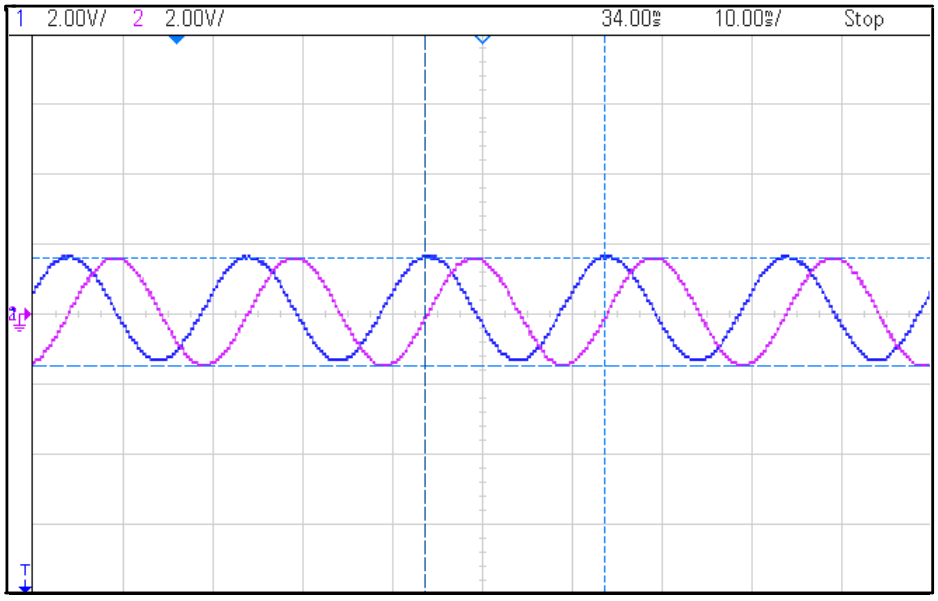


Fig. 4.36 *Hardware result*: $V_{s\alpha}$(blue) and $V_{s\beta}$(violet) after passing through second low pass filter *(Scale: X-axis: 0.01 s/div, Y-axis: 0.4 pu/div or 320 V/div)*

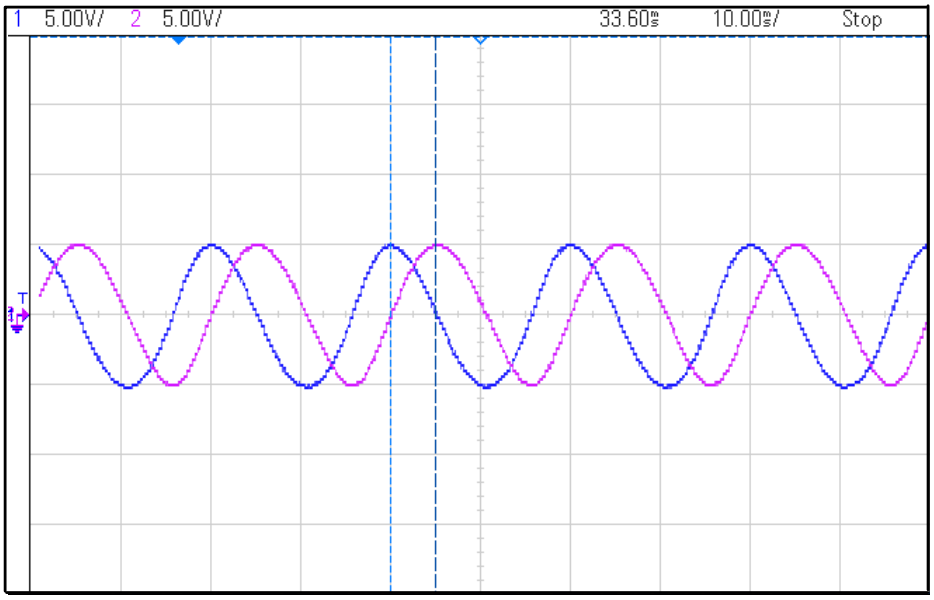


Fig. 4.37 *Hardware result*: $Cos\theta$(blue) and $Sin\theta$(violet) *(Scale: X-axis: 0.01 s/div, Y-axis: 1 pu/div)*

In figure 4.38, it can be observed that the PLL output $Cos\theta$ and the grid voltage V_{sr} are in phase.

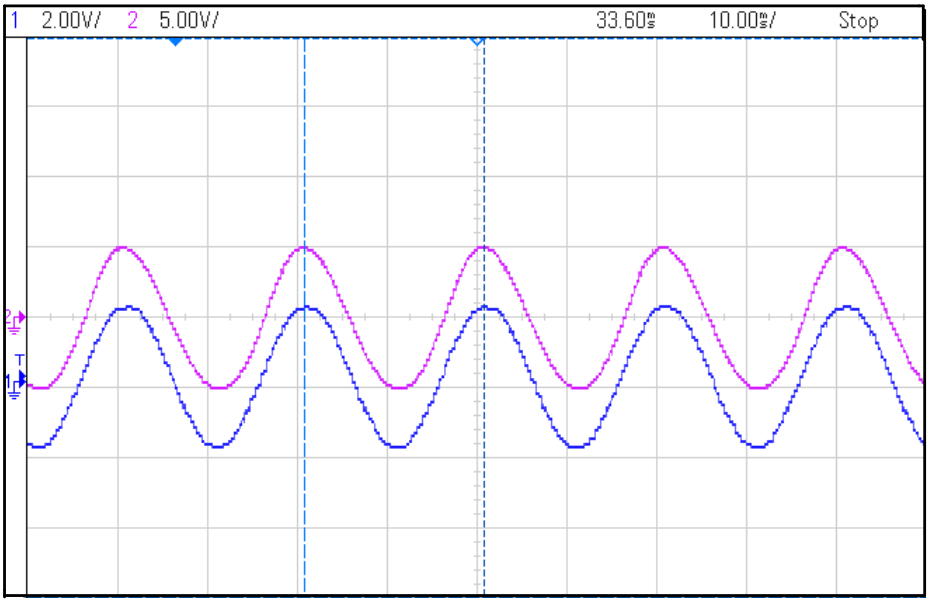


Fig. 4.38 *Hardware result*: V_{sa}(blue -*Scale: X-axis: 0.01 s/div, Y-axis: 0.4 pu/div or 320 V/div)*) and $Cos\theta$(violet - *Scale: X-axis: 0.01 s/div, Y-axis: 1 pu/div)*

4.3.2 3-phase 3-wire FEC results

The important wave forms of 3-phase 3-wire FEC from the hardware are given below.

The charging of DC bus from the initial pre-charged value (through diode bridge rectifier) to the voltage reference value (800V) is shown in figure 4.39. It takes $300ms$ to build up the voltage from the initial pre-charged value (through diode bridge rectifier) to the voltage reference value (800V) .

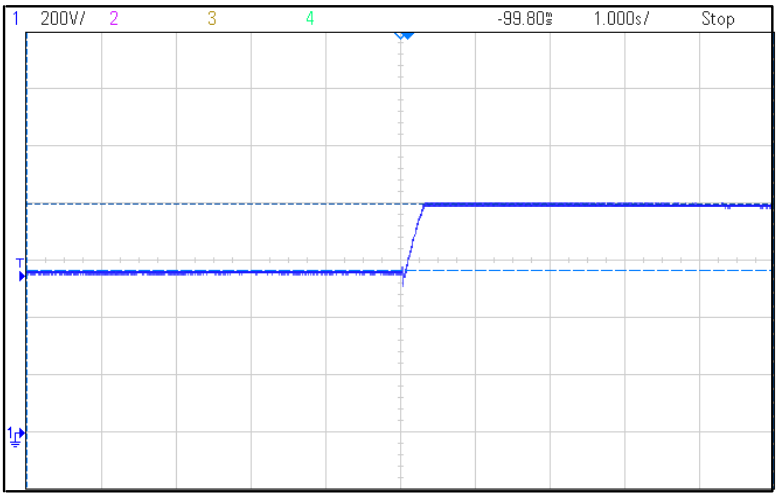


Fig. 4.39 *Hardware result*: DC bus voltage rising from the initial pre-charged value to 800V *(Scale: X-axis: 1 s/div, Y-axis: 200 V/div)*

The line current I_{sa} along with phase voltage V_{sa} is shown in figure 4.40. The figure 4.40 includes I_{sa} and V_{sa} of a three phase diode bridge rectifier, I_{sa} and V_{sa} at the starting of a 3-phase 3-wire FEC and steady state I_{sa} and V_{sa} of a 3-phase 3-wire FEC. Soft start-up for a 3-phase 3-wire FEC is achieved because of reduced starting inrush current. The figure 4.40 also explains that, in the case of 3-phase 3-wire FEC I_{sa} and V_{sa} are in phase, that is AC grid source delivers power at the unity power factor.

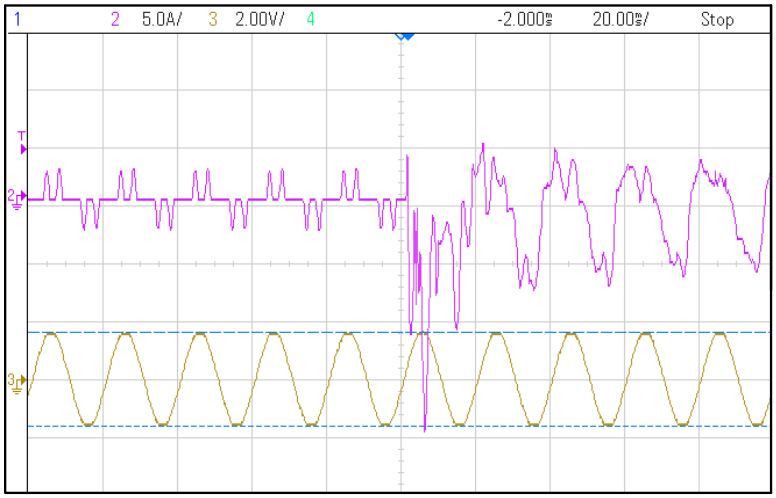


Fig. 4.40 *Hardware result*: Line current I_{sa}(violet -*Scale: X-axis: 0.02 s/div, Y-axis: 5 A/div*) and phase voltage V_{sa} (brown -*Scale: X-axis: 0.02 s/div, Y-axis: 400 V/div*) of a 3-phase 3-wire FEC at the starting

The steady state line current I_{sa} with phase voltage V_{sa} is shown in figure 4.41. Here, I_{sa} and V_{sa} are in phase, that is AC grid source delivers power at the unity power factor.

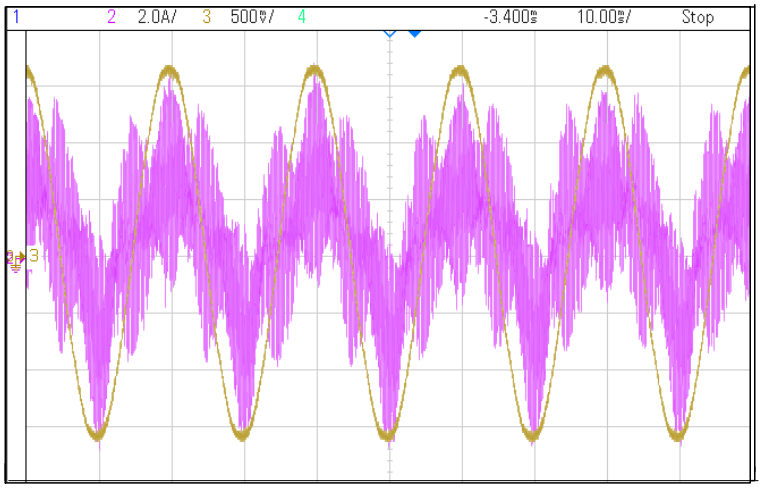


Fig. 4.41 *Hardware result*: Line current I_{sa}(violet -*Scale: X-axis: 0.01 s/div, Y-axis: 2 A/div*) and phase voltage V_{sa} (brown -*Scale: X-axis: 0.01 s/div, Y-axis: 100 V/div*) of a 3-phase 3-wire FEC at the steady state

The d-axis component of current I_{sd} following the reference I^*_{sd} is shown in figure 4.43. From figure 4.43, it can be observed that both I_{sd} and I^*_{sd} are DC in nature and contains switching frequency components.

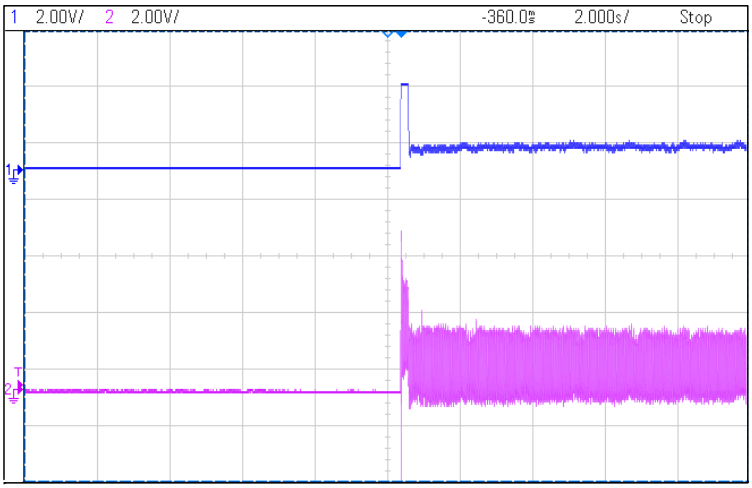


Fig. 4.42 *Hardware result*: I_{sd} (violet) and I^*_{sd} (blue) of a 3-phase 3-wire FEC -*Scale: X-axis: 2 s/div, Y-axis: 0.4 pu/div or 5 A/div*)

The q-axis component of current I_{sq} following the reference I_{sq}^{*} is shown in figure 4.43. From figure 4.43, it can be observed that both I_{sq} is DC in nature but contains switching frequency components while I_{sq}^{*} is DC in nature without any switching frequency components. Also in the figure 4.43 the grid delivers the power at unity power factor, since the reactive component of current is drawn from the grid is zero($I_{sq}^{*} = 0$).

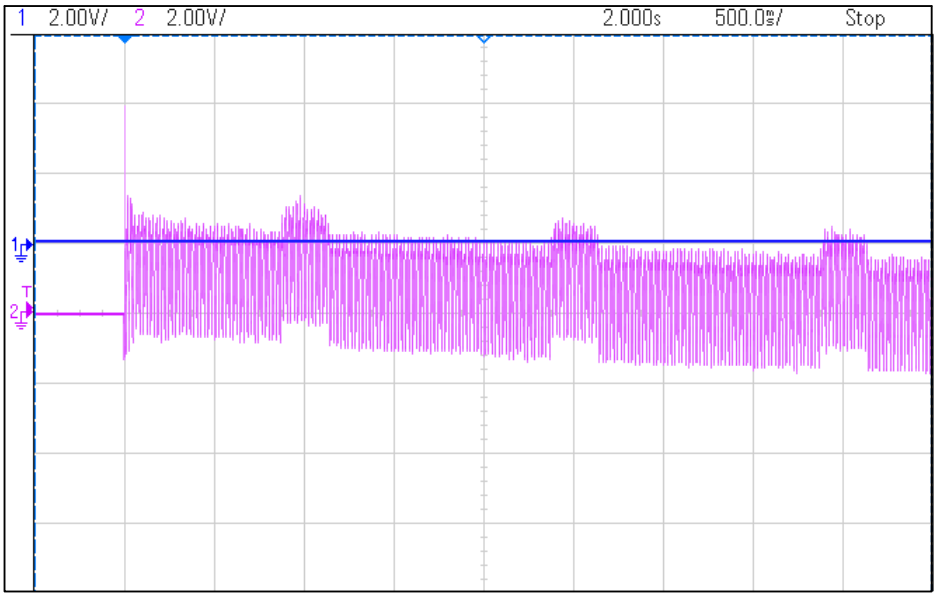


Fig. 4.43 *Hardware result*: I_{sq} (violet) and I_{sq}^{*} (blue) of a 3-phase 3-wire FEC *-Scale: X-axis: 0.5 s/div, Y-axis: 0.4 pu/div or 5 A/div*)

As explained in chapter 2, the reactive power flow from grid can be controlled through I_{sq} controller. That is by varying the I_{sq}^{*}, it is possible to draw power from the grid at different power factor.

The real time variation in line current I_{sa} with respect to change in I_{sq}^{*} is shown in figure 4.44(a), where I_{sq}^{*} is increased from zero to $2pu$ and then decreased to zero and again decreased to $-2pu$. The zoomed version of the marked portion shown in the figure 4.44(a) is shown in figure 4.44(b).

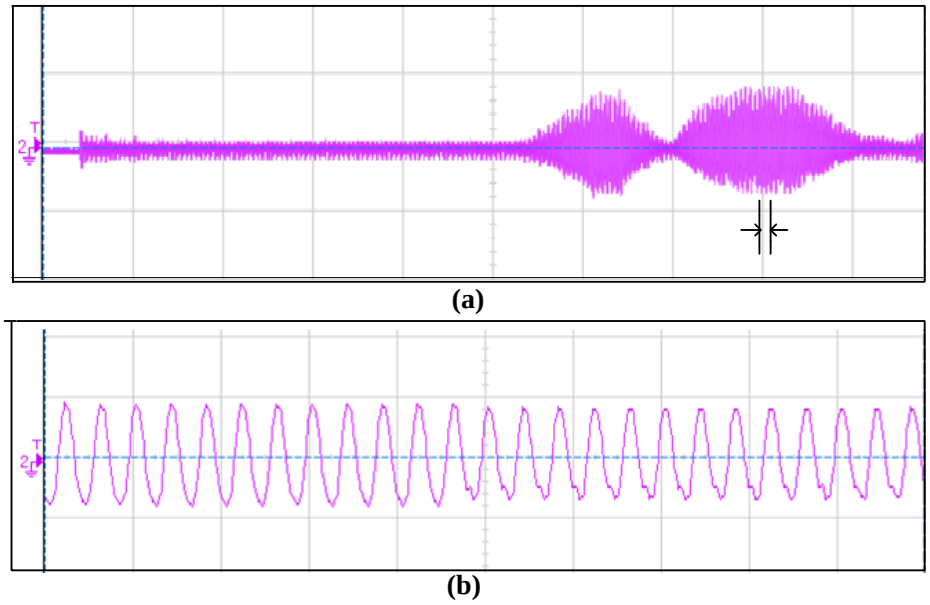


Fig. 4.44 *Hardware result*: Variation in I_{sa} with respect to change in I^*_{sq} (a)-*Scale: X-axis: 5 s/div, Y-axis: 20 A/div* (b)-*Scale: X-axis: 0.05 s/div, Y-axis: 20 A/div*

The real time variation in the current I_{sq} with respect to change in I^*_{sq} is shown in figure 4.45, where I^*_{sq} is increased from zero to $2pu$ and then decreased to zero and again decreased to $-2pu$.

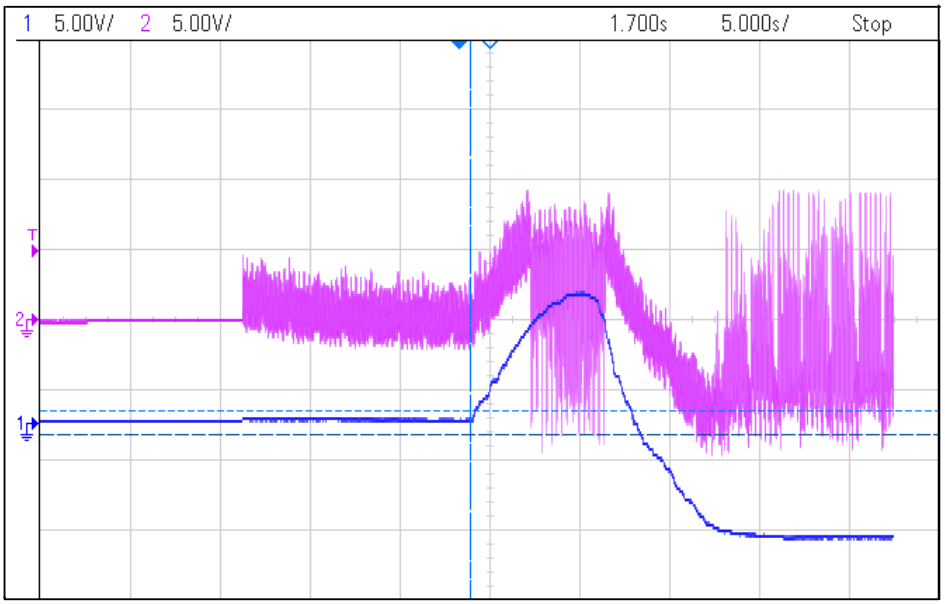


Fig. 4.45 *Hardware result*: Variation in I_{sq} (violet) with respect to change in I^*_{sq} (blue)-*Scale: X-axis: 5 s/div, Y-axis: 1 pu/div or 12.5 A/div*

The line current I_{sa} and phase voltage V_{sa} at $I_{sq}^{*} = 2pu$ is shown in figure 4.46. Here the grid delivers power at leading power factor.

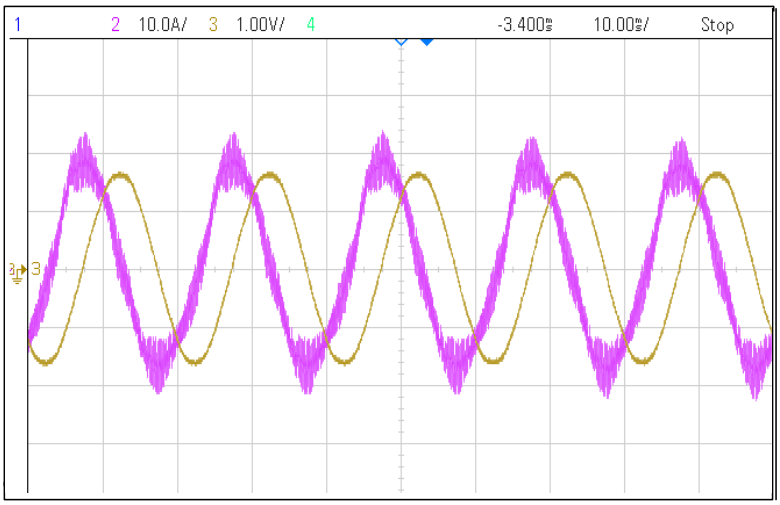


Fig. 4.46 *Hardware result*: Line current I_{sa}(violet -*Scale: X-axis: 0.01 s/div, Y-axis: 1 pu/div or 12.5 A/div*) and phase voltage V_{sa} (blue -*Scale: X-axis: 0.01 s/div, Y-axis: 0.4 pu/div or 320 V/div*) of a 3-phase 3-wire FEC at $I_{sq}^{*} = 2pu$

The line current I_{sa} and phase voltage V_{sa} at $I_{sq}^{*} = -2pu$ is shown in figure 4.47. Here the grid delivers power at lagging power factor.

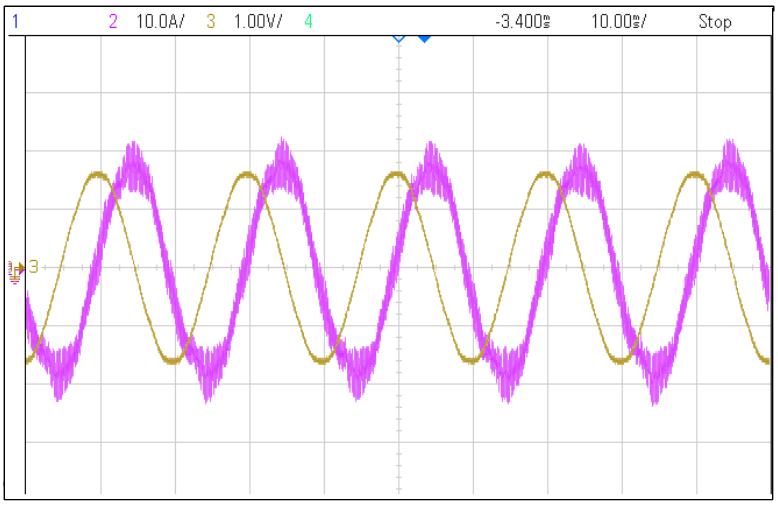


Fig. 4.47 *Hardware result*: Line current I_{sa}(violet -*Scale: X-axis: 0.01 s/div, Y-axis: 1 pu/div or 12.5 A/div*) and phase voltage V_{sa} (blue -*Scale: X-axis: 0.01 s/div, Y-axis: 0.4 pu/div or 320 V/div*) of a 3-phase 3-wire FEC at $I_{sq}^{*} = -2pu$

4.3.3 3-phase 4-wire FEC results

The relevant wave forms of the 3-phase 4-wire FEC are presented in this section.

The charging of DC bus from the initial pre-charged value (through diode bridge rectifier) to the voltage reference value (800V) is shown in figure 4.48. It takes $300ms$ to build up the voltage from the initial pre-charged value (through diode bridge rectifier) to the voltage reference value (800V), which is same as that of 3-phase 3-wire FEC.

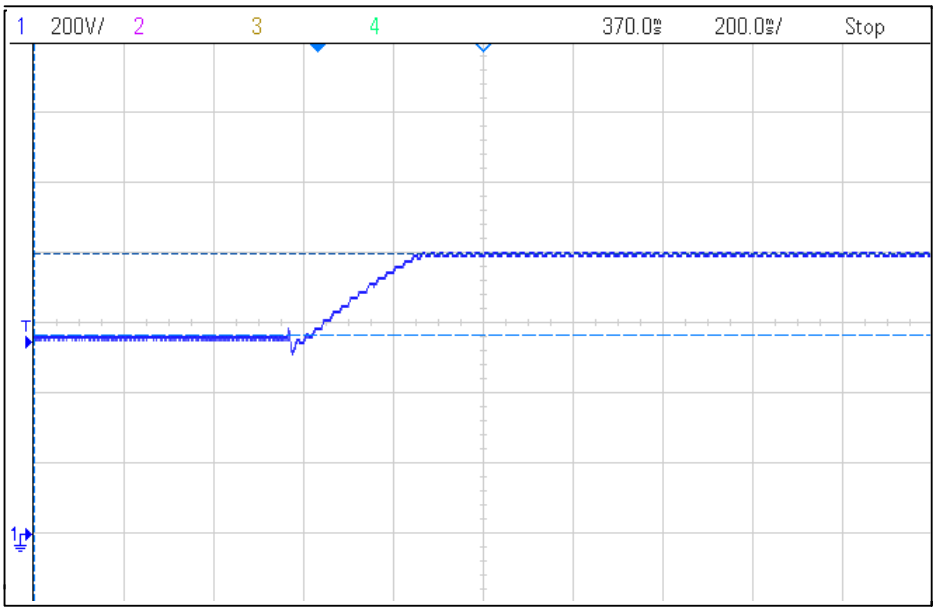


Fig. 4.48 *Hardware result*: DC bus voltage rising from the initial pre-charged value to 800V *(Scale: X-axis: 0.2 s/div, Y-axis: 200 V/div)*

The current through the neutral wire of a 3-phase diode bridge rectifier with resistance as load is shown in figure 4.49. A third harmonic common mode current is flowing through the neutral wire as shown in figure 4.49.

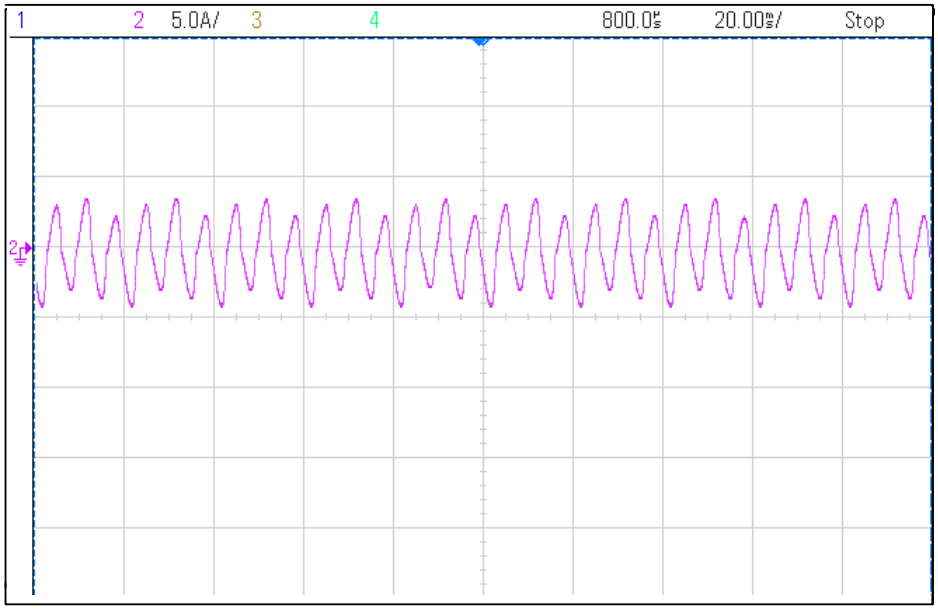


Fig. 4.49 *Hardware result*: Current through the neutral wire of a 3-phase diode bridge rectifier *(Scale: X-axis: 0.02 s/div, Y-axis: 5 A/div)*

The neutral current with SPWM modulation technique, without the neutral current controller is shown in figure 4.50. The neutral current without neutral current controller contains lower order harmonic common mode current and switching ripple current as shown in figure 4.50.

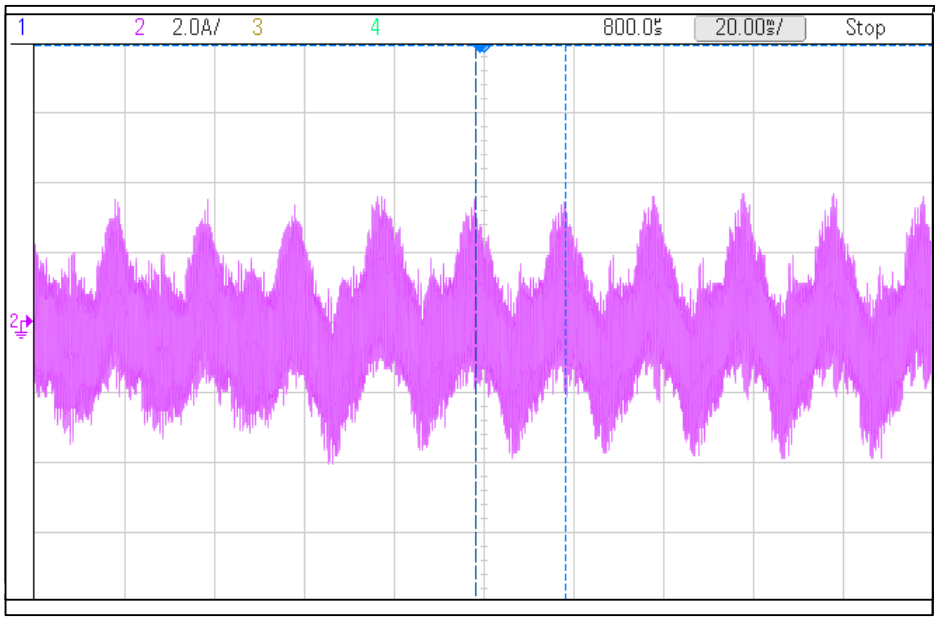


Fig. 4.50 *Hardware result*: Current through the neutral wire of a 3-phase 4-wire FEC without the neutral current controller using SPWM technique *(Scale: X-axis: 0.02 s/div, Y-axis: 2 A/div)*

The lower order harmonic common mode current shown in figure 4.50 can be eliminated using neutral current controller as shown in figure 4.51. The neutral current in a 3-phase 4-wire FEC with the neutral current controller contains only the switching ripple common mode current as observed in figure 4.51.

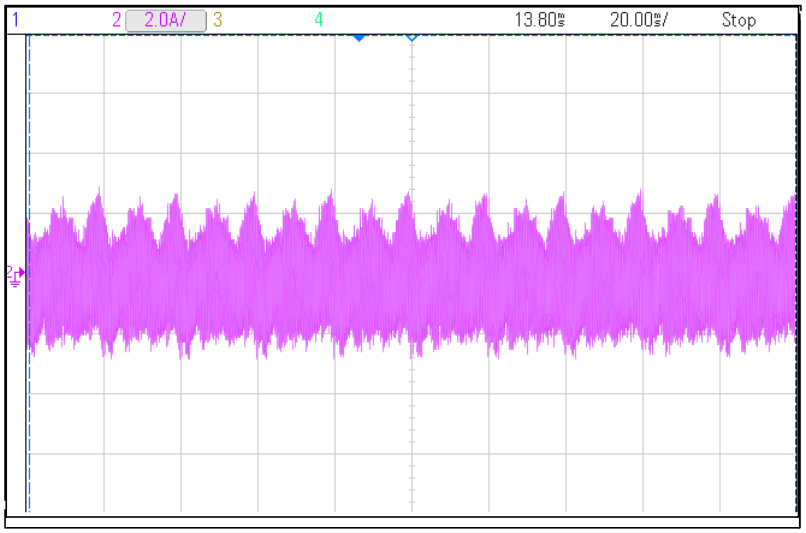


Fig. 4.51 *Hardware result*: Current through the neutral wire of a 3-phase 4-wire FEC with the neutral current controller using SPWM technique *(Scale: X-axis: 0.02 s/div, Y-axis: 2 A/div)*

As explained before two modulation schemes SPWM and SVPWM are tried with 3-phase 4-wire FEC, but SVPWM modulation technique is not suitable for the 3-phase 4-wire FEC as it will inject third order harmonic current through the neutral wire. Though an attempt to study the effect of SVPWM technique on a 3-phase 4-wire FEC has been carried out. In this project the half of middle value of modulating waves at any instant is added to the original 3-phase modulating signals to generate reference signals equivalent to SVPWM. But for the experimental purpose on 3-phase 4-wire FEC, only a fraction of the half of middle value of modulating waves at any instant is added to the original 3-phase modulating signals to generate reference signals equivalent to SVPWM. This is because of the practical limitation on current carrying capacity of the devices, as the SVPWM will cause a huge common mode current.

The SVPWM modulation scheme with two different fraction values (0.01 and 0.1) are experimented on 3-phase 4-wire FEC, where fraction is the multiplication factor (V_{mid}) with the half of middle value of modulating waves.

The neutral current with $V_{mid} = 0.01$, without the neutral current controller is

shown in figure 4.52. But the presence of third harmonic current in the neutral wire is not that much pronounced (as shown in figure 4.52) as the value of V_{mid} value is too low.

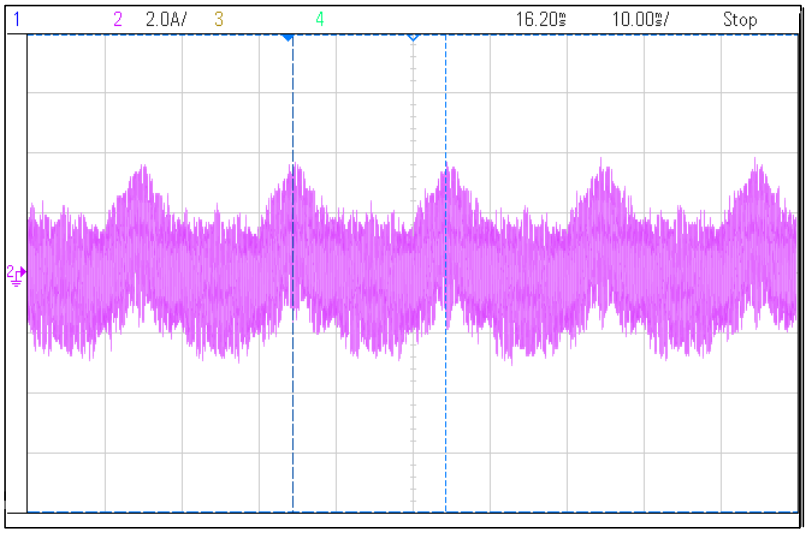


Fig. 4.52 *Hardware result*: Current through the neutral wire of a 3-phase 4-wire FEC without the neutral current controller using SVPWM technique ($V_{mid} = 0.01$) *(Scale: X-axis: 0.01 s/div, Y-axis: 2 A/div)*

The neutral current with $V_{mid} = 0.01$, with the neutral current controller is shown in figure 4.53. Lower order harmonics are eliminated from neutral current as shown in figure 4.53.

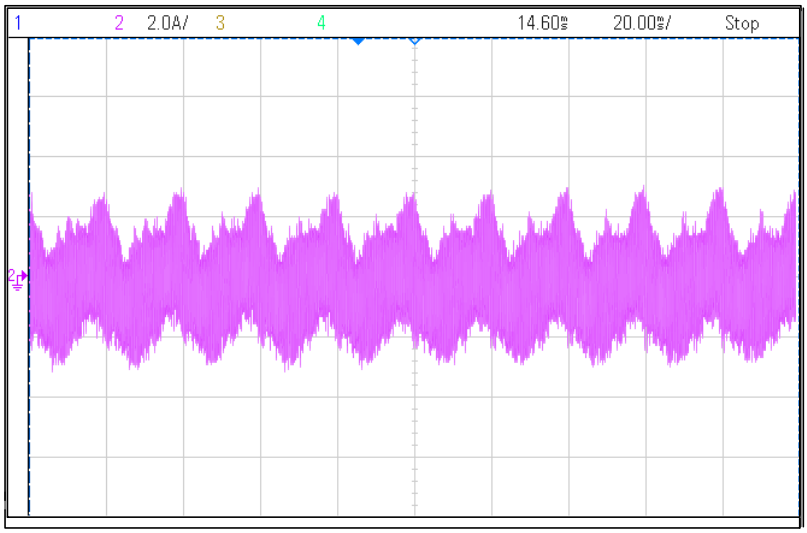


Fig. 4.53 *Hardware result*: Current through the neutral wire of a 3-phase 4-wire FEC with the neutral current controller using SVPWM technique ($V_{mid} = 0.01$) *(Scale: X-axis: 0.01 s/div, Y-axis: 2 A/div)*

The neutral current with $V_{mid} = 0.1$, without the neutral current controller is

shown in figure 4.54. In the case of $V_{mid} = 0.1$, the presence of third harmonic current in the neutral wire is much pronounced than in the case of $V_{mid} = 0.01$ as shown in figure 4.54.

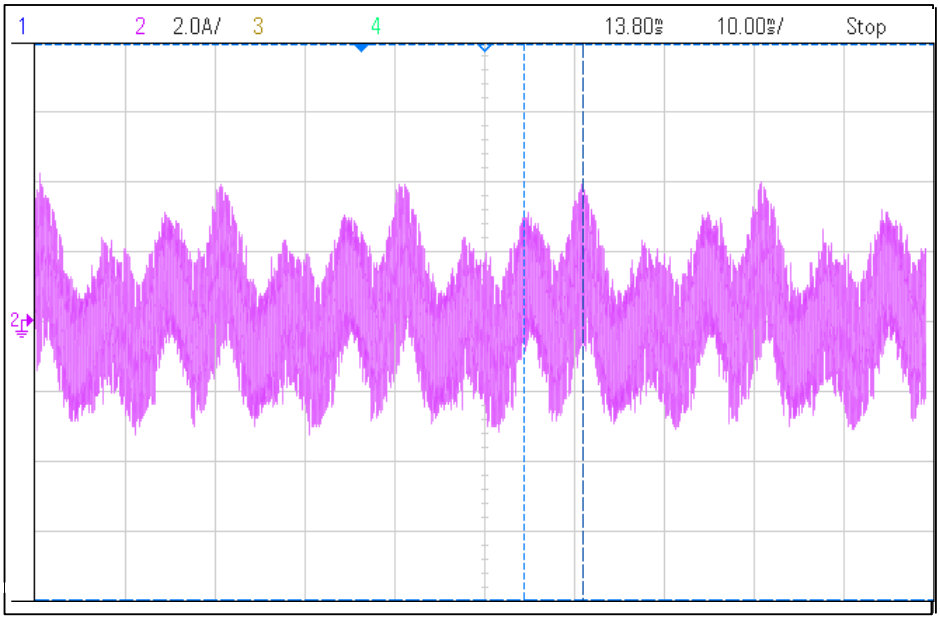


Fig. 4.54 *Hardware result*: Current through the neutral wire of a 3-phase 4-wire FEC without the neutral current controller using SVPWM technique ($V_{mid} = 0.1$) *(Scale: X-axis: 0.01 s/div, Y-axis: 2 A/div)*

The neutral current with $V_{mid} = 0.1$, with the neutral current controller is shown in figure 4.55. In figure 4.55, the neutral current PI controller does not able to eliminate the third harmonic common mode current and switching ripple common mode current from the neutral wire, even though it is able to eliminate other lower order harmonics components of the common mode current. This is because PI controller can't make steady state error into zero for high frequency signals.

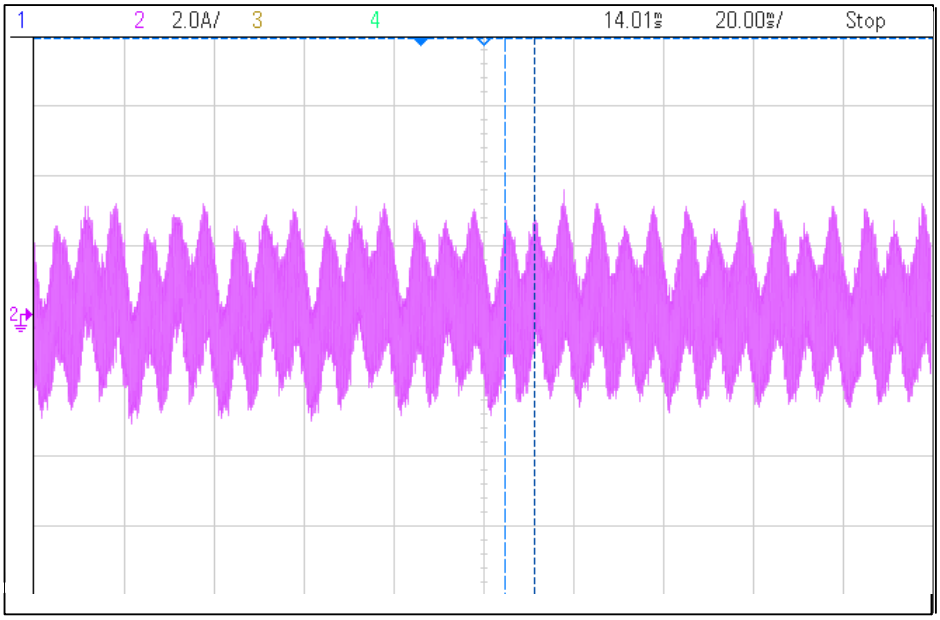


Fig. 4.55 *Hardware result*: Current through the neutral wire of a 3-phase 4-wire FEC with the neutral current controller using SVPWM technique ($V_{mid} = 0.1$) *(Scale: X-axis: 0.02 s/div, Y-axis: 2 A/div)*

4.4 Conclusion

The results from the simulation and experimental of a 10kVA 3-phase 3-wire and 3-phase 4-wire FEC were presented in this chapter. The experimental results are in close agreement with the simulated waveforms, thus validating the control design. The simulation results of elimination of lower order harmonic component from the line current of FEC were also discussed. The suitability of the TMS320F28335 DSC for high performance front end converter applications is also established.

CHAPTER 5

CONCLUSION

5.1 Summary of the Present Work

The vector control for 3-phase 3-wire and 3-phase 4-wire FEC was successfully implemented on a 10 kVA laboratory prototype. The use of DSP board, which is developed in the lab based on TMS320F28335 DSP facilitated and accelerated the implementation, where all the signal conditioning circuitry and the core are in the same board. Vector control of grid connected FEC in synchronous reference frame has been implemented, and objectives of the control like operation at desired power factor, sinusoidal line current, DC bus voltage regulation were tested. PLL was also implemented and tested to get the position information about the grid voltage space vector. In the case of 3-phase 4-wire FEC additional techniques from the 3-phase 3-wire are implemented, in order to eliminate neutral current and the switching frequency distortions from the neutral line. The soft start-up, that is starting of FEC with low starting current is very critical in the implementation of FEC. Soft start-up of FEC has been achieved using various theoretical methods and appropriate hardware implementation. The results obtained from the hardware are also found to be in close with the simulation results .Algorithm for elimination of lower order harmonics from the line current of FEC is implemented only in the simulation.

5.2 Future Scope of Work

There remains a good scope of extending this project, important one is the testing the FEC in the reverse power flow direction. That is DC power from the solar array can be converted to the AC power, and then feed to the grid. The present FEC can also be used as one of the converter in the back-to-back system. The implemented

converter can also be used as a replacement for a diode bridge rectifier for a induction motor drive. In this way the regulation capability of the drive can be ensured with superior input current quality. In this project the implemented PLL can't track the variation in the grid frequency, so there is a scope for modifying the PLL structure with an ability to track the variation in the grid frequency. The vector control for FEC can be done in stationary frame as well, where the PI controllers can't be used. So by doing vector control in stationary frame, results of two types of vector control (stationary reference frame, synchronous reference frame) can be analyzed and choose the best one depending upon the applications. Also there is a possibility of experimenting different PWM techniques in order to eliminate the switching frequency distortions in the case of a 3-phase 4-wire FEC without any other additional hardware set-up.

REFERENCES

[1] W. Leonhard, *Control of Electrical Drives*, ser. Engineering online library. Springer Berlin Heidelberg, 2001. [Online]. Available: https://books.google.co.in/books?id=pdsF210k5ikC

[2] S. Chattopadhyay and V. Ramanarayanan, "A voltage-sensorless control method to balance the input currents of a three-wire boost rectifier under unbalanced input voltages condition," *Industrial Electronics, IEEE Transactions on*, vol. 52, no. 2, pp. 386–398, April 2005.

[3] T. Noguchi, H. Tomiki, S. Kondo, and I. Takahashi, "Direct power control of pwm converter without power-source voltage sensors," *Industry Applications, IEEE Transactions on*, vol. 34, no. 3, pp. 473–479, May 1998.

[4] M. Dai, M. Marwali, J.-W. Jung, and A. Keyhani, "A pwm rectifier control technique for three-phase double conversion ups under unbalanced load," in *Applied Power Electronics Conference and Exposition, 2005. APEC 2005. Twentieth Annual IEEE*, vol. 1, March 2005, pp. 548–552 Vol. 1.

[5] Y.-K. Lo and C.-L. Chen, "Three-phase four wire voltage controlled ac line conditioner with unity input power factor and minimised output voltage harmonics," *Electric Power Applications, IEE Proceedings* -, vol. 142, no. 1, pp. 43–49, Jan 1995.

[6] M. Fraser, C. Manning, and B. Wells, "Transformerless four-wire pwm rectifier and its application in ac-dc-ac converters," *Electric Power Applications, IEE Proceedings* -, vol. 142, no. 6, pp. 410–416, Nov 1995.

[7] V.T.Ranganathan, "Course notes on electric drives," IIsc Bangalore, 2004.

[8] J. Siva Prasad, T. Bhavsar, R. Ghosh, and G. Narayanan, "Vector control of three-phase ac/dc front-end converter," *Sadhana*, vol. 33, no. 5, pp. 591–613, 2008. [Online]. Available: http://dx.doi.org/10.1007/s12046-008-0045-y

[9] S. Chung, "Phase-locked loop for grid-connected three-phase power conversion systems," *Electric Power Applications, IEE Proceedings* -, vol. 147, no. 3, pp. 213–219, May 2000.

[10] P. S. Varma and G. Narayanan, "Space vector pwm as a modified form of sine-triangle pwm for simple analog or digital implementation," *IETE Journal of Research*, vol. 52, no. 6, pp. 435–449, 2006. [Online]. Available: http://dx.doi.org/10.1080/03772063.2006.11416484

[11] S. Madhusoodhanan, S. Bhattacharya, and K. Hatua, "A unified control scheme for harmonic elimination in the front end converter of a 13.8 kv, 100 kva transformerless intelligent power substation grid tied with lcl filter," in *Applied Power Electronics Conference and Exposition (APEC), 2014 Twenty-Ninth Annual IEEE*, March 2014, pp. 964–971.

[12] M. Fraser, C. Manning, and B. Wells, "Transformerless four-wire pwm rectifier and its application in ac-dc-ac converters," *Electric Power Applications, IEE Proceedings* -, vol. 142, no. 6, pp. 410–416, Nov 1995.

[13] J. Tracy and H.-E. Pfitzer, "Achieving high efficiency in a double conversion transformerless ups," in *Industrial Electronics Society, 2005. IECON 2005. 31st Annual Conference of IEEE*, Nov 2005, pp. 4 pp.–.

[14] R. Ghosh, "Modeling, analysis and control of single-phase and three-phase pwm rectifiers," Ph.D Thesis,IIsc Bangalore, 2004.

[15] R. Zhang, F. Lee, and D. Boroyevich, "Four-legged three-phase pfc rectifier with fault tolerant capability," in *Power Electronics Specialists Conference, 2000. PESC 00. 2000 IEEE 31st Annual*, vol. 1, 2000, pp. 359–364 vol.1.

[16] A. Wijenayake, T. Gilmore, R. Lukaszewski, D. Anderson, and G. Waltersdorf, "Modeling and analysis of shared/common dc bus operation of ac drives. i," in *Industry Applications Conference, 1997. Thirty-Second IAS Annual Meeting, IAS '97., Conference Record of the 1997 IEEE*, vol. 1, Oct 1997, pp. 599–604 vol.1.

[17] R. Srinivasan and R. Oruganti, "Analysis and design of power factor correction using half bridge boost topology," in *Applied Power Electronics Conference and Exposition, 1997. APEC '97 Conference Proceedings 1997., Twelfth Annual*, vol. 1, Feb 1997, pp. 489–499 vol.1.

[18] J. Boys and A. Green, "Current-forced single-phase reversible rectifier," *Electric Power Applications, IEE Proceedings B*, vol. 136, no. 5, pp. 205–211, Sep 1989.

[19] C. Quinn, N. Mohan, and H. Mehta, "A four-wire, current-controlled converter provides harmonic neutralization in three-phase, four-wire systems," in *Applied Power Electronics Conference and Exposition, 1993. APEC '93. Conference Proceedings 1993., Eighth Annual*, Mar 1993, pp. 841–846.

[20] H.-L. Jou, J.-C. Wu, K.-D. Wu, W.-J. Chiang, and Y.-H. Chen, "Analysis of zig-zag transformer applying in the three-phase four-wire distribution power system," *Power Delivery, IEEE Transactions on*, vol. 20, no. 2, pp. 1168–1173, April 2005.

[21] TI, "Texas instruments reference guide for pwm module , literature number:sprug04a," Oct 2008.

[22] ——, "Texas instruments reference guide for adc module, literature number:spru812a," Oct 2007.

[23] ——, "Texas instruments reference guide for system control and interrupts, literature number:sprufb0d," Oct 2007.

[24] F. Sargos and S. I. GmbHCo.KG, "Appliction note: Igbt power electronics teaching system," AN-8005, Sep 2008.