VARIABLE FREQUENCY DRIVE WITH POWER FACTOR CORRECTION

A Project Report

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THESIS CERTIFICATE

This is to certify that the thesis titled **LATEX VARIABLE FREQUENCY DRIVE WITH POWER FACTOR CORRECTION**, submitted by **AVULA CHINNI VENKATA RAMANA REDDY**, to the Indian Institute of Technology, Madras, for the award of the degree of **MASTER OF TECHNOLOGY**, is a bona fide record of the research work done by him under our supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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ABSTRACT

KEYWORDS: Variable Frequency Drive; Power Factor Correction; Average Current Control; TMS320F28335

A Variable Frequency Drive (VFD) is a power electronic converter used to control motor speed and torque by varying motor input frequency and voltage. When fans or pumps are driven by a fixed-speed motor, the control of air or liquid flow is normally achieved by conventional mechanical methods, such as throttling control, inlet dampers, and flow control valves, resulting in a substantial amount of energy loss. The fluid flow could be controlled directly by running the motor at different speeds using the VFD. Over the last four decades, Power electronics technology has reduced VFD cost, size and improved performance through advances in semiconductor switching devices. The installation of the VFD in these applications could lead to a significant savings on energy and cost.

The main component of VFD is an inverter which converts DC voltage to AC voltage of desired frequency. Conventional VFD uses a diode bridge rectifier to obtain the DC voltage required by the inverter. However, the bridge rectifier configuration draws a non-sinusoidal peak current and hence, the input power factor will be low and Total Harmonic Distortion of the current will be high. To improve the power quality, Power factor correction (PFC) is required. In medium to high power off-line applications, PFC has become a mandatory feature in order to comply with regulatory standards.

In this report, the design procedure for a 3-Phase Variable Frequency Drive (VFD) with bridge rectifier is presented. A 2 kW prototype was developed and the experimental results are presented. The need for Power Factor Correction in Variable Frequency Drive is explained. Analysis of Dual Boost Bridge-less PFC Converter is presented. Using small signal analysis, the Dual Boost Bridge-less PFC Converter is modelled and the transfer functions of the converter required for designing the controller are derived. The design of a 500 W Dual Boost Bridge-less PFC Converter with average current mode control is presented. A laboratory prototype was developed and the experimental results are presented.

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ABBREVIATIONS

PFC	Power Factor Correction
BPFC	Bridge-less Power Factor Correction
EMI	Electro Magnetic Interference
CM	Common Mode
RMS	Root Mean Square
VFD	Variable Frequency Drive
IPM	Intelligent Power Module
IGBT	Insulated Gate Bipolar Transistor

NOTATION

ω_L	Frequency of Input AC voltage, rad/s
v_g	Input AC voltage, V
i_g	Input AC current, A
L	Boost Inductor , H
C	Capacitor , F
P_{avg}	Average Power, W
P_0	Output Power, W
P_{in}	Input Power, W
V_{rms}	RMS value of AC voltage, V
I_{rms}	RMS value of AC current, A
V_{nom}	Nominal RMS Input Voltage, V

CHAPTER 1

Introduction

1.1 Introduction

A Variable Frequency Drive (VFD) is a power electronic converter used to control motor speed and torque by varying motor input frequency and voltage. When fans or pumps are driven by a fixed-speed motor, the control of air or liquid flow is normally achieved by conventional mechanical methods, such as throttling control, inlet dampers, and flow control valves, resulting in a substantial amount of energy loss [1]. The fluid flow could be controlled directly by running the motor at different speeds using the VFD. Over the last four decades, Power electronics technology has reduced VFD cost, size and improved performance through advances in semiconductor switching devices. The installation of the VFD in these applications could lead to a significant savings on energy and cost.

Unlike conventional mechanical methods of flow control, by using VFD, the efficiency of the overall system is increased due to the fact that the motor only sees the necessary amount of input power to achieve desirable output power. In addition, the motor can be slowly brought up to speed, eliminating huge inrush current. The DC voltage required by the VFD could be obtained easily by rectifying the AC voltage using diode bridge rectifier and a bulk capacitor. However, the bridge rectifier configuration draws a discontinuous non-sinusoidal peak current and hence, the input power factor will be low and Total Harmonic Distortion(THD) of the current will be high [4].

The concept of power factor is a measure of how well the power from the utility grid is utilized. Its value lies in the range 0 to 1 and it is computed as the ratio of the real power to the apparent power.

$$P.F. = \frac{RealPower}{ApparentPower} \tag{1.1}$$

Real power is measured in watts and is the power required to do real work. Assuming that the line voltage is a perfect sinusoidal, the real power (P_{Real}) is defined as

the product of the fundamental of the voltage (V_{RMS}), the fundamental of the current ($I_{RMS,fund.}$) and the cosine of the phase displacement $\cos(\phi)$ between these two fundamentals.

$$P_{Real} = V_{RMS}.I_{RMS,fund.}.\cos(\phi) \tag{1.2}$$

Apparent power ($P_{App.}$), measured in volt-amps, is defined as the product of the RMS voltage ((V_{RMS})) and RMS current ((I_{RMS})):

$$P_{App.} = V_{RMS}.I_{RMS} \tag{1.3}$$

From Eqn. 1.1, Eqn. 1.2 and Eqn. 1.3, the power factor can be expressed as:

$$PF = \frac{I_{RMS,fund.}}{I_{RMS}}.\cos(\phi) \tag{1.4}$$

The ratio $\frac{I_{RMS,fund.}}{I_{RMS}}$ is called the distortion factor and is denoted by K_d. The cosine of the phase displacement between these two fundamentals, $\cos(\phi)$ is called the displacement factor and is denoted by K_ϕ. So, the power factor can be expressed as:

$$PF = K_d.K_\phi \tag{1.5}$$

A measure of harmonic content in a circuit is total harmonic distortion (THD). It is defined as the square root of the ratio of the sum of all of the squared higher-order harmonics to the amplitude of the fundamental harmonic.

$$THD = \frac{\sqrt{(I^2_{RMS,2}) + (I^2_{RMS,3}) + ... + (I^2_{RMS,N})}}{I_{RMS,fund.}} \tag{1.6}$$

The power electronic converters are required to comply with harmonic current emission standards such as IEC61000-3-2 [17]. IEC61000-3-2 is a mandatory standard, which defines the limitations on harmonic currents that can be injected into the mains supply by these converters. Several Power Factor Correction (PFC) techniques are reported in literature to improve the power factor of AC-DC converters and to keep the harmonic content within the limitations imposed by the standard.

PFC techniques can either be passive or active. Passive techniques use passive elements such as inductors and capacitors as a filter that passes current only at line frequency. Active PFC is the use of power electronics to shape the current drawn from the source.

The active PFC methods have many advantages over the passive PFC techniques such as high power factor, reduced harmonics, smaller size and weight. However, the complexity and relatively higher cost are the main drawbacks of active PFC. Several types of Active PFC techniques are proposed in literature. The PFC controllers will have slower voltage response and a voltage ripple at twice the line frequency. Depending on whether bridge rectifier is used or not, the PFC topologies can be classified into two categories: Bridge PFC Topologies and Bridge-less PFC topologies. Having a bridge rectifier increases the conduction losses. So, the bridge-less topologies are expected to give much better efficiency compared to bridge PFC topologies. Today, the PFC converters are followed by another stage of isolated DC/DC converter, to have an isolation and to have a tight output voltage regulation [3],[**?**] as shown in Fig. 1.1.The major disadvantages of this approach of cascading are the reduction of the overall efficiency, the large component count and the increasing control complexity. A brief overview of few Bridge-less PFC Topologies and their comparison is presented in the subsequent section.

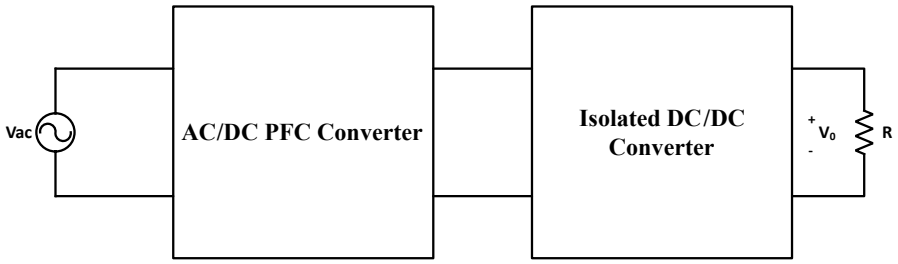
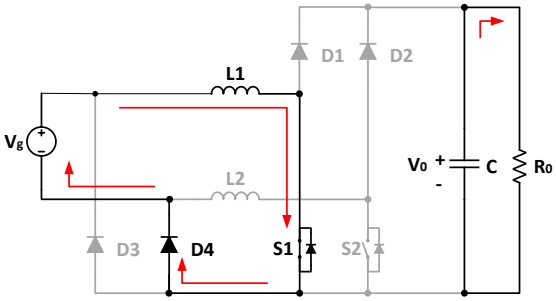


Figure 1.1: Today's widely used single-phase AC/DC-converter system consisting of a front-end PFC boost rectifier stage and a subsequent isolated DC/DC-converter

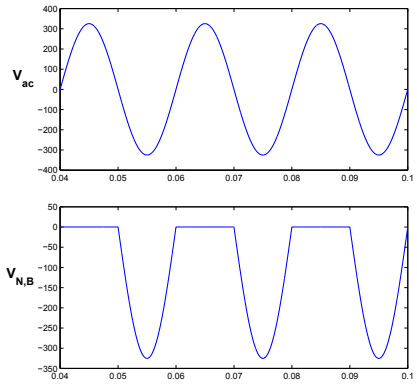
1.2 Overview of Bridge-less PFC Topologies

Traditional single-phase PFCs usually have full-wave rectifiers in the input side, which contribute to a large part of the semiconductor losses [4]. Recently, a new PFC family named Bridge-less PFCs (BPFCs) has been proposed to achieve higher efficiency by removing the front end diode bridge rectifier. The comparison of several BPFC topologies with respect to loss evaluation, efficiency, power semiconductor devices count and Electro Magnetic Interference(EMI) are reported in literature [5]-[14].

Comparing to the Conventional Boost PFC (Fig. 1.2a), BPFC concept improves effi-



(a) Conventional Boost PFC



(b) Potential difference between AC neutral and DC negative lines

Figure 1.2: Conventional Boost PFC Topology

ciency of the converter by removing the bridge rectification system in front of it. With the increasing demands on energy saving in recent years, the implementation of BPFC systems have became more and more attractive. A brief description of principle of operation of few popular BPFC topologies with their pros and cons are presented in the preceding sections.

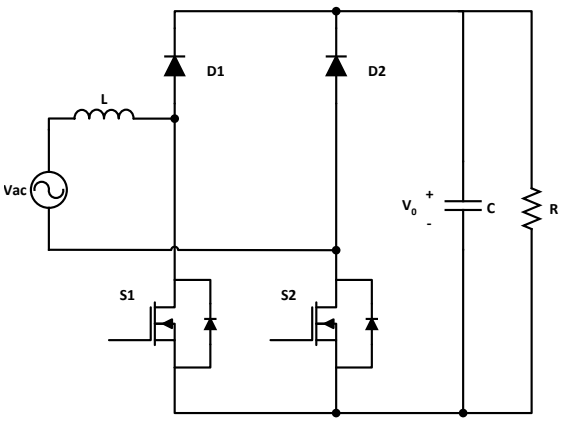
1.2.1 Basic BPFC topology

The basic BPFC topology is shown in Fig. 1.3a. Compared to the conventional Boost PFC (Fig. 1.2a), the important advantage of this topology is that, it doesn't need four line frequency diodes operating as voltage rectifier.

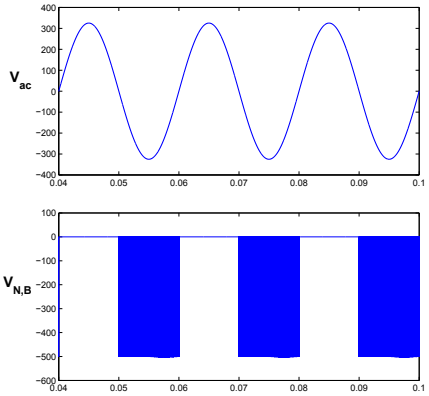
Operating principle: The basic BPFC works symmetrically for both positive and negative input voltages. In the positive AC line period, when S1 is on, the boost inductor L is charged by S1 and the body diode of S2. When S1 is off, the inductor is discharged through Boost diode D1 and the body diode of S2.In the negative AC line period, the inductor L is charged by S2 and the body diode of S1 when S2 is on. when S2 is off, the Boost inductor is discharged through Boost diode D2 and the body diode of S1.

Pros: Compared to the conventional Boost PFC, the basic BPFC has one less line frequency diode in current owing path, which reduces the semiconductor losses and enhance the system efficiency.

Cons: Compared to the conventional Boost PFC, the output ground of basic BPFC has



(a) Basic PFC



(b) Potential difference between AC neutral and DC negative lines

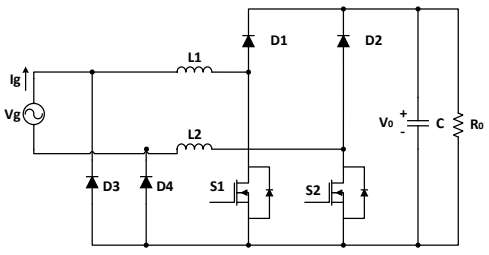
Figure 1.3: Basic PFC Topology

high frequency voltage pulses in the negative AC line period due to which, it doesn't connect to the positive terminal of AC source directly (Fig. 1.3b). These voltage pulses can induce high CM EMI noises which may affect system stability.

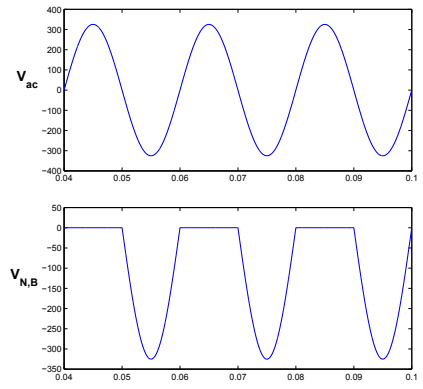
1.2.2 Dual Boost BPFC topology

The Dual Boost BPFC shown in Fig. 1.4a is an EMI improved version of basic BPFC. The Dual Boost BPFC converter employs two complete boost converters, one for each of the AC input voltage cycles.

Operating principle: Similar to the Basic BPFC topology(Fig. 1.3a), the Dual Boost



(a) Dual Boost BPFC Topology



(b) Potential difference between AC neutral and DC negative lines

Figure 1.4: Dual Boost BPFC Converter

BPFC works symmetrically. So, only half of the AC line period is considered here. For example, in the positive AC line period, when S1 is on, the boost inductor L1 is charged by S1 and line frequency diode D4. When S1 is off, the boost inductor L1 is discharged through boost diode D1 and the line frequency diode D4.

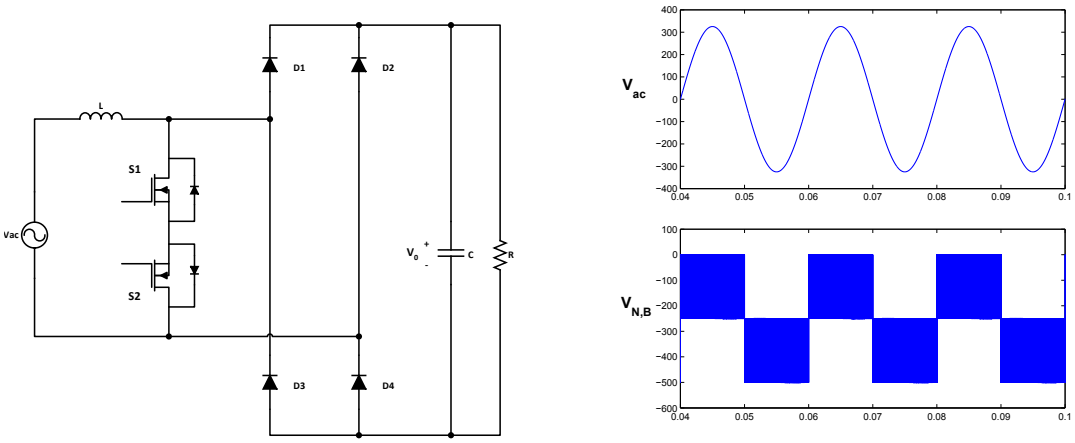
Pros: By implementing two line frequency diodes D3 and D4, the output ground is connected to the terminals of AC mains directly in the whole AC line period, which stabilizes voltage potential of output ground and reduces CM EMI generation (Fig. 1.4b). In additional, instead of using the relatively high forward voltage mosfet's body diodes as a part of the current owing path, using normal line frequency diodes D3 and D4 helps to improve system efficiency.

Cons: Due to the two extra line frequency diodes D3 and D4 and the one extra Boost inductor, this topology has higher cost and volume than the basic BPFC.

1.2.3 BPFC with Bidirectional Switch topology

Fig. 1.5a is an modification of Two-Boost-Circuit BPFC (Fig. 1.4a) by disconnecting the sources of mosfets S1 and S2 from output ground.

Operating principle: This topology works symmetrically for both positive and nega-



(a) BPFC with Bidirectional switch

(b) Potential difference between AC neutral and DC negative lines

Figure 1.5: BPFC with Bidirectional switch Topology

tive input voltages because of bidirectional switch. So, only half of the AC line period is considered here. For example, in the positive AC line period, when S1 is on, the boost inductor L is charged by S1 and the body diode of S2. When S1 is off, the boost

inductor L is discharged through boost diode D1 and D4.

Pros: By having only one boost inductor, this topology has lower cost and volume than the Dual Boost BPFC in Fig. 1.4a.

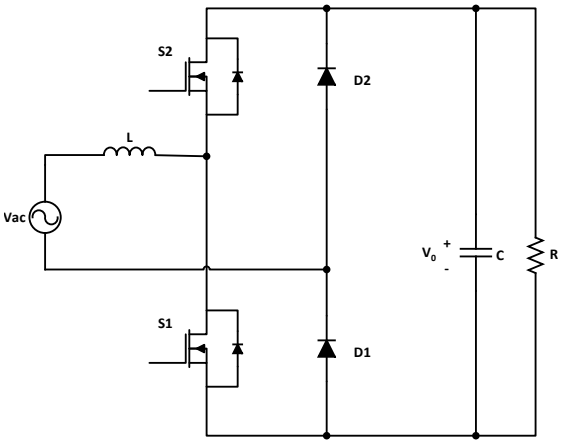
Cons: In this topology, all the diodes are fast recovery diodes. However, in Fig. 1.4a, only D1 and D2 are fast recovery diodes, D3 and D4 are line frequency diodes because each of them conducts in half of the AC line period. Therefore, the conduction losses of this topology can be expected to be higher than the Dual Boost BPFC.

Furthermore, compared to the Dual Boost BPFC, the output ground of this topology has high frequency voltage pulses in the whole AC line period (Fig. 1.5b). These voltage pulses will induce high CM EMI noises and bring difficulties to EMI filter design. Besides, the BPFC in Fig.2.4(a) requires a complex control and drive circuit, due to the sources of mosfets do not connect to the output ground.

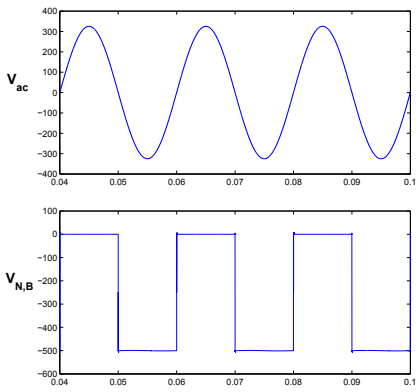
1.2.4 Totem-pole BPFC topology

Fig. 1.6a is a modification of Basic BPFC (Fig. 1.3a). by exchanging the position of Boost diode D1 and mosfet S2.

Operating principle: As the Totem-pole BPFC works symmetrically, only half of the



(a) Totem-pole BPFC



(b) Potential difference between AC neutral and DC negative lines

Figure 1.6: Totem-pole BPFC Topology

AC line period is considered here. For example, during the positive AC period, when S1 is on, diode D1 conducts and the Boost inductor is charged. When S1 is off, the Boost inductor is discharged through body diode of S2 and diode D1.

Pros: As the output ground is directly connected to the terminal of AC source by D1

in the positive line period and the terminal of Boost inductor by the body diode of S1 in the negative line period, the CM EMI generation problem from basic BPFC can be solved.

Cons:The reverse-recovery performance of the body diodes of the mosfets makes continuous current mode (CCM) operation of this BPFC (Fig. 1.6a) difficult. Furthermore, compared to the basic BPFC, although they have the same semiconductor numbers in the current owing path, in the Totem-pole BPFC, each mosfet's body diode conducts in the switching frequency. Additionally, the Totem-pole BPFC requires a complex control and drive circuit, due to the source of MOS S2 doesn't connect to ground.

1.2.5 Summary

Compared to other topologies, the Dual Boost BPFC could be used for operating in a high power level with good efficiency, relatively lower EMI and less complex control and gate drive systems. In publication [15], a 1 kW universal line Dual Boost BPFC with the maximum measured efficiency reaching 97% is presented.

1.3 Organization of the Report

This report is organized as follows.

Chapter 1 : This chapter begins with the introduction of Variable Frequency Drive and its application in flow control systems. The need for Power Factor Correction in Variable Frequency Drive is explained. An overview of topologies belonging to a class of PFC converters called Bridge-less PFC converters is presented.

Chapter 2 : Design and Implementation of a 3 phase Variable Frequency Drive is presented. A 2 KW hardware prototype is built and tested. The experimental results showing the load performance and efficiency are presented.

Chapter 3 : Analysis of Dual Boost Bridge-less PFC Converter is presented. A 500 W Dual Boost BPFC Converter is designed and simulated in MATLAB/SIMULINK. A hardware prototype is built and tested. The performance evaluation of the developed prototype along with the VFD driving a single phase induction motor is presented.

Chapter 5 : This chapter presents the conclusions of the report.

CHAPTER 2

Design and Implementation of a 2 KW Variable Frequency Drive

2.1 Introduction

A Variable Frequency Drive is a power electronic component used to control the torque and speed of AC motors by controlling the frequency and magnitude of the voltage applied to the motor. A VFD consists of a diode bridge rectifier which converts AC voltage to DC voltage and a 3 phase Inverter which converts DC voltage to AC voltage. Using PWM technique, the magnitude and frequency of VFD output voltage can be precisely controlled. The PWM gating pulses controlling the VFD are generated by a

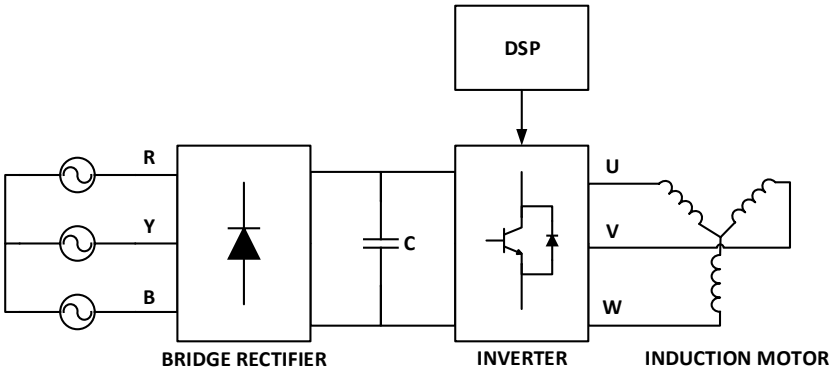


Figure 2.1: Block diagram of the Variable Frequency Drive

Micro Controller. The DC voltage required by the inverter can be obtained by rectifying 3-phase AC voltage using diode bridge rectifier. The ripples in the DC output of the rectifier can be removed by using a capacitor which acts as a low pass filter. The block diagram of a 3-Phase Variable Frequency Drive is shown in Fig. 2.1.In this chapter, the design procedure for a 3-Phase Variable Frequency Drive (VFD) is discussed and a 2 KW laboratory prototype has been evaluated.

2.2 Design and Implementation

The design of the 3-Phase Variable Frequency Drive can be broken down into two stages: The AC-DC rectifier design and the DC-AC inverter design. Each of these two stages of design are discussed in detail in the subsequent sections. The design parameters of the 2 KW Variable Frequency Drive are given in Table. 2.1.

Table 2.1: Design input specifications of a 2 KW Variable Frequency Drive

Parameter	**Specification**
Nominal line-line Input Voltage, $V_{in,rms}$	415 V
Output Voltage line frequency , $f_{out,L}$	0 - 60 Hz
Switching frequency , f_s	10 kHz
Output Power, P_0	2000 W
DC Bus Voltage ripple, ΔV_{dc}	3%

2.2.1 Rectifier Design

The DC voltage required by the 3 phase Inverter is obtained by rectifying 3-phase AC supply using diode bridge rectifier. The rectified voltage is converted to DC voltage using a Capacitor, which acts as a low-pass filter. The voltage on the DC bus capacitor will have a ripple at 6 times the line frequency. For a 415 V line-line 3 phase AC supply, the peak input voltage applied to the bridge rectifier will be

$$V_m = V_{line-line}.\sqrt{2} = 586.81V \tag{2.1}$$

Neglecting the voltage drop across the diodes the average DC voltage across the DC bus capacitor will be close to V_m. The magnitude of the ripple on the DC bus voltage is decided by the DC bus capacitor value. The minimum value of the DC bus capacitor required can be determined by imposing the maximum output voltage ripple limit. Taking 3% ripple in DC bus voltage, the variation in the DC bus voltage will be between V_m and $0.97V_m$. Therefore, the charging time (t_c) and discharging time (t_c) of the capacitor are given by

$$t_c = \frac{90^0 - \sin^{-1}(0.97)}{\omega_L} = 0.78ms \tag{2.2}$$

$$t_d = \frac{2.\pi}{6.\omega_L} - t_c = 2.55ms \tag{2.3}$$

During charging time, the sum of output load current and capacitor charging current is supplied by the input AC source through the diode bridge and during the discharge time, the output load current is supplied by the capacitor. For a constant power load of P_0, the minimum capacitor required for 3% voltage ripple is given by the energy balance on the capacitor as

$$P_0.t_d = \frac{1}{2}.C.(V_0^2 - (V_0 - \Delta V_0)^2) \tag{2.4}$$

$$C_{min} = \frac{2.P_0.t_d}{(V_0^2 - (V_0 - \Delta V_0)^2)} = 503\mu F \tag{2.5}$$

In order to have a safety margin, the value of C chosen was 680 μH. For this value of capacitance, using iterative method, it is found that

$$\Delta V_0 = 13.478 = 2.3\% \tag{2.6}$$

$$t_c = 0.684ms \tag{2.7}$$

$$t_d = 2.646ms \tag{2.8}$$

Assuming that the capacitor discharges linearly, the peak capacitor charging current can be obtained by imposing the charge balance on the capacitor.

$$\frac{1}{2}.I_{c,peak}.t_c = \frac{P_0}{V_0}.t_d + \frac{1}{2}.t_d.(\frac{P_0}{V_0} - \frac{P_0}{(V_0 - \Delta V_0)}) = 0.00892 \tag{2.9}$$

$$I_{c,peak} = \frac{(2).(0.00892)}{t_c} = 26.09A \tag{2.10}$$

The rms current through capacitor during its charging interval is given by

$$I_{c,rms,1} = I_{c,peak}.\sqrt{\frac{t_c}{3.(t_c + t_d)}} = 7.72A \tag{2.11}$$

The rms current through capacitor during its discharging interval is given by

$$I_{c,rms,2} = \sqrt{(\frac{P_0}{V_0}.\sqrt{\frac{t_c}{(t_c+t_d)}})^2 + (\frac{P_0}{V_0} - \frac{P_0}{(V_0-\Delta V_0)}.\sqrt{\frac{t_c}{3(t_c+t_d)}})^2} = 2.939A \tag{2.12}$$

From Eqn. 2.11 and Eqn. 2.12, the rms current through capacitor over one ripple cycle is given by

$$I_{c,rms} = \sqrt{I_{c,rms,1}^2 + I_{c,rms,2}^2} = 8.26A \tag{2.13}$$

The peak current drawn from the bridge rectifier is given by

$$I_{peak,rect} = \frac{P_0}{V_0} + I_{c,peak} = 3.41 + 26.09 = 29.50A \tag{2.14}$$

The average current drawn from the bridge rectifier is given by

$$I_{avg,rect} = \frac{P_0}{V_0} = 3.41A \tag{2.15}$$

The diode bridge rectifier *VS-36MT120 from VISHAY SEMICONDUCTOR*, having blocking voltage rating of 1200 V and continuous forward current of 35 A is selected. From the data sheet of VS-36MT120 [20], for an output current of 3.41 A, maximum total power loss is found to be

$$P_{loss} \approx 10W \tag{2.16}$$

Maximum junction to case thermal resistance,

$$R_{\theta jc} = 1.35K/W \tag{2.17}$$

Maximum case to heat sink thermal resistance,

$$R_{\theta cs} = 0.2K/W \tag{2.18}$$

Maximum allowable junction temperature for the output current of 3.41 A,

$$T_{jmax} = 140^0C = 413K \tag{2.19}$$

Maximum ambient temperature,

$$T_{amax} = 50^0 C = 323K \tag{2.20}$$

So, Maximum heat sink to ambient thermal resistance is given by

$$R_{\theta sa} = \frac{T_{jmax} - T_{amax}}{P_{loss}} - R_{\theta jc} - R_{\theta cs} = 7.45K/W \tag{2.21}$$

During start-up, the capacitor bank takes a huge inrush current. To limit the inrush current, a parallel configuration of relay and resistor network is connected in series to the capacitor. So, at start-up, when the relay is off, the capacitor charges slowly depending on the RC time constant. Once the capacitor is charged fully, the relay turns on, bypassing the resistor. Limiting the peak inrush current to 4 A, the pre charge resistor is given by The peak inrush current during start-up is limited by the equation

$$R_{pre-charge} = \frac{V_{peak}}{I_{inrush}} = 150\Omega \tag{2.22}$$

The time taken by the capacitor to charge upto 99% is given by

$$t_{charge} = 4.R_{pre-charge}.C = 400ms \tag{2.23}$$

So, the relay has to be turned on 400 ms after the power up.

2.2.2 Inverter Design

A 3 phase inverter comprises of three half bridge inverters with each leg able to produce AC voltage having 120^0 phase displacement with respect to each other using sinusoidal pulse width modulation(SPWM) technique. In SPWM, a high frequency triangular carrier signal is compared with a sinusoidal modulating signal that represents the desired fundamental component of the pole voltage waveform. The comparator output is then used to control the high side and low side switches of the particular pole. From the figure, the high duration of the pulses (t_h), during which the pole voltage magnitude is V_{dc}, can be found to be

$$t_h = \frac{T_c}{2}.(1 + \frac{v_m}{\hat{v_c}}) \tag{2.24}$$

where T_c is the time period of the triangular carrier waveform, v_m is the magnitude of the modulating signal and $\hat{v_c}$ is the peak magnitude of the carrier signal. Similarly the low duration of the pulses (t_l), during which the pole voltage magnitude is $-V_{dc}$, can be found to be

$$t_l = \frac{T_c}{2}.(1 - \frac{v_m}{\hat{v_c}}) \tag{2.25}$$

From Eqn. 2.24 and Eqn. 2.25, the DC component of the pole voltage (V_{AO}), in a switching interval T_c can be found to be

$$V_{AO,T_c} = 0.5.V_{dc}.\frac{V_m}{\hat{V_c}} \tag{2.26}$$

For the SPWM technique, as the modulating signal is a sine wave, v_m can be written as

$$v_m = \hat{v_m}.\sin(\omega t) \tag{2.27}$$

where 'ω' is the angular frequency of the modulating waveform. The ratio of the peak magnitudes of modulating wave ($\hat{v_m}$) and the carrier wave ($\hat{V_c}$) is defined as modulation-index (m), given by

$$m = \frac{\hat{v_m}}{\hat{V_c}} \tag{2.28}$$

So, the fundamental component of the Phase-A pole voltage V_{AO} is

$$V_{AO,1} = \frac{m.V_{dc}}{2}.\sin(\omega.t) \tag{2.29}$$

For m=1, the pole output voltage (fundamental component) will have a maximum rms value given by

$$V_{AO,1,rms,max} = \frac{V_{dc}}{2.\sqrt{2}} = 207.18V \tag{2.30}$$

Assuming the load current i_A consists of only fundamental (I_1) and third harmonic component (I_3), we have

$$I_{A,rms} = \sqrt{I_1^2 + I_3^2} \tag{2.31}$$

Since,

$$I_1 = \frac{P_0}{3.V_{AO,1,rms}} = 3.217A \tag{2.32}$$

Further, assuming $I_3 = 0.7I_1$ (which is typical of a single phase rectifier type nonlinear load) we have,

$$I_{A,rms} = 1.22.I_1 = (1.22).(3.217) = 3.924A \tag{2.33}$$

$$I_{A,peak} = \sqrt{2}.(1.22).(3.217) = 5.549A \tag{2.34}$$

The current rating of the IGBTs should be more than 5.549 A.

High power density can be achieved in a 3 phase inverter by using "Intelligent Power Module (IPM)". An IPM is a compact package containing 6 IGBT Switches along with free-wheeling diodes arranged in three phase bridge configuration with built-in protection and gate driver circuitry. For the 2 KW prototype, *"6MBP10VAA120-50 by Fuji Electric"* IPM was selected. The ratings of the IGBT are 1200 V and 10 A. [18]

From the Fuji IGBT simulator of 6MBP10VAA120-50 [19], for an rms output current of 3.924 A in each phase, maximum total power loss is found to be

$$P_{loss} \approx 10W \tag{2.35}$$

Maximum junction to case thermal resistance of each IGBT,

$$R_{\theta jcQ} = 1.28K/W \tag{2.36}$$

Maximum junction to case thermal resistance of each free wheeling diode,

$$R_{\theta jcD} = 2.02K/W \tag{2.37}$$

Typical case to heat sink thermal resistance,

$$R_{\theta cs} = 0.05K/W \tag{2.38}$$

Maximum allowable junction temperature for the output current of 3.924 A,

$$T_{jmax} = 110^0C = 383K \tag{2.39}$$

Maximum ambient temperature,

$$T_{amax} = 50^0C = 323K \tag{2.40}$$

The effective junction to case thermal resistance is given by

$$R_{\theta jc} = \frac{R_{\theta jcQ}}{6} // \frac{R_{\theta jcD}}{6} = 0.2134//0.3367 = 0.1306K/W \tag{2.41}$$

So, Maximum heat sink to ambient thermal resistance is given by

$$R_{\theta sa} = \frac{T_{jmax} - T_{amax}}{P_{loss}} - R_{\theta jc} - R_{\theta cs} = 4.8194K/W \tag{2.42}$$

To validate the design, a 2 KW prototype is built and tested. The hardware implementation of the 2 KW prototype is discussed in the next section.

2.2.3 Hardware Implementation

A 2 KW VFD prototype is developed to validate the design discussed in previous section. A Printed Circuit Board was designed and fabricated. The developed prototype is shown in Fig.2.2. The hardware implementation of the prototype is presented below.

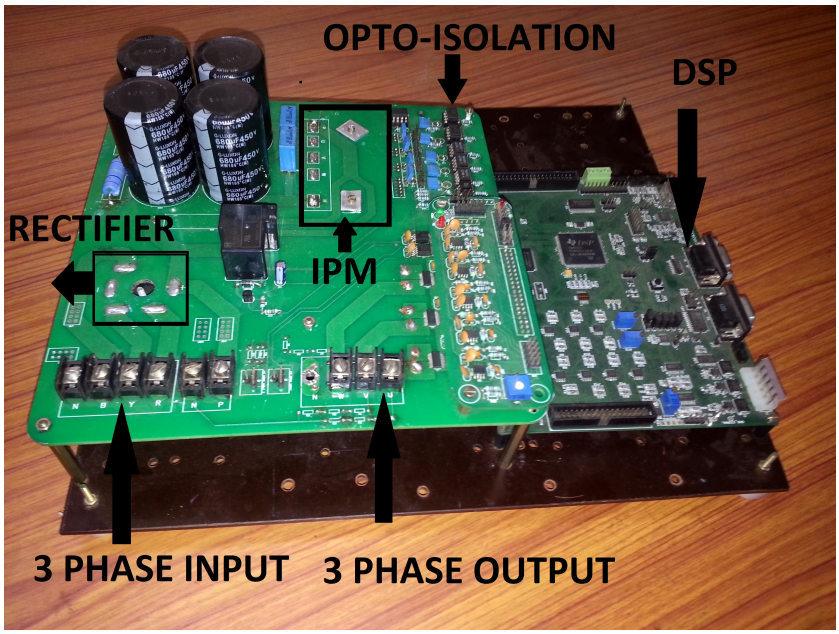


Figure 2.2: 2 KW Laboratory prototype of VFD controlled with TMS320F28335 DSP

Intelligent Power Module: For the 2 KW prototype, the selected 6MBP10VAA120-50 IPM from Fuji Electric is shown in Fig. 2.3. The selected IPM contain 6 IGBT Switches along with free-wheeling diodes arranged in three phase bridge configuration with integrated IGBT gate driver circuitry. For the gate driver of IPM, four isolated 15 V DC power supplies, one for the three lower arm side switches and three for the upper arm side switches (one for each leg upper arm switch) are required. In addition,

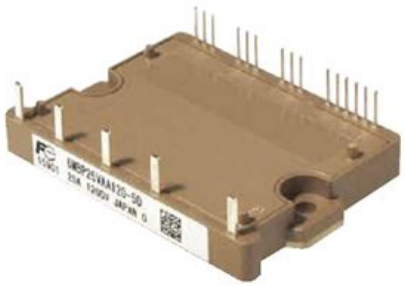


Figure 2.3: 6MBP10VAA120-50 IPM from Fuji Electric

the IPM features integrated fault detection mechanism for IGBT collector over current fault, IGBT junction over temperature fault and gate driver supply under voltage fault. In case of fault, the IPM shuts down the IGBTs and indicates the fault through an alarm pin[18]. After indicating the fault through the alarm pin, the IPM will restart automatically after a specified blank time. The blank time for various fault conditions are listed in Table. 2.2.

Table 2.2: IPM blank time for various fault conditions[18]

Fault condition	**IPM blank time**
IGBT collector over current fault	2 ms
IGBT Gate driver under voltage fault	4 ms
IGBT junction over temperature fault	8 ms

Digital Controller: The PWM switching pulses for controlling the inverter output voltage are generated using *"TMS320F28335 DSP from Texas Instruments"*. The DSP is programmed to generate 6 PWM pulsed for the six IGBTs of inverter module. A switching frequency of 10 kHz is selected based on the IGBT rating. If the gating pulses of the top and bottom switches of a leg overlap, the DC source will be shorted through the leg. To avoid this, a dead time of $3\mu s$ is introduced for the PWM pulses of top and bottom switches of each leg.

Protection: The DSP generates gating pulses for all switches with respect to a common digital ground. Using high speed opto-couplers, the PWM pulses are isolated from DSP and gate pulse is generated with respect to the emitter of each IGBT. In addition, the fault alarm signal from the IPM is isolated from digital ground through an opto-coupler.

As listed in the Table. 2.2, when a fault occurs, the IPM will automatically restart after the specified blank time. In case of a short circuit fault, if the external short circuit is not cleared within the blank time, the automatic restart feature of IPM will activate the IPM and will draw huge current. To protect the device in such scenario, the fault signal has to be latched and the PWM gating signals has to be shut down by DSP. This is achieved using the *Trip Zone(TZ)* feature of the TMS320F28335 DSP.

When the TZ pin of the DSP is set to low, the PWM module of TMS320F28335 DSP will shut down the PWM pulse immediately, independent to the CPU operation. The DSP is programmed to start PWM pulses by a push button, once the fault is cleared. When the layout is designed poorly, the fault alarm signal from IPM can catch noise and a false-trip can happen. The false-trip can be avoided by using *Action Qualifier* feature of DSP.

The Action Qualifier module of TMS320F28335 DSP will monitor the TZ pin for a specified time and acknowledges a change only if the state of the pin is constant during the monitoring period. Using the Trip-Zone and Action Qualifier features of the TMS320F28335 DSP the IPM can be used reliably and the device can be protected even if fault happens.

2.3 Experimental Results

The developed prototype shown in Fig.2.2 is tested with resistive load and motor load. The steady state results obtained are presented below.

2.3.1 VFD with resistive load

The developed 2 KW prototype is tested with resistive load and the results obtained are listed below.

- With 3 phase 404 V line-to-line voltage as input, Fig. 2.4 shows the input line current drawn by the diode bridge rectifier and line-to-line input voltage at 2.5 KW. It was observed that a peak current of 17 A was drawn with RMS current 5.7 A.

- Fig. 2.5 shows the line-line voltage waveforms of two pairs of legs of the inverter at no load condition with a switching frequency of 10 kHz.

- The prototype is loaded from 8% to 112% of rated power using resistors with a 3 phase AC input. The Table 2.3 shows the input power factor and efficiency of the VFD, for the variation of resistive load from 8% to 125% of rated load at 50 Hz line frequency.

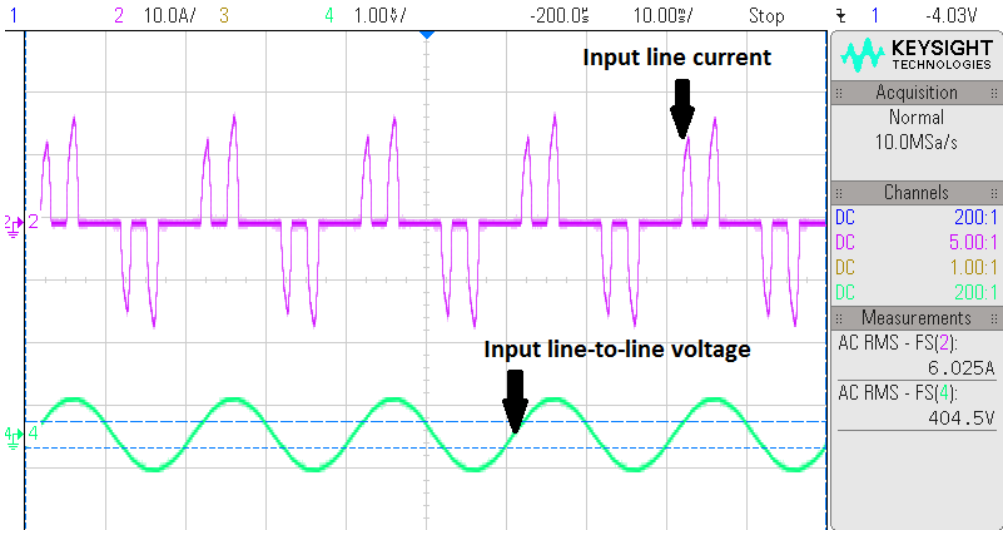


Figure 2.4: Input line current connected to diode bridge rectifier at full load

Table 2.3: Input power factor and Efficiency of VFD for different resistive loads at 50 Hz

% of load	Input Power(W)	Input Power factor	Output Power(W)	Efficiency
8.3	180.20	0.4808	166.00	92.12
14.55	306.30	0.4977	291.00	95.00
28	576.10	0.5433	560.00	97.21
45.55	928.40	0.5496	911.00	98.13
82.40	1674.10	0.6212	1648.00	98.44
98.7	2004.80	0.6416	1974.00	98.46
112.1	2272.40	0.6494	2242.00	98.66
126.4	2565.30	0.6598	2528.00	98.55

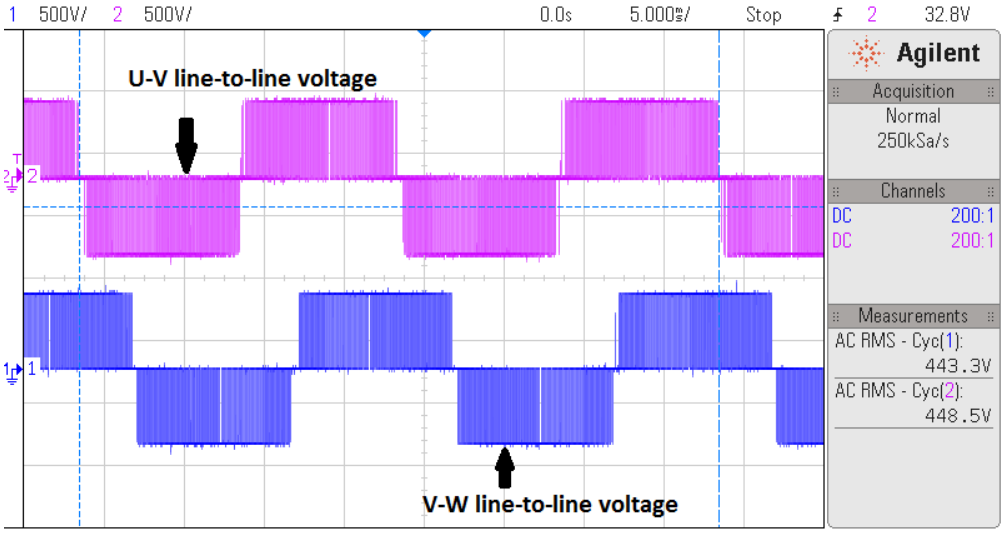


Figure 2.5: Output line-to-line voltages of the inverter

2.3.2 VFD with Induction motor

The developed 2 kW prototype is tested with a 1.5 kW rated 3 phase induction motor coupled to an air blower. The results obtained are listed below.

- Fig. 2.6 shows the pole-to-pole voltage and line current waveforms of the inverter driving a 1.5 kW rated 3 phase induction motor coupled to an air blower. A RMS current of 3.98 A is drawn by the motor at its rated power.

- The Table 2.4 shows the comparison of air flow rate when running the motor at different frequencies. When the line frequency of VFD is decreased from 50 Hz to 40 Hz, it was observed that only 16.4% of CFM of the air flow is reduced with 40.68% reduction in the input power consumption.

Table 2.4: CFM comparison of blower run by VFD at different frequencies

$f\,(Hz)$	$P_{in}\,(W)$	*Input power factor*	$P_{out}\,(W)$	$\eta\,(\%)$	*Air flow rate(CFM)*
20	182	0.42	124	68.13	916.65
30	396	0.45	346	87.37	1752.98
40	781	0.49	761	97.44	2433.38
50	1521	0.52	1456	95.73	2910.60

2.3.3 VFD Fault Protection Tests

To test the performance of the IPM under fault conditions, the prototype is subjected to Short Circuit test and Gate driver under voltage test. The observations are listed below.

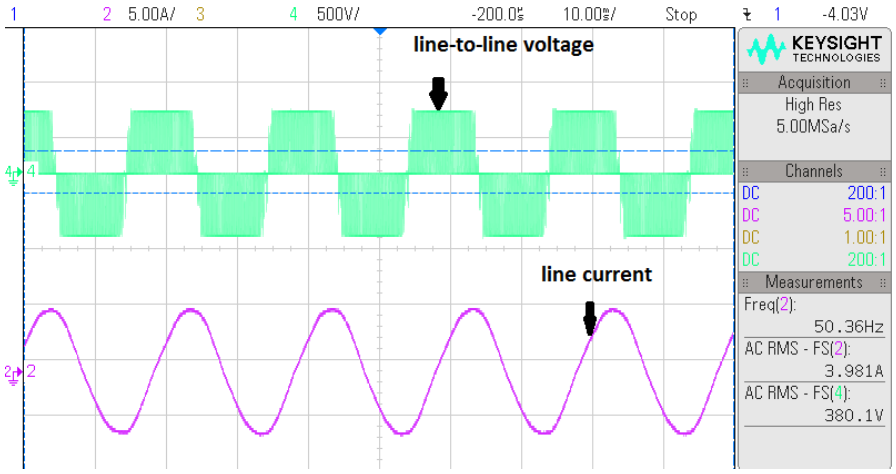


Figure 2.6: Output line current of the inverter connected to an induction motor running at full load

- Fig. 2.7 shows the IPM fault signal during short circuit fault. The IPM blank time is found to be 1.654 ms.

- Fig. 2.8 shows the IPM fault signal during gate driver under voltage fault. The IPM blank time is found to be 4 ms.

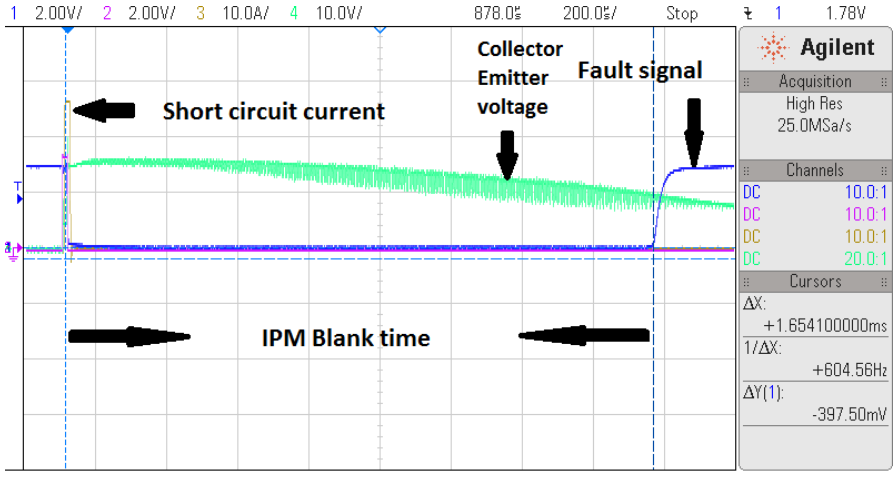


Figure 2.7: Fault signal of IPM during short circuit fault

2.4 Conclusions

The design guidelines of the variable frequency drive are presented. A 2 kW hardware prototype is designed and tested. The experimental results showing the performance

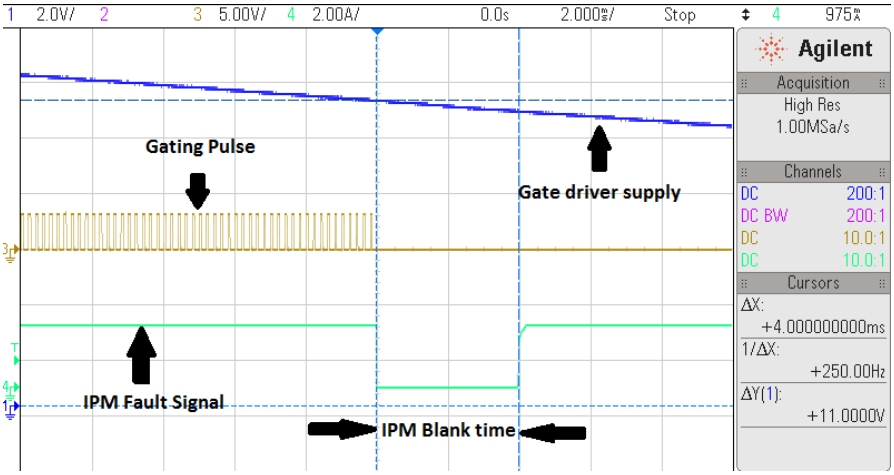


Figure 2.8: Fault signal of IPM during gate driver under voltage fault

of the developed prototype are presented. The prototype is able to achieve maximum efficiency of 98% at rated load condition. But, the input power factor of the VFD is poor, as the AC-DC conversion is done using a diode bridge rectifier. To improve the power factor, an active PFC AC-DC converter is introduced in next chapter.

CHAPTER 3

Analysis, Modelling and Design of Dual Boost BPFC Converter

3.1 Introduction

High efficiency PFC rectifiers are required in many applications that convert AC voltage from utilities into DC voltages for powering electronics in office equipment, telecommunications and consumer electronics. However, as discussed in chapter 1, the conventional PFC rectifier based on a diode bridge and a boost converter has large conduction losses. Compared to the conventional PFC converter, the dual boost PFC converter has one less diode in the current path resulting in better efficiency. The working principle and the circuit analysis of the Dual Boost BPFC Converter are discussed in the subsequent section.

3.2 Circuit Analysis

The Dual Boost BPFC has a symmetric structure. During the positive AC line, diode D1

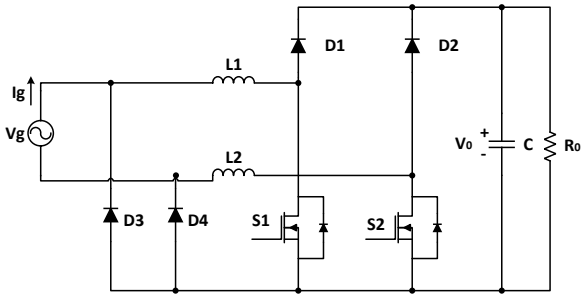
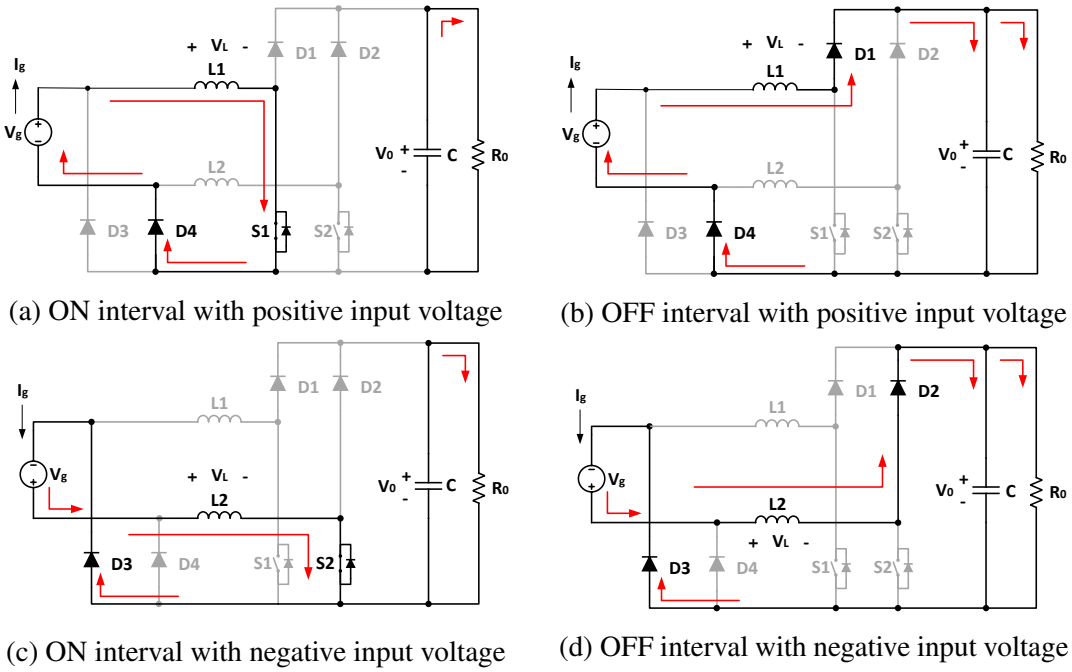


Figure 3.1: Dual Boost BPFC Converter

operates when S1 turns off, and boost inductor L1 discharges and gives energy to load. When S1 turns on, boost inductor L1 is charged, and diode D1 turns off. The output

capacitor discharges and transfers energy to load. Line frequency diode D3 returns current from output ground to neutral and stabilize its voltage potential. In the negative AC line, the BPFC works symmetrically. It could be noted that this converter (Fig. 3.1) is equal to two normal Boost PFCs, one working in positive line period and the other working in negative line period. So the circuit analysis will be same for both positive and negative input voltages. To further simplify the analysis, it is assumed that the boost inductor L and output capacitor C are very large, resulting in a constant DC current I_L and constant DC voltage V_0 with negligible ripple. As the switching frequency is far higher than the line frequency, the analysis is carried out for a switching time interval assuming a constant DC input voltage



(a) ON interval with positive input voltage

(b) OFF interval with positive input voltage

(c) ON interval with negative input voltage

(d) OFF interval with negative input voltage

Figure 3.2: Operation principle of the Dual Boost BPFC

Taking the input line frequency as ω_L, the equation for the input AC voltage, v_g can be written as

$$v_g(t) = \sqrt{2}.V_{rms}.\sin(\omega_L.t) \tag{3.1}$$

where V_{rms} is the RMS value of input AC voltage. Assuming that the PFC controller achieves nearly unity power factor, the equation for the input current i_g can be written as:

$$i_g(t) = \sqrt{2}.I_{rms}.\sin(\omega_L.t) \tag{3.2}$$

where, I_{rms} is the RMS value of input AC current. The instantaneous power drawn from the source can be written as:

$$P_{in}(t) = v_g(t).i_g(t) = V_{rms}.I_{rms}.(1 - \cos(2.\omega_L.t)) \tag{3.3}$$

Operation of the circuit during ON interval:

During this interval (Fig. 3.2a and Fig. 3.2c), the voltage and current equations of boost inductor are:

$$v_L(t) = L.\frac{di_L(t)}{dt} = v_g(t) \tag{3.4}$$

$$i_L(t) = \frac{1}{L}\int_0^t v_L(t).dt + i_L(0) \tag{3.5}$$

From Eqn. 3.4 and 3.5, we get

$$i_L(t) = \frac{v_g(t)}{L}.t + i_L(0) \tag{3.6}$$

Assuming a peak-to-peak ripple of $2\Delta I_L$ in the inductor current, the boundary conditions for the inductor current:

$$i_L(0) = I_L - \Delta I_L \tag{3.7}$$

$$i_L(T_{on}) = I_L + \Delta I_L \tag{3.8}$$

Applying these boundary conditions for equation 3.6, we get the ripple current on the boost inductor as,

$$\Delta I_L = \frac{v_g(t).T_{on}}{2.L} \tag{3.9}$$

Operation of the circuit during OFF interval:

During this interval(Fig. 3.2b and Fig. 3.2d), the voltage and current equations of boost inductor are:

$$v_L(t) = L.\frac{di_L(t)}{dt} = v_g(t) - V_0 \tag{3.10}$$

$$i_L(t) = \frac{1}{L}\int_0^t v_L(t).dt + i_L(0) \tag{3.11}$$

From Eqn. 3.10 and Eqn. 3.11, we get

$$i_L(t) = \frac{(v_g(t) - V_0)}{L}.t + i_L(0) \tag{3.12}$$

The boundary conditions for the inductor current are:

$$i_L(0) = I_L + \Delta I_L \tag{3.13}$$

$$i_L(T_{off}) = I_L - \Delta I_L \tag{3.14}$$

Applying these boundary conditions for equation 3.12, we get the ripple current on the boost inductor as

$$\Delta I_L = \frac{(V_0 - v_g(t)).T_{off}}{2.L} \tag{3.15}$$

At steady state:

The ripple currents during ON and OFF intervals must be equal at steady state. Equating Eqn. 3.9 and Eqn. 3.15 we get

$$v_g.T_{on} = (V_0 - v_g).T_{off} \tag{3.16}$$

From Eqn. 3.16, the duty cycle can be written as

$$d(t) = \frac{T_{on}}{T_{on} + T_{off}} = \frac{(V_0 - v_g(t))}{V_0} \tag{3.17}$$

The duty cycle (Eqn. 3.17) for this converter is similar to that of a boost converter and varies with input voltage. Mathematical modelling and controller design of average current-mode controlled Dual Boost BPFC converter are explained in the subsequent section.

3.3 Mathematical Modelling

The steps involved in the mathematical modelling of average current-mode controlled Dual Boost BPFC controller are explained in this section. State space averaging method is used to obtain small signal model of the converter. It is assumed that all the converter

elements are ideal. Small signal analysis is done on the basic assumption that the natural time constants of the storage elements are much longer than the switching period [4]. Assuming that the converter achieves unity power factor, the input current drawn can be written as

$$i_g(t) = \frac{v_g(t)}{R_e} \tag{3.18}$$

where, R_e is the resistance emulated by the converter, as seen by the source. The average power drawn from the source is given by

$$P_{avg} = \frac{{V_{rms}}^2}{R_e} \tag{3.19}$$

$$R_e = \frac{{V_{rms}}^2}{P_{avg}} \tag{3.20}$$

To attain input resistor emulation, several approaches are presented in literature [4] like average current mode control, input voltage feed forward control, current programmed control, hysteric control etcetera. Average Current Mode Control is the popular method of implementing control of the input current waveform in a low-harmonic rectifier because of its switching noise immunity.

The controller for Dual Boost BPFC converter requires two control loops, an inner current loop to control the input AC current and an outer voltage loop to control the output DC voltage. As the power drawn from the source (Eqn. 3.3) has an AC component at twice the line frequency, the voltage across the output capacitor will have a voltage ripple at this frequency. If the controller inner voltage loop tries to remove this ripple, it will cause the emulated resistance to change at a frequency higher than the line frequency and consequently distorts the input current shape. Thus, the outer voltage loop should have a bandwidth lesser than the input line frequency. To design the controller, we need to model the converter using small signal analysis. For the fast acting current loop, small signal analysis has to be done averaging over switching frequency and to model converter dynamics for much slower voltage loop, small signal analysis has to be done averaging over half period of input AC voltage. The reference current for the inner current loop is set by the outer voltage loop. At steady state, when the current control loop error is zero, from Eqn. 3.18 and 3.20, the reference current is given by

$$i_{ref}(t) = i_g(t) = \frac{v_g(t)}{R_e} = \frac{P_{avg}.v_g(t)}{{V_{rms}}^2} \tag{3.21}$$

From Eqn. 3.21, in addition to the input voltage, the reference current is also dependent on the RMS value of input voltage and average power. For a constant power load, the outer voltage loop can be made immune to the input voltage fluctuations by feed forwarding the rms value of input voltage. So, by feed forwarding $\frac{v_g(t)}{{V_{rms}}^2}$ as shown in Fig. 3.3, the voltage controller produces a reference $V_c(t)$ such that

$$V_c(t) = P_{avg} = V_{rms}.I_{rms} \tag{3.22}$$

From Eqn. 3.22, it is clear that the average power throughput is directly controlled by the outer voltage loop. The Dual Boost BPFC converter with average current mode controller and input voltage feed forward is shown in Fig. 3.3.

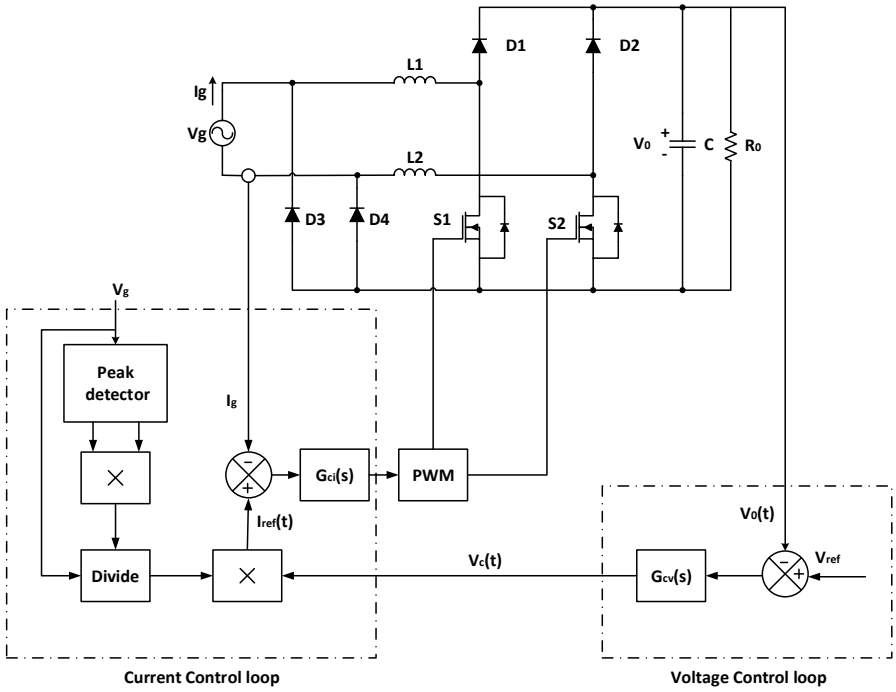


Figure 3.3: Dual Boost BPFC converter with average current mode controller

3.3.1 Current Control Loop

Block diagram of the current control loop for average current mode control of Dual Boost BPFC converter is shown in figure 3.4. The input current to duty transfer function

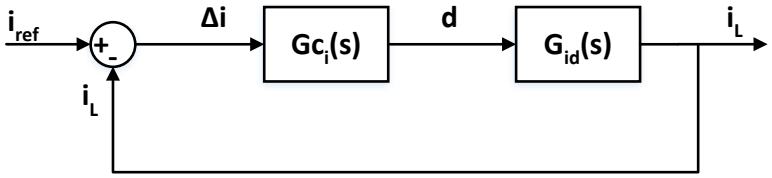


Figure 3.4: Block diagram of the current control loop

of the converter is obtained using state space averaging of the transient equations of the inductor current and capacitor voltage over a switching interval.

i. During ON interval:

$$L.\frac{di_L}{dt} = v_g \tag{3.23}$$

$$C.\frac{dv_0}{dt} = -\frac{v_0}{R_0} \tag{3.24}$$

ii. During OFF interval:

$$L.\frac{di_L}{dt} = v_g - v_0 \tag{3.25}$$

$$C.\frac{dv_0}{dt} = i_L - \frac{v_0}{R_0} \tag{3.26}$$

Averaging the equations over one switching cycle, we get

$$L.\frac{di_L}{dt} = v_g - (1-d)v_0 \tag{3.27}$$

$$C.\frac{dv_0}{dt} = (1-d)i_L - \frac{v_0}{R_0} \tag{3.28}$$

Introducing small perturbation in the state variables i_L, v_g, v_0 and d, we get

$$L.\frac{d(I_L + \hat{i}_L)}{dt} = (V_g + \hat{v}_g) - (1 - D - \hat{d})(V_0 + \hat{v}_0) \tag{3.29}$$

$$C.\frac{d(V_0 + \hat{v}_0)}{dt} = (1 - D - \hat{d}).(I_L + \hat{i}_L) - \frac{(V_0 + \hat{v}_0)}{R_0} \tag{3.30}$$

Equating AC and DC quantities and neglecting second order AC quantities, we get

$$L.\frac{d\hat{i}_L}{dt} = \hat{v}_g - (1-D).\hat{v}_0 + V_0.\hat{d} \tag{3.31}$$

$$C.\frac{d\hat{v}_0}{dt} = (1-D).\hat{i}_L - I_L.\hat{d} - \frac{\hat{v}_0}{R_0} \tag{3.32}$$

Replacing $(1-D)$ with D' and taking Laplace transform, we get

$$s.L.\hat{i}_L(s) + D'.\hat{v}_0(s) = V_0.\hat{d}(s) + \hat{v}_g(s) \tag{3.33}$$

$$D'.\hat{i}_L(s) - (s.C + \frac{1}{R_0}).\hat{v}_0(s) = I_L.\hat{d}(s) \tag{3.34}$$

A simple circuit model, as shown in Fig. 3.5 represents the small signal equations

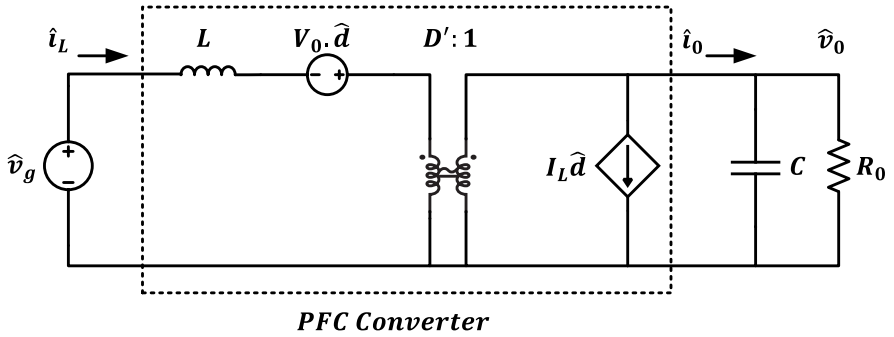


Figure 3.5: Small Signal circuit model averaged over switching cycle

Eqn. 3.33 and Eqn. 3.34. From the Fig. 3.5, the duty to input current transfer function can be written as:

$$\frac{\hat{i}_L(s)}{\hat{d}(s)} = \frac{2.V_0}{R_0.(D')^2}.\frac{1 + (\frac{R_0.C}{2}).s}{1 + (\frac{L}{R_0.(D')^2}).s + (\frac{L.C}{(D')^2}).s^2} \tag{3.35}$$

For s = j.ω, when ω is large enough, the above equation can be approximated to

$$G_{id}(s) = \frac{\hat{i}_L(s)}{\hat{d}(s)} = \frac{V_0}{L.s} \tag{3.36}$$

Taking the PI Controller transfer function as

$$Gc_i(s) = (K_{pi} + \frac{K_{ii}}{s}) \tag{3.37}$$

The closed loop gain can be written as

$$T_i(s) = Gc_i(s).G_{id}(s) = \frac{V_0}{L.s}.(K_{pi} + \frac{K_{ii}}{s}) \tag{3.38}$$

The current control closed loop transfer function can be written as

$$Gi_e(s) = \frac{T_i(s)}{1 + T_i(s)} \tag{3.39}$$

Applying the Nyquist stability criteria for $Gi_e(s)$, we get

$$|T_i(j.\omega_c)| = 1 \tag{3.40}$$

$$\angle T_i(j.\omega_c) = -180^0 + \phi_i \tag{3.41}$$

where ω_c is the gain cross over frequency and ϕ_i is the phase margin at gain cross over frequency. From Eqn. 3.38 and Eqn. 3.41, we get

$$K_{ii} = \frac{K_{pi}.\omega_c}{\tan(\phi_i)} \tag{3.42}$$

From Eqn. 3.38 and Eqn. 3.40, we get

$$|\frac{V_0}{L.(j.\omega_c)}.(K_{pi} + \frac{K_{ii}}{j.\omega_c})| = 1 \tag{3.43}$$

$$\sqrt{(\omega_c.K_{pi})^2 + K_{ii}^2} = \omega_c^2.\frac{L}{V_0} \tag{3.44}$$

Substituting Eqn. 3.42 in Eqn. 3.44, we get

$$\sqrt{(\omega_c.K_{pi})^2 + (\frac{K_{pi}.\omega_c}{\tan(\phi_i)})^2} = \omega_c^2.\frac{L}{V_0} \tag{3.45}$$

$$\frac{\omega_c.K_{pi}}{\tan(\phi_i)}.\sqrt{1 + (\tan(\phi_i))^2} = \omega_c^2.\frac{L}{V_0} \tag{3.46}$$

$$K_{pi} = \frac{L.\omega_c}{V_0}.\sin(\phi_i) \tag{3.47}$$

3.3.2 Voltage Control Loop

Block diagram of the voltage control loop of Dual Boost BPFC converter is shown in figure 3.6. To model the input current to output voltage transfer function of the

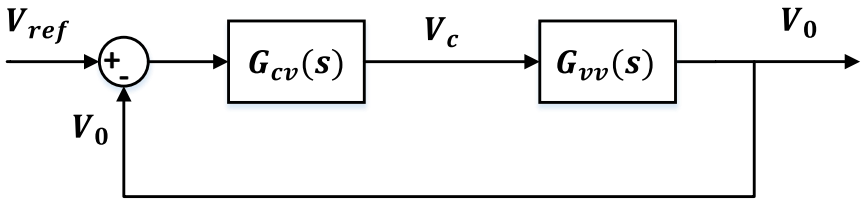


Figure 3.6: Block diagram of the voltage control loop

converter, we take the power balance equation averaged over half cycle of ac input voltage.

$$v_g.i_g = v_0.i_0 \tag{3.48}$$

where, v_g and i_g are RMS values of input voltage and current; whereas, v_0 and i_0 are averaged DC values of output voltage and current.

Introducing small perturbation in the state variables v_g, i_g, v_0 and i_0, we get

$$(V_g + \hat{v}_g).(I_g + \hat{i}_g) = (V_0 + \hat{v}_0).(I_0 + \hat{i}_0) \tag{3.49}$$

Cancelling the steady state terms and neglecting the product of perturbations, we get

$$\hat{i}_0 = \frac{V_g}{V_0}.\hat{i}_g + \frac{I_g}{V_0}.\hat{v}_g - \frac{I_0}{V_0}.\hat{v}_0 \tag{3.50}$$

From Eqn. 3.22 and Eqn. 3.50, we get

$$\hat{i}_0 = \frac{1}{V_0}.\hat{v}_c + \frac{I_g}{V_0}.\hat{v}_g - \frac{I_0}{V_0}.\hat{v}_0 \tag{3.51}$$

A simple circuit model, as shown in Fig. 3.7 represents the small signal equation 3.50 with an output load Z_0. From the small signal model Fig. 3.7, we get

$$\hat{i}_0 = \frac{\hat{v}_0}{Z_0} \tag{3.52}$$

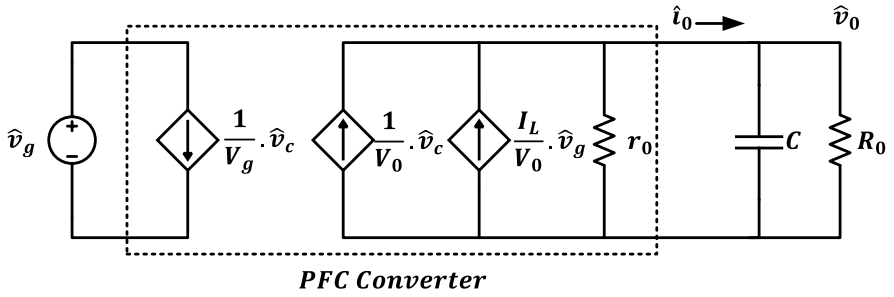


Figure 3.7: Small Signal circuit model averaged over half period of input AC voltage

where, Z_0 is the equivalent resistance of C and R_0. Taking Laplace transform and equating Eqn. 3.50 and Eqn. 3.52 , we get

$$G_{vv}(s) = \frac{\hat{v}_0(s)}{\hat{v}_c(s)} = \frac{1}{V_0}.\frac{(r_0//R_0)}{(1 + C.s.(r_0//R_0))} \tag{3.53}$$

where r_0 is the small signal resistance given by

$$r_0 = \frac{V_0}{I_0} \tag{3.54}$$

In a two stage PFC converters, the front end PFC stage is followed by a second stage of Isolated DC-DC converter for isolation and tight output voltage regulation. The current drawn by the DC-DC converter increases as the output voltage of the PFC decreases. The DC-DC converter appears like a constant power load to the front stage PFC. The impedance presented by the constant power load is negative and is given by

$$R_0 = -\frac{V_0}{I_0} \tag{3.55}$$

From Eqn. 3.53,Eqn. 3.54 and Eqn. 3.55 we get

$$G_{vv}(s) = \frac{\hat{v}_0(s)}{\hat{v}_c(s)} = \frac{1}{V_0.C.s} \tag{3.56}$$

Taking the PI Controller transfer function as

$$Gc_v(s) = (K_{pv} + \frac{K_{iv}}{s}) \tag{3.57}$$

The closed loop gain becomes

$$T_v(s) = Gc_v(s).G_{vv}(s) = \frac{1}{V_0.C.s}.(K_{pv} + \frac{K_{iv}}{s}) \tag{3.58}$$

The voltage control closed loop transfer function can be written as

$$Gv_e(s) = \frac{T_v(s)}{1 + T_v(s)} \tag{3.59}$$

Applying the Nyquist stability criteria for $Gv_e(s)$, we get

$$|T_v(j.\omega_v)| = 1 \tag{3.60}$$

$$\angle T_v(j.\omega_v) = -180^0 + \phi_v \tag{3.61}$$

where ω_v is the gain cross over frequency and ϕ_v is the phase margin at gain cross over frequency. From Eqn. 3.58 and Eqn. 3.61, we get

$$K_{iv} = \frac{K_{pv}.\omega_v}{\tan(\phi_v)} \tag{3.62}$$

From Eqn. 3.58 and Eqn. 3.60, we get

$$|\frac{1}{V_0.C.(j.\omega_v)}.(K_{pv} + \frac{K_{iv}}{j.\omega_v})| = 1 \tag{3.63}$$

$$\sqrt{(\omega_v.K_{pv})^2 + K_{iv}^2} = \omega_v^2.V_0.C \tag{3.64}$$

Substituting Eqn. 3.62 in Eqn. 3.64, we get

$$\sqrt{(\omega_v.K_{pv})^2 + (\frac{K_{pv}.\omega_v}{\tan(\phi_v)})^2} = \omega_v^2.V_0.C \tag{3.65}$$

$$\frac{\omega_v.K_{pv}}{\tan(\phi_v)}.\sqrt{1 + (\tan(\phi_v))^2} = \omega_v^2.V_0.C \tag{3.66}$$

$$K_{pv} = V_0.C.\omega_v.\sin(\phi_v) \tag{3.67}$$

The modelling, steady state analysis and controller design for a Dual Boost BPFC converter explained in this section is verified by simulation and hardware prototype. The 500 W Dual Boost BPFC converter design and hardware implementation is described in the next section.

3.4 Design and Implementation

The power components design and controller design of the 500 W Dual Boost BPFC converter converter is discussed in this section. The design parameters of the 500 W Dual Boost BPFC converter are given in Table. 3.1.

Table 3.1: Design input specifications of a 500 W prototype

Parameter	**Specification**
Nominal Input Voltage, V_{nom}	230 V
Operating Input Voltage range, V_{rms}	85 V - 265 V
Nominal Output Voltage, V_0	400 V
Output Power, P_0	500 W
Switching frequency, f_s	100 kHz
Input current ripple, ΔI_L	20% @ V_{nom}
Output Voltage ripple, ΔV_0	2%

3.4.1 Boost Inductor Design

The boost inductor of the PFC converter is designed based on the switching ripple current and average current. Allowing more ripples will reduce the inductor value, but this will increase input line noise and the peak current through the diode rectifier, and switch. From Eqn. 3.17, the minimum value of duty ratio is obtained at the peak of input voltage. For $230V$ input voltage, the minimum value of duty ratio is

$$d_{min,@230V} = \frac{(V_0 - v_{g,max})}{V_0} = \frac{(400 - 230.\sqrt{2})}{400} = 0.1868 \tag{3.68}$$

The maximum averaged current for 500 W power output at 230 V input is given by

$$I_{L,avg,max,@230V} = \frac{\sqrt{2}.P_{0(max)}}{V_{rms}} = \frac{(\sqrt{2}).(500)}{230} = 3.074A \tag{3.69}$$

The desired peak-to-peak ripple current at 230 V is given as

$$\Delta I_{L,max,@230V} = (0.2).I_{L,avg,max,@230V} = 0.6148A \tag{3.70}$$

The minimum value of the inductor required in each boost circuit, for 20% current ripple at 230 V input is given by

$$L_{min} = \frac{\sqrt{2}.V_{rms}.d_{min,@230V}}{\Delta I_{L,max,@230V}.f_s} = 0.988mH \tag{3.71}$$

In order to have a safety margin, 1.1 mH inductor was chosen. With this inductance the peak-to-peak ripple current at 230 V becomes

$$\Delta I_{L,max,@230V} = \frac{\sqrt{2}.V_{rms}.d_{min,@230V}}{L.f_s} = 0.552A = 18\% I_{L,avg,max,@230V} \tag{3.72}$$

The maximum averaged current for 500 W power output in the whole input voltage operating range of 85 V to 265 V occurs at 85V and is given by

$$I_{L,avg,max} = \frac{\sqrt{2}.P_{0(max)}}{V_{rms,min}} = \frac{(\sqrt{2}).(500)}{85} = 8.319A \tag{3.73}$$

The maximum peak-to-peak current ripple in the whole input operating range which also occurs at 85 V input voltage, is given by

$$\Delta I_{L,max} = \frac{\sqrt{2}.V_{rms}.d_{min,@85V}}{L.f_s} = 0.764A \tag{3.74}$$

The peak input current drawn in the whole input operating range is

$$I_{L,peak} = I_{L,avg(max)} + (0.5).\Delta I_{L(max)} = 8.7012A \tag{3.75}$$

A toroidal core inductor *MCAP115018077A-561LU from Multicomp* of 560 μH inductance with current rating of 10 A is selected for the 500 W prototype. Two such inductors in series add upto 1.12 mH.

3.4.2 Output Capacitor Design

The ripple voltage on the output capacitor is obtained from the power balance equation of the output capacitor. The input power from the AC source is given by

$$P_{in}(t) = (\sqrt{2}.V_{in,rms}.\sin(\omega_L.t)).(\sqrt{2}.I_{in,rms}.\sin(\omega_L.t)) \tag{3.76}$$

$$P_{in}(t) = V_{in,rms}.I_{in,rms}.(1 - \cos(2.\omega_L.t)) \tag{3.77}$$

The output power drawn by the load is given by

$$P_0 = V_0.I_0 = V_{in,rms}.I_{in,rms} \tag{3.78}$$

From Eqn. 3.77 and Eqn. 3.78, the power balance equation of the output capacitor becomes

$$P_C(t) = P_{in}(t) - P_0 \tag{3.79}$$

$$C.\frac{dV_0}{dt}.V_0 = -P_0.\cos(2.\omega_L.t)) \tag{3.80}$$

Integrating the equation over half of the input voltage cycle gives the peak-peak ripple on the output capacitor as

$$\Delta V_c = \frac{I_0}{\omega_L.C} \tag{3.81}$$

A larger value of the output capacitance results in better performance but this can increase the cost and size. The minimum value of the output capacitor required can be determined by imposing the maximum output voltage ripple limit in Eqn. 3.81 and is given by

$$C_{min} = \frac{I_0}{\omega_L.\Delta V_c} = \frac{(500/400)}{(2).(\pi).(50).(0.02).(400)} = 497\mu F \tag{3.82}$$

In order to have a safety margin, the value of C chosen was 680 μF.

3.4.3 Digital Controller Design

In order to achieve a unity power factor, the current loop should have a fast bandwidth. But the bandwidth of a controller implemented in a digital platform is limited

by its sampling frequency. To achieve average current mode control, the sampling of ADC and PWM switching can be synchronised such that the ADC sampling will occur exactly at the middle of switching interval. Also, by using this technique, the ADC sampled data is unaffected by the switching EMI. For slower voltage loop, the output voltage is sampled at a frequency of 1 kHz. The ADC sampling can be modelled as a zero order hold system whose transfer function is given as

$$ZOH(j.\omega) = \frac{1 - e^{-j.\omega.T_{adc}}}{j.\omega} = e^{-\frac{j.\omega.T_{adc}}{2}}.sinc(\frac{\omega.T_{adc}}{2}) \tag{3.83}$$

where T_{adc} is the ADC sampling period. At gain cross over frequency, this ZOH system introduces a phase delay of

$$\Delta\phi = \frac{\omega_c.T_{adc}}{2} \tag{3.84}$$

So the digital controller has to be designed taking this additional phase delay into account.

To avoid sub-harmonic oscillations, the inner current loop gain cross over frequency is limited to $f_s/6$ i.e. 16.67 kHz [16]. Choosing a gain cross over frequency of 10 kHz for the current controller , phase delay added by ADC sampling at 100 kHz is given by Eqn. 3.84 as

$$\Delta\phi_i = \frac{\omega_c.T_{adc}}{2} = 18^0 \tag{3.85}$$

Choosing a phase margin of 70^0, the gain parameters are obtained using Eqn. 3.47 and Eqn. 3.42 as

$$K_{pi} = \frac{L.\omega_c}{V_0}.\sin(\phi_i) = \frac{2.\pi.10^4.(1.1).10^{-3}}{400}.\sin(70^0) = 0.1624 \tag{3.86}$$

$$K_{ii} = \frac{K_{pi}.\omega_c}{\tan(\phi_i)} = \frac{(0.1624).(2.\pi.10^4)}{\tan(70)} = 3713.91 \tag{3.87}$$

Choosing a gain cross over frequency of 20 Hz for the voltage controller , phase delay added by ADC sampling at 1 kHz is given by Eqn. 3.84 as

$$\Delta\phi_v = \frac{\omega_v.T_{adc}}{2} = 3.6^0 \tag{3.88}$$

Choosing a phase margin of 65^0, the gain parameters are obtained using Eqn. 3.67 and

Eqn. 3.62 as

$$K_{pv} = V_0.C.\omega_v.\sin(\phi_v) = (400).(680).10^{-6}.(2.\pi).(20).\sin(65^0) = 30.97 \quad (3.89)$$

$$K_{iv} = \frac{K_{pv}.\omega_v}{\tan(\phi_v)} = \frac{(30.97).(2.\pi).(20)}{\tan(65^0)} = 1815.25 \quad (3.90)$$

The bode plot of loop gains of the uncompensated and compensated systems of the designed system are shown below.

- Fig. 3.8 shows the bode plot of uncompensated input current to duty transfer function ($G_{id}(s)$). It is observed that the system has a gain cross over frequency of 57.9 kHz and phase margin of 90^0.

- Fig. 3.8 shows the bode plot of compensated input current to duty transfer function ($G_{id}(s).G_{ci}(s)$). It is observed that the system gain cross over frequency is shifted from 57.9 kHz to 10 kHz using the designed compensator with a phase margin of 70^0.

- Fig. 3.8 shows the bode plot of uncompensated output voltage to voltage control transfer function ($G_{vv}(s)$) It is observed that the system has a gain cross over frequency of 0.585 Hz and phase margin of 90^0.

- Fig. 3.8 shows the bode plot of compensated output voltage to voltage control transfer function ($G_{vv}(s).G_{cv}(s)$). It is observed that the system gain cross over frequency is shifted from 0.585 Hz to 20 Hz using the designed compensator with a phase margin of 65^0.

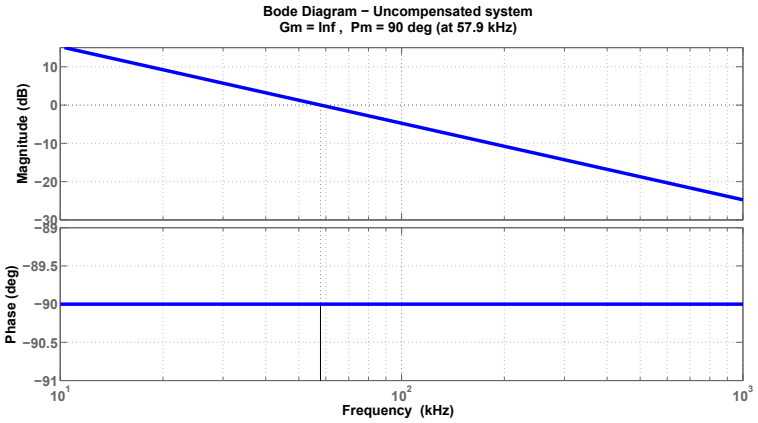


Figure 3.8: Bode plot of uncompensated input current to duty transfer function ($G_{id}(s)$)

To validate the design, a 500 W Dual Boost BPFC converter is simulated and a hardware prototype is developed. The simulation and hardware results of the 500 W prototype are discussed in the next section.

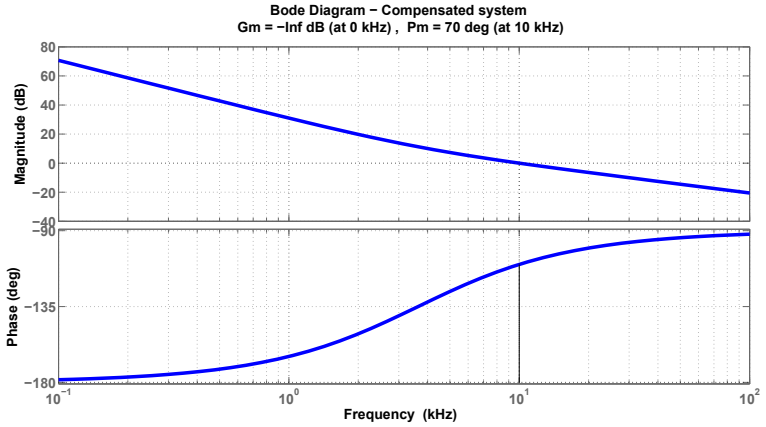


Figure 3.9: Bode plot of compensated input current to duty transfer function ($G_{id}(s).G_{ci}(s)$)

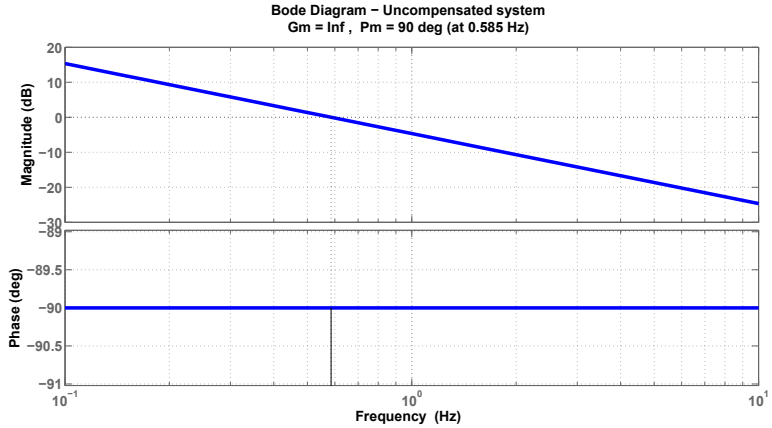


Figure 3.10: Bode plot of uncompensated output voltage to voltage control transfer function ($G_{vv}(s)$)

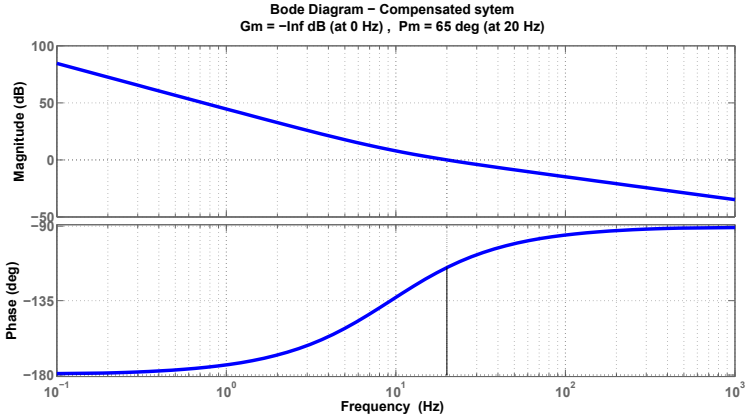


Figure 3.11: Bode plot of compensated output voltage to voltage control transfer function ($G_{vv}(s).G_{cv}(s)$)

3.5 Simulation Results

Performance of the designed system is evaluated by using MATLAB/SIMULINK simulation tool. The obtained simulation results are discussed in this section. The parameters and component values of the designed system are summarized in Table 3.2.

Table 3.2: Specifications of the designed 500 W prototype

Parameter	**Specification**
Nominal Input Voltage, V_{rms}	230 V
Operating Input Voltage range, V_{rms}	85 V - 265 V
Nominal Output Voltage, V_0	400 V
Maximum Output Power, P_0	500 W
Line frequency, f_L	50 Hz
Switching frequency, f_s	100 kHz
Boost Inductor, L	1.1 mH
Output Capacitor, C	680 μH
K_{pi}	0.1624
K_{ii}	3713.91
K_{pv}	30.97
K_{iv}	1815.25

3.5.1 Steady State Performance

- Fig. 3.12 shows the steady state waveforms of input voltage, input current and the output voltage of the converter at full-load of 500 W with input voltage of 230 V. At steady state, a near sinusoidal input current was obtained with the input power factor (PF) of 0.9986. A THD of 9.8% in the input current waveform and output voltage ripple of 1.5% was achieved.

- Fig. 3.13 shows the steady state waveforms of input voltage, input current and the output voltage of the converter at full-load with 85 V input voltage. It was observed that, input power factor of 0.9998, input current THD of 3% and output voltage ripple of 1.5% was achieved.

- Fig. 3.14 shows the steady state waveforms of input voltage, input current and the output voltage of the converter at full-load with 265 V input voltage, for which an input power factor of 0.9978, input current THD of 10.2% and output voltage ripple of 1.5% were observed.

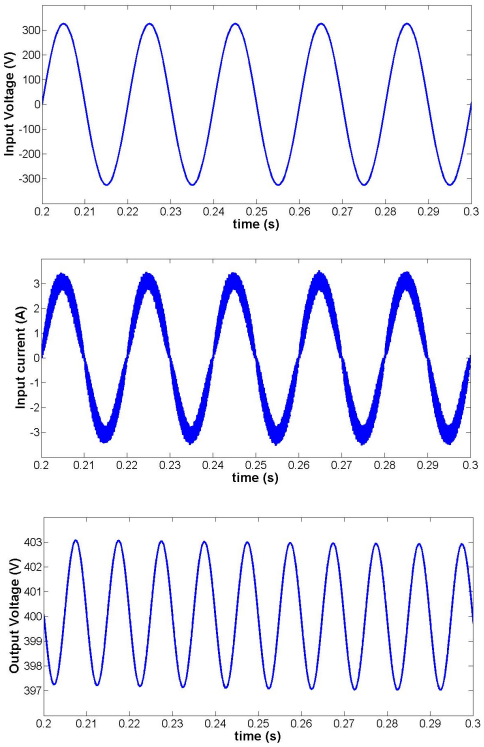


Figure 3.12: Simulation results showing steady state response of converter at full load with 230 V input voltage

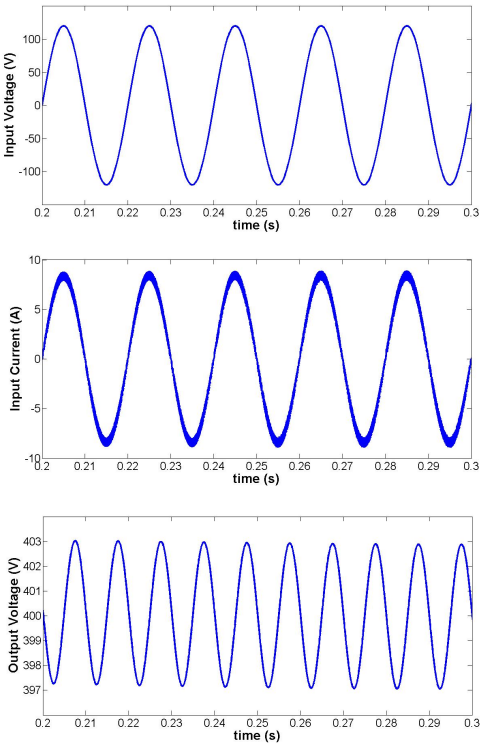


Figure 3.13: Simulation results showing steady state response of converter at full load with 85 V input voltage

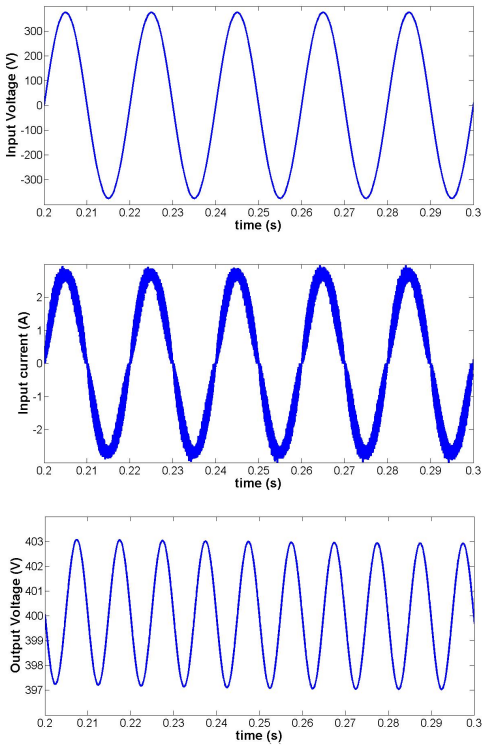


Figure 3.14: Simulation results showing steady state response of converter at full load with 265 V input voltage

3.5.2 Dynamic Performance

To observe the dynamic response of the converter, a step load change from 50% to 100% of rated power was applied with nominal input voltage of 230 V. Fig. 3.15 shows the output voltage and the input current response of the converter for the step load change. The pre-shoot and over-shoot of the output voltage is within 2% and settles within 100 ms which is five times the bandwidth of the converter.

3.6 Experimental Results

The developed 500 W Dual Boost BPFC converter prototype shown in Fig.3.16, is tested with resistive load and motor load. The steady state results obtained are presented below.

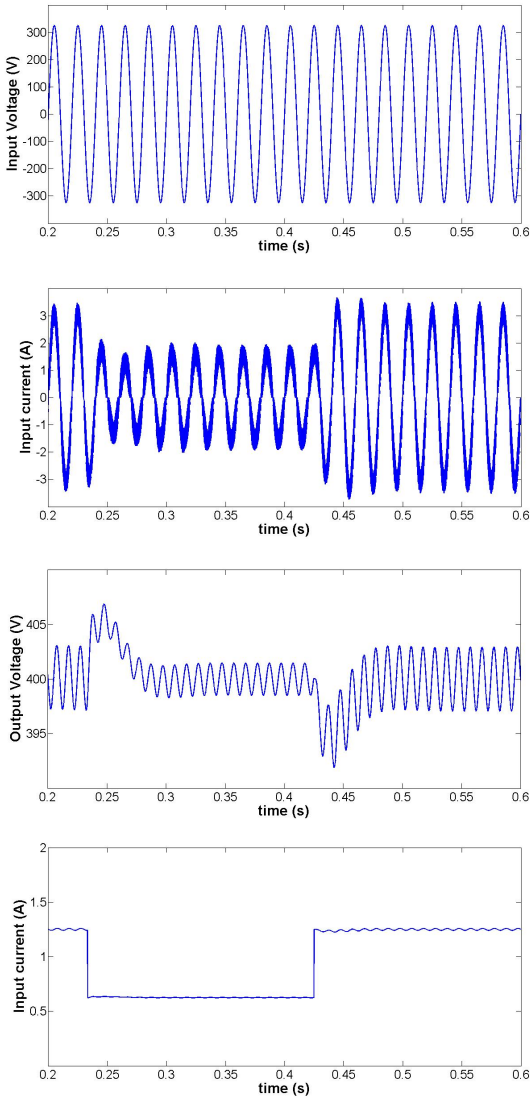


Figure 3.15: Simulation results showing dynamic response of converter for step load change from 50% to 100% of full load and back to 50%

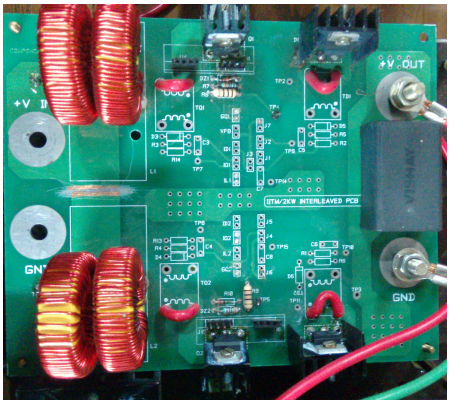


Figure 3.16: 500 W Dual Boost BPfC converter prototype

3.6.1 BPFC converter with resistive load

The developed 500 W prototype is tested with resistive load and the results obtained are listed below.

- Fig. 3.17 shows the duty ratio and switch drain-to-source voltage waveforms of Dual Boost BPFC converter. It is observed that the duty is varying sinusoidally with the input voltage and minimum duty is achieved at maximum input voltage. The drain-to-source voltage waveforms of the two switches S1 and S2 indicate that only one switch is operational in each half cycle of input voltage.

- Fig. 3.18 shows the steady state input voltage and input current waveforms at 230 V AC input and 123 W load with an input power factor of 0.985.

- Fig. 3.19 shows the steady state input voltage and input current waveforms at 90 V AC input and 123 W load with an input power factor of 0.997.

- Table 3.3 shows the input power factor and efficiency of the Dual Boost BPFC converter with input voltage of 230 V and varying resistive loads. The converter was tested upto 125 W due to board layout limitations.

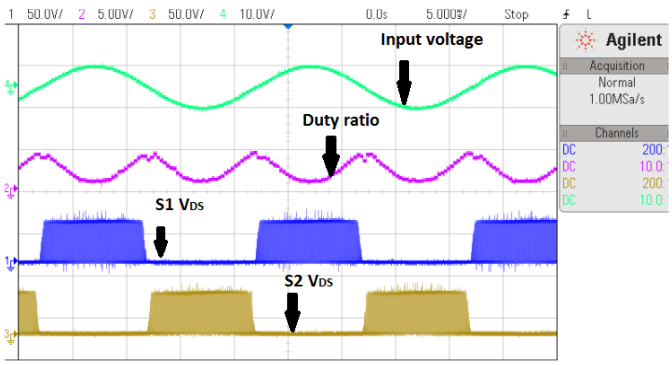


Figure 3.17: Duty ratio and switch drain-to-source voltage waveforms of Dual Boost BPFC converter

3.6.2 BPFC converter with VFD

The developed 500 W Dual Boost BPFC converter is used as a DC source for VFD driving a 100 W fan with single phase induction motor. The hardware setup is shown in Fig. 3.20. The results obtained are listed below.

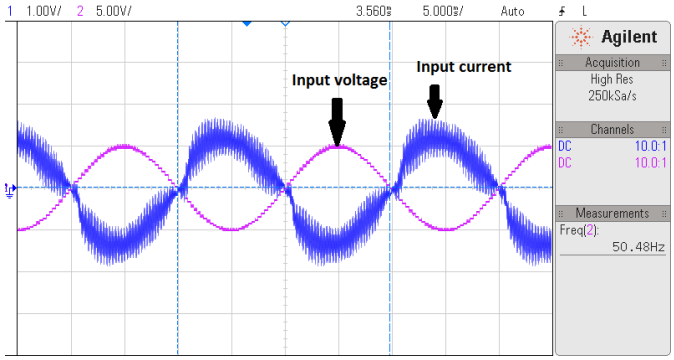


Figure 3.18: Steady state input current waveforms with input voltage of 230V

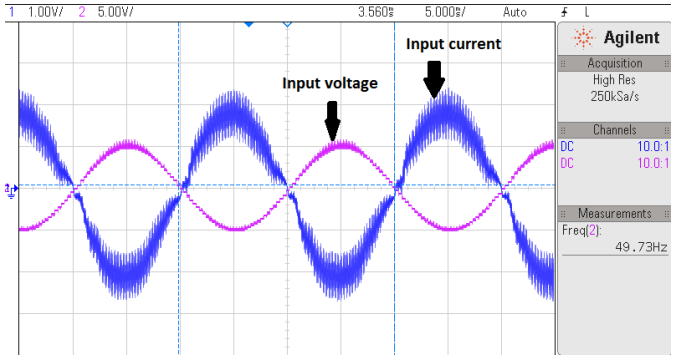


Figure 3.19: Steady state input current waveforms with input voltage of 90V

Table 3.3: Input power factor and efficiency of Dual Boost PFC converter for different resistive loads with 230 V AC input

Input Power(W)	**Input Power factor**	**Output Power(W)**	**Efficiency**
40.23	0.972	38.45	95.21
49.99	0.974	48.125	96.25
64.95	0.973	62.77	96.64
72.34	0.977	68.49	94.68
99.61	0.981	94.53	94.89
131.25	0.985	123.07	93.76

- Fig. 3.21 shows the steady state input voltage, input current and VFD output voltage waveforms of the VFD driving a 100 W fan, without Dual Boost BPFC converter. A 300 V DC is obtained by rectifying the 230 V AC input and is fed to the VFD.

- Fig. 3.22 shows the steady state input voltage, input current and VFD output voltage waveforms of the VFD driving a 100 W fan, with Dual Boost BPFC converter. The 400 V DC from the Dual Boost BPFC converter is fed to the VFD.

- Table 3.4 shows the input power factor comparison of VFD driving a 100W fan, with and without Dual Boost BPFC converter.

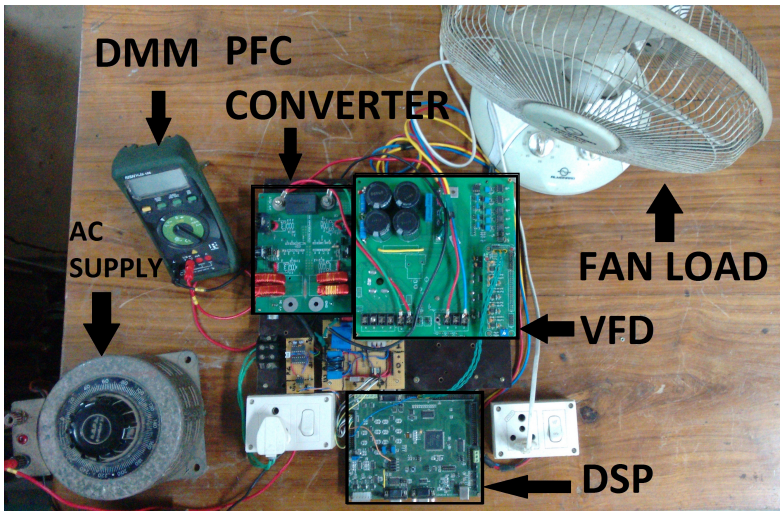


Figure 3.20: Experimental setup of Dual Boost BPfC converter with VFD driving a Fan

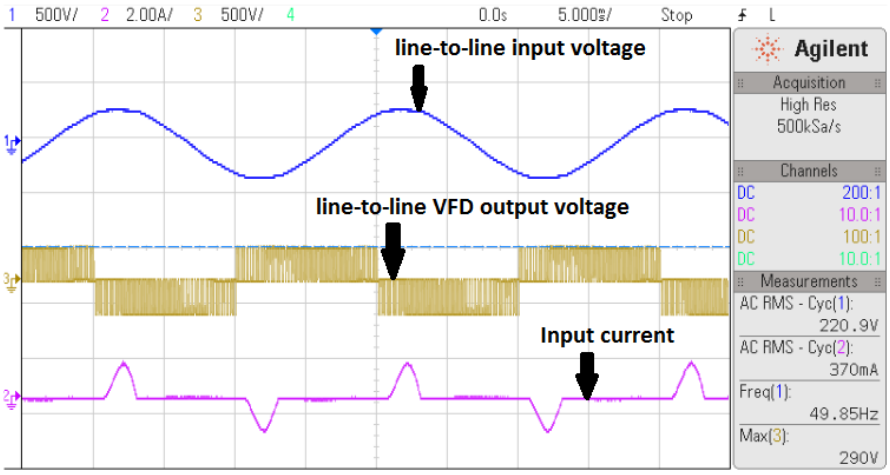


Figure 3.21: Steady state waveforms of the VFD driving a 100 W fan without Dual Boost BPFC converter

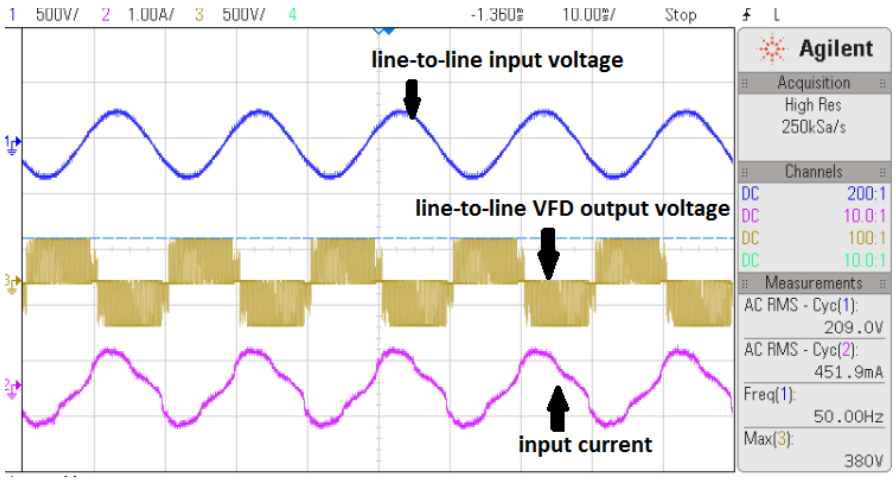


Figure 3.22: Steady state waveforms of the VFD driving a 100 W fan with Dual Boost BPFC converter

Table 3.4: Comparison of input power factor of VFD driving a 100 W Fan, with and without PFC converter

% speed	Power factor without PFC	Power factor with PFC
33%	0.5812	0.922
66%	0.5855	0.930
100%	0.5946	0.945

3.7 Conclusions

Dual Boost BPFC converter with average current-mode control is explained. A detailed analysis on modelling and controller design are presented. The power stage transfer functions of Dual Boost BPFC converter are developed, which are necessary to implement average current-mode control. Inner current loop controller and outer voltage loop controller are designed and implemented. A 500 W Dual Boost BPFC converter with average current-mode control is simulated in MATLAB/SIMULINK. The steady state and dynamic response of the converter obtained from the simulation results are presented. A laboratory prototype of the Dual Boost BPFC converter is built and tested upto 125 W and the experimental results are presented.

CHAPTER 4

Conclusions

4.1 Conclusions

In this thesis, guidelines for the design and selection of components for the Variable Frequency Drive is presented. A 2000 W VFD laboratory prototype is built and tested. The experimental results showing the load performance and efficiency are presented. The prototype achieved 98.5% efficiency at rated load condition with 0.65 input power factor. The need for Power Factor Correction in Variable Frequency Drive is explained. An overview of topologies belonging to a class of PFC converters called Bridge-less PFC converters is presented.

Dual Boost Bridge-less PFC Converter with average current control is explained. A detailed analysis on modelling and controller design are presented. State space averaging method is used to obtain small signal model of the Dual Boost BPFC Converter with average current-mode control. The power stage transfer functions of Dual Boost BPFC converter are developed, which are necessary to implement average current-mode control. A 500 W Dual Boost Bridge-less PFC Converter with average current-mode control is simulated in MATLAB/SIMULINK. The results obtained are in close agreement with the analytical model. Simulation results showing the steady state and dynamic performance of the simulated converter are presented. A laboratory prototype of the Dual Boost BPFC converter is built and tested upto 100 W and the experimental results are presented.

4.2 Future scope

Using the design procedure presented in this report, the Dual Boost Bridge-less PFC Converter can be scaled upto higher power levels. The feasibility of Dual Boost Bridge-less PFC Converter cascaded with another DC-DC converter to get 600 V to drive a 3-phase induction motor has to be explored.

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