An Analysis of Zero Temperature Coefficient Points in Si Channel nMOSFETs and SiGe channel pMOSFETs

A Project Report

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CERTIFICATE

This is to certify that the report titled **An Analysis of Zero Temperature Coefficient Points in Si Channel nMOSFETs and SiGe channel pMOSFETs**, submitted by **Mohammed Ajmal C, EE10B066** to the Indian Institute of Technology Madras, for the award of the degrees of **Bachelor of Technology** and **Master of Technology**, is a bona fide record of the project work done by him under my supervision. The contents of this report, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

Place: Chennai

Date: 6th May 2015

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Place: Chennai Mohammed Ajmal C

Date : 6th May 2015

ABSTRACT

KEYWORDS: ZTC Operating Point; Device characterization; Mobility; Threshold voltage; Temperature effects.

Proper Knowledge of temperature dependence of several parameters of a MOSFET is important in designing VLSI circuits, since the circuits may operate far above room temperature. The effect of temperature on drain current can be attributed to two factors-mobility and threshold voltage. It is noted that, in some cases the temperature dependences of mobility and threshold voltage mutually compensate, paving a way to the existence of a bias point where the drain current doesn't depend on temperature, called zero temperature coefficient (ZTC) point. In this work, efforts have been made to investigate the existence of ZTC points in Si channel nMOSFETs and SiGe channel pMOSFETs, and to justify their existence by examining the temperature dependences of mobility as well as threshold voltage. The conditions for existence of ZTC points has been derived mathematically. I-V and C-V measurements at various temperatures are taken for devices with various lengths and ZTC points are observed for NFETs in both linear and saturation regions and for PFETs in linear region. Threshold voltage has been extracted using constant current method and mobility values at various temperatures have been extracted using C-V and I-V characteristics. The very low value of thermal coefficient of threshold voltage and the temperature dependence power value of mobility model close to -1 validate the conditions for existence of ZTC points. The results obtained were cross checked using TCAD simulations and have found to be accurate.

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ABBREVIATIONS

MOSFET	Metal Oxide Semiconductor Field Effect Transistor
DTMOS	Dynamic Threshold voltage MOSFET
ZTC	Zero Temperature Coefficient
VLSI	Very Large Scale Integration
TCAD	Technology Computer-Aided Design
JFET	Junction Field Effect Transistor
CC	Constant Current
Si	Silicon
SiGe	Silicon Germanium
HfO_2	Halfnium Oxide
SMU	Source Measurement Unit
CMU	Capacitance Measurement Unit
IEEE	Institute of Electrical and Electronics Engineers

NOTATIONS

I_D	Darin Current
V_{GS}	Gate to source voltage
V_{DS}	Drain to source voltage
V_T	Threshold Voltage
μ_n	Electron Mobility
μ_{eff}	Effective Mobility
$\frac{W}{L}$	Aspect Ratio
W	Gate width of transistor
L	Channel length of transistor
C_{ox}	Oxide Capacitance
T	Temperature
T_0	Reference Temperature
α_{VT}	Thermal Coeffcient of Threshold Voltage
α_μ	Temperature dependence power of mobility model
V_{GSF}	Temperature independent gate voltage
I_{DF}	Temperature independent drain current
Q_n	Mobile channel charge density
k	Boltzmann Constant
C_{GC}	Gate to channel capacitance
C_{ov}	Overlapping capacitance
C_{ch}	Channel capacitance

CHAPTER 1

INTRODUCTION

The metal oxide semiconductor field effect transistor (MOSFET) is one of the cornerstones of modern semiconductor technology. The main reasons for preferring MOSFETs over other types of transistors are their high integration density and relatively simple manufacturing process. In an n-type MOSFET, heavily doped source and drain regions are implanted in to a lightly doped p-type substrate(body). A metal or poly crystalline gate covers the region between source and drain, but is separated from the semiconductor by gate oxide. The cross section of a typical NMOS transistor is shown in figure 1.1.

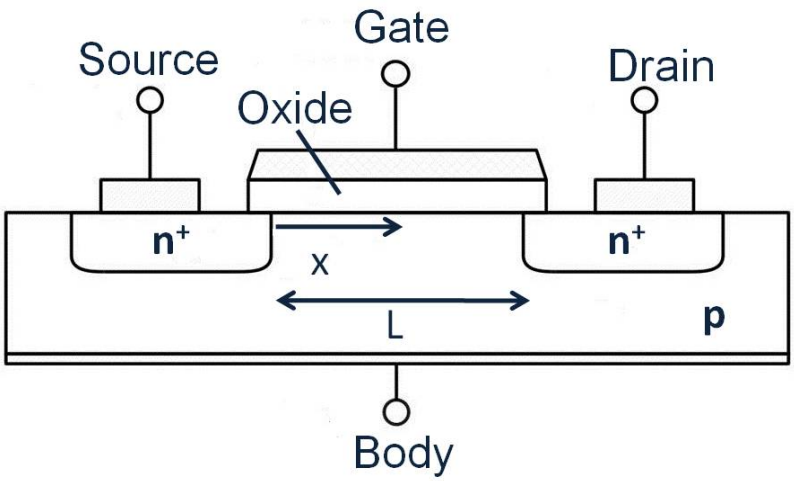

Fig. 1.1 Cross section of n-type MOSFET structure

In NMOS transistor, the current carriers are electrons. The flow of electrons from the source to the drain is controlled by the voltage applied to the gate. A positive voltage applied to the gate, attracts electrons to the interface between the gate dielectric and the semiconductor. These electrons form a conducting channel between the source and the drain, called the inversion layer. No gate current is required to maintain the inversion layer at the interface since the gate oxide blocks any carrier flow. The net result is that the current between drain and source is controlled by the voltage which is applied to the gate. Another MOS device can be formed by having source and drain heavily doped with acceptor impurities, in a lightly doped n-type substrate. Such devices are called

PMOS transistors and in those devices, the current is carried by holes through a p-type channel [1].

1.1 Threshold Voltage of a MOSFET

The threshold voltage(V_T) is the minimum gate-to-source voltage differential that is needed to create a conducting path between the source and drain terminals. For voltages less than V_T, the channel is cut off and MOSFETs don't conduct.By operating the MOSFET in particular bias regions, based on the V_{GS}, V_{DS} and I_D, it can be used to perform a variety of functions. The two regions that the MOSFET device can operate in are the ohmic (linear) and saturation (active) regions. Shown in figure 1.2 is the MOSFET I_D-V_{DS} curve for constant values of V_{GS}. Notice the ohmic region that exist when V_{DS} is very small. For a MOSFET, when $V_{DS} < V_{GS} - V_T$, it is said to be linear region and when V_{DS} exceeds $V_{GS} - V_T$, the MOSFET is said to be in saturation region [2].

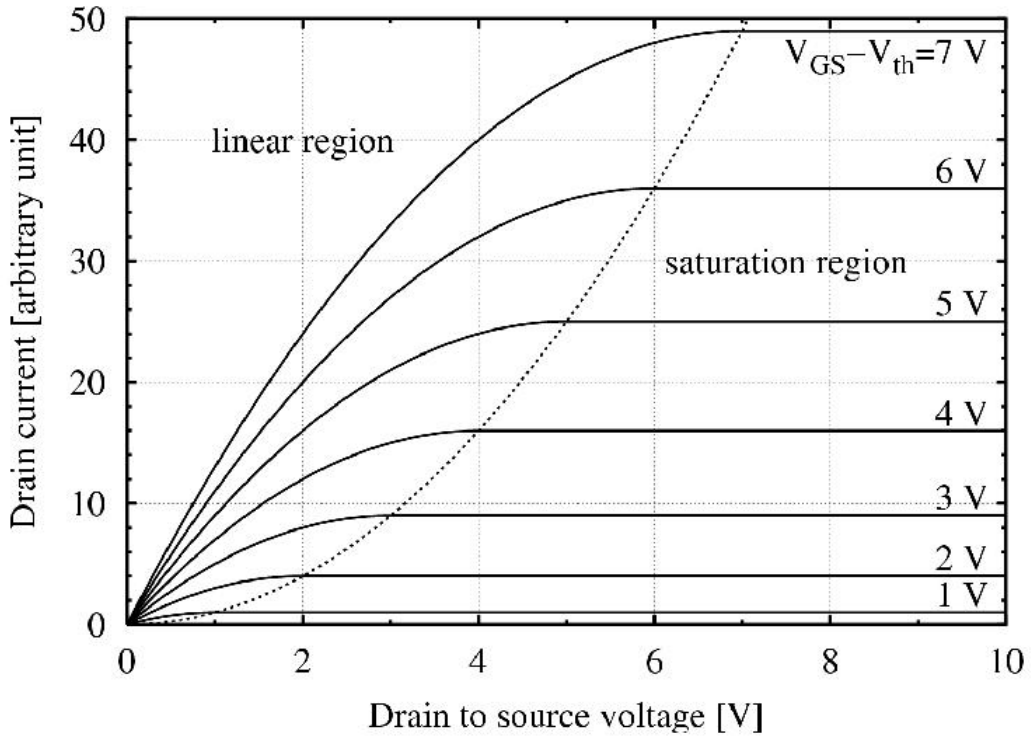

Fig. 1.2 Cross section of n-type MOSFET structure

1.2 Temperature Dependence of MOSFET parameters

The temperature dependence of electrical parameters has been an interesting area for research. The current through a MOSFET depends upon temperature too since the factors such as mobility and threshold voltage have significant dependence on temperature. Since we are living in an era where integrated circuits often work at a high temperature ambience, it is important to study the effect of temperature on electrical parameters since such a study will be very useful in designing VLSI circuits. The $I_D - V_{GS}$ characteristics of MOSFETs give us insight about the temperature dependence of important parameters.

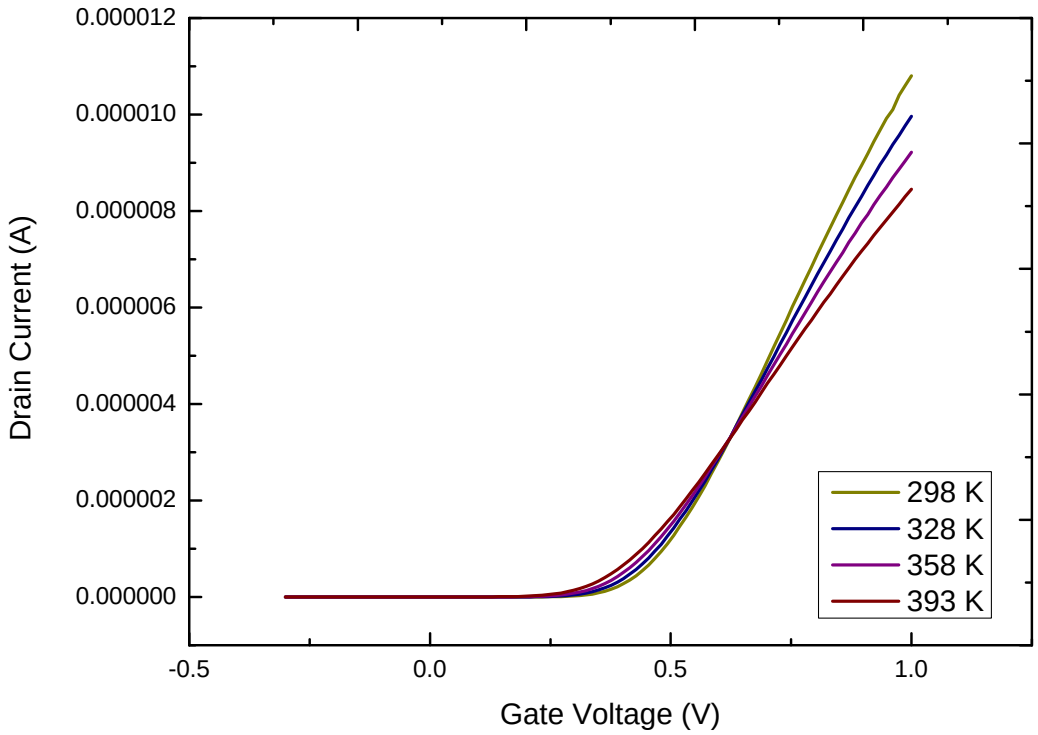

Fig. 1.3 Zero Temperature Coefficient point Observed for Si channel nMOSFET with $W = 1, L = 1$

Figure 1.3 shows the $I_D - V_{GS}$ characteristics, with temperature as a parameter, for a transistor designed in $32nm$ CMOS technology. One can see that the characteristics have a common intercept point . If the MOSFET is biased to this point, then the drain current will not depend on the temperature. This is the Zero Temperature Coefficient(ZTC) point [3]. Such a point comes to existence when the temperature effects of

both threshold voltage and mobility mutually compensate [4].

1.3 Introduction to the Problem

In this thesis, we are aiming to analyse the existence of ZTC points in silicon channel nMOSFETs and silicon-germanium channel pMOSFETs. For this goal, $I_D - V_{GS}$ characteristics at different temperatures have to be measured for various values of V_{DS}. By conducting the experiments on devices with different lengths, the dependence of ZTC points on the geometry of the device could also be found out. Then, to explain the behaviour of $I_D - V_{GS}$ curves at various temperatures, the dependency of threshold voltage as well as mobility on temperature have to be studied. For this goal to be achieved, channel to gate capacitance is measured at diverse temperatures. Using the temperature dependences observed in both threshold voltage and mobility, their mutual correlation has to be analysed to justify the existence or absence of ZTC points, if present or not. Finally, TCAD simulations could be used to compare the experimental results.

1.4 Applications of ZTC Point

Since the temperature dependence of mobility and threshold voltage is important in designing VLSI circuits, there are so many applications . The main application of ZTC points is in temperature stabilization of bias currents and voltages [4]. The temperature stable bias point resulted by the mutual compensation of mobility and threshold voltage temperature variations can be used to design a voltage reference circuit [5]. The circuit designed includes an operational amplifier that provides biasing of a diode-connected MOS transistor to the ZTC bias point. ZTC points are also used in operational amplifiers with a JFET input stage to provide temperature stable operating point [6]. Self biased current references are also presented using ZTC points [7], instead of the usual way of generating current reference of implementation of a voltage reference and applying this voltage over a resistive device. It is noted that the lower ZTC operating points(V_{GS}) with higher overdrive current of DTMOS improves the integrated circuit speed and efficiency for the low-power-consumption concept in green CMOS technology [8]. The ZTC bias point voltage also determines the optimal V_{DD} voltage in the digital circuits for

temperature insensitive operation [3]. The property of existence of ZTC point enables a diode-connected transistor to be used as a temperature sensor [9]. In order to detect abnormal temperature changes so as to detect defects on chip, and increase reliability and service life of devices, an all CMOS temperature sensor for sub-micron circuits' test based on ZTC operating point is suggested [10].

1.5 Organization of the Report

A brief outline of the report is as follows. *Chapter* 2 considers the mathematical analysis of conditions for existence of Zero Temperature Coefficient (ZTC) points and on how the temperature dependences of both threshold voltage and mobility leads to ZTC points. *Chapter* 3 deals with the results obtained through experiments on silicon channel NFETs and silicon-germanium channel PFETs at various temperatures . A more detailed analysis done in *Chapter* 4 talks about the temperature dependence of threshold voltage as well as mobility in the devices under experiments and investigates the origin of ZTC points in given devices. *Chapter* 5 contrasts the data obtained through simulation to that by experiments. The report is concluded in *Chapter* 6 with a summary of the work presented and putting forth suggestions for future work.

CHAPTER 2

Compensation of Mobility And Threshold Voltage Temperature Effects

This chapter describes how the temperature effects of both threshold voltage and mobility compensate mutually, thus resulting in Zero Temperature Coefficient(ZTC) Point. This chapter also discusses the conditions to be met for perfect compensation of temperature effects.

2.1 Condition for existence of ZTC point for nMOSFETs in saturation region

Most of the literature talk about the existence of ZTC point for devices when they are in strong inversion and mathematically analyzes the conditions for existence of ZTC points. Let us consider an n-channel transistor with drain current equation [11], when operating under strong inversion.

$$I_D = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)(V_{GS} - V_T)^2 \tag{2.1}$$

where μ_n is the carrier mobility, C_{ox} is the oxide capacitance, $\frac{W}{L}$ is the aspect ratio, V_{gs} is the gate to source voltage and V_T is the threshold voltage of the device.The temperature dependence of threshold voltage is usually given as [12]

$$V_T(T) = V_T(T_0) + \alpha_{VT}(T - T_0) \tag{2.2}$$

where T is the absolute temperature and T_0 is the reference temperature and $\partial V_T/\partial T = \alpha_{VT}$, the thermal coefficient (TC) of threshold voltage is a negative constant. Mobility of carriers is given by [13] the equation

$$\mu_n(T) = \mu_n(T_0)(T/T_0)^{\alpha_\mu} \tag{2.3}$$

where α_μ is the temperature dependence power of mobility model. We assume that α_μ is a constant. If there exist a point where the current is constant for all temperature vlaues at a particular bias voltage, we have drain current, at temperature T_1 satisfying condition $\partial I_d/\partial T = 0|_{T=T_1}$. Now, one can find the bias voltage for given temperature T_1 as

$$V_{GS} = V_T(T_1) + \left[2\mu_n \frac{\partial V_T/\partial T}{\partial \mu_n/\partial T}\right]\Bigg|_{T=T_1} \tag{2.4}$$

Now, when equations 2.2 and 2.3 are substituted in (2.4), we get the required gate to source bias voltage as

$$V_{GS} = V_T(T_0) + \alpha_{VT} T_1 \left(1 + \frac{2}{\alpha\mu}\right) - \alpha_{VT} T_0 \tag{2.5}$$

In addition, if $\alpha_\mu = -2$, then there exists a specific temperature independent voltage

$$V_{GS} = V_{GSF} = V_T(T_0) - \alpha_{VT} T_0 \tag{2.6}$$

which bias the n-channel transistor to a temperature independent drain current I_{DF}. If we substitute (2.1) and (2.2) into (2.4), we obtain

$$I_D = \frac{\mu_n(T) C_{ox}}{2}\left(\frac{W}{L}\right)(\alpha_{VT} T)^2 \tag{2.7}$$

If we substitute the mobility temperature dependence defined in (2.3) in (2.1) with $\alpha_\mu = -2$, we get

$$I_D = I_{DF} = \frac{\mu_n(T_0) T_0^2 C_{ox}}{2}\left(\frac{W}{L}\right)\alpha_{VT}^2 \tag{2.8}$$

So, here the decrease in carrier mobility with temperature is getting compensated with decrease in threshold voltage of the device with temperature, and the transistor biased by voltage V_{GSF} is producing a temperature independent drain current I_{DF} when $\alpha_\mu = -2$. We can have the same derivation for p-channel transistors too, indicating the presence zero temperature coefficient(ZTC) points.

2.2 Condition for existence of ZTC point for nMOSFETs in linear region

In literatures, the existence of zero temperature coefficient (ZTC) point when biased in saturation region is only discussed. Equation 2.1, from which we derived the condition for existence of ZTC point is only valid for saturation region. As we are measuring transfer characteristics for lower V_{DS}, the conditions for existence of ZTC points when biased in linear region should also be discussed. The following is an attempt to do that.

Let us consider an n-channel device biased in linear region, with drain current equation [11]

$$I_D = \mu_n C_{ox}\left(\frac{W}{L}\right)\left((V_{GS}-V_T)V_{DS}-\frac{V_{DS}^2}{2}\right) \tag{2.9}$$

If there exist a point where the current is constant for all temperature vlaues at a particular bias voltage, we have drain current, at Temperature T_1 satisfying condition $\partial I_d/\partial T = 0|_{T=T_1}$. Then,

$$V_{GS} = V_T(T_1)+\frac{V_{DS}}{2}+\left[\mu_n\frac{\partial V_T/\partial T}{\partial \mu_n/\partial T}\right]\Bigg|_{T=T_1} \tag{2.10}$$

Now, we substitute equations 2.2 and 2.3 in to equation 2.10, we get

$$V_{GS} = V_T(T_0)+\frac{V_{DS}}{2}+\alpha_{VT}T_1\left(1+\frac{1}{\alpha_\mu}\right)-\alpha_{VT}T_0 \tag{2.11}$$

For equation 2.11 to be temperature independent, α_μ should be equal to -1. Then, the temperature independent gate bias voltage can be expressed as

$$V_{GS} = V_{GSF} = V_T(T_0)+\frac{V_{DS}}{2}-\alpha_{VT}T_0 \tag{2.12}$$

Now,at ZTC bias point, the current could be written as

$$I_D = \mu_n(T)C_{ox}\left(\frac{W}{L}\right)(V_{DS}\alpha_{VT}T) \tag{2.13}$$

For $\alpha_\mu = -1$, if we substitute (2.3) in equation 2.13, we get

$$I_D = I_{DF} = \mu_n(T_0) C_{ox} \left(\frac{W}{L} \right) V_{DS} \alpha_{VT} T_0 \tag{2.14}$$

So again, the decrease in mobility with temperature is perfectly compensated with the reduction in threshold voltage for linear region too, subject to the condition that $\alpha_\mu = -1$. We can obtain the same condition for p-channel devices too.

CHAPTER 3

Analysis of Zero Temperature Coefficient Point

3.1 Experiment Setup

In this study, measurements are taken from Si channel nMOSFETs and SiGe channel pMOSFETs [14], with gate first high-k dielectric and metal gate technology, with the help of Cascade Microtech Summit 12000MP semi-automatic thermal probe station. HfO_2 is the high-k dielectric used in the devices. The I-V characteristics of devices of width $1\mu m$ and of lengths $1\mu m$, $90nm$ and $30nm$ have been measured at temperatures 25^oC, 55^oC, 85^oC and 120^oC. Temperature is controlled using a thermal chuck and measurements are realized using Agilent B1500 device analyser.

3.2 Experiment Proceedure

The wafer is loaded in to cascade microtech thermal probe station. Temperature is initially set to 25^oC using the thermal chuck. The source measurement units(SMU) of the device analyser Agilent b1500A is connected to the thermal probe station. Calibration of the probes are done from Agilent EasyExpert Software. Through Agilent EasyExpert, proper voltages are applied to drain, source and substrate pads of the device under measurement. For transfer characteristics in linear region, drain voltage is set to $50mV$ for NFETs($-50mV$ for PFETs) and for measurement in saturation region, drain voltage is set to $1V$ for NFETs($-1V$ for PFETs). Gate voltage is sweeped and corresponding drain to source current is measured. This procedure is repeated after changing the temperature to 55^oC, 85^oC and 120^oC for all devices.

3.3 Experiment for NFETs

$I_D - V_{GS}$ characteristics have been collected for silicon channel NFETs with a width of $1\mu m$ and lengths $1\mu m$, $90nm$ and $30nm$ for drain voltages $50mV$ and $1V$. Figure 3.1

shows a sample transfer characteristics generated by device analyser for NFET with length and width each of $1\mu m$ for $V_DS = 50mV$ at a temperature of 25^oC.

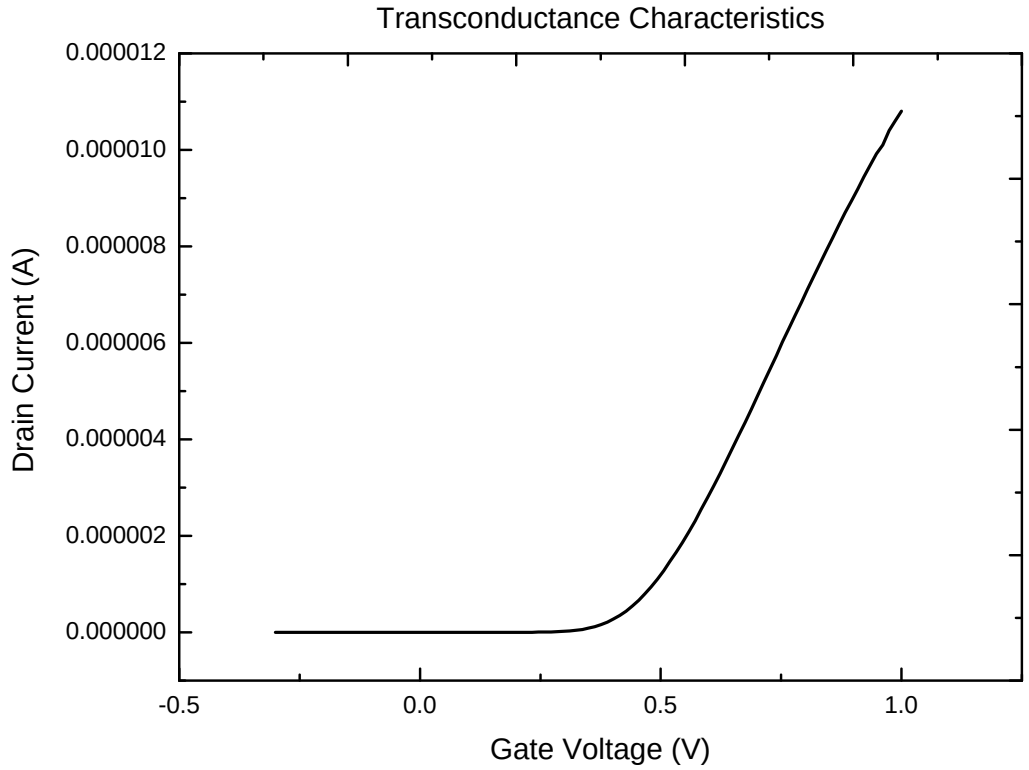

Fig. 3.1 A I-V graph obtained using the proceedure explained

3.3.1 NFET with $W = 1\mu m$ and $L = 1\mu m$ at $V_{DS} = 50mV$

Figure 4.16 shows the transfer characteristics obtained for silicon channel NFET with length and width each $1\mu m$ at different temperatures when $V_{DS} = 50mV$ is applied and V_{GS} is varied from $-0.3V$ to $1V$. Figure 4.16 indicates the existence of Zero Temperature Coefficient(ZTC) point for the device in linear region.

Figure 3.3, which is a rescaled version of figure 4.16 suggests that the curves for different temperatures does not actually cross over at an exact single point, rather they form a bottle neck around $V_{GS} = 0.625V$ to $V_{GS} = 0.63V$.

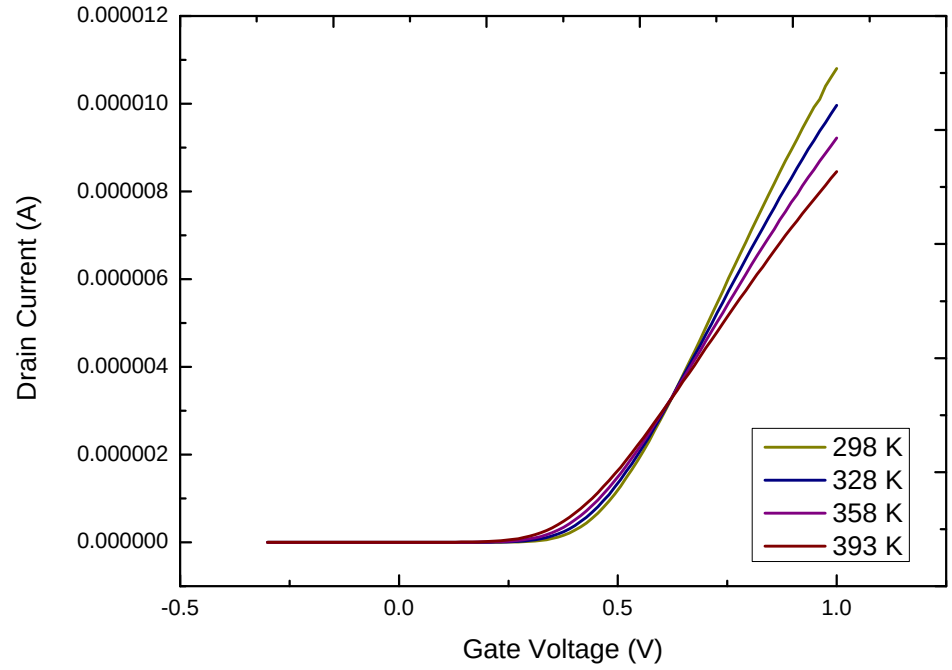

Fig. 3.2 I-V characteristics for NFET with $W = 1\mu m$, $L = 1\mu m$ at $V_{DS} = 50mV$ with temperature as a parameter

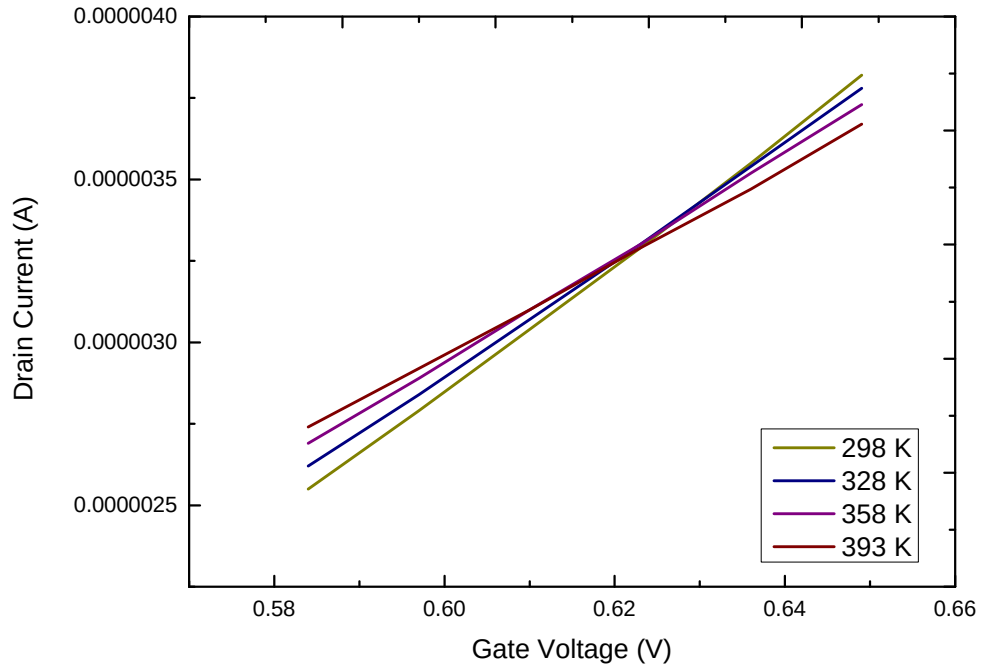

Fig. 3.3 Rescaled transfer characteristics for NFET with $W = 1\mu m$, $L = 1\mu m$ at $V_{DS} = 50mV$ with temperature as a parameter

3.3.2 NFET with $W = 1\mu m$ and $L = 90nm$ at $V_{DS} = 50mV$

The transfer characteristics for the device is shown in figure 3.4, which indicates the existence of ZTC point around $V_{GS} = 0.70V$ when $V_{DS} = 50mV$.

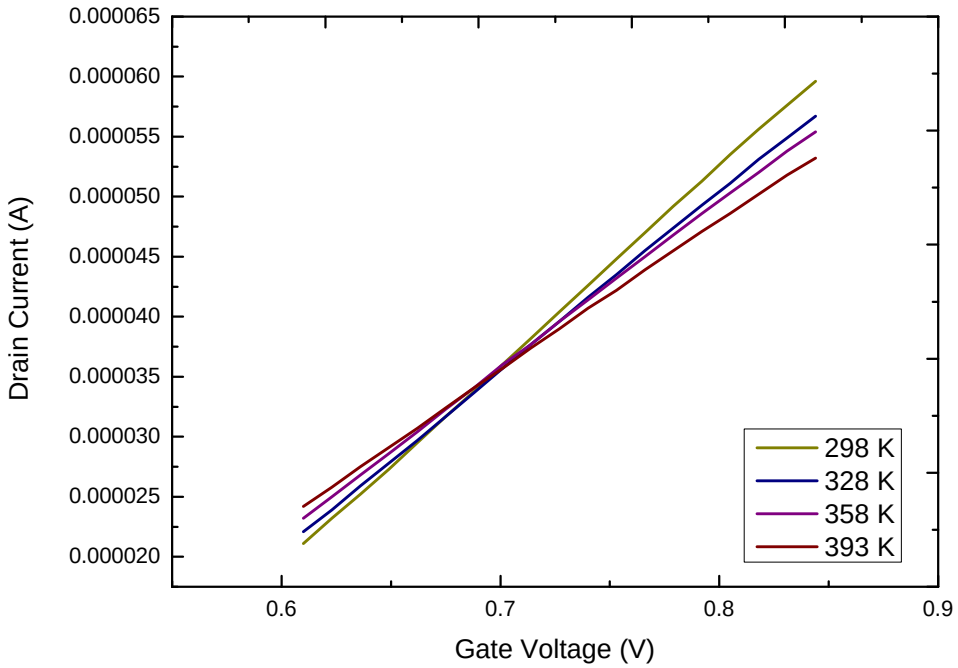

Fig. 3.4 I-V characteristics for NFET with $W = 1\mu m$, $L = 90nm$ at $V_{DS} = 50mV$ with temperature as a parameter

3.3.3 NFET with $W = 1\mu m$ and $L = 30nm$ at $V_{DS} = 50mV$

The transfer characteristics obtained for silicon channel NFET with a length of $30nm$ and a width of $1\mu m$ at different temperatures when $V_{DS} = 50mV$ is applied and V_{GS} is sweeped from $-0.3V$ to $1V$ is shown in figure 3.5. The presence of a ZTC point around $V_{GS} = 0.80V$ is suggested by figure 3.9.

3.3.4 NFET with $W = 1\mu m$ and $L = 1\mu m$ at $V_{DS} = 1V$

Figure 4.16 shows the transfer characteristics obtained for silicon channel NFET with length and width each $1\mu m$ at different temperatures when $V_{DS} = 1V$ is applied and V_{GS} is sweeped from $-0.3V$ to $1V$. Figure 3.6 shows the presence of Zero Temperature

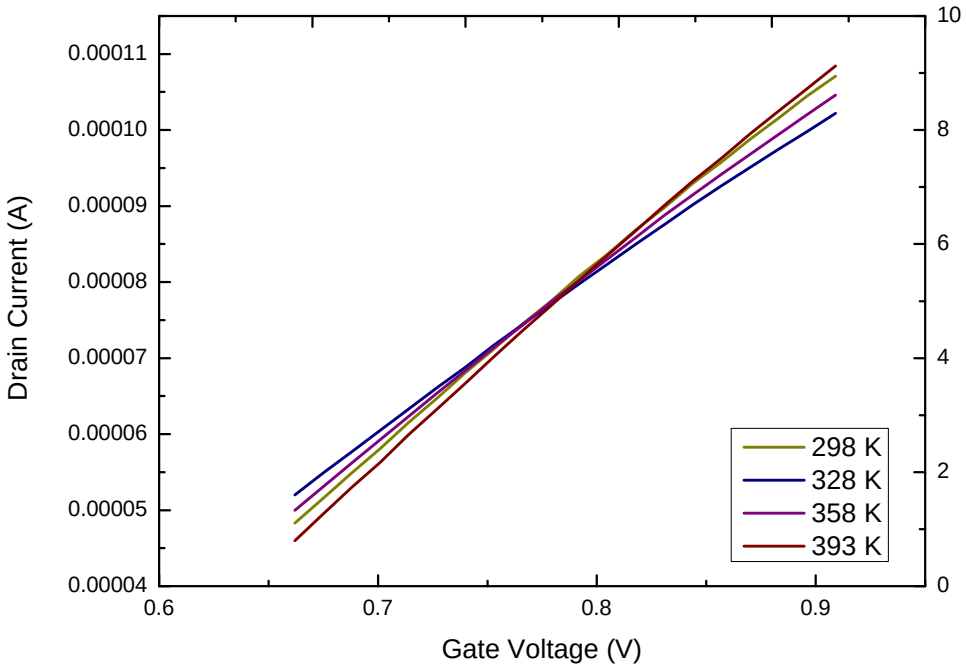

Fig. 3.5 I-V characteristics for NFET with $W = 1\mu m$, $L = 30nm$ at $V_{DS} = 50mV$ with temperature as a parameter

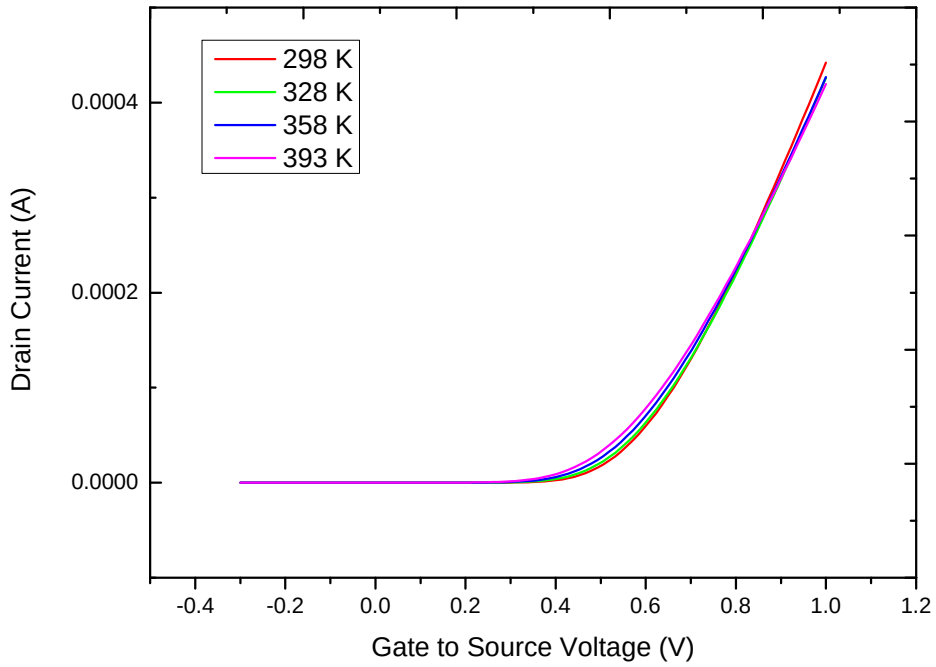

Fig. 3.6 I-V characteristics for NFET with $W = 1\mu m$, $L = 1\mu m$ at $V_{DS} = 1V$ with temperature as a parameter

Coefficient(ZTC) point for the device in saturation region.

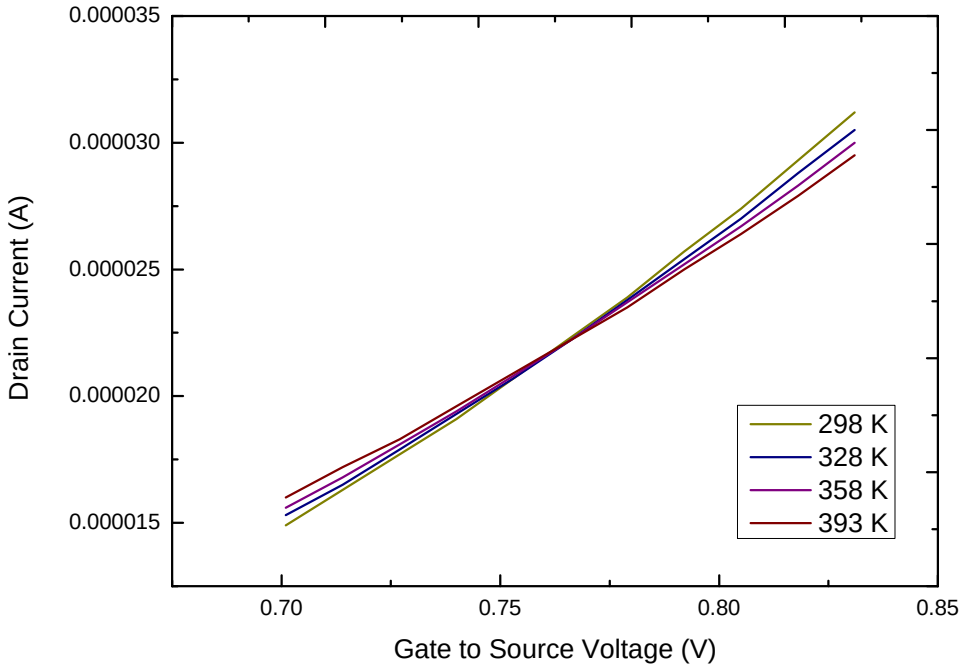

Fig. 3.7 Rescaled transfer characteristics for NFET with $W = 1\mu m, L = 1\mu m$ at $V_{DS} = 1V$ with temperature as a parameter

Figure 3.7, which is a rescaled version of figure 3.6 indicates that the curves for different temperatures actually cross over at an exact single point here, when compared to plots for $V_{DS} = 50mV$ at $V_{GS} = 0.76V$.

3.3.5 NFET with $W = 1\mu m$ and $L = 90nm$ at $V_{DS} = 1V$

The transfer characteristics for the device when $V_{DS} = 1V$ is shown in figure 3.8. The curves don't cross over at a single point, rather they form a bottle neck around $V_{GS} = 0.81V$.

3.3.6 NFET with $W = 1\mu m$ and $L = 30nm$ at $V_{DS} = 1V$

The transfer characteristics obtained for silicon channel NFET with a length of $30nm$ and a width of $1\mu m$ at different temperatures when $V_{DS} = 1mV$ is applied and V_{GS} is sweeped from $-0.3V$ to $1V$ is shown in figure 3.9. Figure 3.5 suggests that an ex-

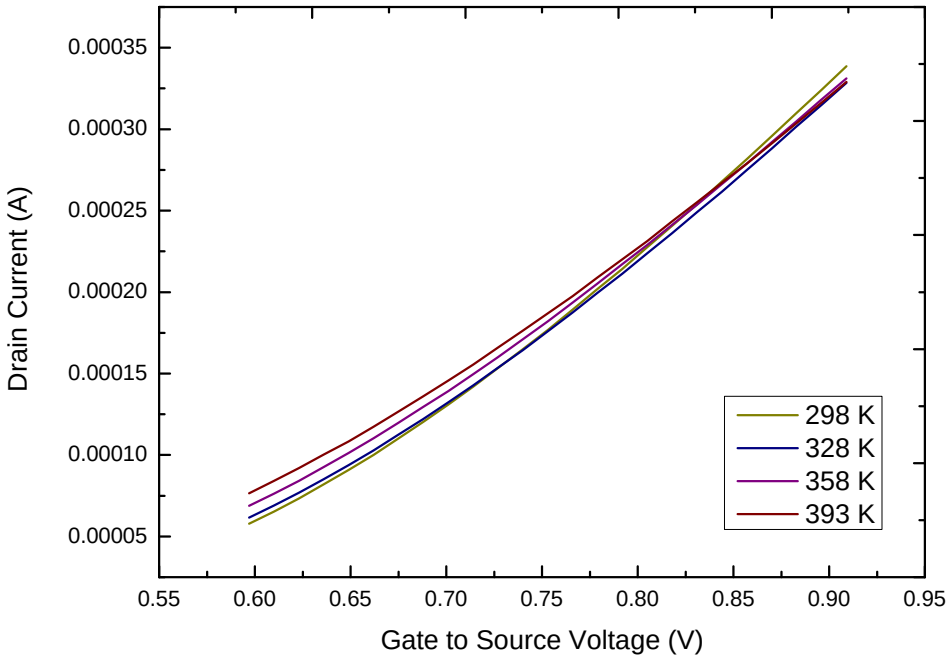

Fig. 3.8 I-V characteristics for NFET with $W = 1\mu m$, $L = 90nm$ at $V_{DS} = 1mV$ with temperature as a parameter

act ZTC point doesn't exist for $L = 30nm$ in the saturation region for silicon channel NFETS as in the cases of $L = 1\mu m$ and $L = 90nm$, but there exists a bottle neck around 0.95 V. The range of the bottle neck region is broader here.

3.4 Experiment for PFETs

Using device analyser, the I-V measurement for silicon-germanium channel PFETs with a width of $1\mu m$ and of lengths $1\mu m$, $90nm$ and $30nm$ have been made at the temperatures 55^oC, 85^oC and 120^oC. Gate voltage is sweeped from -1 V to 0.3 V for each measurement and substrate as well as source are grounded. Measurements are done for $V_{DS} = -50mV$ and $V_{DS} = -1V$. Figure 3.10 shows absolute value of drain current plotted versus the gate to source voltage.

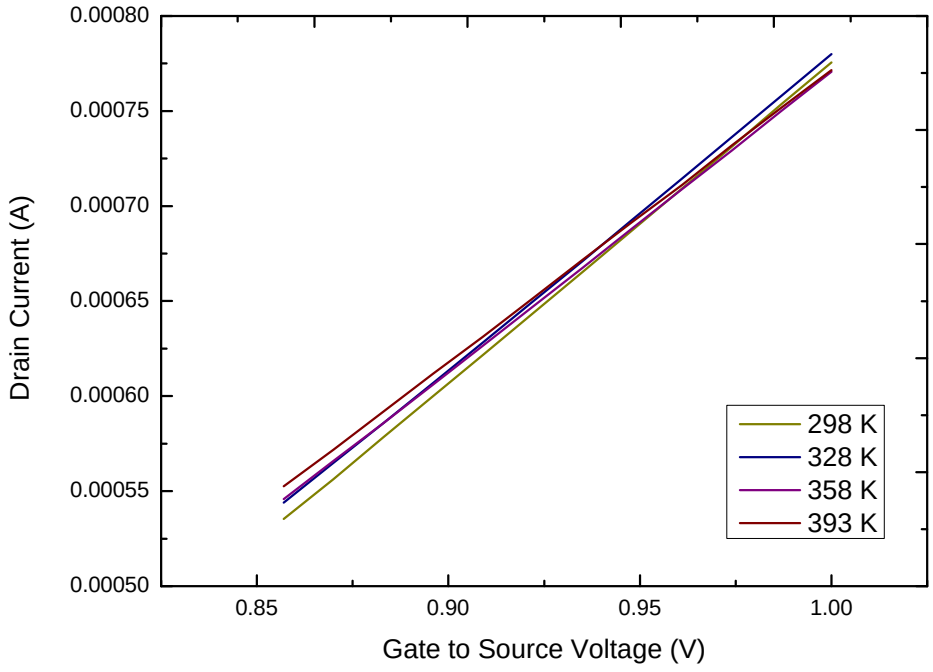

Fig. 3.9 I-V characteristics for NFET with $W = 1\mu m$, $L = 30nm$ at $V_{DS} = 1V$ with temperature as a parameter

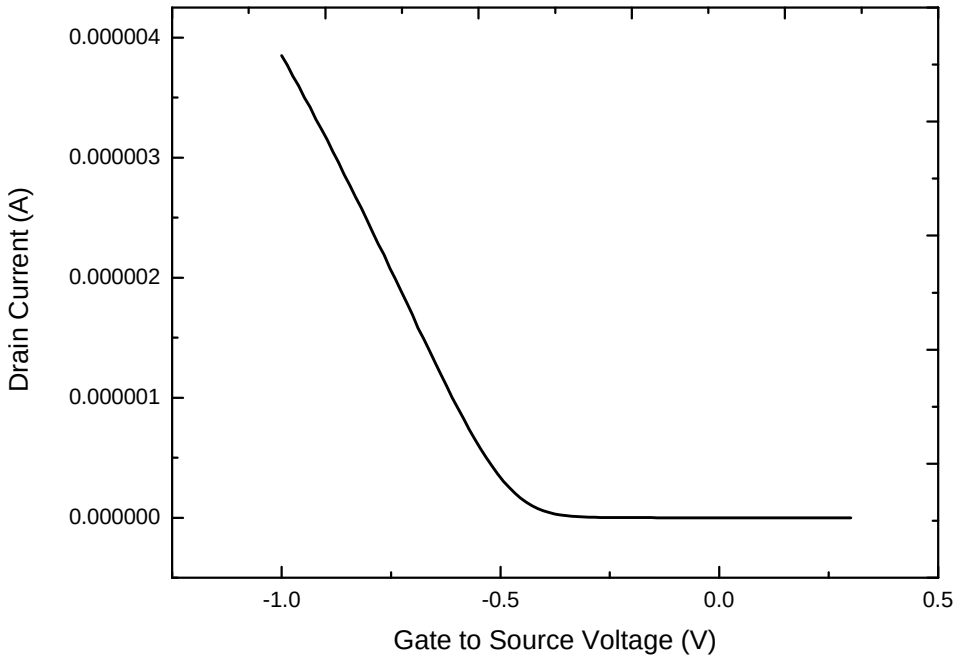

Fig. 3.10 I-V characteristics for PFET with $W = 1\mu m$, $L = 30nm$ at $V_{DS} = 1V$ at 25^oC

3.4.1 PFET with $W = 1\mu m$ and $L = 1\mu m$ at $V_{DS} = -50mV$

Figure 3.11 shows the transfer characteristics obtained for silicon-germanium channel PFET with length and width each $1\mu m$ at different temperatures when $V_{DS} = -50mV$ is applied and V_{GS} is sweeped from $-1V$ to $0.3V$.

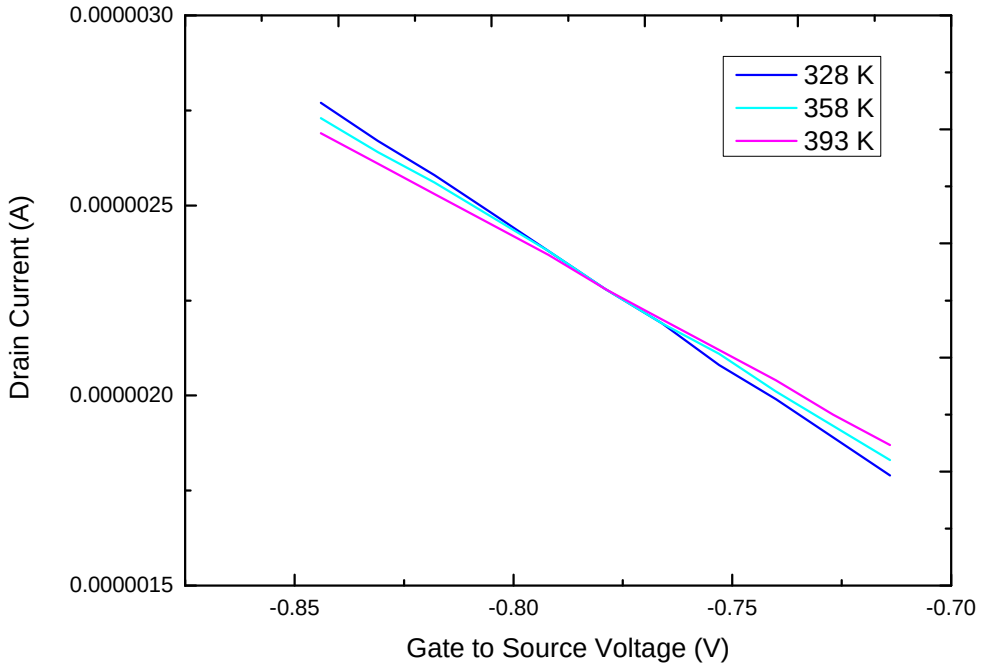

Fig. 3.11 I-V characteristics for PFET with $W = 1\mu m$, $L = 1\mu m$ at $V_{DS} = -50mV$ with temperature as a parameter

Figure 3.11 indicates the presence of a ZTC point at $V_{GS} = -0.78V$.

3.4.2 PFET with $W = 1\mu m$ and $L = 90nm$ at $V_{DS} = -50mV$

The transfer characteristics for silicon-germanium channel PFET with $W = 1\mu m$ and $L = 90nm$ at $V_{DS} = -50mV$ at different temperatures is plotted in figure 3.12. We can observe a ZTC point at $V_{GS} = -0.86V$.

3.4.3 PFET with $W = 1\mu m$ and $L = 30nm$ at $V_{DS} = -50mV$

Figure 3.13 shows the I-V characteristics for the device at various temperatures. We can observe a bottle neck of cross over around $V_{GS} = -0.87V$.

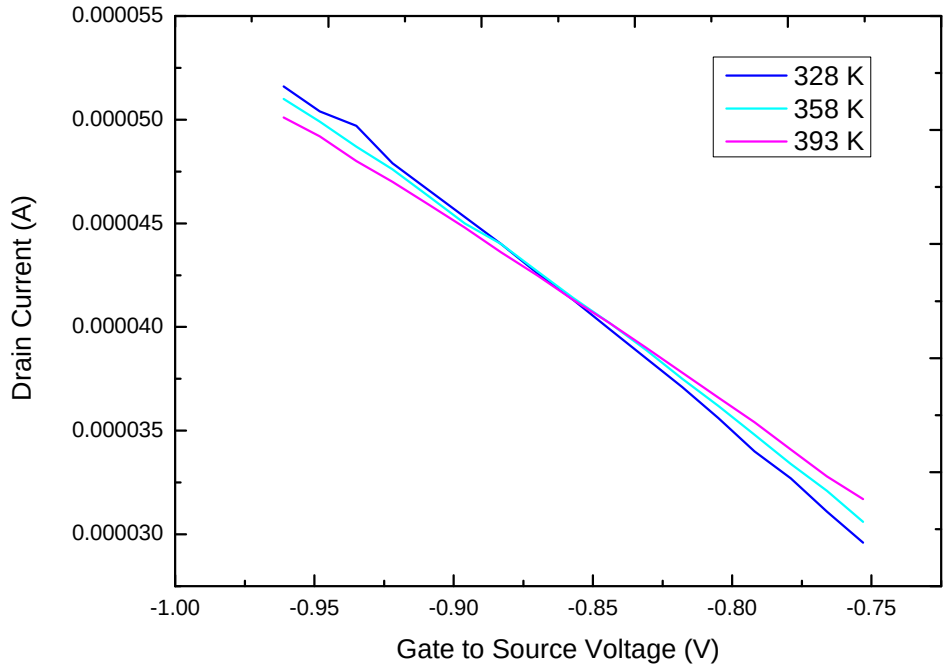

Fig. 3.12 I-V characteristics for PFET with $W = 1\mu m$, $L = 90nm$ at $V_{DS} = -50mV$ with temperature as a parameter

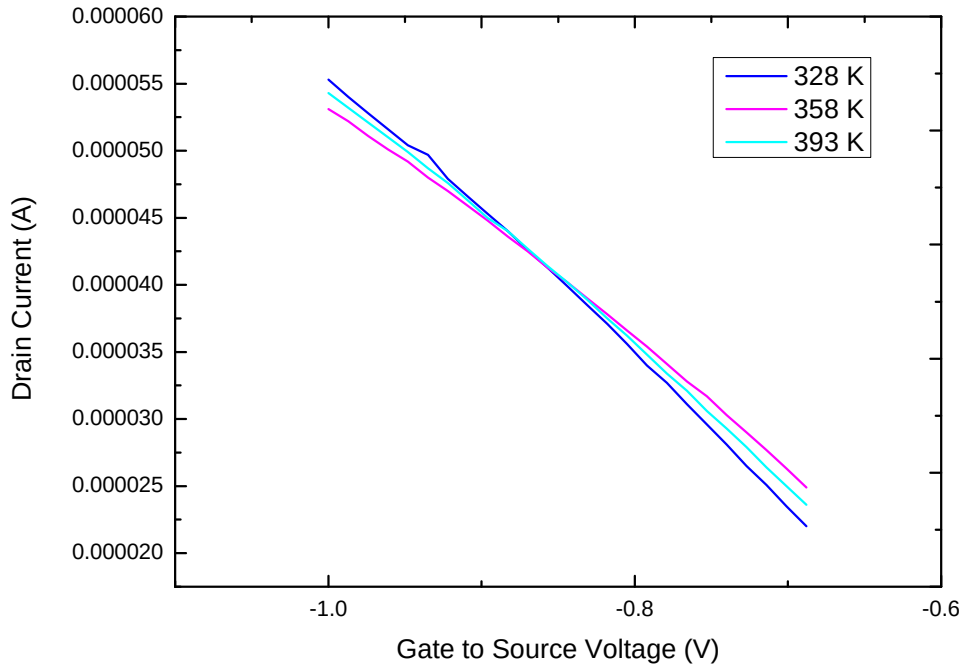

Fig. 3.13 I-V characteristics for PFET with $W = 1\mu m$, $L = 30nm$ at $V_{DS} = -50mV$ with temperature as a parameter

3.4.4 PFET with $W = 1\mu m$ and $L = 1\mu m$ at $V_{DS} = -1V$

The transfer characteristics for silicon-germanium channel PFET with length and width each $1\mu m$ at different temperatures has been plotted in figure 3.14.

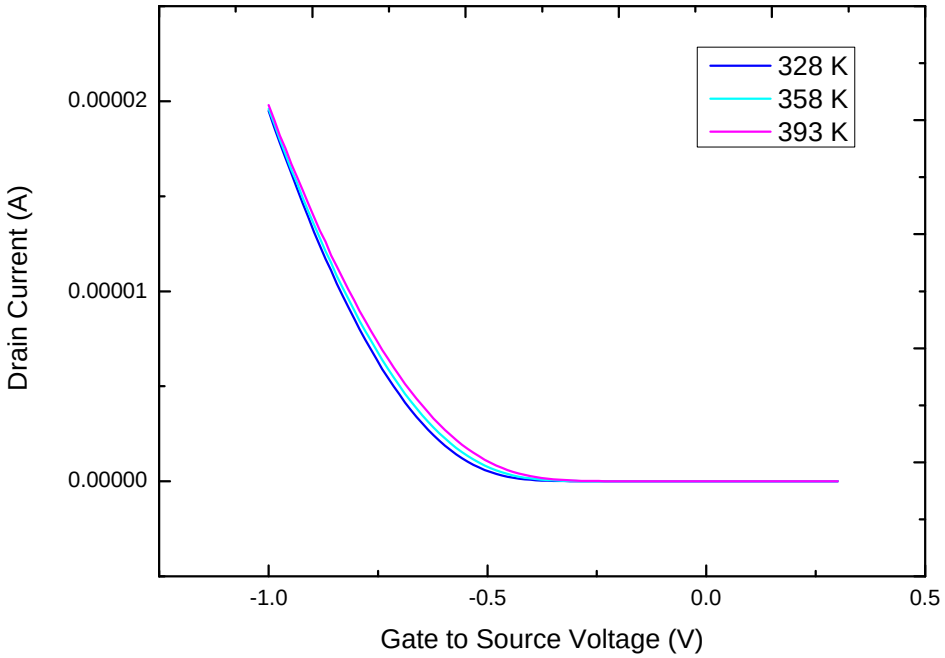

Fig. 3.14 I-V characteristics for PFET with $W = 1\mu m$, $L = 1\mu m$ at $V_{DS} = -1V$ with temperature as a parameter

Figure 3.14 has been replotted in figure 3.15 by narrowing down the range of gate to source voltage for better visibility.

From figure3.14 and figure 3.15, it is clear that, even though the transfer curves at different temperatures tend to cross over, they don't have a common point as in the other cases presented before and hence zero temperature coefficient(ZTC) point doesn't exist for the device under test at saturation region.

3.4.5 PFET with $W = 1\mu m$ and $L = 90nm$ at $V_{DS} = -1V$

The transfer characteristics for silicon-germanium channel PFET with $W = 1\mu m$ and $L = 90nm$ at $V_{DS} = -1V$ at different temperatures is plotted in figure 3.16. As in the case of PFET with $L = 1\mu m$, this device with length $90nm$ doesn't have a zero temperature coefficient(ZTC) point when biased at saturation region.

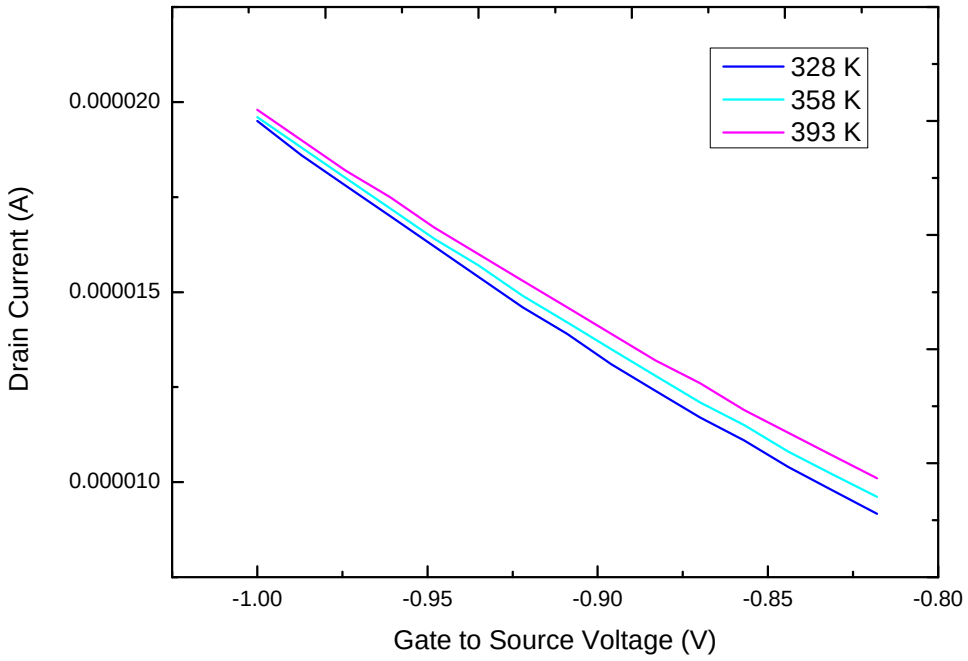

Fig. 3.15 Rescaled I-V characteristics for PFET with $W = 1\mu m$, $L = 1\mu m$ at $V_{DS} = -1V$ with temperature as a parameter

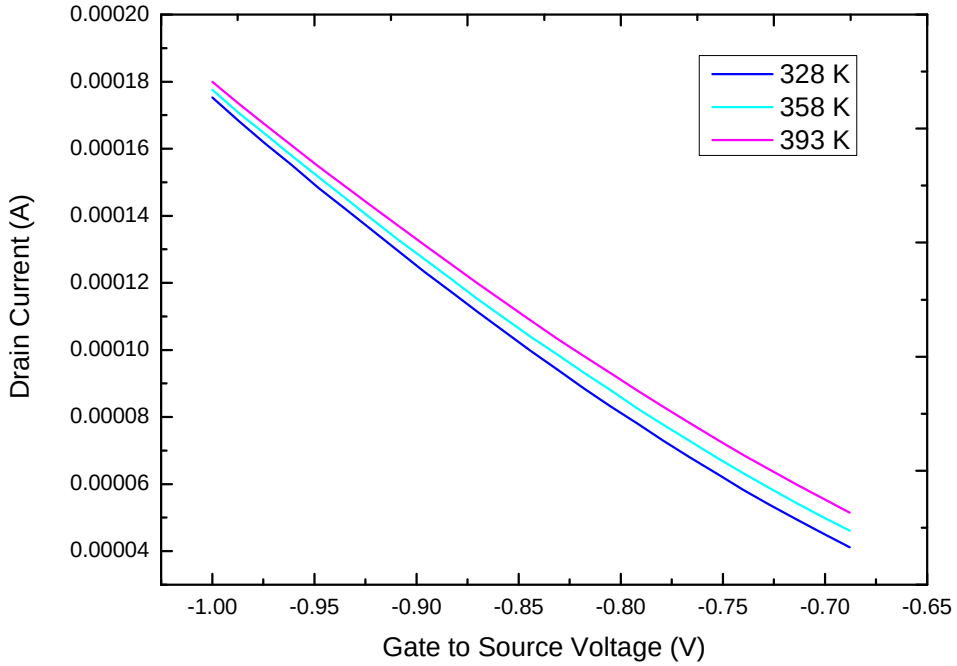

Fig. 3.16 I-V characteristics for PFET with $W = 1\mu m$, $L = 90nm$ at $V_{DS} = -1V$ with temperature as a parameter

3.4.6 PFET with $W = 1\mu m$ and $L = 30nm$ at $V_{DS} = -1V$

Figure 3.13 shows the I-V characteristics for the device at various temperatures.The plot indicates that zero temperature coefficient(ZTC) point doesn't exist for shorter channel devices too in saturation region.

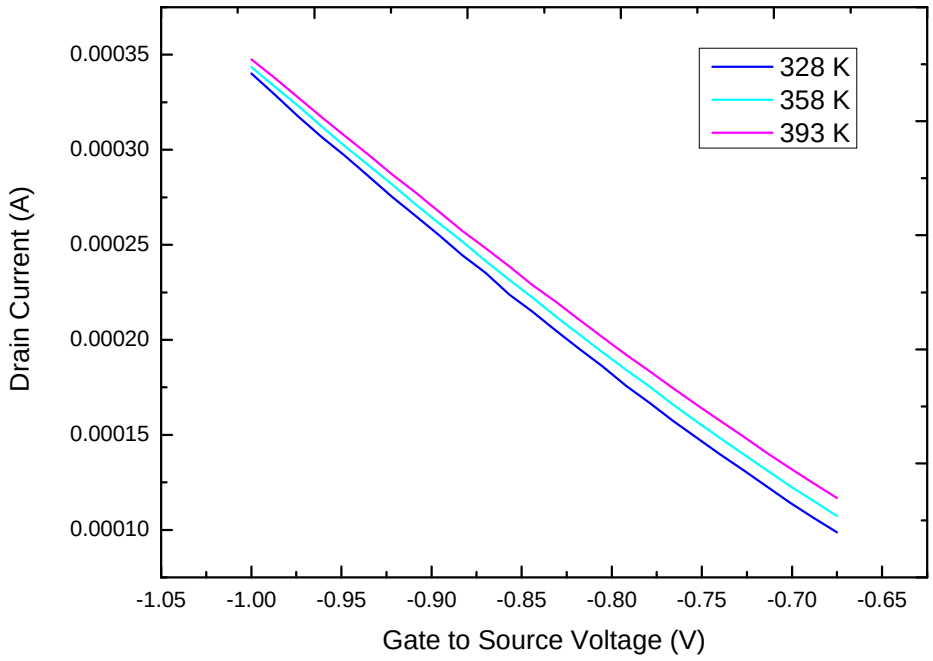

Fig. 3.17 I-V characteristics for PFET with $W = 1\mu m$, $L = 30nm$ at $V_{DS} = -1V$ with temperature as a parameter

3.5 Results and Discussion

In this chapter, I_D versus V_{GS} characteristics for silicon channel NFETs and silicon-germanium channel PFETs are plotted for both linear and saturation regions at different temperatures. Table 5.1 contains the gate to source voltages to be applied to bias the silicon channel NFET devices at zero temperature coefficient(ZTC) points for their respective lengths. V_{GS} corresponding to ZTC points has been plotted against length of NFETs in log scale in figure 3.18 and figure 3.19 for $V_{DS} = 50mV$ and $V_{DS} = 1V$ respectively.

From table 3.1 and figures 3.18 and 3.19, we can infer the following:

Length	V_{GS} at ZTC point for $V_{DS} = 50mV$	V_{GS} at ZTC point for $V_{DS} = 1V$
$1\mu m$	0.625	0.810
$90nm$	0.70	0.84
$30nm$	0.790	0.95

Table 3.1 ZTC points at for silicon channel NFET devices with different lengths

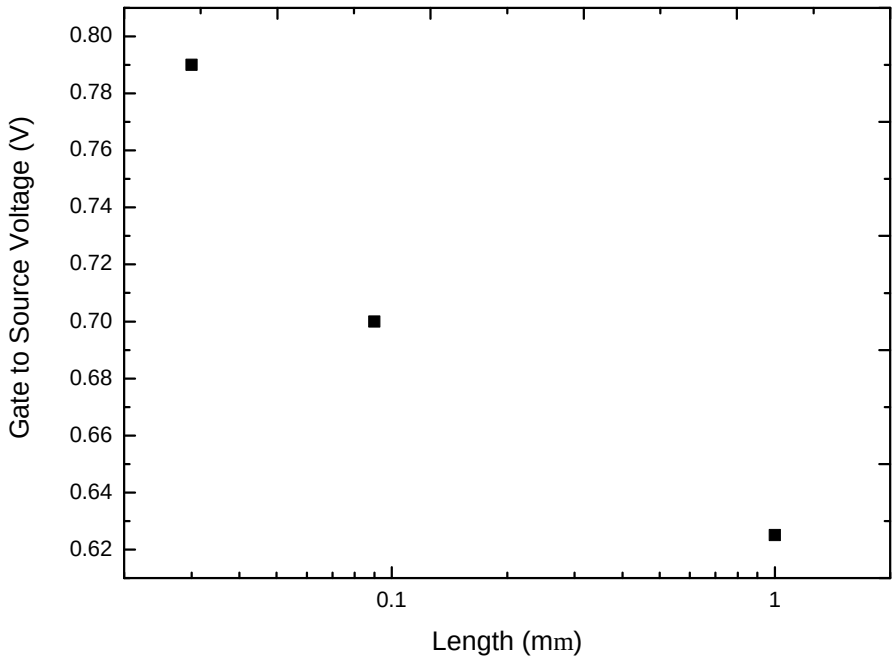

Fig. 3.18 ZTC bias points for NFET devices plotted against length of the device when $V_{DS} = 50mV$

- We observe that zero temperature coefficient (ZTC) point exists for silicon channel NFET devices when biased at linear region. This indicates the mutual compensation of temperature variations of threshold voltage and mobility.
- For saturation region too, zero temperature coefficient (ZTC) points exist. It can be noted that V_{GS} value at ZTC point for saturation region for a device of certain length is higher than the V_{GS} value at ZTC point for linear region.
- As we zoom in the I-V characteristics at different temperatures, we can see that there may be minute differences in intersection points of each curve. Figure 4.20 shows the rescaled version of transfer characteristics ate different temperatures for NFET with $W = 1\mu m$ an $L = 1\mu m$. We can see that the I-V curves at different temperatures cross over in a bottle neck ranging from $V_{GS} = 0.622$ to $V_{GS} = 0.627$. This must be because of the variation in the value of α_μ from -1, which is the ideal figure for perfect compensation of temperature effects of mobility and threshold voltage.
- Figure 4.21 shows the rescaled plot for NFET in saturation region. Here, the range of cross over varies from $0.87V$ to $0.98V$, which is much broader compared to the

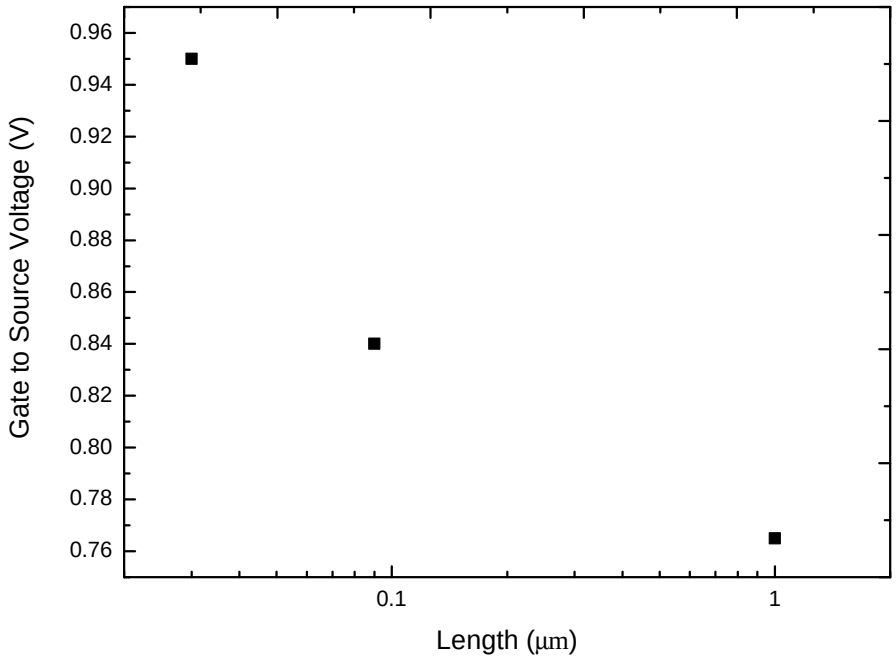

Fig. 3.19 ZTC bias points for NFET devices plotted against length of the device when $V_{DS} = 1V$

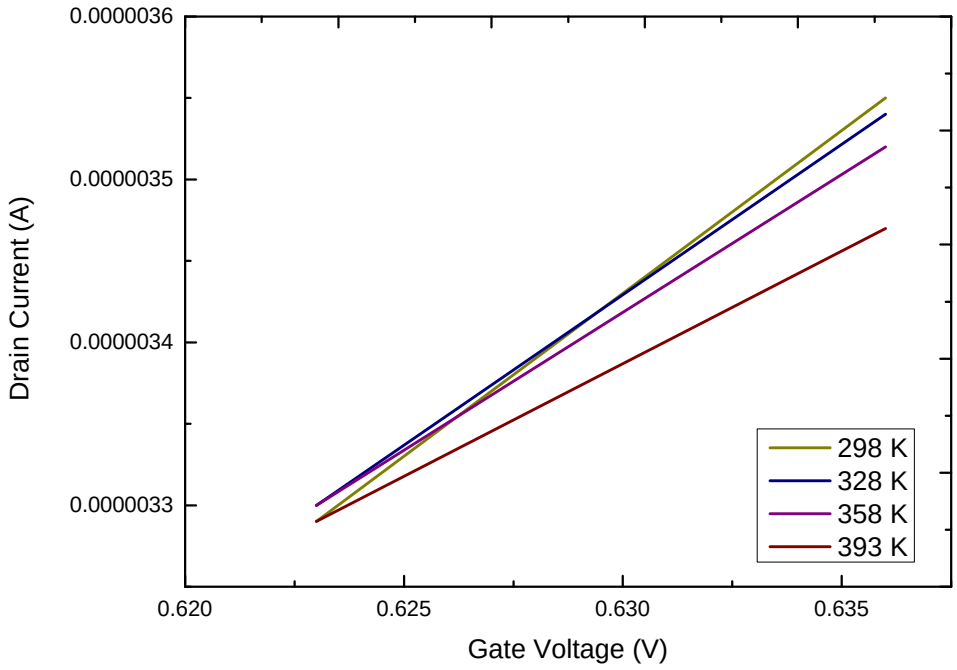

Fig. 3.20 Rescaled I-V characteristics showing a bottleneck of ZTC points in Si channel nMOSFETs for $V_{DS} = 50mV$

Length	V_{GS} at ZTC point for $V_{DS} = -50mV$	V_{GS} at ZTC point for $V_{DS} = -1V$
$1\mu m$	-0.78	-
$90nm$	-0.825	-
$30nm$	-0.86	-

Table 3.2 ZTC points at for silicon-germanium channel PFET devices with different lengths

range we onserved in figure 4.20. The reason may be that the practical value of α_μ may be much different from ideal value of -2.

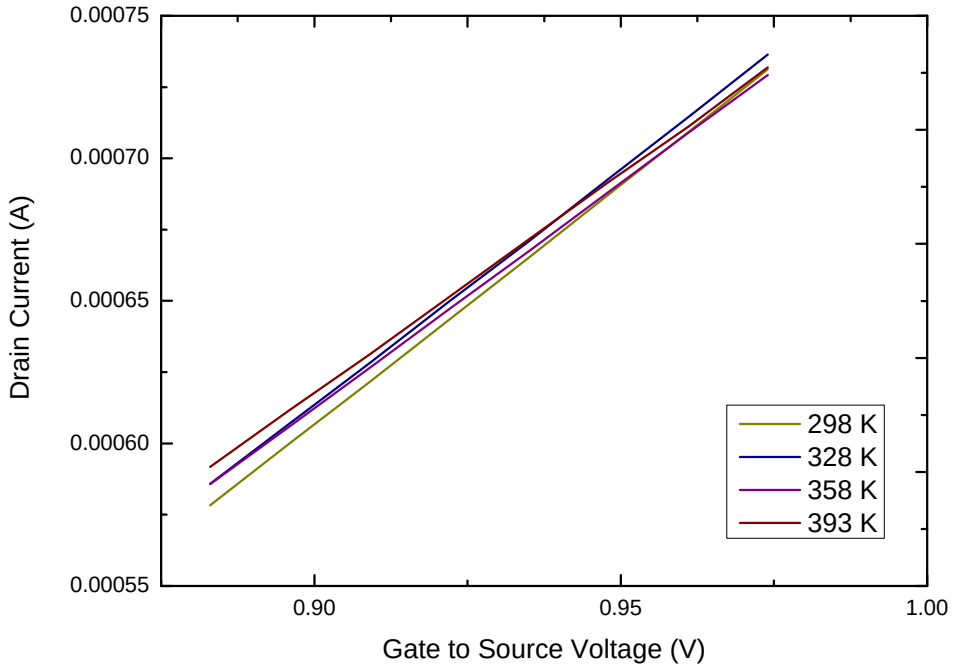

Fig. 3.21 Rescaled I-V characteristics showing a bottleneck of ZTC points in Si channel nMOSFETs for $V_{DS} = 50mV$

- The plots clearly indicate that V_{GS} at ZTC bias points decreases as the channels become shorter.

Table 3.2 refers to the gate to source bias points at zero temperature coefficient (ZTC) points for PFET devices for both linear and saturation regions. In figure 3.22, the ZTC bias points are plotted against length.

Following conclusions can be made from table 5.2 and figure 3.22

- Zero temperature coefficient (ZTC) points exist for silicon-germanium channel PFET devices when biased in linear region($V_{DS} = -50mV$), which indicates the mutual compensation of temperature effects of threshold voltage and mobility.

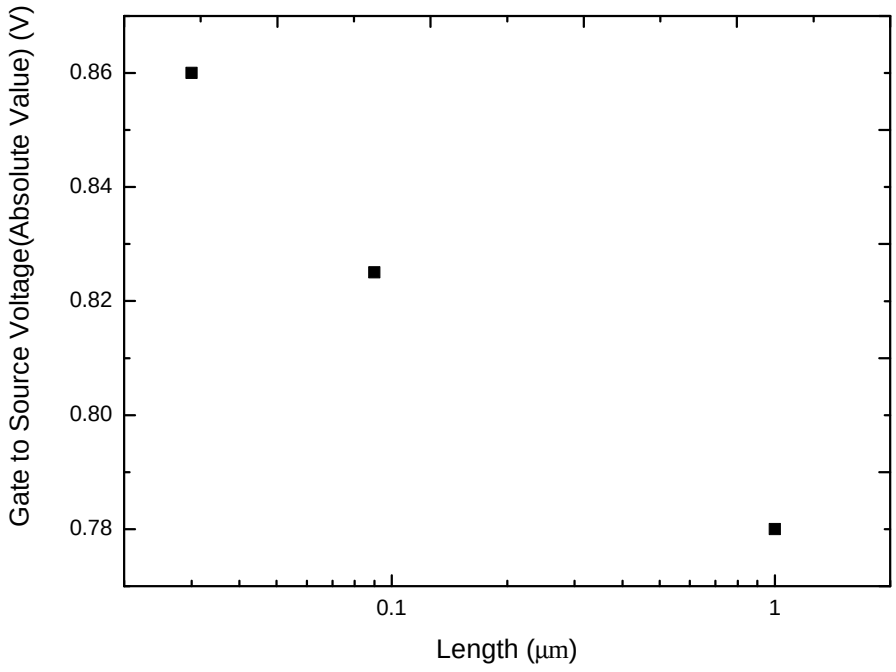

Fig. 3.22 ZTC bias points for PFET devices plotted against length of the device when $V_{DS} = -50mV$

- When these devices are biased in saturation region(i.e, $V_{DS} = -1V$), even though the curves tend to cross over, it doesn't happen for devices of any length. Hence ZTC points don't exist when biased in saturation region.
- For shorter channels, the gate to source bias for ZTC points become more and more negative.

CHAPTER 4

The Temperature Dependences of Threshold Voltage and Mobility

As we discussed in chapter 1, the origin of existence of zero temperature coefficient (ZTC) points, which are observed through experimental results in chapter 3 is due to the mutual compensation of temperature dependences of both threshold voltage as well as mobility. In this chapter, we explore the temperature dependence of both threshold voltage and mobility and try to assert the exact reasons for existence of zero temperature coefficient (ZTC) points for devices under test.

4.1 Temperature dependence of Threshold Voltage

The threshold voltage is an important parameter for MOSFET modeling and characterization. As we mentioned earlier, literature suggests that threshold voltage of transistors shows linear dependency on temperature. The temperature dependence of threshold voltage is usually given as

$$V_T(T) = V_T(T_0) + \alpha_{VT}(T - T_0) \tag{4.1}$$

Here, it is assumed that α_{VT} is temperature independent. Normally, the value of α_{VT} vary from $-1mV/^oC$ to $-4mV/^oC$ [15]. α_{VT} is an extracted parameter in BSIM model [16]. The threshold voltage increases with decreasing temperature. For an n-channel MOSFET, threshold voltage V_T can be given as

$$V_T = -(E_G/2q) + \phi_s + \frac{1}{C_{ox}}[4q\varepsilon_{Si}N_A\phi_s]^{1/2} \tag{4.2}$$

Here E_G is the energy gap, ϕ_s is the potential difference between the Fermi level and the intrinsic level, ε_{Si} is the silicon dielectric constant and N_A is the channel doping concentration. The increase of threshold voltage at low temperatures result from increase of ϕ_s and E_G [15].

Temperature(^oC)	Threshold Voltage(V)
25	0.4062
55	0.3874
85	0.3671
120	0.3432

Table 4.1 Threshold voltages at different temperatures for n-channel MOSFET with $L = 1\mu m$

4.2 Determination of threshold voltage from I-V characteristics

Various methods are used to calculate threshold voltage from $I_D - V_{GS}$ characteristics. Essentially, threshold voltage can be understood as gate voltage value at which the transition between weak and strong inversion takes place in MOSFET channel.Here, Constant-current method has been employed to calculate the threshold voltage [17].

Constant-current method evaluates threshold voltage as the value of the gate voltage V_G corresponding to a given arbitrary constant drain current I_D. This method is widely used because of its simplicity, the threshold voltage can be determined quickly with only one voltage measurement.For the n-channel silicon channel MOSFET we have,

$$I_D = 300\left(\frac{W}{L}\right)nA\Big|_{V_{GS}=V_T} \tag{4.3}$$

And for the p-channel silicon-germanium MOSFET, we use the following equation to evaluate the threshold voltage using CC method.

$$I_D = 70\left(\frac{W}{L}\right)nA\Big|_{V_{GS}=V_T} \tag{4.4}$$

4.3 Experimental Results and Discussions

The threshold voltages of n-channel MOSFETs have been measured for transistor width of $1\mu m$ and for lengths $1\mu m$,$90nm$ and $30nm$. Figure 4.1 gives us an idea about the the variation of threshold voltage with temperature. For n-channel devices, threshold voltage decreases with an increase in temperature, which is in tandem with equation 4.1. As expected, α_{VT} is negative and figure 4.1 suggests that α_{VT} can be approximated

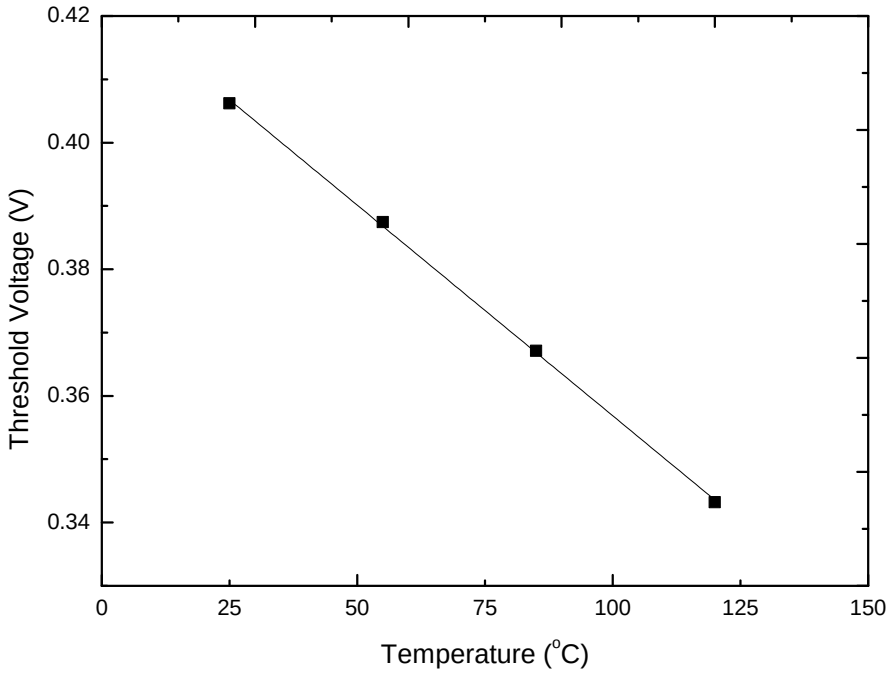

Fig. 4.1 Temperature Dependence of threshold voltage of the n-channel device with $L = 1\mu m$

to a constant.

Figure 4.2 shows the threshold voltage evaluated using constant current method for NFET devices of lengths $1\mu m$, $90nm$ and $30nm$ plotted against the temperature. We can observe that the threshold voltages of NFET devices increase as the channel lengths become shorter. As mentioned, for all the three lengths, the threshold voltage versus temperature curve can be approximated as a straight line and the value of α_{VT} corresponds to the slope of approximated straight line. In figure 4.1, the data points at four temperatures have been fitted to a straight line. The slope of line, which is equivalent to α_{VT} is $-6.6519 * 10^{-4}$.

In figures 4.3 and 4.4, the threshold voltage calculated at different temperatures are plotted for n-channel devices with lengths $90nm$ and $30nm$ respectively.The data points on the plots have been fitted to straight lines in both the cases.

Table 4.2 shows the extracted α_{VT} for different channel lengths by approximating the variation of threshold voltage with respect to temperature as linear. We can conclude that α_{VT}, the temperature coefficient of threshold voltage almost remains constant at $-0.6\, mV/^oC$.

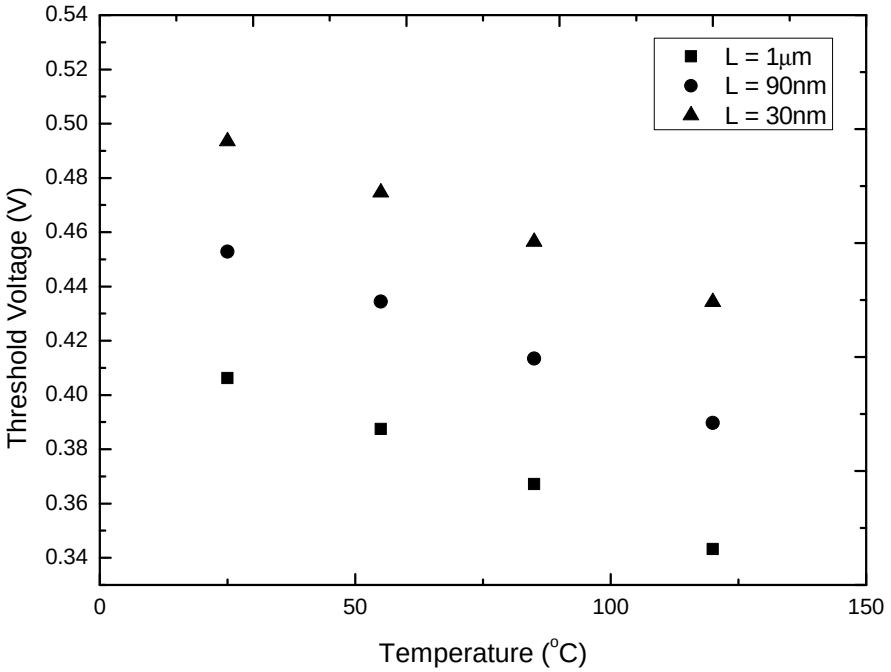

Fig. 4.2 Temperature Dependence of threshold voltage of the n-channel device

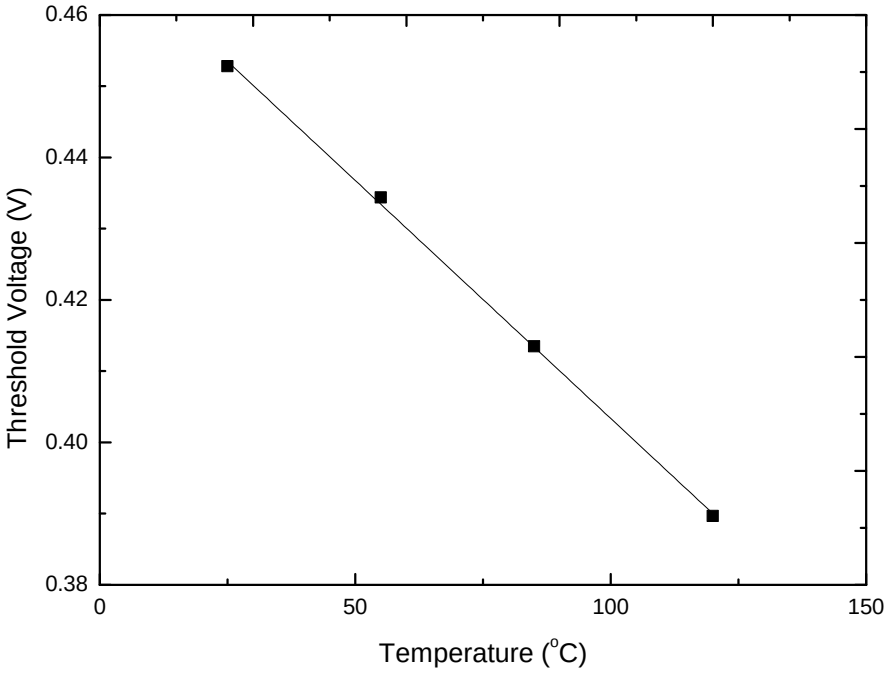

Fig. 4.3 Temperature Dependence of threshold voltage of the n-channel device with $L = 90nm$

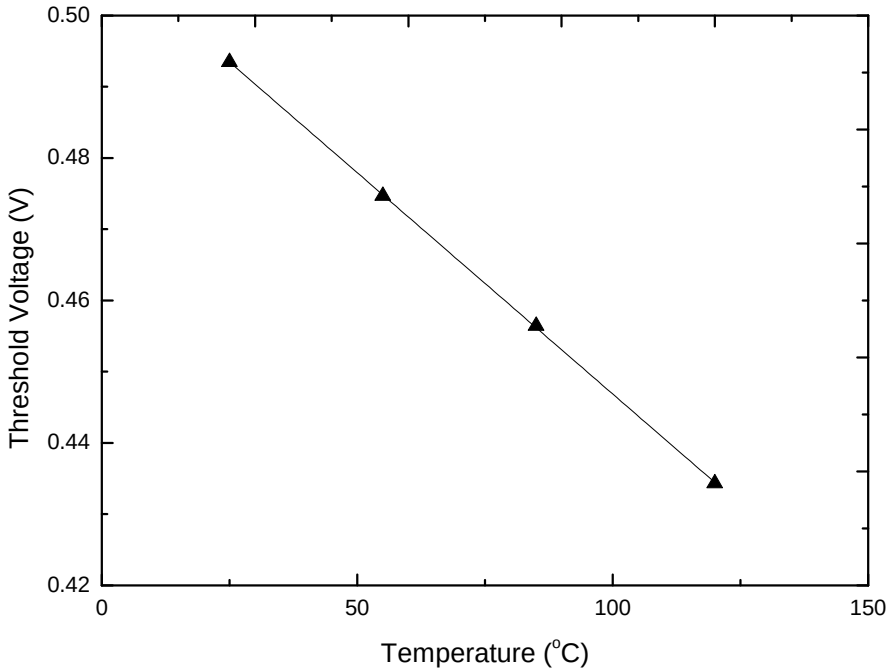

Fig. 4.4 Temperature Dependence of threshold voltage of the n-channel device with $L = 30nm$

Length of the device	α_{VT} extracted from linear fit models
$1\mu m$	$-6.6519 * 10^{-4}$
$90nm$	$-6.6809 * 10^{-4}$
$30nm$	$-6.62099 * 10^{-4}$

Table 4.2 Extracted α_{VT} for devices with different channel lengths

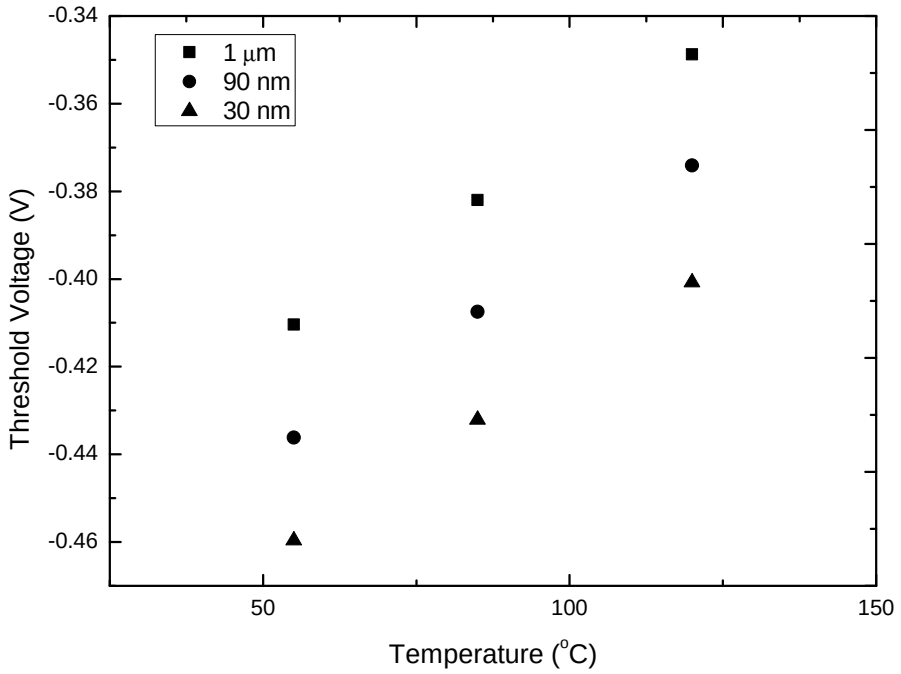

Fig. 4.5 Temperature Dependence of threshold voltage of p-channel devices

Length of the device	α_{VT} extracted from linear fit models
$1\mu m$	$9.4771 * 10^{-4}$
$90nm$	$9.5530 * 10^{-4}$
$30nm$	$9.0433 * 10^{-4}$

Table 4.3 Extracted α_{VT} for p-channel devices with different channel lengths

Now, in figure 4.5, threshold voltage calculated using constant-current method is plotted against temperature for silicon-germanium channel PFETs of lengths $1\mu m$, $90nm$ and $30nm$. We can infer that the threshold voltage become less negative as temperature increases for devices of particular length. Also, at a particular temperature, threshold voltages become more negative for shorter channel PFETs, which is evident from equation 4.1.

In figures 4.6, 4.7 and 4.8, the threshold voltage versus temperature plots for p-channel devices of length $1\mu m$, $90nm$ and $30nm$ respectively are fitted in to a straight line. The slope of these straight lines will give the temperature coefficient of threshold voltage and the extracted values of α_{VT} for all channel lengths are given in table 4.3.

As mentioned before, literature review suggests that the value of α_{VT} normally vary from $-1\ mV/^oC$ to $-4\ mV/^oC$. One of the key points to note here is that the values

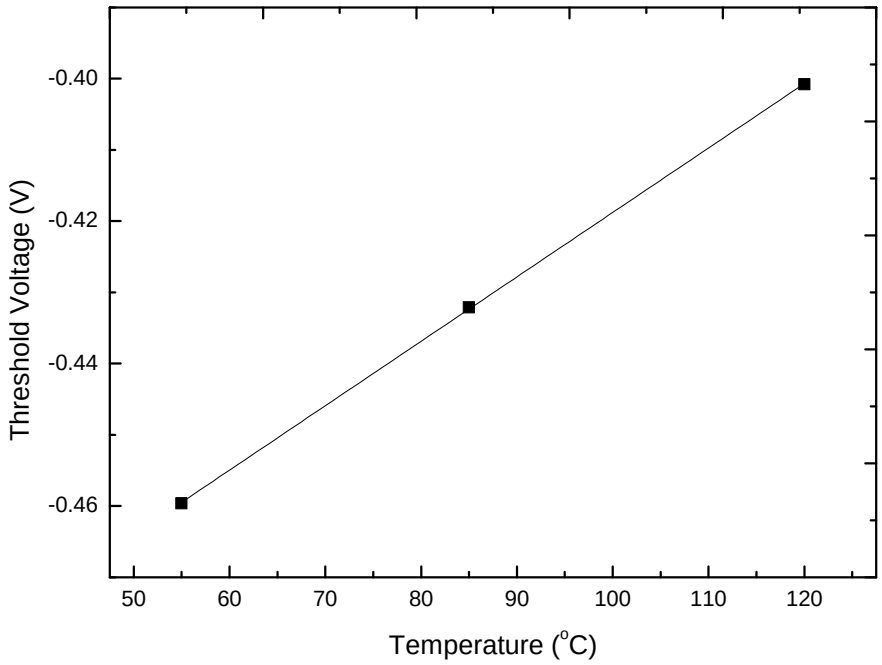

Fig. 4.6 Temperature Dependence of threshold voltage of the p-channel device with $L = 1\mu m$

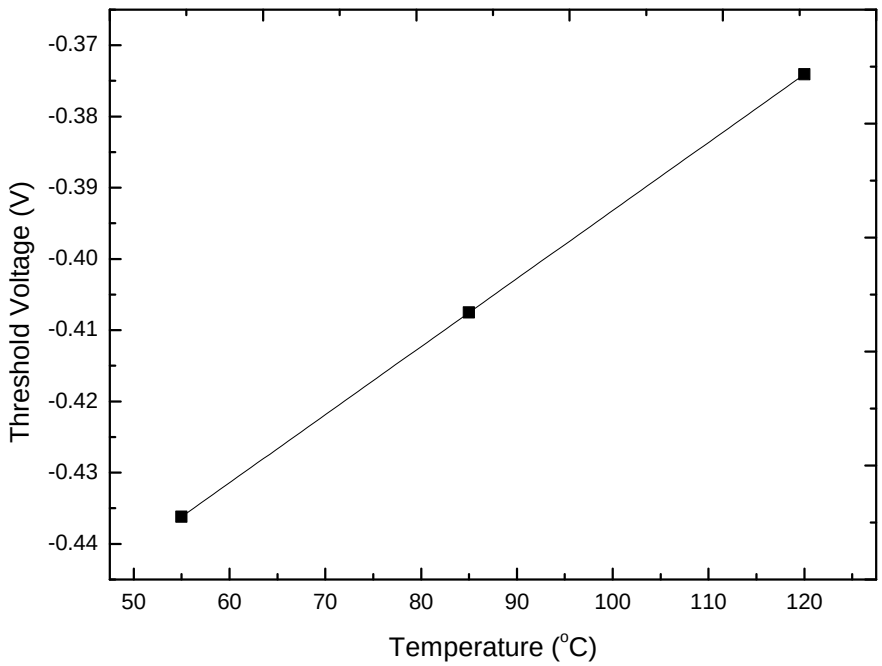

Fig. 4.7 Temperature Dependence of threshold voltage of the p-channel device with $L = 90nm$

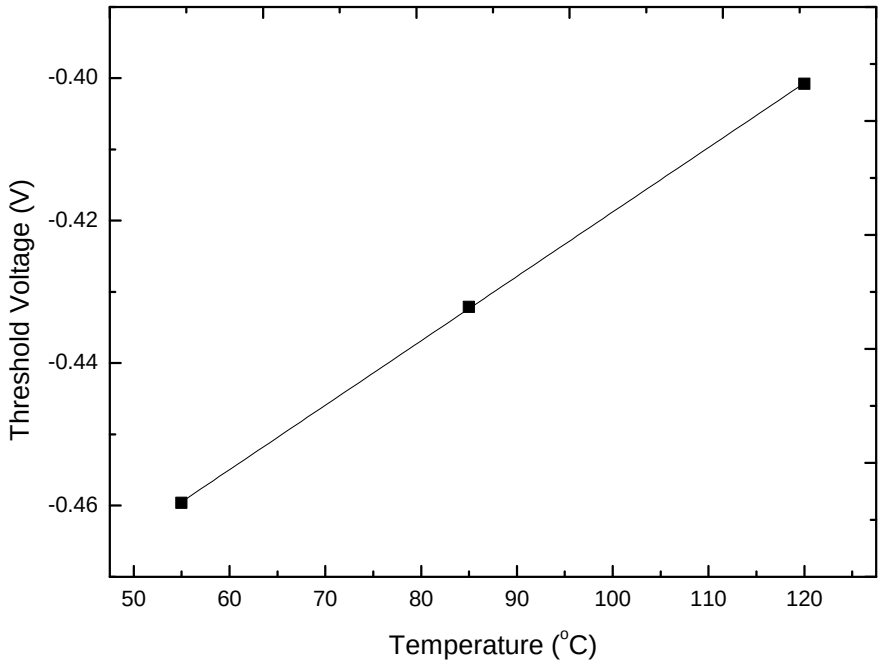

Fig. 4.8 Temperature Dependence of threshold voltage of the p-channel device with $L = 30nm$

of α_{VT} for NFETs and PFETs are around $-0.6\ mV/^oC$ and $0.9\ mV/^oC$, which are of one order of magnitude less than the expected values as per literature. Also, the thermal coefficient of threshold voltage seems to be channel length independent.

4.4 Extraction of Mobility from C-V and I-V characteristics

As explained in chapter 2, the temperature dependence of mobility is given by

$$\mu_n(T) = \mu_n(T_0)(T/T_0)^{\alpha_\mu} \tag{4.5}$$

To explain the existence of zero temperature coefficient (ZTC) point, it is very important to extract the dependence of mobility on temperature and find its correlation with temperature dependence of threshold voltage. The parameter α_μ is considered independent on temperature [18]. The most frequent figure used for α_μ is -1.5 [4]. This figure comes from the assumption that the acoustic phonon interaction is the dominant

scattering mechanism, which is given by

$$\mu_a = (m_e)^{-5/2} T^{-3/2} \tag{4.6}$$

where m_e is the conductivity effect mass. Hence $\alpha_\mu = -1.5$ is valid when this scattering mechanism is dominant. But, we can't neglect the other doping mechanisms. As a result of additional mechanisms, the mobility decrease is not as it predicted in equation 4.5.

Let us consider an n-channel MOSFET of gate length L and width W. The drain to source current I_D can be expressed as

$$I_D = \frac{W \mu_{eff} Q_n V_{DS}}{L} - W \mu_{eff} \frac{kT}{q} \frac{dQ_n}{dx} \tag{4.7}$$

where μ_{eff} is the effective mobility (which has to be calculated), Q_n is the mobile channel charge density(C/cm^2) and V_{DS} is the source to drain voltage. The first term in equation 4.7 represents the drift component and the second term represents the diffusion component of drain current. Typically, effective mobility calculation are done at low drain voltage.At low drain voltage, we can approximate the mobile channel charge density, Q_n to be a constant and hence drop the diffusive component of drain current. Hence the drain current at low V_{DS} can be written as

$$I_D = \frac{W \mu_{eff} Q_n V_{DS}}{L} \tag{4.8}$$

From equation 4.8, we can solve for effective mobility and it gives

$$\mu_{eff} = \frac{I_D}{Q_n V_{DS}} \frac{L}{W} \tag{4.9}$$

We already have I_D from the measurements and we know V_{DS} too. So, we have to find Q_n to calculate the effective mobility.

A method suggested suggested to evaluate Q_n is from the measurement of gate-to-channel capacitance per unit area.

$$Q_n = \int_{-\infty}^{V_{GS}} C_{GC} dV_{GS} \tag{4.10}$$

where C_{GC} is the gate-to-channel capacitance measured and V_{GS} is the gate to source

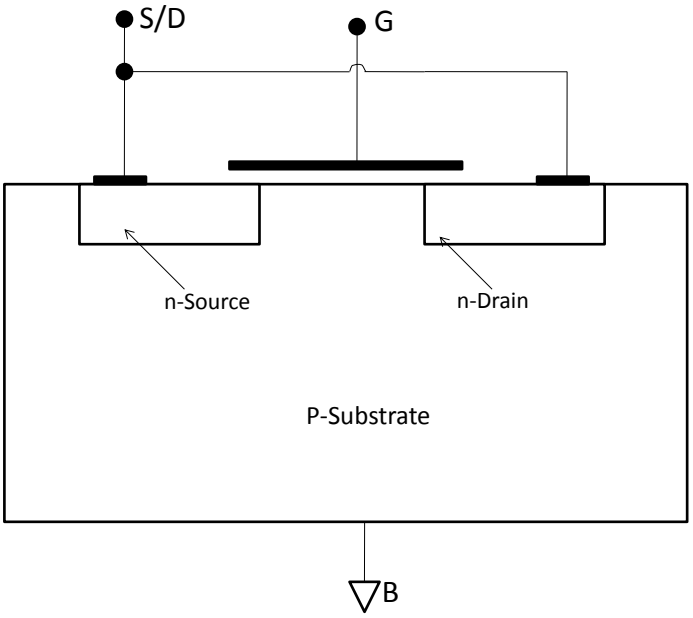

Fig. 4.9 Configuration for gate-to-channel capacitance measurement

voltage. The mobile channel charge density measurement technique is known as split C-V technique [19]. The method was originally proposed by Koomen to measure interface trapped charge density and the substrate doping density [20]. It was later adopted for mobility calculations.

C_{GC} can be measured using the set-up shown in figure 4.9 [19]. The source and drain terminals of the device are shorted and substrate terminal is grounded. The capacitance measurement unit (CMU) of the probe station is connected between the gate and the source-drain. When the gate voltage is negative, the channel is in accumulation region and the capacitance measured will be the capacitances due to overlapping between gate-source and gate-drain ($2C_{ov}$). The surface condition when negative gate-to-source voltage is applied is shown in detail in figure 4.10. When the gate voltage is greater than threshold voltage, the channel is inverted, and gate to channel capacitance as well as the two overlap capacitances are measured. The surface condition at this condition is shown in figure 4.11. C_{GC} versus V_{GS} curve obtained is shown in figure 4.12.

Subtracting $2C_{ov}$ from figure 4.12 and integrating with respect to gate voltage gives us the variation of mobile channel charge density with the gate to source voltage, which is shown in figure 4.13.

We already have the I_D - V_{GS} measurements and now using equation 4.9, we can ex-

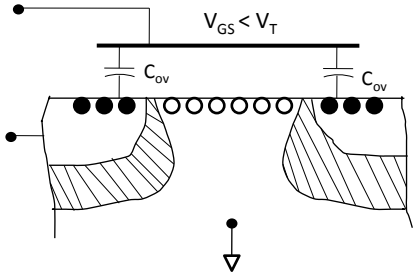

Fig. 4.10 Surface conditions for gate-to-channel capacitance measurements for $V_{GS} < V_T$

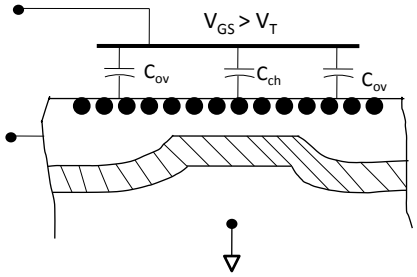

Fig. 4.11 Surface conditions for gate-to-channel capacitance measurements for $V_{GS} > V_T$

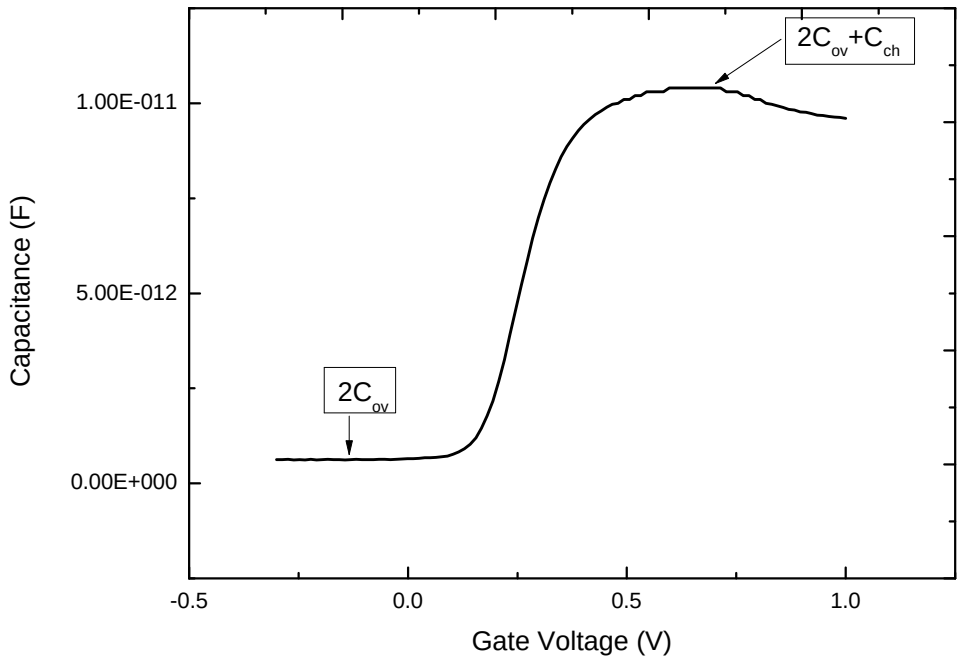

Fig. 4.12 Measured capacitance plotted against the gate-to-source voltage value

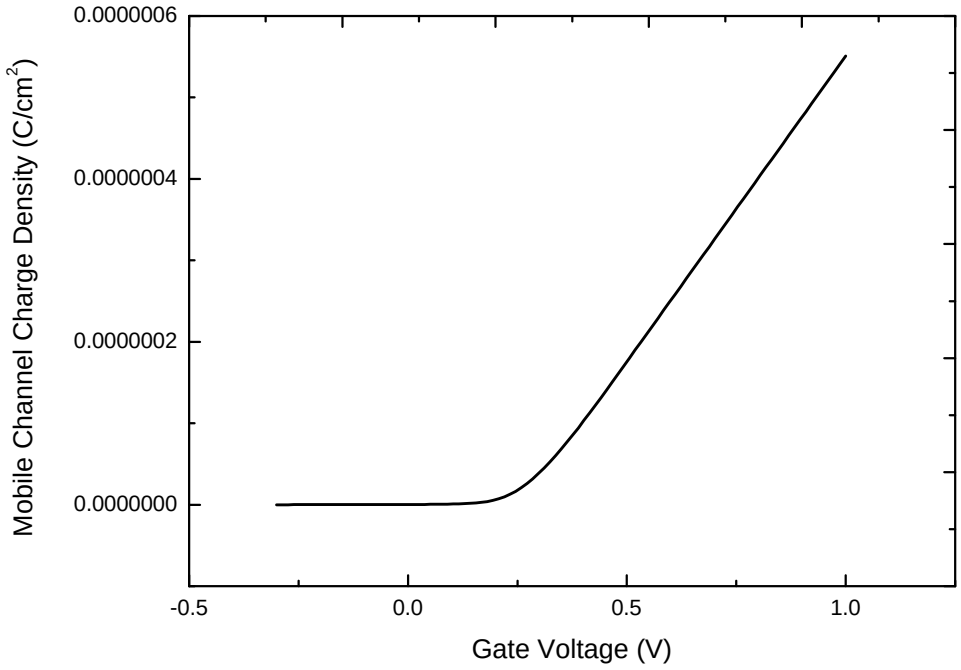

Fig. 4.13 Mobile channel charge density versus Gate Voltage obtained by integrating channel capacitance

tract mobility for each V_{GS}. Since we are sweeping both current as well as capacitance against the gate to source voltage, we used numerical integration technique to calculate effective mobility at each V_{GS} for which current and capacitance are measured.

4.5 Sources of error in mobility measurement technique

Even though we can determine the mobility using equation 4.9 and 4.10, there are certain sources of error in the method suggested. In figure 4.9 we have depicted the configuration for measuring C_{GC} for different values of V_{GS}. It is clear that $V_{DS} = 0$ at this configuration, but for measuring drain current, we have to apply a certain value of V_{DS}. Non zero V_{DS} introduces an error in effective mobility calculation when V_{GS} is close to threshold voltage, because Q_n reduces as V_{DS} is increased for a given V_{GS} [21]. A good way to reduce this error is to take I_D measurements at lower values of V_{DS}. One of the basic and fundamental assumptions we made for this approach is that the inversion carriers have a uniform concentration across the entire channel under a small bias. However, whenever there is a drain bias, non uniformity in inversion carrier

density exists. This non uniformity even get worse as V_{DS} increases. Also, as the error in assumption increases as the device dimensions are scaled.

Two methods can be used to counter this error. Based on above understanding, the error in mobility extraction is due to the non uniform distribution of inversion charge in the channel existing because of the non zero V_{DS} applied while measuring drain current. In the first approach to counter this error, we can have current measurements at different values of V_{DS} and have mobility extracted from those measurements subsequently at different values of V_{DS}. Later, the effective mobility versus V_{DS} curve can be extrapolated for $V_{DS} = 0$ and hence the error could be avoided.

An easier alternative is to measure current at V_{DS} of opposite polarities and use the average of the current values obtained to extract mobility. Inversion charge density at $V_{DS} = 0$ can be approximated using this technique [22].

Another source of error is introduced by assuming that the only contributor to the drain current is drift current, and diffusion current was ignored. Our assumption that $\frac{dQ_n}{dx} = 0$ may be a good approximation for V_{GS} well above threshold voltage, but diffusion current will become more prominent as the V_{GS} becomes closer to V_T. Also, in the sub threshold regions (i.e, $V_{GS} < V_T$), diffusion current is the prominent contributor for drain current. So care should be taken while extracting μ_{eff} and the mobility values at higher V_{GS} could only be considered for further calculations.

4.6 Step-by-Step procedure for mobility extraction

The exact steps followed for extracting mobility from the devices under experiment is enumerated below:

Step 1: Capacitance is measured using the capacitance measurement unit(CMU) of the Cascade Microtech Semi automatic probe station. A high frequency of $100KHz$ is used and capacitance values for the set up shown in figure is measured at different values of V_{GS}, incrementing from $-0.3V$ to $1V$.

Step 2: Figure 4.12 shows the obtained capacitance plot. The retrieved capacitance is in farads.Since we are measuring on a structure with $W = 5\mu m$ and $L = 5\mu m$ with 50 stripes, to convert it to capacitance per unit area, we divide the values measured by $5 * 5 * 50 * 10^{-8}$ after subtracting the overlapping capacitances, $2C_{ov}$, which is equal to the minimum value among measured capacitances.

Step 3: Now, the mobile channel charge density, Q_n is calculated at each V_{GS} via numerical integration of gate-to-channel capacitance per unit area(C_{ch}) obtained from step 2. We assume the Q_n for lowest voltage to be 0. We use the following expression to perform numerical integration.

$$Q_{n_m} = Q_{n_{m-1}} + [C_{ch_{m-1}} + C_{ch_m}] * \frac{V_{step}}{2} \tag{4.11}$$

where Q_{n_m} and $Q_{n_{m-}}$ represents the mobile channel charge densities at successive V_{GS} data points and $C_{ch_{m-1}}$ and C_{ch_m} are the gate-to-channel capacitances per unit area at successive V_{GS} data points. By this method, we evaluate Q_n for each V_{GS} at which current and capacitance measurements are carried out. Figure 4.13 shows the variation of Q_n with respected to V_{GS}, determined using equation 4.11.

Step 4: As mentioned above, V_{DS} has to be measured at lower values to reduce error. We choose $V_{DS} = \pm 50mV$, which is a reasonable value for I_D measurements. The average value of I_D, at $V_{DS} = 50mV$ and $V_{DS} = -50mV$ have been taken to use in mobility extraction equation 4.9.

Step 5: Effective mobility, μ_{eff} for each value of V_{GS} has been calculated using equation 4.9.

4.7 Experimental results obtained using mobility extraction technique

In this section, we discuss about the experimental results obtained by employing the method for mobility extraction described in the previous sections. Both C_{GC} - V_{GS} and I_D - V_{GS} measurements are taken at 25^oC, 55^oC, 85^oC and 120^oC. Effective mobility is extracted at all the above temperatures to study the temperature dependence of mobility.

Figure 4.14 shows the gate-to-channel capacitance sweeped against V_{GS} at different temperatures. From figure 4.14, the overlapping capacitance, $2C_{ov} \approxeq 620fF$. We subtract overlapping capacitance, convert the units to F/cm^2 by dividing by area and integrate it to obtain Q_n as described in steps 2 and 3.

Figure 4.15 shows the inversion charge density obtained. We can observe that more charge is inverted at higher temperatures.

Figure 4.16 shows the I_D - V_{GS} measured at different temperatures. Now, using steps 4 and 5, we determine the effective mobility.

The extracted mobility plotted against the V_{GS} values is shown in figure 4.17. As we

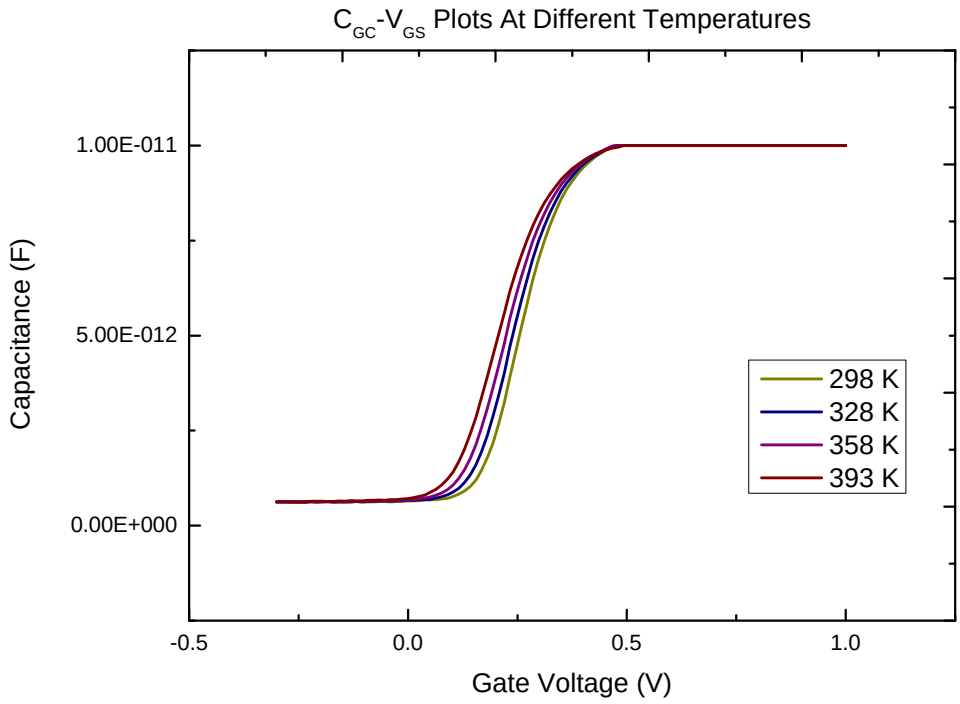

Fig. 4.14 Gate-to-channel capacitance versus Gate Voltage at different temperatures determined by Step 1

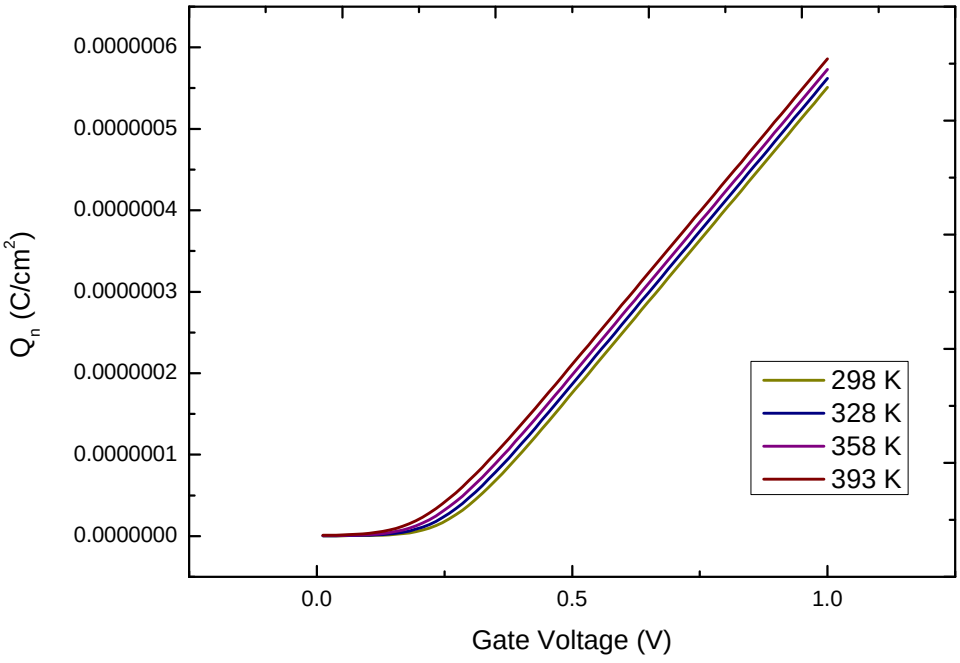

Fig. 4.15 Mobile channel charge density versus Gate Voltage at different temperatures determined by Step 1

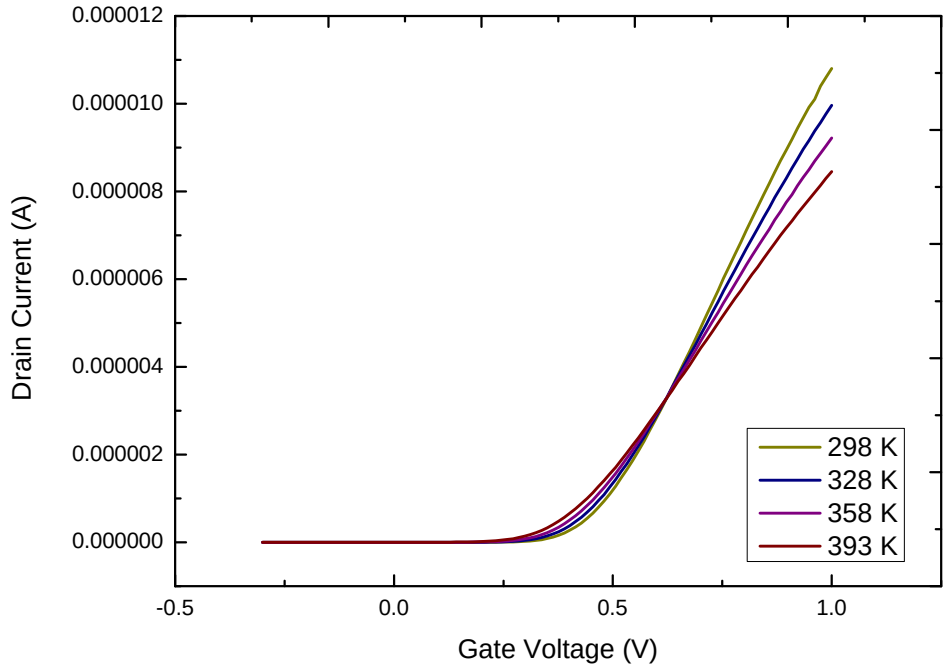

Fig. 4.16 I-V characteristics for NFET with $W = 1\mu m$, $L = 1\mu m$ at $V_{DS} = 50mV$ with temperature as a parameter

have mentioned the previous section, mobility at V_GS values closer to threshold voltage is not acceptable since diffusion current is prominent at those regions and our assumption that $\frac{dQ_n}{dx} = 0$ doesn't hold good. Hence we re-plot the μ_{eff} versus V_{GS} curve for higher values of V_{GS} for which our assumption holds good. Figure 4.18 shows the μ_{eff} versus V_{GS} plot.

4.8 Evaluation of α_μ from mobility-temperature dependence

Now, we need to evaluate the temperature dependence of mobility in the devices we have. Since the values of effective mobility for higher temperatures is more accurate due to above said reasons, we use μ_{eff} at $V_{GS} = 1V$ at temperatures 25^oC, 55^oC, 85^oC and 120^oC to assess the value of α_μ. Table 4.4 shows the values of effective mobility calculated at $V_{GS} = 1$ for different temperatures.

Mobility with a power law dependence on temperature is being used in a BSIM model

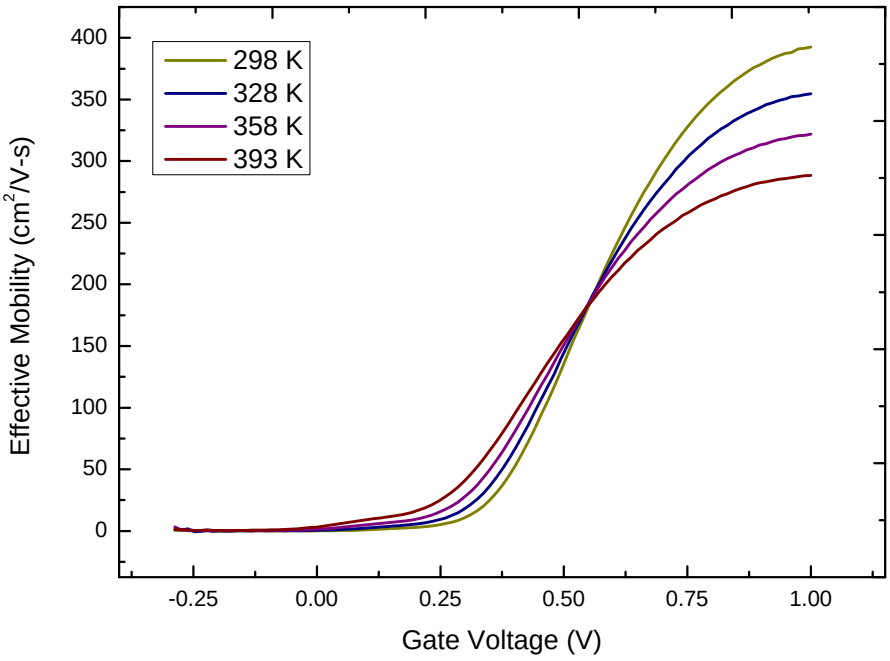

Fig. 4.17 Mobility plotted against gate-to-source voltage at different temperatures

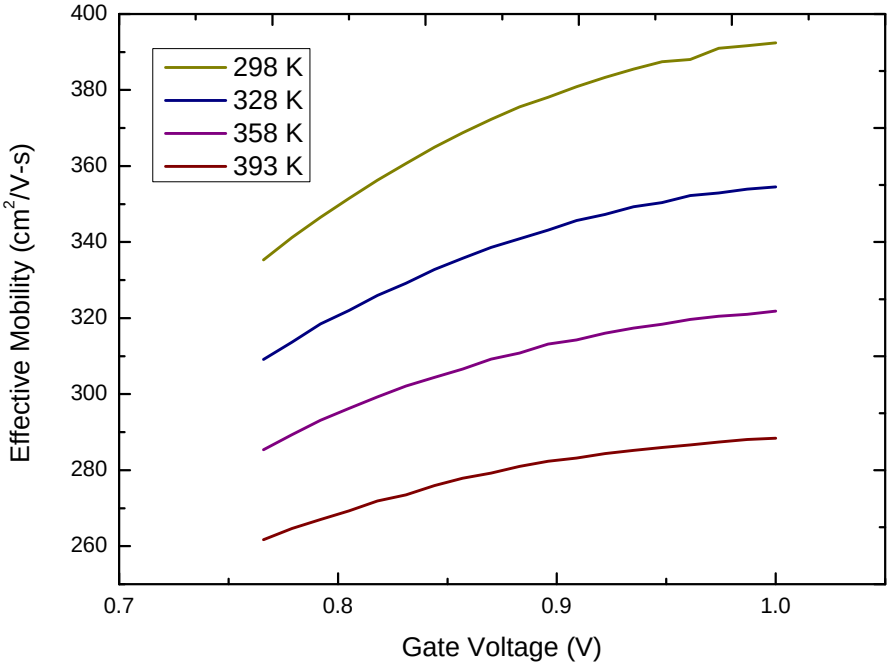

Fig. 4.18 Mobilty plotted against higher values of gate-to-source voltage at different temperatures, where $\frac{dQ_n}{dx} = 0$ is applicable

Temperature(^oC)	μ_{eff} at $V_{GS} = 1V$
25	392.43
55	354.55
85	321.80
120	288.383

Table 4.4 Effective mobility values calculated at different temperatures for n-channel device when $V_{GS} = 1V$

[16]. We can observe this dependence in equation 4.5. Using MATLAB curve fitting tool, the data in table 4.4 can be fitted in to the following expression:

$$\mu_{eff}(T) = 392.43(T/298)^{\alpha_\mu} \tag{4.12}$$

where reference temperature, $T_0 = 298K$ and $\mu(T_0) = \mu(298) = 392.43cm^2/Vs$. The mobility versus temperature data points, as well as the fitted curve generated using MATLAB Curve Fitting Tool are shown in figure 4.19.The value of α_μ as per the fitted curve is -1.093.

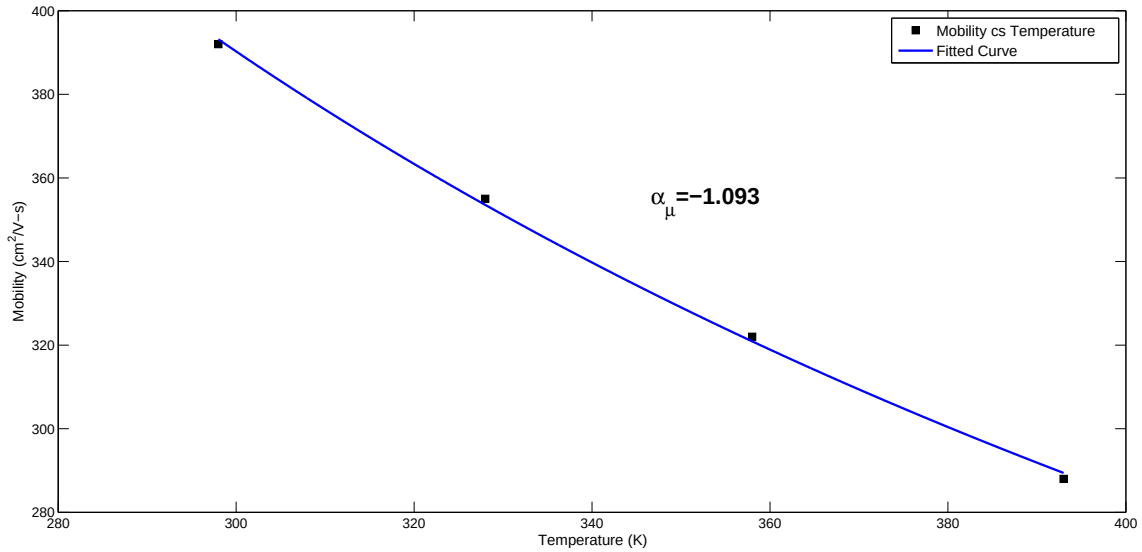

Fig. 4.19 Effective mobility at $V_{GS} = 1$ plotted against temperature

4.9 Reason for the Existence of Zero Temperature Coefficient (ZTC) point

As mentioned in chapter 2, if $\alpha_\mu = -1$, zero temperature coefficient (ZTC) points exist as a single value for linear region. As we have shown through the results obtained via experiments in chapter 3, in the devices under experiment, ZTC points don't exist as a single value, rather the cross over of I-V curves are confined to a small bottleneck. Figure 4.20 shows the explained behaviour. We have $\alpha_\mu = -1.093$, where as the expected value for existence of an ideal ZTC point is $\alpha_\mu = -1$. A little deviation of α_μ from its ideal of -1 explains the existence of this narrow bottle neck shown in figure 4.20. In figure 4.20, we can observe that the range of cross over of I-V curves at different temperatures vary from 0.622 to 0.627, which is quite a small range.

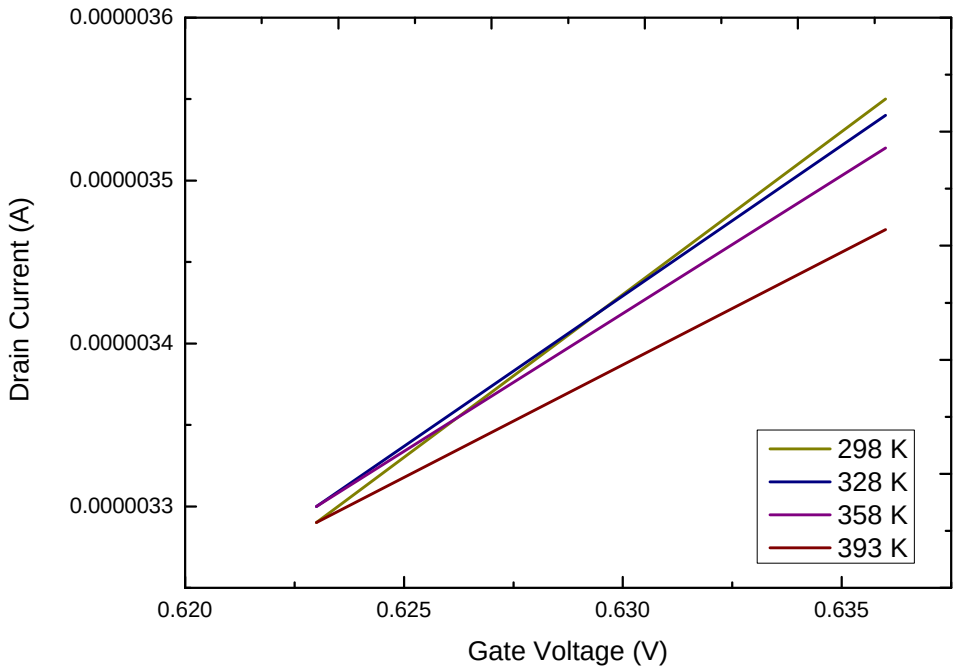

Fig. 4.20 Rescaled I-V characteristics showing a bottleneck of ZTC points

Figure 4.21 shows the rescaled $I_D - V_{GS}$ characteristics at different temperatures for n channel MOSFETs biased in saturation region. For existence of ZTC bias point in saturation region for nMOSFETs, the value of α_μ must be -2, which is not the case her. As we can observe, the bottle neck obtained here ranges from $0.88V$ to $0.99V$, which is very broad compared to the bottle neck region present for the same devices biased

in linear region. Analysis shows that the low value of α_{VT} too contribute towards the existence of zero temperature coefficient bottle neck region. Even though the practical value of α_μ is way from the ideal value of -1, the bottle neck seems to be narrow. Literature review suggested that the reported values of α_{VT} ranges from $-1mV/^oC$ to $-4mV/^oC$. But as given in table 4.2, the average value of α_{VT} for n-channel devices is $-0.6mV/^oC$, which is very low compared to those reported. In chapter 2, we have derived that if the drain current is not varying with temperature, then

$$V_{GS} = V_T(T_0) + \alpha_{VT} T_1 \left(1 + \frac{2}{\alpha\mu}\right) - \alpha_{VT} T_0 \tag{4.13}$$

We then came to the conclusion that,if $\alpha_\mu = -2$, the second term of equation 4.13 will become nullified and if this condition is met, the gate to source bias no longer depends on the current temperature T_1. So, the second term of equation 4.13 is the only term which depends on T_1. For the devices under experiment, α_{VT} is extremely low. Since $-1 < \alpha_\mu < 0$, $\left(1 + \frac{2}{\alpha\mu}\right) < 0$. So, the term $\alpha_{VT} T_1 \left(1 + \frac{2}{\alpha\mu}\right)$ becomes very low when compared to the other two terms of equation 4.13. Hence, the only part of equation 4.13 which is influenced by T_1 contributes very small towards the gate bias voltage when drain current variation with respect to temperature is zero. So, we can conclude that the value of α_μ, which is a little higher compared to -2 -the ideal value, along with the extremely low measured value of α_{VT} makes sure that $I_D - V_{GS}$ characteristics at different temperatures converge to a vary narrow range. Through this, we can justify the existence of ZTC points happening when biased in saturation region as a bottle neck in the given devices as observed in the experiments.

In chapter 3, we also observed that even though ZTC points exist in NFETs for both linear as well as saturation regions of bias, the ZTC bias points for saturation region is higher than those for linear region. As we know from chapter 2, in linear region,

$$V_{GSF} = V_T(T_0) + \frac{V_{DS}}{2} - \alpha_{VT} T_0 \tag{4.14}$$

where as in saturation region,

$$V_{GSF} = V_T(T_0) - \alpha_{VT} T_0 \tag{4.15}$$

So the additional term of $V_{DS}/2$ in equation 4.14 explains the higher ZTC bias values in

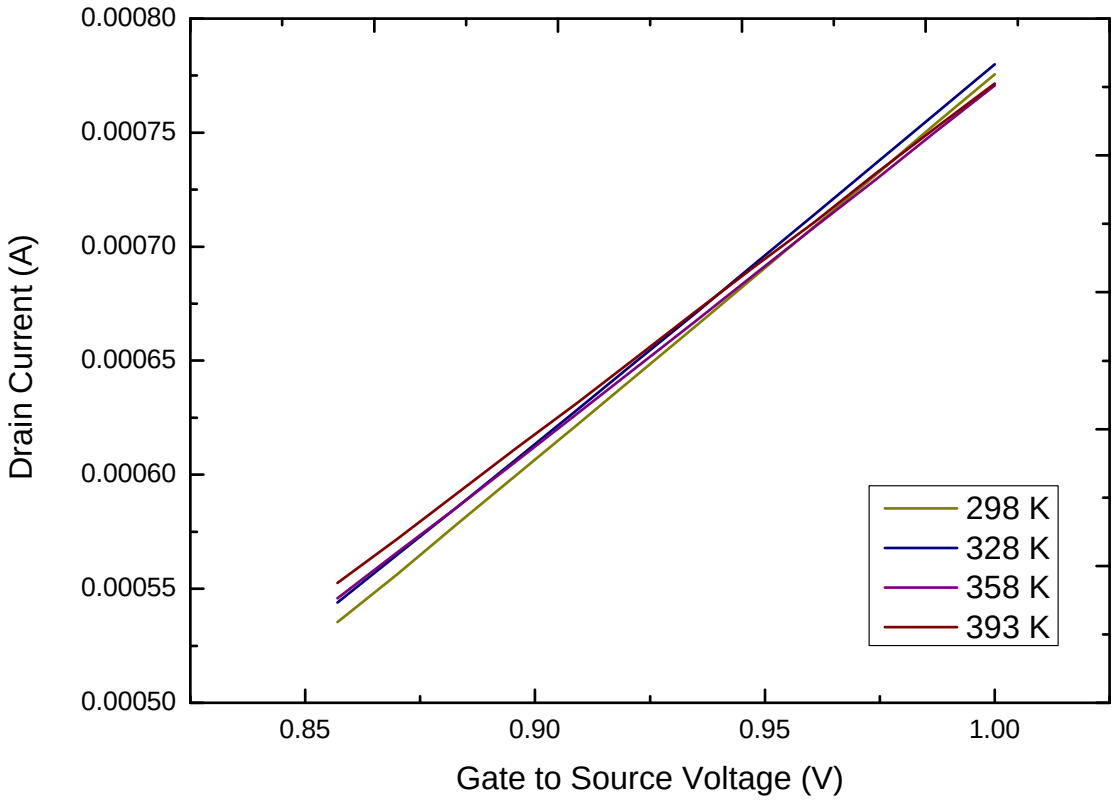

Fig. 4.21 Rescaled I-V characteristics for nMOSFET in saturation region

linear region.

CHAPTER 5

Comparing ZTC points obtained through Experiment and Simulation

A TCAD process suite, Sentaurus comprising of process and device simulation capabilities is used [23] to supplement the experimental study. The whole process followed for realizing the silicon channel NFET as well as silicon-germanium channel PFET has been simulated using Sentaurus process simulator. The device thus by created has been used to run device simulation, using Sentaurus.

As a first step, the simulation is calibrated to match the experiment data. Work functions has been adjusted to adjust the off currents. For Si channel nMOSFETs, a work function of 4.08 is used to calibrate with the experimental data. For SiGe pMOSFETs, the value of of work function used in 4.80.

5.1 TCAD simulations for Si channel nMOSFETs

In figure 5.1, the $I_D - V_{GS}$ characteristics achieved through both simulation as well as experiment for Si channel NFET for $V_{DS} = 50mV$ at 25^oC are demonstrated. The simulation shows reasonable agreement with measurement.

Figures 5.2, 5.3 and 5.4 show the $I_D - V_{GS}$ plots obtained through simulations for the temperatures 25^oC, 55^oC, 85^oC and 120^oC in linear region for NFETs of length $1\mu m$, $90nm$ and $30nm$ respectively. We can observe the ZTC points in the simulations too. Table 5.1 displays the comparison of ZTC operating points revealed through simulation with the original values retrieved from experiments, and the percentage error in the simulation values.

Figures 5.5, 5.6 and 5.7 the $I_D - V_{GS}$ plots obtained through simulations for the temperatures 25^oC, 55^oC, 85^oC and 120^oC in saturation region for NFETs of length $1\mu m$, $90nm$ and $30nm$ respectively. As expected, the simulations also demonstrate the existence of ZTC bias points in saturation region for Si channel NFETs. In table 5.2, the

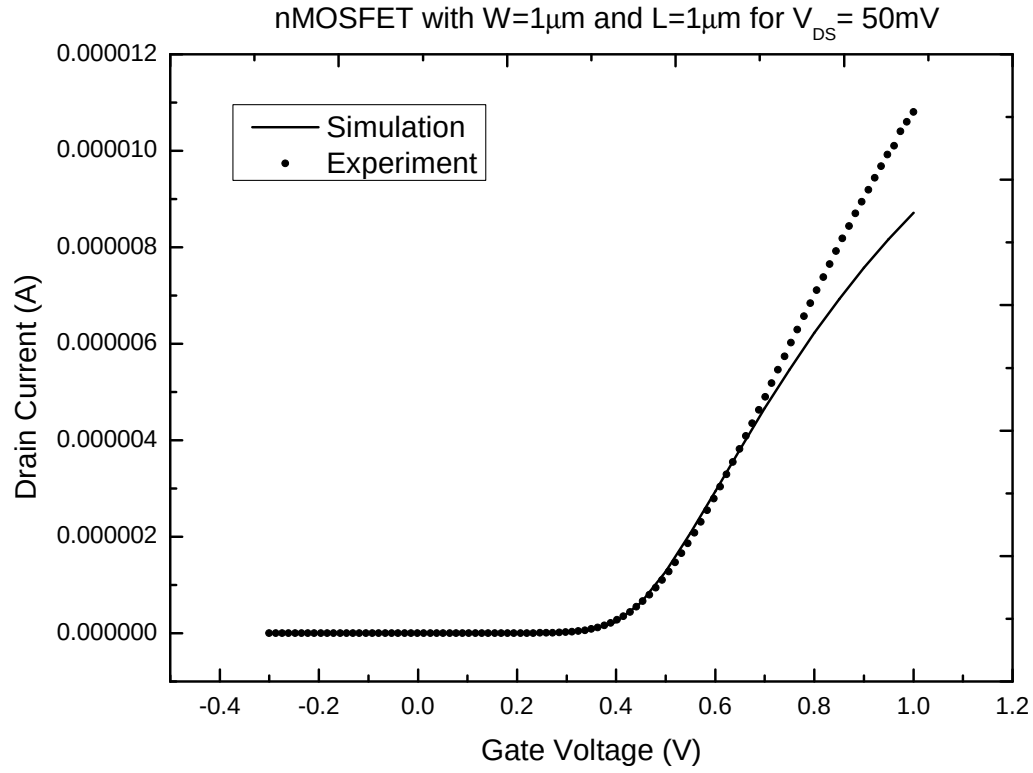

Fig. 5.1 I-V characteristics obtained through simulation as well as experiment for pMOSFET with $W = 1\mu m$, $L = 1\mu m$ at 25^oC for $V_{DS} = 50mV$

Length	ZTC bias point in experiment	ZTC bias point in simulation	% error in simulation
$1\mu m$	0.625	0.640	2.4%
$90nm$	0.700	0.690	1.42%
$30nm$	0.790	0.740	6.32%

Table 5.1 Comparison between ZTC points obtained through experiment and simulation for Si channel NFET devices for $V_{DS} = 50mV$

ZTC bias points obtained by means of both simulation and experiment are compared and the percentage error in simulation values are noted down.

5.2 TCAD simulations for SiGe channel pMOSFETs

Figure 5.8 shows the transfer characteristics obtained through simulation as well as experiment for pMOSFET with $W = 1\mu m$, $L = 30nm$ at 25^oC for $V_{DS} = -50mV$. Figure 5.8 shows the $I_D - V_{GS}$ characteristics obtained through simulation as well as experiment for pMOSFET with $W = 1\mu m$, $L = 30nm$ at 25^oC for $V_{DS} = -1V$. From both figures 5.8

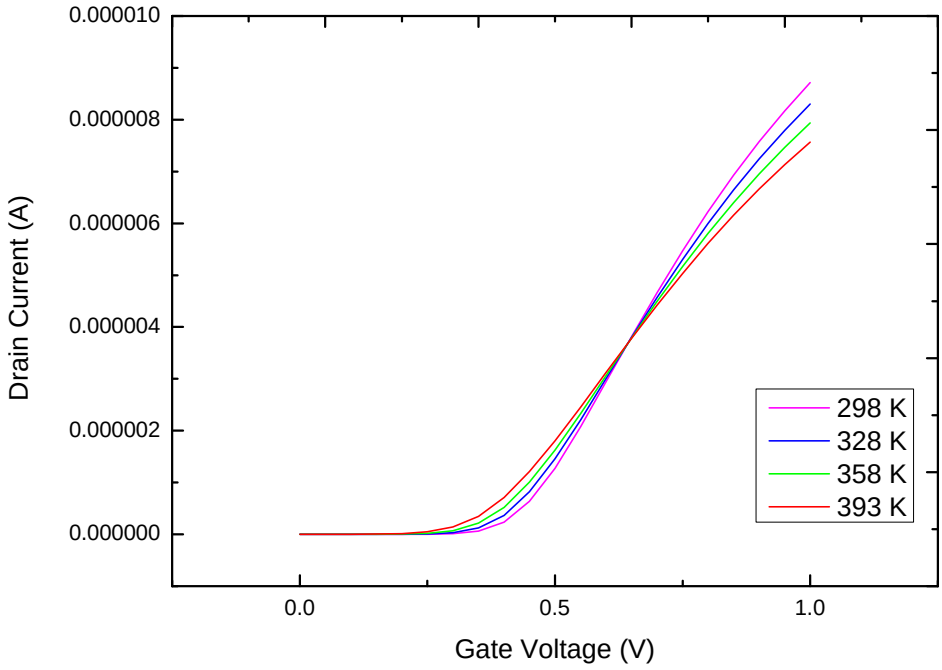

Fig. 5.2 $I_D - V_{GS}$ characteristics obtained through simulation nMOSFET with $W = 1\mu m$, $L = 1\mu m$ at different temperatures for $V_{DS} = 50mV$

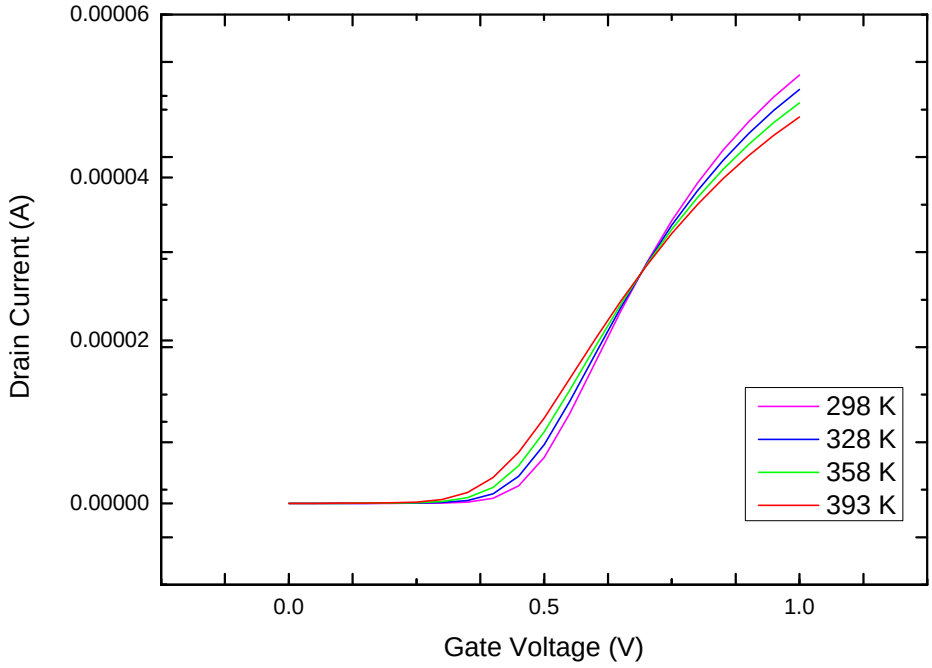

Fig. 5.3 $I_D - V_{GS}$ characteristics obtained through simulation nMOSFET with $W = 1\mu m$, $L = 90nm$ at different temperatures for $V_{DS} = 50mV$

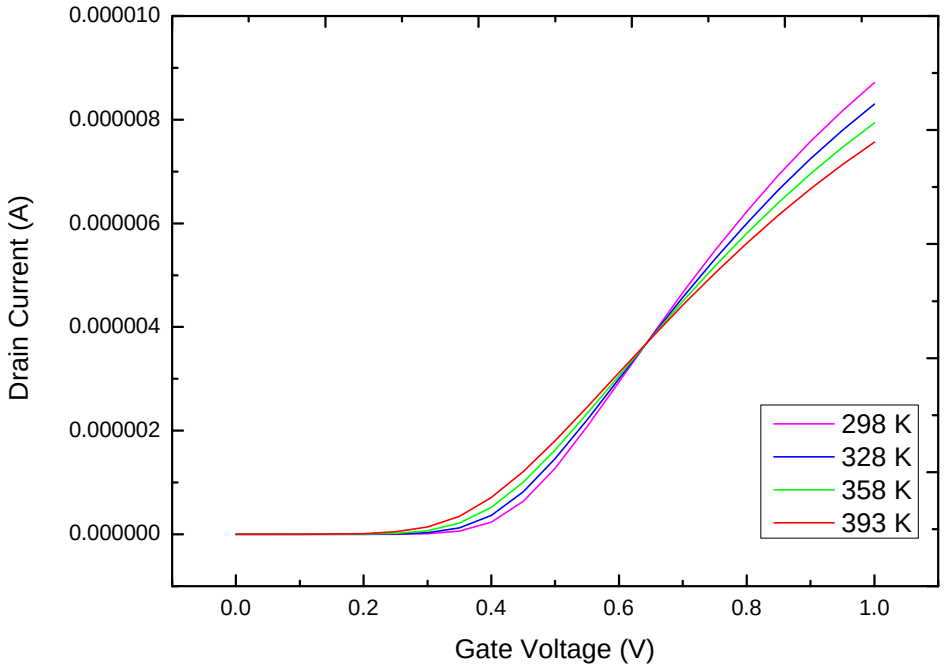

Fig. 5.4 $I_D - V_{GS}$ characteristics obtained through simulation nMOSFET with $W = 1\mu m$, $L = 30nm$ at different temperatures for $V_{DS} = 50mV$

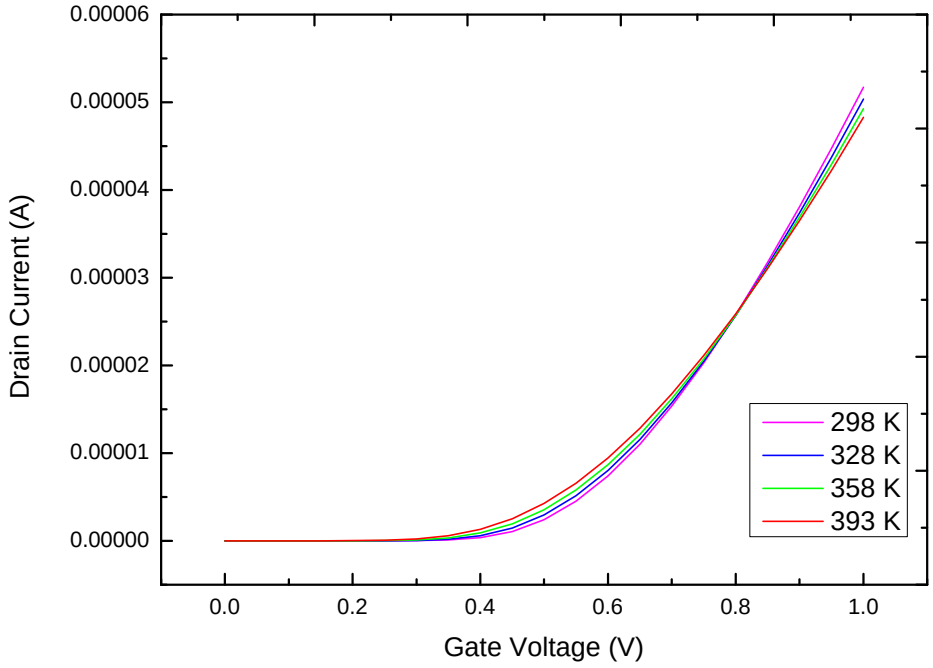

Fig. 5.5 $I_D - V_{GS}$ characteristics obtained through simulation nMOSFET with $W = 1\mu m$, $L = 1\mu m$ at different temperatures for $V_{DS} = 1V$

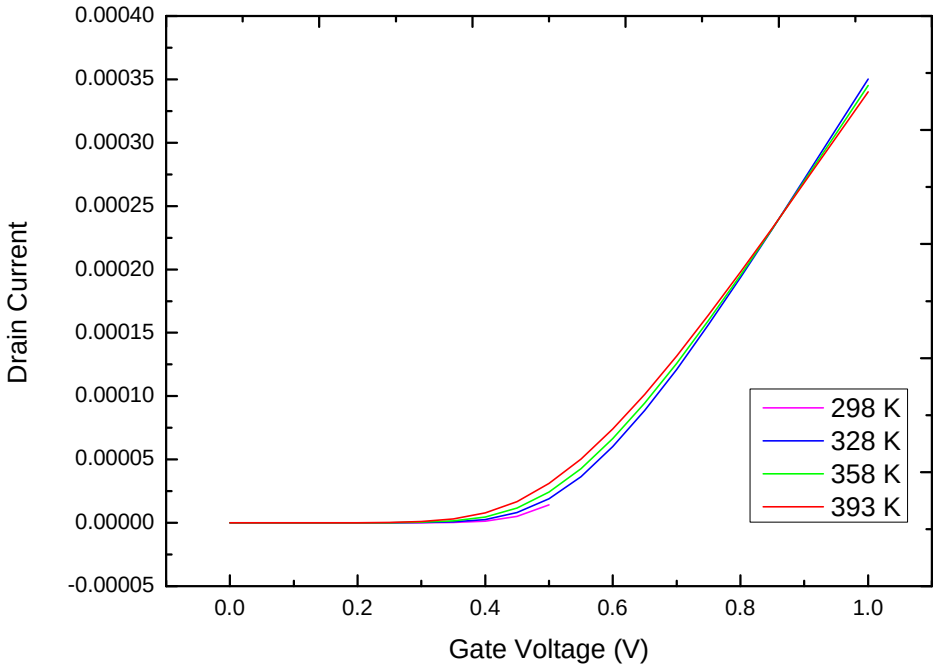

Fig. 5.6 $I_D - V_{GS}$ characteristics obtained through simulation nMOSFET with $W = 1\mu m$, $L = 90nm$ at different temperatures for $V_{DS} = 1V$

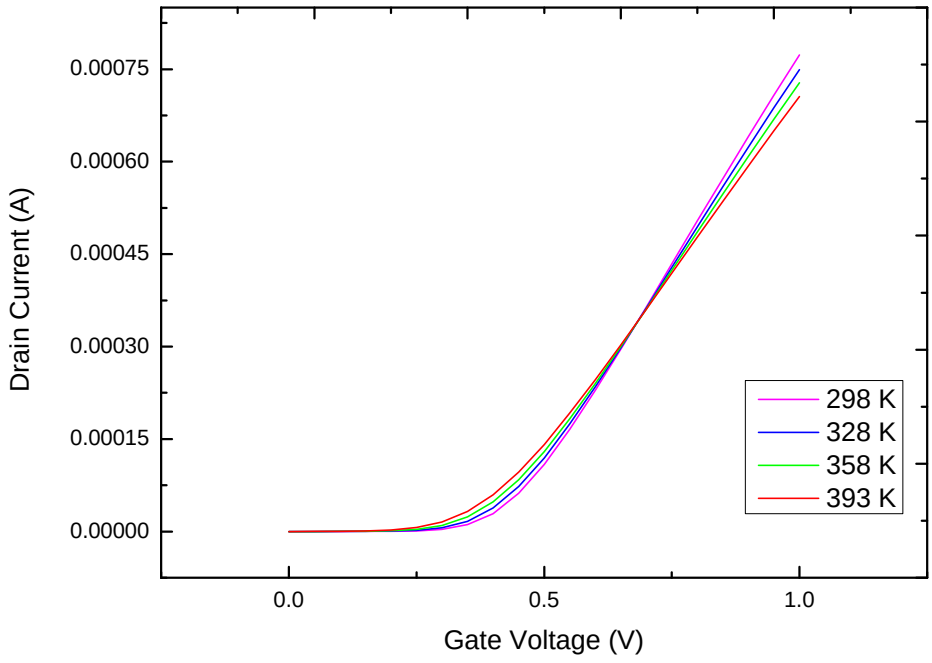

Fig. 5.7 $I_D - V_{GS}$ characteristics obtained through simulation nMOSFET with $W = 1\mu m$, $L = 30nm$ at different temperatures for $V_{DS} = 1V$

Length	ZTC bias point in experiment	ZTC bias point in simulation	% error in simulation
$1\mu m$	0.810	0.800	1.23%
$90nm$	0.840	0.860	2.38%
$30nm$	0.950	0.89	6.31%

Table 5.2 Comparison between ZTC points obtained through experiment and simulation for Si channel NFET devices for $V_{DS} = 1V$

and 5.9, we can see that the TCAD simulation is well calibrated with the data obtained through measurements from wafer.

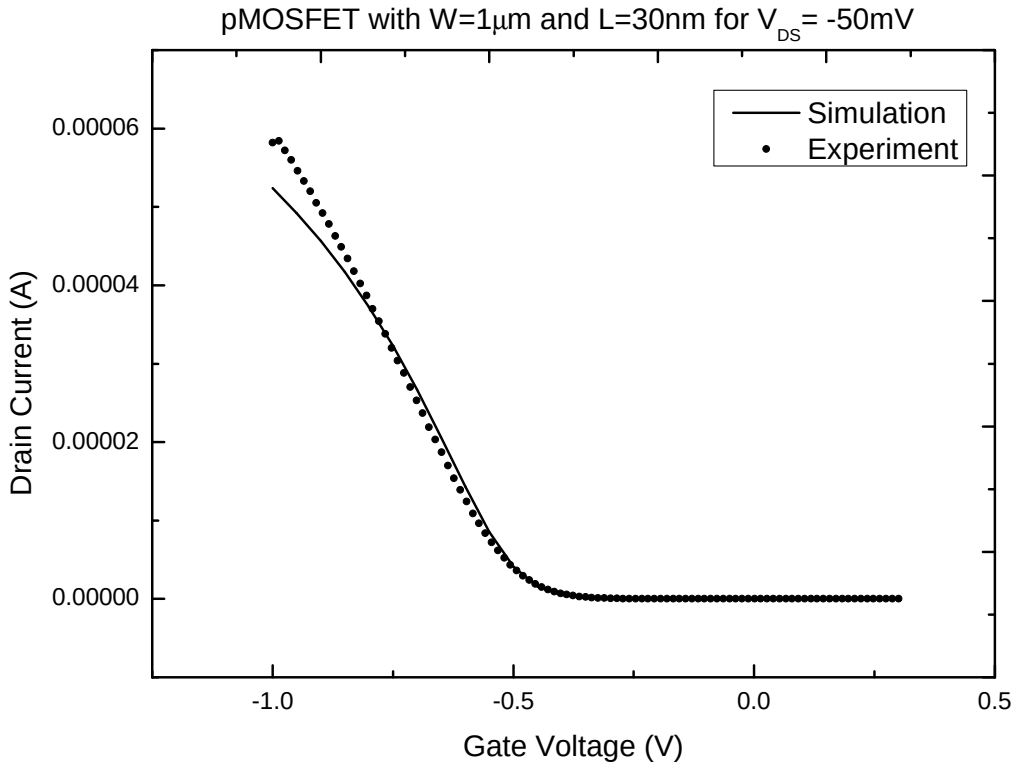

Fig. 5.8 $I_D - V_{GS}$ characteristics obtained through simulation as well as experiment for pMOSFET with $W = 1\mu m$, $L = 30nm$ at 25^oC for $V_{DS} = -50mV$

Figures 5.10, 5.11 and 5.12 the $I_D - V_{GS}$ plots obtained through simulations for the temperatures 25^oC, 55^oC, 85^oC and 120^oC in linear region for PFETs of length $1\mu m$, $90nm$ and $30nm$ respectively. We can observe the ZTC points in the simulations too. In table 5.3, the ZTC operating points observed through experiment as well as simulation are contrasted.

Figures 5.13, 5.14 and 5.15 the $I_D - V_{GS}$ plots obtained through simulations for the temperatures 25^oC, 55^oC, 85^oC and 120^oC insaturation region for PFETs of length

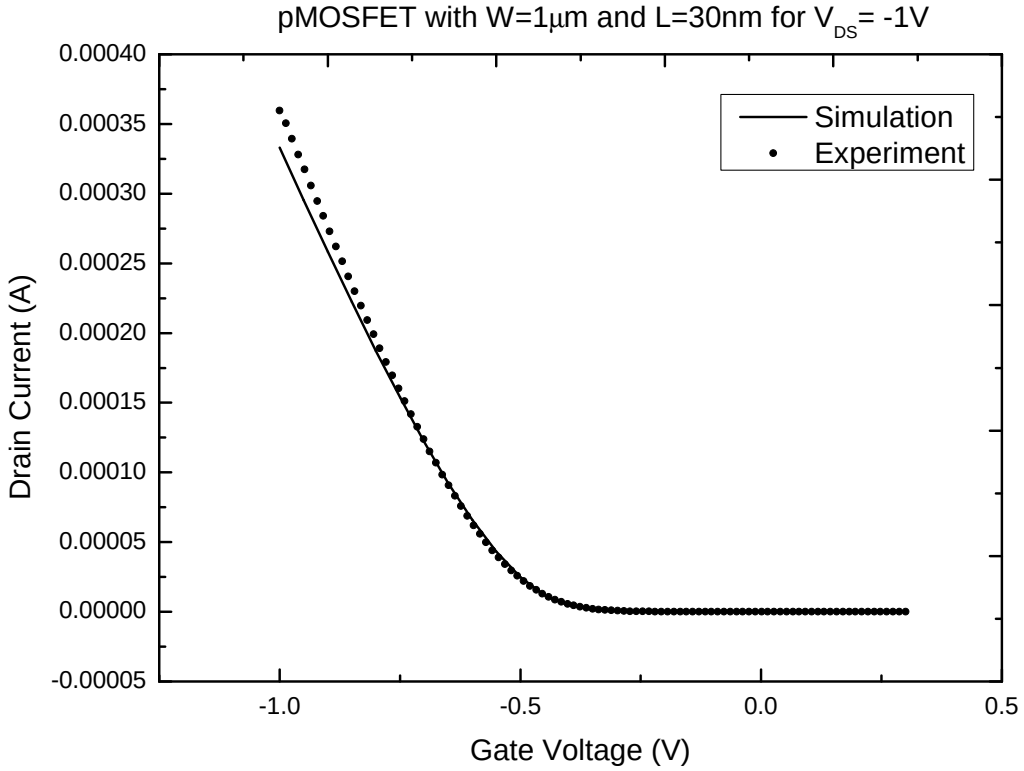

Fig. 5.9 $I_D - V_{GS}$ characteristics obtained through simulation as well as experiment for pMOSFET with $W = 1\mu m$, $L = 30nm$ at 25^oC for $V_{DS} = -1V$

Length	ZTC bias point in experiment	ZTC bias point in simulation	% error in simulation
$1\mu m$	-0.780	-0.76	2.56%
$90nm$	-0.825	-0.805	1.83%
$30nm$	-0.86	-0.82	4.65%

Table 5.3 Comparison between ZTC points obtained through experiment and simulation for SiGe channel PFET devices for $V_{DS} = -50mV$

$1\mu m$, $90nm$ and $30nm$ respectively. We can witness that the simulations are in good agreement with experiments, SiGe p channel MOSFETs don't exhibit ZTC points when biased at saturation region.

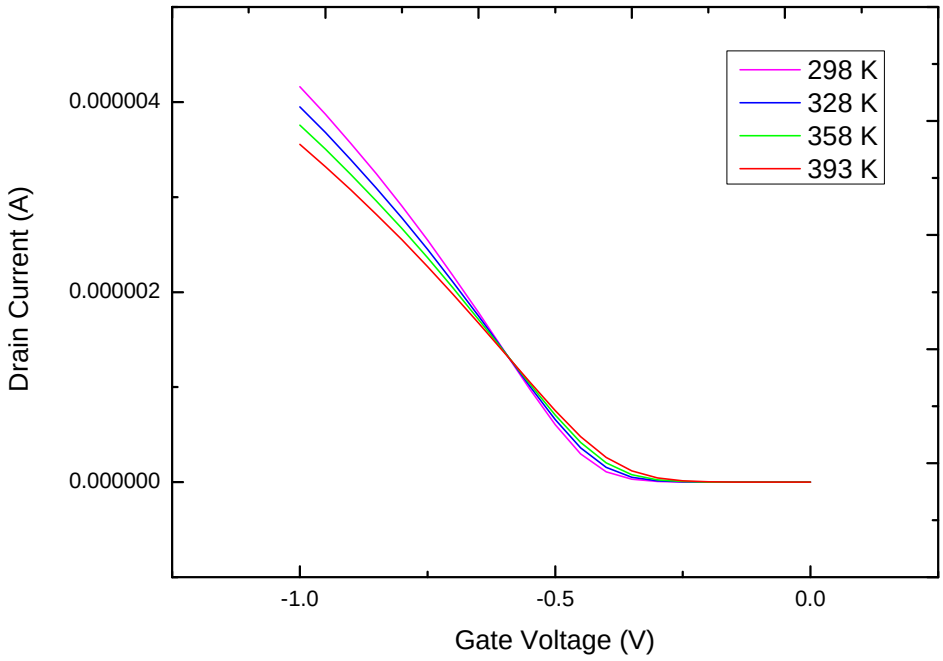

Fig. 5.10 $I_D - V_{GS}$ characteristics obtained through simulation pMOSFET with $W = 1\mu m$, $L = 1\mu m$ at different temperatures for $V_{DS} = -50mV$

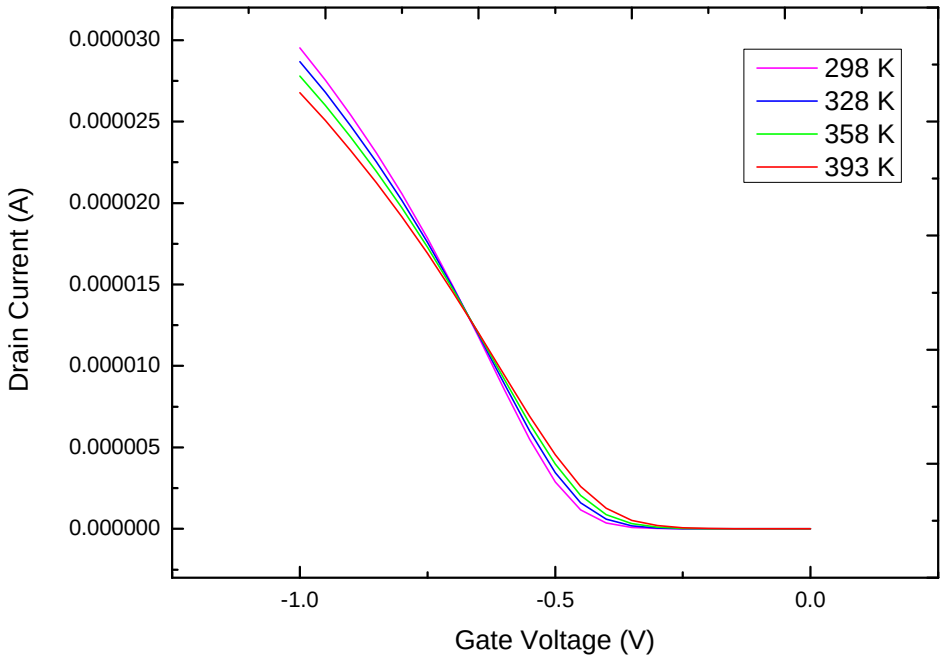

Fig. 5.11 $I_D - V_{GS}$ characteristics obtained through simulation pMOSFET with $W = 1\mu m$, $L = 90nm$ at different temperatures for $V_{DS} = -50mV$

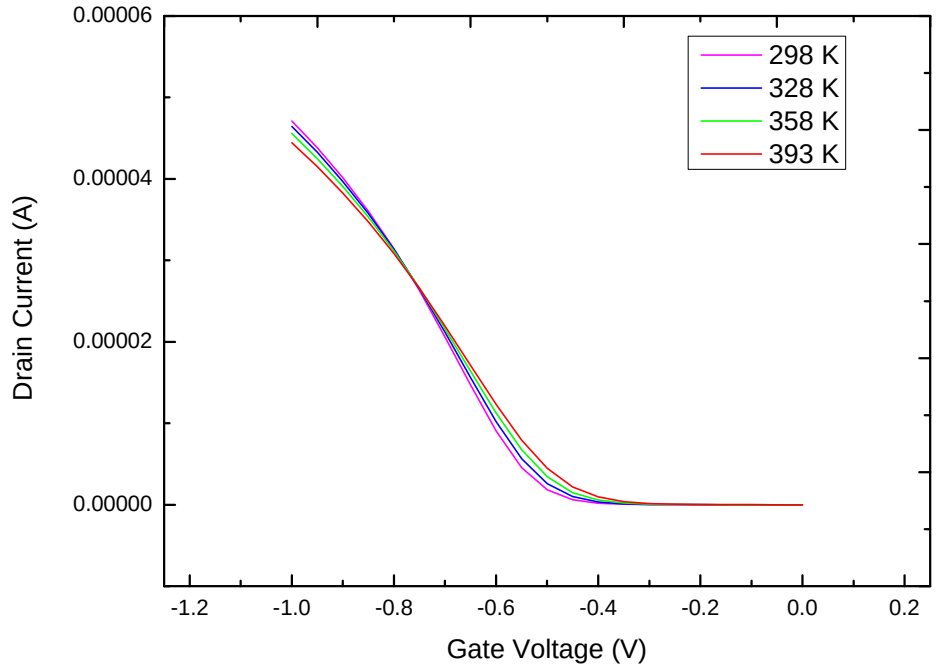

Fig. 5.12 $I_D - V_{GS}$ characteristics obtained through simulation pMOSFET with $W = 1\mu m$, $L = 30nm$ at different temperatures for $V_{DS} = -50mV$

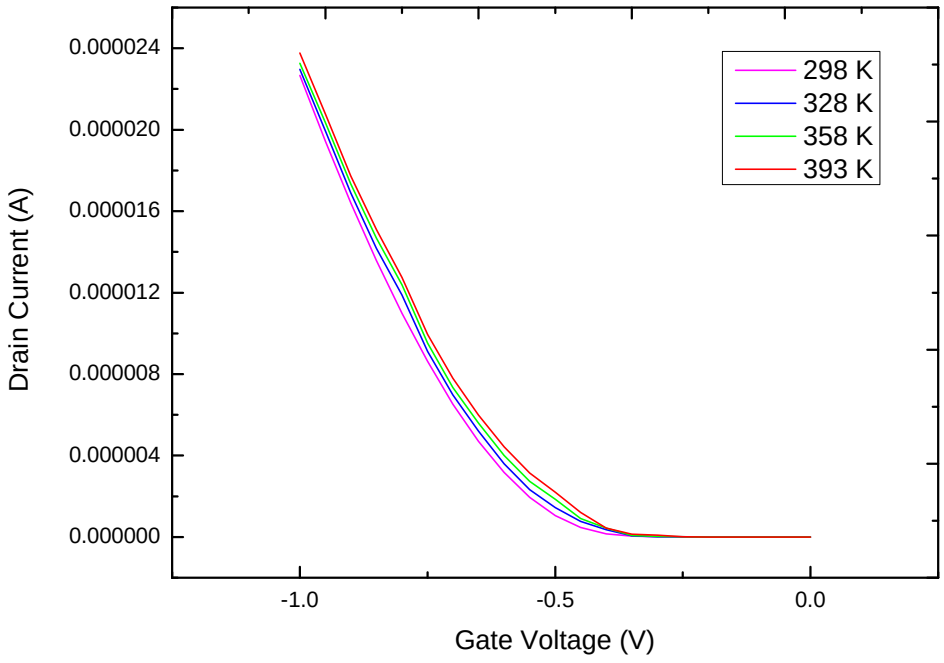

Fig. 5.13 $I_D - V_{GS}$ characteristics obtained through simulation pMOSFET with $W = 1\mu m$, $L = 1\mu m$ at different temperatures for $V_{DS} = -1V$

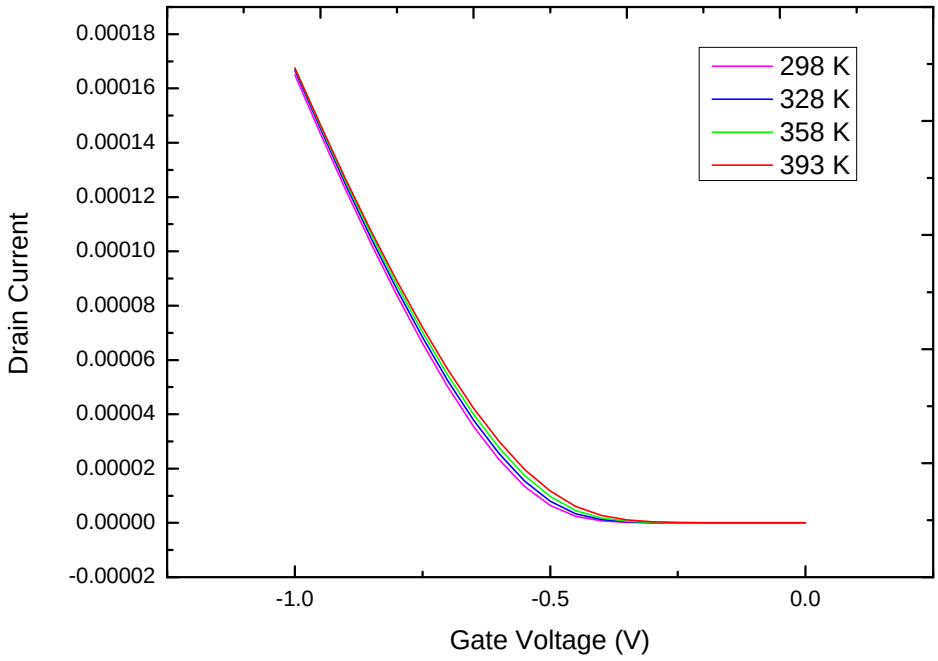

Fig. 5.14 $I_D - V_{GS}$ characteristics obtained through simulation pMOSFET with $W = 1\mu m$, $L = 90nm$ at different temperatures for $V_{DS} = -1V$

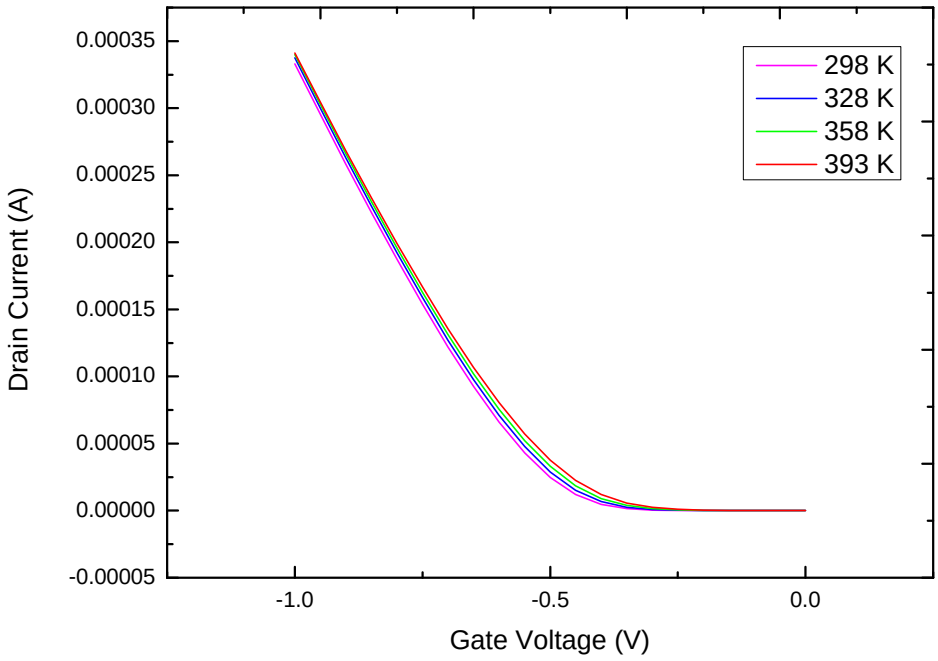

Fig. 5.15 $I_D - V_{GS}$ characteristics obtained through simulation pMOSFET with $W = 1\mu m$, $L = 30nm$ at different temperatures for $V_{DS} = -1V$

CHAPTER 6

CONCLUSIONS

Some of the conclusions that can be drawn from the results presented in the previous chapter are summarized in the present chapter. A discussion on the limitations of the present work and future scope of the work are also included.

6.1 Conclusions

We infer that ZTC bias points exist as a bottleneck in the silicon channel NFET devices for both linear as well as saturation regions. The range of bottle neck appears to be very narrow for linear region and comparatively broader for saturation region. For silicon-germanium channel PFET devices, ZTC bias points exist when biased in linear region, but not in saturation region. The temperature dependence of threshold voltage for both NFETs and PFETs has been analysed and it is noted that the thermal coefficient of threshold voltage appears to be a constant for all lengths of devices. The values of α_{VT} appears to be as low as $-0.6mV/^oC$, which is very low compared to values reported in literature. The thermal coefficient of threshold voltage appears to be channel length independent. Mobility of the n-channel device has been extracted and its dependence on temperature has been studied. The value of $\alpha_\mu = -1.09$, which is very close to the ideal value of $\alpha_\mu = -1$ linear region causes the existence of ZTC point. Since the expected value of α_μ for existence of ZTC point in saturation region is -2, the value $\alpha_\mu = -1.09$ creates the comparatively broader bottle neck instead of exact single point. But, the very low value of α_{VT} makes sure that the range of bottle neck observed is very slim. Transconductance curves has been simulated at various temperatures and those have been well calibrated with characteristics obtained through experiments. The simulations also indicate the presence of ZTC points. The ZTC bias point values obtained through simulations have been compared with those retrieved via experiments and they show good correlation.

6.2 Future Scope of the Work

Some of the improvements recommended include the following.

1. Mobility extraction has been made only for Si channel nMOSFET devices. Further studies on temperature dependence of mobility for SiGe channel pMOSFET can be done.

2. The value of α_{VT} seems to be almost constant and channel length independent for all lengths of devices, which is unexpected. Since we have used only one channel length ($L = 30nm$) in the shorter channel range, extending the study to more short channel devices will reveal the dependence of α_{VT} on channel length.

3. Nothing in literature stipulates that either α_{μ} or α_{VT} should be a constant. A detailed study on both will be possible if measurements are taken at more temperatures. Thus, the temperature dependence of both α_{μ} and α_{VT} can be analysed.

4. The value of α_{μ} is calculated for a regular V_T device. Variation of α_{μ} with high V_T and low V_T devices can be investigated.

5. One of the major applications of ZTC operating points is to design a voltage reference or a current reference circuit. Such an attempt can be looked forward to. Also, circuits can be designed to act a as temperature sensor using ZTC bias points.

6. While extracting mobility, we observe an increase in mobility with increasing V_{GS} which is unexpected. Further studies has to be done to explain this behaviour.

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