STUDY OF MBE GROWN INSULATED GATE BIPOLAR TRANSISTORS AND THEIR CHARACTERISTICS

A project report

submitted by

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THESIS CERTIFICATE

This is to certify that the report titled "**Study of MBE Grown Insulated Gate Bipolar Transistors and their Characteristics**", submitted by **Pranav Sairam Kalaga**, to the Indian Institute of Technology Madras, for the award of the degrees of **Bachelor of Technology in Electrical Engineering and Master of Technology in Microelectronics and VLSI Design**, is a bona fide record of the work done by him under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other institute or university for the award of any degree or diploma.

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ABSTRACT

An Insulated Gate Bipolar Transistor is a device that brings together the strengths of a power MOSFET and power BJT. The aim of this work is to study the advantages provided to an MBE grown vertical IGBT structure by replacing its Homogenously Doped Channel with a Locally Doped Channel, which implies an intrinsic channel with a delta-doped layer replacing a uniform channel doping. The device is entirely diffusion-less and thus provides a greater flexibility in the channel doping profile, allowing us greater freedom in tailoring the electric field within the channel. This has been studied in conventional horizontal MOS devices and we aim to study the effect provided by this in a vertical channel IGBT structure.

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1. INTRODUCTION

The study of power electronics dates back to the early 1900s, with research primarily into high-power applications for conventional electronic devices primarily as a switch. Their major applications include rectifiers, inverters and converters. Over time with the advancement in semiconductor technology and the application of semiconductor devices as switches, these were adapted into power devices. Initial devices include the diode and thyristor, which were designed to handle high reverse blocking voltages and high current capacities. Over time BJTs and MOSFETs were incorporated into the line-up of power semiconductor devices. The Insulated Gate Bipolar Transistor (IGBT) was introduced to circumvent some of the disadvantages of the power BJT and power MOSFET while still retaining their advantages.

The main parameters of interest for a power device are its conduction characteristics, its transfer characteristics, breakdown voltage, on-resistance and switching characteristics. Various power devices are employed for different regimes, mainly over the parameters of operational frequency and voltage, and cost. There exists considerable interest in pursuing novel materials such as GaN and SiC for achieving better voltage and switching frequency ratings compared to conventional silicon devices.

The question now arises as to where the IGBT device fits into this whole scheme of things. Within the silicon device regime, the IGBT performs extremely well within high voltage and current requirement regimes where high amperage and power dissipation is expected. It also functions well in situations that demand low to medium switching frequencies. IGBT devices have demonstrated blocking voltages of up to 6000 V and current capacities of up to 2000 A. They have also been demonstrated to perform extremely well in scenarios where switching frequencies are modest.

IGBTs have extremely varied applications for power switching devices and range all the way from being used in air-conditioners to electric cars and trains. They are extremely versatile and they address issues that significantly impair the performance of a power BJT or power MOSFET in the same scenarios. Though initial IGBTs had significant flaws such as latch-up and secondary breakdowns, modern IGBTS rival power MOSFETs in terms of switching speeds and even exceed their tolerance limits. Conventionally, IGBTs have been designed as lateral devices, similar to MOSFETs, but vertically grown, or trench IGBTs, have also been investigated due to the flexibility provided by vertical stacking processes and other allied advantages, such as device density. The

work presented here explores the advantages provided by one such modification brought about by the flexibility of the vertical IGBT; the growth of a thin delta doped layer in the channel and the advantages it provides. While the work both involves device simulation and also experimental validation, at the moment of writing the report the device for the delta-doped IGBT has not been fabricated due to certain hiccups in the fabrication process.

The thesis is organized organically to document the work done and the concepts used to that end. Chapter 2 provides a review, beginning with a brief introduction to the history of power electronics from the Mercury Arc Rectifier in the 1900s to the modern day concept of power semiconductor devices, particularly the IGBT. It then segues into a review of the fundamental physics and operation of the IGBT device, following which there is a brief discussion on the simulation software, Silvaco ATLAS. This sub-chapter highlights the nuances of the software and provides some essential tips to beginners using it. The next chapter, Chapter 3, discusses the devices that are the subject of this report, the Vertical Channel MBE grown IGBT. Here, we outline the devices under consideration and their structures, following which the simulation results are presented with a concise discussion on them. Chapter 4 provides concluding remarks to the report. Appendices A and B contain the codes used in the simulation which may provide a framework for related studies in the future and the poster presented at the IWPSD conference on the topic.

2.REVIEW

In this chapter, we discuss the history of the power electronics technology industry, beginning with the Mercury Arc Rectifier to modern day semiconductor technologies followed by a review of the IGBT device and its structure and characteristics. We then proceed onto a discussion on the Silvaco ATLAS device simulator platform after which we outline the objective of the report.

2.1 From the Mercury Arc Rectifier to the IGBT

Electronic devices are indispensable in modern day networks and systems. They have allowed automation to an extremely high degree, and in the process improved system efficiency, reliability and reduced mundane manpower. One of the major contributors to this is the MOSFET. As with most silicon based electronic devices, the MOSFET presents excellent integration and fabrication qualities, which when coupled with its potential as a switch allowed it to be a staple in large scale reliable networks.

The switching capability of an electronic device (with amplification being another major regime) is what made electronics ubiquitous in almost all present schemes to control systems, both simple and complex. Modern power systems are extremely complex, by virtue of their scale and the tolerances they demand. To control the voltages and currents that operate within these networks is not a task that can be consigned to a simple MOSFET that may be employed elsewhere and these demand devices designed specifically for the purpose of controlling them, with principles that may be

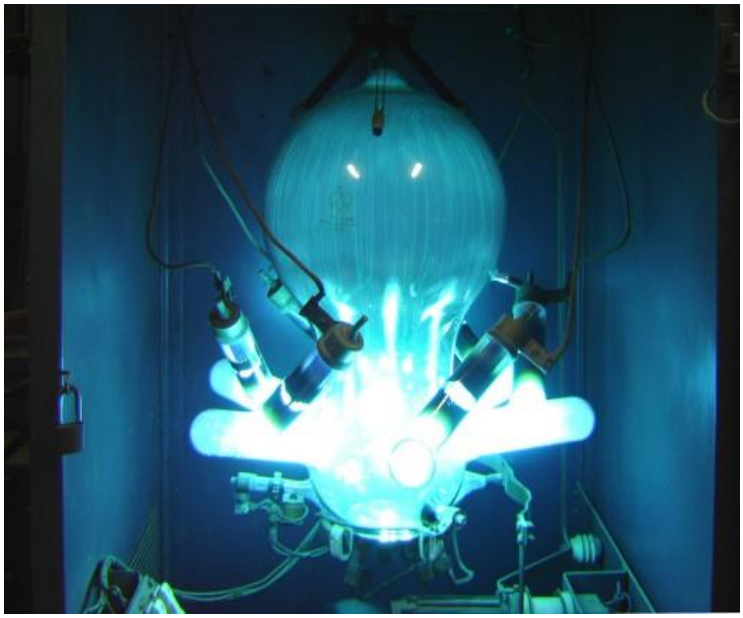


Fig. 1: Mercury Arc Valve

appropriated from devices designed for lower tolerance system. This is the domain of power electronics.

Power electronics, as evident from the name, is the application of electronics to power systems to control and modulate the flows within it, be it generation, distribution or whatever purpose one may seek to achieve. Initial power electronics devices weren't semiconductor devices as we know them today. They were mostly devices that depended on ionized vapours to control and convert electrical flows. The advent of power electronics around 1902 can be credited to the Mercury Arc Rectifier, shown in Fig. 1, which was used to convert AC currents to DC currents.

Further research continued into similar devices, such as thyratrons and mercury arc valves, until the advent of the 1950s when stalwarts such as Hall and Shockley demonstrated stable, reliable and efficient solid state semiconductor devices and the research into using such devices for power electronic purposes grew over time, and eventually semiconductor devices began replacing vacuum tubes.

In 1952, R.N. Hall studying the characteristics of a germanium diode demonstrated that it had a reverse blocking capability of around 200 V and current ratings of up to 30 A. He would go on to be credited with one of the discoverers of the Shockley-Read-Hall non-radiative recombination process, but this doesn't take away from the importance of compact semiconductor power device that he helped bring to light. Over time, the MOSFET and BJT were modified to for power applications and worked on the same principles for both applications, with the only major difference being the voltages and currents they were rated to handle. The thyristor was another important device for power applications. A brief discussion of the power MOSFET and the power BJT is warranted here.

Power BJT:

BJTs for power are generally constructed with a drift region as shown in Fig 2. This is to allow for the device to handle higher voltages and currents. For power devices, the common configuration is the Common Emitter, i.e. base is the input terminal and the emitter is common to the input and output. The poor current gain usually requires that the device be operated in a darlington configuration (Multiple transistors connected together to act as a single transistor with better gain – Fig. 3).

The power BJT is a device that has many shortcomings compared to its counterparts. It cannot handle high current or voltage ratings with ease. The drift region is what primarily determines its breakdown capabilities and a thicker drift region is desirable, though the thickness limits the currents

that can be passed through the device. One also desires a thin base region for amplification but a thin base region also corresponds to lower breakdown performance.

Primary breakdown within the device is due to avalanche breakdown. The device also exhibits secondary breakdown characteristics, which is due to the thermal runaway that is characteristic of BJT devices. These characteristics limit its use within high power regimes. The reverse blocking capabilities are also fairly limited and usually require the use of a power diode.

The BJTs also require high base currents if they are to be designed to carry and handle large currents, which translates to high power losses in the device. The darlington configuration the device requires also limits the switching times that may be achieved by such a device.

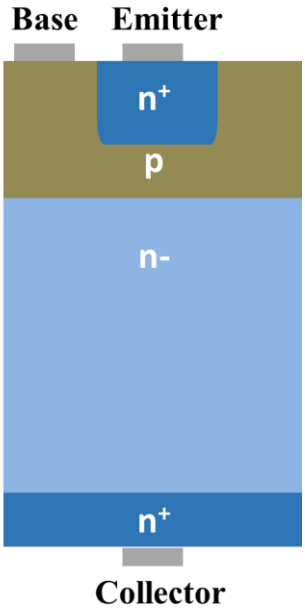


Fig. 2: Power BJT

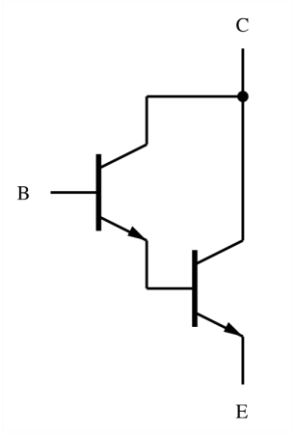


Fig. 3: Darlington Configuration

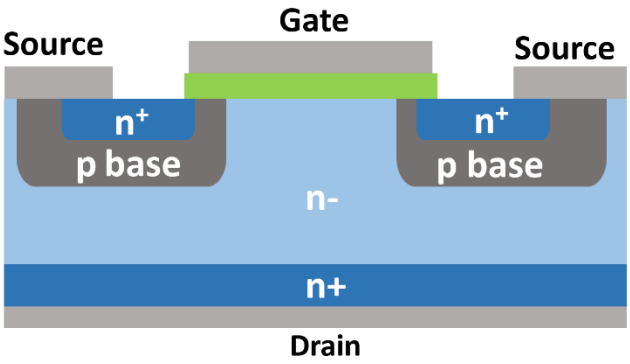


Fig 4: Power MOSFET

Power MOSFET:

The power MOSFET is the high power counterpart of the MOSFET device that is used in low-power applications. Both devices mostly operate on the same principle and for the same purpose, as a switch. Power MOSFETs mainly differ from conventional lateral MOSFETs in that they are vertical. In lateral devices, current and voltage ratings are a function of the channel length whereas in vertical devices they are a function of the thickness of the substrate.

The main advantage the power MOSFET provides over the power BJT is in the switching characteristics. While the BJT requires a large base current, the gate current in the MOSFET is negligible; almost zero. It is easier to control the flow of current through the device given the creation of the inversion layer (leading to a conduction path) is solely dependent on the gate voltage. Power losses in the device are minimized compared to the BJT, here, the power loss being due to the on-resistance of the device. This also brings a trade-off to the fore, the thicker the substrate, the better the breakdown characteristics but this also contributes to higher power losses due to a higher on-resistance. The power loss is also a function of the switching frequency and the capacitances of the MOSFET.

Power MOSFETs unfortunately have no reverse blocking characteristics. Their lack of symmetry also doesn't allow the drain and source contacts to be interchanged. Another limitation on the devices is that the gate voltage is strictly limited by the gate oxide thickness and may be as low as 20-30V to prevent breakdown of the oxide layer. The power losses from the device also make it less attractive for high-frequency applications and very high currents or voltage ratings, upwards of 100 A and 1500 V respectively.

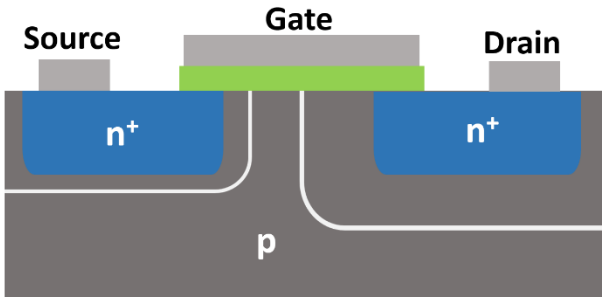


Fig 5: Conventional MOSFET

Power MOSFET to the IGBT

Fig. 5 shows a conventional MOSFET in the off-state. This means that the gate and source are connected to the ground (0V) while a positive voltage is applied to the drain. This represents a real world scenario where the device functions as a switch and is expected to block currents through it. The control signal for this device is the gate voltage which determines if the switch is open or closed.

The issue for tolerances with this device are threefold, the maximum gate voltage that causes oxide breakdown, the maximum currents that the device can handle and the maximum drain to source voltage that causes breakdown. Let us focus on the drain to source voltage. As we noted, the gate and source are both connected to ground. The depletion region for the source region is the zero-bias depletion region. There currently exists no effect of the gate under the depletion region due to it being at ground, if there does exist any such region under the gate it is owing to the source and drain region. What we would expect from an ideal switch behaviour in a MOSFET is that it should be able to block any voltage applied to the drain (given that source is connected to ground).

As the drain voltage is increased, the reverse bias at the drain-body junction increases too. This leads to a widening of the depletion region in the lower-doped region. The depletion region continues extending into the body under the channel and eventually punches through. This is the source of breakdown and also a conventional MOSFET's poor blocking characteristics in a high-power regime.

Circumventing this issue by increasing the body doping or reducing the drain (source) doping does not go a long way as it compromises the i-V characteristics and the threshold voltage of the device. One cannot indiscriminately increase the channel length as this is a trade-off with the capacitance and switching characteristics of the device. A plausible solution to this issue is a halo implant and the like. This however, while useful for low-power and short-channel schemes fails to work in a scenario where the voltages are higher. Another improvement that may be considered is the Drain-Extended MOSFET.

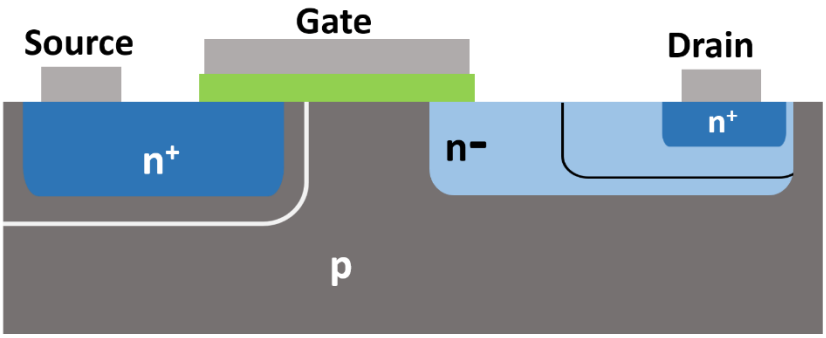


Fig 6: Drain-Extended MOSFET

The Drain-Extended MOSFET, as shown in Fig. 6, represents a step in the direction of being able to switch higher voltages without conduction or channel pinch-off occurring in the device. The device variation compared to the conventional MOSFET is that we maintain the same channel length but add an intermediary n- doping layer in the drain before the highly doped drain contact layer. The highly doped n+ layer provides the required contact surface. The n- layer is doped lower than the substrate p layer. This causes the depletion layer under the gate that was a major issue in the previous scenario to instead be absorbed by the n- layer.

The lateral n- layer is doped lower than the substrate. A voltage applied to the drain increases the width of the depletion region, but this time it extends into the n- layer given its lower doping. This is an effective solution but also brings its own share of issues. For one, extending the drain with a low doped profile increases the on-state resistance of the device. This also leads to increased power losses during operation and switching. Another issue with this implementation is the increased device footprint. To accommodate higher blocking voltages the length of the n- region also needs to be increased.

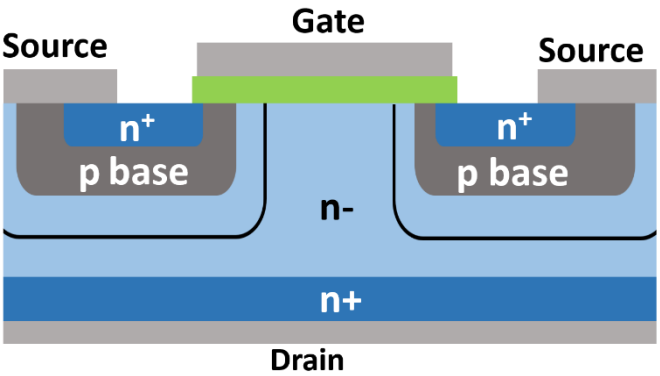


Fig 7: Power MOSFET

Fig. 7 represents the schematic of the logical next-step of the drain-extended MOSFET, the power MOSFET. We continue to use a highly doped n+ as the source and drain and a p-region as the channel region.

The important difference to note here is the channel region and the substrate. The channel which used to be a part of a p-substrate is reduced to a p-well in an n- substrate. This is in an effort to effectively increase the drain extended region and therefore be able to block significantly higher voltages. Note in the figure that the drain contact is now at the bottom of the substrate and there exist two source contacts on either side of the gate. Effectively, this represents two individual devices.

Compared to the previous drain extended case, here the drain extension is the substrate. This reduces the device footprint as there now is a much larger n- region for the depletion layer extension from an applied drain voltage to be absorbed into. This also reduces the field crowding in the channel. The implementation of the substrate as the drain extension region also gives a much better device density as the lateral footprint required for a given breakdown voltage is significantly reduced. This however does not resolve the issue of the on-state resistance. While the area of current flow is increased proportional to the channel width, it is not feasible to indiscriminately increase this area. Therefore on-state conduction and allied power losses are still a significant issue in this device. This is where the aforementioned desirable characteristics of the IGBT come in and this is achieved by a small design change.

Fig. 8 gives the schematic of an Insulated Gate Bipolar Transistor. The figure represents the vertical implementation of the IGBT. The IGBT is achieved by replacing the drain n+ region with a p+ region. This can be done for the structure in Fig. 14 to get the vertical schematic of the IGBT or for the structure in Fig. 13 to get the lateral implementation.

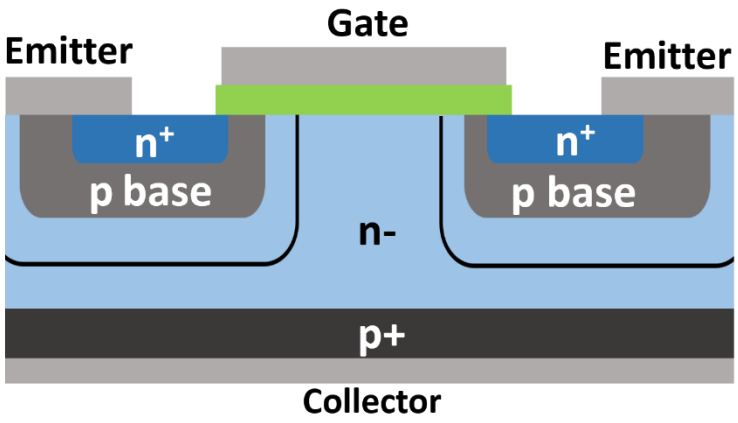


Fig 8: Insulated Gate Bipolar Transistor

The off-state picture is similar to the power MOSFET. The major difference here is the on-state operation and characteristics. During operation, the p+ collector region injects holes into the drift region increasing the minority carriers significantly. This difference can be as large as an order of 3 or higher. This reduces the on-state resistance of the drift region, thereby minimizing power dissipation losses too. This can be seen as similar to BJT action. The off-state still maintains similar breakdown voltages and characteristics as the power MOSFET. There is also an intrinsic junction at the bottom collector junction that provides reverse blocking capabilities.

There are however certain compromises with regards to device switching characteristics. The device also has an initial cut-in voltage due to the bottom collector junction. We shall explore the device physics of the IGBT in detail.

Insulated Gate Bipolar Transistor (IGBT):

The IGBT was the culmination of efforts made to combine the best of the power MOSFET and the power BJT. Their main purpose was to be able to replace power BJTs, or at the very least improve upon their ratings and characteristics. The initial attempts were efforts to create hybrid BJT-MOSFET circuits on the same chip, such as in Fig. 9 and Fig. 10, but these didn't make use of intrinsic device physics and operated on a circuit level. They relied on making use of the MOSFET to control the high base currents that inhibit the power BJT's usefulness, and the BJT's low on-

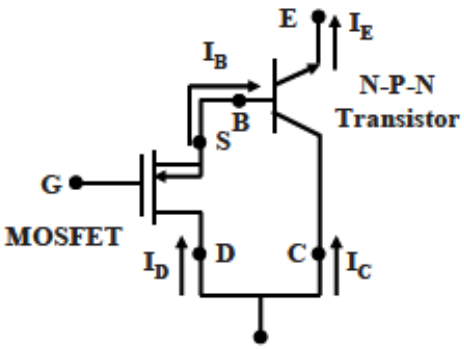


Fig 9: MOSFET-BJT equivalent circuit

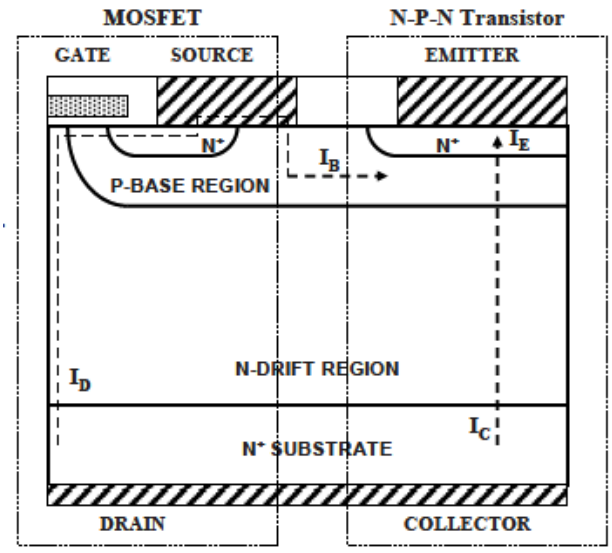


Fig 10: Hybrid power MOSFET-BJT

resistance and better on-state characteristics counter the MOSFET's poor characteristics.

Let us briefly discuss the operation of the hybrid device shown in Fig. 10. The MOSFET and BJT regions are highlighted in the figure itself, and is a single-chip device that is represented by the circuit in Fig. 9. This structure is both compact and effective compared to two discreet structures but it is a poor implementation as it does not meld the physics of the two devices into one. This device has the advantage of applying low input voltages as this simply is the gate drive of the MOSFET that in turn drives the BJT. The BJT portion of the device carries the majority of the on-state current given its better on-state performance.

However, being two devices brings its own share of problems to the performance of the hybrid implementation. Both the MOSFET and the BJT require to have similar ratings for blocking high-voltages, given that this simply is the case of the weakest link in the chain. The device compactness is also marred by the requirement for the MOSFET requiring a large area, due to the high on-state resistance. The switching frequency is also not improved due to the fact that the BJT still has a high base current which takes time to die down, resulting in the device not being easily turned off.

The IGBT represents the merging of the device physics of both the MOSFET and the BJT. This is a device that melds the device physics of the BJT and MOSFET by integrating the device regions of the two individual devices. Here the gate region binds the emitter and drift regions creating the conduction path for the MOSFET and the high currents are conducted through a low on-resistance drift region owing to the BJT action in the same device. The IGBT in itself may be modelled as either a MOSFET and a BJT, or as a MOSFET and a diode. This is from either seeing the conduction due to the BJT action or carrier injection from the bottom collector junction.

Another tremendous advantage of the device that is easy to see is that it has an inherent reverse blocking capability. Note that one mustn't confuse the IGBT structure with the thyristor, as they are inherently different in physics and operation. Initial IGBT models suffered from slow-switching speeds and latch-up, but with the efforts of stalwarts like Jayant Baliga and Nakagawa, these were shown to be easily manageable, in fact, completely suppressible. These are complete non-issues in modern IGBT circuits.

The IGBT brings the best of both worlds to a power engineer. Apart from all the above mentioned advantages, it also boasts of an excellent safe operation regime. IGBT devices have been demonstrated to handle up to 50 kW/cm^2 power densities. They have also demonstrated blocking

voltages upwards of 6kV and current capacities exceeding 1500A. This device is the subject of our current work and we assume a novel approach to the fabrication of the device and study its characteristics with the replacement of a homogenous channel doping with a locally doped channel.

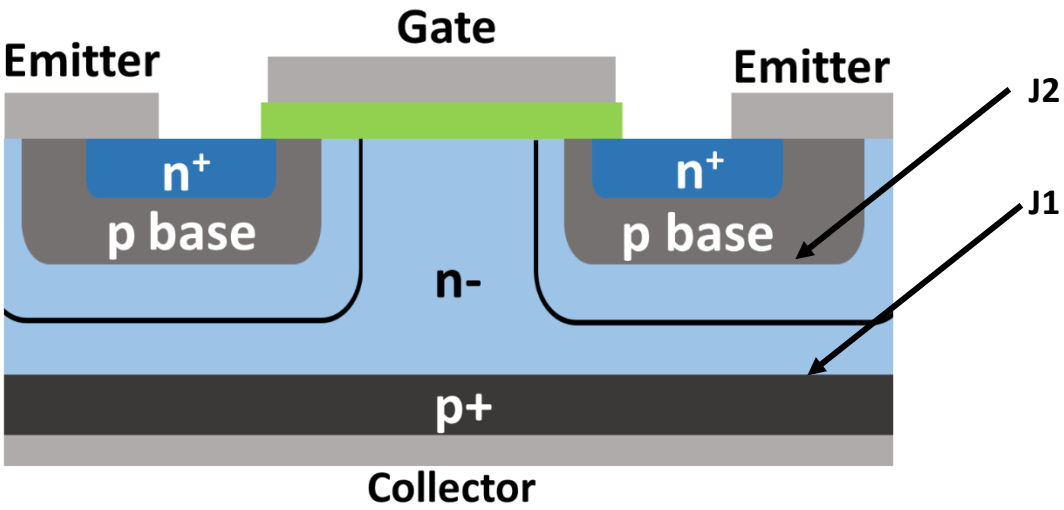


Fig 11: IGBT device with junctions J1 and J2

2.2 IGBT device physics and characteristics

In this section, we shall discuss about the basic operation of the IGBT, the device physics in its operation and the characteristics that specifically differentiate it from other popular power devices. For the purposes of this discussion we shall primarily consider a conventional lateral IGBT device. While there exist multiple IGBT structures such in both the lateral and vertical (trench) sense, the basic device physics and operation is consistent across the device variations. Also note that for the convenience of explanation we shall only touch upon the n-channel IGBT and for further reference, the texts provided in the bibliography provide an excellent and comprehensive guide.

IGBT Device Physics:

The Insulated Gate Bipolar Transistor is the result of bringing together the device physics of the power MOSFET and BJT. The IGBT is a 3-terminal device, with the terminals being the Emitter, Gate and Collector. These terminals correspond to the Source, Gate and Drain terminals of the power MOSFET respectively. While the terminals are named emitter and collector referring to the BJT action that is present in the device, one mustn't give too much importance to it.

The device is similar to a power MOSFET except for the doping of the layer under the drain being replaced by a p+ layer. This functions to create a pnp BJT action (this can also be seen as a pn junction at the collector electrode). The IGBT consists of four major regions, the emitter, channel, drift and collector regions.

The IGBT consists of three junctions. One junction at the emitter-channel interface, one at the channel-drift region interface and one at the drift-collector interface. The junction at the drift-collector interface is what gives the IGBT an inherent reverse blocking capability. This poses an issue in certain situations where one requires a reverse conduction feature but in scenarios where reverse blocking diodes are used, this reduces their redundancy. Also, for scenarios where reverse conduction is required in high-power regimes, diodes are shown to have higher performance than the inherent reverse conduction of the MOSFET.

The lateral scheme, though easy to integrate with conventional IC fabrication processes, occupies too much Si surface area, increasing as the breakdown ratings increase. It also suffers from severe latch-up problems due to deficiencies to use lifetime killing processes in the IC fabrication process in this lateral scheme and substrate leakage currents. The vertical IGBT however circumvents these issues and is a more favourable scheme for the design of power IGBTs, particularly discrete devices.

There are three major regimes of operation for an IGBT device. These can be broadly termed as (1) Reverse Blocking, (2) Forward Blocking and (3) Forward Conducting. (1) Reverse blocking refers to the ability of the device to prevent currents that flow against the desired direction of flow, which in this case is from the collector to the emitter. (2) Forward blocking refers to the ability of the device to function as a switch, where it cuts off flows depending on if a voltage is applied to the gate or not. (3) Forward conducting also refers to the device as a switch but when it is closed and conducting. All three are very important to the operation of any power device, but as such (2) forward blocking and (3) forward conducting are more sought after for the simple reason that (1) reverse blocking can easily be handled by a power diode, which demonstrates better ratings than a discrete switch device. We shall examine the device's schemes of operation briefly, considering a depletion-mode device for the convenience of explanation.

1. Reverse Blocking

Reverse blocking refers to the situation where a negative voltage is applied at the collector contact. The emitter contact is usually considered as the reference and is grounded. Let us refer to the junction between the p+ collector and the n- drift region as J_1 and the junction between the p-base (or deep p+) and the n- drift region as J_2. This is shown in Fig. 11 for reference. The junction between the p-base region and the n+ region isn't examined specially for the reason that the p-base region bears the MOSFET-action channel under the gate and as such, the junction wouldn't be of special consequence beyond looking at punch through characteristics.

In this scenario, J_1 is reverse biased while J_2 is forward biased. The reverse blocking occurs at J_1 almost wholly and the depletion region extends into the n- drift region. The maximum electric field also occurs at this junction and therefore, this plays a major part in determining the breakdown voltage rating in this blocking regime. An n- layer that is very thick results in avalanche breakdown occurring when this maximum electric field reaches the critical field value. A thick drift region also implies higher on-state resistance. A thin drift layer lends itself to the possibility of the depletion layer extending through the complete thickness of the layer. This is known as the "reach-through" condition. When this occurs, carriers injected from J_2 cause an increase in the current at the collector junction, similar to the punch-through condition.

Adding the n+ buffer layer allows us to control the reach-through breakdown condition, by absorbing a significant portion of the depletion layer into the buffer layer. This does compromise the conduction characteristics of the device though. The reverse blocking is useful in situations and topologies where a reverse current is expected, such as AC current circuits, and power MOSFETs are unable to handle the blocking ratings, even with the assistance of a diode.

2. Forward Blocking

We shall use a similar naming scheme for the junctions as before for the purposes of this discussion. In the forward blocking scenario, a positive voltage is applied at the collector junction and the emitter is at ground. The gate is shorted with the emitter; to ground. That is to say that the IGBT is functioning as an open switch. The n+ buffer layer and other such modifications seek to improve the characteristics of the device in the forward blocking and conduction regime while sacrificing performance in the reverse blocking scheme.

In this regime, J_1 is forward biased while J_2 is reverse biased. J_2 bears the applied voltage and depletion region and contributes to the blocking capability of the device. As before, the depletion layer extends into the drift region mainly and the maximum electric field occurs at this junction. As before in the reverse blocking scenario, the voltage is limited either by the critical electric field; avalanche breakdown, or by the reach-through phenomenon. The limitation of using an extremely large drift region also is prominent due to the on-state resistance increasing. This will be further discussed in the forward conduction regime.

The prominent breakdown in this regime is the open-base transistor breakdown. This occurs when the depletion width increasing in the drift region also increases the base transport factor until the base

current gain equals unity which results in breakdown. An interesting point to note is how the breakdown voltage is dependent on temperature. As temperature increases, the impact ionization factor decreases thereby increasing the breakdown voltage. While the base transport factor also increases due to the increase in carrier lifetime, this is not as prominent as the former. This lends to the IGBT its excellent performance over a wide range of temperatures.

3. Forward Conducting

We shall use the same naming scheme for the junctions as we used for the previous regimes. In this state, a positive voltage is applied to the collector with the emitter to ground. The difference being that the gate is also biased with a forward voltage, essentially creating a conducting channel in the p-base, at voltages above the threshold voltage. This conducting channel is essentially the inversion layer that is created by the MOSFET-gate action in the p-base.

The inversion layer bridges the n+ emitter and the n- drift region, and this creates a path from the emitter to the collector, through the forward biased J_2. This junction injects holes into the n- drift region, and at substantial values of the collector voltage this can be as significant as an order of 3 increase in hole concentration in the drift region, tremendously increasing the conductivity and reducing the on-state resistance of the IGBT. This is known as a high-level injection. Two important points to note here are that J_2 requires a minimum cut-in voltage before this action begins and very large thicknesses of the drift region diminishes this effect due to more recombination happening as the carriers travel through it.

The current conduction in this regime is primarily via a drift process. This action can be seen as similar to a p-i-n diode in series with a MOSFET for high gate voltages. Whereas for gate voltages not significantly above the threshold voltage this can be seen as a MOSFET providing the base drive for a pnp transistor. For the two cases, the MOSFET operates in the linear region for the former and in saturation for the latter.

Device Static Characteristics:

In this section, we shall present some standard IGBT static characteristics with the intention to provide a basic familiarity with how the IGBT performs qualitatively and what kind of characteristics one may expect from the device. The mathematical modelling or experimental validation for the statistics may be gathered in detail from the texts mentioned in the bibliography. The characteristics presented here are for the n-channel IGBT, and one may refer to literature for a detailed analysis of the p-channel IGBT. To this end, the reader is referred to J. Baliga's Fundamentals of Power Semiconductor Devices for a concise yet detailed explanation of the IGBT device.

i-V characteristics

Conventionally, for the purposes of studying the i-V characteristics, the emitter contact is biased to ground. This is our reference voltage with respect to which other voltages will be assessed.

For calculating the forward characteristics, the collector voltage is swept over a range of positive values for various fixed values of the gate voltage. This procedure is similar to that done for a depletion-mode MOSFET.

For the reverse characteristics, we are particularly interested in the reverse blocking voltage. In this case, the gate and emitter contacts are shorted to ground and a negative voltage is applied to the collector. We keep increasing the magnitude of this negative voltage till we observe a breakdown and a sudden increase in the current. This is where the breakdown voltage of the device lies and determines the reverse blocking rating of the device. These characteristics are qualitatively shown in Fig. 12.

Note in the characteristics that a small value of collector voltage is required before the device begins to show the desired characteristics. This is due to the fact that the junction that exists between the collector and drift regions requires a cut-in voltage before injecting carriers into the drift region. This value is approximately 0.7 V. The forward characteristics are qualitatively similar to the MOSFET's with the major difference being a quantitatively significant increase in the current magnitudes.

It is also easy to observe how the reverse characteristics primarily resemble a p-n junction diode as the collector junction functions as the reverse blocking region in the IGBT. One can also see how the

forward characteristics can be modelled by the two models for the IGBT we discussed earlier, with the p-i-n injection for the region where the MOSFET-action is linear and as a MOSFET providing the BJT base drive current. Here, the regions labelled in Fig. 12 correspond to the BJT regime scheme and the active region corresponds to the MOSFET-saturated action and the saturation region corresponds to the MOSFET-linear action.

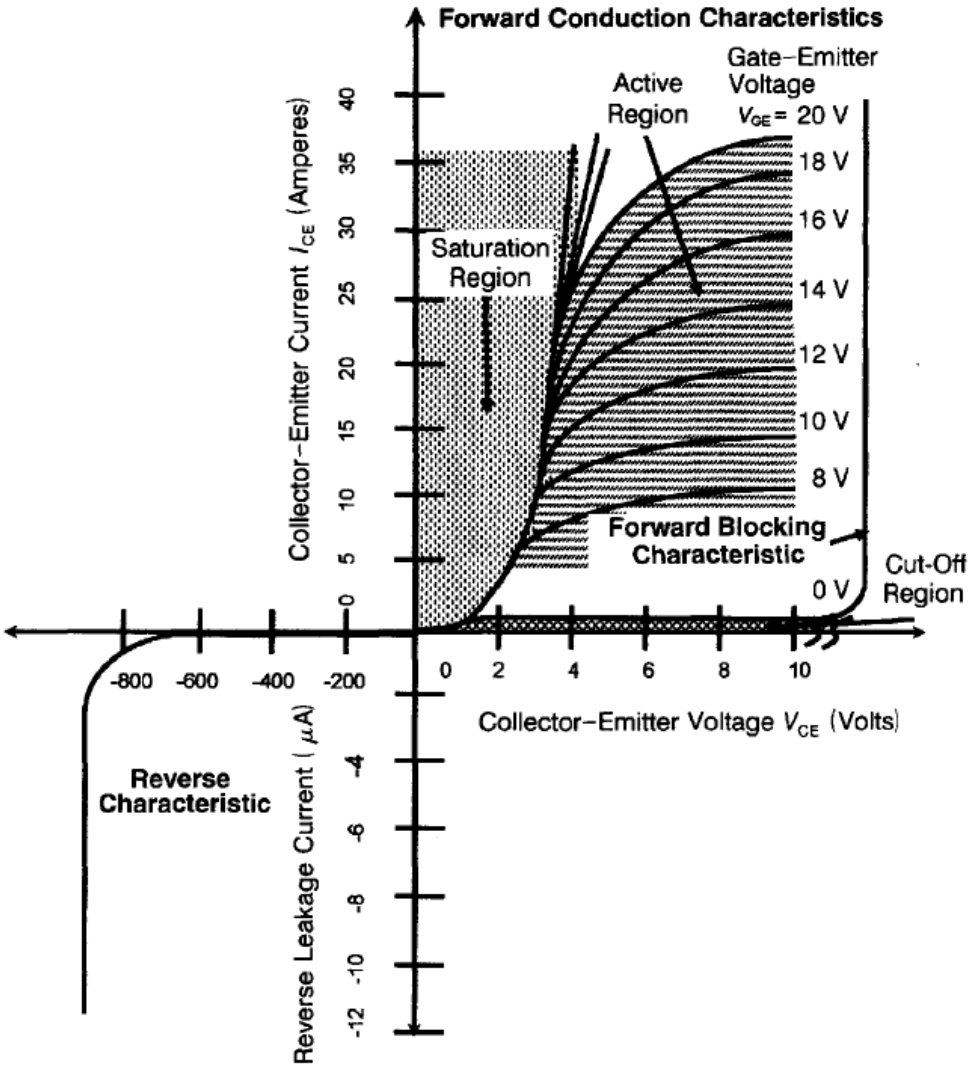


Fig 12: i-V Characteristics of an IGBT device

2.3 The Silvaco ATLAS platform

Silvaco Atlas is a physically based 2D and 3D device simulator. Its features include simulating DC, AC, and transient analysis for silicon and a slew of other material based devices. Atlas consists of multiple sub-modules and can be initialized from the DeckBuild environment. DeckBuild is the front-end interface to multiple TCAD software solutions in the Silvaco domain. This allows integration of Atlas with various other solutions allowing for a robust device simulator.

Atlas can be used to create the device and simulate it based on various models available in the simulator library. Atlas can also be used in tandem with Athena, which is a process simulator, TonyPlot which is a plotting and visualization software and other tools. Atlas is a physically based simulator which means that the device's electrical characteristics are calculated by an iterative process on differential equations that are applied at various grid points on the device, known as nodes. The output from the Atlas file can be visualized graphically or otherwise using TonyPlot and can be exported to SPICE modelling softwares

Procedure to simulate using Atlas

The nitty-gritty of the simulation syntax and procedure is left to the reader. Chapter 2 of the Atlas User's manual provides a good introduction to the software and Chapter 3 provides an overview of the physics and differential equations used in the simulator. This section only seeks to highlight some basic, but important, nuances of using the software.

Any simulation in Atlas requires a device to be simulated. This can either be imported from an Athena process simulation for fabricating the device, or it can be specified in Atlas itself. One can even specify user defined materials to this end, building up from a variety of existing material systems (Refer to **Material** in the **Statements** section of the Atlas User's Manual for the syntax to do this and to the appendices for the available material systems).

The next important step is to define an appropriate mesh. A mesh is actually a collection of several node points placed in the device region and around it, this defines both how accurate and fast the simulation is, as well as the region within which the simulation is carried out. While it is safe practice to include the complete device within the mesh, there might occur scenarios where one may

only wish to simulate a region of the complete device. There are some important points to remember while defining this mesh.

- Mesh definitions aren't arbitrary and are defined as gridlines for x and y axes individually. The nodes are the intersection points of these gridlines.
- Within any given region of change, such as depletion regions where the electric fields are changing or regions with doping, it is a good rule of thumb to include at least 10 grid-lines along the direction of change.
- It is a good practice to at least roughly obtain the dimensions of the regions where expected potential and field changes initially before beginning the meshing.
- To ascertain whether a mesh is accurate enough or not, begin with an initial coarse meshing and increase the density by a factor of 10 along either one or both axes till the results from the iterations of the simulation are within a desired degree of error. If making the mesh finer does not cause significant improvement in the results, then one may return to using the coarser mesh for faster and less intense simulation times.
- One cannot have regions within the mesh that are undefined. Every portion of the meshed region must be defined, even if as air or vacuum.

It is important to place the various statements in order. The first statement after initializing Atlas is to define the mesh, this gives the reference for everything else to be defined and put in place. The x-axis of the mesh is from left to right and the y-axis is from top to bottom. After this the device structure is specified, inclusive of doping region, meshing, materials, contacts and the ilk.

- To tie two contacts together for the complete simulation or otherwise, simply name them the same.
- Shorthand definitions for electrode or region definitions such as top, bottom etc exist. They aren't really of any significant help but are worth taking a look at.
- For certain electrode definitions, it is sufficient just to define the limit of where they interface with the device rather than specify their complete thicknesses.
- Electrode material definitions are important to consider the workfunction otherwise they are ideal ohmic contacts.

One of the most important steps of the device simulation is defining the models. It is good practice to have a qualitative understanding of the models and what processes are involved in the device functioning. This is very important and can be understood either from a study of the device or from referring to an example.

- Never hesitate to refer to examples. Atlas has various examples that provide a lot of information as to what syntax, models or methods to use. In examples, we trust.

Methods refer to how the differential equation will be solved. This usually contributes to the simulation time and resources. The gummel method is fast but is more prone to convergence issues whereas the newton method tends to provide better convergence at the cost of longer simulation times. Refer to the Methods section within the statements chapter of the manual.

- For breakdown simulations, do not forget to include the statement “method carriers=2”. Refer to breakdown within the statements chapter.

Here on out, one may proceed to start the simulations. After that, the results may either be extracted or plotted.

- If convergence errors occur during the simulation, it may be worthwhile reducing the bias step for the simulation or relooking how the device was meshed.
- Sometimes one may see random lines appear in the plot of the device. This can be for one of two reasons.
- (1) The bias step needs to be reduced because at some point in the simulation there was a convergence error and this caused the simulator to cut the bias voltage to an average of the previous successful value and the current one.
- (2) Log files tend to save all the data the simulations generate after the log statement until the next such statement is specified. Running an initialize statement after the simulation ends, or simulating two values far away in succession can cause this issue to happen.
- Sometimes convergence errors may occur if the simulation begins at 0 V, so in such scenarios it helps to simulate a voltage close to it before proceeding to 0 V.
- It sometimes helps to run the simulation to a desired value before the log statement. This is useful in scenarios where we would like a fixed biasing voltage while we sweep over other voltages, for example: We would like to measure iV characteristics at a fixed gate voltage of 6V. It would be unwise to begin initializing the system after we begin recording as this will add some spurious values in our data, which may be undesirable. It may also happen that it leads to a convergence error, so this is sometimes avoidable by simulating the gate voltage to a close value such as 5.5 V prior to the log statement and initializing the gate voltage to 6 V after the log statement.

TonyPlot is used for plotting the characteristics obtained from the log file, or from a str file for showing the device structure with contours and materials as desired.

- One useful feature is the cutline feature accessed by pressing F2. This gives us the graph of the desired data from the device structure along a cross-section
- For obtaining the contours of parameters like fields, potentials, band-diagrams and so on, it is important to specify them in an "output" statement and then run a basic simulation using the "solve" statement . This plots the desired parameters at the values of the biasing specified in the solve statement. "solve init" sets all the biasing conditions to 0.
- To save the data for reference later, the reader is encouraged to use the extract statement, particularly the dat file format (TonyPlot data) and all the data if one wants to record all the simulated data. One can also "on screen" for just the values the user is currently viewing in the plot but this does not allow to view any other plots other than the one being viewed when saved later.

For tips on how to change the graphs obtained from TonyPlot, the reader is directed to the following link- http://www.silvaco.com/tech_lib_TCAD/simulationstandard/2014/apr_may_jun/hints1/hints1.html

Some tips for the reader-

- If the reader wishes to refer to the manual, the most important chapter is the statements chapter. This cannot be overemphasized. While the introduction to Atlas chapter is helpful, once a familiarity with the device simulator has been obtained, the statements chapter provides the best reference to any doubts regarding statements and has many useful links to the physics or equations involved.

- The examples are extremely helpful in learning the software. It provides a lot of information with regards to syntax, device characteristics, models, methods and physics. The user can save a lot of his time by studying the examples in detail.

- If the simulation runs into memory management errors, it is advisable to attempt running the simulation once or twice more as the issue tends to sort itself out sometimes. If not, the user is advised to reduce mesh density.

- Do not mesh indiscriminately. The simulations may end up taking hours to finish depending on the method being used.

- It is wise to save the simulation codes used for different results rather than constantly modifying the same file over and over. This may seem self-evident but is easy to overlook. This helps save time and also provides a reference if one would like to refer to a method he may have tried once.

- Never hesitate to ask for help. You're here to learn and it'll be surprising to see how many people you may meet who are willing to assist you. Sometimes problems that may have stumped you for a long time may yield solutions during a discussion.

2.4 Objectives of the Thesis

The objectives of the current thesis are to study a vertically grown MBE based IGBT structure that has been fabricated at the University of Stuttgart and to validate the characteristics of the fabricated device and to provide a simulation analysis of the modified device improved by changing the Homogenous Channel Layer to a Locally Doped Channel.

3. VERTICAL CHANNEL IGBT

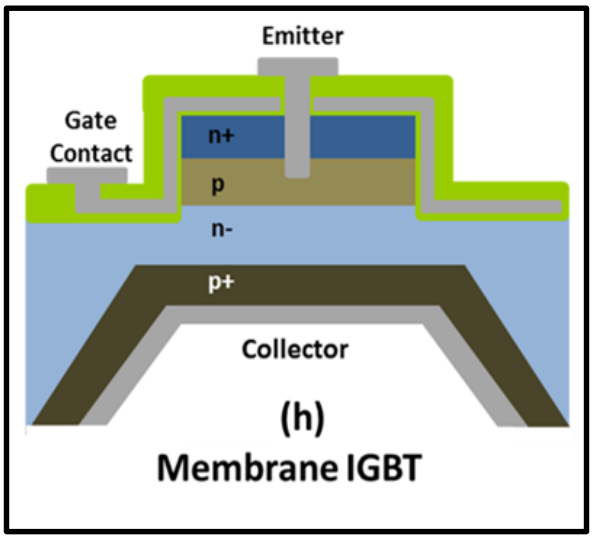


Fig 13: Cut-section of device fabricated at Stuttgart

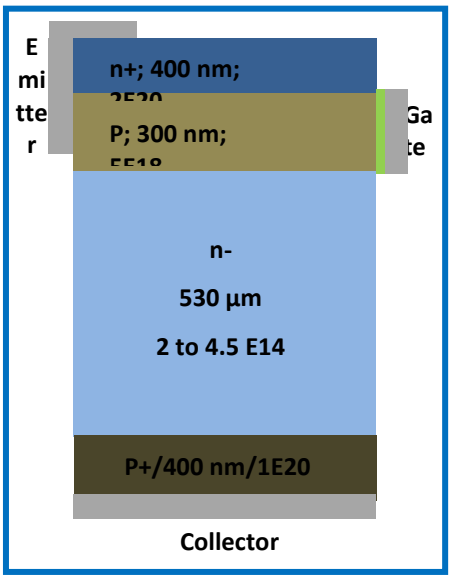


Fig 14: Proposed schematic of device fabricated at Stuttgart – Prior to correcting the dimensions of the drift region

Our work aimed to study a novel structure for a vertical IGBT that is constructed using an MBE process. The reason for this is that MBE provides a greater flexibility with respect to the fabrication process and that the fabrication team that approached us was an MBE team. The work of the IIT-M team involved simulating the device they fabricated for the purposes of studying them and predicting the behaviour of proposed structures.

Fig. 13 shows the cut-section of the initial device fabricated at IHT, University of Stuttgart. This is referred to as the Homogenously Doped Channel (HDC) IGBT henceforth. This comes from the fact that the channel region of the IGBT has a uniform doping profile.

Initial work at Stuttgart involved the designing and fabricating the basic structure shown in Fig. 13 and preliminary simulations and characterization. They approached IIT-M for carrying out the simulations as they felt they weren't well equipped for their foray into power semiconductor devices.

3.1 Homogenously Doped Channel (HDC) IGBT

3.1.1 Device Structure

This device is similar to the trench IGBT structure except that the fabrication here is by an MBE process. The schematic of the device used for simulation is given in Fig. 14. One can notice that the structure, though resembling the vertical IGBT, is different in the MOSFET region. This occurs in

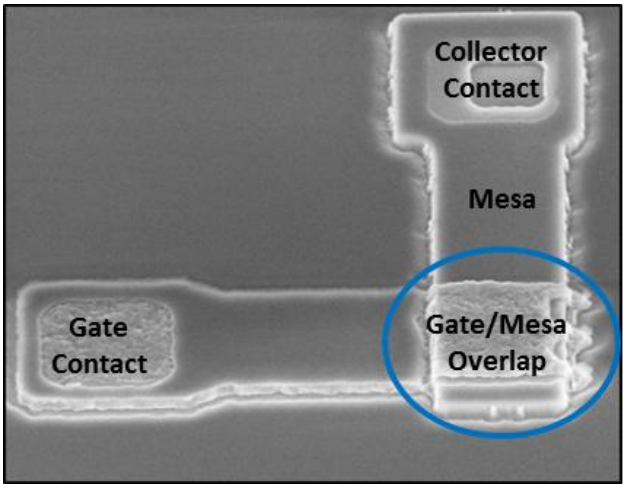


Fig 15(a): Tilted SEM image of fabricated IGBT

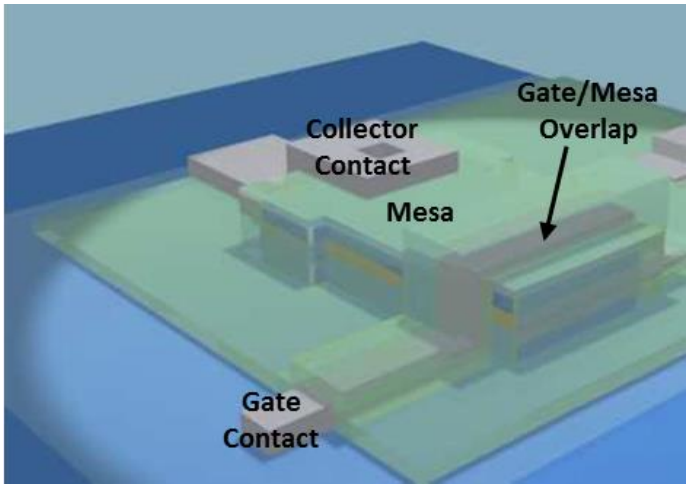


Fig 15(b): 3D image of IGBT

the vertical direction rather than the conventional vertical dimension, this is known as a "trench" structure.

The dimensions have been chosen by iterative testing at Stuttgart. Do note that the substrate thickness of 530µ is an error in communication, this highlights the reason why they required a simulation team familiar with device physics concepts. This was due to the device having different thicknesses on different parts of the substrate, being 530µ and ~100µ. The fabrication team was unsure as to what thickness to specify for the device simulation and the actual thickness was divined from looking at their preliminary simulation files before making the correction from our side.

The regions are evident from the figure and their functions have been discussed earlier. The electrodes for the device are worth discussing though. The collector is as usual, but the emitter extends to only a small portion of the top and left of the device. This is actually a translation of the 3-D mesa structure into a structure that can be simulated. The gate electrode is vertically aligned and the oxide is PECVD grown with a thickness of 20nm. The emitter and gate electrode do not touch, this is shown in Fig. 15. The emitter contact shorts the region under the gate so as to eliminate body effects.

In the 3D figure, it is interesting to note the gate contact. It wraps around the device as a finger contact. The gate extending over the emitter region is not much of a problem but it is essential for some portion of it to extend over the drift region. The collector contact is on a mesa region away from the gate of the device. This creates a lateral current flow till the gate before flowing vertically to the collector.

One is to note that this structure is constrained by the existing masks and techologies used at the Stuttgart university and therefore presents itself as odd. This structure was fabricated as a proof of concept to demonstrate the effectiveness of a locally doped channel IGBT and superjunction IGBT over the homogenously doped IGBT.

Fig. 16 shows the results of characterising the HDC IGBT. One notices that the forward characteristics are conventional of an IGBT though the reverse characteristics shows a poor performance. This is considered to be due to scratching on the bottom of surface of the fabricated device due to wear and tear during the process causing a short with the collector electrode and the drift region in some regions and with the collector at other regions on the wafer. This is considered the most probably cause given that the bottom collector junction is only 400nm thick. The German team has proposed methods to circumvent this issue and is currently working on the fabrication of this and other IGBT devices. We shall now outline the fabrication method for the HDC IGBT.

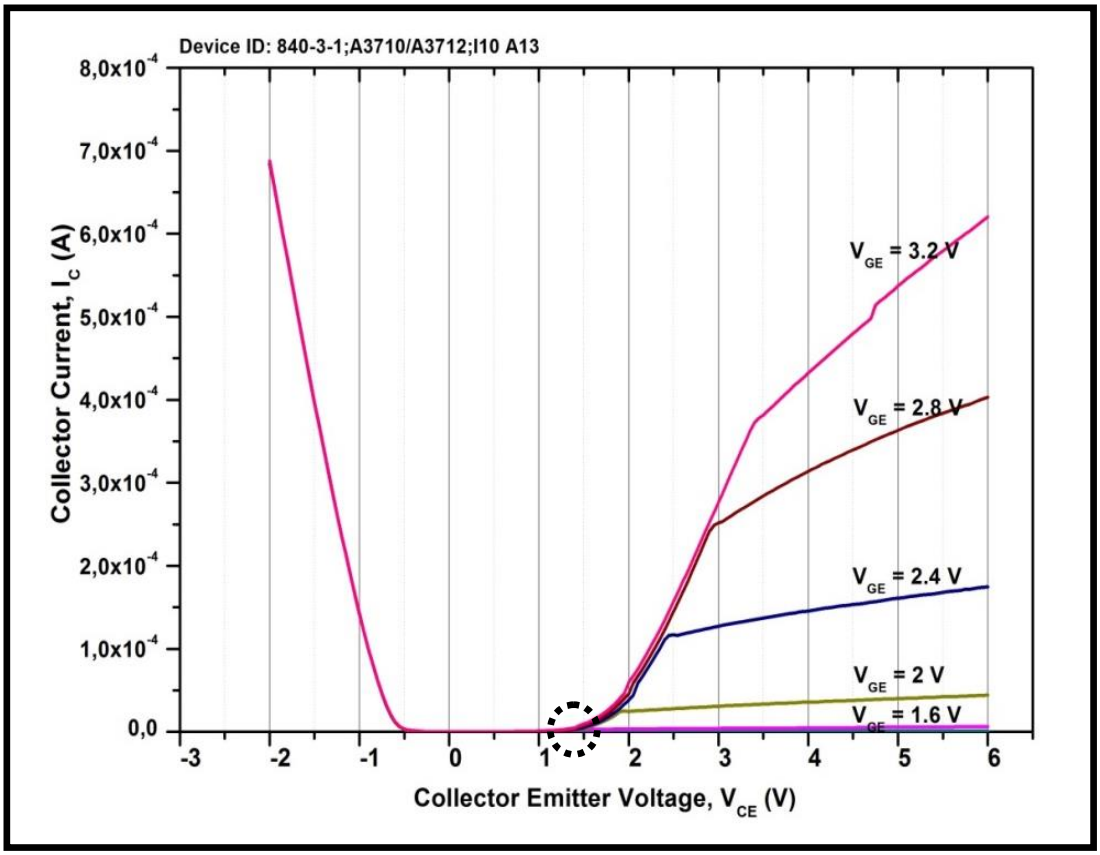


Fig 16: Experimental characterization of the fabricated IGBT at IHT

Ic – Vce characteristics of the HDC IGBT

3.1.2 Fabricating the HDC IGBT

1. Wafer Selection: **n-** Si (2 to 4.5 x $10^{14}/cm^3$); Thickness: 530

2. SiO_2 deposition on front and back side of the wafer, followed by Photoresist coating on both the sides.

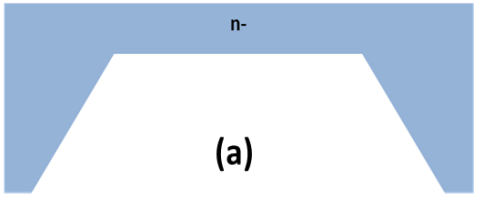
3. Photoresist pattern on back side of the wafer and oxide etch by BHF.

4. Photoresist removal.

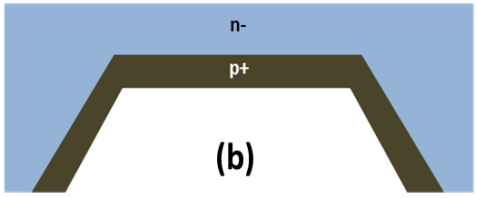
5. Si etch in TMAH.

6. Oxide Removal. Substrate is ready for device fabrication.

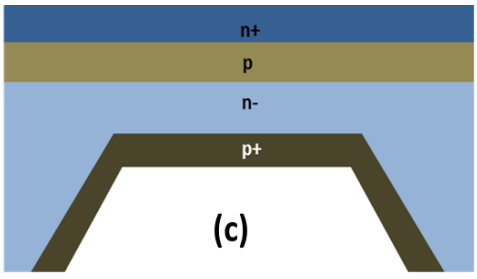
So far, we have been processing the backside of the wafer and now we shall outline the steps involved in processing the rest of the chip. This involves flipping the wafer over. Do note that in the steps mentioned above, the ridges are as shown for the whole chip and that doesn't signify a recurring pattern of valleys. For the fabricated devices there are two such valleys in both directions on a square substrate, giving us effectively four such valley regions.



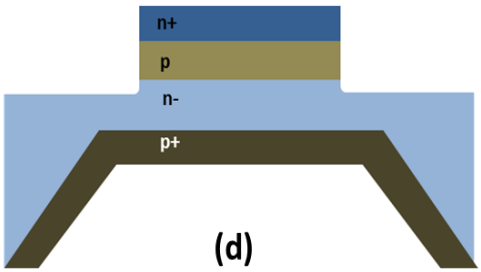
a. Back side etched 70 µm thick membrane wafer which is the starting material (lightly doped n type Si drift region)



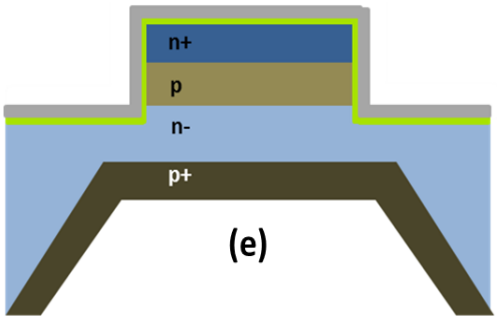
b. **Collector Fabrication:** Epitaxial growth of Boron doped Si on the back side of membrane by MBE



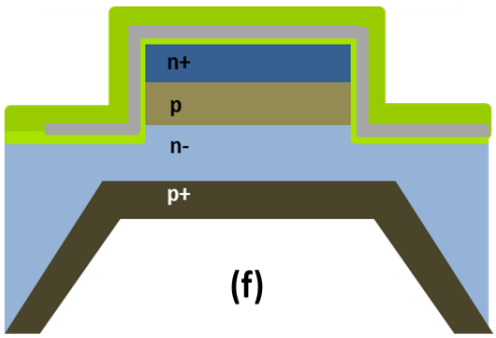
c. **Channel & Emitter Fabrication:** Epitaxial growth of Boron doped Si (channel) on the front side of membrane followed by the growth of highly Sb doped Si (Emitter) by MBE. It should be noted that we employed only MBE to fabricate the entire IGBT and no Diffusion or Ion Implantation processes are used.



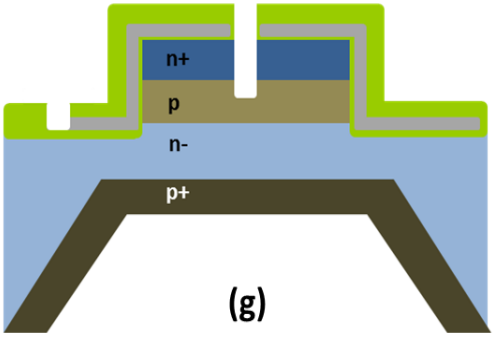
d. **Mesa Fabrication:** Patterning and reactive ion etching of the n+ and p layers



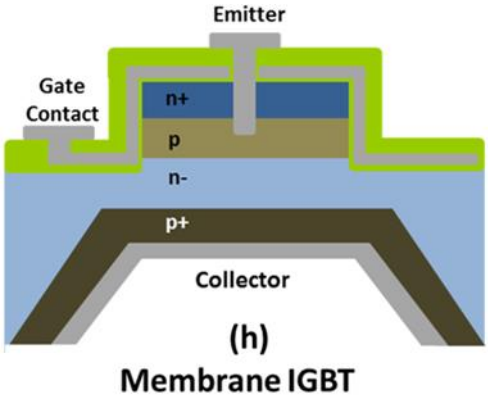
e. **Gate Fabrication:** Deposition of 20 nm thick low temperature SiO_2 for gate oxide using ICPCVD followed by deposition of Aluminum Gate.



f. **Passivation:** Patterning and etching of Gate metal. Deposition of low temperature passivation oxide



g. **Via-hole Fabrication:** Patterning and etching of via hole. Deep etching of Emitter window to short emitter and body. Refer to Fig. 15



h. **Contact Fabrication & Final Device:** Aluminum metal deposition, patterning and etching of Aluminum for final contacts.

We shall now move on to describing the next step of our study, the Locally Doped Channel (LDC) IGBT.

3.2 Locally Doped Channel (LDC) IGBT

3.2.1 Device structure

The Locally Doped Channel IGBT is named so because of how the channel is doped in the IGBT device. The schematic of the device we study is given in Fig. 17. Compared to the HDC IGBT where the channel has a uniform doping throughout the channel, the LDC IGBT has an intrinsic channel doping with a delta doping layer within it. While not perfectly intrinsic, the doping in the channel is indicative of the process and fabrication restrictions. This layer is grown by an MBE process and varies in thickness from 3nm – 8nm. While there isn't a reliable fabrication process yet for this device, the testing of a proposed methodology is currently underway.

The structure of this device schematic is similar to the HDC IGBT with the only difference being the channel region. The doping of the delta layer is approximately $5x10^{19}/cm^3$. We shall now outline the reasoning behind the δ-doping feature.

3.2.2 Local Doping in Channels

For this section we shall particularly refer to the paper "Electric Field Tailoring in MBE-grown sub-100nm MOSFETs" by W. Hansch et al. This paper talks about the advantages provided by the local doping profile in a MOSFET channel. Electric field tailoring particularly refers to modifying the electric field within the channel to provide effects that are considered desirable. This field is dependent on the doping profiles in the device as well as the applied voltages. While the applied voltages determine the device ratings and performance, tinkering with the doping profile provides us with a greater flexibility and freedom with the device voltage and current ratings.

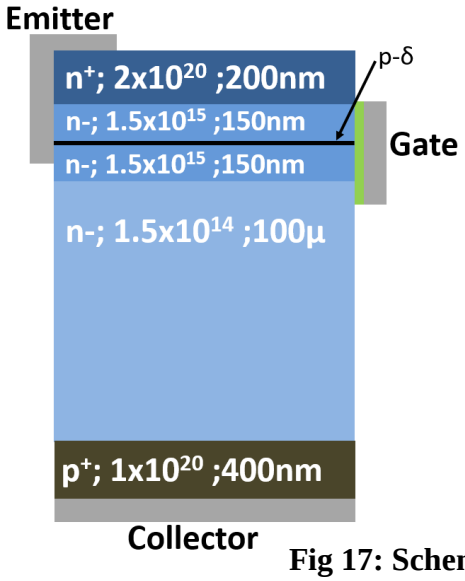


Fig 17: Schematic of the LDC IGBT
δ-layer doping is $5x10^{19}/cm^3$

Fig 18:

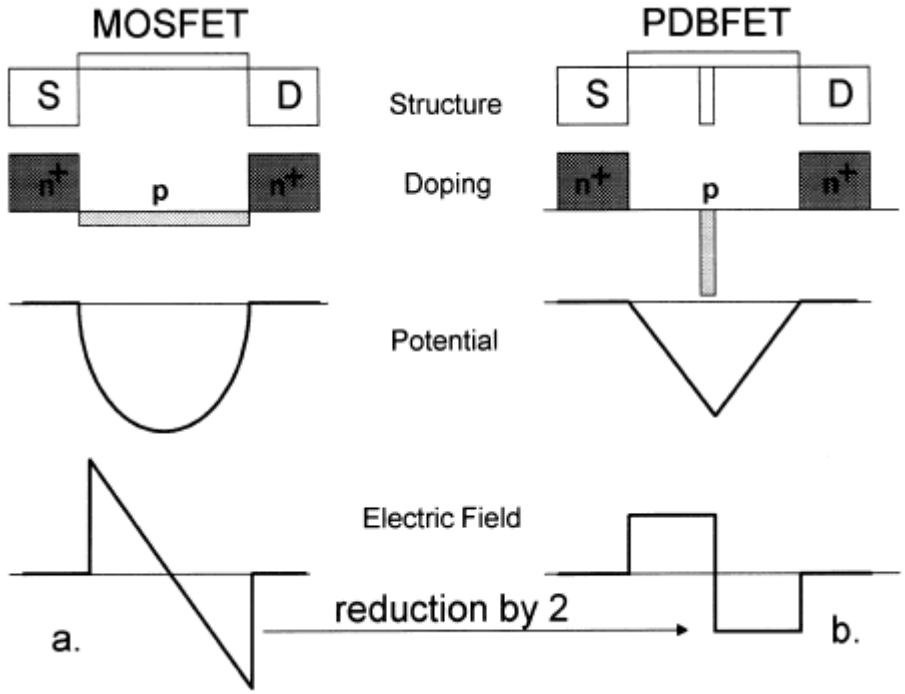


Fig 18: Potential and Electric Field profiles in (a) Homogenously doped channel and (b) Locally Doped Channel

Fig. 18 shows the theoretically expected potential and electric fields in the channel of a MOSFET device with homogenous doping and local doping profiles. Within the uniformly doped channel the potential exhibits a parabolic profile and the electric field a triangular profile. The locally doped channel, with the local doping symmetrically placed at the centre of the channel, the potential exhibits a triangular profile and the respective electric field as evident in Fig. 30.

The electric field normal to the gate determines the confinement of carriers to the inversion layer (interface layer) in the channel region. For the homogenously doped channel, with constant contact voltages, this is likely to occur towards the drain end (assuming that the source is taken as the reference at ground), whereas for the locally doped channel, this clearly occurs at the locally doped layer. The electric field under similar bias conditions is shown to be reduced by a factor of 2 for the local doping in the paper. This reduces surface scattering effects as the electric field is more spread out from the surface for the locally doped channel.

Another thing to note is the lateral electric field. In uniformly doped channels under a bias, the maximum electric field is attained at the drain end of the channel. This is also where carriers exhibit velocity saturation. As channel lengths grow smaller, hot-carrier effects tend to become more prominent and the tendency of the device to breakdown also increases.

In the locally doped channel, this is subverted by means of the doping profile. The local doping causes the maximum field to occur within the channel, leading to the carrier velocity overshoot to

occur within the channel too. This implies that the carriers travel with a faster velocity in the channel as compared to the uniformly doped channel, thus leading to shorter travel times. This, combined with the intrinsic doping in the channel, gives rise to higher electron mobility. This doping profile also shows a higher velocity overshoot and suppressed avalanche breakdown activity. This essentially means the locally doped channel exhibits better conduction and breakdown characteristics.

3.3 Simulation Results and discussion

This section will talk about the results we have obtained and the methodology involved. It shall also go into a discussion on what the results imply. This section not only hopes to present and discuss the results obtained but also talk on the methodology that may be employed in arriving at the results reliably. While this isn't the exact methodology followed during the course of this study, it represents what the author considers a good procedure after personally following an iterative process that is more roundabout.

Before simulating the device

Before actually beginning to work on the device, it is important to first calibrate the simulator. It is always unwise to begin working with the main project as troubleshooting becomes harder than it needs to be. It also makes it hard to know whether the results from the simulation are reliable or not. It is for this reason that baby steps are both important and advised.

Initial simulations do require some amount of analytical analysis. To begin with, start with a uniformly doped semiconductor block. Analytically study the expected currents and voltages to cross-verify the simulation results. If the results don't match, one is advised to relook the models and numerical method involved.

The next step would be to study the p-n junction, after which one would be advised to look at a BJT or MOSFET structures provided in a standard text and simulate them. This especially provides one with the opportunity to look at the various models that the simulator provides and study their particular nuances.

While there are many methods to reliably simulate the device, one particular method is highlighted here. To simulate the HDC IGBT shown in Fig. 19, it is suggested to begin the simulation adding layer by layer.

So to say, one is advised to begin with the drift layer or emitter layer with contacts on either side. From there, an adjoining layer can be added, the simulation is then that of a p-n junction. The next step would be the simulation of a BJT or MOSFET. This also lets one study the effect of the layer lengths, for instance, of the drift region. It is an interesting study to see the device performance change as the drift region length increases. After that one may proceed to finally simulate the IGBT device.

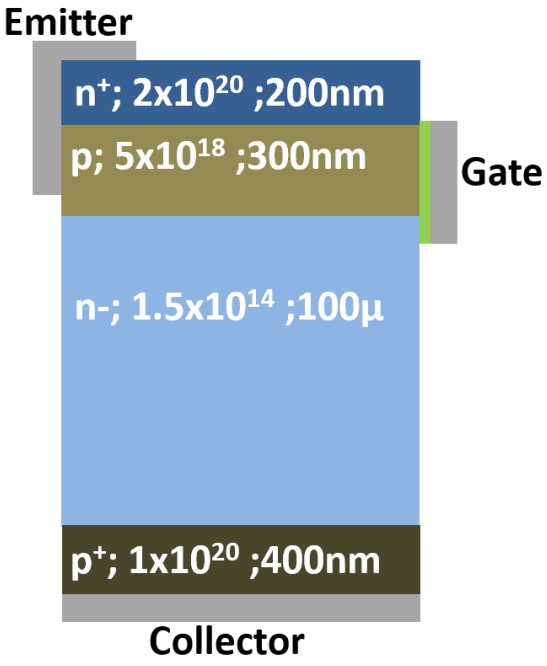


Fig 19: HDC IGBT

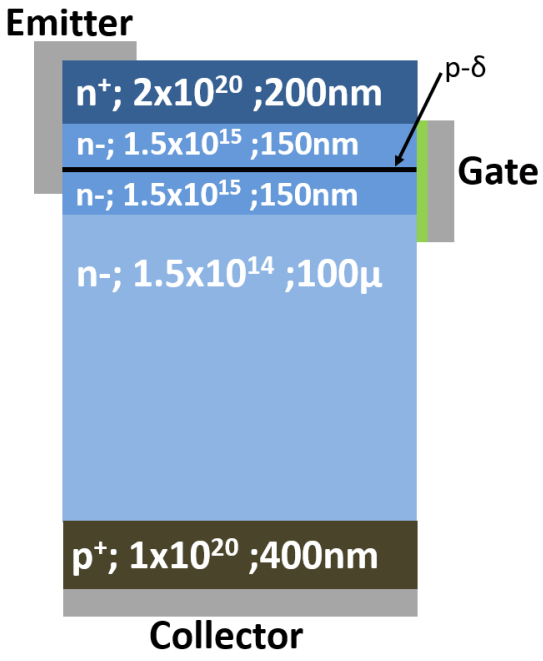


Fig 20 :LDC IGBT

Results and Discussion section

This section will devote itself to presenting the results from the simulations of the HDC and LDC IGBT devices. It won't go into detail on all the results that are considered unsuccessful but seeks to be succinct. Fig. 20 shows the schematic of the HDC and LDC IGBTs, and Fig. 33 gives the doping profile within the channel. Initial work was on trying to calibrate the simulation results with the experimental results in the forward direction. Fig. 22 represents the I_C-V_{CE} characteristics for the device initially simulated. The current here is normalized with respect to the thickness, but as is evident, it is many magnitudes lower than the experimental results. This was the result of a miscommunication which was later corrected.

Fig. 23 represents the results obtained for the characteristics after making the requisite corrections. This is the current normalized with respect to the thickness as before. The improvement in the characteristics is self-evident. This involved correcting the dimensions and also varying the models, workfunction and lifetime parameters. The graph is substandard due to the fact that these were initial runs and the issues were fixed later. The basic models were taken from the IGBT device examples bundled with the ATLAS software.

The final models used in the simulation include:

- No-fixed charges at the semiconductor-oxide interface

- SRH recombination
- Drift-diffusion transport
- Bandgap narrowing
- Concentration dependent mobility
- Impact ionization for breakdown simulations

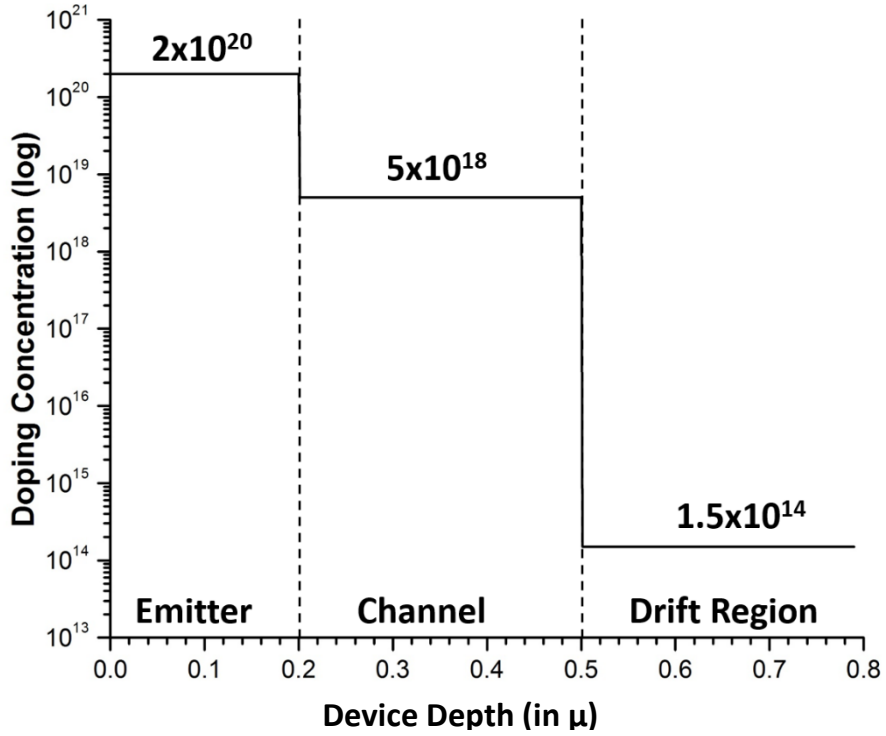
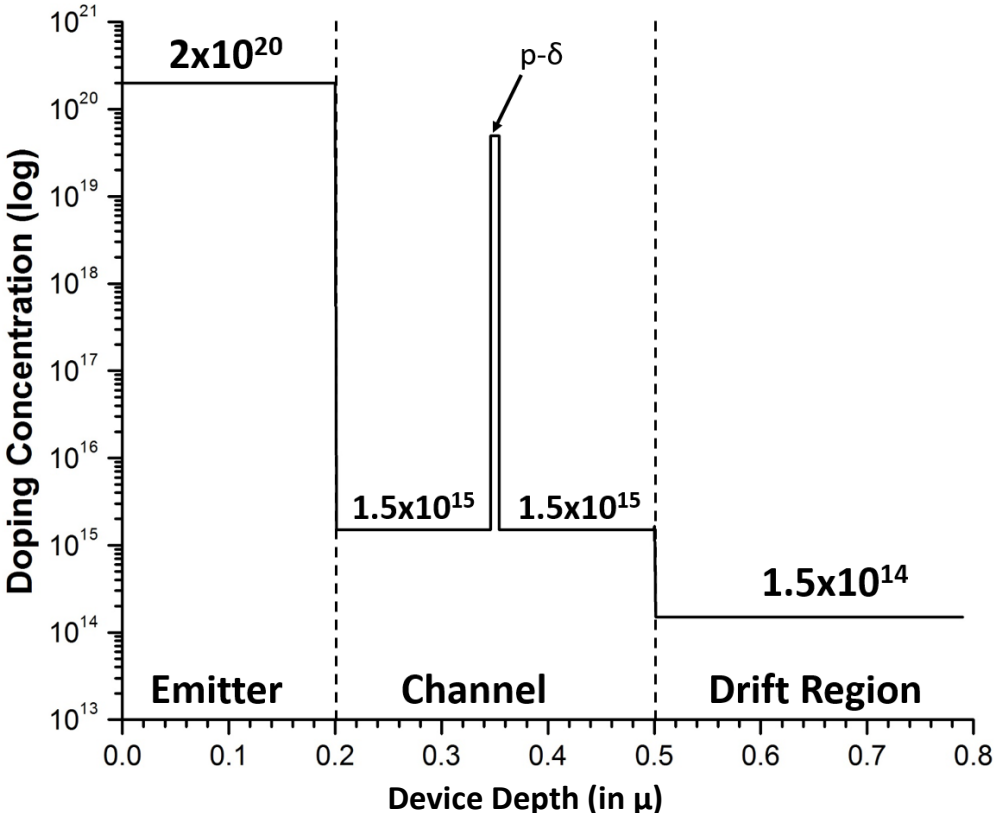


Fig 21(a): HDC IGBT Doping Profile



.

Fig 21(b): LDC IGBT Doping Profile

We shall now proceed to only discuss final results. It would be tedium to go into the details of arriving at these results and for the purposes of this section, irrelevant too. For anyone interested in the complete set of results and work files, they shall be uploaded to an online repository and the link will be provided in the bibliography.

Fig. 22 shows the final results together for the I_C-V_{CE} characteristics of the HDC IGBT and LDC IGBT and the improvement is self-evident. Compared to the HDC IGBT, the LDC IGBT demonstrates a current that is 4-5 times higher and also shows a reduced voltage drop for a given current.

Fig. 23 shows the results for the transfer characteristics of the devices. Here too, one notices the improvement in the lower threshold voltage and a significantly higher current for a given voltage. The reason for the low threshold voltage also has to do with the design and thickness of the individual devices. Both devices are simulated with the same dimensions so as to observe the immediate impact of the doping profiles and it is very easy to modify other parameters individually.

The electric fields obtained within the channel are presented in Fig. 24 and Fig. 25. These were taken at the gate-semiconductor interface. The electric field contours for the same are presented in the following two figures.

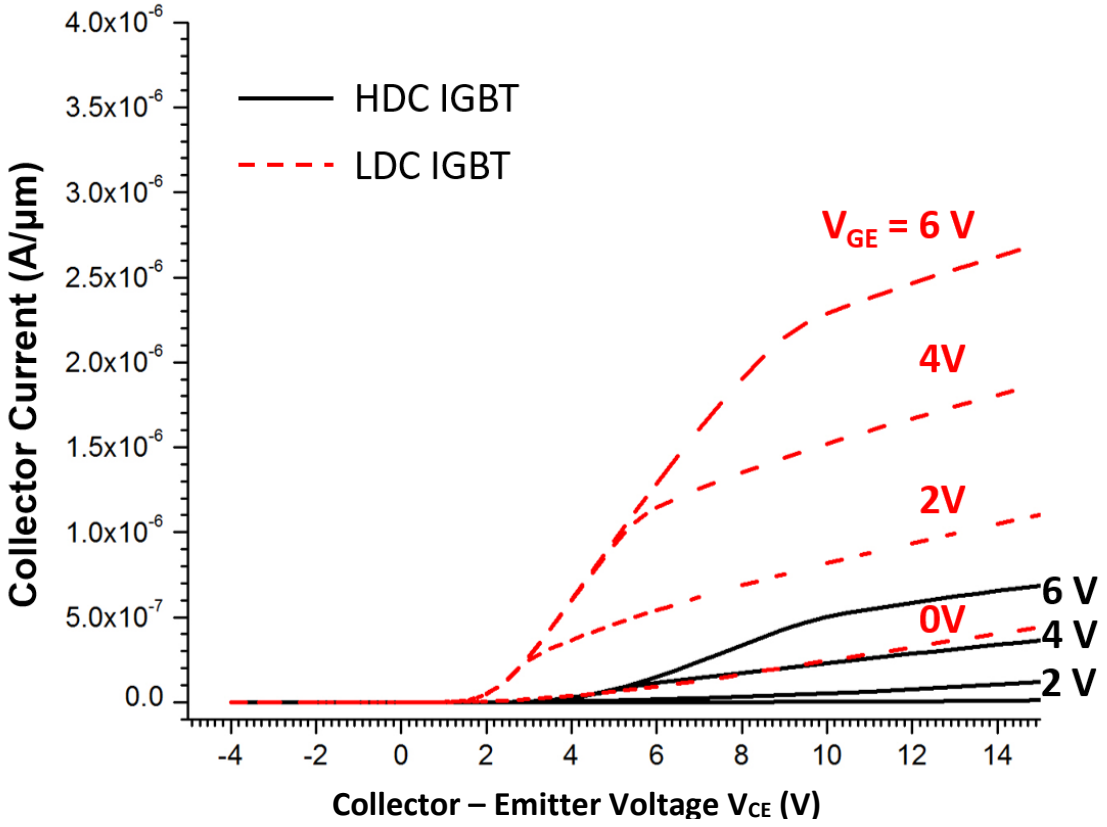


Fig. 22: I_C-V_{CE} characteristics of the HDC IGBT and LDC

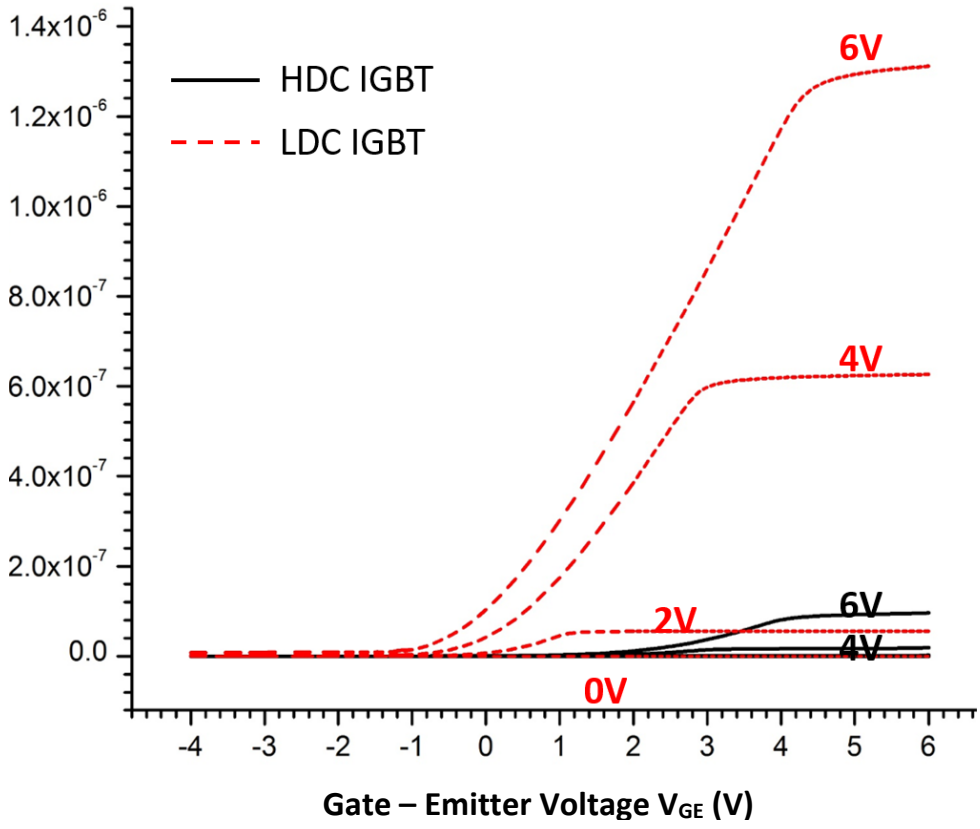


Fig. 23: Transfer characteristics of the HDC IGBT and LDC IGBT

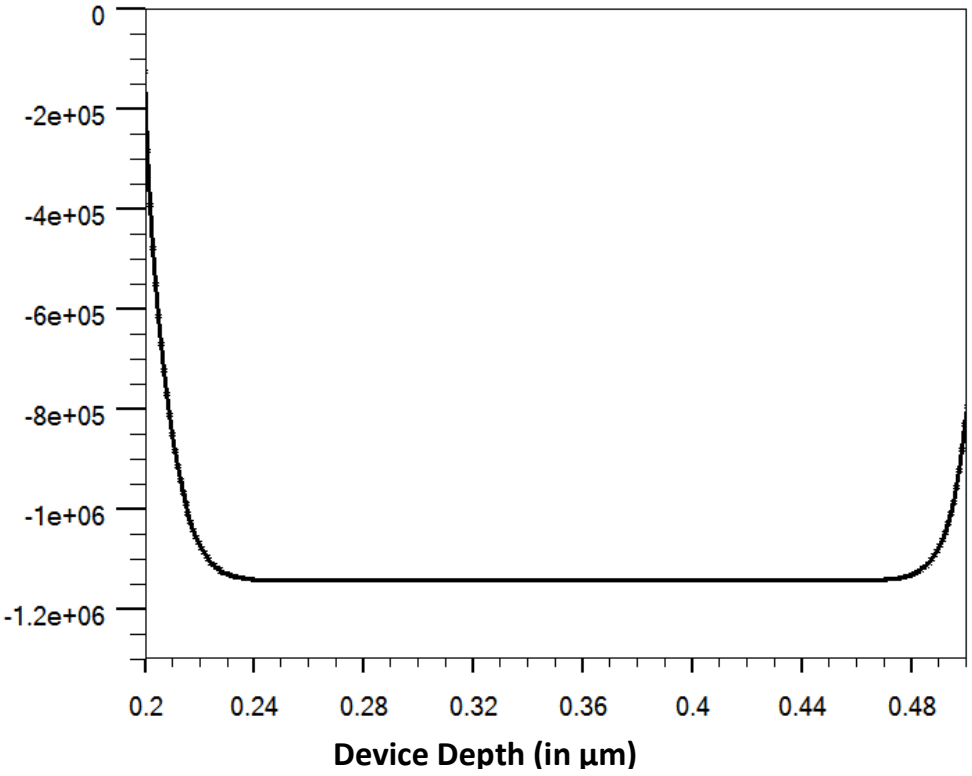


Fig 24: Electric Field in the channel for HDC IGBT

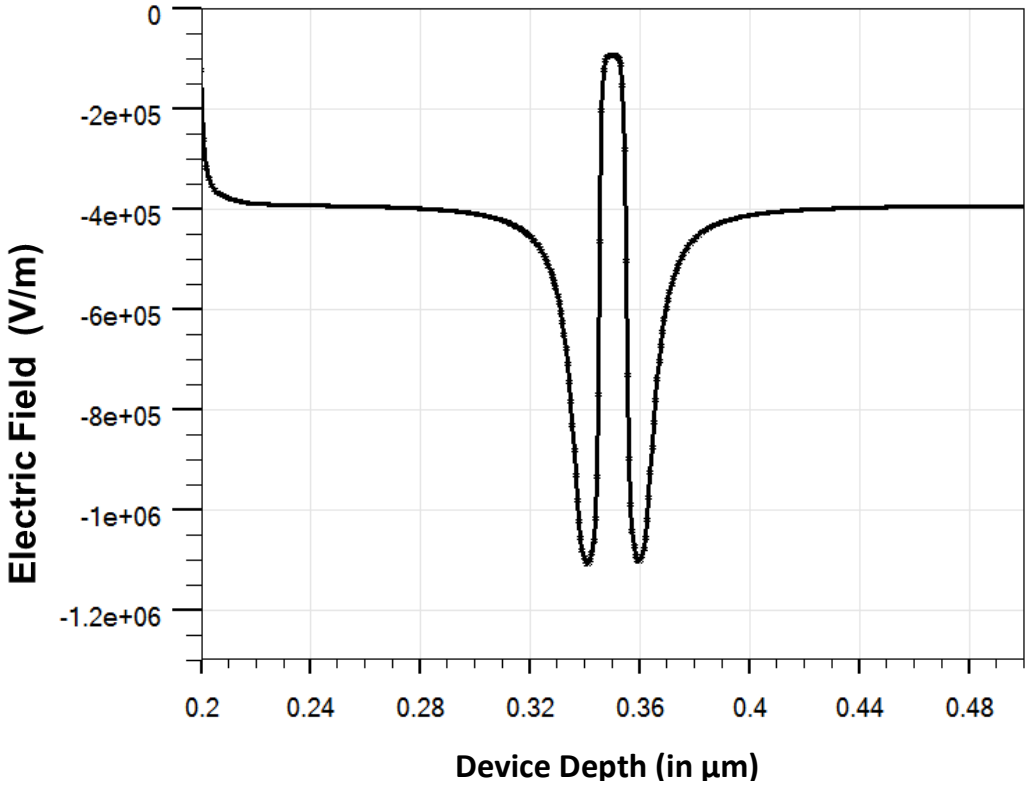


Fig. 25: Electric Field in the channel for LDC IGBT

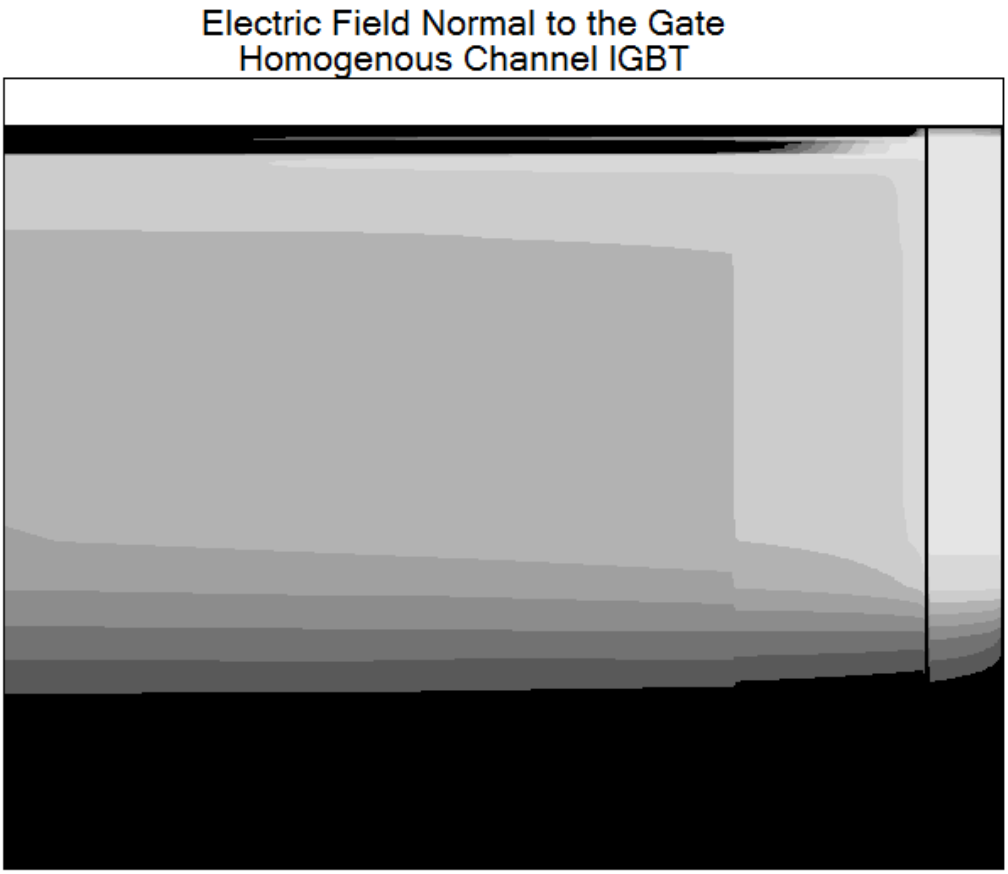


Fig 26: Electric Field contours in the channel for HDC IGBT

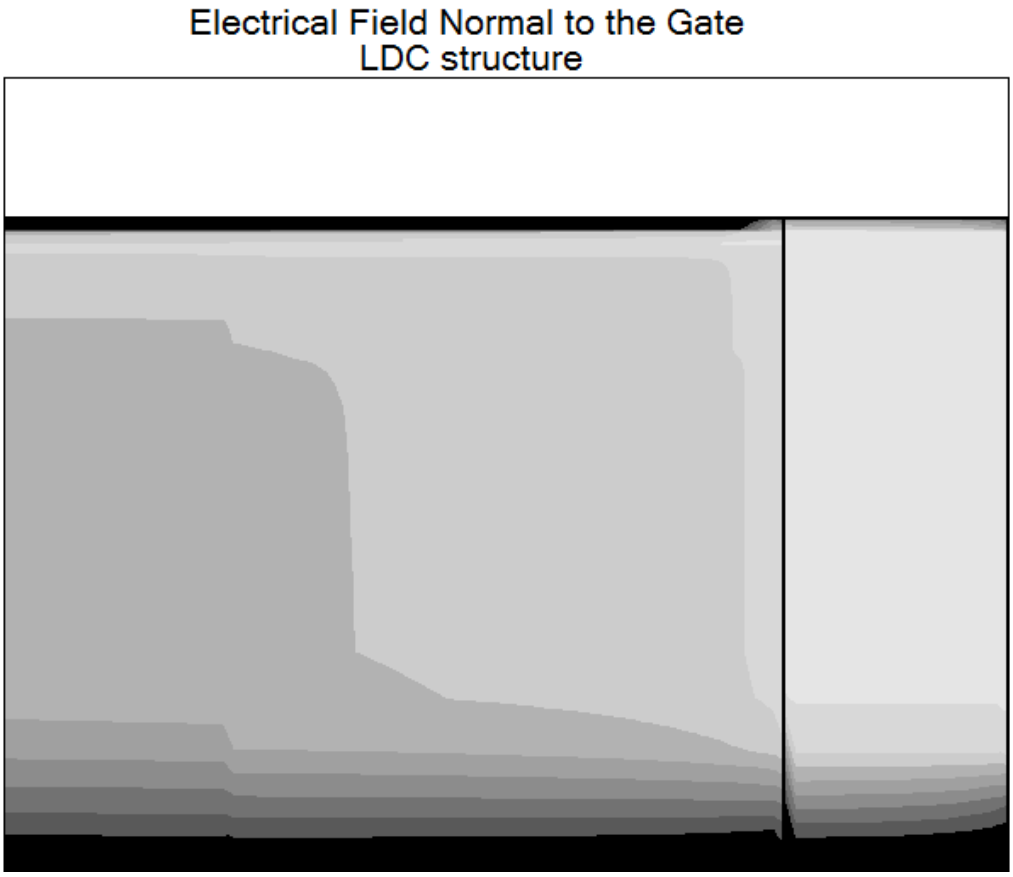


Fig 27: Electric Field contours in the channel for LDC IGBT

4. CONCLUSIONS

The LDC IGBT represents the logical next step from the HDC IGBT. This, in fact, works as a very useful improvement that can be applied over a whole gamut of device structures. The local doping presents itself as an effective tool in devices grown using MBE. This is due to the fact that with conventional diffusion processes do not give us effective tools to create sharp doping profiles unlike MBE which is more useful and accurate in creating sharp doping profile within sub-micron devices.

The immediate advantages provided by changing the doping profile are self-evident from the results. There has been preliminary work done on the breakdown characteristics and further work can include a more detailed analysis on the breakdown and switching characteristics of the device. The logical conclusion of this work was to study the characteristics of the superjunction IGBT but this is left to posterity.

The fabrication of the LDC IGBT is underway and the validation of the characteristics with the simulated characteristics presents itself as another area of future work.

References

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[8]. Silvaco user manuals for Atlas and TonyPlot

[9]. **For all files and results, contact the author of the report or visit link:**

https://drive.google.com/file/d/0B0VW-73fQXGKdkxVUndRdno5MUU/view?usp=sharing

Appendix A: Silvaco ATLAS codes

1. I_C-V_{CE} Characteristics

```
go atlas

mesh

x.m l=0.0  spac=0.1
x.m l=1.5 spac=0.1
x.m l=1.99  spac=0.1
x.m l=2.02 spac=0.1

y.m l=0.0   spac=0.1
y.m l=0.15   spac=0.1
y.m l=0.2 spac=0.001
y.m l=0.34   spac=0.0001
y.m l=0.4   spac=0.0001
y.m l=0.5  spac=0.001
y.m l=0.55 spac=0.01
y.m l=2.0 spac=20.0
y.m l=100.0   spac=40.0
y.m l=100.4 spac=0.1
y.m l=100.9 spac=0.1

region num=1 silicon x.min=0.0 x.max=2.0  y.min=0.0 y.max=100.9
region num=2 oxide   x.min=2.0 x.max=2.02 y.min=0.0 y.max=100.9
#region num=3 x.min=2.0 x.max=2.02 y.min=0.0 y.max=0.4  user.material=empty
#region num=4 x.min=2.0 x.max=2.02 y.min=2.0 y.max=100.7  user.material=empty

electrode name=emitter1 x.min=0.0 x.max=2.0 y.max=0.0
electrode name=emitter2 x.max=0.0 y.min=0.0 y.max=0.6
electrode name=gate    x.min=2.02 y.min=0.2 y.max=2.0
electrode name=collector x.min=0.0 x.max=2.0 y.min=100.9

doping uniform n.type conc=2.0e20 x.left=0.0 x.right=2.0 y.min=0.0   y.max=0.2

#Channel Doping
#doping uniform p.type conc=5.0e18 x.left=0.0 x.right=2.0 y.min=0.2   y.max=0.5
doping uniform n.type conc=1.5e15 x.left=0.0 x.right=2.0 y.min=0.2   y.max=0.5
doping uniform p.type conc=5e19 x.left=0.0 x.right=2.0 y.min=0.346 y.max=0.354

doping uniform n.type conc=1.5e14 x.left=0.0 x.right=2.0 y.min=0.5   y.max=100.5
doping uniform p.type conc=1.0e20 x.left=0.0 x.right=2.0 y.min=100.5 y.max=100.9


contact name=gate aluminum

mater region=1 taup0=1e-6 taun0=1e-6

#interface charge=3.0e12 x.min=1.95 x.max=2.02 y.min=0.0 y.max=1.0


#material material=empty user.group=insulator user.default=oxide permittivity=1e-10

models   analytic srh auger conmob surfmob bgn
#impact   selb

output ey.field ex.field band.temp con.band val.band

output     e.field j.electron j.hole j.conduc j.total ex.field \
       ey.field jy.electron \
```

```
    impact


#solve init



method newton trap climit=1e-5 maxtraps=8

solve init
solve vgate=4.0
solve vcollector=10.0
solve vemitter1=0.0
solve vemitter2=0.0


solve vcollector=0.0 vemitter1=0.0 vemitter2=0.0 vgate=0.0

save outf=dev.str
tonyplot dev.str

quit
```

2. Transfer Characteristics

```
go atlas

mesh

x.m l=0.0  spac=0.1
x.m l=1.95 spac=0.1
x.m l=1.99  spac=0.01
x.m l=2.02 spac=0.01

y.m l=0.0   spac=0.1
y.m l=0.15   spac=0.1
y.m l=0.19 spac=0.01
y.m l=0.339 spac=0.01
y.m l=0.34   spac=0.0001
y.m l=0.355   spac=0.0001
y.m l=0.4   spac=0.1
y.m l=0.48  spac=0.1
#y.m l=0.4888124 spac=0.0011876
#y.m l=0.5   spac=0.011876
y.m l=0.55 spac=0.001
y.m l=2.0 spac=0.1
y.m l=5.0 spac=0.5
y.m l=10.0 spac=1.0
y.m l=30.78   spac=5.0
y.m l=90.0    spac=5.0
y.m l=95.0    spac=0.5
y.m l=100.0   spac=0.1
y.m l=100.499999999 spac=0.01
#y.m l=100.5 spac=0.012654
#y.m l=100.500012654 spac=0.000012654
y.m l=100.9 spac=0.1

region num=1 silicon x.min=0.0 x.max=2.0  y.min=0.0 y.max=100.9
region num=2 oxide   x.min=2.0 x.max=2.02 y.min=0.0 y.max=100.9
#region num=3 x.min=2.0 x.max=2.02 y.min=0.0 y.max=0.4  user.material=empty
#region num=4 x.min=2.0 x.max=2.02 y.min=2.0 y.max=100.7  user.material=empty

electrode name=emitter1 x.min=0.0 x.max=2.0 y.max=0.0
electrode name=emitter2 x.max=0.0 y.min=0.0 y.max=0.6
```

```
electrode name=gate    x.min=2.02 y.min=0.2 y.max=2.0
electrode name=collector x.min=0.0 x.max=2.0 y.min=100.9

doping uniform n.type conc=2.0e20 x.left=0.0 x.right=2.0 y.min=0.0   y.max=0.2

#Channel Doping
doping uniform p.type conc=5.0e18 x.left=0.0 x.right=2.0 y.min=0.2   y.max=0.5
#doping uniform n.type conc=1.5e15 x.left=0.0 x.right=2.0 y.min=0.2   y.max=0.5
#doping uniform p.type conc=5.0e19 x.left=0.0 x.right=2.0 y.min=0.346 y.max=0.354

doping uniform n.type conc=1.5e14 x.left=0.0 x.right=2.0 y.min=0.5   y.max=100.5
doping uniform p.type conc=1.0e20 x.left=0.0 x.right=2.0 y.min=100.5 y.max=100.9


contact name=gate aluminum

mater region=1 taup0=1e-6 taun0=1e-6

#interface charge=3.0e12 x.min=1.95 x.max=2.02 y.min=0.0 y.max=1.0


#material material=empty user.group=insulator user.default=oxide permittivity=1e-10

models   analytic srh auger conmob surfmob bgn
#impact   selb

output ey.field ex.field band.temp con.band val.band

#output     e.field j.electron j.hole j.conduc j.total ex.field \
       ey.field jy.electron \
       impact


#solve init

#save outf=dev.str
#tonyplot dev.str

#trap climit=1e-5 maxtraps=8
method newton trap climit=1e-5 maxtraps=8

solve init
solve vcollector=0.0
solve vemitter1=0.0
solve vemitter2=0.0
solve vgate=0.0

solve vcollector=0.0 vemitter1=0.0 vemitter2=0.0 vgate=0.0

solve init
solve vcollector=0.0 vemitter1=0.0 vemitter2=0.0

#rev current
log outf=sim0.log master
solve vcollector=0.0
solve vgate=0 vstep=-0.1 vfinal=-0.5 name=gate
solve vgate=-0.5 vstep=-0.5 vfinal=-4.0 name=gate
solve vgate=-2.0 vstep=0.1 vfinal=0.0 name=gate

solve vgate=0.0 vstep=0.1 vfinal=2.0 name=gate
solve vgate=2.0 vstep=0.05 vfinal=6.0 name=gate
#solve vgate=6.0 vstep=0.25 vfinal=15.0 name=gate

solve init
solve vcollector=0.0 vemitter1=0.0 vemitter2=0.0

log outf=sim2.log master
```

```
solve vcollector=2.0

solve vgate=0 vstep=-0.1 vfinal=-0.5 name=gate
solve vgate=-0.5 vstep=-0.5 vfinal=-4.0 name=gate
solve vgate=-2.0 vstep=0.1 vfinal=0.0 name=gate

solve vgate=0.0 vstep=0.1 vfinal=2.0 name=gate
solve vgate=2.0 vstep=0.05 vfinal=5 name=gate
solve vgate=5.0 vstep=0.05 vfinal=6.0 name=gate


solve init
solve vcollector=0.0 vemitter1=0.0 vemitter2=0.0

log outf=sim4.log master
solve vcollector=4.0
solve vgate=0 vstep=-0.1 vfinal=-0.5 name=gate
solve vgate=-0.5 vstep=-0.5 vfinal=-4.0 name=gate
solve vgate=-2.0 vstep=0.1 vfinal=0.0 name=gate


solve vgate=0.0 vstep=0.1 vfinal=2.0 name=gate
solve vgate=2.0 vstep=0.05 vfinal=6.0 name=gate
#solve vgate=6.0 vstep=0.25 vfinal=15.0 name=gate


solve init
solve vcollector=0.0 vemitter1=0.0 vemitter2=0.0

log outf=sim6.log master
solve vcollector=6.0

solve vgate=0 vstep=-0.1 vfinal=-0.5 name=gate
solve vgate=-0.5 vstep=-0.5 vfinal=-4.0 name=gate
solve vgate=-2.0 vstep=0.1 vfinal=0.0 name=gate

solve vgate=0.0 vstep=0.1 vfinal=2.0 name=gate
solve vgate=2.0 vstep=0.05 vfinal=6.0 name=gate
#solve vgate=6.0 vstep=0.25 vfinal=15.0 name=gate



tonyplot -overlay sim0.log sim2.log sim4.log sim6.log


quit
```

3. Electric Field

```
go atlas

mesh

x.m l=0.0  spac=0.1
x.m l=1.5 spac=0.1
x.m l=1.99  spac=0.1
x.m l=2.02 spac=0.1

y.m l=0.0   spac=0.1
y.m l=0.15   spac=0.1
y.m l=0.2 spac=0.001
y.m l=0.34   spac=0.0001
```

```
y.m l=0.4   spac=0.0001
y.m l=0.5  spac=0.001
y.m l=0.55 spac=0.01
y.m l=2.0 spac=20.0
y.m l=100.0   spac=40.0
y.m l=100.4 spac=0.1
y.m l=100.9 spac=0.1

region num=1 silicon x.min=0.0 x.max=2.0  y.min=0.0 y.max=100.9
region num=2 oxide   x.min=2.0 x.max=2.02 y.min=0.0 y.max=100.9
#region num=3 x.min=2.0 x.max=2.02 y.min=0.0 y.max=0.4  user.material=empty
#region num=4 x.min=2.0 x.max=2.02 y.min=2.0 y.max=100.7  user.material=empty

electrode name=emitter1 x.min=0.0 x.max=2.0 y.max=0.0
electrode name=emitter2 x.max=0.0 y.min=0.0 y.max=0.6
electrode name=gate    x.min=2.02 y.min=0.2 y.max=2.0
electrode name=collector x.min=0.0 x.max=2.0 y.min=100.9

doping uniform n.type conc=2.0e20 x.left=0.0 x.right=2.0 y.min=0.0   y.max=0.2

#Channel Doping
#doping uniform p.type conc=5.0e18 x.left=0.0 x.right=2.0 y.min=0.2   y.max=0.5
doping uniform n.type conc=1.5e15 x.left=0.0 x.right=2.0 y.min=0.2   y.max=0.5
doping uniform p.type conc=5e19 x.left=0.0 x.right=2.0 y.min=0.346 y.max=0.354

doping uniform n.type conc=1.5e14 x.left=0.0 x.right=2.0 y.min=0.5   y.max=100.5
doping uniform p.type conc=1.0e20 x.left=0.0 x.right=2.0 y.min=100.5 y.max=100.9


contact name=gate aluminum

mater region=1 taup0=1e-6 taun0=1e-6

#interface charge=3.0e12 x.min=1.95 x.max=2.02 y.min=0.0 y.max=1.0


#material material=empty user.group=insulator user.default=oxide permittivity=1e-10

models   analytic srh auger conmob surfmob bgn
#impact   selb

output ey.field ex.field band.temp con.band val.band

output     e.field j.electron j.hole j.conduc j.total ex.field \
       ey.field jy.electron \
       impact


#solve init



method newton trap climit=1e-5 maxtraps=8

solve init
solve vgate=4.0
solve vcollector=10.0
solve vemitter1=0.0
solve vemitter2=0.0


solve vcollector=0.0 vemitter1=0.0 vemitter2=0.0 vgate=0.0

save outf=dev.str
tonyplot dev.str

quit
```

4. Breakdown Characteristics

```
go atlas

mesh

x.m l=0.0  spac=0.1
x.m l=1.95 spac=0.1
x.m l=1.99  spac=0.001
x.m l=2.02 spac=0.001

y.m l=0.0   spac=0.1
y.m l=0.15   spac=0.1
y.m l=0.19 spac=0.01
#y.m l=0.2994115 spac=0.005885
y.m l=0.339 spac=0.0005885
y.m l=0.34   spac=0.0001
y.m l=0.355   spac=0.1
y.m l=0.4   spac=0.1
y.m l=0.48  spac=0.1
#y.m l=0.4888124 spac=0.0011876
#y.m l=0.5   spac=0.011876
y.m l=0.55 spac=0.001
y.m l=2.0 spac=0.1
y.m l=5.0 spac=0.5
y.m l=10.0 spac=1.0
y.m l=30.78   spac=5.0
y.m l=90.0    spac=5.0
y.m l=95.0    spac=0.5
y.m l=100.0   spac=0.1
y.m l=100.499999999 spac=0.01
#y.m l=100.5 spac=0.012654
#y.m l=100.500012654 spac=0.000012654
y.m l=100.9 spac=0.1


region num=1 silicon x.min=0.0 x.max=2.0  y.min=0.0 y.max=100.9
region num=2 oxide   x.min=2.0 x.max=2.02 y.min=0.0 y.max=100.9
#region num=3 x.min=2.0 x.max=2.02 y.min=0.0 y.max=0.4  user.material=empty
#region num=4 x.min=2.0 x.max=2.02 y.min=2.0 y.max=100.7  user.material=empty

electrode name=emitter1 x.min=0.0 x.max=2.0 y.max=0.0
electrode name=emitter2 x.max=0.0 y.min=0.0 y.max=0.6
electrode name=gate    x.min=2.02 y.min=0.2 y.max=2.0
electrode name=collector x.min=0.0 x.max=2.0 y.min=100.9

doping uniform n.type conc=2.0e20 x.left=0.0 x.right=2.0 y.min=0.0   y.max=0.2

#Channel Doping
doping uniform p.type conc=5.0e18 x.left=0.0 x.right=2.0 y.min=0.2   y.max=0.5
#doping uniform n.type conc=1.5e15 x.left=0.0 x.right=2.0 y.min=0.2   y.max=0.5
#doping uniform p.type conc=5e19 x.left=0.0 x.right=2.0 y.min=0.346 y.max=0.354

doping uniform n.type conc=1.5e14 x.left=0.0 x.right=2.0 y.min=0.5   y.max=100.5
doping uniform p.type conc=1.0e20 x.left=0.0 x.right=2.0 y.min=100.5 y.max=100.9


contact name=gate aluminum

mater region=1 taup0=1e-6 taun0=1e-6

#interface charge=3.0e12 x.min=1.95 x.max=2.02 y.min=0.0 y.max=1.0
```

```
#material material=empty user.group=insulator user.default=oxide permittivity=1e-10

models   cvt srh
impact   selb

output ey.field ex.field band.temp con.band val.band

output     e.field j.electron j.hole j.conduc j.total ex.field \
       ey.field jy.electron \
       impact


#solve init



method newton trap climit=1e-5 maxtraps=8
method carriers = 2

solve init
solve vgate=0.0
solve vcollector=0.0
solve vemitter1=0.0
solve vemitter2=0.0


solve vcollector=0.0 vemitter1=0.0 vemitter2=0.0 vgate=0.0

log outf=sim1.log master
solve vgate=0.0
solve vcollector=0.0 vstep=10.0 vfinal=350.0 name=collector

#solve vcollector=350.0 vstep=0.1 vfinal=355 name=collector

tonyplot sim1.log

#solve  vstep=2.0 vfinal=50 name=collector
#solve  vstep=10.0 vfinal=500 name=collector compl=1.e-7 cname=collector \
#    outf=bk. log master

#tonyplot bk.log


quit
```

5. Reverse Breakdown Characteristics

```
go atlas

mesh

x.m l=0.0  spac=0.1
x.m l=1.95 spac=0.1
x.m l=1.99  spac=0.001
x.m l=2.02 spac=0.001

y.m l=0.0   spac=0.1
y.m l=0.15   spac=0.1
y.m l=0.19 spac=0.01
#y.m l=0.2994115 spac=0.005885
y.m l=0.340 spac=0.1
y.m l=0.345   spac=0.00005885
```

```
y.m l=0.360   spac=0.1
y.m l=0.4   spac=0.1
y.m l=0.48  spac=0.1
#y.m l=0.4888124 spac=0.0011876
#y.m l=0.5   spac=0.011876
y.m l=0.55 spac=0.001
y.m l=2.0 spac=0.1
y.m l=5.0 spac=0.5
y.m l=10.0 spac=1.0
y.m l=30.78   spac=5.0
y.m l=90.0    spac=5.0
y.m l=95.0    spac=0.5
y.m l=100.0   spac=0.1
y.m l=100.499999999 spac=0.01
#y.m l=100.5 spac=0.012654
#y.m l=100.500012654 spac=0.000012654
y.m l=100.9 spac=0.1

region num=1 silicon x.min=0.0 x.max=2.0  y.min=0.0 y.max=100.9
region num=2 oxide   x.min=2.0 x.max=2.02 y.min=0.0 y.max=100.9
#region num=3 x.min=2.0 x.max=2.02 y.min=0.0 y.max=0.4  user.material=empty
#region num=4 x.min=2.0 x.max=2.02 y.min=2.0 y.max=100.7  user.material=empty

electrode name=emitter1 x.min=0.0 x.max=2.0 y.max=0.0
electrode name=emitter2 x.max=0.0 y.min=0.0 y.max=0.6
electrode name=gate    x.min=2.02 y.min=0.2 y.max=8.0
electrode name=collector x.min=0.0 x.max=2.0 y.min=100.9

doping uniform n.type conc=2.0e20 x.left=0.0 x.right=2.0 y.min=0.0   y.max=0.2
doping uniform n.type conc=1.5e14 x.left=0.0 x.right=2.0 y.min=0.2   y.max=0.5
doping uniform n.type conc=1.5e14 x.left=0.0 x.right=2.0 y.min=0.5   y.max=100.5
doping uniform p.type conc=1.0e20 x.left=0.0 x.right=2.0 y.min=100.5 y.max=100.9

doping uniform p.type conc=4.2e20 x.left=0.0 x.right=2.0 y.min=0.345 y.max=0.355

#doping reg=1 gauss   p.type conc=2e20 peak=0.4  char=0.005
#doping reg=1 gauss   n.type conc=5e18 peak=0.7  char=0.005
#doping reg=1 gauss   n.type conc=1e20 peak=530.7  char=0.005

contact name=gate aluminum

mater region=1 taup0=1e-6 taun0=1e-6

interface charge=3.0e12 x.min=1.95 x.max=2.02 y.min=0.3 y.max=8.2

#material material=empty user.group=insulator user.default=oxide permittivity=1e-10

models   analytic srh auger conmob surfmob bgn
impact   selb

output ey.field ex.field band.temp con.band val.band

#output     e.field j.electron j.hole j.conduc j.total ex.field \
       ey.field jy.electron \
       impact

#solve init

#save outf=dev.str
#tonyplot dev.str

method newton trap climit=1e-5 maxtraps=8
method carriers=2

solve init
#solve vcollector=0.0
#solve vemitter1=0.0
```

```
#solve vemitter2=0.0
#solve vgate=0.0

log outf=o1.log master

solve vcollector=0.025
solve vcollector=0.05
solve vcollector=0.1
solve vcollector=0.4

solve vstep=0.2 vfinal=10 name=collector compl=5e2 cname=collector
solve vstep=5.0 vfinal=100 name=collector compl=5e2 cname=collector

# Extract the design parameter, Vbd
extract name="NVbd" x.val from curve(abs(v."collector"),abs(i."collector")) where y.val=1e-9

tonyplot o1.log

quit
```

Appendix B: IWPSD 2015 Abstract and Poster

Performance Improvement of IGBT with Locally Doped Channel

P. Kalaga[1*], V. S. Senthil Srinivasan[2], R. Koerner[2], J. Schulze[2], S. Karmalkar[1]

[1]*Department of Electrical Engineering, Indian Institute of Technology Madras, Chennai, India*
[2]*Institute of Semiconductor Engineering, University of Stuttgart, Stuttgart, Germany*

*pranav.kalaga@gmail.com

ABSTRACT

The Insulated Gate Bipolar Transistor (IGBT) combines the strengths of both the power MOSFET and power BJT. It has widespread applications in low-to-medium power, and frequency requirements. Performance of the IGBTs were efficiently improved over time by novel technologies like punch through IGBT, field stop IGBT etc. In this work, we study a simplified diffusion-less MBE grown vertical IGBT device shown in Fig. 1, where the channel is vertical as in a trench gate IGBT and the characteristics resemble those of a conventional IGBT. Specifically, we explore the advantages of replacing the homogeneously doped channel (HDC) (as in Fig. 1(a)) with a locally doped channel (LDC), i.e. an intrinsic channel with a delta doped layer (as in Fig. 1(b)).

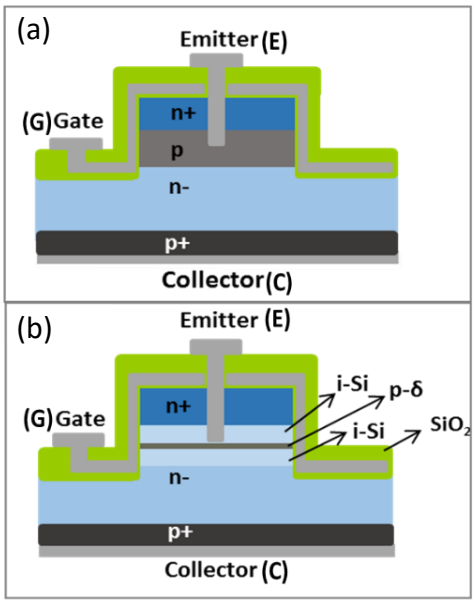


Fig. 1 IGBT structure with vertical current flow. (a) Homogenously Doped Channel; (b) Locally Doped Channel.

The structures shown in Fig. 1 can be fabricated in the following steps. Highly doped n^+ Si emitter and channel, which is p-type in (a) and an i-p-i stack in (b), are grown by molecular beam epitaxy on the front side of n^- Si wafer. Highly doped p^+ Si collector is similarly grown on the back side of the n^- wafer. Mesa is RIE etched after patterning. 20 nm thick low temperature PECVD SiO_2 is deposited as a gate oxide and aluminium is sputtered to form a gate metal and patterned. Final contact is made by aluminium sputtering and patterning, after passivation oxide deposition and via hole etch.

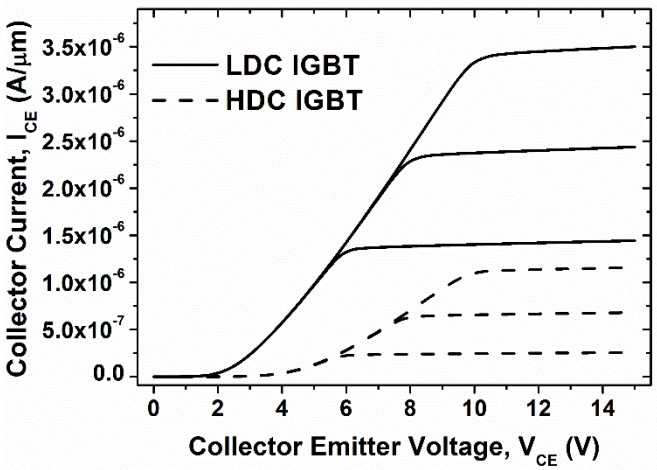


Fig. 2: Simulated output characteristics of Homogeneously Doped Channel IGBT (HDC IGBT) and Locally Doped channel IGBT (LDC IGBT)

The HDC and LDC structures were simulated using Silvaco ATLAS. Fig. 2 shows the

collector current versus collector voltage. It is seen that the current for a given voltage in LDC IGBT is higher by a factor of ~ 3-4, while the voltage drop for a given current is reduced by more than a factor of two. As a consequence of these, we anticipate a significant improvement in the device performance. The increase in current can be attributed to the lowering of channel doping which consequently increases the channel mobility, and to the increase in the carrier velocity saturated portion of the channel.

HDC structure has been fabricated and fabrication of the LDC structure is underway, motivated by the improvements demonstrated in simulations.The full paper will explain the advantages of the LDC device over the HDC device with the help of the simulated electric field distributions, and provide details of the measured characteristics on fabricated devices.

Performance Improvement of IGBT with Locally Doped Channel

P. Kalaga[1]*, V. S. Senthil Srinivasan[2], R. Koerner[2], J. Schulze[2], S. Karmalkar[1]

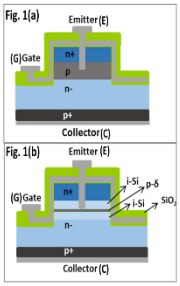
1 Department of Electrical Engineering, Indian Institute of Technology – Madras, Chennai, India

2 Institute of Semiconductor Engineering, University of Stuttgart, Stuttgart, Germany

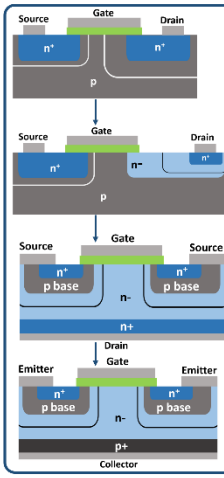
*pranav.kalaga@gmail.com

1. Abstract

- Insulated Gate Bipolar Transistor (IGBT) combines the strengths of power MOSFET and power BJT.
- We study a diffusionless MBE grown IGBT where the current flow is vertical (see Fig. 1)
- Fig. 1(a): a Homogenously Doped Channel (HDC) IGBT whose structure resembles a trench gate IGBT and characteristics resemble a conventional lateral IGBT.
- Fig. 1(b): a Locally Doped Channel (LDC) IGBT, which has a delta-doped layer in an intrinsic channel.
- C. Fink. et al, studied advantages of local channel doping in power MOSFET
- We study the advantages of LDC IGBT over HDC IGBT.

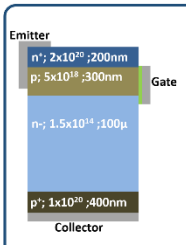


2. Concept



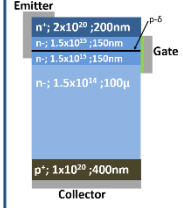
1. Conventional MOSFET
   - off-state depletion region extends into channel
   - channel length is small, hence breakdown voltage is low
2. Drain extended MOSFET
   - off-state depletion region extends into low doped drain
   - the drain can be long, and hence breakdown can be high
3. Power MOSFET
   - n-type lightly doped substrate absorbs the off-state depletion region
   - thick substrate and reduced field crowding at the gate lead to even higher breakdown
   - reduced lateral footprint leads to higher device density
4. Lateral IGBT Device
   - n+ part of the power MOSFET drain replaced by a p+ region called the collector
   - in the ON-state, the p+ region injects holes into the n- region reducing the voltage drop
   - Off-state picture same as in power MOSFET

3. Device Description



Homogenously Doped Channel (HDC) IGBT schematic

- Emitter, channel and collector regions grown on an intrinsic substrate by MBE
- PECVD grown 20 nm thick oxide
- Similar to a trench gate IGBT
- Emitter contact shorts emitter and body (channel) eliminating body effects



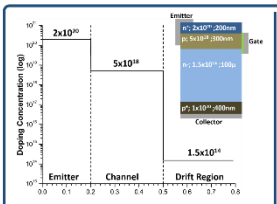
Locally Doped Channel (LDC) IGBT schematic

- same as above except for a delta doped boron region in the channel that has a surface doping of 2.1 x 10^{14} cm^{-2} and thickness of 8nm

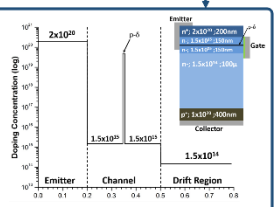
4. Simulation and Results

- Simulations based on Silvaco ATLAS 2D
- Models assumed
  - no fixed charges at semiconductor-oxide interface
  - SRH Recombination
  - Drift-diffusion transport
  - Bandgap narrowing
  - Concentration dependent mobility

Doping Profile

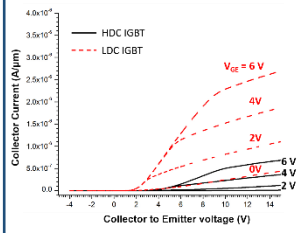


HDC IGBT Doping profile along the vertical direction



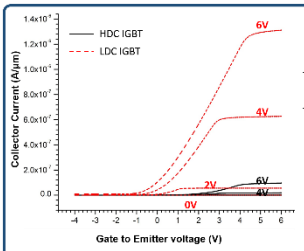
LDC IGBT Doping profile along the vertical direction

$I_C - V_{CE}$ Characteristics



- V_{GE} is the gate to emitter voltage
- as compared to HDC IGBT, the LDC IGBT demonstrates
  4-5 times higher current for a given voltage bias
- reduced voltage drop for a given current

Transfer Characteristics



- V_{CE} is the collector to emitter voltage
- As compared to HDC IGBT, the LDC IGBT demonstrates
  a lower threshold voltage
  a significantly higher current for a given voltage

5. Conclusions and Further Work

- An LDC IGBT provides lower threshold voltage and higher current over the HDC IGBT, because the electric field can be tailored by optimizing the delta-doped p-layer.
- We have fabricated the HDC IGBT. Fabrication of LDC IGBT is currently underway.
- Our present study motivates the investigation of a superjunction IGBT structure and exploration of its advantages over an LDC IGBT.

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[1] V.K. Khanna, Insulated Gate Bipolar Transistor Theory and Design, IEEE Press and John Wiley, 2003.

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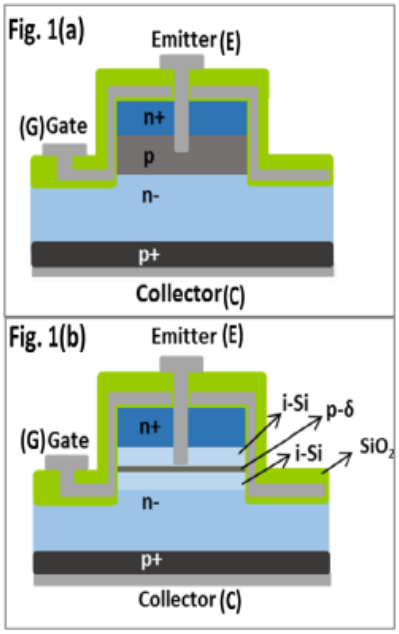

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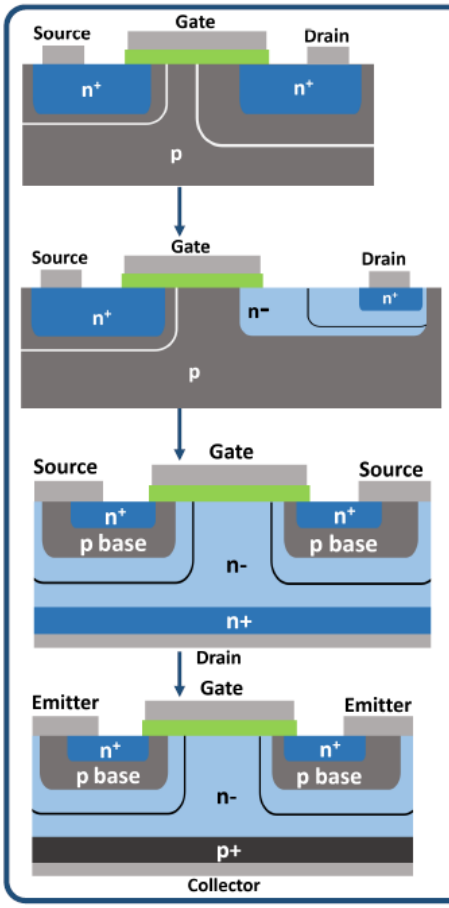

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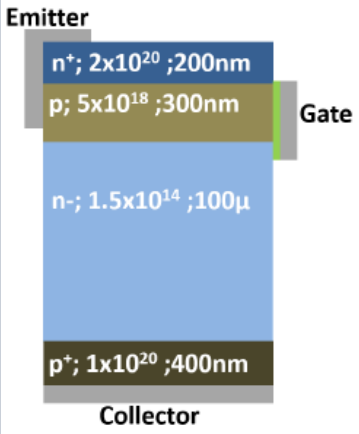

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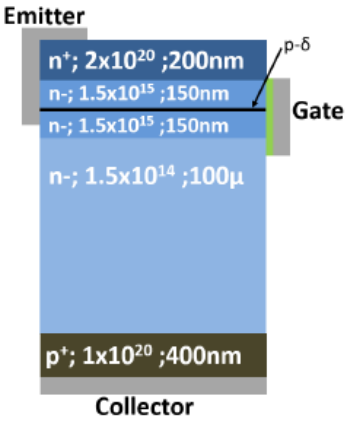

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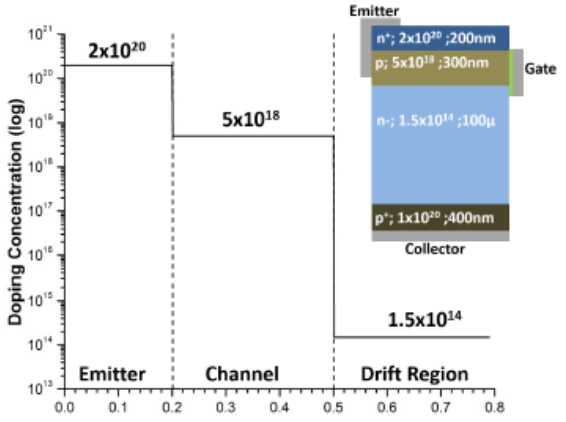
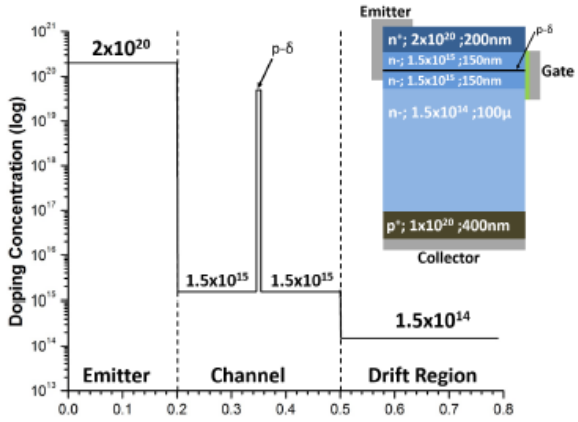


HDC IGBT Doping profile along the vertical direction



LDC IGBT Doping profile along the vertical direction

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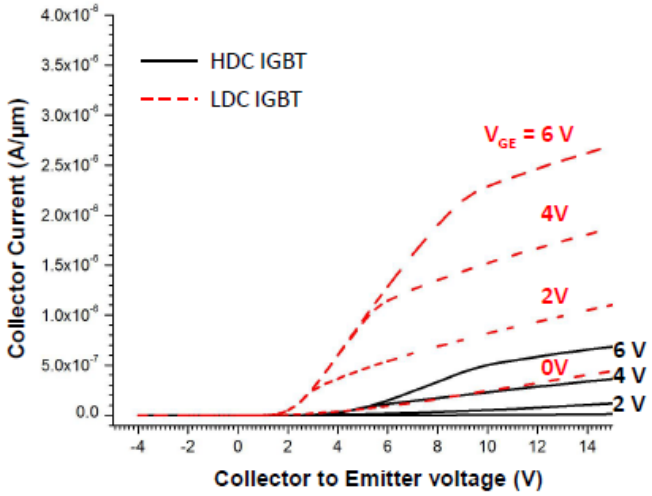

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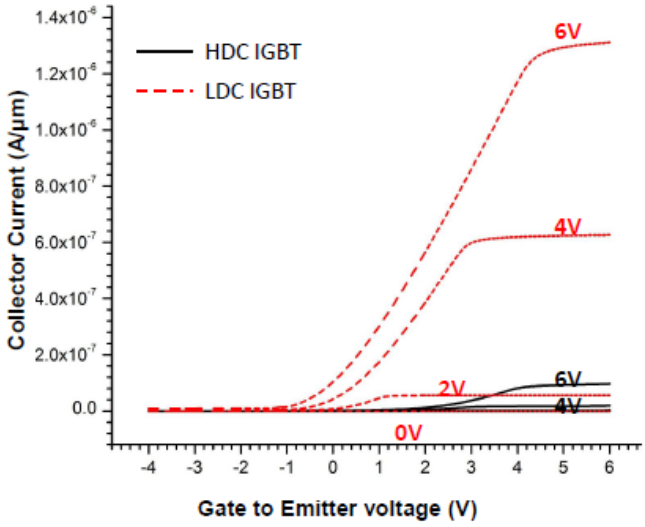

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List of Publications

P. Kalaga, V. Senthil Srinivasan, R. Koerner, J. Schulze and S. Karmalkar, "Performance Improvement of IGBT with Locally Doped Channel," in *International Workshop on Physics of Semiconductor Devices, Bangalore* , 2015.