COMPACT MODELING OF SOI-LDMOS TRANSISTORS

A Project Report

submitted by

NITIN PRASAD

in partial fulfilment of the requirements

for the award of the degree of

BACHELOR OF TECHNOLOGY

DEPARTMENT OF ELECTRICAL ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY MADRAS.

JUNE 2014

THESIS CERTIFICATE

This is to certify that the thesis titled **Compact Modeling of SOI-LDMOS Transistors**, submitted by **Nitin Prasad**, to the Indian Institute of Technology, Madras, for the award of the degree of **Bachelor of Technology**, is a bona fide record of the research work done by him under our supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

Prof. Anjan Chakravorty
Research Guide
Associate Professor
Dept. of Electrical Engg.
IIT-Madras, 600 036

Prof. Nandita Dasgupta
Research Guide
Professor
Dept. of Electrical Engg.
IIT-Madras, 600 036

Prof. Amitava Dasgupta
Research Guide
Professor
Dept. of Electrical Engg.
IIT-Madras, 600 036

Place: Chennai

Date: June 6, 2014

Contents

List of Figures

Abbreviations

MOSFET	Metal Oxide Semiconductor Field Effect Transistor
SOI	Silicon On Insulator
BOX	Buried Oxide
LDMOS	Lateral Double Diffused MOS
VDMOS	Vertical Double Diffused MOS
HVIC	High Voltage Integrated Circuit
RFIC	Radio Frequency Integrated Circuit
JFET	Junction Field Effect Transistor
NMOS	N-channel MOSFET
PMOS	P-channel MOSFET
DC	Direct Current
AC	Alternating Current
WD	Ward-Dutton
MWD	Modified Ward-Dutton

Symbols

V_{GS}	Gate to source voltage
V_{GB}	Gate to bulk voltage
V_{GC}	Gate to quasi-Fermi level voltage
V_{DS}	Drain to source voltage
V_{DiS}	Voltage drop across channel (region-I)
$V_{D'D_i}$	Voltage drop across drift region under gate oxide (region-II)
$V_{DD'}$	Voltage drop across drift region under field oxide (region-III)
V_{GD_i}	Gate to D_i voltage
$V_{GD'}$	Gate to D' voltage
$V_{sat,ch}$	Channel saturation voltage
$V_{sat,dr}$	region-II saturation voltage
$V_{DiS,eff}$	Effective voltage drop in region-I
$V_{D'D_i,eff}$	Effective voltage drop in region-II
I_{DS}	Drain to source current
I_{ch}	Channel region current
I_{dr}	Current in region-II
I_{dr1}	Current in region-III
L_{ch}	Length of region-I
L_{dr}	Length of region-II
L_{LC}	Length of region-III
W	Width of LDMOS
C_{ox}	Oxide capacitance
t_{ox}	Oxide thickness
A	Cross section area of LDMOS
t_{si}	Silicon film thickness
t_{BOX}	Thickness of buried oxide

N_{ch}	Doping concentration in region-I
N_{dr}	Doping concentration in region-II
N_{dr1}	Doping concentration in region-III
V_T	Thermal voltage
ϵ_{si}	Permittivity of silicon
ϵ_{ox}	Permittivity of silicon dioxide
ψ_s^{ch}	Surface potential in region-I
ψ_s^{dr}	Surface potential in region-II
Q_{inv}^{ch}	Inversion charge per unit area in region-I
Q_{acc}^{ch}	Accumulation charge per unit area in region-I
Q_{dep}^{ch}	Depletion charge per unit area in region-I
Q_{gate}^{ch}	Total gate charge in region-I
Q_{acc}^{dr}	Accumulation charge per unit area in region-II
Q_{dep}^{dr}	Depletion charge per unit area in region-II
Q_{inv}^{dr}	Inversion charge per unit area in region-II
Q_{gate}^{dr}	Total gate charge in region-II
Q_G	Charge assigned to gate terminal
Q_D	Charge assigned to drain terminal
Q_S	Charge assigned to source terminal
Q_B	Charge assigned to bulk terminal
Q_{D_i}	Charge assigned to D_i terminal
$Q_{D'}$	Charge assigned to $D^{'}$ terminal
V_{FB}^{ch}	Flat band voltage in channel
V_{FB}^{dr}	Flat band voltage in region-II
v_{sat}^{ch}	Saturation velocity of electrons in region-I
v_{sat}^{dr}	Saturation velocity of electrons in region-II
v_{sat}	Saturation velocity of electrons in region-III
μ_{ch}	Effective mobility in channel
μ_{dr}	Effective mobility in region-II
μ_{dr1}	Zero field mobility in region-III
$\theta_{3,ch}$	Velocity saturation parameter in channel
θ_1	Channel mobility reduction parameter
θ_2	Channel mobility reduction parameter
$\theta_{3,dr}$	Velocity saturation parameter in region-II

θ_{dr1}	Velocity saturation parameter in region-III
$\theta_{1,dr1}$	Velocity saturation parameter in region-III
λ_{ch}	Channel length modulation parameter
λ_{dr1}	Drift length modulation parameter
C_{ij}	Capacitance between terminals i and j

Chapter 1

Introduction

1.1 Overview of power semiconductor devices

Power semiconductor devices have become integral components of the semiconductor industry in designing high voltage integrated circuits (HVICs). They have come a long way since the inception of bipolar junction transistors and thyristors. Although the first commercial HV devices were introduced by Texas Instruments in 1954, it took almost a decade for them to find practical applications in high voltage circuits. Thyristors were the first class of power devices but they had the disadvantage of poor switching speed and difficulty of integration.

Further advancement in silicon fabrication technology let to the development of novel device structures such as power MOSFETs. These devices were introduced in late seventies [3] and they made way for the development of new generation of devices. By breaking the symmetry of a conventional MOSFET, the power MOSFETs were developed. The symmetry was broken to improve the the reverse blocking capability of the device[4]. One such power MOSFET that was developed was the lateral double diffused metal oxide semiconductor (LDMOS) transistors.

One of the main advantages of LDMOS devices is that they can be easily integrated with low voltage circuitry. They continue to be industry standard even today for medium voltage power applications. Their main drawback is the fact that they suffer from low current rating and breakdown voltage on-resistance trade off. To increase the voltage handling capabilities of this device, we need to increase the

length of lightly doped drain region across which the reverse voltage is dropped. This increases the area requirements of the device.

To circumvent this problem, vertical double diffused MOS (VDMOS) technology was developed. VDMOS provides larger current ratings and higher breakdown voltage compared to LDMOS[5], but requires complicated process steps and integration with low voltage circuitry is not easy. Though VDMOS finds applications in high voltage industries, medium power applications are still dominated by LDMOS devices.

Nowadays, HVICs and power integrated circuits (PICs) are replacing discrete elements such as DC-DC converter, switch mode power supplies and power amplifiers [6],[7],[8]. Integration of high and low voltage circuits on the same chip improves the overall performance and reduces the chip size. PICs are used as a bridge between power load and low voltage digital logic[9],[10]. They are also useful in Power line communications (PLCs) where digital information is transmitted over a power line. LDMOS devices form an integral part of many of these interesting applications.

1.2 Current scenario in LDMOS transistor modeling

With the advent of LDMOS devices in interesting consumer and automotive applications, it becomes essential to develop an accurate model for LDMOS transistors. Recently, fabrication of LDMOS devices on a Silion-on-Insulator (SOI) substrate has become popular. LDMOS fabricated on an SOI substrate offers additional advantages such as lower leakage currents, higher latchup, higher packing density and reduced parasitics[11]. Further, the use of an SOI substrate enables isolation between power devices and low voltage circuitry which is essential in smart power ICs. Thus compact models for SOI-LDMOS transistors capable of modeling device characteristics over wide range of bias and temperature and for various lengths is essential for a fail safe design of power integrated circuits.

There have been many approaches for modeling LDMOS transistors. Two main approaches followed are (i) macro-modeling and (ii) compact modeling. Macro

modeling procedure consists of trying to describe the behavior of device through a circuit consisting of several discrete elements or modules. As the number of effects rises, the number of elements in the circuit increases and results in increase in computation time and convergence problems. There are many existing macro models based on SPICE which consider SPICE models for MOSFETs, JFETS and diodes to model LDMOS[12],[13],[14]. One such macro model uses BSIM4 to model the MOSFET and JFET to model drift region and a shorted PMOS transistors to model capacitance behavior of drift region[15]. These models have a large number of non-physical model parameters.

Compact modeling, on the other hand, maintains device unity through a set of self consistent expressions which are able to produce device behavior. All internal node equations are solved in the model itself, thereby reducing computation time. Also, the expressions obtained are from physical principles and do away with non-physical parameters introduced in macro-modeling. There are several compact models available for SOI-LDMOS, important among them being HiSIM-HV [16][17], EKV model[18],[19],[20] and MM20 HVMOS model[21]. In this thesis, MM20 model developed by NXP semiconductors is used as a basis upon which further formulations have been built. MM20 HVMOS model is a surface potential based model. It models the channel and drift region under the gate oxide of the LDMOS transistor. It does not model the region under field oxide and hence cannot be used for high voltage devices.

The effect of quasi-saturation in drift region under field oxide was considered in [22]. Further, high voltage effects such as impact-ionization, snapback and self-heating in an SOI-LDMOS was successfully modeled by [23]. However, the bias voltage dependence of the quasi-saturation current was not studied in detail in these works. This thesis deals with modeling this effect, along with displaying the scalability of the model with respect to the length of the drift region under the field oxide.

Apart from accurately predicting the DC characteristics of a device, a good model must also accurately predict various capacitances which are important for the AC characteristics of the device. With the integration of LDMOS in high speed circuits such as RFICs, predicting the high speed performance of LDMOS becomes

important. In literature, there have been few detailed studies on modeling capacitances in devices such as LDMOS and SOI-LDMOS and some of them have resulted in model development[1],[24],[25],[26]. One of the basic principles used for modeling capacitances is charge partitioning. The charges are modeled accurately and then they are partitioned between different terminals of the device based on Ward-Dutton partition principle[27]. MM20 model uses a modified version of Ward-Dutton model to obtain various capacitances. It does not clearly explain the basis behind such a partition and charge modeling also has some inherent approximations. Also, the match obtained between the device and model simulations are not satisfactory.

Therefore, there is a need for a comprehensive charge model which accounts for aforementioned effects. An attempt was made to modify the MM20 charge partitioning scheme by [31]. But, several inaccuracies in the charge model was reported. In this thesis, an extensive model to describe the static and dynamic characteristics of SOI-LDMOS is proposed. MM20 model and the model proposed by [31] serves as a starting point for describing various currents and charges in the device, but the model description goes a long way from these approaches. The model considers field dependent mobility reduction, velocity saturation in channel and quasi-saturation in the drift region. A new charge partitioning scheme is proposed and physical reasoning behind such a partition is explained.

1.3 Objectives

The main objectives of this thesis are as follows.

- To analyze the behavior of SOI-LDMOS in channel, drift region under gate oxide and drift region under field oxide for various gate and drain bias voltages.
- To develop a scalable quasi-saturation model for the drift region under the field oxide which accounts for the bias dependence of the quasi-saturation current.
- To analyze the charges present in the device and provide a physics based charge-partition model to partition charges between various terminals.

- To predict various capacitances from the developed charge model.

1.4 Structure of the thesis

The thesis is organized as follows.

- **Chapter 2: Analysis of physical effects**

  A physical description of the working of LDMOS device is provided in this section. This is done by analyzing the internal node voltages to arrive at a typical output characteristic of an SOI-LDMOS. Further, various charges present in the operation of the SOI-LDMOS are pointed out along with a crude charge assignment scheme. The device behavior is analyzed with the help of a physics-based device simulator - MEDICI.

- **Chapter 3: Model and Verilog-A implementation**

  In this chapter, first, a compact DC model to explain the observed physical effects is proposed. The model uses MM20 model for channel and drift region under gate oxide and a new quasi-saturation model is developed to capture the bias dependence of the quasi-saturation current and to account for scalability of region-III length. Later, a comprehensive charge model is proposed, based on a modified Ward-Dutton charge partitioning scheme.

- **Chapter 4: Results and discussions**

  Static output characteristics, various capacitance plots and transient plots are compared with MEDICI simulation results.

- **Chapter 5: Conclusions**

  Contributions offered by with work are presented. Scope for future work is listed.

Chapter 2

Analysis of Physical Effects

In this chapter, we focus on the physical effects which gives rise to unique AC and DC output characteristics of an SOI-LDMOS transistor. Firstly, the effect of gate and drain voltage on static currents is analyzed. A particular focus is laid on the effects caused my the presence of the drift region of the transistor. Next, we study various charges that arises in an SOI-LDMOS transistor with application of a gate and a drain bias. A 2-D device simulator Taurus MEDICI [28] is used for studying these effects.

2.1 Device Structure

SOI-LDMOS transistor is an asymetric device which is constructed by adding an additional resistive drift region to a conventional MOSFET structure. The schematic cross-section of the device is as shown in Fig. 2.1. The channel region is self aligned to the gate and is formed by p-diffusion through the source opening. This creates a p-well structure under the gate, although it has a non-uniform doping profile; the source end of the channel has a higher doping concentration under he gate. Once the p-well for the channel is created, the source contact is formed by an $n+$ diffusion through the same opening. Since there are two lateral diffusions processes, this device is called as the lateral double-diffused MOSFET. The n-drift region sustains the reverse voltage applied at the drain end, and hence is lightly doped in comparison to the channel. Thus, the depletion region at

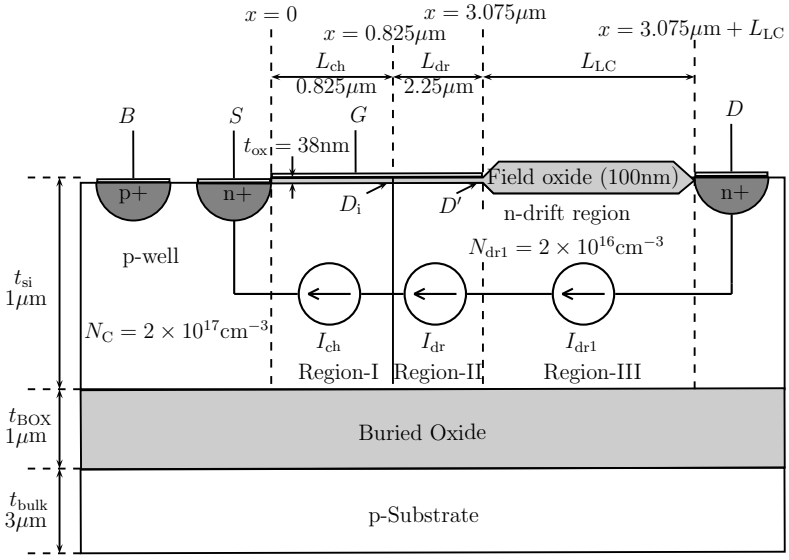


FIGURE 2.1: Schematic cross-section of the investigated SOI-LDMOS transistor.

the junction of the channel and the drift region extends mostly into the drift region. The gate electrode covers the surface of the drift region and a part of the drift region. The gate oxide and the field oxide are of different thicknesses. A thicker field oxide helps in reducing the gate drain overlap capacitance, and hence improving the speed of the device. The active part of the device is isolated from the bulk by a thick buried oxide which reduces parasitics.

As seen in Fig 2.1, the LDMOS transistor is divided into three important regions (denoted by region, region-II and region-III, corresponding to channel region in the p-well, drift region under the gate oxide and the drift region under the field oxide, respectively). The transition between region-I and region-Ii ids denoted by D_i and that between region -II and region-III is denoted by D'. While modeling the LDMOS structure, we analyze these three regions separately to obtain current and charge expressions for each of these regions.

The non-uniformity of the the doping concentration from the source to the drain side poses complexities in modeling the current and the associated charges. Hence, as a simplifying assumption, the channel doping is maintained constant in further formalisms and simulations. For the device under discussion, the p-well (region-I) has a uniform doping concentration of $2 \times 10^{17}\text{cm}^{-3}$, the drift region (region-II and region-III) has a doping concentration of $2 \times 10^{16}\text{cm}^{-3}$ (ten times lower than

channel doping). A contact doping of $1 \times 10^{20}\text{cm}^{-3}$ is used for $(n+)$ source and $(n+)$ drain contacts (the same doping is assumed for the gate polysilicon) and $5 \times 10^{21}\text{cm}^{-3}$ is used for the $(p+)$ bulk contact. The length of the channel region (region-I) $L_{ch} = 0.825\mu$m and the length of the drift region under the gate oxide (region-II) $L_{dr} = 2.25\mu$m. The default length for the drift region under the field oxide (region-III) is $L_{dr1} = 3.45\mu$m, unless explicitly stated. The gate oxide and field oxide thickness are 38nm and 100nm respectively. The thickness of the active region is 1μm and the thickness of the buried oxide used is 1μm.

2.2 Static Currents

To make the analysis of the LDMOS transistor simple, we separate the device into three distinct regions: region-I, II and III. Although this is not a physical separation, this helps to analyze the effects and model the device using a simple approach. All throughout the charge and current analysis, it is assumed that the source and bulk terminals are shorted. As a result, in this thesis, we use the notations V_{GB} and V_{GS}, V_{DB} and V_{DS} interchangeably[1]. Current modeling has been dealt with in great detail in [29] and [30]. As far as the DC static current model is concerned, this thesis tries to explain the current modeling carried out by [29, 30] in a concise form, with more focus laid on analyzing the scaling the length of region-III.

As V_{GS} is increased beyond the threshold voltage[2] of the channel, the region-I gets inverted, allowing conduction between the source and the drain, just as in the case of a MOSFET. However, since there is a gate overlap in the drift region (region-II), accumulation layer of electrons is formed (if sufficiently high gate voltage is applied). Hence conduction in region-II comprises of two components: conduction due to accumulation layer charge and the bulk conduction. Further, region-III can enter velocity saturation for sufficiently high drain and gate voltages. These effects manifest in the output characteristics as shown in Fig. 2.2.

[1] It is possible to easily extend the analysis for a case in which $V_{SB} \neq 0$

[2] The threshold voltage of the channel is assumed to be a constant throughout the channel. However, if we take into account the non-uniformity in the p-well doping caused because of fabrication related issues, the threshold voltage varies across the channel.

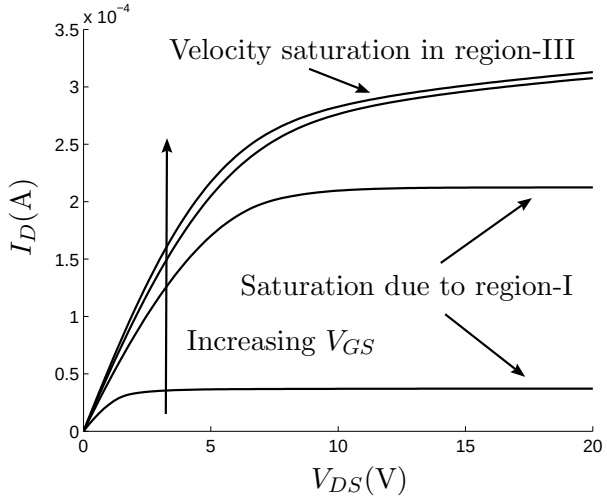


FIGURE 2.2: $I_D - V_{DS}$ characteristics for $V_{GS} = 5, 10, 15$ and 20V, simulated in MEDICI

2.2.1 Analysis of potential drops across the three regions

For easier understanding of the behavior of the LDMOS transistor under different bias voltages, we need to understand the variation of intermediate voltages at D_i and D' as a function of terminal voltages. A detailed account of this analysis can be found in [30]. Only a brief summary is dealt with in this thesis.

For a low value of V_{GS}, the conductivity of region-I and II is lesser than or comparable to that of that of the drift region. Hence, a significant portion of the applied drain voltage gets dropped across region-I and II. Hence, as V_{DS} is increased, at low V_{DS}, the current saturation is caused because region-I and II enter velocity saturation or pinch-off.

For a high value of V_{GS}, the conductivity of region-I and region-II are much greater than that of region-III. Hence, most of the applied voltage is dropped across region-III. For a sufficiently high value of V_{DS}, the region-III enters velocity saturation and causes a current saturation. This kind of current saturation caused because region-III enters velocity saturation is referred to as the *quasi-saturation*. Due to quasi-saturation at high V_{GS}, the drain current almost becomes independent of the gate voltage[3].

[3]There is a small dependence of the quasi-saturation current on the gate voltage (as we shall see later), but this is a second-order effect.

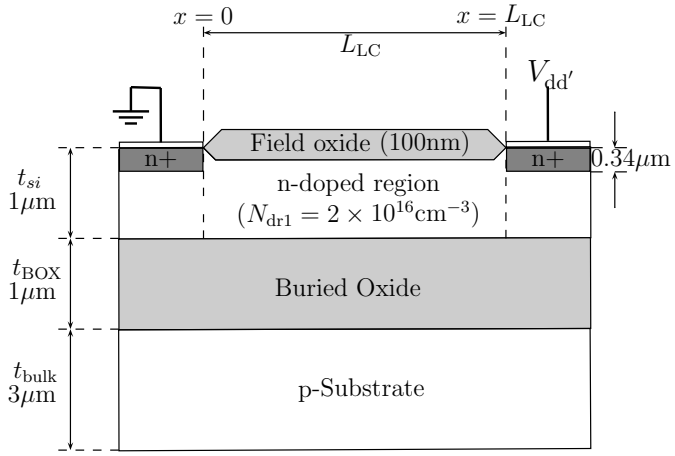


FIGURE 2.3: Schematic cross-section of the 2-D resistor structure simulated to model the velocity saturation characteristics.

2.2.2 Gate and drain voltage dependence of the quasi-saturation current.

For a sufficiently high value of V_{GS}, since both region-I and II have high conductivity, almost all the applied voltage is dropped across region-III. Hence, region-III is expected to enter velocity saturation as V_{DS} is increased. The velocity saturation current of a resistor is not expected to depend on the applied voltage across it. Further, since the gate voltage does not affect the performance of region-III, we do not expect V_{GS} dependence of the drain current.

Contrary to our expectations, the quasi-saturation current shows both drain and gate voltage dependence as shown in Fig. 2.2.

2.2.2.1 Drain voltage dependence

To understand the drain voltage dependence of the quasi-saturation current, let us first analyze a simple two-dimensional SOI-resistor shown in Fig. 2.3. Even in a case of a simple two-dimensional SOI-resistor, the velocity saturated drain current is not independent of the applied voltage; there is a mild increase in the velocity saturated current with increase in the applied voltage. Further, this rate of this increase in drain current increases with decrease in the length of the 2-D resistor.

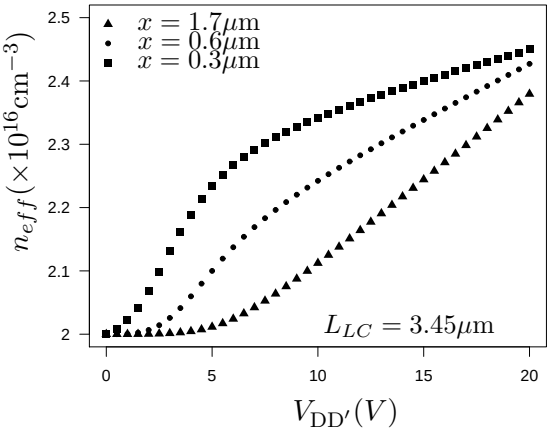
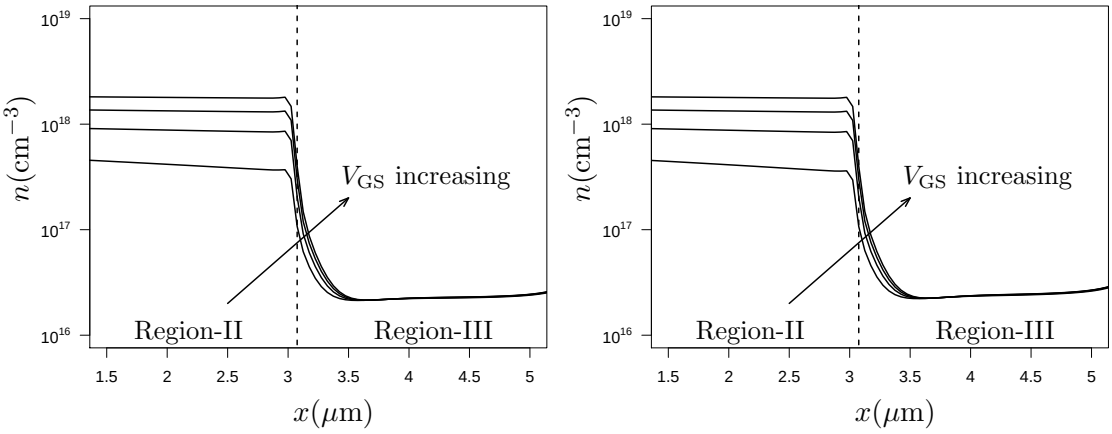


FIGURE 2.4: Variation of charge carrier concentration as a function of voltage across the resistor. The n_{eff} data from MEDICI is probed at $t_{si}/2$ below the top oxide-silicon interface.

This increase was said to be due to channel length modulation by [29]. But, as pointed out in [17], this parameter should be attributed to the increase in charge carrier concentration once velocity saturation condition is reached and not to the channel length modulation. This increase is caused by the presence of highly doped contacts and the 2-D geometry of the resistor. Fig. 2.4 shows that the electron concentration (n_{eff}) at different locations of the resistor starts to increase after different $V_{DD'}$ values. Threshold $V_{DD'}$ values are much lower near the metal contacts.

2.2.2.2 Gate voltage dependence

A plot of the net electron density along the top oxide-semiconductor surface of the device in 2.1. Fig.2.5 shows the simulated electron density for different values of V_{GS} and at high $V_{DS}(= 20V)$. We observe that there is some amount of spill over of the electron concentration into region-III from region-II, which has very high electron concentration due to accumulation condition at the surface. As the gate to D' voltage ($V_{GD'}$) is increased, the accumulation charge at D' increases and consequently the spill over of the electron concentration increases leading to a reduction in the effective length of region-III. This reduction of the effective length with increase in V_{GS} causes the increase in drain current with increase in $V_{GD'}$.



(A) $V_{DS} = 15V$ (B) $V_{DS} = 20V$

FIGURE 2.5: Net electron density (obtained from MEDICI) as a function of x along the top oxide-semiconductor surface of the device for $V_{GS} = 5, 10, 15, 20V$. The vertical dashed line represents the D' node shown in Fig. 2.1

2.3 Regional Charge assignments

In this thesis, we are trying to carry out the AC model using a charge based approach for all bias voltages (negative and positive). Hence, a proper understanding of various charges present in the device is needed. Also, the identified charges need to be assigned to various terminals so that the associated capacitance of each terminal can be derived from the charges by using:

$$C_{ij} = (2\delta_{ij} - 1)\frac{\partial Q_i}{\partial V_j} \tag{2.1}$$

where $i, j \in D, G, S, B$ and δ_{ij} is the Kronecker delta function.

Fig. 2.6 shows various charges associated with the LDMOS structure for different representative bias points. To systematically analyze the various charges that one needs to account for while modeling these charges, let us look at various charges present in the device region wise.

2.3.1 Region-I surface charges

The region-I analysis of charges is similar to that of a regular MOSFET. When $V_{GS} < V_{FB,ch}$, where $V_{FB,ch}$ is the flat band voltage of region-I, the surface of region-I enters accumulation mode of operation. A accumulation layer of holes

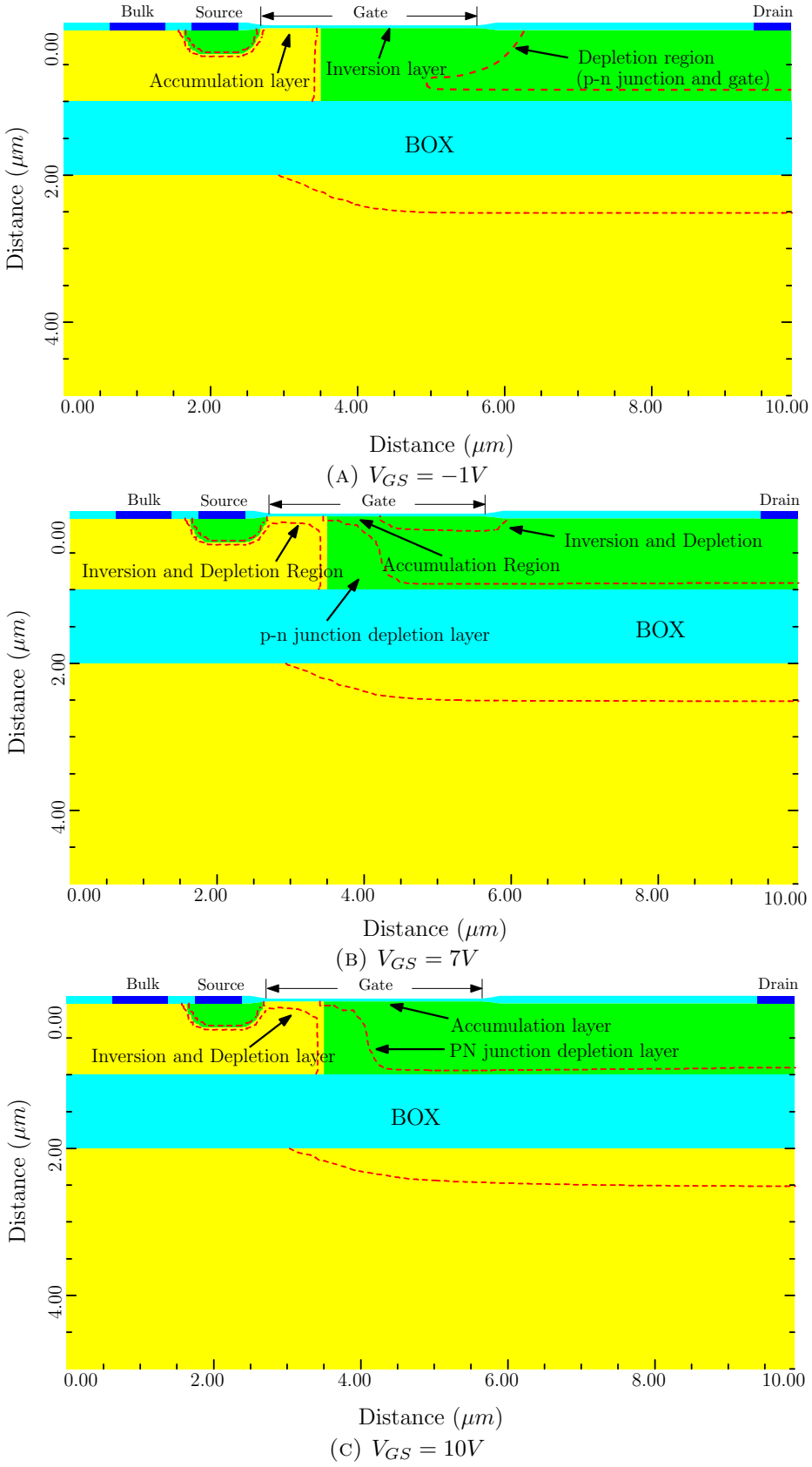


FIGURE 2.6: Cross-section of the SOI-LDMOS transistor indicating the depletion region and other associated charges at various bias points

is formed along the surface of region-I. These accumulation charges (holes) are assigned to the bulk of the device (p doped) where the majority carriers are holes.

For $V_{GS} > V_{FB,ch}$, depletion and inversion layer charges are formed along the surface. The depletion layer charges is again associated with the bulk of the device. The inversion layer charge (formed by electrons) on the other hand is associated with S and D_i nodes (n doped). One needs to model the split of charges between the source and the drain terminal. This model is referred to as a 'charge partitioning scheme' in the literature.

2.3.2 Region-II surface charges

When the LDMOS transistor is biased such that $V_{GDi} > V_{FB,dr}$, where $V_{FB,dr}$ is the flat band voltage of region-II, the surface of region-II is in accumulation mode. This accumulation charges (electrons) must come from a n doped region. Hence, the charges need to be partitioned between the D_i and the D' nodes (n doped).

For $V_{GDi} < V_{FB,dr}$, region-II enters depletion and inversion modes. Similar to the case when the source and the drain (n-doped) regions give rise to the electron inversion charge in region-I (p-doped), when region-II (n-doped) is biased in inversion, the hole inversion layer charge should come from the bulk (p-doped) of the transistor. Hence the hole charge associated with region-II comes from the bulk. Further, The depletion layer charge in the drift region needs to be assigned to D_i and D' nodes of the device, just as the case where the depletion layer charge in region-I is assigned to the bulk.

2.3.3 p-n junction charges

Apart from surface charges caused due to MOS capacitor action, region I and II have yet another source of charge: the depletion region caused due to the reverse biased p-n junctions present between region-I and II and between the source and region-I. These depletion layer charge assignments is similar to that of MOS capacitor depletion layer charge assignment. The depletion charges present

TABLE 2.1: Charge assignment to various terminals

	Region-I	Region-II
Accumulation charge	B	D_i and D'
Depletion charge	B	D_i and D'
Inversion charge	S and D_i	B

on the region-I side is assigned to the bulk of the device, on the region-II side is assigned to the D_i node[4] and on the source side is assigned to the source terminal.

2.3.4 Region-III charges

The only charge variation in region-III of the LDMOS transistor is caused due to the increase in n_{eff} as seen in Fig. 2.4. This increase in effective carrier concentration is insignificant compared to the magnitude of charge variation caused due to other sources. Hence, these charges are neglected while modeling the charges,

The summary of charge assignment to various terminals can be seen in Table 2.1. Apart from the charges mentioned in Table. 2.1, the reverse biased p-n junction charges also need to be taken into account as discussed.

[4]In principle, this depletion charges too need to be partitioned between the D' and the D_i nodes. However, we encounter a few technical issues if done so. These will be dealt in the later chapters.

Chapter 3

Model and Verilog-A implementation

A comprehensive model for any device must be capable of predicting the device performance over a wide range of biases, temperatures and device geometries. Since SOI-LDMOS forms an integral part of HVICs, accurate modeling of these devices is necessary to ensure fail-safe design of HVIC circuits.

Any good LDMOS model must have the following features:

- Accurate modeling of AC/DC terminal currents and the nodal charges in linear, saturation and off modes.
- Continuity of device models in different regions and continuity in their derivatives and double derivatives.
- Conservative nature of charge model.
- Accurate modeling of capacitances to predict the dynamic behavior of the device.
- Modeling high frequency behavior where device operates in Non-Quasi static regime.
- Capability to model impact ionization and snapback and in turn predict SOA.

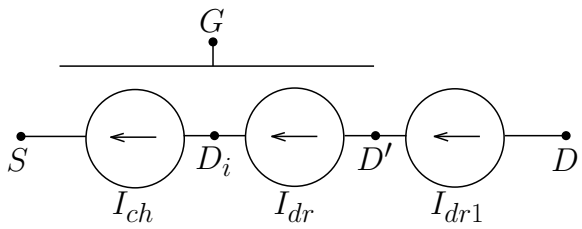


FIGURE 3.1: EC Model for static MOSFET currents.

- Capability to model self heating which requires temperature dependence of model parameters.
- Modeling various types of noise i.e. $1/f$ noise, thermal noise etc.
- Scalability of the model over wide range of bias, geometries and temperatures.

Extensive work has been carried out by [29] in developing a DC model for low bias voltages. [30] extends this model to incorporate various high bias effects like snapback, self-heating and impact-ionization. An charge-partition based AC model is proposed by [31]. In this chapter, a summary of the models proposed by [29–31] is investigated, along with incorporating many changes in both the AC and DC models. The model proposed provides an improvement over one of the currently existing industrial standard compact models: the MM20 model [1, 2, 21].

3.1 Static current model

For the ease of modeling, the LDMOS transistor is divided into three regions - region-I, II and III. For all the analysis to follow, we shall look at these three regions separately and develop compact models for these three regions individually. The LDMOS transistor model is modeled using three current sources [29, 30] as shown in Fig. 3.1. Here I_{ch} is the channel current which is a function of the potential drop across region-I (V_{DiS}). The potential drop across region-II is given by $V_{D'Di}$ and it determines the current flowing through region-II, given by I_{dr}. The current through region-III is I_{dr1} and it is a function of the potential drop across region-III, given by $V_{DD'}$. The current source models are explained in the following subsections.

3.1.1 Formulation of current in channel region

Channel current is modeled using a surface potential approach. The current I_{ch} through the channel is obtained by adding the drift and the diffusion components of the current, i.e.,

$$I_{ch} = \frac{W\mu_{ch}}{L_{ch}} \left(\int_{\psi_{s,0}^{ch}}^{\psi_{s,L}^{ch}} \left(-Q_{inv}^{ch}\right) d\psi_s^{ch} + V_T \left(Q_{inv,L}^{ch} - Q_{inv,0}^{ch}\right) \right) \tag{3.1}$$

where W is the channel width, μ_{ch} is the channel mobility taking into account the effect of lateral and vertical electric fields. L_{ch} is the channel length, ψ_s^{ch} is the surface potential, V_T is the thermal voltage and Q_{inv}^{ch} is the inversion charge per unit area given as $Q_{inv}^{ch} = -C_{ox}V_{inv}$ with $Q_{inv,0}^{ch}$ and $Q_{inv,L}^{ch}$ being the inversion charges at the source and the drain (D_i) terminals. Inversion potential V_{inv} is given by

$$V_{inv} = V_{GB} - V_{FB,ch} - \psi_s^{ch} - k_{ch}\sqrt{\psi_s^{ch}} \tag{3.2}$$

where V_{GB} is the applied gate to bulk voltage, $V_{FB,ch}$ is the flatband voltage of the channel region and k_{ch} is the channel body effect coefficient. On linearizing V_{inv} with respect to the source surface potential $\psi_{s,0}^{ch}$, we get

$$V_{inv} = V_{inv,0} - \zeta \left(\psi_s^{ch} - \psi_{s,0}^{ch}\right) \tag{3.3}$$

with $\zeta = \left(1 + \dfrac{k_{ch}}{2\sqrt{\psi_{s,0}^{ch}}}\right)$[1] and the inversion potential on the source side is given by

$$V_{inv,0} = V_{inv}\,|_{\psi_s^{ch}=\psi_{s,0}^{ch}} = V_{GB} - V_{FB,ch} - \psi_{s,0}^{ch} - k_{ch}\sqrt{\psi_{s,0}^{ch}} \tag{3.4}$$

Using (3.2), (3.3) and (3.4), (3.1) can be simplified as

$$I_{ch} = \frac{W\mu_{ch}C_{ox}}{L_{ch}} \left(V_{inv,0} - \frac{1}{2}\zeta\Delta\psi_s^{ch} + \zeta V_T \right) \Delta\psi_s^{ch} \tag{3.5}$$

[1]This linearization becomes invalid around $\psi_{s,0}^{ch} = 0$ as ζ blows up. To avoid this condition, we use $\zeta = \left(1 + \dfrac{k_{ch}}{2\sqrt{\psi_{s,0}^{ch} + \delta}}\right)$, where δ is a small increment, sufficiently to never allow $\psi_{s,0}^{ch}$ to take a zero value. Of course, this can be completely avoided by not linearizing V_{inv}. But that will add just on to the complexity of the model.

where $\Delta\psi_s^{ch} = \psi_{s,L}^{ch} - \psi_{s,0}^{ch}$, $\psi_{s,0}^{ch}$ and $\psi_{s,L}^{ch}$ are the surface potential at S and D_i nodes respectively. Mobility reduction due to lateral fields which accounts for velocity saturation is given by

$$\mu_{ch} = \frac{\mu_{eff,ch}}{1 + \theta_{3,ch}\Delta\psi_s^{ch}} \tag{3.6}$$

where $\theta_{3,ch} = \dfrac{\mu_{0,ch}}{L_{ch} v_{sat}^{ch}}$ is the parameter that takes care of velocity saturation in the channel, where $\mu_{0,ch}$ is the zero field channel mobility and v_{sat}^{ch} is the saturation velocity in channel. $\mu_{eff,ch}$ accounts for mobility reduction due to the vertical field and is given by

$$\mu_{eff,ch} = \frac{\mu_{0,ch}}{\left(1 + \theta_1 V_{inv,0} + \theta_2 \left(\sqrt{\psi_{s,0}^{ch}} - \sqrt{\psi_{s,0}^{ch}\,|_{V_{SB}=0}}\right)\right)} \tag{3.7}$$

where θ_1 and θ_2 are model parameters. Further, if we incorporate the channel length modulation effects, the expression for channel current becomes

$$I_{ch} = (1 + \lambda_{ch} V_{DiS}) \frac{W \mu_{ch} C_{ox}}{L_{ch}} \left(V_{inv,0} - \frac{1}{2}\zeta\Delta\psi_s^{ch} + \zeta V_T\right) \Delta\psi_s^{ch} \tag{3.8}$$

where λ_{ch} is the channel modulation parameter. The surface potentials at the source and the D_i nodes are computed following the approach of [32]. The surface potential at the source and D_i nodes can be written as

$$\begin{aligned} \psi_{s,0}^{ch} &= \psi\left[V_{GB} - V_{FB,ch}, V_{SB}, k_{ch}\right] \\ \psi_{s,L_{ch}}^{ch} &= \psi\left[V_{GB} - V_{FB,ch}, V_{DiB}, k_{ch}\right]. \end{aligned} \tag{3.9}$$

3.1.2 Formulation of current under gate oxide

The drift current formulation is done in terms of the Quasi-Fermi potential as opposed to the surface potential formulation for the channel current. The current in region-II is a combination of two currents: The surface current caused due to the presence of accumulation charges and the bulk current due to the presence of the n doped drift region. Hence, the current equations can be written as

$$I_{dr} = \frac{W\mu_{dr}}{L_{dr}} \int_{V_{D_i}}^{V_{D'}} \left(-Q_{acc}^{dr}\right) dV_c + \frac{qW\mu_{0,dr} N_{dr} t_{si}}{L_{dr}} V_{D'D_i} \tag{3.10}$$

where V_c represents the quasi-Fermi level along the top oxide semiconductor interface, Q_{acc}^{dr} represents accumulation charge per unit area, W is the drift region width L_{dr} is the drift region length, μ_{dr} is region-II mobility taking into effect of mobility reduction due to lateral and vertical electric fields, $\mu_{0,dr}$ is the low field mobility, $V_{D'D_i}$ is the voltage across region-II, t_{si} is the thickness of the active layer above the buried oxide and q is the electronic charge. The first term of (3.10) refers to the surface current and the second term estimates the bulk current[2]. Note that a one-dimensional analysis is carried out in estimating the region-II current[3].

The surface conduction happens only along the accumulation layer formed along the surface of region-II. This accumulation layer charge can be approximated using

$$Q_{acc}^{dr} = -C_{ox}\left(V_{GC} - V_{FB,dr} - \psi_s^{dr}\right). \tag{3.11}$$

When $V_{GC} > V_{FB,dr}$, accumulation layer will be formed and depletion charge is negligible. Also, under accumulation condition, most of the voltage drop occurs across the gate oxide and value of surface potential is negligible. Hence, one can rewrite (3.11) as

$$Q_{acc}^{dr} = -C_{ox}\left(V_{GC} - V_{FB,dr}\right). \tag{3.12}$$

Following the same approach as previous section, one can linearize the above charge with respect to the terminal D_i. If we consider $V_n^{dr} = -Q_{acc}^{dr}/C_{ox}$, then one can write V_n^{dr} as

$$V_n^{dr} = V_n^{dr}\,|_{V_c=V_{D_i}} - (V_c - V_{D_i}) \tag{3.13}$$

The mobility reduction due to lateral and perpendicular fields is modeled similar to the channel region as follows

$$\mu_{dr} = \frac{\mu_{eff,dr}}{\left(1 + \theta_{3,dr} V_{D'D_i}\right)} \tag{3.14}$$

where $\theta_{3,dr} = \dfrac{\mu_{0,dr}}{L_{dr} v_{sat}^{dr}}$ is the parameter that takes into account velocity saturation in region-II, with v_{sat}^{dr} being the saturation velocity of region-II surface and $\mu_{0,dr}$

[2]The actual bulk current should be estimated by subtracting the depletion regions caused due to the presence of the p-n junction and the gate. However, it is seen that the above expression is a good enough approximation and removing the depletion layer charge does not cause significant improvement in the model.

[3]This is a major drawback of this formulation, as we shall see in Chapter 4

being the low-field mobility. $\mu_{eff,dr}$ account for the mobility reduction due to vertical field and is given by

$$\mu_{eff,dr} = \frac{\mu_{0,dr}}{(1 + \theta_{acc}\,(0.5V_{GD_i} + 0.5V_{GD'} - V_{FB,dr}))} \tag{3.15}$$

where θ_{acc} is a model parameter. Substituting (3.13 , 3.15) in (3.10) gives region-II current as

$$I_{dr} = \frac{W\mu_{dr}C_{ox}}{L_{dr}}\left(V_n^{dr}\mid_{V_c=V_{D_i}} -0.5V_{D'D_i}\right)V_{D'D_i} + \frac{qW\mu_{0,dr}N_{dr}t_{si}}{L_{dr}}V_{D'D_i}. \tag{3.16}$$

This model is only till the onset of saturation. To model saturation, one must compute the saturation potential by forcing $\frac{\partial I_{acc}}{\partial V_{D'D_i}}\mid_{V_{D'D_i}=V_{sat,dr}} = 0$, where I_{acc} is the accumulation current of in region-II given by the first term of (3.16). This gives the region-II saturation potential as

$$V_{sat,dr} = \frac{2V_n^{dr}\mid_{V_c=V_{D_i}}}{1 + \sqrt{1 + 2\theta_{3,dr}V_n^{dr}\mid_{V_c=V_{D_i}}}}. \tag{3.17}$$

The final expression for region-II is given by

$$I_{dr} = \frac{W\mu_{eff,dr}C_{ox}}{L_{dr}}\frac{\left(V_n^{dr}\mid_{V_c=V_{D_i}} -0.5V_{D'D_{i,eff}}\right)V_{D'D_{i,eff}}}{\left(1 + \theta_{3,dr}V_{D'D_{i,eff}}\right)} + \frac{qW\mu_{0,dr}N_{dr}t_{si}}{L_{dr}}V_{D'D_i}. \tag{3.18}$$

where $V_{D'D_{i,eff}}$ is the effective potential drop across region-II which is the minimum of $V_{D'D_i}$ and $V_{sat,dr}$. The transition from linear region to the saturation region is made differentiable by using appropriate smoothing function.

3.1.3 Formulation of current under field oxide

3.1.3.1 2-D resistor under velocity saturation

The drift region under the field oxide could be modeled as a conventional resistor incorporating velocity saturation effects. Using a conventional velocity saturation

model [33], the current I though the 1-D semiconductor block is given by

$$\begin{aligned} I &= q\mu N_{dr1} t_{si} W E_{eff}, \\ \mu &= \frac{\mu_{dr1}}{\left(1+\left(E_{eff}/E_C\right)^{\theta_{dr1}}\right)^{1/\theta_{dr1}}}, \\ E_{eff} &= V_{DD'}/L_{LC}, \\ E_C &= v_{sat}/\mu_{dr1}, \end{aligned} \tag{3.19}$$

where q is the electronic charge, N_{dr1} is the doping concentration, t_{si}, W and L_{LC} are the thickness, width and length of the resistor, respectively, μ_{dr1} is the low field mobility, v_{sat} is the saturation velocity, θ_{dr1} is a model parameter and $V_{DD'}$ is the voltage applied across the resistor. For a large value of $V_{DD'}$, when $E_{eff} \gg E_C$, it can be shown that I saturates due to velocity saturation and becomes independent of $V_{DD'}$.

However, in the case of a 2-D SOI resistor (Fig. 2.3), it is observed that the current increases even after the velocity saturation condition is reached, due to the increase in carrier concentration. This is usually taken care by using a linear correction parameter λ_{dr1} [29] as

$$I' = I(1 + \lambda_{dr1} V_{DD'}), \tag{3.20}$$

where I is given by (3.19). As discussed in Chapter 2, the carrier concentration increase is not strictly linear. There exists threshold values of $V_{DD'}$ beyond which carrier concentration n_{eff} increases. However, as seen in Fig. 2.4, there is no unique threshold value of $V_{DD'}$ beyond which the carrier concentration increases. Further, if a single threshold is considered, as in [17], we found that the model is inaccurate for lower resistor lengths. Hence, considering the average effect of n_{eff} increase at different locations (Fig. 2.4), the n_{eff} is modeled to increase linearly with $V_{DD'}$.

Further, numerical simulations show that λ_{dr1} depends on the length of the resistor. To analyze this dependence, the slope of the I-$V_{DD'}$ characteristics (i.e. λ_{dr1}) for different L_{LC} values are calculated from numerically simulated data at high $V_{DD'}(= 20V)$. It is seen that the variation of λ_{dr1} with respect to L_{LC} follows an

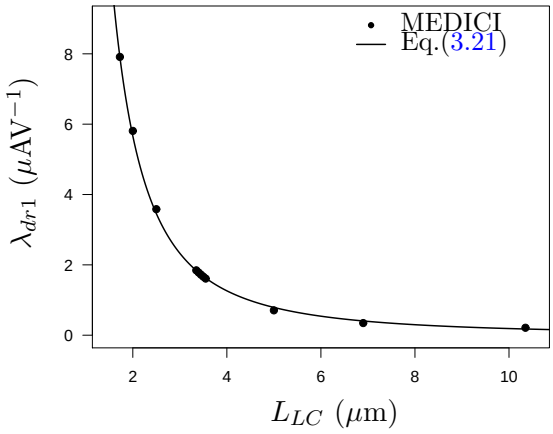


FIGURE 3.2: Inverse square law behaviour (as described in (3.21)) of λ_{dr1} at high $V_{DD'}(= 20V)$.

inverse square law, as shown in Fig. 3.2, given by

$$\lambda_{dr1} = \lambda_{VD}/L^2_{LC,eff}, \tag{3.21}$$

where $L_{LC,eff} = L_{LC} - \Delta L_{LC}$ represents the effective length of the resistor taking into account the 2-D current flow, and λ_{VD} and ΔL_{LC} are model parameters independent of length of the resistor.

Hence, the 2-D resistor, including velocity saturation effects, can be modeled as

$$\begin{aligned}
I &= q\mu_{eff} n_{eff} t_{si} W E_{eff}, \\
\mu_{eff} &= \frac{\mu_{dr1}}{\left(1+\left(E_{eff}/E_C\right)^{\theta_{dr1}}\right)^{1/\theta_{dr1}}}, \\
n_{eff} &= N_{dr1}\left(1 + \left(\lambda_{Vd}/L^2_{LC,eff}\right)V_{DD'}\right), \\
E_{eff} &= V_{DD'}/L_{LC,eff}, \\
E_C &= v_{sat}/\mu_{dr1}.
\end{aligned}$$

3.1.3.2 Modeling the Gate voltage dependence

When an LDMOS transistor is subject to sufficiently high gate and drain voltages, the drain current is controlled by the velocity saturation current of region-III, and the transistor is said to be in quasi-saturation regime of operation. Under such operating conditions, one would expect that the gate voltage does not affect the region-III performance, and hence the drain current becomes independent of gate

voltage. However, the device simulation data indicates that the drain current continues to increase with increasing gate voltage. This effect has been modeled previously by a linear correction term [16], but the source of the effect has not been well studied. Further, the scalability of this effect for varying drift region lengths has not been demonstrated.

As discussed in Chapter 2, the gate voltage dependence is caused due to change in region-III length due to the carrier spill over effect.

This control of effective region-III length by the gate voltage can be modeled by a linear approximation, i.e.,

$$L'_{LC,eff} = L_{LC,eff}(1 - \lambda_{VG} V_{GD'}), \tag{3.22}$$

where $\lambda_{VG}(= \Delta L_{LC,VG}/L_{LC,eff})$ is the region-III length modulation factor (which is the fractional change in the drift region length for a unit change in $V_{GD'}$), $\Delta L_{LC,VG}$ is the change in region-III length for a unit change in $V_{GD'}$ and is independent of region-III length. The parameter $\Delta L_{LC,VG}$ used in the model is obtained from measuring the change in the effective region-III length from Fig. 2.5.

3.1.3.3 Region-III model

The final model for region-III of the SOI-LDMOS transistor, taking into account the 2-D velocity saturation effects, can be written as

$$\begin{aligned} I_{dr1} &= \frac{q n_{eff} \mu_{eff} V_{DD'} W t_{si}}{L_{LC,eff}(1 - \lambda_{VG} V_{GD'})}, \\ \mu_{eff} &= \frac{\mu_{dr1}}{\left(1 + \left(E_{eff}/E_C\right)^{\theta_{dr1}}\right)^{1/\theta_{dr1}}}, \end{aligned}$$

$$\begin{aligned} n_{eff} &= N_{dr1}(1 + \lambda_{dr1} V_{DD'}), & L_{LC,eff} &= L_{LC} - \Delta L_{LC}, \\ E_{eff} &= V_{DD'}/L_{LC,eff}, & E_C &= v_{sat}/\mu_{dr1}, \\ \lambda_{dr1} &= \lambda_{VD}/L^2_{LC,eff}, & \lambda_{VG} &= \Delta L_{LC,VG}/L_{LC,eff}. \end{aligned} \tag{3.23}$$

Here, the model parameters ΔL_{LC}, $\Delta L_{LC,VG}$, λ_{Vd}, μ_{dr1}, θ_{dr1} and v_{sat} are invariant under any change in the region-III length.

3.2 Charge Model

In this thesis, the transient and AC analysis is carried out using a charge based modeling approach. This means that we need to assign charges to various nodes accurately. Once the charges are assigned accurately to each node, the corresponding time derivative gives the transient current through that node.

Charge modeling of an LDMOS transistor has been dealt with in great detail in [31]. However, there were several reported inaccuracies in the model in [31]. This was especially true in the negative V_{GS} regime where the accumulation charge in region-I and inversion charge in region-II were incorrectly assigned. Further, the p-n junction charges present due to the region-I and II reverse biased junction were not accounted for. In this section, a new accurate description of the charge model is proposed.

Table 2.1 gives the charge assignment of various kinds of charges in an SOI-LDMOS transistor. The accumulation charges in region-II and the inversion layer charges in region-I needs to be split between the S, D_i and D' nodes.

3.2.1 The MM20 approach

The MM20 model, which is taken as the base case for our model, uses a Modified Ward-Dutton partitioning scheme (MWD scheme) to achieve this split of charges. The MM20 group published two papers [1] and [2] where they seemingly advocated two different models for charge partitioning. In this section, we shall have a look at these two models individually and show the equivalence between the formulations in these two works.

3.2.1.1 Model proposed by [1]

The following is the summary of the model proposed by [1]. This nodal charge model has four nodes: gate (G), drain (D), source (S) and bulk (B). Region-III is elimated from the discussion of charge model, as it is modeled as a voltage dependent resistor, void of any capacitive effects. Further, this model lifts the necessity of using an internal node (D_i), which forms the distinction between region-I and region-II, by carefully handling the charge partitioning at the source and drain terminals. The source terminal is the reference node, and the charge at this terminal Q_S is computed by the conservation of charge, given by:

$$Q_S = -(Q_G + Q_B + Q_D) \tag{3.24}$$

where Q_G, Q_B and Q_D represents the gate, bulk and drain charges respectively.

The total gate charge is given by adding the channel region (region-I) contribution (Q_G^{ch}) and the drift region (region-II) contribution (Q_G^{dr}), i.e., $Q_G = Q_G^{ch} + Q_G^{dr}$, where

$$\begin{aligned} Q_G^{ch} &= -W \int_0^{L} (Q_{acc}^{ch} + Q_{dep}^{ch} + Q_{inv}^{ch}) dx, \\ Q_G^{dr} &= -W \int_{L}^{L+L_D} (Q_{acc}^{dr} + Q_{dep}^{dr} + Q_{inv}^{dr}) dx. \end{aligned} \tag{3.25}$$

Here, Q_{acc} is the accumulation charge density, Q_{inv} is the inversion layer charge density and Q_{dep} is the depletion layer charge density. The superscripts *ch* and *dr* represents channel (region-I) and drift (region-II) regions respectively of the LDMOS transistor (the same convention has been adopted throughout).

The hole charge when Region-I is biased in accumulation (Q_{acc}^{ch}) and the depletion layer charge (Q_{dep}^{ch}) when biased in weak/strong inversion is attributed to the bulk terminal of the transistor. Further, similar to the case when the source and the drain (n-doped) regions give rise to the electron inversion charge in the channel (p-doped), when region-II (n-doped) is biased in inversion, the hole inversion layer charge (Q_{inv}^{dr}) can be assumed to come from the bulk (p-doped) of the transistor.

Hence the total bulk $Q_B = Q_B^{ch} + Q_B^{dr}$ is given by

$$Q_B^{ch} = -W \int_0^L (Q_{acc}^{ch} + Q_{dep}^{ch}) dx,$$
$$Q_B^{dr} = -W \int_L^{L+L_D} Q_{inv}^{dr} dx. \tag{3.26}$$

Now, all that is left is to assign charge to the drain terminal. According to [1], the charge assignment to the drain terminal is done in two different ways corresponding to the weak and the strong inversion conditions of region-I. This charge partitioning scheme is referred to as the MWD scheme.

Before jumping into the charge assignment equations proposed by [1], we shall understand the motivation behind the MWD source-drain charge partitioning.

1. The entire depletion layer charge $Q_{dep,D}^{dr}$ that arises in region-II (during inversion) is attributed to the drain, just as bulk terminal gives rise to the depletion charge in region-I.

2. Following the usual WD partitioning scheme, we assign a part of the drift region accumulation charge $Q_{acc,D}^{dr}$ to the drain terminal.

3. The other portion of the drift region accumulation charge $Q_{acc,S}^{dr}$, which is supposed to be assigned to the source, is further divided into two portions, and assigned to the source and the drain respectively. This split depends on how close the source terminal is to the boundary of region-II, and is decided by the factor $F_L = L/(L + L_D)$. The source terminal is attributed $(1 - F_L)Q_{acc,S}^{dr}$ and the drain terminal is assigned $F_L Q_{acc,S}^{dr}$. Observe that smaller the L with respect to L_D, larger (smaller) is the fraction of charge assigned to the source (drain).

4. A similar partitioning is done for the electron inversion layer in region-I. A part of the inversion layer charge $Q_{inv,S}^{ch}$, following the usual WD partitioning is assigned to the source. Again, the other portion which should be assigned to the drain is split into two parts, and assigned to the source $((1-F_L)Q_{inv,D}^{ch})$ and the drain $(F_L Q_{inv,D}^{ch})$ respectively, owing to the isolation of the drain terminal caused by the region-II.

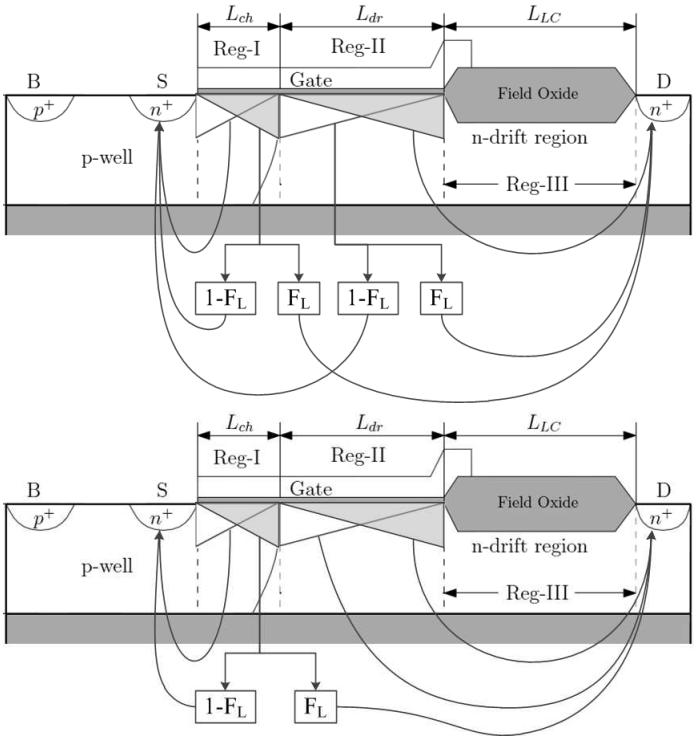


FIGURE 3.3: Charge partitioning under strong (top) and weak (bottom) inversions of region-I.

The last three points are summarized in Figure 3.3, which shows the source-drain charge partitioning of inversion/accumulation layer charges. Hence, the charge attributed to the drain can be written as

$$Q_D = F_L Q^{ch}_{inv,D} + Q^{dr}_{acc,D} + F_L Q^{dr}_{acc,S} + Q^{dr}_{dep,D}, \tag{3.27}$$

where

$$\begin{aligned}
Q^{ch}_{inv,D} &= W \int_0^L \frac{x}{L} Q^{ch}_{inv} dx, \\
Q^{dr}_{acc,D} &= W \int_0^{L_D} \frac{\tilde{x}}{L_D} Q^{dr}_{acc} d\tilde{x}, \\
Q^{dr}_{acc,S} &= W \int_0^{L_D} \left(1 - \frac{\tilde{x}}{L_D}\right) Q^{dr}_{acc} d\tilde{x}, \\
Q^{dr}_{dep,D} &= W \int_0^{L_D} Q^{dr}_{dep} dx.
\end{aligned} \tag{3.28}$$

Here, $\tilde{x} = x - L$, a shifted co-ordinate system.

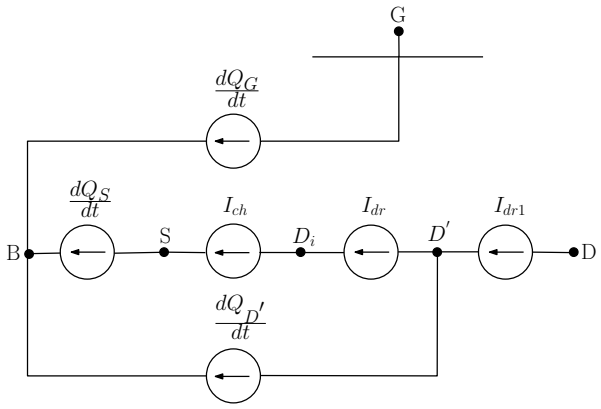


FIGURE 3.4: EC Model for static and dynamic and LDMOS transistor currents using MM20 formulation

In the case when region-I is in accumulation or weak inversion, all the accumulation charge of the drain region is attributed to the drain (refer Figure 3.3). The motivation behind doing such a charge assignment probably lies in the fact that the region-II is isolated from the source when the channel is in weak inversion, and hence the source terminal is not responsible for the electron accumulation charge in region-II. Therefore, the drain drift region charge is approximated as

$$Q_D = F_L Q^{ch}_{inv,D} + Q^{dr}_{acc,D} + Q^{dr}_{acc,S} + Q^{dr}_{dep,D}. \tag{3.29}$$

3.2.1.2 Model proposed by [2]

Many features of charge partitioning model given by [2] similar to that of [1]. Only the aspects in which [2] is different from [1] is discussed here.

The reference terminal in this model, instead of the source, is the bulk terminal. Further, the charge partitioning equations appear differently as compared to [1]. The gate charge equation is same as that in (3.25). The charge at the drain and source terminal is assigned as

$$Q_D = Q^{ch}_D + Q^{dr}_D, \quad Q_S = Q^{ch}_S + Q^{dr}_S. \tag{3.30}$$

The channel contributions to the source and the drain charges are

$$Q_D^{ch} = W \int_0^L \frac{x}{L + L_D} Q_{inv}^{ch} dx,$$
$$Q_S^{ch} = W \int_0^L \left(1 - \frac{x}{L + L_D}\right) Q_{inv}^{ch} dx, \tag{3.31}$$

The region-II contribution is, as carried out in [1], is considered in two cases. When region-I is in strong inversion, the source and drain contributions to drift region charge is given by

$$Q_D^{dr} = W \int_L^{L+L_D} \frac{x}{L + L_D} (Q_{acc}^{dr} + Q_{dep}^{dr}) dx,$$
$$Q_S^{dr} = W \int_L^{L+L_D} \left(1 - \frac{x}{L + L_D}\right) (Q_{acc}^{dr} + Q_{dep}^{dr}) dx. \tag{3.32}$$

and under weak inversion, the contribution to the drift charge is completely given to the drain region.

$$Q_D^{dr} = W \int_L^{L+L_D} (Q_{acc}^{dr} + Q_{dep}^{dr}) dx,$$
$$Q_S^{dr} = 0. \tag{3.33}$$

3.2.1.3 A Comparative study

Although the models proposed by [1] and [2] seem vastly different, they can be shown to be equivalent. Consider, for instance, the drift region contribution to the drain charge when region-I is in strong inversion. When region-I is in strong inversion, region-II is likely to be in accumulation. This means that the region-II depletion layer charge $Q_{dep}^{dr} = 0$. Hence, according to [1],

$$\begin{aligned}
Q_D &= F_L Q_{inv,D}^{ch} + Q_{acc,D}^{dr} + F_L Q_{acc,S}^{dr} \\
&= \frac{WL}{L + L_D} \int_0^L \frac{x}{L} Q_{inv}^{ch} dx + W \int_0^{L_D} \frac{\tilde{x}}{L_D} Q_{acc}^{dr} d\tilde{x} + \frac{WL}{L + L_D} \int_0^{L_D} \left(1 - \frac{\tilde{x}}{L_D}\right) Q_{acc}^{dr} d\tilde{x} \\
&= W \int_0^L \frac{x}{L + L_D} Q_{inv}^{ch} dx + W \int_0^{L_D} \left(\frac{\tilde{x}}{L_D}\right) \left(\frac{L_D - \tilde{x}}{L + L_D}\right) Q_{acc}^{dr} d\tilde{x} \\
&= W \int_0^L \frac{x}{L + L_D} Q_{inv}^{ch} dx + W \int_L^{L+L_D} \left(\frac{x - L}{L_D}\right) \left(\frac{L_D - (x - L)}{L + L_D}\right) Q_{acc}^{dr} dx \\
&= W \int_0^L \frac{x}{L + L_D} Q_{inv}^{ch} dx + W \int_L^{L+L_D} \frac{x}{L + L_D} Q_{acc}^{dr} dx,
\end{aligned}$$

which is precisely the expression for charge partitioning in [2] for the drain terminal, when region-I is in strong inversion. A similar equivalence can be shown for the charge partitioning when region-I is in weak inversion, or in accumulation.

3.2.1.4 EC Model for MM20 charge partitioning

Figure 3.4 shows the equivalent circuit model of MM20 model. The charges are assigned to four terminals, i.e., G, D', S and B. From each of these terminals the displacement current source dQ/dt is connected to the bulk terminal which is a reference. Due to the circuit topology and by charge conservation, dQ_B/dt is calculated automatically.

3.2.2 A New Charge Partitioning scheme

A new charge partitioning scheme is proposed in this section by the addition of an internal node.

3.2.2.1 Need for an additional internal node

The following are the advantages of incorporating an internal node and assigning charges to the internal node in the charge partitioning scheme:

1. The MM20 equations elevates the necessity of the internal node by making several assumptions to the charge partitioning. One of the major unexplained feature of MM20 method of charge partitioning is the way in which there is a difference in the above threshold and below threshold charge assignments, as given by (3.27) and (3.29). Special care should be taken to implement this change in a smooth manner, so that there are no discontinuities in the model because of the usage of two different equations in two operating regions. However, as we shall see later, even if the model is implemented in a smooth manner, there are notable discontinuities in the capacitance plots. These discontinuities become more significant for wider region-II lengths (i.e., $L_{dr} \gg L_{ch}$). These discontinuities can be completely

avoided by the use of an internal node, in which there are no region based differences in charge partitioning.

2. The MM20 model assumes that $I_{ch} = I_{dr}$ for all cases, including the transient situation. However, if the system is not in steady state, it is observed that $I_{ch} \neq I_{dr}$. This difference arises because the two regions are electrostatically different. Under a transient input, both the currents will achieve the same value only when the input stabilizes to a steady value. An addition of an internal node ensures that the electostatically different region-I and region-II charges are dealt with differently.

3. Finally, as an added advantage, the accuracy of the model increases further by the addition of an extra internal node.

3.2.2.2 The proposed charge partitioning scheme

A physical basis for charge partitioning using an internal node D_i was discussed briefly in Chapter 2. A summary of the discussion can be found in Table 2.1. To split the inversion charge in region-I between the nodes S and D_i, and to split the accumulation and depletion charges in region-II between the nodes D_i and D' we use a Ward-Dutton partitioning scheme[27].

The following equations describe the new proposed charge partitioning scheme

$$
\begin{aligned}
Q_S &= W \int_0^{L_{ch}} \left(1 - \frac{x}{L_{ch}}\right) Q_{inv}^{ch} dx + Q_n^{pns}, \\
Q_{D_i} &= W \int_0^{L_{ch}} \left(\frac{x}{L_{ch}}\right) Q_{inv}^{ch} dx + W \int_0^{L_{dr}} \left(1 - \frac{x'}{L_{dr}}\right) \left(Q_{acc}^{dr} + Q_{dep}^{dr}\right) dx' + Q_n^{pnd}, \\
Q_{D'} &= W \int_0^{L_{dr}} \left(\frac{x'}{L_{dr}}\right) \left(Q_{acc}^{dr} + Q_{dep}^{dr}\right) dx', \\
Q_G &= -W \int_0^{L_{ch}} \left(Q_{acc}^{ch} + Q_{dep}^{ch} + Q_{inv}^{ch}\right) dx - W \int_0^{L_{dr}} \left(Q_{acc}^{dr} + Q_{dep}^{dr} + Q_{inv}^{dr}\right) dx', \\
Q_B &= W \int_0^{L_{ch}} \left(Q_{acc}^{ch} + Q_{dep}^{ch}\right) dx + W \int_0^{L_{dr}} \left(Q_{inv}^{dr}\right) dx' + Q_p^{pnd} + Q_p^{pns}.
\end{aligned}
$$

Here, Q_i represents total charge assigned to node i ($i \in G, S, B, D_i, D'$), Q_{acc} is the accumulation charge density per unit area, Q_{inv} is the inversion layer charge density per unit area and Q_{dep} is the depletion layer charge density per unit area.

The subscripts *ch* and *dr* represents channel (region-I) and drift (region-II) regions respectively of LDMOS transistor. Further, Q_n^{pnd} (Q_n^{pns}) represents the total p-n junction charge in the n-drift region (source junction) and $Q_p^{pnd} = -Q_n^{pnd}$ ($Q_p^{pns} = -Q_n^{pns}$) is the total p-n junction charge in the p-well on the drain (source) side. Note that x is a co-ordinate system starting from the source terminal and x' is a shifted co-ordinate system starting from the D_i node.

Notice that the total charge remains conserved, i.e,

$$Q_B + Q_G + Q_S + Q_{D'} + Q_{D_i} = 0. \tag{3.34}$$

3.2.2.3 Formulation of charge in region-I

Since the channel region of SOI-LDMOS is structurally similar to an NMOSFET, charge modeling should be similar to MOS charge modeling. Charges that are of interest to us are the depletion, inversion and accumulation charges. The (negative) depletion charge per unit area Q_{dep}^{ch} can be written as

$$Q_{dep}^{ch} = \begin{cases} -C_{ox} k_{ch} \sqrt{\psi_s^{ch}} & \text{for } \psi_s^{ch} \geq 0, \\ 0 & \text{for } \psi_s^{ch} < 0, \end{cases} \tag{3.35}$$

where ψ_s^{ch} is the surface potential of the channel. Similarly, the (negative) inversion (Q_{inv}^{ch}) and the (positive) accumulation (Q_{acc}^{ch}) charge are given by

$$Q_{inv}^{ch} = \begin{cases} -C_{ox} \left(V_{GB} - V_{FB,ch} - \psi_s^{ch} - k_{ch} \sqrt{\psi_s^{ch}} \right) & \text{for } \psi_s^{ch} \geq 0, \\ 0 & \text{for } \psi_s^{ch} < 0. \end{cases} \tag{3.36}$$

$$Q_{acc}^{ch} = \begin{cases} -C_{ox} \left(V_{GB} - V_{FB,ch} \right) & \text{for } \psi_s^{ch} < 0, \\ 0 & \text{for } \psi_s^{ch} \geq 0. \end{cases} \tag{3.37}$$

We shall first consider that there are only inversion and depletion charges present in the channel, i.e., $V_{GC} > V_{FB,ch}$ everywhere in region-I. Potentials V_{dep} and V_{inv} can be defined as $V_{dep} = -Q_{dep}^{ch}/C_{ox}$ and $V_{inv} = -Q_{inv}^{ch}/C_{ox}$ so that the analysis of charges can be done completely in terms of potentials. Since V_{dep} and V_{inv} are non-linear functions of surface potential, approximations of these charges are done

with respect to the source terminal (similar to Sec 3.1.1) as

$$\begin{aligned} V_{dep} &= V_{dep}\mid_{\psi_s^{ch}=\psi_{s,0}^{ch}} + (\zeta-1)\left(\psi_s^{ch}-\psi_{s,0}^{ch}\right), \\ V_{inv} &= V_{inv}\mid_{\psi_s^{ch}=\psi_{s,0}^{ch}} -\zeta\left(\psi_s^{ch}-\psi_{s,0}^{ch}\right), \end{aligned} \tag{3.38}$$

where $\zeta = \left(1+\dfrac{1}{2\sqrt{\psi_{s,0}^{ch}}}\right)$. The charges have now been defined and approximated with respect to the source terminal. To obtain the final gate, source and drain expressions, one must know the variation of charge densities as a function of x. Hence, one must find the dependence of ψ_s^{ch} with x so that the charges can be expressed as a function of x. To obtain that, we use the channel current expression. The channel current can be written as

$$I_{ch} = W\mu_{ch}C_{ox}\left(V_{inv}\frac{d\psi_s}{dx} - V_T\frac{dV_{inv}}{dx}\right), \tag{3.39}$$

where the parameters in the equation are as defined in Sec 3.1.1. Incorporating the linearization made in (3.38) and integrating the above expression from 0 to x, we get

$$I_{ch}x = W\mu_{ch}C_{ox}\left[\int_{\psi_{s,0}^{ch}}^{\psi_s^{ch}(x)}\left(V_{inv,0}-\zeta\left(\psi_s^{ch}-\psi_{s,0}^{ch}\right)\right)d\psi_s + \zeta V_T\int_{\psi_{s,0}^{ch}}^{\psi_s^{ch}(x)} d\psi_s^{ch}\right]. \tag{3.40}$$

Upon replacing I_{ch} with (3.5) and simplifying we get

$$x = L_{ch}\left[\frac{\left(V_{inv,0}+\zeta\psi_{s,0}^{ch}+\zeta V_T\right)\left(\psi_s^{ch}(x)-\psi_{s,0}^{ch}\right) - \zeta\left(\dfrac{(\psi_s^{ch}(x))^2-(\psi_{s,0}^{ch})^2}{2}\right)}{\left(V_{inv,0}-\dfrac{1}{2}\zeta\Delta\psi_s^{ch}+\zeta V_T\right)\Delta\psi_s^{ch}}\right]. \tag{3.41}$$

Instead of expressing ψ_s as a function of x, x has been represented as a function of ψ_s. This is to make future integration calculations simpler.[4] Since the drain and source terminals for the channel region in LDMOS are D_i and S terminals, charge partitioning is done between those two terminals. Now we can proceed to

[4]If ψ_s^{ch} is represented as a function of x, then we encounter polynomial under square root during the integration computation which is cumbersome to solve. Writing x in terms of ψ_s^{ch} results in solving quadratic expression under integral.

calculate various charges as follows

$$\begin{aligned} Q_G^{ch} &= WC_{ox}\int_0^{L_{ch}} (V_{inv,0}+V_{dep,0}) - \left(\psi_s^{ch}(x)-\psi_{s,0}^{ch}\right) dx, \\ Q_{D_i}^{ch} &= -WC_{ox}\int_0^{L_{ch}} \left(\frac{x}{L_{ch}}\right)\left(V_{inv,0}-\zeta\left(\psi_s^{ch}(x)-\psi_{s,0}^{ch}\right)\right) dx, \\ Q_S^{ch} &= -WC_{ox}\int_0^{L_{ch}} \left(1-\frac{x}{L_{ch}}\right)\left(V_{inv,0}-\zeta\left(\psi_s^{ch}(x)-\psi_{s,0}^{ch}\right)\right) dx. \end{aligned} \tag{3.42}$$

After integration, various charge expressions are

$$\begin{aligned} Q_G^{ch} &= C_{ox}WL_{ch}\left[V_{GB}-V_{FB}^{ch}-\frac{1}{2}\left(\psi_{s,L}^{ch}+\psi_{s,0}^{ch}\right)+\frac{F_{ch}}{12\zeta}\Delta V_{GT}\right], \\ Q_{D_i}^{ch} &= -\frac{C_{ox}}{2}WL_{ch}\left[\overline{V}_{GT}-\frac{\Delta V_{GT}}{6}\left(1-\frac{F_{ch}}{2}-\frac{F_{ch}^2}{20}\right)\right], \\ Q_S^{ch} &= -\frac{C_{ox}}{2}WL_{ch}\left[\overline{V}_{GT}+\frac{\Delta V_{GT}}{6}\left(1+\frac{F_{ch}}{2}-\frac{F_{ch}^2}{20}\right)\right], \end{aligned} \tag{3.43}$$

where

$$\Delta V_{GT} = V_{inv,0}-V_{inv,L_{ch}},\ \overline{V}_{GT}=\frac{V_{inv,0}+V_{inv,L_{ch}}}{2},\ F_{ch}=\frac{\Delta V_{GT}}{\overline{V}_{GT}+\zeta V_T}. \tag{3.44}$$

The surface potentials $\psi_{s,0}^{ch}$ and $\psi_{s,L}^{ch}$ are computed using a surface potential function[5] [21]. The surface potential at the source and D_i terminal can be written as

$$\begin{aligned} \psi_{s,0}^{ch} &= \psi\left[V_{GB}-V_{FB,ch}, V_{SB}, k_{ch}\right], \\ \psi_{s,L}^{ch} &= \psi\left[V_{GB}-V_{FB,ch}, V_{DiB}, k_{ch}\right]. \end{aligned} \tag{3.45}$$

In the negative V_{GS} regime of operation (i.e., when $V_{GS} < V_{FB,ch}$), it is not very difficult to notice that the same expressions as (3.43) holds true. This is because, the inversion layer charge (and hence V_{inv}) is zero. As a result, the following equations are obtained[6]

$$\begin{aligned} Q_G^{ch} &\approx C_{ox}WL_{ch}\left[V_{GB}-V_{FB}^{ch}\right], \\ Q_{D_i}^{ch} &= 0, \\ Q_S^{ch} &= 0. \end{aligned} \tag{3.46}$$

[5] Alternatively, one can also follow [34] for the implementation of the surface potential function.

[6] The same equations can be obtained by considering accumulation region of operation in the beginning.

By the principle of conservation of charges, the bulk charge automatically gets determined from (3.43) and (3.46).

3.2.2.4 Formulation of charge in region-II

Charge modeling in drift region is algorithmically similar to the channel region. Since the current formulation is done in terms of quasi-Fermi potential V_c, charge modeling is also done in accordance with that. We shall first analyse region-II in the accumulation mode of operation. The net accumulation charge density in the drift region can be written as

$$Q_{acc}^{dr} = -C_{ox}\left(V_{GC} - V_{FB,dr} - \psi_s^{dr}\right). \tag{3.47}$$

If we consider $V_n^{dr} = -Q_{acc}^{dr}/C_{ox}$, and upon linearizing the potential with respect to D_i terminal, we get

$$V_n^{dr} = V_n^{dr}\,|_{V_c=V_{D_i}} - (V_c - V_{D_i}). \tag{3.48}$$

The above expression is substituted in the drift current expression and integrated from 0 to x to obtain

$$I_{acc}x = W\mu_{dr}C_{ox}\left[\int_{V_{D_i}}^{V_c}\left(V_n^{dr}\,|_{V_c=V_{D_i}} - (V_c - V_{D_i})\right)dV_c\right]. \tag{3.49}$$

Upon replacing I_{acc} with (3.16) and simplifying one gets

$$x = L_{dr}\left[\frac{\left(V_n^{dr}\,|_{V_c=V_{D_i}} + V_{D_i}\right)(V_c(x) - V_{D_i}) - \dfrac{V_c(x)^2}{2}}{\left(V_n^{dr}\,|_{V_c=V_{D_i}} - 0.5V_{D'D_i}\right)V_{D'D_i}}\right]. \tag{3.50}$$

The analogous drain and source terminals for the drift region in LDMOS are D' and D_i terminals and charge partition is done between those two terminals. Now

one can proceed to calculate various charges as follows

$$\begin{aligned} Q_G^{dr} &= WC_{ox}\int_0^{L_{dr}} \left(V_n^{dr}\mid_{V_c=V_{D_i}} - (V_c - V_{D_i})\right) dx', \\ Q_{D'}^{dr} &= -WC_{ox}\int_0^{L_{dr}} \left(\frac{x}{L_{dr}}\right)\left(V_n^{dr}\mid_{V_c=V_{D_i}} - (V_c - V_{D_i})\right) dx', \\ Q_{D_i}^{dr} &= -WC_{ox}\int_0^{L_{dr}} \left(1-\frac{x}{L_{dr}}\right)\left(V_n^{dr}\mid_{V_c=V_{D_i}} - (V_c - V_{D_i})\right) dx'. \end{aligned} \tag{3.51}$$

After integration, various charge expressions are

$$\begin{aligned} Q_G^{dr} &= C_{ox}WL_{dr}\left[\frac{1}{2}\left(V_{GD_i}^{dr} + V_{GD'}^{dr} - 2V_{FB}^{dr}\right) - \frac{1}{2}\left(\psi_{sD_i}^{dr} + \psi_{sD'}^{dr}\right) + \frac{F^{dr}}{12}\Delta V_q^{dr}\right], \\ Q_{D'}^{dr} &= -\frac{C_{ox}}{2}WL_{dr}\left[\overline{V}_q^{dr} - \frac{\Delta V_q^{dr}}{6}\left(1 - \frac{F^{dr}}{2} - \frac{F^{dr^2}}{20}\right)\right], \\ Q_{D_i}^{dr} &= -\frac{C_{ox}}{2}WL_{dr}\left[\overline{V}_q^{dr} + \frac{\Delta V_q^{dr}}{6}\left(1 + \frac{F^{dr}}{2} - \frac{F^{dr^2}}{20}\right)\right], \end{aligned} \tag{3.52}$$

where

$$\Delta V_q^{dr} = V_{nD_i}^{dr} - V_{nD'}^{dr},\ \overline{V}_q^{dr} = \frac{V_{nD_i}^{dr} + V_{nD'}^{dr}}{2},\ F^{dr} = \frac{\Delta V_q^{dr}}{\overline{V_q^{dr}}}. \tag{3.53}$$

The surface potentials $\psi_{sD_i}^{dr}$ and $\psi_{sD'}^{dr}$ are computed using the same surface potential function as discussed in previous section. The surface potential at terminals D_i and D' are

$$\begin{aligned} \psi_{sD_i}^{dr} &= -\psi\left[-V_{GD_i} + V_{FB,dr}, V_{D_iB}, k_{dr}\right], \\ \psi_{sD'}^{dr} &= -\psi\left[-V_{GD'} + V_{FB,dr}, V_{D'B}, k_{dr}\right]. \end{aligned} \tag{3.54}$$

However, when $V_{GC} < V_{FB,dr}$, the region-III operates in depletion and inversion region of operation. The depletion charges needs to be partitioned between D_i and D' similar to (3.52), whereas the inversion charges are attributed to the bulk. Hence, (3.52) can be used for both positive and negative V_{GS} regime with a transformation of V_n^{dr} being replaced by $V_{accdep}^{dr} = -(Q_{acc}^{dr} + Q_{dep}^{dr})/C_{ox}$. As in case of region-I, the inversion charges are automatically assigned to the bulk by the principle of charge conservation.

3.2.2.5 Formulation of the p-n junction charges

The p-n junction charges on the drain side are modeled by using standard charge expressions for the depletion region in a reverse bias diode. P-n junction charges in region-I needs to assigned to the bulk, but on the side of region-II needs to be assigned to both D_i and D'. However, due to the proximity of the p-n junction to the D_i node, and due to the fact that region-II fails to have a two-dimensional mode, we just assign all the p-n junction charges to the D_i node.

$$Q_n^{pnd} = W t_{si} \sqrt{\frac{2\epsilon_{si} q N_{ch} N_{dr} (V_{bid} + V_{D'B})}{N_{ch} + N_{dr}}} = -Q_p^{pnd}, \tag{3.55}$$

where $V_{D'B}$ is the voltage that appears across the reverse biased diode, V_{bid} is the built in potential of the p-n junction given by

$$V_{bid} = V_T \ln \left(\frac{N_C N_D}{n_i^2} \right), \tag{3.56}$$

V_T is the thermal voltage, N_C and N_V are the effective density of states in the conduction and valence bands respectively, n_i is the intrinsic carrier concentration.

Using a similar approach, we model the p-n junction charges on the source side. However, a problem that arises on the source side is the fact the junction itself is not a 1-D junction. Hence, for the ease of modeling, the junction is considered to be a rectangular junction and the p-n junction charges are estimated using

$$Q_n^{pns} = W(W_{src} + 2D_{src}) \sqrt{\frac{2\epsilon_{si} q N_{ch} N_s (V_{bis} + V_{SB})}{N_{ch} + N_s}} = -Q_p^{pns}, \tag{3.57}$$

where V_{SB} is the voltage that appears across the reverse biased diode, V_{bis} is the built in potential of the p-n junction given by

$$V_{bis} = V_T \ln \left(\frac{N_C N_s}{n_i^2} \right), \tag{3.58}$$

and N_s is the doping concentration on the source junction.

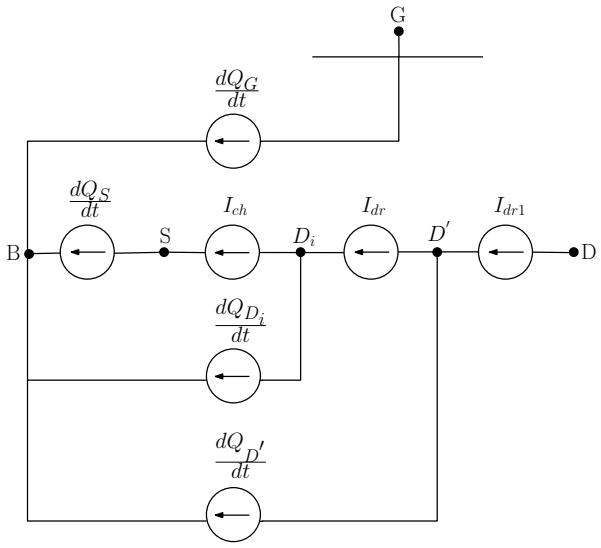


FIGURE 3.5: EC Model for static and dynamic and LDMOS transistor currents using the proposed formulation

3.2.2.6 EC Model for the proposed charge partitioning

Figure 3.5 shows the equivalent circuit model of the proposed model. The charges are assigned to five terminals, i.e., G, D', D_i, S and B as

$$\begin{aligned} Q_G &= Q_G^{ch} + Q_G^{dr}, \\ Q_S &= Q_S^{ch} + Q_n^{pns}, \\ Q_{D_i} &= Q_{D_i}^{ch} + Q_{D_i}^{dr} + Q_n^{pnd}, \\ Q_{D'} &= Q_{D'}^{dr}, \\ Q_B &= -\left(Q_G + Q_S + Q_{D_i} + Q_D^{'}\right). \end{aligned} \tag{3.59}$$

From each of these terminals the displacement current source dQ/dt is connected to the bulk terminal which is a reference. Due to the circuit topology and by charge conservation, dQ_B/dt is calculated automatically. Note the region-III is assumed to be a passive region in charge analysis[7].

[7]This is not entirely true. As we saw earlier, there is an effective carrier concentration increase, once velocity saturation sets in.

Chapter 4

Results and Discussions

Physics-based device simulations are carried out using the commercially available device simulator Taurus-MEDICI[28]. The proposed model is implemented in Verilog-A[35, 36]. Circuit simulations using the implemented model are carried out using the commercially available circuit simulator Cadence Spectre[37]. In all the plots in this chapter, solid lines represent Verilog-A implemented model results and symbols represent MEDICI simulation results. Arrows represent the direction in which corresponding quantities increase. The parameter values used in the model are given in Appendix A

4.1 Static Characteristics

4.1.1 2-D resistor characteristics

A scalable two-dimensional model was proposed for region-II in Sec 3.1.3.1. Fig. 4.1 demonstrates the scalability of the resistor model (3.22) by comparing the model data with the MEDICI simulations for the structure shown in Fig. 2.3. It is observed that the proposed 2-D SOI-resistor model accurately predicts the device simulation data over a wide range of resistor lengths.

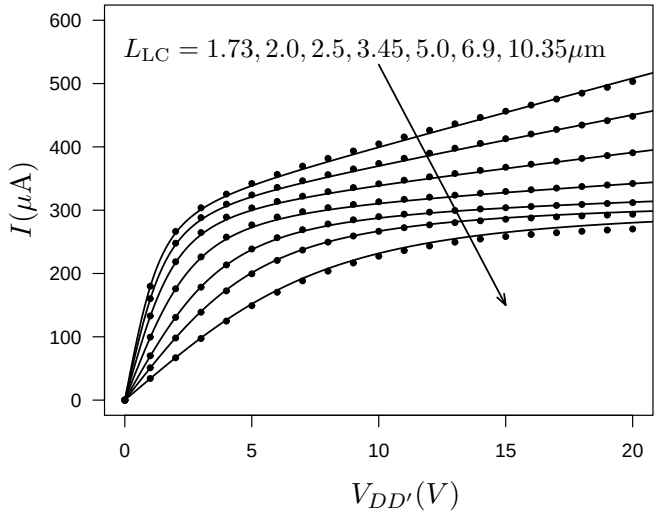


FIGURE 4.1: Comparison of 2-D resistor characteristics for different resistor lengths obtained using the proposed model (solid lines) with MEDICI data (symbols)

4.1.2 Static SOI-LDMOS characteristics

Incorporating the newly proposed region-III model as discussed in Chapter 3, the output characteristics ($I_D - V_{GS}$ and $I_D - V_{DS}$) were simulated. Fig. 4.2 shows the comparison of model results along with the device simulator MEDICI data. We note that there is an excellent agreement between the device simulator and the model data over a wide range of region-III lengths. the model captures the quasi-saturation effect caused by the presence of region-III accurately. Hence, this successfully demonstrates the scalability of the proposed SOI-LDMOS model over a wide range of region-III lengths.

4.2 Capacitance Characteristics

From the implemented model, the capacitances of the LDMOS transistor are extracted by applying a small signal voltage at a frequency $f = 100MHz$ to a particular terminal and extracting the imaginary part of the current flowing from the different terminals. These imaginary currents arise due to the displacement current terms (dQ/dt terms) in the equivalent circuit model. The net small signal

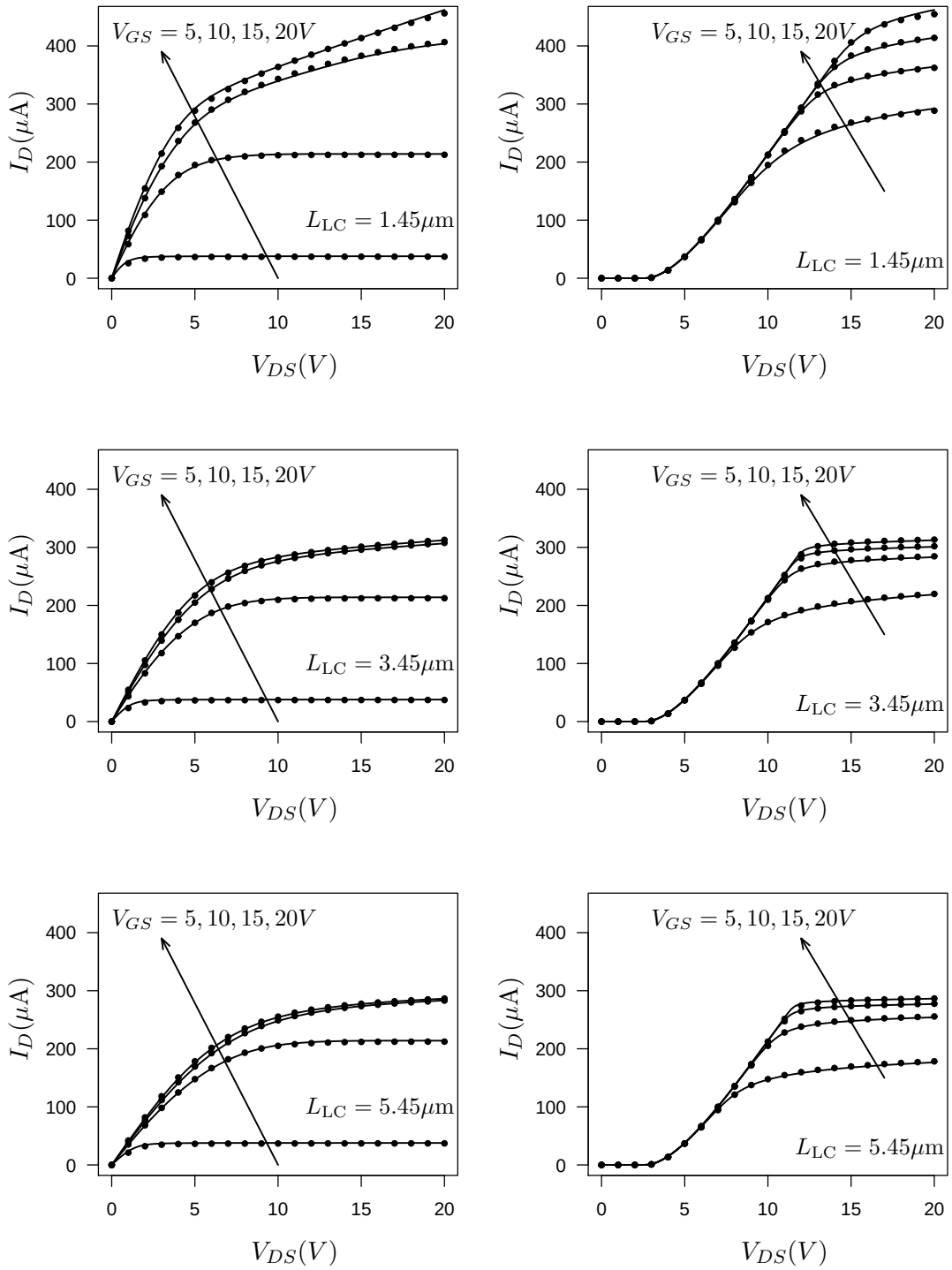


FIGURE 4.2: Comparison of $I_D - V_{GS}$ and $I_D - V_{DS}$ characteristics of an SOI-LDMOS using the proposed model (solid lines), for $L_{LC} = 1.45, 3.45$ and 5.45μm, with MEDICI data (symbols)

current flowing from a terminal can be expressed as

$$i_m = (g_{mn} + j\omega C_{mn})v_n, \tag{4.1}$$

where small signal voltage is applied at the terminal m and the current flowing from the terminal n is measured. The capacitance can now be extracted as

$$C_{mn} = (2\delta_{mn} - 1)\mathrm{Im}\left\{\frac{Y_{mn}}{2\pi f}\right\}, \tag{4.2}$$

where Y_{mn} is the conductance between terminal m and n, i.e., $Y_{mn} = i_m/v_n$. The chosen frequency for extracting the capacitances is 100MHz to ensure that the LDMOS transistor is operated well within the quasi-static regime.

Fig. 4.3, 4.4, 4.5 and 4.6 show the comparison of various capacitances obtained by the proposed model and MEDICI data.

Out of the four different kind of capacitance plots (C_{xG}, C_{xD}, C_{xS} and C_{xB}, $x \in D, G, S, B$), it C_{xG} gives the most useful insights into the LDMOS charge behavior. In C_{GG} curve, we observe that for negative values of V_{GS} and for large positive values of V_{GS}, the capacitance is constant. This is because, these two regions correspond to accumulation/inversion regions where charge variation is linear with V_{GS}. The peak and dips in the C_{GG} plot (or any other capacitance plots) corresponds to the transition from depletion to accumulation condition of the drift region under the gate oxide.

The accuracy of C_{GG} plot confirms the total gate charge estimation. On the other hand, to establish the charge partitioning scheme, we need to examine the C_{SG} and C_{DG} plots. For negative V_{GS}, we observe that both C_{SG} and C_{DG} go to zero. This is because the bulk terminal is responsible for the charge variations under negative bias and any variation in the gate bias has no effect on the drain or the source charges. For large values of V_{GS}, C_{DG} goes to zero, whereas C_{SG} reaches a finite value. The cause of this effect lies in the fact that in the high V_{GS} regime, the variation in the internal node voltages with the internal node voltage with V_{DS} is negligible. Since the drain current depends upon the voltage difference $V_{DD'}$, there is negligible variation in the drain current. Source charge on the other hand, is a fraction of of the inversion layer charge present in the channel region. Any

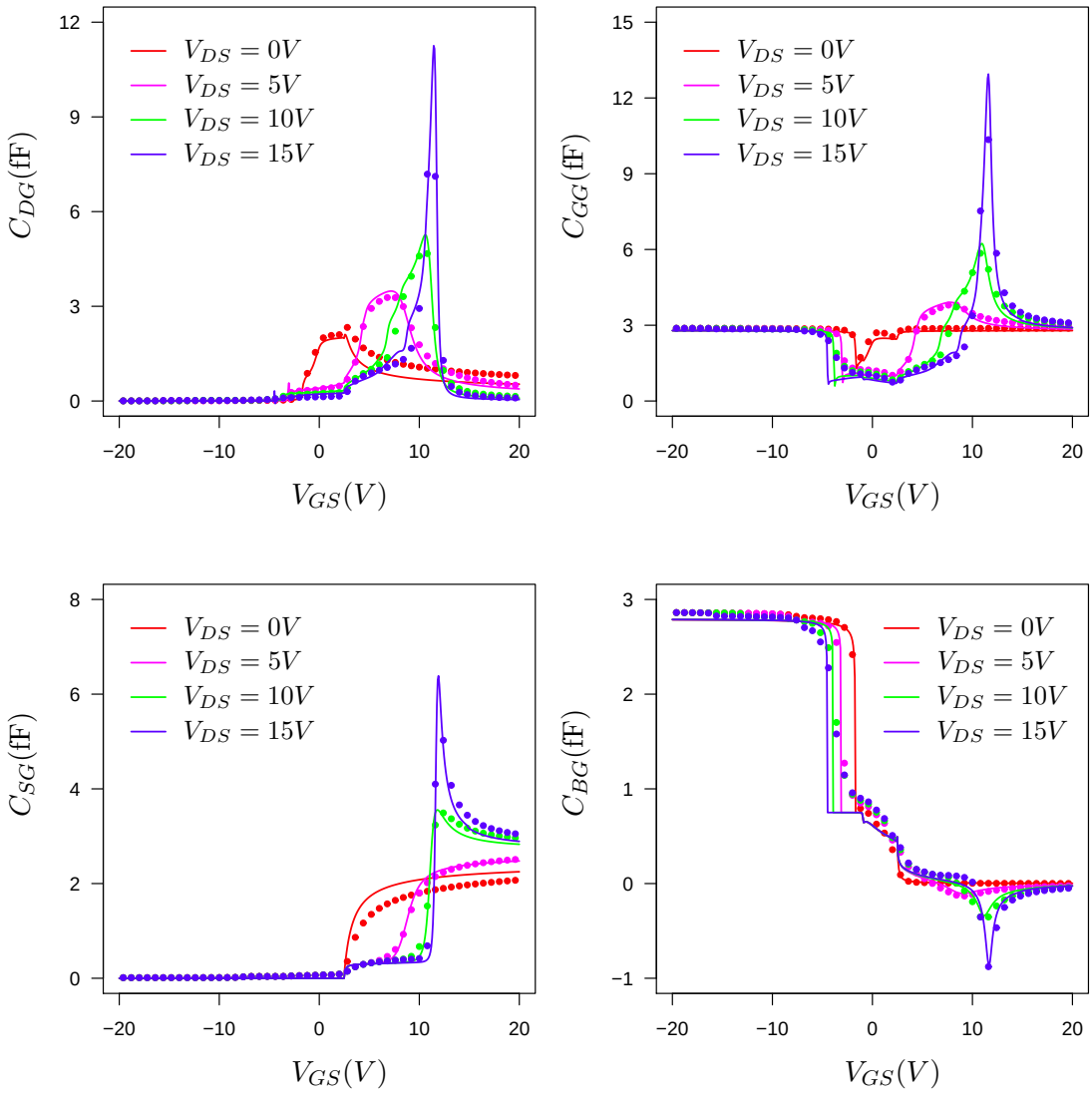


FIGURE 4.3: Comparison of $C_{xG} - V_{GS}$ $(x \in \{D, G, S, B\})$ plots obtained by using the proposed model (solid lines), for $V_{DS} = 0, 5, 10, 15V$, with MEDICI data (symbols).

variation in the gate voltage results in a linear change in the source charge which gives rise to a constant C_{SG} for higher values of V_{GS}.

The C_{BG} plot too gives us an insight into the charge behavior in an LDMOS transistor. For negative values of V_{GS}, the associated region-I accumulation charge and the region-II inversion charge is attributed to the bulk of the transistor. Since these charges vary linearly with the applied voltage, C_{BG} saturates to a positive value. Similarly, for large negative values of V_{GS}, C_{BG} goes to zero, as the bulk is not responsible for the electron inversion and accumulation charges. For moderate

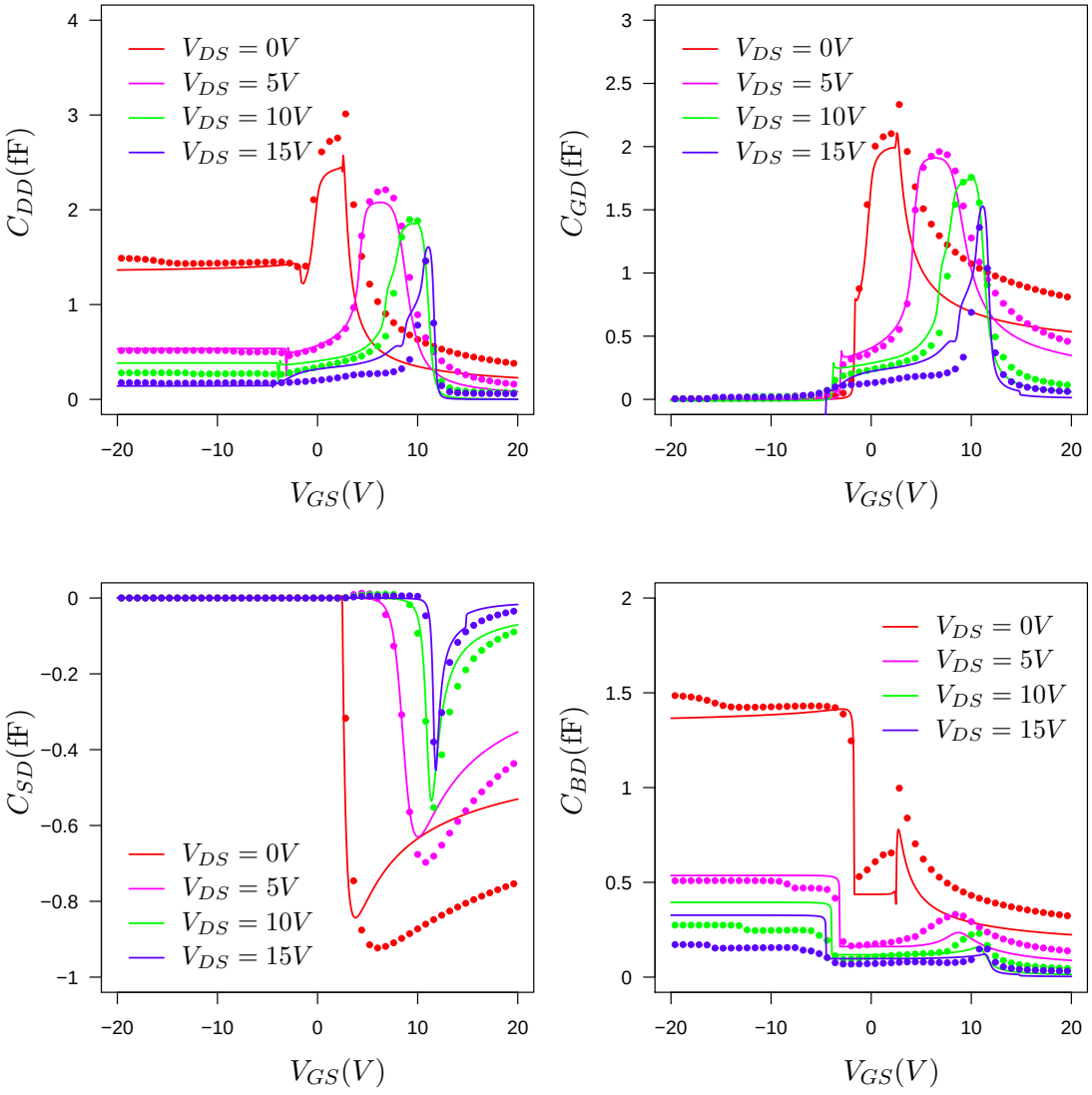


FIGURE 4.4: Comparison of $C_{xD} - V_{GS}$ ($x \in \{D, G, S, B\}$) plots obtained by using the proposed model (solid lines), for $V_{DS} = 0, 5, 10, 15V$, with MEDICI data (symbols).

values of V_{GS}, the C_{BG} shows a negative peak. This is attributed to the p-n junction charges present in the drain-bulk reverse-biased junction.

For showing the superiority of the proposed model over the MM20 way of partitioning the charge, a few important capacitance plots (namely C_{DG}, C_{SG}, C_{BG} and C_{DD}) have been plotted using the MM20 charge partitioning scheme (Fig. 4.7). It can be observed that there are notable inaccuracies in the capacitance plots obtained using the MM20 charge partitioning scheme, the reasons for which was discussed in Chapter 3.

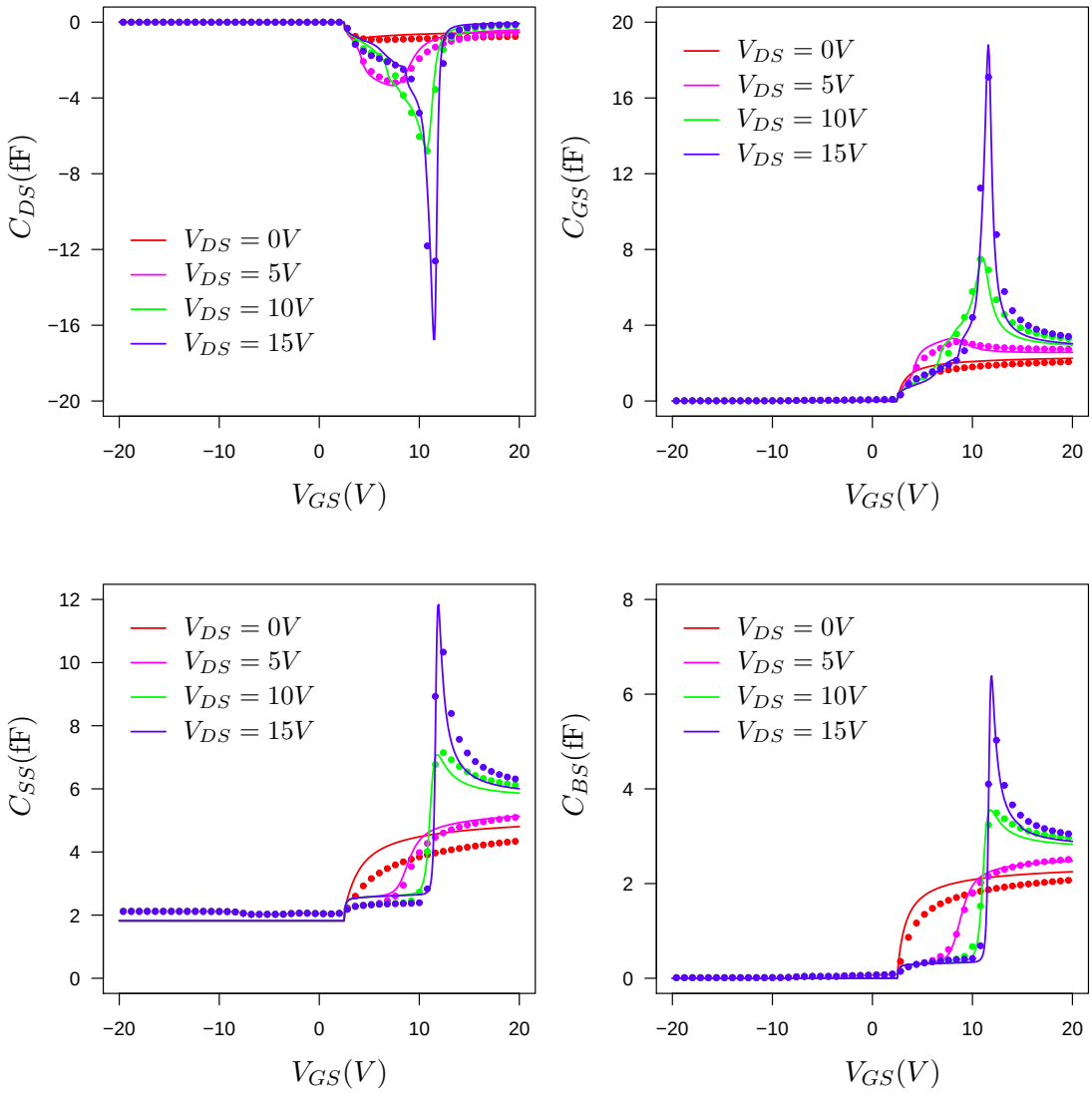


FIGURE 4.5: Comparison of $C_{xS} - V_{GS}$ ($x \in \{D, G, S, B\}$) plots obtained by using the proposed model (solid lines), for $V_{DS} = 0, 5, 10, 15V$, with MEDICI data (symbols).

Compared to a regular MOSFET, the capacitance plots of an LDMOS transistor shows a peaky behavior, and the maximum capacitance goes much beyond AC_{ox} (A is the total gate area). We analyze the reason for this peaky behavior in the C_{xG} plots. By using a similar argument, one can extend it to other capacitances as well. C_{xG} plots are obtained by exiting the gate terminal and measuring the changes in the charge at the x terminal. When a positive drain voltage is applied, a positive ac disturbance at the gate causes the internal node voltages to collapse. Hence, the channel sees a much larger V_{GC} change, and hence the amount of charge-change is amplified in the process. The amount of amplification depends

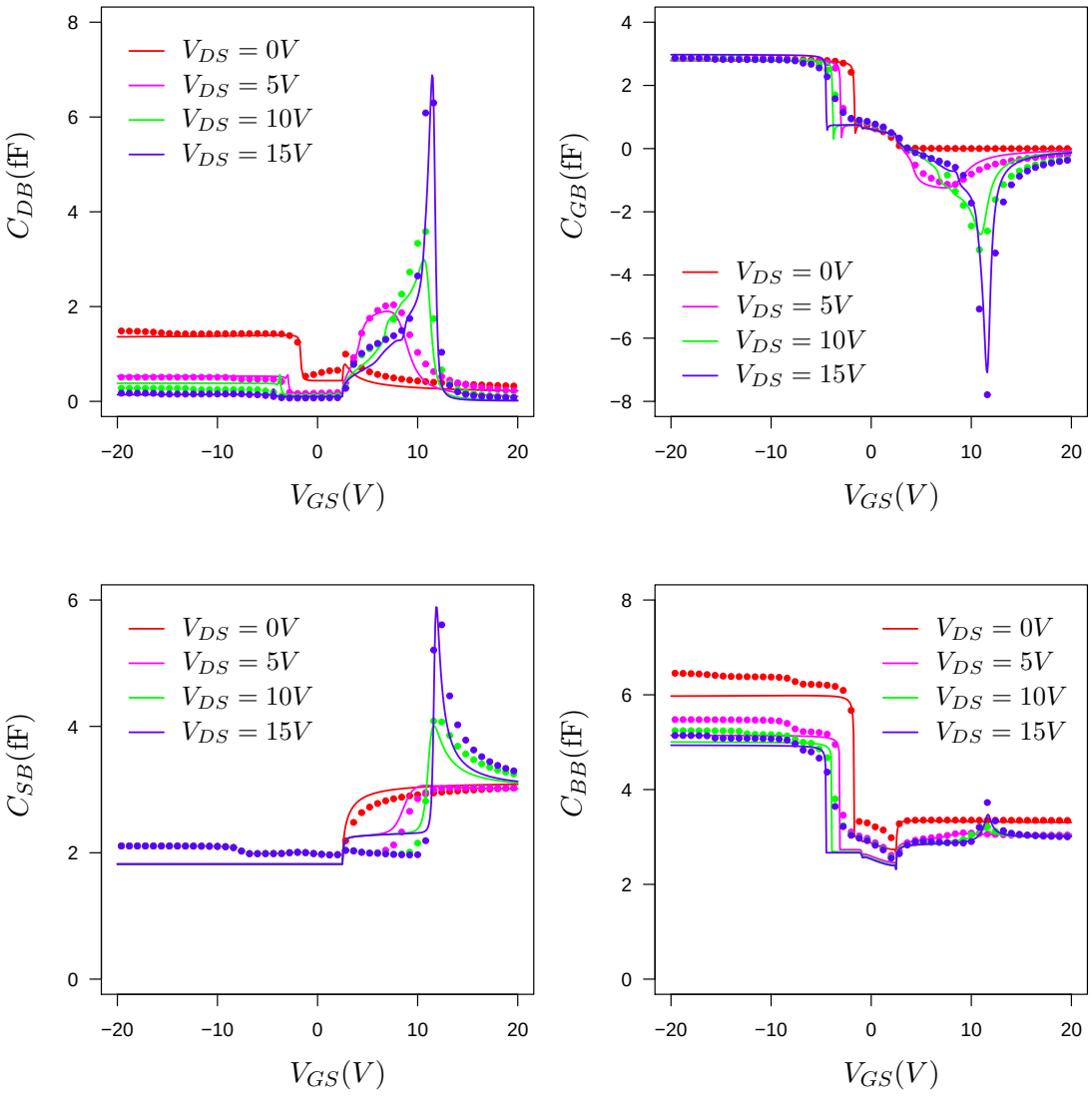


FIGURE 4.6: Comparison of $C_{xB} - V_{GS}$ ($x \in \{D, G, S, B\}$) plots obtained by using the proposed model (solid lines), for $V_{DS} = 0, 5, 10, 15V$, with MEDICI data (symbols).

on how fast V_{DS} changes with change in V_{GS}. For a very low and very high value of V_{GS}, the change is slow. Hence, the capacitances converge to around AC_{ox}. For an intermediate value of V_{GS}, the change is rapid; this gives rise to the peaks in the capacitance plots. It must be noted that there are no peaks for $V_{DS} = 0$ as there is no scope for the internal drain voltages to change under this bias. Hence, the maximum capacitance never exceeds AC_{ox}.

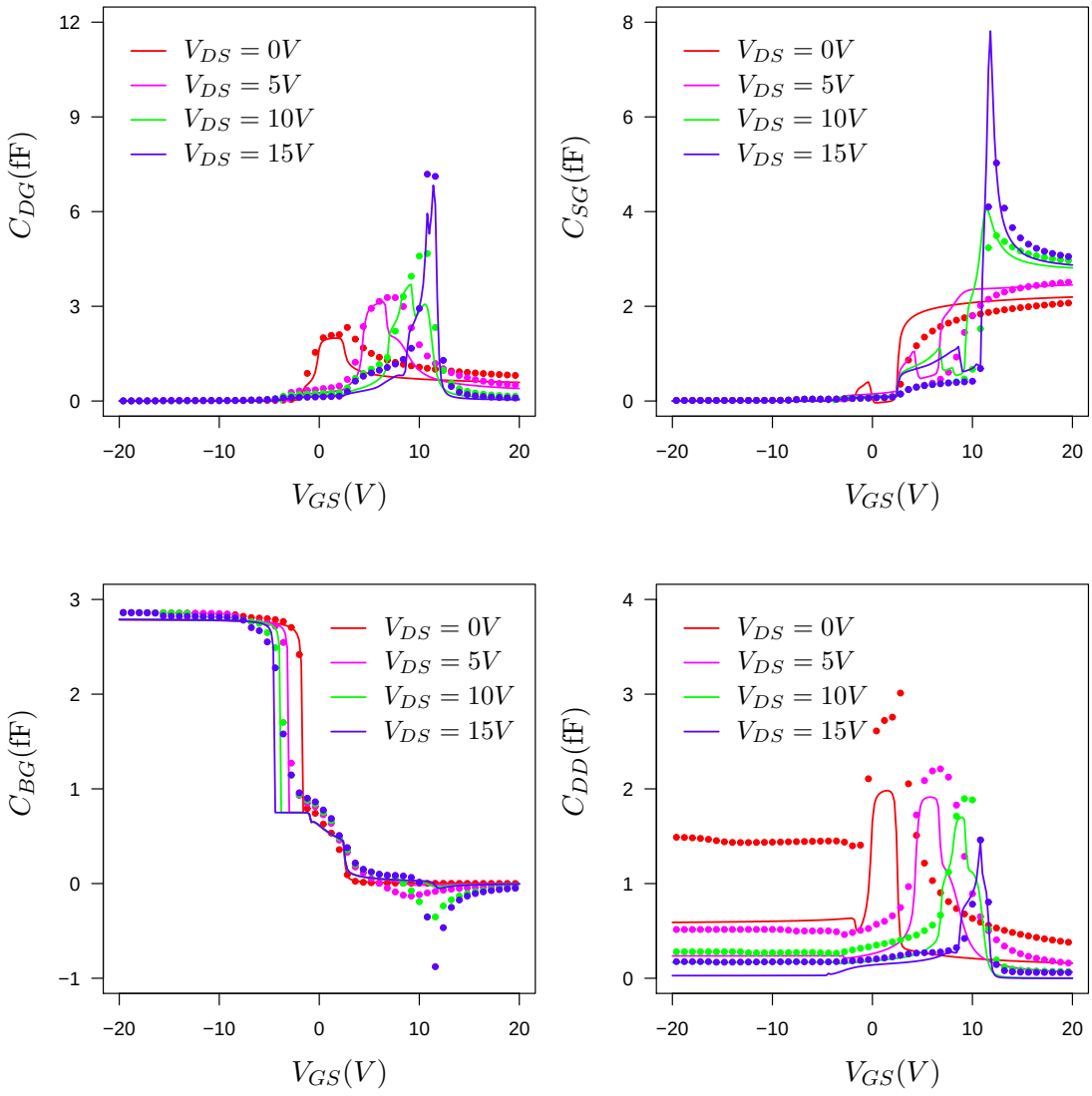


FIGURE 4.7: Comparison of a few Capacitance plots obtained using the MM20 charge partitioning scheme (solid lines), for $V_{DS} = 0, 5, 10, 15V$, with MEDICI data (symbols).

4.3 Transient Currents

To validate the claim that the conduction currents in region-I and region-II need not be identical at all points of time, a transient simulation was done in MEDICI and compared with the results obtained from the Verilog-A implementation of the proposed model. The drain voltage is held constant and the gate voltage is ramped up from 0 to 20V in time t_1 (rise time) and held constant for time t_2 as shown in 4.8

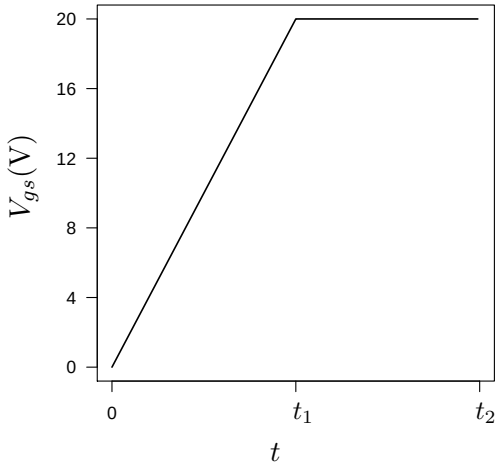


FIGURE 4.8: Input voltage profile at the gate terminal for transient simulations.

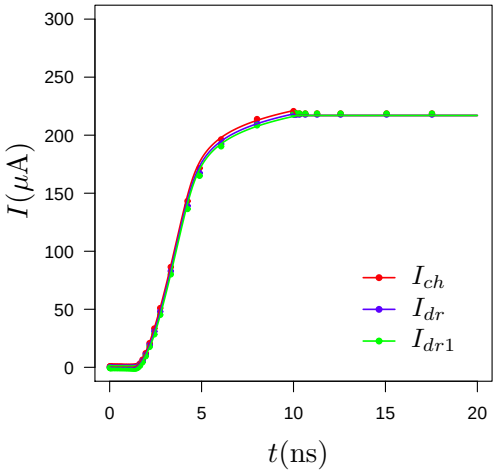
The conduction currents I_{ch}, I_{dr} and I_{dr1} are extracted from the transient simulations in MEDICI by considering the cross-section at the middle of region-I, II and III. The conduction current density in the considered cross-sections are integrated over the cross-section to obtain estimates of I_{ch}, I_{dr} and I_{dr1}.

It can be seen that I_{ch}, I_{dr} and I_{dr1} are all different during the rise and fall of the gate voltage. This is because region-I, II and III are electrostatically different. Any sudden rise in the voltage will result in unequal conduction currents flowing in region-I, II and III. Further, as the rise time of the ramp is varied, the difference between the three conduction currents increases. This can be seen in Fig. 4.9, 4.10 and 4.11.

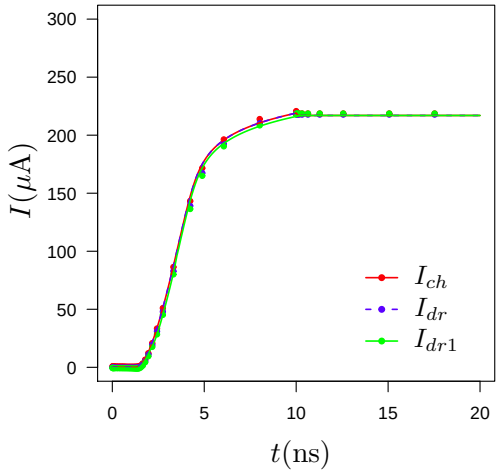
Due to the incorrect assumption made by the MM20 model (that $I_{ch} = I_{dr}$ at all times), even the terminal drain current (which follows I_{dr1}) is not tracked properly by the MM20 model.

4.4 Drawbacks of the model and reasons for inaccuracies

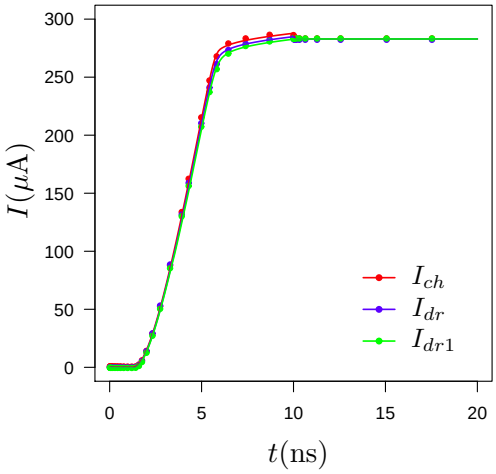
Although the model is fairly accurate in reproducing the AC, DC and transient characteristics of the SOI-LDMOS transistor, there is one major drawback of the model which manifests itself in several parts of the output characteristics, i.e.



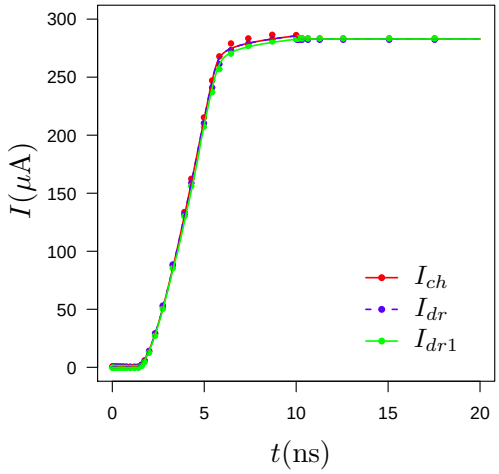
(A) Proposed model, $V_{DS} = 5$V



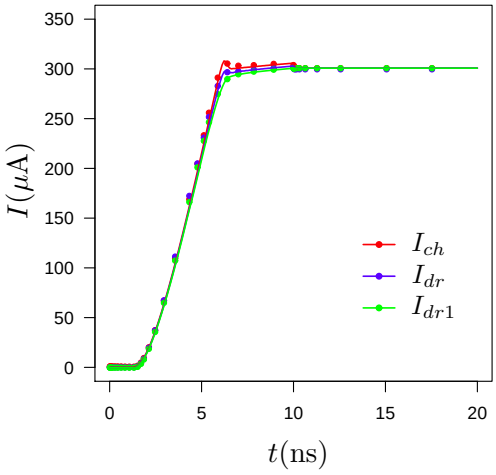
(B) MM20 model, $V_{DS} = 5$V



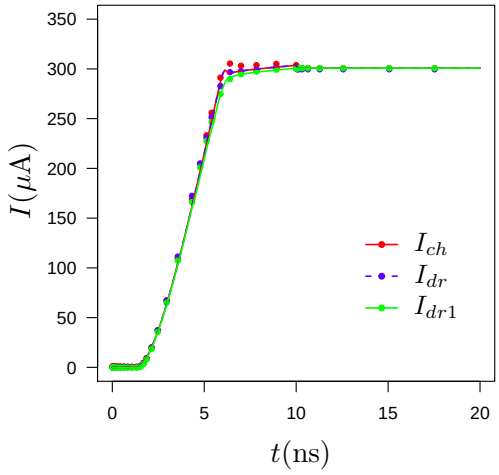
(C) Proposed model, $V_{DS} = 10$V



(D) MM20 model, $V_{DS} = 10$V

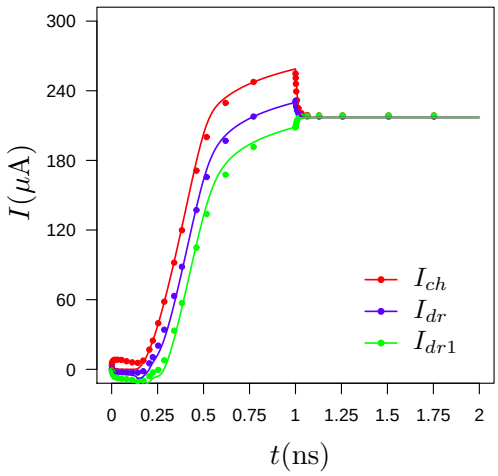


(E) Proposed model, $V_{DS} = 15$V

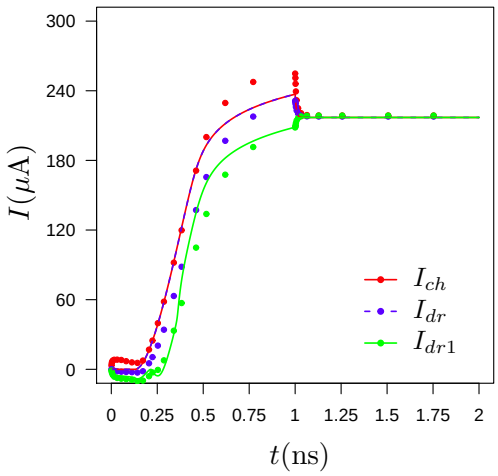


(F) MM20 model, $V_{DS} = 15$V

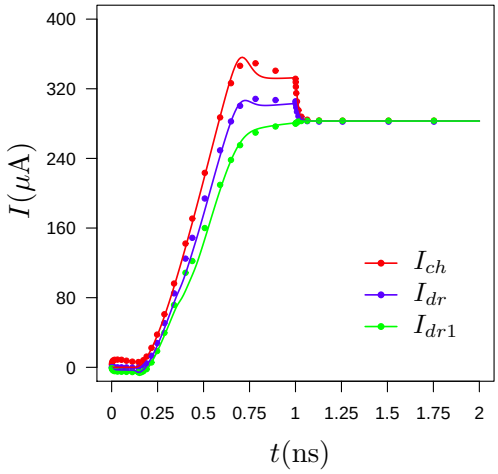
FIGURE 4.9: Response of I_{ch}, I_{dr} and I_{dr1} from the proposed model (left) and that of MM20 (right) when V_{GS} is ramped up at peak to peak rise time of 10ns. Solid lines represent model results and symbols represent MEDICI data.



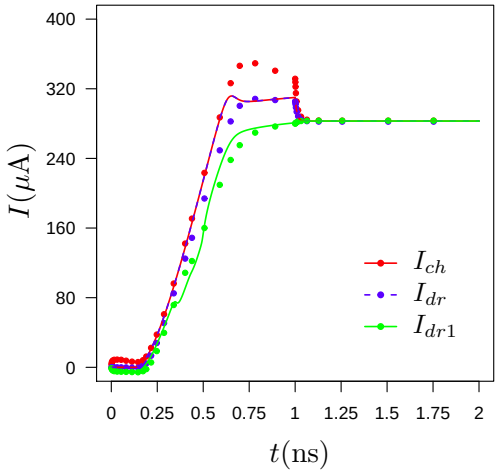
(A) Proposed model, $V_{DS} = 5$V



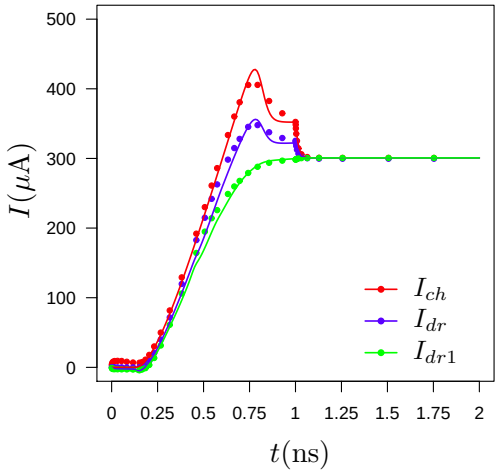
(B) MM20 model, $V_{DS} = 5$V



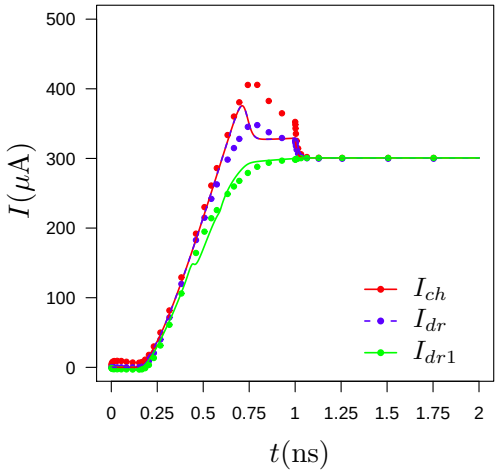
(C) Proposed model, $V_{DS} = 10$V



(D) MM20 model, $V_{DS} = 10$V

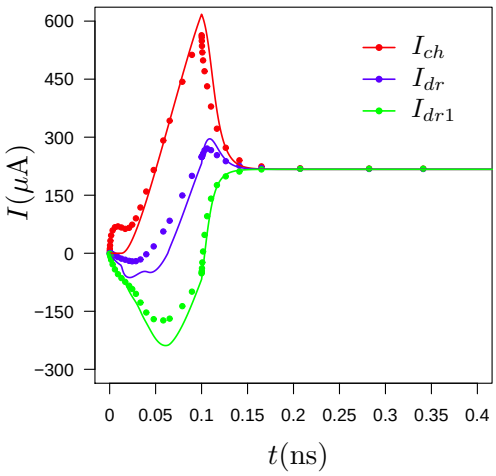


(E) Proposed model, $V_{DS} = 15$V

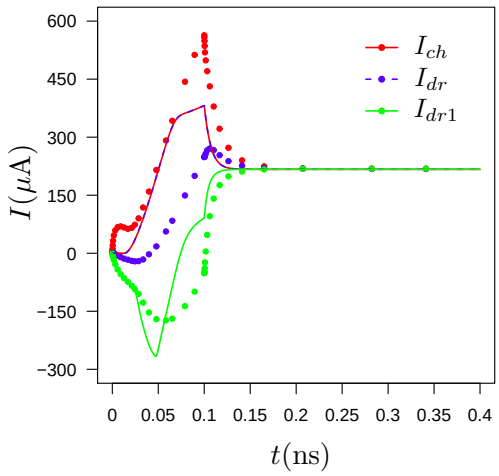


(F) MM20 model, $V_{DS} = 15$V

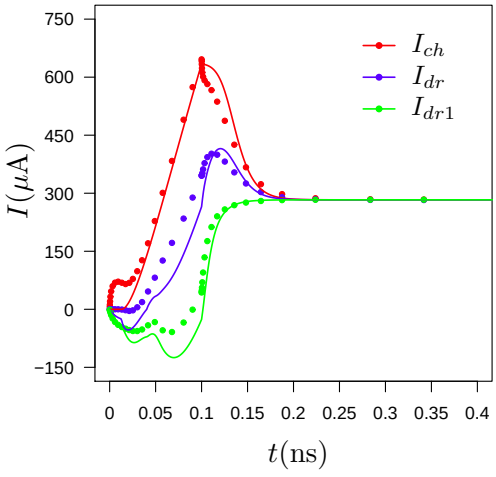
FIGURE 4.10: Response of I_{ch}, I_{dr} and I_{dr1} from the proposed model (left) and that of MM20 (right) when V_{GS} is ramped up at peak to peak rise time of 1ns. Solid lines represent model results and symbols represent MEDICI data.



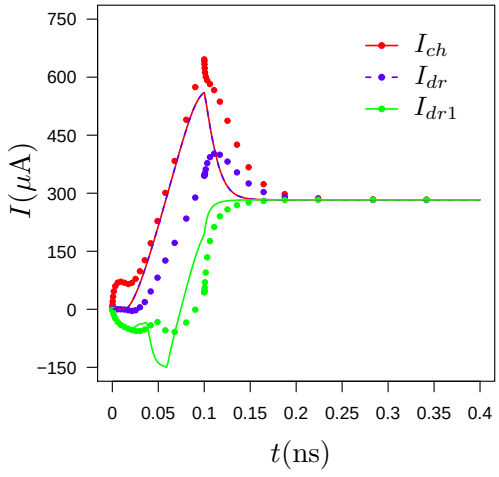
(A) Proposed model, $V_{DS} = 5$V



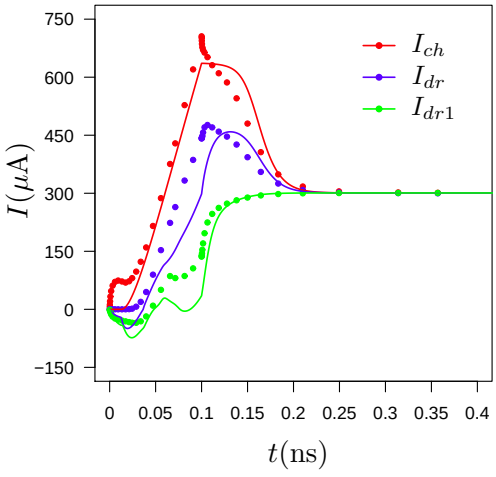
(B) MM20 model, $V_{DS} = 5$V



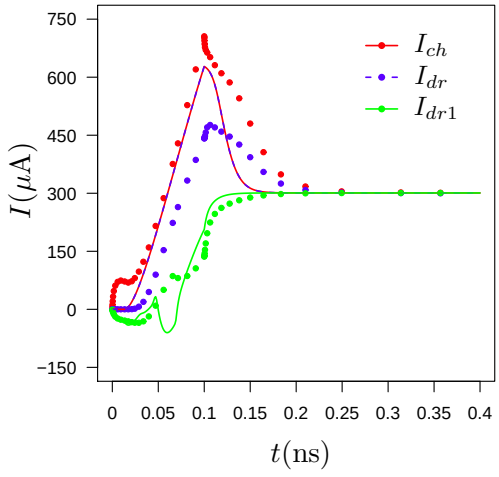
(C) Proposed model, $V_{DS} = 10$V



(D) MM20 model, $V_{DS} = 10$V



(E) Proposed model, $V_{DS} = 15$V



(F) MM20 model, $V_{DS} = 15$V

FIGURE 4.11: Response of I_{ch}, I_{dr} and I_{dr1} from the proposed model (left) and that of MM20 (right) when V_{GS} is ramped up at peak to peak rise time of 0.1ns. Solid lines represent model results and symbols represent MEDICI data.

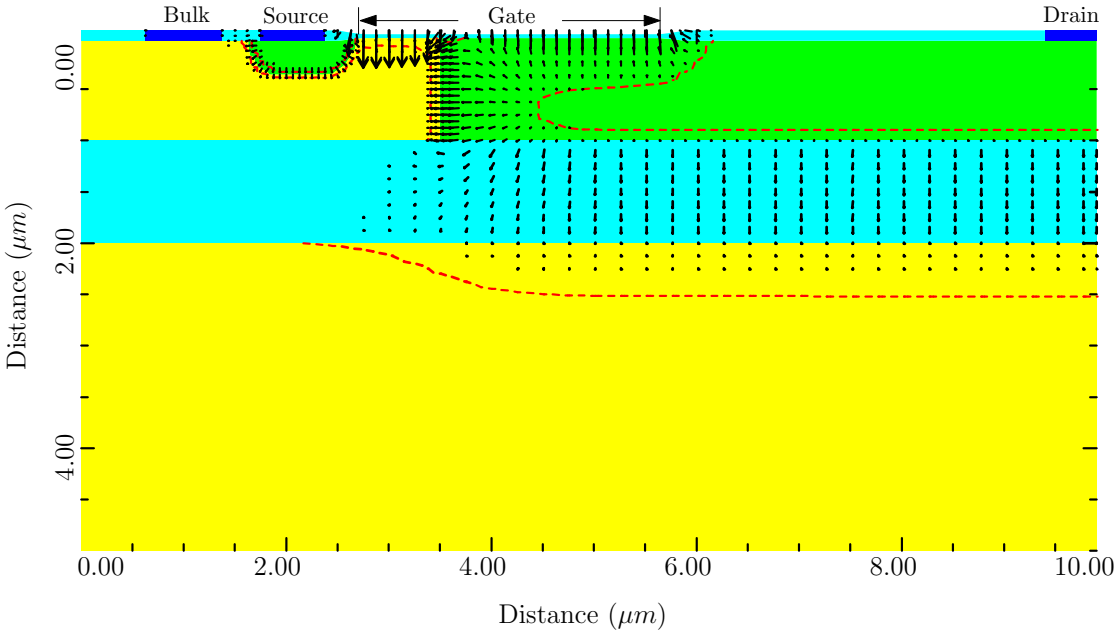


FIGURE 4.12: Electric Field lines for $V_{GS} = 4$V and $V_{DS} = 10$V.

modeling of region-II. The following points give an insight into why region-II needs to be modeled following a completely new approach.

1. **2-D current flow in region-II**

   As discussed in Chapter 1, the current flow in region-II is contributed by two different sources: flow of current through the bulk and flow of current through the surface (due to the presence of gate). A major assumption made in the analysis is that these two current sources are independent of each other, i.e., the current that flows along the surface continues to flow along the surface, and the bulk current flows only through the bulk. However, under certain bias conditions, the surface current can completely get redirected towards the bulk, before the surface current reaches the D' point. This is because of the complex nature of the 2-D electric field caused due to the presence of the gate and applied high voltage at the drain terminal. Hence, a simple 1-D analysis for region-II is insufficient in describing its behavior. This can be clearly seen by plotting the electric field profile along the cross-section of the LDMOS device (Fig. 4.12). 2-D Poisson equation needs to be solved in order to accurately determine the nature of region-II behavior under applied bias.

2. **Presence of p-n junction between region-I and II**

Apart from the vertical electrical field caused by the gate, the presence of the p-n junction enforces a horizontal electric field in region-II. This has adverse effects on the behavior of the LDMOS, that is not accurately captured in the model. Take for instance the capacitance plots. Specifically, the C_{BG} versus V_{GS} plots (Fig. 4.3). In the negative V_{GS} regime of operation, no current flows through the LDMOS transistor. Hence, the voltage at D' and D_i nodes estimated by the model are the same. Hence, as V_{GS} is reduced, the entire region-II enters accumulation mode together according to the model. This is seen as a sharp increase in C_{BG} in the capacitance plots below a certain gate voltage V_{GS}. However, as one can see from MEDICI data, the increase in C_{BG} with reduction in V_{GS} is much more gradual. This gradual increase in C_{BG} is caused due to the presence of the p-n junction. The depletion region caused by the presence of the p-n junction ensures that the quasi-Fermi levels are in a way that allows D_i side of region-II enters accumulation much earlier than the D' side as V_{GS} is reduced. This effect is present even in the C_{GG} and other capacitance plot. Since we have considered that the p-n junction is independent of the applied gate voltage and the region-II surface charge is unaffected by the p-n junction, there are inaccuracies in the capacitance plots.

3. **Bulk conduction in region-II**

   The bulk conduction in region-II is currently approximated by a constant conductance model, independent of the applied bias. Even if one does not include 2-D effects into region-II, one needs to make the bulk conductance bias dependent. This is because not the entire bulk of region-II participates in current conduction. Free carriers are removed from the p-n junction depletion region and the depletion region due to the application of the gate voltage.

4. **Non-physical value of region-II mobility**

   The value of mobility used to model region-II is $230\text{m}^2\text{V}^{-1}\text{s}^{-1}$, which is a highly skewed value from the nominal value of approximately $960\text{m}^2\text{V}^{-1}\text{s}^{-1}$. Currently, the unphysical value is compensating the incorrect modeling of region-II.

Chapter 5

Conclusions and Scope of Future Work

5.1 Findings of the thesis

In this work, the operation of the SOI-LDMOS transistor has been analyzed using results obtained from MEDICI simulations and a comprehensive physics based static and dynamic models to include static currents and capacitances has been proposed. The developed model has been implemented in Verilog-A.

The major contributions of the work are listed as following:

1. Corrections to region-I and II DC model has been incorporated to make the region-I of the model fully surface potential based and to incorporate bulk conduction in region-II.

2. A scalable two-dimensional DC quasi-saturation model has been proposed for the drift region under the field oxide. The proposed model is shown to be scalable in the region-III length for a wide range of values.

3. A comprehensive charge model has been proposed, taking into account all the charges present in the SOI-LDMOS. The device is separated into three regions and charges in each of these regions is analyzed separately.

4. The proposed AC and DC models have been implemented in Verilog-A and the results obtained from the model are compared with the MEDICI data. The comparison shows excellent match between the model and MEDICI data.

5. The major reason for imperfections in the capacitance plots was shown to be the inaccurate modeling of region-II using a 1-D approach.

5.2 Scope of Future Work

1. The model assumes uniform doping concentration in the channel region. In practice, the doping varies laterally from source to drain end. This effect must be included for an efficient model.

2. The drift region is modeled based on a 1D electrostatic assumption. Due to the presence of a reverse biased PN junction under the gate and due to the presence of bulk conduction in region-II, the current flow in region-II is 2-dimensional. One must solve a 2D Poisson equation in the drift region to exactly arrive at the drift region current. Further, a similar 2-D approach needs to be adopted for modeling the charges in this region.

3. Dynamic model to explain the non-quasi static behavior and a comprehensive noise model to model various noise sources in LDMOS are two major areas yet to be explored.

4. Work in the direction of device scalability with regards to region-I and II lengths and doping variations is yet to be carried out. Device scalability ensures that the model is applicable for various lengths of region-I, II and III.

Appendix A

Model Parameters and Constants

A.1 Model Parameter Values

Parameter	Description	Symbol	Value	Units
t_{ox}	Gate oxide thickness	TOX	38×10^{-9}	m
t_{si}	Silicon Film thickness above the BOX	TSI	1×10^{-6}	m
W	Width of the LDMOS transistor	W	1×10^{-6}	m
L_{ch}	Length of region I	LC	0.825×10^{-6}	m
L_{dr}	Length of region II	LD	2.25×10^{-6}	m
L_{dr1}	Length of region III	LLOCOS	3.45×10^{-6}	m
W_{src}	Source junction width	SJW	0.7×10^{-6}	m
D_{src}	Source junction depth	SJD	0.34×10^{-6}	m
$\mu_{0,ch}$	Region I low field mobility	UC	490×10^{-4}	$m^2V^{-1}s^{-1}$
$\mu_{0,dr}$	Region II low field mobility	UD	230×10^{-4}	$m^2V^{-1}s^{-1}$
μ_{dr1}	Region II low field mobility	UCR	960×10^{-4}	$m^2V^{-1}s^{-1}$
N_{ch}	p-doping in region I	NC	2×10^{23}	m^{-3}
N_{dr}, N_{dr1}	n-doping in region II and III	ND	2×10^{22}	m^{-3}

N_s	n-doping of the source junction	`NS`	2×10^{26}	m^{-3}
n_i	Intrinsic carrier concentration at room temperature	`NI`	1.5×10^{16}	m^{-3}
$V_{FB,ch}$	Flatband Voltage in region I	`VFB_I`	-0.95	V
$V_{FB,dr}$	Flatband Voltage in Region II	`VFBD_I`	-0.15	V
v_{sat}^{ch}	Velocity saturation in region-I	`VSAT_1`	1.035×10^5	ms^{-1}
v_{sat}^{dr}	Velocity saturation in region-II	`VSAT_2`	1.035×10^5	ms^{-1}
v_{sat}	Velocity saturation in region-III	`VSAT_3`	0.85×10^5	ms^{-1}
θ_1	Mobility correction due to vertical electric field, $x = 0$ correction	`THE1_I`	0.016	V^{-1}
θ_2	Mobility correction due to vertical electric field, channel variation correction	`THE2_I`	0.025	$V^{-1/2}$
λ_{ch}	Channel Length modification parameter	`LAMD_I`	0	V^{-1}
$\theta_{1,acc}$	Mobility correction due to vertical electric field, x = 0 correction	`THE1ACC_I`	0.04	V^{-1}
λ_{VD}	Parameter to account for drain voltage dependence of quasi-saturation current	`LAMD_VD`	7.5×10^{-14}	$V^{-1}m^2$

$\Delta L_{LC,VG}$	Parameter to account for gate voltage dependence of quasi-saturation current	DELLVG	6.5×10^{-9}	$V^{-1}m$
ΔL_{LC}	Parameter to take into account the effective region-III length	DELLLC	2×10^{-8}	m
θ_{dr1}	Velocity saturation smoothing parameter in region-III	THETAX	2.4	-
M_{exp}	Smoothing Parameter	MEXP	0.7	-
$M_{exp,d}$	Smoothing Parameter	MEXPD	3.0	-

A.2 Constants

Constant	**Description**	**Symbol**	**Value**	**Units**
q	Electronic Charge	P_ELECTRON	$1.60217657 \times 10^{-19}$	C
ϵ_{ox}	Permittivity of SiO_2	P_EPSOX	$3.45313325 \times 10^{-11}$	Fm^{-1}
ϵ_{si}	Permittivity of Si	P_EPSSI	$3.45313325 \times 10^{-10}$	Fm^{-1}
k	Boltzmann constant	P_BOLTZMANN	$1.3806488 \times 10^{-23}$	JK^{-1}

Appendix B

Source Codes

B.1 MEDICI SOI-LDMOS Source Code

B.1.1 Device Definition and Formalism

```
$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
COMMENT MESH DEFINTIONS
$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$

MESH   SMOOTH=1
X.MESH WIDTH=9.9 H1=0.125
Y.MESH N=1 L=-0.038
Y.MESH N=3 L=0.0
Y.MESH DEPTH=2.0 H1=0.125
Y.MESH DEPTH=3.0 H1=0.125
ELIMIN COLUMNS Y.MIN=1.1

$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
COMMENT REGION AND DOPING DEFINITIONS
$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$

SPREAD LEFT WIDTH=2.625 UP=1 LO=3 THICK=0.1 ENC=2
SPREAD RIGHT WIDTH=4.125 UP=1 LO=3 THICK=0.1 ENC=2
SPREAD LEFT WIDTH=100 UP=3 LO=4 Y.LO=0.125
REGION SILICON Y.MIN=0.0 Y.MAX=1.0 X.MIN=0 X.MAX=9.9
REGION OXIDE Y.MIN=1.0 Y.MAX=2.0 X.MIN=0 X.MAX=9.9
REGION SILICON Y.MIN=2.0 Y.MAX=5.0 X.MIN=0 X.MAX=9.9
REGION OXIDE IY.MAX=3
ELECTR NAME=Gate X.MIN=2.625 X.MAX=5.8 TOP
$ ELECTR NAME=Substrate BOTTOM
ELECTR NAME=Substrate X.MIN=0.6 X.MAX=1.5 IY.MAX=3
ELECTR NAME=Source X.MIN=1.7 X.MAX=2.5 IY.MAX=3
$ ELECTR NAME=Source X.MAX=2.5 X.MIN= 0.7 IY.MAX=3.0
```

```
29 ELECTR NAME=Drain X.MIN=9.3 IY.MAX=3.0
30
31 PROFILE N-TYPE N.PEAK=2.0E16 UNIFORM Y.MIN=0.0 Y.MAX=1.0 X.MIN= 3.5 X.MAX=9.9
       OUT.FILE=M1
32 PROFILE P-TYPE N.PEAK=2.0E17 UNIFORM Y.MIN=0.0 Y.MAX=1.0 X.MIN= 0.0 X.MAX=3.5
33 PROFILE P-TYPE N.PEAK=3E15 UNIFORM Y.MIN=2.0 Y.MAX=5.0 X.MIN= 0 X.MAX=9.9
34 COMMENT PROFILE P-TYPE N.PEAK=2E16 Y.CHAR=0.25
35 PROFILE N-TYPE N.PEAK=2E20 Y.JUNC=.34 X.MIN=1.9 WIDTH=0.5
36 +       XY.RAT=0.75
37 PROFILE P-TYPE N.PEAK=2E22 Y.JUNC=.34 X.MIN=0.75 WIDTH=0.5
38 +       XY.RAT=0.75
39 PROFILE N-TYPE N.PEAK=2E20 Y.JUNC=.34 X.MIN=9.4 WIDTH=0.5
40 +       XY.RAT=0.75
41
42 $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
43 COMMENT DOPING AND POTENTIAL REGRID
44 $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
45
46 REGRID DOPING LOG IGNORE=OXIDE RATIO=2 SMOOTH=1
47 +       IN.FILE=M1
48 $PLOT.2D GRID TITLE="DOPING REGRID" FILL SCALE
49 CONTACT NAME=Gate N.POLY
50
51 SYMB CARRIERS=0
52
53 METHOD ICCG DAMPED
54 SOLVE
55 REGRID POTEN IGNORE=OXIDE RATIO=0.2 MAX=1 SMOOTH=1
56 +       IN.FILE=M1
57 +       OUT.FILE=M2
58 $PLOT.2D GRID TITLE="POT REGRID" FILL SCALE
59 $+ DEVICE = POSTSCRIPT PLOT.OUT=ldmos-regrid.ps
60
61 SYMB CARRIERS=0
62 MODELS ANALYTIC FLDMOB CONSRH AUGER BGN PRPMOB
63 SOLVE OUT.FILE = M3
```

B.1.2 DC Analysis

```
1 $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
2 COMMENT DC ANALYSIS
3 $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
4
5 MESH IN.FILE=M2
6 LOAD IN.FILE=M3
7
8 SYMB NEWTON CARRIERS=2 ELECTRON HOLE
9 MODELS ANALYTIC FLDMOB CONSRH AUGER BGN PRPMOB
```

```
10 METHOD ICCG DAMPED
11
12 COMMENT Y CUT ANALYSIS
13
14 LOOP STEPS=21
15 ASSIGN NAME=ITER N.VALUE=0 DELTA=1
16 ASSIGN NAME=FILENAM1 C2="potential_cut_"@ITER"_20.ps"
17 ASSIGN NAME=FILENAM2 C2="potential_cut_"@ITER"_20.dat"
18 SOLVE V(Source)=0 V(Substrate)=0 V(Gate)=@ITER V(Drain)=20 OUT.FILE=M3
19 PLOT.1D QFN X.START=0 X.END=10.0 Y.START=0.06 Y.END=0.06  C.SIZE=1.0 COLOR=1
       TITLE="VOLTAGE CUT FERMIN"
20 + DEVICE=POSTSCRIPT PLOT.OUT=@FILENAM1
21 +^ORDER OUT.FILE=@FILENAM2
22 L.END
23
24 PLOT.1D ELE.VEL X.START=0 X.END=10.0 Y.START=0.06 Y.END=0.06  C.SIZE=1.0 COLOR=1
       TITLE="VOLTAGE CUT FERMIN"
25
26 PLOT.1D DOPING X.START=4.5 X.END=4.5 Y.START=0.0 Y.END=1.0 Y.LOG  BOT=1E10
       TOP=1E21 COLOR=2 TITLE=" IMPURITY PROFILE ALONG X DIRECTION"
27
28 PLOT.1D N.MOBILI X.STA=0.0 X.END=10.0 Y.STA=0.0 Y.END =0.0
29
30
31 COMMENT 2-D CONTOUR PLOTS
32
33 PLOT.2D DEPLETIO TITLE="E-FIELD DISTRIBUTION" FILL SCALE
34 VECTOR E.FIELD
35 + DEVICE=POSTSCRIPT PLOT.OUT=Depletion5_20.ps
36
37 PLOT.2D DEPL    SCALE FILL
38 +       TITLE="DEPLETION"
39
40
41 COMMENT ID-VDS CHARACTERISTICS
42
43 LOOP STEPS=5
44 ASSIGN NAME=ITER N.VALUE=0 DELTA=5
45 ASSIGN NAME=FILENAM1 C2="LDSOI1VG"@ITER"-Ids-Vds.ps"
46 ASSIGN NAME=FILENAM2 C2="LDSOI1VG"@ITER"-Ids-Vds.dat"
47 SOLVE V(Gate)=@ITER
48 LOG OUT.FILE=LDSOI1
49 SOLVE V(Drain)=0.0 ELEC=Drain VSTEP=0.1 NSTEP=200
50 PLOT.1D Y.AXIS=I(Drain) X.AXIS=V(Drain)
51 +POINTS COLOR=2 TITLE="Ids-Vds Characteristics, Vgs ="@ITER
52 +DEVICE=POSTSCRIPT PLOT.OUT=@FILENAM1
53 +^ORDER OUT.FILE=@FILENAM2
54 L.END
```

B.1.3 AC Analysis

```
$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
COMMENT AC ANALYSIS
$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$


MESH  IN.FILE=M2
LOAD  IN.FILE=M3
$ASSIGN NAME=ITER N.VALUE=6
$ASSIGN NAME=ITER1 C1=6
MODELS   ANALYTIC FLDMOB CONSRH AUGER BGN PRPMOB
SYMB  CARRIERS=0
METHOD  ICCG  DAMPED
SOLVE V(Source)=0.0
SOLVE V(Gate)=0.0
SOLVE V(Substrate)=0.0
SOLVE V(Drain)=0
COMMENT SOLVE V(Substrate1)=0.0
MODELS ANALYTIC FLDMOB CONSRH AUGER BGN PRPMOB
SYMB NEWTON CARRIERS=2

LOOP STEPS=1
ASSIGN NAME=ITER N.VALUE=0 DELTA=5
ASSIGN NAME=FILNAMDD C2="cdd-vds-vgs-"@ITER".dat"
ASSIGN NAME=FILNAMGD C2="cgd-vds-vgs-"@ITER".dat"
ASSIGN NAME=FILNAMSD C2="csd-vds-vgs-"@ITER".dat"
ASSIGN NAME=FILNAMBD C2="cbd-vds-vgs-"@ITER".dat"
ASSIGN NAME=FILNAMDG C2="cdg-vds-vgs-"@ITER".dat"
ASSIGN NAME=FILNAMGG C2="cgg-vds-vgs-"@ITER".dat"
ASSIGN NAME=FILNAMSG C2="csg-vds-vgs-"@ITER".dat"
ASSIGN NAME=FILNAMBG C2="cbg-vds-vgs-"@ITER".dat"
ASSIGN NAME=FILNAMDS C2="cds-vds-vgs-"@ITER".dat"
ASSIGN NAME=FILNAMGS C2="cgs-vds-vgs-"@ITER".dat"
ASSIGN NAME=FILNAMSS C2="css-vds-vgs-"@ITER".dat"
ASSIGN NAME=FILNAMBS C2="cbs-vds-vgs-"@ITER".dat"
ASSIGN NAME=FILNAMDB C2="cdb-vds-vgs-"@ITER".dat"
ASSIGN NAME=FILNAMGB C2="cgb-vds-vgs-"@ITER".dat"
ASSIGN NAME=FILNAMSB C2="csb-vds-vgs-"@ITER".dat"
ASSIGN NAME=FILNAMBB C2="cbb-vds-vgs-"@ITER".dat"

ASSIGN NAME=PSNAMDD C2="cdd-vds-vgs-"@ITER".ps"
ASSIGN NAME=PSNAMGD C2="cgd-vds-vgs-"@ITER".ps"
ASSIGN NAME=PSNAMSD C2="csd-vds-vgs-"@ITER".ps"
ASSIGN NAME=PSNAMBD C2="cbd-vds-vgs-"@ITER".ps"
ASSIGN NAME=PSNAMDG C2="cdg-vds-vgs-"@ITER".ps"
ASSIGN NAME=PSNAMGG C2="cgg-vds-vgs-"@ITER".ps"
ASSIGN NAME=PSNAMSG C2="csg-vds-vgs-"@ITER".ps"
ASSIGN NAME=PSNAMBG C2="cbg-vds-vgs-"@ITER".ps"
ASSIGN NAME=PSNAMDS C2="cds-vds-vgs-"@ITER".ps"
ASSIGN NAME=PSNAMGS C2="cgs-vds-vgs-"@ITER".ps"
ASSIGN NAME=PSNAMSS C2="css-vds-vgs-"@ITER".ps"
```

```
51 ASSIGN NAME=PSNAMBS C2="cbs-vds-vgs-"@ITER".ps"
52 ASSIGN NAME=PSNAMDB C2="cdb-vds-vgs-"@ITER".ps"
53 ASSIGN NAME=PSNAMGB C2="cgb-vds-vgs-"@ITER".ps"
54 ASSIGN NAME=PSNAMSB C2="csb-vds-vgs-"@ITER".ps"
55 ASSIGN NAME=PsNAMBB C2="cbb-vds-vgs-"@ITER".ps"
56
57
58 SOLVE V(Source)=0.0
59 SOLVE V(Gate)=@ITER
60 SOLVE V(Substrate)=0.0
61 SOLVE V(Drain)=0
62 SOLVE  ELEC=Drain VSTEP=0.4 NSTEP=50 AC.ANAL FREQ=1E8 VSS=0.1
       TERM="(Gate,Drain,Source,Substrate)"
63 $SOLVE ELEC=Gate VSTEP=0.2 NSTEP=200 AC.CHARG TERMINAL=Gate
64
65
66 PLOT.1D Y.AXIS="C(Drain,Drain)" X.AXIS=V(Drain) POINTS  COLOR=2
67 + DEVICE=POSTSCRIPT PLOT.OUT=@PSNAMDD
68 +^ORDER OUT.FILE=@FILNAMDD
69 PLOT.1D Y.AXIS="C(Gate,Drain)" X.AXIS=V(Drain)  POINTS  COLOR=2
70 + DEVICE=POSTSCRIPT PLOT.OUT=@PSNAMGD
71 +^ORDER OUT.FILE=@FILNAMGD
72 PLOT.1D Y.AXIS="C(Source,Drain)" X.AXIS=V(Drain)  POINTS  COLOR=2
73 + DEVICE=POSTSCRIPT PLOT.OUT=@PSNAMSD
74 +^ORDER OUT.FILE=@FILNAMSD
75 PLOT.1D Y.AXIS="C(Substrate,Drain)" X.AXIS=V(Drain) POINTS  COLOR=2
76 + DEVICE=POSTSCRIPT PLOT.OUT=@PSNAMBD
77 +^ORDER OUT.FILE=@FILNAMBD
78
79 PLOT.1D Y.AXIS="C(Drain,Gate)" X.AXIS=V(Drain)  POINTS  COLOR=2
80 + DEVICE=POSTSCRIPT PLOT.OUT=@PSNAMDG
81 +^ORDER OUT.FILE=@FILNAMDG
82 PLOT.1D Y.AXIS="C(Gate,Gate)" X.AXIS=V(Drain) POINTS  COLOR=2
83 + DEVICE=POSTSCRIPT PLOT.OUT=@PSNAMGG
84 +^ORDER OUT.FILE=@FILNAMGG
85 PLOT.1D Y.AXIS="C(Source,Gate)" X.AXIS=V(Drain) POINTS  COLOR=2
86 + DEVICE=POSTSCRIPT PLOT.OUT=@PSNAMSG
87 +^ORDER OUT.FILE=@FILNAMSG
88 PLOT.1D Y.AXIS="C(Substrate,Gate)" X.AXIS=V(Drain)  POINTS  COLOR=2
89 + DEVICE=POSTSCRIPT PLOT.OUT=@PSNAMBG
90 +^ORDER OUT.FILE=@FILNAMBG
91
92 PLOT.1D Y.AXIS="C(Drain,Source)" X.AXIS=V(Drain)  POINTS  COLOR=2
93 + DEVICE=POSTSCRIPT PLOT.OUT=@PSNAMDS
94 +^ORDER OUT.FILE=@FILNAMDS
95 PLOT.1D Y.AXIS="C(Gate,Source)" X.AXIS=V(Drain) POINTS  COLOR=2
96 + DEVICE=POSTSCRIPT PLOT.OUT=@PSNAMGS
97 +^ORDER OUT.FILE=@FILNAMGS
98 PLOT.1D Y.AXIS="C(Source,Source)" X.AXIS=V(Drain) POINTS  COLOR=2
99 + DEVICE=POSTSCRIPT PLOT.OUT=@PSNAMSS
100 +^ORDER OUT.FILE=@FILNAMSS
101 PLOT.1D Y.AXIS="C(Substrate,Source)" X.AXIS=V(Drain)  POINTS  COLOR=2
```

```
102 + DEVICE=POSTSCRIPT PLOT.OUT=@PSNAMBS
103 +^ORDER OUT.FILE=@FILNAMBS
104
105 PLOT.1D Y.AXIS="C(Drain,Substrate)" X.AXIS=V(Drain) POINTS  COLOR=2
106 + DEVICE=POSTSCRIPT PLOT.OUT=@PSNAMDB
107 +^ORDER OUT.FILE=@FILNAMDB
108 PLOT.1D Y.AXIS="C(Gate,Substrate)" X.AXIS=V(Drain)  POINTS  COLOR=2
109 + DEVICE=POSTSCRIPT PLOT.OUT=@PSNAMGB
110 +^ORDER OUT.FILE=@FILNAMGB
111 PLOT.1D Y.AXIS="C(Source,Substrate)" X.AXIS=V(Drain)  POINTS  COLOR=2
112 + DEVICE=POSTSCRIPT PLOT.OUT=@PSNAMSB
113 +^ORDER OUT.FILE=@FILNAMSB
114 PLOT.1D Y.AXIS="C(Substrate,Substrate)" X.AXIS=V(Drain) POINTS  COLOR=2
115 + DEVICE=POSTSCRIPT PLOT.OUT=@PSNAMBB
116 +^ORDER OUT.FILE=@FILNAMBB
```

B.1.4 Transient Analysis

```
1  $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
2  COMMENT TRANSIENT ANALYSIS
3  $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
4
5  MESH IN.FILE=M2
6  LOAD IN.FILE=M3
7
8  ASSIGN NAME=VDRAIN N.VALUE=5
9  ASSIGN NAME=RISETI N.VALUE=1E-10
10 ASSIGN NAME=VGSTIM C1="vgs_vs_time_d"@VDRAIN".dat"
11
12 SYMB NEWTON CARRIERS=2 ELECTRON HOLE
13 MODELS ANALYTIC FLDMOB CONSRH AUGER BGN PRPMOB
14 METHOD ICCG DAMPED
15
16 LOG OUT.FILE=TEST1
17 SOLVE   V(GATE)=0  V(DRAIN)=@VDRAIN
18 SOLVE V(Gate)=20 V(Drain)=@VDRAIN TSTEP=@RISETI*1E-3 RAMPTIME=@RISETI
       TSTOP=@RISETI        OUT.FILE=ISOL5D100
19 SOLVE V(Gate)=20 V(Drain)=@VDRAIN TSTEP=@RISETI*1E-3 TSTOP=@RISETI*4
       OUT.FILE=IISOL5D100
20
21 PLOT.1D IN.FILE=TEST1 X.AXIS=TIME Y.AXIS=V(GATE) COLOR=2  SYMB=2
22 + TITLE="TRANSIENT ANALYSIS" OUT.FILE=@VGSTIM
23
24 LOOP STEPS=21
25 ASSIGN NAME=ITER1 N.VALUE=100 DELTA=1
26 ASSIGN NAME=FILEI1 C1="ISOL5D"@ITER1
27 ASSIGN NAME=FILEI2 C2="Jconduc_"@FILEI1"_reg1_vgsramp_d"@VDRAIN".dat"
28 ASSIGN NAME=FILEI3 C2="Jconduc_"@FILEI1"_reg2_vgsramp_d"@VDRAIN".dat"
```

```
29 ASSIGN NAME=FILEI4 C2="Jconduc_"@FILEI1"_reg3_vgsramp_d"@VDRAIN".dat"
30 LOAD IN.FILE=@FILEI1
31 PLOT.1D J.CONDUC X.COMPONENT X.STA=3.1 X.END=3.1 Y.STA=0 Y.END=1 OUT.FILE=@FILEI2
32 PLOT.1D J.CONDUC X.COMPONENT X.STA=4.5 X.END=4.5 Y.STA=0 Y.END=1 OUT.FILE=@FILEI3
33 PLOT.1D J.CONDUC X.COMPONENT X.STA=8.0 X.END=8.0 Y.STA=0 Y.END=1 OUT.FILE=@FILEI4
34 L.END
35
36 LOOP STEPS=16
37 ASSIGN NAME=ITER1 N.VALUE=100 DELTA=1
38 ASSIGN NAME=FILEII1 C1="IISOL5D"@ITER1
39 ASSIGN NAME=FILEII2 C2="Jconduc_"@FILEII1"_reg1_vgsramp_d"@VDRAIN".dat"
40 ASSIGN NAME=FILEII3 C2="Jconduc_"@FILEII1"_reg2_vgsramp_d"@VDRAIN".dat"
41 ASSIGN NAME=FILEII4 C2="Jconduc_"@FILEII1"_reg3_vgsramp_d"@VDRAIN".dat"
42 LOAD IN.FILE=@FILEII1
43 PLOT.1D J.CONDUC X.COMPONENT X.STA=3.1 X.END=3.1 Y.STA=0 Y.END=1
       OUT.FILE=@FILEII2
44 PLOT.1D J.CONDUC X.COMPONENT X.STA=4.5 X.END=4.5 Y.STA=0 Y.END=1
       OUT.FILE=@FILEII3
45 PLOT.1D J.CONDUC X.COMPONENT X.STA=8.0 X.END=8.0 Y.STA=0 Y.END=1
       OUT.FILE=@FILEII4
46 L.END
```

B.2 2-D SOI-Resistor MEDICI Source

```
1  $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
2  COMMENT MESH DEFINTIONS
3  $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
4
5  ASSIGN NAME=LEN N.VALUE=3.45
6  ASSIGN NAME=TOTLEN N.VALUE=0.7+0.7+@LEN
7
8  ASSIGN NAME=TSI N.VALUE=1.0
9
10 MESH   SMOOTH=1
11 X.MESH WIDTH=@TOTLEN H1=0.125
12 Y.MESH N=1 L=-0.1
13 Y.MESH N=3 L=0.0
14 Y.MESH DEPTH=@TSI H1=0.125
15 Y.MESH DEPTH=5.0-@TSI H1=0.125
16 ELIMIN COLUMNS Y.MIN=1.1
17
18 $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
19 COMMENT REGION AND DOPING DEFINITIONS
20 $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
21
22 SPREAD LEFT WIDTH=0.7 UP=1 LO=3 THICK=0.1 ENC=2
23 SPREAD RIGHT WIDTH=0.7+@LEN UP=1 LO=3 THICK=0.1 ENC=2
```

```
24 $SPREAD LEFT WIDTH=100 UP=3 LO=4 Y.LO=0.125
25
26 REGION SILICON Y.MIN=0.0 Y.MAX=@TSI X.MIN=0 X.MAX=@TOTLEN
27 REGION OXIDE Y.MIN=@TSI Y.MAX=@TSI+1 X.MIN=0 X.MAX=@TOTLEN
28 REGION SILICON Y.MIN=@TSI+1 Y.MAX=5.0 X.MIN=0 X.MAX=@TOTLEN
29 REGION OXIDE IY.MAX=3
30
31 ELECTR NAME=Source X.MAX=0.6 IY.MAX=3.0
32 ELECTR NAME=Drain X.MIN=0.8+@LEN IY.MAX=3.0
33
34 PROFILE N-TYPE N.PEAK=2.0E16 UNIFORM Y.MIN=0.0 Y.MAX=@TSI X.MIN=0.0
       X.MAX=@TOTLEN OUT.FILE=M1
35 PROFILE P-TYPE N.PEAK=3E15 UNIFORM Y.MIN=@TSI+1 Y.MAX=5.0 X.MIN=0 X.MAX=@TOTLEN
36 PROFILE N-TYPE N.PEAK=2E20 Y.JUNC=0.34 X.MIN=0.0 WIDTH=0.7
37 +        XY.RAT=0.75
38 PROFILE N-TYPE N.PEAK=2E20 Y.JUNC=0.34 X.MIN=0.7+@LEN WIDTH=0.7
39 +        XY.RAT=0.75
40
41 $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
42 COMMENT DOPING AND POTENTIAL REGRID
43 $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
44
45 REGRID DOPING LOG IGNORE=OXIDE RATIO=2 SMOOTH=1
46 +        IN.FILE=M1
47 PLOT.2D GRID TITLE="DOPING REGRID" FILL SCALE
48 $CONTACT NAME=Gate N.POLY
49
50 SYMB CARRIERS=0
51
52 METHOD ICCG DAMPED
53 SOLVE
54 REGRID POTEN IGNORE=OXIDE RATIO=0.2 MAX=1 SMOOTH=1
55 +        IN.FILE=M1
56 +        OUT.FILE=M2
57 PLOT.2D GRID TITLE="POT REGRID" FILL SCALE
58 $+ DEVICE = POSTSCRIPT PLOT.OUT=ldmos-regrid.ps
59
60 SYMB CARRIERS=0
61 MODELS ANALYTIC FLDMOB CONSRH AUGER BGN PRPMOB
62 SOLVE OUT.FILE = M3
63
64 MESH IN.FILE=M2
65 LOAD IN.FILE=M3
66
67 SYMB NEWTON CARRIERS=2 ELECTRON HOLE
68 MODELS ANALYTIC FLDMOB CONSRH AUGER BGN PRPMOB
69 METHOD ICCG DAMPED
70
71 $LOG OUT.FILE=LDSOI1
72 $SOLVE V(Drain)=0 ELEC=Drain VSTEP=0.1 NSTEP=200
73 $PLOT.1D Y.AXIS=I(Drain) X.AXIS=V(Drain)
74 $+POINTS COLOR=2 TITLE="Id-Vd Characteristics"
```

```
$+DEVICE=POSTSCRIPT PLOT.OUT="Length3_45.ps"
$+^ORDER OUT.FILE="Length3_45.dat"

LOOP STEPS=41
ASSIGN NAME=ITER N.VALUE=0 DELTA=0.5
ASSIGN NAME=FILENAM C2="Length3_45_"@ITER"_quarter.dat"
SOLVE V(Source)=0 V(Drain)=@ITER OUT.FILE=M3
PLOT.1D NET.CARR X.START=0.7+0.6 X.END=0.7+0.6 Y.START=0 Y.END=1 TITLE="Net
    Carrier concentration"
+DEVICE=POSTSCRIPT PLOT.OUT="Length3_45.ps"
+^ORDER OUT.FILE=@FILENAM
L.END

$PLOT.1D DOPING INTERFAC IX.MIN=0.0 IX.MAX=@TOTLEN IY.MIN=0.0 IY.MAX=0.1
    C.SIZE=1.0 COLOR=1 TITLE="Doping profile" Y.LOGARI
```

B.3 Verilog-A Source Code

```
// LDMOS Version_5: Verilog-A Description

// ********************************************************************************
// Last Edit: 05 June 2014
// Default simulator: Cadence Virtuoso Spectre
// ********************************************************************************

`include "discipline.h"
`define LocalModel

module test(d, g, s, b);
    // ********************************************************************************
    //               CONSTANT DEFINTIONS
    // ********************************************************************************

    `define GMIN             5E-16
    `define GMIN1            5E-16
    `define EPS1             2.0E-2
    `define EPS2             1.0E-2
    `define EPS3             4.0E-2
    `define EPS4             1.0E-1
    `define EPS5             1.0E-4
    `define EPS6             1.0E-5
    `define EPS7             1.0E-1
    `define EPS8             3.0E-2
    `define EPS9             1E-20
    `define LN_MINDOUBLE    -800

    //Physical Constants
```

```
30    `define P_ELECTRON      1.60217657E-19      // Electronic Charge
      Unit: C
31    `define P_EPSOX         3.45313325E-11      // Permittivity of SiO2
      Unit: F/m
32    `define P_EPSSI         1.03416914E-10      // Permittivity of silicon
      Unit: F/m
33    `define P_BOLTZMANN     1.3806488E-23       // Boltzmann constant
      Unit: J/K
34    `define P_KELVIN_CONV   273.15              // Offset for conversion from
      Celcius to Kelvin scale Unit: K
35
36    // ********************************************************************
37    //              NODE DEFINITIONS
38    // ********************************************************************
39
40    inout      d, g, s, b;
41    electrical d, g, s, b;
42    electrical di,d1;
43
44    // ********************************************************************
45    //              PARAMETER INITIALISATION
46    // ********************************************************************
47
48    `ifdef LocalModel
49
50        // Operating conditions
51        parameter real TA       = 27;           // Ambient Temperature of
      Operation (Celcius)
52
53        // Device Dimensions
54        parameter real TOX      = 38e-9;        // Gate oxide thickness (m)
55        parameter real TSI      = 1e-6;         // Silicon Film thickness above
      the BOX Layer (m)
56        parameter real W        = 1e-6;         // Width of the LDMOS (m)
57        parameter real LC       = 0.825e-6;     // Length of Region I (m)
58        parameter real LD       = 2.25e-6;      // Length of Region II (m)
59        parameter real LLOCOS   = 3.45e-6;      // Length of LOCOS oxide layer
      and Region III (m)
60        parameter real DELLLC   = 0.02e-6;      // Parameter to take into
      account the effective region-III length (m)
61        parameter real SJW      = 0.7e-6;       // Source junction width (m)
62        parameter real SJD      = 0.34e-6;      // Source junction depth (m)
63
64        // Mobility
65        parameter real UC       = 490e-4;       // Region I Mobility (m^2/Vs)
66        parameter real UD       = 230e-4;       // Region II Mobility (m^2/Vs)
67        parameter real UDR      = 960e-4;       // Region III Mobility (m^2/Vs)
68
69        // Doping
70        parameter real NC       = 2e23;         // P doping in Region I (/m^3)
71        parameter real ND       = 2e22;         // N doping in Region II (/m^3)
```

```
72          parameter real NS       = 2e26;         // Source doping concentration
    (/m^3)
73          parameter real NI       = 1.5E16;       // Intrinsic carrier
    concentration in silicon at Room Temperature (/m^3)
74
75          // Surface Potentials
76          parameter real VFB_I    = -0.95;        // Flatband Voltage in Region I
    (V)
77          parameter real VFBD_I   = -0.15;        // Flatband Voltage in Region II
    (V)
78
79          // Other Region-I parameters
80          parameter real VSAT_1   = 1.035e5;      // Velocity saturation in
    Region-I
81          parameter real THE1_I   = 0.016;        // Mobility correction due to
    vertical electric field, x = 0 correction (V^-1)
82          parameter real THE2_I   = 0.025;        // Mobility correction due to
    vertical electric field, channel variation correction (V^-0.5)
83          parameter real LAMD_I   = 0;            // Channel Length modification
    parameter (V^-1)
84          parameter real M0       = 0;            // Parameter for the
    short-channel subthreshold slope
85          parameter real MEXP     = 0.7;          // Smoothing parameter from
    linear to saturation regime
86
87          // Other Region-II parameters
88          parameter real VSAT_2   = 1.035e5;      // Velocity saturation in
    Region-I (m/s)
89          parameter real THE1ACC_I= 0.04;         // Mobility correction due to
    vertical electric field, x = 0 correction (V^-1)
90          parameter real MEXPD    = 3.0;          // Smoothing parameter from
    linear to quasi-saturation regime
91
92          //Other Region-III parameters
93          parameter real THETAX   = 2.4;          // Velocity saturation smoothing
    parameter in region-III
94          parameter real LAMD_VD  = 7.5E-14;      // Parameter to account for
    drain voltage dependence of the quasi saturation current (m^2/V)
95          parameter real VSAT_3   = 0.85E5;       // Saturation velocity of
    electrons (m/s)
96          parameter real DELLVG   = 6.5e-9;       // Parameter to account for gate
    voltage dependence of the quasi saturation current (m/V)
97
98          //SECONDARY PARAMETERS
99          parameter real THE3_1   = UC/(VSAT_1*LC);
100         parameter real THE3D    = UD/(VSAT_2*LD);
101         parameter real LAMD_VG  = DELLVG/(LLOCOS-DELLLC);
102         parameter real Cox      = `P_EPSOX/TOX;
    // Gate Oxide Capacitance per unit area
103         parameter real ko_id    = sqrt(2*`P_EPSSI*`P_ELECTRON*NC)*TOX/`P_EPSOX;
    // Body effect parameter in region-I
```

```
104         parameter real kod_id    = sqrt(2*`P_EPSSI*`P_ELECTRON*ND)*TOX/`P_EPSOX;
    // Body effect parameter in region-II and III
105
106         parameter real phiT      = `P_BOLTZMANN*(TA+`P_KELVIN_CONV)/`P_ELECTRON;
    // Thermal Voltage (V)
107         parameter real phib_id   = 2*phiT*ln(NC/NI);
108         parameter real phibd_id  = 2*phiT*ln(ND/NI);
109
110         parameter real rd_id     = LD/(W*UD*`P_ELECTRON*ND*TSI);
111
112         parameter real bet_id    = UC*`P_EPSOX*W/(TOX*LC);
113         parameter real betacc_id= UD*`P_EPSOX*W/(TOX*LD);
114
115     `else
116
117     `endif
118
119     real Vlimit;
120     real Vds, Vgs, Vsb, Vds2, Vgdi, Vdis, Vd1s, Vdib, Vd1b, Vddi, Vgb, Vdd1;
121     real absd, hyp_a, hyp_b, hyp_c, hyp_d, hyp_x;
122     real absx, absy, iabs, hypm_q, hypm_t, hypm_tm, hypm_it;
123     real x, y;
124     real phio, ko_2, ko2_4, kod_2, kod2_4, i16phph, Acci, Accd;
125     real Vgb_t, Vsb_t, Vds1, Vgs_t, Vgd_t, Vinv0_v, delta_v, ksi_v, Vsb_t0;
126     real Vdep0_v, Vdep00_v, Fmob_v, Voxp, Fmobacc;
127     real Vdis_eff, Vgdi_t, Vgdi_t_eff, Vdib_t, hypmarg, Vq_dr_eff, Vddi_eff,
    rd_i;
128     real Vddi_sat, Vdis_sat_v;
129     real ko_i, kod_i, betacc_i, bet_i, phib_i, phibd_i;
130     real psi_s00, Vdibt_eff, Vgb_eff;
131     real Idrift, Ich, Idr;
132     real psis, psid, delta_psi_s, psis_acc, psisd, psisaccd, psisdi, psisaccdi,
    psi_satdi, psi_satd, psi_sat;
133     real Vq_dr_di, Vq_dr_dig, Vq_dr_d1, Vq_dr_del, Vq_dr_delg, Vq_dr_avg,
    Vq_dr_avgg, Fdr, Q_dr_di, zeta;
134     real Qgchmos, Qdchmos, Qschmos, Qbchmos, Q_gch, Q_bch, Q_dch, Q_sch, Qgch,
    Qgdr, Qddrmos, Qsdrmos;
135     real Fact1, Fact2, Qs, Qd, VinvL, vgtdel, vgtavg, Fch, Igtran, Iditran,
    Id1tran, Istran;
136     real QQg, QQd1, QQdi, QQs;
137     real delacc, delaccdi, delaccd, Vdig_eff, V_oxdidr, V_depdi, V_invdi,
    V_qaccdepdi, V_qdrdi, V_qdrdieff, V_ddisat, V_ddieff;
138     real V_gdteff, V_dsdreff, V_dgeff, V_dbt, V_oxddr, V_invd, V_depd,
    V_qaccdepd, V_qdrd, V_qdrdeff;
139     real V_qdrdeffavg, delV_qaccdep, F_jdr, Q_daccdep, Q_saccdep, V_Tt,
    V_gdilim, V_gdlim, V_gdacclim, V_gdiacclim, delV_acclim, V_acclimavg,
    F_jacclim, Q_sacclim;
140     real Q_dmm20, Q_gmm20, Q_smm20, Q_bmm20, Q_ddr, Q_gdr, Q_sdr, Q_bdr,
    Idtranmm20, Igtranmm20, Istranmm20;
141     real Leff, Eeff, Ec;
142     real V_bi, V_bis, Qpnns, Qpnn;
143
```

```
144     //---------- smoothing functions--------------
145
146     analog function real hyp;
147         input x, eps;
148         real  x, eps;
149         begin
150             hyp = 0.5*(x+sqrt(x*x+4*eps*eps));
151         end
152     endfunction
153
154
155     analog function real hypm;
156     //The hypm function just implements this:
157     //hypm = x*y/pow((pow(x,2*m)+pow(y,2*m)), 1/(2*m));
158         input x, y, m;
159         real x, y, m;
160         real absx, absy, hypm_q, hypm_t, hypm_tm;
161         begin
162             if (x == 0.0 && y == 0.0) begin
163                 hypm = 0.0;
164             end else begin
165                 absx = (x>=0.0) ? x : -x;
166                 absy = (y>=0.0) ? y : -y;
167                 if (absx > absy) begin
168                     hypm_q  = absy/absx;
169                     hypm_t  = pow(hypm_q, 2.0*m);
170                     hypm_tm = pow(1.0 + hypm_t, 0.5 / m);
171                     hypm    = (x/absx) * (y/hypm_tm);
172                 end else begin
173                     hypm_q  = absx/absy;
174                     hypm_t  = pow(hypm_q, 2.0*m);
175                     hypm_tm = pow(1.0 + hypm_t, 0.5 / m);
176                     hypm    = (y/absy) * (x/hypm_tm);
177                 end
178             end
179         end
180     endfunction
181
182     analog function real PSISAT;
183             input vgbeff, del, k0;
184             real vgbeff, del, k0;
185             begin
186                 PSISAT =
    pow((vgbeff+del)/(k0/2+sqrt(vgbeff+del+pow(k0/2,2))),2)-del;
187             end
188     endfunction
189
190     analog function real PSIS; //MM20 version of calculating surface potential
    (inversion)
191         input vgbeff, psisat, delacc, vcbt, k, m0;
192         real vgbeff, psisat, delacc, vcbt, k, m0;
193         real f1, f2, f3;
```

```
194         begin
195             f1      = psisat - hyp(psisat-vcbt,'EPS1);
196             f2      = f1 - (psisat-f1)/sqrt(1+pow(psisat-f1,2)/(16*phiT*phiT));
197             f3      = vgbeff - f2;
198             PSIS    = f1 + phiT*(1+m0)*ln(1+((pow(f3/k,2)-f1-delacc)/phiT));
199         end
200     endfunction
201
202     analog function real PSISACC; //MM20 version of calculating surface
    potential (accumulation)
203         input vgbt, vgbeff, k, Acci;
204         real vgbt, vgbeff, k, Acci;
205         real f1, f2, f3;
206         begin
207             f1      = Acci*(vgbt-vgbeff);
208             f2      = f1/sqrt(1+(f1*f1)/(16*phiT*phiT));
209             f3      = vgbt - vgbeff - f2;
210             PSISACC = - phiT*ln(1+((pow(f3/k,2)-f2)/phiT));
211         end
212     endfunction
213
214     analog function real VINVEX;
215         input psi_s, del, vcbt, k, m;
216         real psi_s, del, vcbt, k, m;
217         real nr, dr;
218         begin
219             nr      = k * (phiT*exp((psi_s-vcbt)/((1+m)*phiT)));
220             dr      = hyp(psi_s+del, 'EPS8) +
    phiT*exp((psi_s-vcbt)/((1+m)*phiT)) + sqrt(hyp(psi_s+del,'EPS8));
221             VINVEX  = nr/sqrt(dr);
222         end
223     endfunction
224
225     analog function real delpsieps;
226             input psival, eps1;
227             real psival, eps1;
228             begin
229                 delpsieps = exp((psival - phib_id - eps1)/phiT);
230             end
231     endfunction
232
233     analog function real vinv;
234         input vgbeff1, psis1, deltaacc1, k1    ;
235         real root, vgbeff1, psis1, deltaacc1, k1;
236         begin
237             root = sqrt(hyp(psis1 + deltaacc1, 'EPS2));
238             vinv = hyp(vgbeff1 - psis1 - k1 * root, 'EPS5);
239         end
240     endfunction
241
242     analog function real vdep;
243         input psis, delacc, k0, eps;
```

```
244         real psis, delacc, k0, eps;
245         begin
246             vdep = k0*sqrt(hyp(psis+delacc,eps));
247         end
248     endfunction
249 
250     analog function real Vqdr;
251         input Vgdit, kodid, Voxp;
252         real Vgdit, kodid, Voxp;
253         begin
254             if (Vgdit > 0.0) begin
255                 Vqdr    =       Voxp + Vgdit;
256             end else begin
257                 Vqdr    =       Voxp + kodid * (- kodid/2 + sqrt(pow(kodid/2,2)
    - Vgdit));
258             end
259         end
260     endfunction
261 
262     //--------------- Beginning of actual model calculations--------------------
263 
264     analog begin
265         Vlimit          =       4.0*phiT;
266         phio            =       0.5 * (phib_id + phibd_id);
267         ko_2            =       0.5 * ko_id;
268         ko2_4           =       ko_2 * ko_2;
269         kod_2           =       0.5 * kod_id;
270         kod2_4          =       kod_2 * kod_2;
271         i16phph         =       1.0 / (16.0 * phiT * phiT);
272         phib_i          =       phib_id ;
273         phibd_i         =       phibd_id ;
274         ko_i            =       ko_id ;
275         kod_i           =       kod_id ;
276         bet_i           =       bet_id;
277         betacc_i        =       betacc_id;
278         rd_i            =       rd_id ;
279 
280         Acci            =       1.0/(1.0+ko_i/sqrt(2.0*phiT));
281         Accd            =       1.0/(1.0+kod_i/sqrt(2.0*phiT));
282         Fact1           =       LC/(LC+LD);
283 
284 
285        //-------------- Branch voltages assigned to variables-----------
286 
287         Vds             =       V(d,s);
288         Vgb             =       V(g,b);
289         Vgs             =       V(g,s);
290         Vsb             =       V(s,b);
291         Vdis            =       V(di,s);
292         Vdib            =       V(di,b);
293         Vd1b            =       V(d1,b);
294         Vddi            =       V(d1,di);
```

```
295         Vdd1            =       V(d,d1);
296         Vd1s            =       V(d1,s);
297         Vgdi            =       V(g,di);
298
299         Vgb_t           =       Vgs + Vsb - VFB_I;
300         Vsb_t           =       hyp(Vsb + 0.9*phib_i, `EPS2) + 0.1*phib_i;
301         if (Vds < 0.0) begin
302             Vds1        =       hypm(Vds, Vsb_t, MEXPD);
303         end else begin
304             Vds1        =       Vds;
305         end
306         Vgs_t           =       Vgs - VFBD_I;
307         Vgd_t           =       Vgs_t - Vds1;
308
309         //---------- Channel region quantities--------------------------
310
311         // Surface potential at the source
312         Vgb_eff         =       hyp(Vgb_t,`EPS1);
313         //In case you decide to include DIBL, add a delta_Vg term to Vgb_t here
314         //and call all previous occurences of Vgb_t as Vgb_t0
315         delacc          =       phiT*(exp(-(Acci*Vgb_eff-`EPS1)/phiT)-1.0);
316         psi_sat         =       PSISAT(Vgb_eff,delacc,ko_i);
317         psis            =       PSIS(Vgb_eff, psi_sat, delacc, Vsb_t, ko_i, M0);
318
319         // Inversion and depletion layer voltages
320         Vinv0_v         =       hyp(Vgb_eff - psis - ko_i *
    sqrt(hyp(psis+delacc, `EPS2)), `EPS5);
321         ksi_v           =       1.0 + ko_i / (2 * sqrt(delacc + psis));
322         Vdis_sat_v      =       2.0 * (Vinv0_v/ksi_v) / (1 + sqrt(1.0 +
    2.0*THE3_1*(Vinv0_v/ksi_v)));
323         Vsb_t0          =       hyp(0.9*phib_i, `EPS2) + 0.1*phib_i;
324         Vdep0_v         =       vdep(psis, delacc, ko_i, `EPS2);
325         psi_s00         =       PSIS(Vgb_eff, psi_sat, delacc, Vsb_t0, ko_i, M0);
326         Vdep00_v        =       vdep(psi_s00, delacc, ko_i, `EPS2);
327         Fmob_v          =       1.0 + THE1_I * Vinv0_v + THE2_I * (Vdep0_v -
    Vdep00_v) / ko_i;
328
329         // Surface potential at the internal drain
330         Vdis_eff        =       hypm(Vdis, Vdis_sat_v, MEXP);
331         Vdibt_eff       =       hyp(Vsb+Vdis_eff+0.9*phib_i, `EPS2) + 0.1*phib_i;
332         psid            =       PSIS(Vgb_eff, psi_sat, delacc, Vdibt_eff, ko_i,
    M0);
333         delta_psi_s     =       psid - psis;
334
335         //------------ Channel Current calculation: Ich---------------------
336
337         if (Vdis < 0.0) begin
338             Ich         =      (bet_i/Fmob_v) * (Vinv0_v - 0.5*ksi_v*Vdis +
    ksi_v*phiT) * Vdis / (1.0-THE3_1*delta_psi_s) + `GMIN*ko_i*ko_i*Vdis;
339         end else begin
```

```
340             Ich         =       (1.0+LAMD_I*Vdis) * (bet_i/Fmob_v) * (Vinv0_v -
    0.5*ksi_v*delta_psi_s + ksi_v*phiT) * delta_psi_s / (1.0+THE3_1*delta_psi_s)
    + `GMIN*ko_i*ko_i*Vdis;
341         end
342
343         //--------- Drift Region (Under gate oxide) quantities -------------
344
345         Vgdi_t          =       Vgs_t - Vdis;
346         Vdib_t          =       hyp(Vsb + Vdis + 0.9*phibd_i, `EPS2) +
    0.1*phibd_i;
347
348         Voxp            =       1 / (rd_i * betacc_i);
349         Fmobacc         =       1.0 + 0.5 * THE1ACC_I * (hyp(Vgs_t, `EPS2) +
    hyp(Vgd_t, `EPS2));
350
351         if (Vgdi_t > 0.0) begin
352           Vgdi_t_eff  =       Vgdi_t;
353         end else begin
354             hypmarg     =       phibd_i + kod_i * sqrt(phibd_i);
355             Vgdi_t_eff  =       hypm(Vgdi_t, hypmarg, 1);
356         end
357
358         Vq_dr_eff       =       hyp(Vgdi_t_eff + Voxp,`EPS2);
359
360         Vddi_sat        =       2.0 * Vq_dr_eff / (1.0 + sqrt(1.0 +
    2.0*THE3D*Vq_dr_eff));
361         Vddi_eff        =       hypm(Vddi,Vddi_sat, MEXPD);
362
363         //-------- Drift Region (Under gate oxide) Current calculation: Idr-----
364        if (Vddi < 0.0) begin
365             Idr         =       (betacc_i/Fmobacc) * (Vq_dr_eff-0.5*Vddi)*Vddi /
    (1.0+THE3D*Vddi) + `GMIN1*kod_i*kod_i*Vddi;
366         end else begin
367             Idr         =       (betacc_i/Fmobacc) * (Vq_dr_eff
    -0.5*Vddi_eff)*Vddi_eff / (1.0+THE3D*Vddi_eff) + betacc_i*Voxp*Vddi +
    `GMIN1*kod_i*kod_i*Vddi;
368         end
369
370         //------Drift Current Formulation under the thick oxide region:Idrift---
371         Ec              =       VSAT_3/(UDR);
372         if(Vdd1 < 0.0) begin
373             Idrift      =       (`P_ELECTRON*W*TSI*ND*UDR*Vdd1/LLOCOS);
374         end else begin
375             Leff        =       (LLOCOS-DELLLC) * (1 - LAMD_VG*Vgdi);
376             Eeff        =       Vdd1/(LLOCOS-DELLLC);
377             Idrift      =       (1+LAMD_VD*Vdd1/pow((LLOCOS-DELLLC),2)) *
    (`P_ELECTRON*W*TSI*ND*UDR*Vdd1/Leff) / pow((1+pow(Eeff/Ec,THETAX)),1/THETAX);
378         end
379
380
381         //------------ Channel accumulation mode of operation ---------------
382         psis_acc        =       PSISACC(Vgb_t, Vgb_eff, ko_i, Acci);
```

```
383         VinvL           =       hyp(Vgb_eff - psid - ko_i *
    sqrt(hyp(psid+delacc, `EPS2)), `EPS5);
384         zeta            =       (1.0 +
    ko_id/(2.0*sqrt(1.0+hyp(psis+delacc,`EPS5))));
385         vgtdel          =       Vinv0_v - VinvL;
386         vgtavg          =       (Vinv0_v + VinvL)/2.0;
387         Fch             =       vgtdel/(vgtavg+zeta*phiT);
388
389         Qgchmos         =       Cox*W*LC*(Vgb - VFB_I - 0.5*(psis+psid) +
    Fch*vgtdel/(12.0*zeta));
390         Qdchmos         =       -Cox*W*LC*0.5*(vgtavg - (vgtdel/6.0)*(1.0 -
    (Fch/2.0) - (Fch*Fch/20.0)));
391         Qschmos         =       -Cox*W*LC*0.5*(vgtavg + (vgtdel/6.0)*(1.0 +
    (Fch/2.0) - (Fch*Fch/20.0)));
392         Qbchmos         =       -(Qgchmos+Qdchmos+Qbchmos);
393
394         //MM20 specific
395         Q_gch           =       Qgchmos;
396         Q_dch           =       Qdchmos * Fact1;
397         Q_sch           =       Qschmos + (1.0-Fact1)*Qschmos;
398         Q_bch           =       -(Q_gch+Q_dch+Q_sch);
399
400         //---------- P-N junction charges ----------------------------------
401         V_bi            =       phiT*ln((NC*ND)/(NI*NI));
402         Qpnn            =
    W*TSI*sqrt(2*`P_EPSSI*`P_ELECTRON*(NC/(NC+ND))*hyp(V_bi+Vd1b, 1e-2)*ND);
403         V_bis           =       phiT*ln((1e26*ND)/(NI*NI));
404         Qpnns           =
    W*(SJW+2*SJD)*sqrt(2*`P_EPSSI*`P_ELECTRON*NS*(NC/(NC+NS))*hyp(V_bis+Vsb,
    1e-2));
405
406         //---------- Drift Region Formulation ------------------------------
407
408         // Surface potential at internal drain - Region II
409         Vdig_eff        =       hyp(-Vgdi_t, `EPS7);
410         delaccdi        =       phiT * exp((-Accd*(Vdig_eff-`EPS7)/phiT)-1.0);
411         psi_satdi       =       PSISAT(Vdig_eff, delaccdi, kod_i);
412         psisdi          =       PSIS(Vdig_eff,psi_satdi,delaccdi,Vdib_t,kod_i,
    M0);
413         psisaccdi       =       PSISACC(-Vgdi_t, Vdig_eff, kod_i, Accd);
414
415         //Drift region charges at the internal drain
416         V_oxdidr        =       Vgdi_t + psisdi + psisaccdi;
417         V_depdi         =       vdep(psisdi - Vdib, delaccdi, kod_i, `EPS2);
418         V_invdi         =       vinv(Vdig_eff, psisdi, delaccdi, kod_i);
419         V_qaccdepdi     =       V_oxdidr + V_invdi;
420         V_qdrdi         =       Voxp + V_qaccdepdi;
421         V_qdrdieff      =       Vlimit + hyp(V_qdrdi-Vlimit, `EPS7);
422         V_ddisat        =       2.0*V_qdrdieff/(1.0+2.0*THE3D*V_qdrdieff);
423         V_ddieff        =       hypm(Vddi, V_ddisat, MEXPD);
424
425         // Surface potential at the drain in the drift region
```

```
426         V_dsdreff       =       Vdis + Vddi_eff;
427         V_gdteff        =       Vgs_t - V_dsdreff;
428         V_dgeff         =       hyp(-V_gdteff, `EPS7);
429         delaccd         =       phiT*(exp(-Accd*(V_dgeff-`EPS7)/phiT)-1.0);
430         psi_satd        =       PSISAT(V_dgeff, delaccd, kod_i);
431         V_dbt           =       hyp(Vsb+V_dsdreff+0.9*phibd_i,`EPS2)+
        0.1*phibd_i;
432         psisd           =       PSIS(V_dgeff, psi_satd, delaccd, V_dbt, kod_i,
        M0);
433         psisaccd        =       PSISACC(-V_gdteff,V_dgeff, kod_id, Accd);
434
435         // Drift region charges at the drain
436         V_oxddr         =       V_gdteff + psisd + psisaccd;
437         V_depd          =       vdep(psisd - Vd1b, delaccd, kod_i, `EPS2);
438         V_invd          =       vinv(V_dgeff, psisd, delaccd, kod_i);
439         V_qaccdepd      =       V_oxddr + V_invd;
440         V_qdrd          =       Voxp + V_qaccdepd;
441         V_qdrdeff       =       Vlimit + hyp(V_qdrd-Vlimit, `EPS7);
442
443         // Total charges in the drift region
444         V_qdrdeffavg    =       0.5*(V_qdrdieff+V_qdrdeff);
445         delV_qaccdep    =       V_qaccdepdi - V_qaccdepd;
446         F_jdr           =       delV_qaccdep/(V_qdrdeffavg);
447         Q_daccdep       =       -Cox*W*LD*0.5*(V_qdrdeffavg -
        (delV_qaccdep/6.0)*(1.0 - (F_jdr/2.0) - (F_jdr*F_jdr/20.0)));
448         Q_saccdep       =       -Cox*W*LD*0.5*(V_qdrdeffavg +
        (delV_qaccdep/6.0)*(1.0 + (F_jdr/2.0) - (F_jdr*F_jdr/20.0)));
449
450         // MM20 Asymmmetry inclusion
451         V_Tt            =       VFB_I + phib_i - VFBD_I + ko_i * sqrt(Vdibt_eff);
452         V_gdilim        =       Vgdi_t - hyp(Vgdi_t-V_Tt, `EPS7);
453         V_gdlim         =       V_gdilim - Vddi_eff;
454         V_gdacclim      =       hyp(V_gdlim,`EPS7);
455         V_gdiacclim     =       hyp(V_gdilim,`EPS7);
456         delV_acclim     =       V_gdiacclim - V_gdacclim;
457         V_acclimavg     =       0.5*(V_gdiacclim + V_gdacclim);
458         F_jacclim       =       delV_acclim/(V_acclimavg + Voxp);
459         Q_sacclim       =       -Cox*W*LD*0.5*(V_acclimavg +
        (delV_acclim/6.0)*(1.0 + (F_jacclim/2.0) - (F_jacclim*F_jacclim/20.0)));
460
461         // MM20 Total drift region charge
462         Q_ddr           =       (Q_daccdep + Fact1*Q_saccdep +
        (1-Fact1)*Q_sacclim);// -
        (LAMD_VD*Vdd1/pow((LLOCOS-DELLLC),2))*ND*`P_ELECTRON*W*TSI*LLOCOS;
463         Q_sdr           =       ((1.0-Fact1)*(Q_saccdep - Q_sacclim));
464         Q_bdr           =       Cox*W*LD*0.5*(V_invd+V_invdi);
465         Q_gdr           =       -(Q_ddr + Q_sdr + Q_bdr);
466
467         //-------------- Our model -----------------------------
468         QQg             =       Q_gdr + Q_gch ;
469         QQd1            =       Q_daccdep + Qpnn;
470         QQs             =       Qschmos + Qpnns;
```

```
471         QQdi            =       Qdchmos + Q_saccdep;
472
473         Igtran          =       ddt(QQg);
474         Iditran         =       ddt(QQdi);
475         Id1tran         =       ddt(QQd1);
476         Istran          =       ddt(QQs);
477
478
479         //Load the currents into the EC
480
481         I(di,s)         <+      Ich;
482         I(d1,di)        <+      Idr;
483         I(d,d1)         <+      Idrift;
484         I(g,b)          <+      Igtran;
485         I(di,b)         <+      Iditran;
486         I(d1,b)         <+      Id1tran;
487         I(s,b)          <+      Istran;
488
489         /*//-------------- MM20 Model ------------------------------
490         Q_gmm20       =       Q_gch + Q_gdr;
491         Q_dmm20         =       Q_dch + Q_ddr;
492         Q_smm20         =       Q_sch + Q_sdr;
493         Q_bmm20         =       -(Q_gmm20+Q_dmm20+Q_smm20);
494
495         Igtranmm20      =       ddt(Q_gmm20);
496         Idtranmm20      =       ddt(Q_dmm20);
497         Istranmm20      =       ddt(Q_smm20);
498
499         //Load the currents into the EC MM20 Model
500         I(di,s)         <+      Ich;
501         I(d1,di)        <+      Idr;
502         I(d,d1)         <+      Idrift;
503         I(g,b)          <+      Igtranmm20;
504         I(d1,b)         <+      Idtranmm20;
505         I(s,b)          <+      Istranmm20;*/
506
507     end
508
509 endmodule
```

Bibliography

[1] Annemarie Aarts, Nele D'Halleweyn, and Ronald van Langevelde. A surface-potential-based high-voltage compact LDMOS transistor model. *Electron Devices, IEEE Transactions on*, 52(5):999–1007, 2005.

[2] Annemarie CT Aarts and Alireza Tajic. MM20 HVMOS Model: A Surface-Potential-Based LDMOS Model for Circuit Simulation. In *POWER/HVMOS Devices Compact Modeling*, pages 65–93. Springer, 2010.

[3] Michael S Adler, King W Owyang, B Jayant Baliga, and Richard A Kokosa. The evolution of power device technology. *Electron Devices, IEEE Transactions on*, 31(11):1570–1591, 1984.

[4] MICHEL J Declercq and JAMES D Plummer. Avalanche breakdown in high-voltage D-MOS devices. *Electron Devices, IEEE Transactions on*, 23(1):1–4, 1976.

[5] VAK Temple and PV Gray. Theoretical comparison of DMOS and VMOS structures for voltage and on-resistance. In *Electron Devices Meeting, 1979 Internationa*, volume 25, pages 88–92. IEEE, 1979.

[6] Kozo Sakamoto, Nobutaka Fuchigami, Kyoichi Takagawa, and Shigeo Ohtaka. A three-terminal intelligent power MOSFET with built-in reverse battery protection for automotive applications. *Electron Devices, IEEE Transactions on*, 46(11):2228–2234, 1999.

[7] Prasanth Perugupalli, Malay Trivedi, Krishna Shenai, and SK Leong. Modeling and characterization of an 80 V silicon LDMOSFET for emerging RFIC applications. *Electron Devices, IEEE Transactions on*, 45(7):1468–1478, 1998.

[8] Paul GY Tsui, PV Gilbert, and Shih Wei Sun. Integration of power LDMOS into a low-voltage 0.5 μm BiCMOS technology. In *Electron Devices Meeting, 1992. IEDM'92. Technical Digest., International*, pages 27–30. IEEE, 1992.

[9] Paul GY Tsui, PV Gilbert, and S-W Sun. A versatile half-micron complementary BiCMOS technology for microprocessor-based smart power applications. *Electron Devices, IEEE Transactions on*, 42(3):564–570, 1995.

[10] B Jayant Baliga. An overview of smart power technology. *Electron Devices, IEEE Transactions on*, 38(7):1568–1575, 1991.

[11] PM Holland and PM Igic. An alternative process architecture for CMOS based high side RESURF LDMOS transistors. In *Microelectronics, 2006 25th International Conference on*, pages 195–198. IEEE, 2006.

[12] Jacob A van der Pol, AW Ludikhuize, HGA Huizing, B Van Velzen, RJE Hueting, JF Mom, G Van Lijnschoten, GJJ Hessels, EF Hooghoudt, R van Huizen, et al. A-BCD: An economic 100 V RESURF silicon-on-insulator BCD technology for consumer and automotive applications. In *Power Semiconductor Devices and ICs, 2000. Proceedings. The 12th International Symposium on*, pages 327–330. IEEE, 2000.

[13] MN Darwish. Study of the quasi-saturation effect in VDMOS transistors. *Electron Devices, IEEE Transactions on*, 33(11):1710–1716, 1986.

[14] Malay Trivedi, Pankaj Khandelwal, and Krishna Shenai. Performance modeling of RF power MOSFETs. *Electron Devices, IEEE Transactions on*, 46 (8):1794–1802, 1999.

[15] Wenwei Yang, Mohan V. Dunga, Xuemei Xi, et al. *BSIM 4.6.2 MOSFET model-user manual*, 2008. URL http://www-device.eecs.berkeley.edu/bsim3/BSIM4.

[16] Yasunori Oritsuki, Masahiro Yokomichi, Takahiro Kajiwara, Akihiro Tanaka, Norio Sadachika, Masataka Miyake, Hideyuki Kikuchihara, Koh Johguchi, Uwe Feldmann, Hans Jürgen Mattausch, et al. HiSIM-HV: A compact model for simulation of high-voltage MOSFET circuits. *Electron Devices, IEEE Transactions on*, 57(10):2671–2678, 2010.

[17] Akihiro Tanaka, Yasunori Oritsuki, Hideyuki Kikuchihara, Masataka Miyake, Hans Juergen Mattausch, Mitiko Miura-Mattausch, Y Liu, and Keith Green. Quasi-2-dimensional compact resistor model for the drift region in high-voltage LDMOS devices. *Electron Devices, IEEE Transactions on*, 58(7): 2072–2080, 2011.

[18] Matthias Bucher, Christophe Lallement, Christian Enz, Fabien Theodoloz, and Francois Krummenacher. The EPFL-EKV MOSFET model equations for simulation technical report, model version 2.6. Technical report, 1998. URL http://legwww.epfl.ch/ekv/model.

[19] JM Sallese and A-S Porret. A novel approach to charge-based non-quasi-static model of the MOS transistor valid in all modes of operation. *Solid-State Electronics*, 44(6):887–894, 2000.

[20] Yogesh Singh Chauhan, Costin Anghel, Francois Krummenacher, Christian Maier, Renaud Gillon, Benoit Bakeroot, Bart Desoete, Steven Frere, Andre Baguenier Desormeaux, Abhinav Sharma, et al. Scalable general high voltage MOSFET model including quasi-saturation and self-heating effects. *Solid-state electronics*, 50(11):1801–1813, 2006.

[21] *MOS Model 20, Level 2002*, 2008. URL http://www.nxp.com/models/simkit/high-voltage-models/model-20.html.

[22] T Lekshmi, AK Mittal, A DasGupta, A Chakravorty, and N DasGupta. Compact modeling of SOI-LDMOS including quasi-saturation effect. In *Electron Devices and Semiconductor Technology, 2009. IEDST'09. 2nd International Workshop on*, pages 1–4. IEEE, 2009.

[23] Ujwal Radhakrishna, Amitava DasGupta, Nandita DasGupta, and Anjan Chakravorty. Modeling of SOI-LDMOS transistor including impact ionization, snapback, and self-heating. *Electron Devices, IEEE Transactions on*, 58 (11):4035–4041, 2011.

[24] SF Frre, J Rhayem, HO Adawe, R Gillon, M Tack, and AJ Walton. LDMOS capacitance analysis versus gate and drain biases, based on comparison between TCAD simulations and measurements. In *Solid-State Device Research Conference, 2001. Proceeding of the 31st European*, pages 219–222. IEEE, 2001.

[25] Longxing Shi, Kan Jia, and Weifeng Sun. A novel compact high-voltage LDMOS transistor model for circuit simulation. 2013.

[26] Wenyuan Wang, Bogdan Tudor, Xuemei Xi, Weidong Liu, and Frank Jyhchwen Lee. An accurate and robust compact model for high-voltage MOS IC simulation. 2013.

[27] Soo-Young Oh, Donald E Ward, and Robert W Dutton. Transient analysis of MOS transistors. *Electron Devices, IEEE Transactions on*, 27(8):1571–1578, 1980.

[28] *Taurus Medici User's Guide, Version V-2003, Synopsys Inc, Mountain View, CA*, 2003.

[29] T Lekshmi. DC modeling of SOI-LDMOS including quasi-saturation and self-heating. Master's thesis, Indian Institute of Technology Madras, 2009.

[30] Ujwal Radhakrishna. Compact modeling of SOI-LDMOS transistor including impact ionization, snapback and self-heating. Master's thesis, Indian Institute of Technology Madras, May 2011.

[31] Prasad Sarangapani. Modeling of Charges and Capacitance in SOI-LDMOS Transistors. Master's thesis, Indian Institute of Technology Madras, May 2013.

[32] *MOS model 20, Level 2002, NXP Semiconductors*, 20011.

[33] STEPHEN D SHAPIRO. Carrier mobilities m silicon empirically related to doping and field. *Proceedings of the IEEE*, 1967.

[34] Kan Jia, Weifeng Sun, and Longxing Shi. A novel surface potential-based short channel MOSFET model for circuit simulation. *Microelectronics Journal*, 42(10):1169–1175, 2011.

[35] *Verilog-AMS Language Reference Manual, Version 2.3.1*, 2009. URL http://www.designers-guide.org/VerilogAMS.

[36] Geoffrey J Coram. How to (and how not to) write a compact model in verilog-a. In *Behavioral Modeling and Simulation Conference, 2004. BMAS 2004. Proceedings of the 2004 IEEE International*, pages 97–106. IEEE, 2004.

[37] *Virtuoso Spectre Circuit Simulator Guide, Version 7.0.1*, 2008. URL http://www.d.umn.edu/~htang/cadence_doc.