Design of a Digital Delta-Sigma Modulator

A Project Report

submitted by

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THESIS CERTIFICATE

This is to certify that the thesis titled **Design of a Digital Delta-Sigma converter**, submitted by **Girish Ramakrishnan**, to the Indian Institute of Technology, Madras, for the award of the degree of **Bachelor of Technology and Master of Technology**, is a bona fide record of the research work done by him under our supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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ABSTRACT

This Thesis is organized into three parts. Part 1 deals with the design considerations for a digital-to-digital cascaded Delta-Sigma modulator. Part 2 describes the design of a Switched Capacitor dual return-to-zero (SCDRZ) Continuous-time Delta-Sigma modulator (CTDSM). Part 3 is an analytic description of a Ring Amplifier (RingAmp) for switched capacitor circuits.

The first chapter deals with the design considerations of a Digital Delta-Sigma Modulator and the design challenges faced while designing the digital backend for a high resolution modulator.

The Second chapter extends a Switched Capacitor Return-to-Zero DAC to a Switched Capacitor Dual-Return-to-Zero DAC which benefits from the properties of the SCRZ DAC while providing linearity advantages and better anti-aliasing properties than an SCRZ DAC.

The Third Chapter deals with an analytical description of a Ring Amplifier and an example of its application in Switched Capacitor Circuits.

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ABBREVIATIONS

CTDSM	Continuous Time Delta-Sigma Modulator
DSM	Delta-Sigma Modulator
VQ	Vector Quantizer
DEM	Dynamic Element Matching
DWA	Data Weighted Averaging
RingAmp	Ring Amplifier
SCRZ	Switched Capacitor Return-to-Zero
SCDRZ	Switched Capacitor dual Return-to-zero
RZ	Return-to-Zero
DAC	Digital to Analog Converter
ADC	Analog to Digital Converter

CHAPTER 1

Digital Delta-Sigma Modulator

1.1 Introduction

1.1.1 Motivation

High resolution audio in excess of 18 bits is routinely used in applications like DVD-Audio and Blue-Ray formats. Audio DACs and ADCs operate with low-signal bandwidths, typically sampling the audio stream/processing a digital audio stream at 48kHz. In this light, sigma-delta converters become the architecture of choice for audio processing. For high resolution audio, they become the only choice!

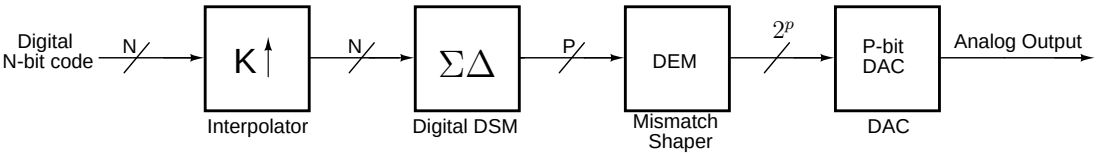


Figure 1.1: Delta-Sigma Digital to Analog converter

A Delta-Sigma DAC typically consists of a digital backend which performs the oversampling and noise-shaping operations on the input bitstream. The oversampled, noise shaped bitstream is fed to the front-end DAC which is typically a single-bit DAC. The analog output of the DAC is then low-pass filtered to attenuate the out-of-band noise and the resulting waveform drives the speakers.

Designing the modulator so as to have a single-bit output serves to simplify the analog DAC design. A single-bit DAC does not exhibit static non-linearity caused by mismatch due to the DAC elements.

A multi-bit DAC on the other hand, has the advantage of better jitter performance because of smaller DAC step sizes. A multi-bit DAC in the digital delta-sigma loop also allows the loop to support a larger MSA for a given NTF. In other words, the out of band noise when a multi-bit DAC is used is less than that when a single-bit DAC is

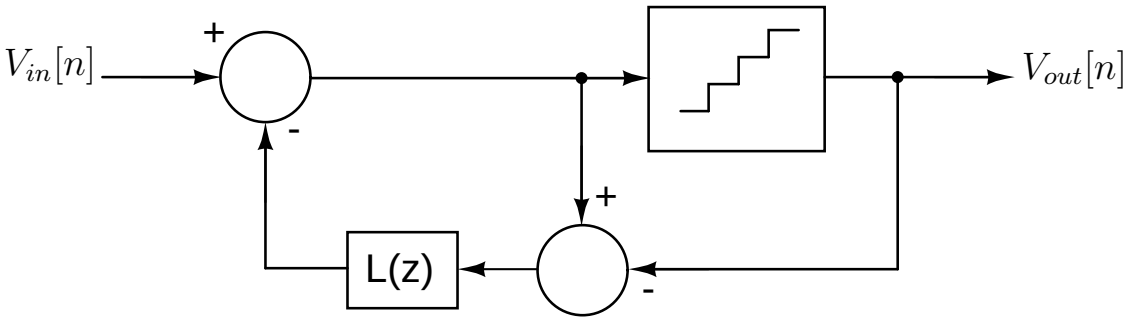


Figure 1.2: Digital Delta-Sigma Modulator

used. This is because the peak fed back error in a multi-bit architecture is less than that in a single-bit architecture.

In high resolution DACs, the non-linearity of the front end filter can cause intermodulation of the out of band noise, into the signal band. In this light, it is important that both the out of band noise, as well as any tonal out of band component is kept within bounds.

1.1.2 Design Objective

The objective of this work is to design the backend digital section of a Delta Sigma audio DAC. The design specifications are given in Table 1.1.

Table 1.1: Design Specifications for Digital Delta-Sigma Modulator

Signal Bandwidth	20Hz to 20kHz
Input bitstream	24 bits wide at 48kHz
Targered SNR	120dB
Technology	UMC 180nm

1.2 Cascaded Modulator

With reference to the arguments in Subsection 1.1.1, the design for a high resolution DAC should take into consideration not only inband noise performance but also out of band noise performance. To this end, an architecture that can reduce the out of band noise, with no penalty to the in-band noise is desirable. The cascaded modulator topology in 1 is one such architecture.

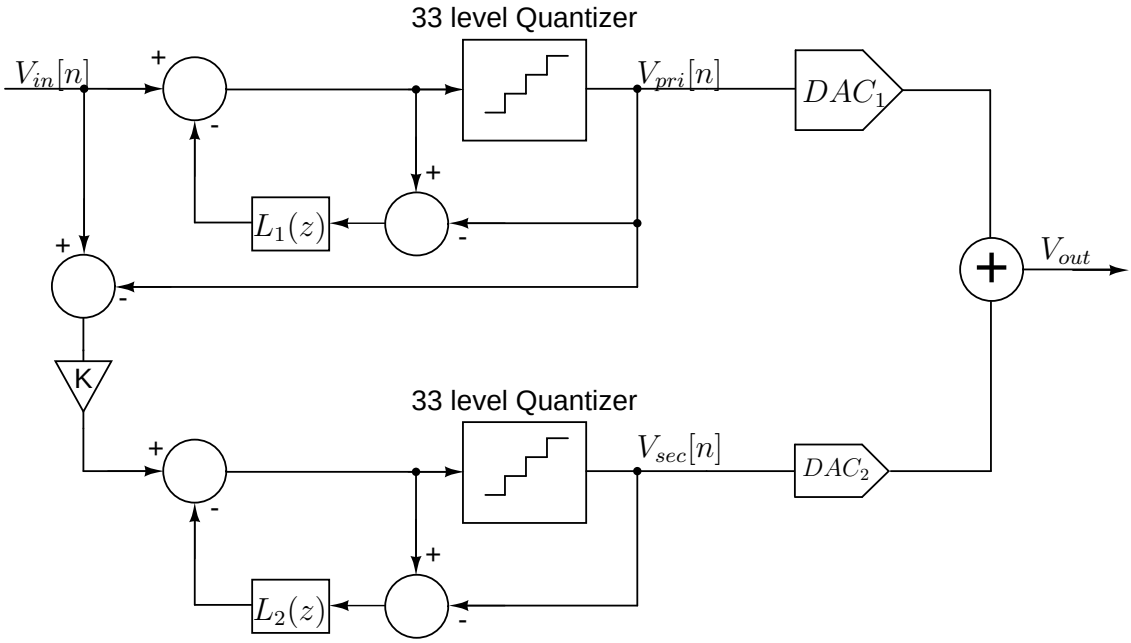


Figure 1.3: The Cascaded Delta-Sigma Modulator. The Secondary DAC has a scaling of $\frac{1}{k}$ as compared to the primary.

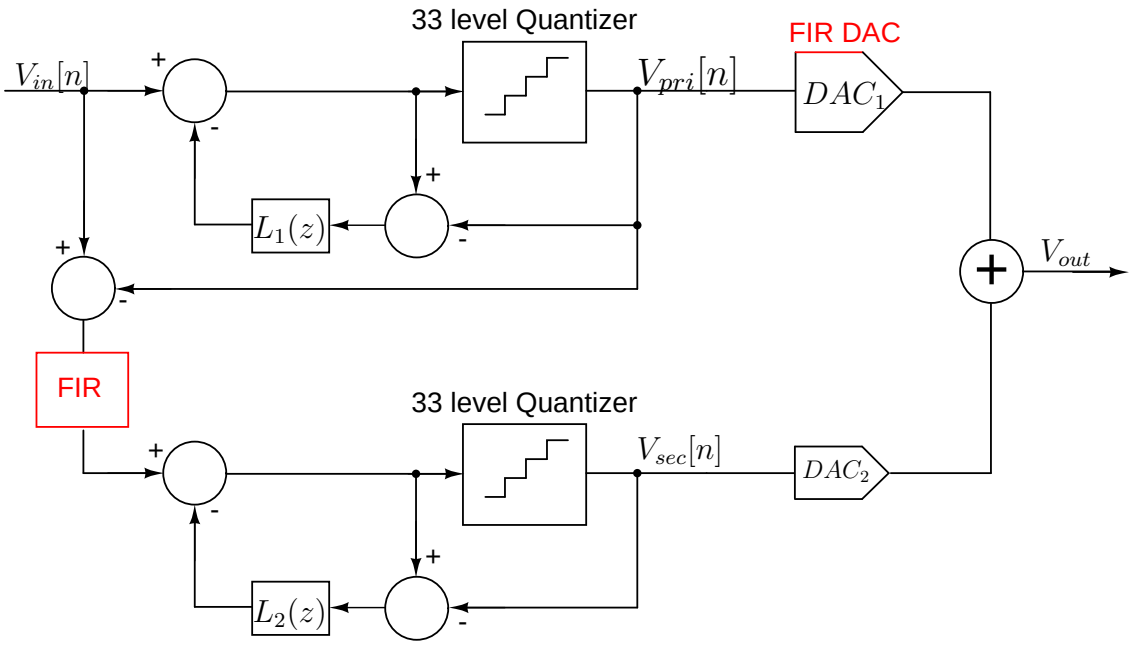
Figure 1.3 shows the block diagram of the cascaded Digital DSM. The cascaded modulator is composed of two individual Digital DSMs. The output error from the primary DSM, is gained up by a factor of k and fed as an input to the secondary DSM. The output of the secondary modulator is then scaled down by the factor k in the analog domain and subtracted from the output of the primary DAC. For a two level cascaded system, It can be shown that

$$V_{pri}(z) = V_{in}(z) + NTF_1(z)E_1(z) \tag{1.1}$$

$$V_{sec}(z) = -k \times NTF_1(z)E_1(z) + NTF_2(z)E_2(z) \tag{1.2}$$

$$V_{out}(z) = V_{in}(z) + \frac{1}{k} \times NTF_2(z)E_2(z) \tag{1.3}$$

As can be seen, the output of the cascaded structure is composed of the signal component and attenuated, shaped quantization noise from the secondary modulator. This attenuation of the shaped quantization noise occurs both to the inband noise as well as the out of band noise with the price paid being only the additional digital modulator



and the secondary DAC. The gain parameter k can be increased until the secondary modulator starts to saturate.

1.3 The FIR cascaded Modulator

The FIR cascaded modulator replaces the gain factor k between the primary and secondary modulator with an FIR filter with a low-frequency gain of k'. The FIR filter serves to filter the error signal from the primary modulator. Since most signal power lies in the high frequency spectrum, the FIR filter should be lowpass. To compensate for the FIR filter in the error path, an equivalent FIR filter should be implemented in the primary DAC. In the presence of the FIR filter, I higher value of k' can be used in comparison to k in the case of the generalized cascaded modulator before the secondary modulator saturates.

The Digital Modulator designed uses a four tap FIR cascaded modulator topology with a k' of 24. With the generalized cascaded modulator, a k of 10 could be used before the secondary modulator saturated. An effective gain of 8 dB SQNR is attained using the new cascaded topology.

1.4 Interpolator

The digital bitstream is fed into the audio DAC at the rate of 48kHz. The DSM, however operates at 3.072MHz with an OSR of 64. Therefore, the input signal must be upsampled by a factor of 64. Simply upsampling done by zero padding causes a reduction in the signal amplitude as well as introduction of images of the signal about multiples of the input sampling frequency. We thus, need an interpolation filter.

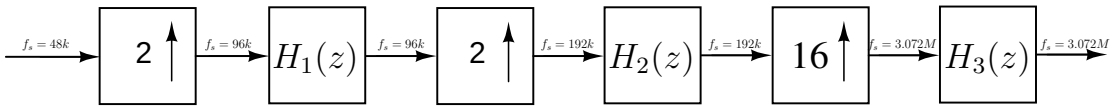


Figure 1.4: Multi-Stage Interpolation filter. $H_1(z)$ and $H_2(z)$ have halfband transfer functions while $H_3(z)$ has a $sinc^4$ response.

Upsampling the signal at one go by 64, and then interpolating puts tight constraints on the interpolation filter as the ratio of the frequency at which the filter operates to the signal band cut-off frequency is very high. The filter required would be an extremely large filter. Instead, upsampling the signal and filtering it in multiple stages is a preferred approach. The first few upsampling operations are responsible for the images closest to the signal band, whose filtering is most critical. Thus, we adopt a filtering scheme where the interpolation is done in a $2 \times 2 \times 16$ fashion.

1.4.1 Halfband Filter implementation

The first two interpolations were realized using halfband filters. Halfband filters possess passband-stopband symmetry (ie. Their passband and stopband ripples are equal and the respective cut-off frequencies are symmetric about $\frac{f_s}{2}$). Furthermore, the impulse response of FIR halfband filters has alternate samples to go to zero. A linear phase implementation of an N tap halfband FIR filter, requires a storage of only $\frac{N}{4} + 1$ coefficients.

The halfband filters were implemented using a polyphase architecture. A polyphase implementation of an interpolator takes advantage of the fact that upsampling by a factor of L by zero padding renders L-1 samples zero for every non-zero sample. For the samples that go to zero, the multiplication operation is redundant. A polyphase implementation of the halfband filters, thus halves the number of multiply operations.

A further reduction of 2 is obtained by recognizing that the impulse response of the filter is symmetric and the distributive property of multiplication over addition allows another reduction in the multiply operation by half.

Both halfband filters were implemented using multiplier reuse topologies. A single multiplier was clocked at 16 times the filter operating frequency in the first filter and used over 15 filter coefficients. In the second filter, a single multiplier was clocked at 8 times the filter operating frequency and used over 5 filter coefficients. The multiplier reuse gives considerable savings in the interpolation filter area.

1.4.2 First stage filter

The first stage filter is implemented as a 59 tap halfband filter. The filter was designed to so as to have 75dB of stopband attenuation. The filter coefficients were quantized to 13 bits of precision.

The filter transfer function is obtained as,
$H_1(z) = 2 - 5z^{-2} + 10z^{-4} - 20z^{-6} + 35z^{-8} - 58z^{-10} + 90z^{-12} - 137z^{-14} + 201z^{-16} - 291z^{-18} + 420z^{-20} - 614z^{-22} + 945z^{-24} - 1678z^{-26} + 5195z^{-28} + 8191z^{-29} + 5195z^{-30} - 1678z^{-32} + 945z^{-34} - 614z^{-36} + 420z^{-38} - 291z^{-40} + 201z^{-42} - 137z^{-44} + 90z^{-46} - 58z^{-48} + 35z^{-50} - 20z^{-52} + 10z^{-54} - 5z^{-56} + 2z^{-58}$

1.4.3 Second stage filter

The second stage filter is also required to have a stopband attenuation of 75dB. However, the wider transition width facilitated by the filtering done by the first halfband reduces the complexity of the required filter. a 15 tap halfband filter is used for the second stage. The filter coefficients were quantized to 12 bits of precision. The filter transfer function is obtained as,
$H_2(z) = -22 + 143z^{-2} - 560z^{-4} + 2486z^{-6} + 4095z^{-7} + 2486z^{-8} - 560z^{-10} + 143z^{-12} - 22z^{-14}$

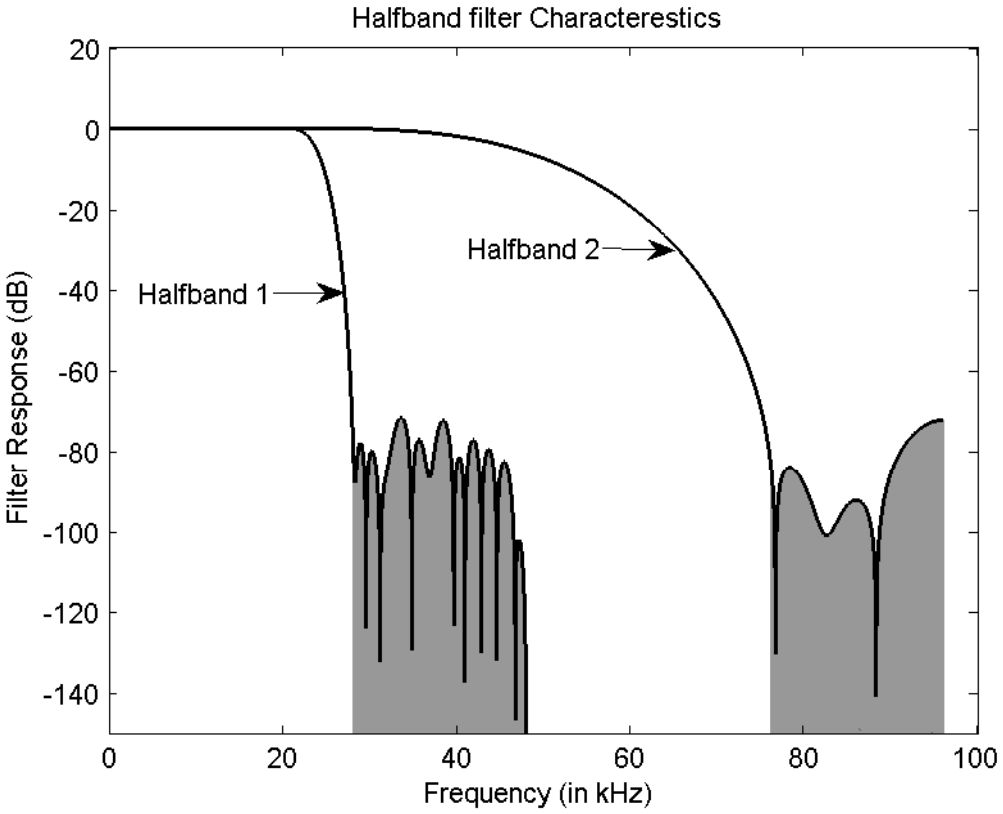


Figure 1.5: Filter response of the first and second stage halfband filters. The shaded region corresponds to the respective image frequency bands.

1.4.4 Third Stage CIC filter

The third stage filter is implemented as a cascaded integrator comb (CIC) filter as described in 2.

A CIC filter is a filter structure integrated with an upsampling or down sampling operation, optimized for simple implementation. A CIC filter can be implemented without the use of multipliers, just using accumulation and differentiation stages.

The input signal is fed into a cascade of 3 comb stages (differentiators), the intermediate output is then upsampled by a factor of 16 (by padding zeros) and fed into a cascade of 3 integrators (accumulators). The filter response is equivalent to a cascade of 3 sinc filters. The Transfer function of the CIC filter (operating at the upsampled bitstream's frequency) is given by:

$$H_3(z) = \left(\frac{1 - z^{-16}}{1 - z^{-1}}\right)^3$$

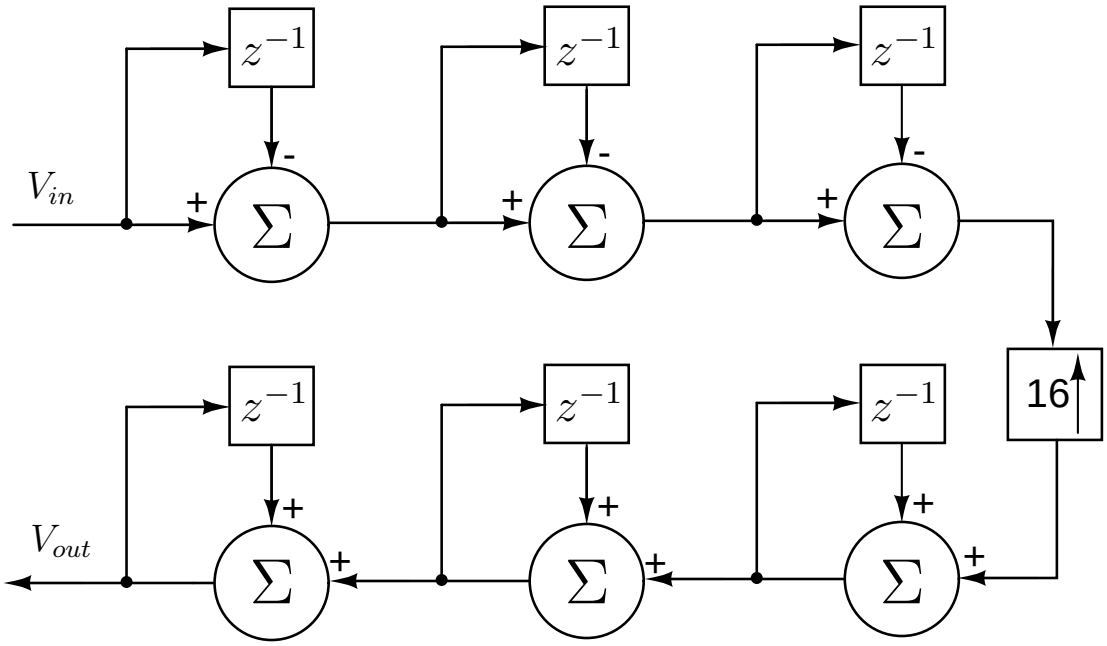


Figure 1.6: Block Diagram of the CIC interpolating filter

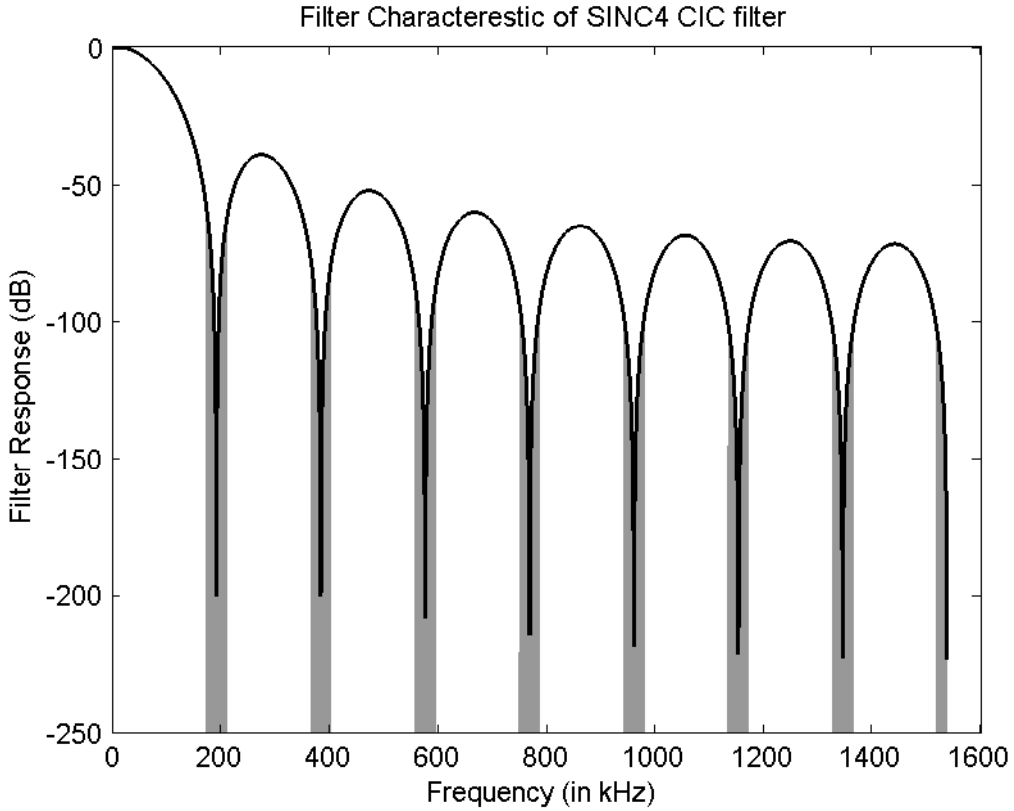


Figure 1.7: Filter response of the third stage interpolation filter. The shaded regions correspond to the image frequency bands.

1.5 Delta Sigma Modulator

The Digital Delta-Sigma Modulator is responsible for encoding the 24-bit oversampled input from the interpolator to a 5-bit noise shaped bit sequence. The Nyquist bandwidth

of the input bit-sequence is 48kHz. An OSR of 64 was chosen so that the DSM operates at 3.072MHz. As discussed in section 1.1.1, the focus on designing high resolution DACs is not only to minimize inband noise, but also out of band noise. This requires the modulator design to have a passive NTF, with a sufficiently low OBG and a multi-bit quantizer. For the cascaded modulator architecture, both these conditions need to be satisfied only for the secondary modulator. However, following the same design criteria for the primary modulator serves to reduce the error signal from the primary allowing the use of a larger value of the gain factor 'k'. It is in our interest to maximize k as the quantization noise of the cascaded modulator architecture is attenuated by the same factor k, as seen from Equation 1.3.

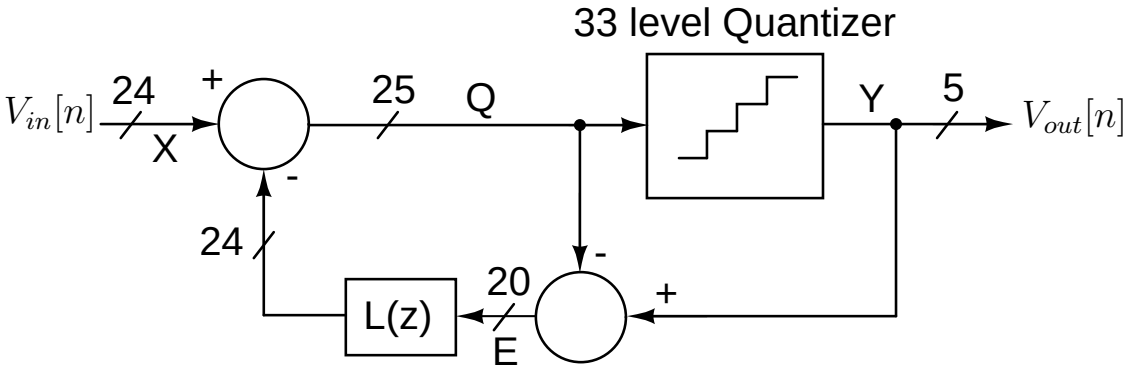


Figure 1.8: Block Diagram of the Digital Delta Sigma modulator used

The primary and secondary modulator are designed identically with the same Loop filter transfer functions and the same quantizers. The architecture used to design the modulators is the error feedback architecture. as shown in Figure 1.8. The STF and NTF of this architecture can be obtained as follows:

$$Q(z) = X(z) - E(z)L(z) \tag{1.4}$$

$$E(z) = Y(z) - Q(z) \tag{1.5}$$

$$Y(z) = E(z) + Q(z) \tag{1.6}$$

$$Y(z) = X(z) + (1 - L(z))E(z) \tag{1.7}$$

Comparing it with the generalized equation,

$$Y(z) = STF(z)X(z) + NTF(z)E(z) \tag{1.8}$$

we obtain

$$STF(z) = 1 \tag{1.9}$$

$$NTF(z) = 1 - L(z) \tag{1.10}$$

Thus,

$$L(z) = 1 - NTF(z) \tag{1.11}$$

As can be seen, the STF of the error feedback architecture is 1. In the light of the cascaded modulator, it is advantageous to use the error feedback architecture as the cascaded modulator relies on the cancellation of the shaped quantization noise from the primary modulator. Since the quantization noise in the primary modulator spans the whole band from 0 to $\frac{f_s}{2}$, the cancellation will be imperfect if the secondary modulator's STF does not exhibit an all-pass response. A third order NTF with an OBG of 2.5 was chosen for both modulators. The NTF, quantized to five bit coefficients is given by the expression,

$$NTF(z) = \frac{4 - 12z^{-1} + 12z^{-2} - 4z^{-3}}{4 - 5z^{-1} + 3z^{-2} - z^{-3}} \tag{1.12}$$

The required loop filter transfer function is

$$L(z) = \frac{7z^{-1} - 9z^{-2} + 3z^{-3}}{4 - 5z^{-1} + 3z^{-2} - z^{-3}} \tag{1.13}$$

An IIR-NTF was adopted without converting it to an equivalent FIR to minimize the filter complexity.

The Quantizer was implemented as a 5-bit (33 level) quantizer to lower the out-of-band quantization noise.

The NTF was implemented without optimized zeroes. The main reason for this was that to accurately realize the NTF with optimized zeroes, 12 bits of coefficient quantization was required. In high resolution multi-bit DACs, the noise floor is shaped by the mismatch transfer function of the DEM loop rather than the NTF itself.

Thus, although in the absence of mismatch, an NTF with optimized zeroes and finer co-efficient quantization is advantageous, in a real scenario, the advantage of implementing optimized zeros is negated by the error due to mismatch.

1.6 Mismatch Shaper

The digital Delta-Sigma Modulator is followed by a mismatch shaper. Both the primary and secondary modulators have an output 5-bit sequence. The usage of multi-bit quantizers in the primary and secondary is in order to increase the value of k and reduce the out of band noise respectively.

Multi-bit DACs which follow the digital delta-sigma loop when driven traditionally are prone to non-linearities on account of mismatch between individual DAC elements. There are many methods to mitigate these problems. DAC elements can be matched better by laser trimming, although it is a costly affair. Other methods for dealing with element mismatch include digital calibration (where the element mismatch is cancelled out using a calibration circuit), or if the mismatch is known beforehand, digital correction. However, most of the above methods are either too costly or require prior knowledge of element mismatch. However, there are also certain mismatch shaping schemes which can mitigate mismatch by cleverly choosing DAC elements so that the error due to mismatch is shaped according to a pre-determined Transfer function. Naturally, these methods are applicable only to oversampling converters.

1.6.1 Effect of Mismatch

Traditionally driven multi-bit DACs driven by thermometer-coded input words suffer from non-linearity due to element mismatch. Consider a 2-bit thermometer coded DAC with the respective elements being excited according to the bitstreams b_0, b_1, b_2.

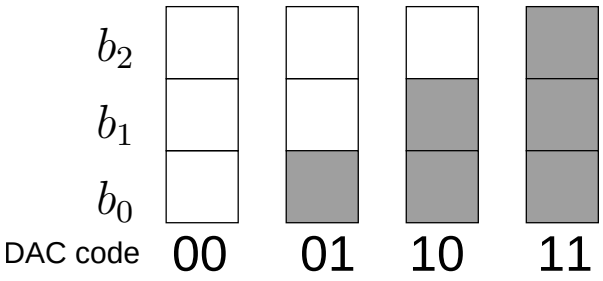


Figure 1.9: DAC behaviour for a thermometrically excited 2-bit DAC

From Figure 1.9, the DAC output is

$$V_{out} = \psi \times (b_0 + b_1 + b_2) \tag{1.14}$$

where ψ is the digital to analog DAC scaling factor. It is easy to see that while b_0, b_1, b_2 are non-linear functions of the DAC code, their sum is a linear function of the DAC code. This means, that the linearity of the DAC is conditional to the exact cancellation of harmonics in the PSDs of the bit sequences $b_0, b_1 and b_2$. A mismatched DAC will exhibit an analog output,

$$V_{out} = \psi_0 \times b_0 + \psi_1 \times b_1 + \psi_2 \times b_2 \tag{1.15}$$

where ψ_0, ψ_1 and ψ_2 are mismatched DAC weightages. The mismatch in DAC elements causes an incomplete cancellation of undesirable harmonic content in b_0, b_2, b_3 which causes the output waveform to contain harmonics.

Mismatch shaping techniques ensure that the bitstreams b_0, b_1 and b_2 do not contain any harmonic content but rather have shaped PSDs themselves, while at the same time maintaining the required sum $b_0 + b_1 + b_2$. This ensures that any mismatch between the elements does not affect the inband performance. Outside the signal band, the quantization noise dominates.

1.6.2 Data Weighted Averaging

Data Weighted Averaging (DWA) is a mismatch shaping technique that performs first order low-pass shaping on the DAC excitation bitstreams. It is marked by the simplicity in its implementation. Figure 1.10 depicts data weighted averaging applied on a two-bit DAC.

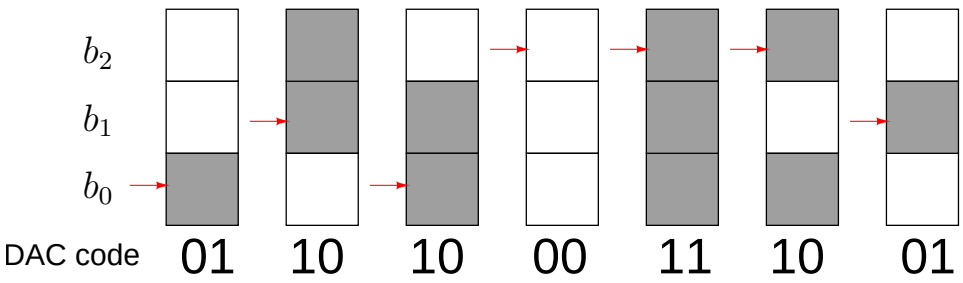


Figure 1.10: The DAC bitstreams after Data weighted averaging is applied

The DWA scheme choses a contiguous set of DAC elements based on a rotating pointer. The pointer denoted by the red arrow in Figure 1.10, cyclically shifts in such a manner that the new position of the pointer is offset from the previous position by the

DAC code-

$$p_{new} = mod_n(p_{old} + (b_0 + b_1 + b_2)) \tag{1.16}$$

where n is the number of elements in the DAC. This mismatch shaping scheme shapes the mismatch error according to the transfer function $1 - z^{-1}$.

The mismatch shaping can be accomplished by simply cascading the Digital DSM with a barrel shifter. In the implementation in the 32-level DAC, a logarithmic shifter gave power and area savings and was used to implement the DWA logic.

1.6.3 Vector Quantization

Data weighted averaging can at most provide first order mismatch shaping. There are a few techniques capable of performing higher order shaping. The method of the vector quantizer introduced in 3, is depicted in Figure 1.11

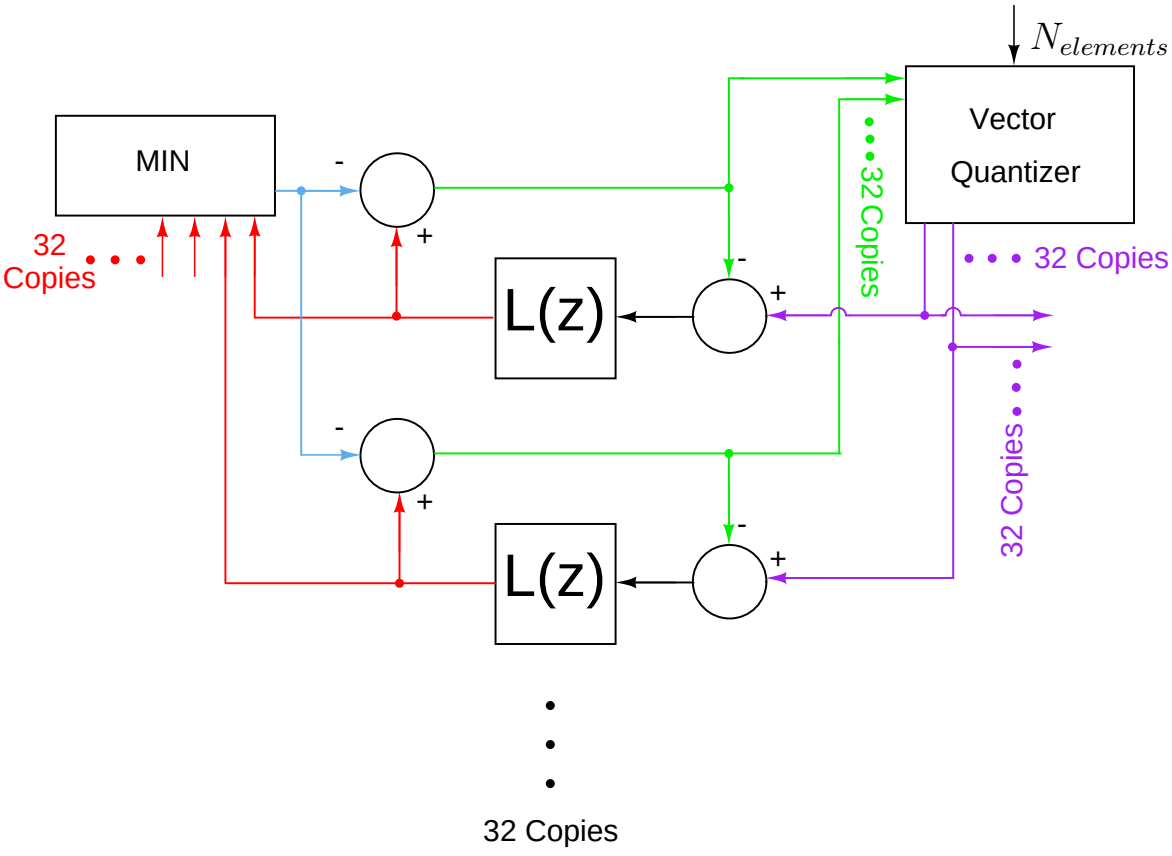


Figure 1.11: Vector Quantizer based DEM block

The vector quantizer shapes element mismatch similar to the way a DSM shapes quantization noise. The vector quantizer logic for an N+1-level DAC (N-element DAC)

consists of N-subloops feeding into a common "vector quantizer" block. The vector quantizer is a digital circuit which sorts N-digital numbers (the green lines) and corresponding to the highest $N_{elements}$ lines, sets $N_{elements}$ 1-bit output lines to logic high (the violet lines). It operates so that $N_{elements}$ output lines from the vector quantizer are always high and the individual logic lines are shaped according to an NTF given by $1 + L(z)$.

This can be observed by recognizing that The individual loops in Figure 1.11 are similar to DSMs themselves, with the vector quantizer behaving like a one-bit quantizer with the reference level varying based on $N_{elements}$. The output lines of the vector quantizer are used to drive the DAC elements. The block labelled MIN computes the minimum of the 32 red lines which correspond to the filter output. This keeps the input to the vector quantizer within bounds and simplifies its design.

A vector quantizer based DEM block was also designed and evaluated for the Digital Delta-Sigma Modulator. A second order NTF with an OBG of 4 was used for simplicity of the filter and vector quantizer realization. It was observed that 5 bits was sufficient to represent the input signal to the vector quantizer at each of the 32 lines. The vector quantizer was realized using a batcher hardware sorting network. There exist simplified realizations of the vector quantizer which perform partial sorting to trade-off reduced hardware complexity with degraded mismatch shaping performance.

The Figure 1.12 shows the DAC excitation bitstream for the two different schemes discussed and for a thermometer encoded DAC. As can be seen, there is considerable harmonic content in the excitation bitstream for the thermometer encoded DAC.

1.6.4 Final Mismatch Shaping implementation

The mismatch shaper was eventually implemented using the pointer Rotation DWA. Although the vector quantizer gives superior mismatch shaping, the complexity of implementation of the vector quantizer is inhibitive. Furthermore, although more aggressive NTFs with optimized zeros can be used to obtain better mismatch shaping, this also comes at the cost of the sorter complexity.

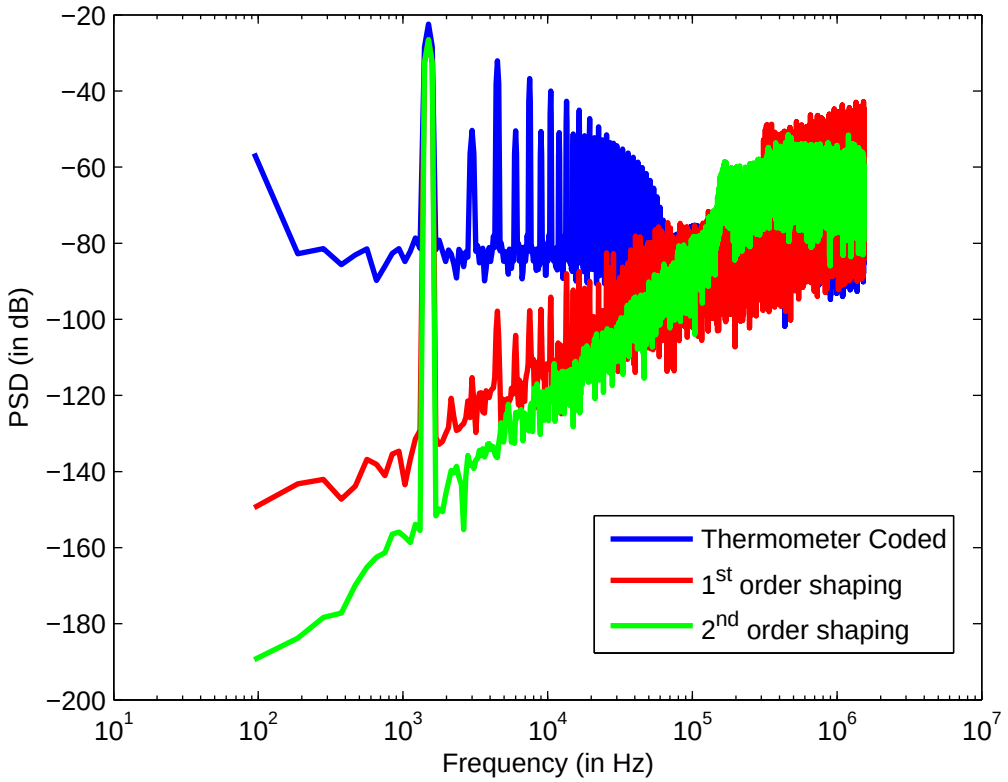


Figure 1.12: DAC excitation bitstreams

1.7 Performance

The netlist was synthesized and simulated and PSDs of the signals were plotted. The input signal is a single tone at 6kHz, with an amplitude of 0.95 times the MSA.

As can be seen from figure 1.13, the output of the interpolator contains the attenuated image frequencies Since the first halfband filter was designed with an attenuation of at least 75 dB, the first image at 42 kHz, sees an attenuation of 86dB.

The Power Spectral Density of the Primary Modulator output and Cascaded modulator output are plotted in Figure 1.14 The filtered out image frequencies are seen in the output PSD. They lie out of band and hence, do not contribute directly to the SNDR of the modulator.

Figure 1.15, depicts the predicted analog DAC output in the presence of 0.1% element mismatch. The SQNR in the absence of any DEM algorithm is 95.2 dB. With first order shaping, it is 131dB and with second order shaping, it is 143.5 dB.

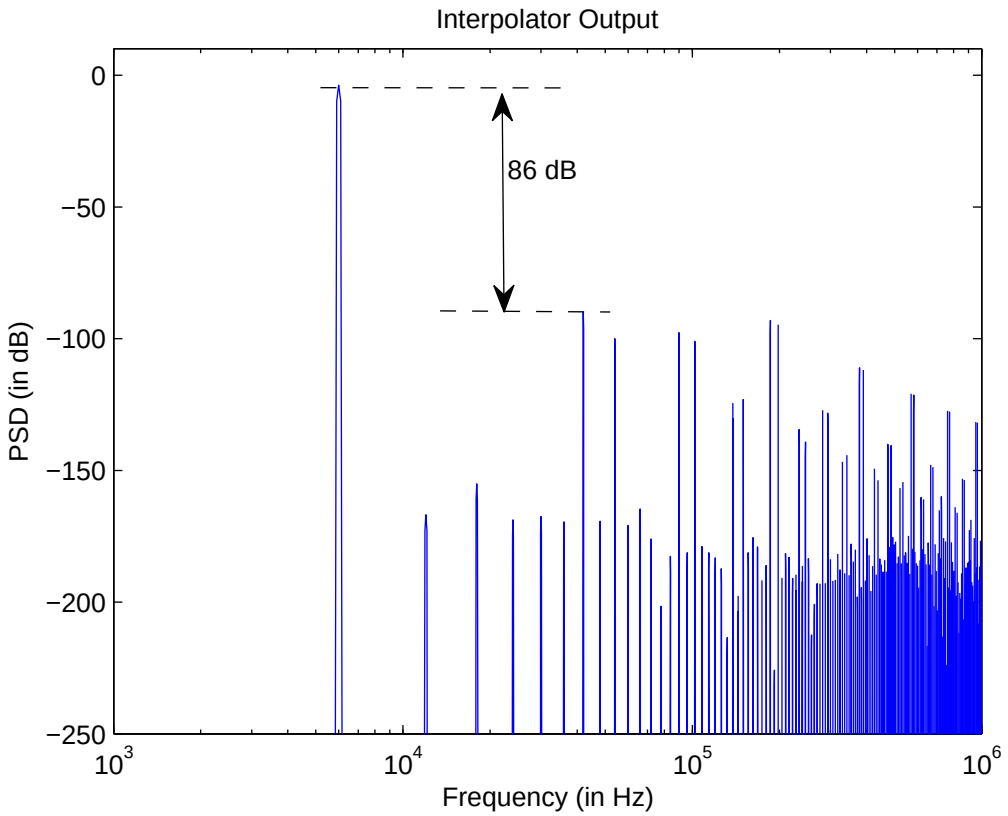


Figure 1.13: Output at interpolator showing the rejection of the first image frequency

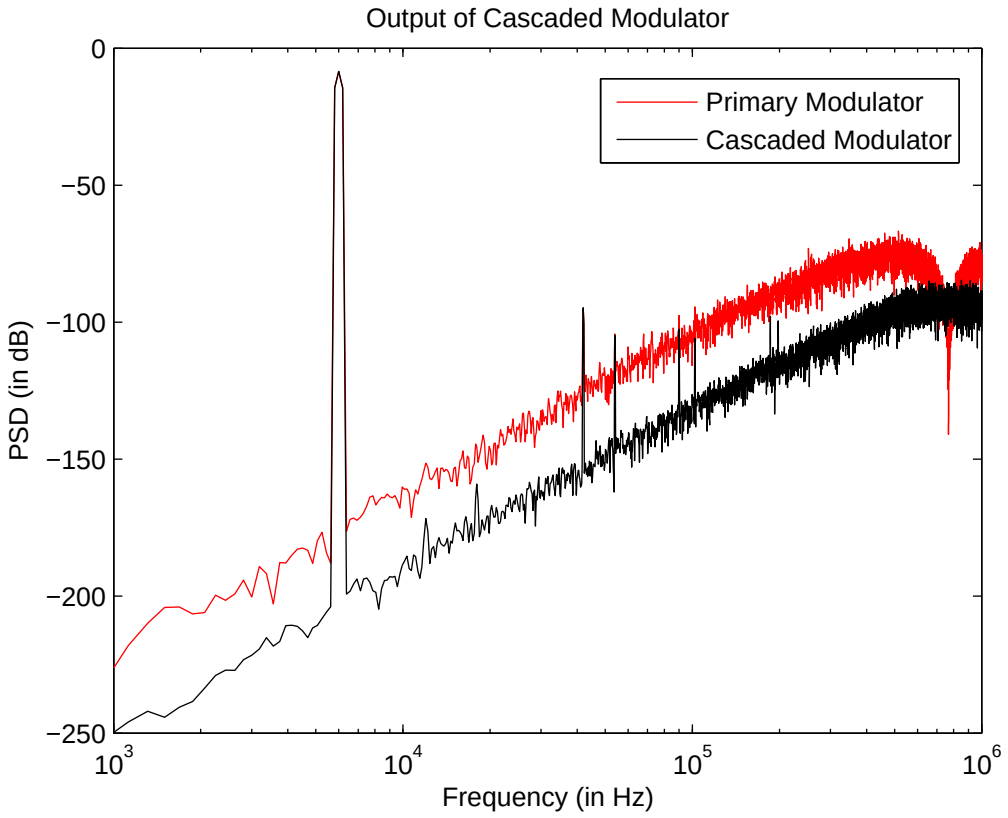


Figure 1.14: PSD at the output of the primary and secondary modulator.

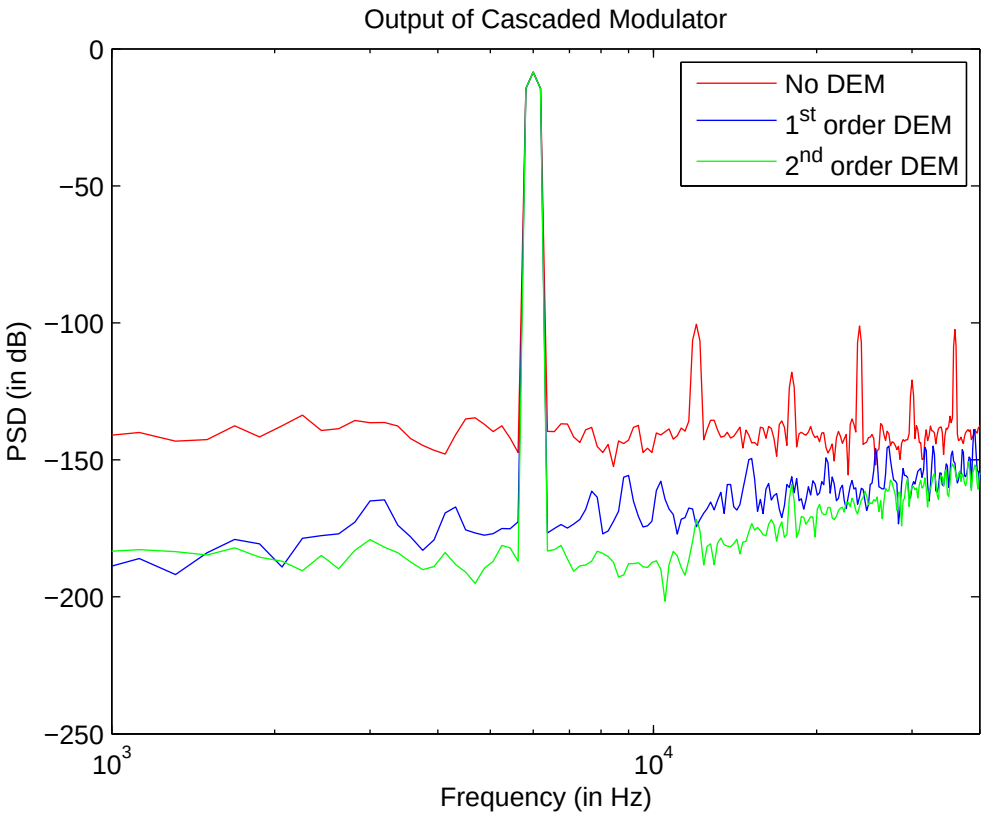


Figure 1.15: Comparison of DEM schemes

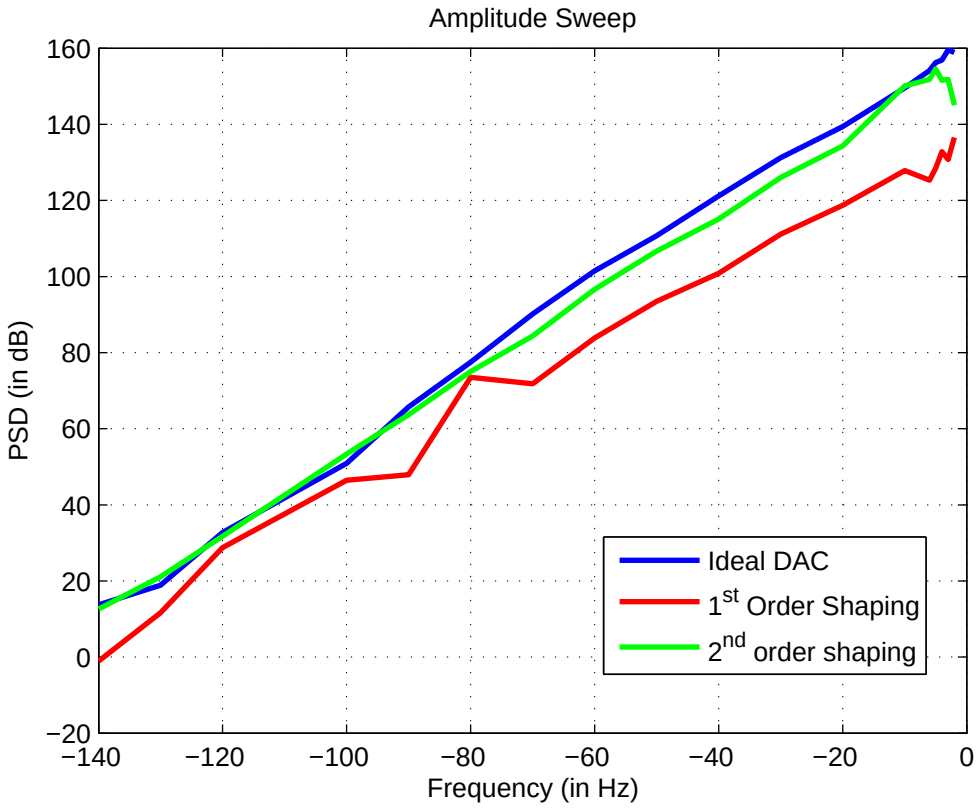


Figure 1.16: Comparison of DEM schemes

Figure 1.16 depicts the variation of SNR with amplitude. Due to the low put of band gain and large quantizer, the MSA is very high (around -0.5dBfs).

Table 1.2: SNDR with an input tone of 6kHz at -4dBfs

S. No.	Scheme	SQNR
1	Primary Modulator	119dB
2	Cascaded FIR modulator (k=24)	146dB
3	2 with thermometer coded DAC	93dB
4	2 with DWA	133 dB
5	2 with 2nd Order DEM ($MTF(z) = (1 - z^{-1})^2$	143dB

Table 1.3: Area and Power numbers

Area	$0.45mm^2$	Power	$250\mu W$
Interpolator	60%	Interpolator	44%
Digital Delta-Sigma	16%	Digital Delta-Sigma	30%
DWA	8%	DWA	17%

1.8 Future Work

This chapter only deals with the design of the Digital section in a Delta-Sigma DAC. This multi-bit DAC usually drives a pair of analog primary and secondary DACs. A complete design would include the analog front end as well.

1.9 Conclusions

The digital backend of a delta-sigma DAC was designed and synthesized. Simulation results were presented. The SQNR achieved was 120 dB with a 0.1% element mismatch. The modulator operates at a rate of 3.072 MHz. The effect of different mimatch shaping techniques was investigated.

CHAPTER 2

Part II - Design of a Dual-SCRZ CTDSM

2.1 Introduction

Oversampling Data Converters are the ADC architecture of choice when processing low frequency signals that need to be resolved to a very high resolution. Continuous-time Delta-Sigma modulators have the added advantage of the implicit anti-aliasing obtained by embedding the continuous time Loop-Filter within the Delta-Sigma loop.

2.1.1 Motivation

The CTDSM described in 4 introduces the Switched-capacitor Return to Zero DAC that alleviates the dual problems of clock-jitter as well as Inter-symbol interference in the feedback network of a CTDSM. Clock-jitter in the DAC path leads to an increase in the noise floor, while inter-symbol interference causes even harmonic distortion at the output of the CTDSM. Switched capacitor DACs however, are prone to disrupting the anti-aliasing advantage offered by CTDSMs.

An extension to this idea is a modification of the DAC so that, the DAC waveform is a switched capacitor dual-RZ waveform (SC-DRZ). Using a switched capacitor-dual RZ DAC reduces the peak current that the first amplifier of the CTDSM needs to support and recovers the anti-aliasing properties of the CTDSM.

2.1.2 Design Specifications

The design specifications for the CTDSM are shown in Table 2.1. The specifications targeted are the same as in 4.

Table 2.1: Design Specifications for CTDSM

Signal Bandwidth	2 MHz
Sampling Rate	256 MHz
Resolution	15 bit
DAC pulse shape	Switched Capacitor Dual RZ
Technology	UMC 180nm

2.1.3 Switched-Capacitor Return to Zero DAC

The switched capacitor return-to-zero DAC was first proposed in 4. It provides the dual advantages of the jitter tolerance of switched capacitor DACs as well as the improved linearity of Return-to-Zero DACs.

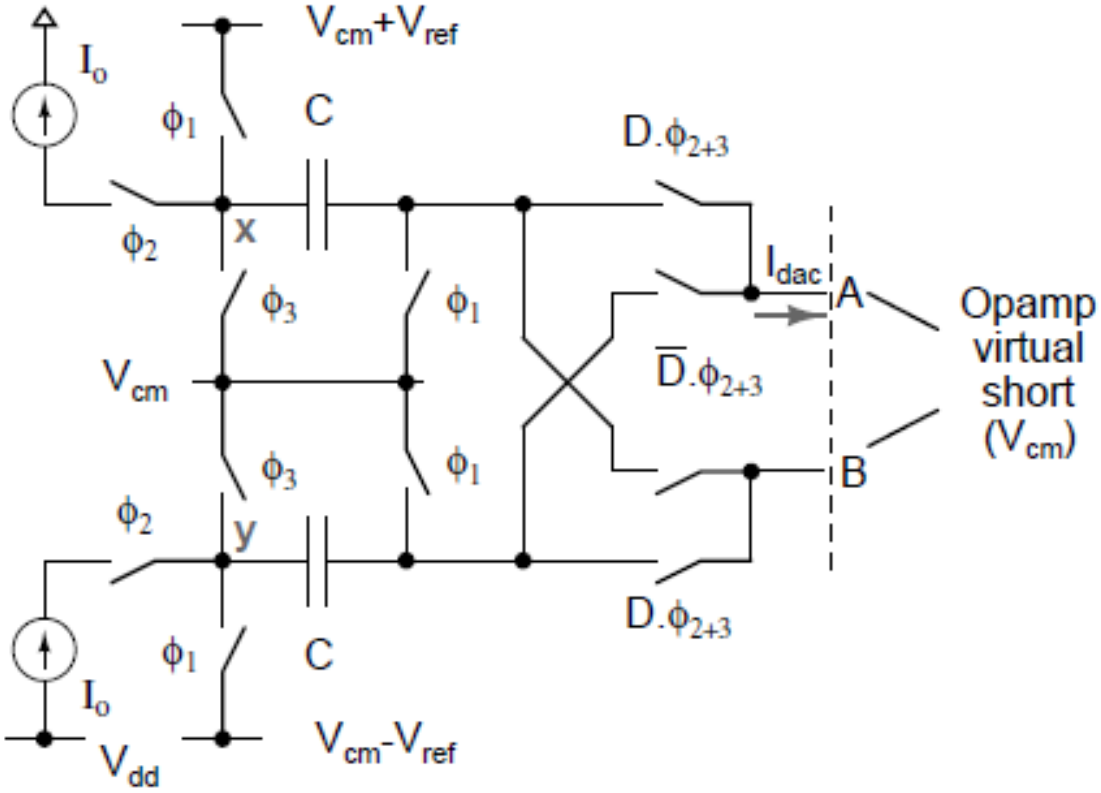


Figure 2.1: Structure of an SCRZ DAC (from 5)

Figure 2.1 shows an SCRZ DAC as described in 5. The operation of the DAC is divided into three phases. The first phase (ϕ_1) is the charging phase, the second phase, (phi_2) is the constant current discharging phase and the third phase (phi_3) is the exponential discharging phase.

The operation of the DAC is as follows-

1) In ϕ_1, the DAC capacitors C are charged to voltages $Q_{ref} = CV_{ref}$. Since the

DAC output is open circuited at this point, the DAC output current is zero.

2) In ϕ_2, the DAC capacitors are discharged using a constant current source I_0, of a nominal value $I_0 = \frac{2 \times C \times V_{ref}}{T_s}$. This current is injected into the virtual ground node of the first amplifier. The current is injected so that the capacitors are completely discharged by the end of ϕ_2. This phase is responsible for the main difference between an SCRZ and an SC DAC as this technique is used to limit the peak DAC current output.

3) In ϕ_3, the nodes X and Y are disconnected from the current sources and shorted to V_{cm}. In this phase, the DAC is wired exactly like a switched capacitor DAC, except that under ideal DAC operation, the voltage across the capacitors is already zero.

In the presence of clock jitter, the error charge remaining in the capacitors at the end of ϕ_2 is discharged out in phi_3 and the tolerance of the switched capacitor DAC to jitter is preserved.

2.1.4 Switched Capacitor Dual Return to Zero DAC

The Switched Capacitor Dual Return to Zero DAC is an extension of the SCRZ DAC. The Dual RZ waveform is composed of two half-RZ waveforms that are time shifted with respect to each other by $\frac{T_s}{2}$. The resulting DAC waveform is similar to an NRZ waveform. The dual RZ waveform trades-off smaller peak current for DAC complexity. It retains the immunity to ISI of the individual half-RZ waveforms. It also recovers the anti-alias properties of the CTDSM.

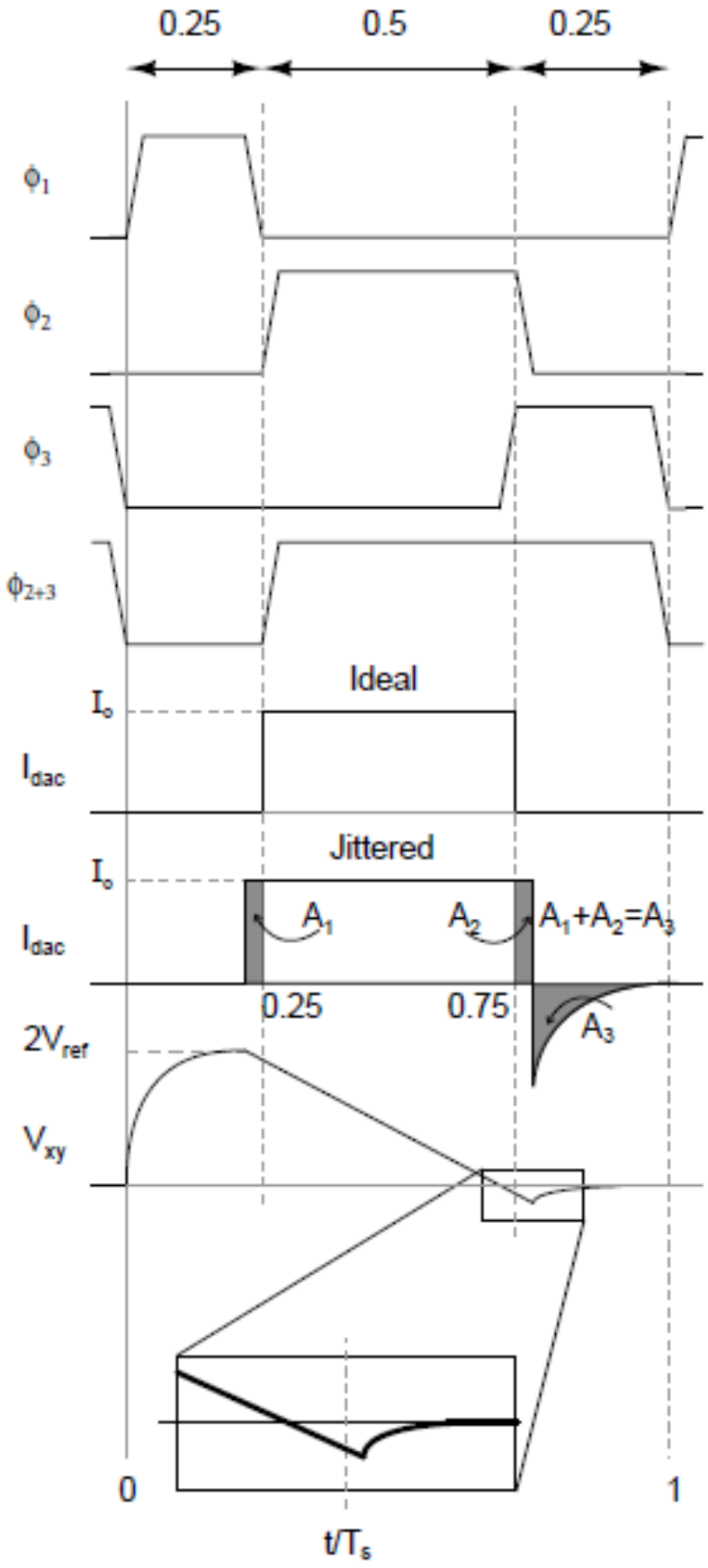


Figure 2.2: SCRZ DAC clocking (from 5)

2.1.5 Design of the Loop Filter

The NTF chosen was a fourth-order NTF with an OBG of 1.65 and one optimized zero. With a signal bandwidth of 2 MHz and a sampling frequency of 256 MHz, the OSR is 64.

The NTF that is to be realized is obtained from the $\Delta\Sigma$ toolbox in MATLAB as-

$$NTF(z) = \frac{(1 - 2z^{-1} + z^{-2})(1 - 1.998z^{-1} + z^{-2})}{(1 - 1.391z^{-1} + 0.494z^{-2})(1 - 1.617z^{-1} + 0.7428z^{-2})} \tag{2.1}$$

The NTF adopted with a single-bit feedback DAC exhibits an MSA of 0.48 and an peak SQNR of 104 dB from MATLAB simulations.

The loop filter is designed so that the sampled impulse response of the continuous time loop filter matches as closely as possible with the discrete time impulse response of the required discrete time loop filter. The coefficients are so chosen that the loop filter is adequately compensated for the excess loop delay of the feedback circuitry of the modulator. This requires a direct path component from the output of the quantizer to the output of the Loop Filter.

The implementation of the Loop Filter is as a CIFF structure as shown in Figure 2.3, as a cascade of integrators. The final stage integrator plays the dual role of an integrator and a summer op-amp. The paths in blue through C1, C2, C3 are the feed-forward paths that decide the contribution of the different integrator paths to the final Loop Filter transfer function. The path in green forms a high-Q biquad for realizing the optimized zero. The path through C0 is a direct feedback path that is required for compensating the Loop Filter.

The values of the loop filter elements are as follows-
$R1 = 5.33k\Omega$, $R2 = 7.5k\Omega$, $R3 = 45k\Omega$, $R4 = 277k\Omega$,
$C1 = 8.77pF, C2 = 721fF, C3 = 270fF, C4 = 236fF$
$Ca = 190fF, Cb = 114fF, Cc = 91fF, C0 = 13fF$,
$Rf = 975k\Omega$

The Loop Filter opamps are all designed as two stage opamps with a telescopic first stage, utilizing the high-gain of the topology. The opamps are feedforward compensated with the feedforward transconductors sharing current with the second stage transconductors.

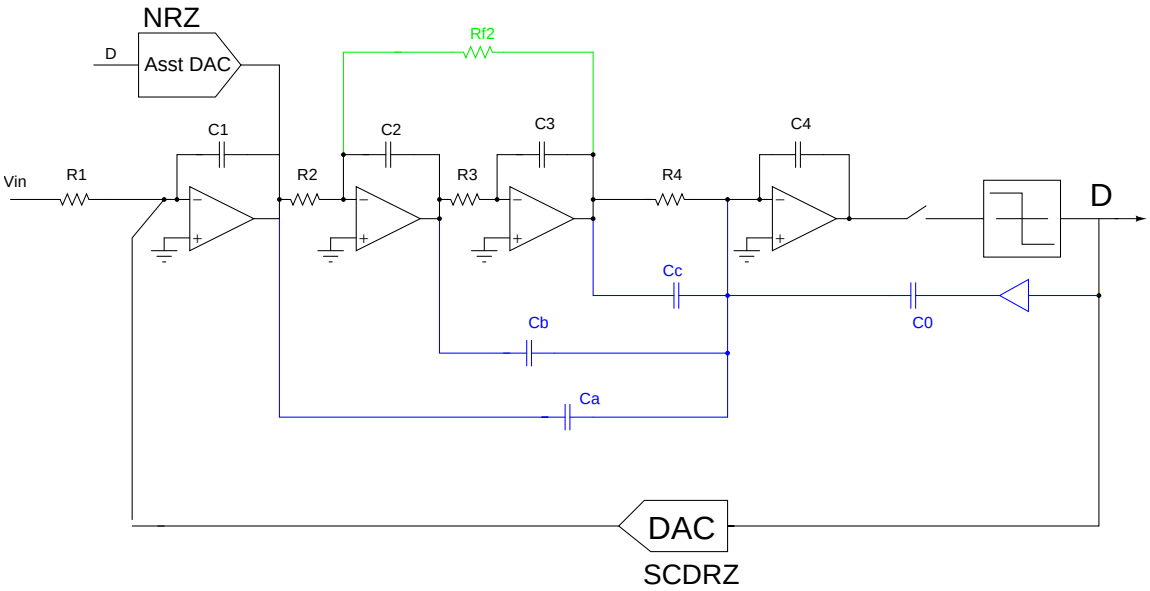


Figure 2.3: Continuous time Delta-Sigma Modulator structure

2.2 Work done

The SCRZ DAC based CTDSM from 5 was modified to a dual SCRZ structure along with layout changes. The schematic design and layout were both completed. However, there were some issues with simulations in some of the corners with the layout extracted design. The correctness of the co-efficient tuning across process corners in the layout extracted view and the common-mode stability of the opamp were a couple of the problems.

CHAPTER 3

Ring Amplifier

3.1 Introduction

3.1.1 Motivation

Advancements in process technology has been the driving force for miniaturized circuitry occupying smaller area and burning lesser power. Unfortunately, the inability to scale supply voltages at a suitable rate has put limits on MOSFET scaling. The difficulties in supply scaling are even more so difficult in analog circuit design because most of analog design still relies on transistors operating in saturation. Analog circuits are also routinely designed with multiple stacked transistors which need a higher voltage supply to support their circuit operation.

The challenges of designing accurate efficient transistors operating from low voltage supplies is well known. With reducing supply voltages, the difficulty in supporting amplifiers with high gain and/or output swing has only increased. As a result, circuits which have relied heavily on amplifiers, like pipelined ADCs do not scale as well as others not requiring amplifiers, into advanced nodes.

The ring amplifier is an amplifier topology - a derivative circuit of the ring oscillator, that partially overcomes this problem. It is a simple amplifier topology, designed using cascaded inverters which adopts scalability of digital circuits. It is capable of nearly rail to rail output swings and can be constructed simply using a few inverters and capacitors.

3.2 Basics

3.2.1 From the Ring Oscillator to the Ring Amplifier

A ring oscillator is a an odd number of cascaded inverters forming a closed loop, so that they exhibit oscillations. The oscillatory behaviour of a ring oscillator in steady state is

attributed to the fact that the oscillator exhibits a negative phase margin. The ring oscillator can be stabilized by adding a compensation capacitor, either at the output nodes of one of the inverters or as a miller capacitor across one of the inverters. However, this can severely degrade the slew-rate and the bandwidth of the inverter. The ring amplifier is an implementation of a ring oscillator like structure which is capable of dynamic biasing so that it can be stabilized without compensating the slew or bandwidth while stabilization.

The ring amplifier has poles that dynamically shift as the ring amplifier operates, so that, whilst settled, the ring amplifier looks like a well compensated single pole amplifier with an extremely low 3-dB Bandwidth. While stabilizing however, the dominant pole shifts and the slew rate and bandwidth are as dictated by a conventional 3 stage inverter. It has the advantages of the 3 stage gain offered by the ring oscillator and is stable without the necessity for an unreasonable compensation capacitor at the output.

3.2.2 Structure

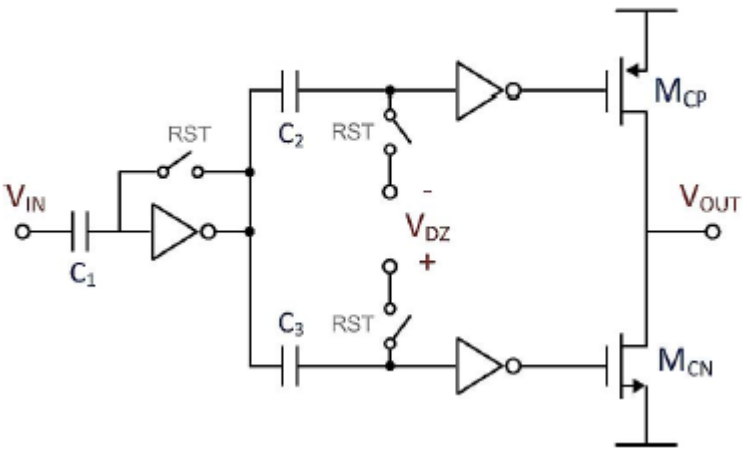


Figure 3.1: Structure of the Ring amplifier (From 6)

The ring amplifier in Figure 3.1 is essentially a ring oscillator biased so that, for a certain range of the input voltage, both the output transistors M_{CN} and M_{CP} are cutoff. The range of input values for which both MOSFETs are non-conducting is referred to as the dead zone. This is in direct contradiction with a ring oscillator, where when one of the final stage MOSFETs is in subthreshold, the other MOSFET has a large enough overdrive to be biased in triode or saturation. The width of the dead zone for a

ring amplifier with reasonably high second stage voltage gain is nearly the total offset between the caps C2 and C3. The input referred value of the dead zone is a function of the dead zone applied and the gain of the first inverter.

3.2.3 Functioning of the Ring Amplifier

A ring amplifier with a large enough dead zone will respond to impulse steps by slewing to, stabilizing and finally locking into the deadzone.. With a ring oscillator with no deadzone, the oscillator never locks. With a smaller deadzone, the stabilization takes longer. The analysis of the stabilization and locking aren't straightforward to analyze as they are large-signal processes and highly signal dependent. The ring amplifier may move between triode, saturation and deep subthreshold while stabilizing. Because of the inherent large signal behaviour, the same ring amplifier may operate in two different conditions (triode and saturation for instance) for two different inputs before stabilizing.

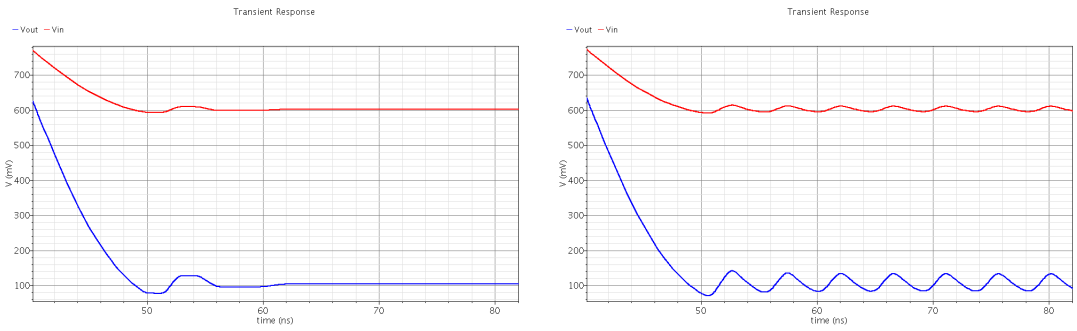


Figure 3.2: Output waveform of Ring Amplifier

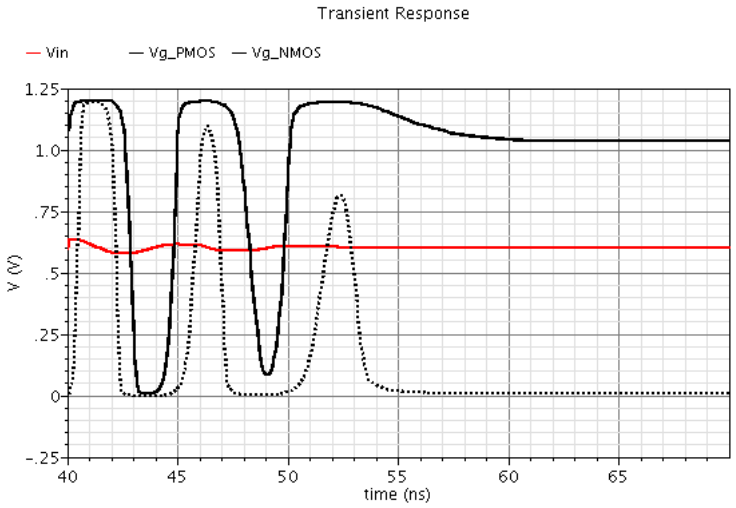


Figure 3.3: Internal Node signals

3.2.4 Initial Slewing

In response to an input step, the ring amplifier initially charges the output capacitor by slew-based charging. In Figure 3.2, this is the region between 40ns and 50ns. Both the gate voltages of the NMOS and the PMOS are close to Vdd. The PMOS is cut off and the NMOS starts off at the edge of triode and finally operates in deep triode. For a given drain voltage, the output transistors are charging the capacitor as fast as can be done. This form of charging is highly efficient because of the absence of any static power dissipation. The rate of charging drops if the output voltage approaches the rails as the charging MOSFETs are in deep triode. One would expect the output voltage (and hence the virtual ground voltage) to overshoot because of the finite loop delay. This causes the feedback direction to change and causes the amplifier to ring.

After the initial ramping stage, the amplifier starts ringing because of the delay of the amplifier loop. Depending on the deadzone width, the output capacitance, the output voltage and the inverter gains, the ringing may turn into oscillations or may die down soon. For instance, the Figure 3.2, the figure on the left, depicts the response when the deadzone is large enough so that the ringing dies down in a couple of cycles. The figure on the right is the other extreme where the amplifier starts oscillating because of the non-existence of a deadzone.

3.2.5 Ringing and Stabilization

A closer look at the first plot in Figure 3.2 and Figure 3.3 gives some insight as to how the oscillations die down. The presence of the deadzone decouples the voltage driving the gates of the NMOS and PMOS. In the case where the embedded offset in C2 and C3 is zero, the gate voltages driving the output transistors are equal and while one transistor is off, the other is necessarily on. By embedding the dead zone, we create a scenario (for instance between 50ns and 51ns in Figure 3.3) where both the NMOS and PMOS are in deep subthreshold. This causes the amplifier to momentarily have a highly reduced bandwidth because both the output transistors are operating in subthreshold. This cuts off the amount of ringing the amplifier can sustain and the fedback signal starts diminishing in magnitude The "plateaus" in the first plot of Figure 3.2 are caused by this effect. As the feedback becomes smaller and smaller, the plateaus

grow larger until the fedback signals amplitude grows smaller than the input referred deadzone. In this state, the output MOSFETs are cut-off for the whole cycle and the amplifier settles.

3.3 Design Methodology

3.3.1 Settling Accuracy

The settling accuracy is determined by the magnitude of the embedded offset and the gain of the first stage. The input referred deadzone is given to a good approximation by $V_{DZ} = \frac{V_{OS}}{A_1}$, where V_{OS} is the embedded offset stored across the capacitors and the voltage gain of the first inverter is A_1. High Gain Ring Amplifiers with nearly non-existent dead zones, have their settling accuracy determined by the three-stage gain rather than the dead-zone. Settling Accuracy for low-accuracy Ring Amplifiers can be traded-off for stability benefits.

3.3.2 Speed

The maximum frequency of operation is a function of both the ramping time and the settling time. For large input steps, the ramping time is dominant and is given by $t_{ramp} = \frac{C_{load}+0.5C_{in}}{I_{ramp}} \times V_{out}$, where V_{out} is the output settled voltage, C_{load} is the load capacitance and C_{in} is the input capacitance. For smaller input steps, the time taken for stabilization is usually dominant. There is a trade-off between the ramping time and settling time. A larger output voltage slew (Larger peak current and smaller output capacitance) aids faster ramping at the cost of settling time as the effective amplifier gain increases with the slew rate.

3.3.3 Stability

The stability is closely related to the time taken for stabilization. A larger deadzone, a larger load capacitor and a weaker output stage transistors aid stability. The stability should be ensured for smaller input steps where the output transistors operate well

out of triode and their drive is maximal. The stability can be traded off for accuracy (deadzone width), speed (by changing the load capacitor). One important consideration for stability is the amount of time the amplifier stays in the deadzone. If the amount of time spent in the deadzone is a significant fraction of the loop delay, the oscillations eventually die down.

3.4 Analysis of the Trajectory

The ring amplifier itself, (unlike an opamp) is a highly non-linear block and because of its application as a switched capacitor amplifier, the transient signals necessarily cannot be treated as small signals about an operating point. Moreover, the stabilization of a ring amplifier occurs when the output voltage settles into the deadzone, a region where both the output MOSFETs settle in the subthreshold region. The ramping and stabilization, however, occur when at least one of the MOSFETs is switched on. This means, that because of the varying operating point, a small signal analysis is rendered almost useless. There is a need to model the amplifier so that the model is sufficiently complex to incorporate the nuances of operation and predict the steady state trajectory, while at the same time, the model should be sufficiently simple, so as to allow an analytical study of the waveforms involved.

3.4.1 Modelling

The Ring Amplifier can be modelled in many ways. The most intuitive way to model it, is to model each of the inverters in the Ring amplifier individually and cascade them to get the overall ring amplifier performance. It is also likely that such a model will be a very accurate model if the large signal behaviour of the inverters is modelled as well. However, a more simplistic approach to modelling would be to treat the ring amplifier as a large signal VCCS, with a defined input-output characteristic, taking into account the deadzone as well as the peak current saturation, treating the ring amplifier as a black box. Some intuition as well as analytic understanding can be gained by treating the amplifier as a blackbox without getting distracted by the internal workings of the amplifier. Knowing the stimulus, one can always plot the internal signals of the amplifier.

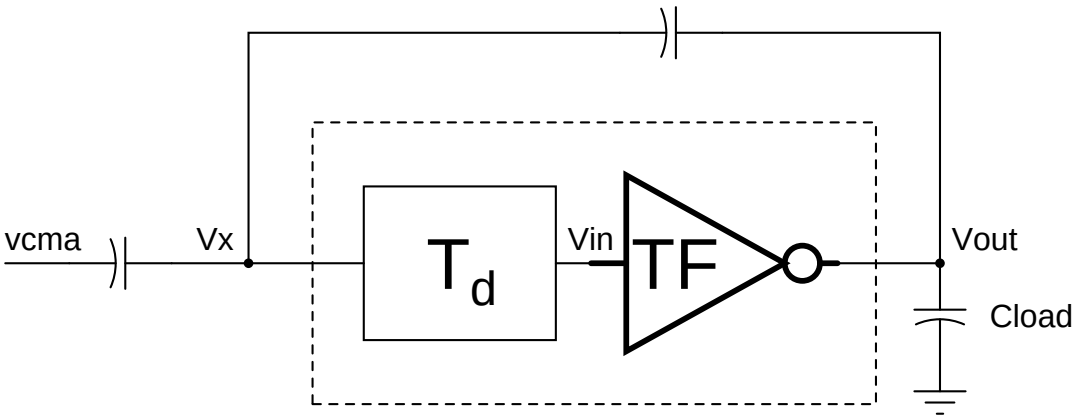


Figure 3.4: Model of the Amplifier

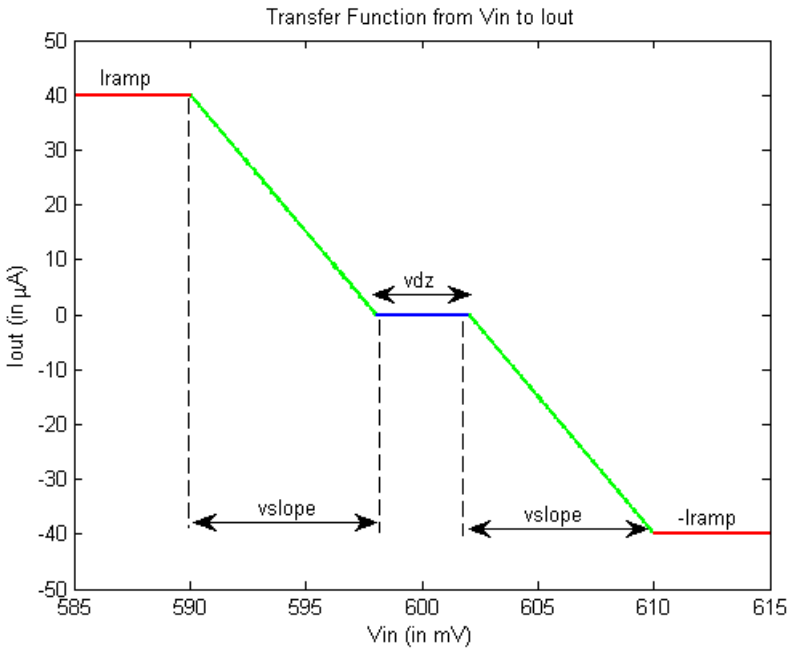


Figure 3.5: Proposed V-I characteristics

3.5 Preliminaries

The models proposed below have been solved in MATLAB and solutions have been plotted and analyzed. The nature of the model proposed compels us to solve a set of delay differential equations to estimate the voltage waveform with respect to time. However, wherever applicable, simplifying assumptions have been made and justified. The precise equation that needs to be solved for obtaining the output waveform as a function of time is given by

$$dV_{out} = \psi \frac{I_{out}(V_{in}(t))}{C_{load}} \times dt \tag{3.1}$$

Substituting V_{in} in terms of V_x, we obtain

$$dV_{out} = \psi \frac{I_{out}(V_x(t - T_d))}{C_{load}} \times dt \tag{3.2}$$

By applying charge conservation at the virtual ground node, we also have,

$$V_x = \frac{V_{cm}}{2} - V_{samp} + \frac{V_{out}}{2} \tag{3.3}$$

where V_{cm} is the common mode voltage and V_{samp} is the voltage sampled across the input capacitor in the sampling phase of the operation. In the ideal settled case, V_{out} settles to $V_{cm} + 2 \times V_{samp}$, thus ensuring that the virtual ground node settles to the common mode voltage. Voltages V_x, V_{in} and V_{out} are as depicted in Figure 3.4. The function $I_{out}(V)$ is as described in Figure 3.5. ψ is the fraction of the output current of the amplifier that flows into the capacitor and is given by $\frac{C_{load}}{C_{load}+0.5\times C_{in}}$, where C_{in} is the sampling capacitor of the SHA/MDAC.

Solving Equations 3.2 and 3.3, we obtain the voltage at the output node (or the virtual ground node) as a function of time. Unfortunately, this exercise is complicated by the presence of the delay element.

3.6 Stability Analysis

Consider a Ring Amplifier modelled according to the Figure in 3.4. Criteria for stability can be obtained by finding upper and lower bounds for the loop delay over which the amplifier will be stable. A lower bound has been obtained, below which stability is guaranteed and an upper bound for the time delay, beyond which instability guaranteed. Consider the extreme cases where the $v_{slope} = 0$ and where $v_{dz} = 0$. The first case is a case where the transition between the deadzone region and slewing region is abrupt. The second case is the case of a simple linear network with delayed feedback (as long as the amplifier does not slew).

Figure 3.6 depicts plots of the voltage input to current output characteristic of the the ring amplifier in three cases. The region over which the ring amplifier does not slew is kept equal for comparison. The plot in red is indicative of the case where the

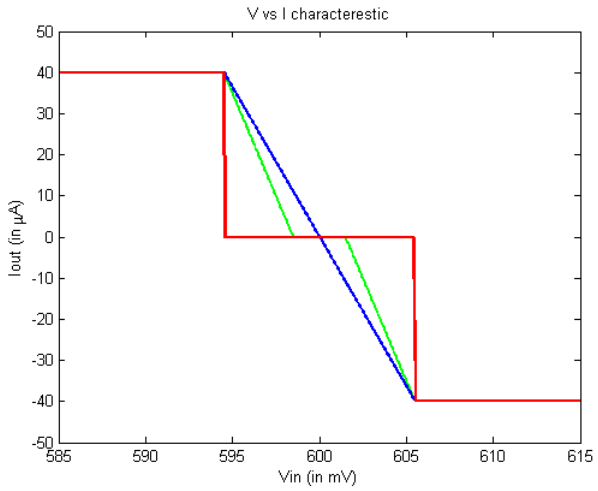


Figure 3.6: V-I characteristic for stability analysis

deadzone is maximum. The plot in blue is indicative of the case where the deadzone is zero. The plot in green corresponds to an intermediate case.

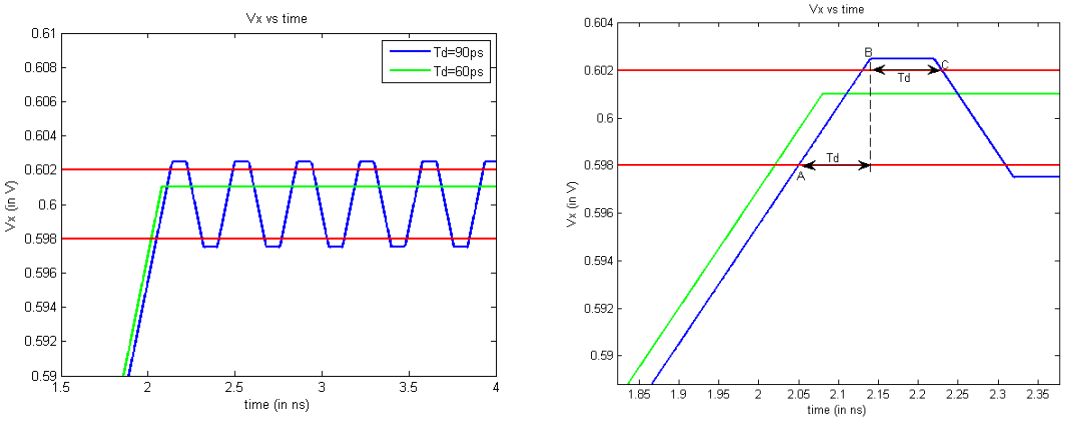


Figure 3.7: Voltage waveform when deadzone is maximum

3.6.1 Upper Bound on Time Delay

As can be seen in Figure 3.7, when the V-I characteristic follows the red curve, the output voltage waveform is piecewise linear.

With reference to the figure on the right, the overshoot of the virtual ground node voltage from the deadzone edge (ie. from A to B) is given by

$$V_{overshoot} = \frac{1}{2} \times \psi \times \frac{I_{ramp}}{C_{load}} \times T_d \tag{3.4}$$

, where the factor of half comes because of referring the output voltage back to the

virtual ground node using Equation 3.3. It can be shown that in the event where the slewing current, both while sourcing and sinking are equal, if the voltage overshoot at the virtual ground node is greater than the deadzone width, the amplifier cannot stabilize and exhibits perpetual oscillatory behaviour. This can be understood by noting that the time difference between points B and C is also T_d. This means, that after the feedback kicks in, the overshoot in the virtual ground node voltage will be given by the same expression as before and the virtual ground node will never settle into the deadzone.

If the time delay is small enough that the feedback kicks in before the whole of the deadzone is traversed, the settling takes place without any oscillations. The settled error in this case is given by -

$$V_{err} = \frac{1}{2} \times \psi \times \frac{I_{ramp}}{C_{load}} \times T_d - \frac{V_{dz}}{2} \tag{3.5}$$

Thus, a necessary condition for stability is given by $T_d < 2 \times \frac{V_{dz} \times C_{load}}{\psi \times I_{ramp}}$ In the event that the peak sourcing current and sinking current are unequal, the stability criterion is determined by the smaller of the two currents, thus allowing for a larger loop delay.

It is easy to reason that because of the larger deadzone, a ring amplifier characterized by the red curve will be more easily stabilized than a ring amplifier characterized by the green curve. Thus, we can conclude that an upper bound on the time delay for stable operation of a general ring amplifier is given by

$$T_{upperbound} = 4 \times \frac{C_{load}}{I_{ramp}} \times (v_{slope} + \frac{v_{dz}}{2}) \tag{3.6}$$

3.6.2 Lower Bound on Stability

A lower bound can be obtained by finding a stability bound for the ring amplifier modelled by the blue characteristic in Figure 3.6. Since, as long as the amplifier does not slew, a linear model can be used to describe the characteristic, a bound is obtained by using linear control theoretic approaches. From Equations 3.2 and 3.3, it is apparent that the delay differential equation describing the amplifier response is given by-

$$2 \times C_{load} \times \frac{dV_x(t)}{dt} = -k \times \frac{dV_x(t - T_d)}{dt} \tag{3.7}$$

where k is the slope of the I-V characteristic Writing this in the s-domain, we get the relation,

$$2 \times s \times C_{load} \times V_x(s) = -k \times V_x(s) \times e^{-T_d} \tag{3.8}$$

Expressing s as a generalized complex variable $s = \lambda + j\omega$ and separating out the real and imaginary sub-equations, we get,

$$2 \times \lambda \times C_{load} + k \times e^{-\lambda T_d} cos(\omega T_d) = 0 \tag{3.9}$$

$$2 \times \omega \times C_{load} - k \times e^{-\lambda T_d} sin(\omega T_d) = 0 \tag{3.10}$$

Placing the constraint that $\lambda < 0$ to guarantee stability, we obtain from Equation 3.9,

$$cos(\omega T_d) > 0 \tag{3.11}$$

Thus,

$$T_d < \frac{\pi}{2 \times \omega} \tag{3.12}$$

Similarly, in the limit that λ goes to zero, we obtain from Equations 3.9 and 3.10,

$$\omega = \frac{k}{2 \times C_{load}} \tag{3.13}$$

Thus, we obtain that

$$T_d < \frac{\pi \times C_{load}}{k} \tag{3.14}$$

Recognizing that the ring amplifier characterized by the blue curve will always have a tighter condition for stability (because of the absence of a deadzone) as compared to the one characterized by the green curve, we conclude that this provides a lower limit on the time delay, below which stability is guaranteed. By appropriately substituting for k, we obtain

$$T_{lowerbound} = \pi \times \frac{C_{load}}{I_{ramp}} \times (v_{slope} + \frac{v_{dz}}{2}) \tag{3.15}$$

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