MODELING OF CHARGES AND CAPACITANCES IN SOI-LDMOS TRANSISTORS

A Project Report

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THESIS CERTIFICATE

This is to certify that the thesis titled **Modeling of Charges and Capacitances in SOI-LDMOS Transistors**, submitted by **Prasad Sarangapani**, to the Indian Institute of Technology, Madras, for the award of the degree of **Master of Technology and Bachelor of Technology (Dual Degree)**, is a bona fide record of the research work done by him under our supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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ABSTRACT

KEYWORDS: LDMOS; Compact Modeling; Capacitances; Charge Partition.

Lateral double diffused MOSFET (LDMOS) has garnered a lot of interest these days due to its ease of integration with low voltage circuitry to form high voltage integrated circuits (HVICs), capable of handling hundreds of volts. Designing HVICs require accurate LDMOS models capable of predicting parameters over wide ranges of voltages and temperatures. In recent years, LDMOS has been integrated into RF circuits and this calls for accurate prediction of DC and high frequency behavior. Hence modeling DC static currents and capacitances is essential.

In this thesis, a physics based compact model for SOI-LDMOS is presented which aims to accurately predict various capacitances and static currents in the device. Various capacitances are realized by modeling the charges present in the device and by partitioning them across various terminals. MM20 HVMOS is a standard LDMOS model which provides a partitioning scheme in LDMOS known as Modified Ward-Dutton partition. Arguing from continuity and current equations, we show that such a partition function will be physically inconsistent and provide an alternative partition function for LDMOS.

Comparison of the model with device simulation show that the model exhibits reasonable accuracy over a wide range of bias voltages. Several reasons are provided for the inaccuracies in the capacitance plots and methods are proposed to mitigate them.

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ABBREVIATIONS

MOSFET	Metal Oxide Semiconductor Field Effect Transistor
SOI	Silicon On Insulator
BOX	Buried Oxide
LDMOS	Lateral Double Diffused MOS
VDMOS	Vertical Double Diffused MOS
HVIC	High Voltage Integrated Circuit
RFIC	Radio Frequency Integrated Circuit
JFET	Junction Field Effect Transistor
NMOS	N-channel MOSFET
PMOS	P-channel MOSFET
DC	Direct Current
AC	Alternating Current
WD	Ward-Dutton
MWD	Modified Ward-Dutton

NOTATION

V_{GS}	Gate to source voltage
V_{GB}	Gate to bulk voltage
V_{GC}	Gate to quasi-Fermi level voltage
V_{DS}	Drain to source voltage
V_{DiS}	Voltage drop across channel
$V_{D'D_i}$	Voltage drop across drift region under gate oxide
$V_{DD'}$	Voltage drop across drift region under field oxide
$V_{sat,ch}$	Channel saturation voltage
$V_{sat,dr}$	Reg-II saturation voltage
$V_{DiS,eff}$	Effective voltage drop in channel
$V_{D'D_i,eff}$	Effective voltage drop in Reg-II
I_{DS}	Drain to source current
I_{ch}	Channel region current
I_{dr}	Current in Reg-II
I_{dr1}	Current in Reg-III
L_{ch}	Length of channel region
L_{dr}	Length of Reg-II
L_{LC}	Length of Reg-III
W	Width of LDMOS
C_{ox}	Oxide capacitance
t_{ox}	Oxide thickness
A	Cross section area of LDMOS
t_{si}	Silicon film thickness
t_{BOX}	Thickness of buried oxide
N_{dr}	Doping concentration in Reg-II
V_T	Thermal voltage
ϵ_{si}	Permittivity of silicon
ψ_s^{ch}	Surface potential in channel
ψ_s^{dr}	Surface potential in Reg-II
Q_{inv}	Inversion charge per unit area in Reg-I
Q_{gate}^{ch}	Gate charge in Reg-I
Q_n^{dr}	Total drift charge per unit area in Reg-II
Q_{acc}^{dr}	Accumulation charge per unit area in Reg-II
Q_{dep}^{dr}	Depletion charge per unit area in Reg-II
Q_{inv}^{dr}	Inversion charge per unit area in Reg-II
Q_{gate}^{dr}	Gate charge in Reg-II
n_{ch}	Charge density in Reg-I
n_{dr}	Charge density in Reg-II
Q_G	Charge assigned to gate terminal
Q_D	Charge assigned to drain terminal
Q_S	Charge assigned to source terminal

Q_B	Charge assigned to bulk terminal
Q_{D_i}	Charge assigned to D_i terminal
$Q_{D'}$	Charge assigned to $D^{'}$ terminal
τ	Time lag between conduction currents in Reg-I and II
V_{FB}^{ch}	Flat band voltage in channel
V_{FB}^{dr}	Flat band voltage in Reg-II
v_{sat}	Saturation velocity of electrons
μ_{ch}	Effective mobility in channel
μ_{dr}	Effective mobility in Reg-II
μ_{dr1}	Zero field mobility in Reg-III
$\theta_{3,ch}$	Velocity saturation parameter in channel
θ_1	Channel mobility reduction parameter
θ_2	Channel mobility reduction parameter
$\theta_{3,dr}$	Velocity saturation parameter in Reg-II
θ_{dr1}	Velocity saturation parameter in Reg-III
$\theta_{1,dr1}$	Velocity saturation parameter in Reg-III
λ_{ch}	Channel length modulation parameter
λ_{dr1}	Drift length modulation parameter
C_{ij}	Capacitance between terminals i and j

CHAPTER 1

INTRODUCTION

1.1 Overview of power semiconductor devices

Power semiconductor devices have become industry's choice today in designing high voltage integrated circuits (HVICs). They have come a long way since the inception of bipolar junction transistors and thyristors. They were initially introduced by Texas Instruments in 1954 but it took almost a decade for them to find practical applications in high voltage circuits. Thyristors were the first class of power devices but they had the disadvantage of poor switching speed and difficulty of integration. Advances in silicon fabrication technology let to the development of novel device structures such as power MOSFETs. These devices were introduced in late seventies (Adler *et al.*, 1984) and they paved way for the development of new generation of devices. The power MOSFETs were developed by converting a conventional MOSFET into an asymmetric device to improve the reverse blocking capability of the device(Declercq and Plummer, 1976). This ultimately led to the creation of lateral double diffused metal oxide semiconductors (LDMOS) transistors.

One of the main advantages of LDMOS devices is that they can be easily integrated with low voltage circuitry and continue to be industry standard even today for medium voltage power applications. On the other hand, they suffer from low current rating and breakdown voltage on-resistance trade off. To increase the voltage handling capabilities of this device, one has to increase the length of lightly doped drain region across which the reverse voltage is dropped. This increases the area requirements of the device.

To circumvent this problem, vertical double diffused MOS (VDMOS) technology was developed. VDMOS provides larger current ratings and higher breakdown voltage compared to LDMOS(Temple and Gray, 1979), but requires complicated process steps and integration with low voltage circuitry is not easy. Though VDMOS finds applications in high voltage industries, medium power applications are still dominated by LDMOS devices.

Nowadays, HVICs and power integrated circuits (PICs) are replacing discrete elements such as DC-DC converter, switch mode power supplies and power amplifiers (Sakamoto *et al.*, 1999),(Perugupalli *et al.*, 1998),(Tsui *et al.*, 1992). Integration of high and low voltage circuits on the same chip improves the overall performance and reduces the chip size. PICs are used as a bridge between power load and low voltage digital logic(Tsui *et al.*, 1995),(Baliga, 1991). They are also useful in Power line communications (PLCs) where digital information is transmitted over a power line. LDMOS devices form an integral part of many of these interesting applications.

1.2 Current scenario in LDMOS transistor modeling

As LDMOS technology is finding its use in interesting consumer and automotive applications, it becomes imperative to model LDMOS transistors. A recent trend is the processing of LDMOS devices on silicon on insulator (SOI) platform. LDMOS fabricated on SOI substrate have several advantages like lower leakage currents, higher latchup, higher packing density and reduced parasitics(Holland and Igic, 2006). SOI enables isolation between power devices and low voltage circuitry which is essential in smart power ICs. Thus compact models for SOI-LDMOS transistors capable of modeling device characteristics over wide range of bias and temperature and for various lengths is essential for a fail safe design of power integrated circuits.

There have been many approaches for modeling LDMOS transistors. Two main approaches followed are (i) macro-modeling and (ii) compact modeling. Macro modeling procedure consists of trying to describe the behavior of device through a circuit consisting of several discrete elements or modules. As the number of effects rises, the number of elements in the circuit increases and results in increase in computation time and convergence problems. There are many existing macro models based on SPICE which consider SPICE models for MOSFETs, JFETS and diodes to model LDMOS(van der Pol *et al.*, 2000),(Darwish, 1986),(Trivedi *et al.*, 1999). One such macro model uses BSIM4 to model the MOSFET and JFET to model drift region and a shorted PMOS transistors to model capacitance behavior of drift region(Yang *et al.*, 2008). These models have a large number of non-physical model parameters.

Compact modeling, on the other hand, maintains device unity through a set of self

consistent expressions which are able to produce device behavior. All internal node equations are solved in the model itself, thereby reducing computation time. Also, the expressions obtained are from physical principles and do away with non-physical parameters introduced in macro-modeling. There are several compact models available for SOI-LDMOS, important among them being HiSIM-HV (Oritsuki *et al.*, 2010), EKV model(Bucher *et al.*, 1998),(Sallese and Porret, 2000),(Chauhan *et al.*, 2006*a*) and MM20 HVMOS model(MM2, 2008). In this thesis, MM20 model developed by NXP semiconductors is used as a basis upon which further formulations have been built. It is a surface potential based model and takes into account channel and drift region under the gate oxide. It does not model the region under field oxide and hence cannot be used for high voltage devices. The effect of quasi-saturation in drift region under field oxide is considered in (Lekshmi *et al.*, 2009).

Apart from accurately predicting the DC characteristics of a device, a good model must also accurately predict various capacitances which are important for the AC characteristics of the device. With the integration of LDMOS in high speed circuits such as RFICs, predicting the high speed performance of LDMOS becomes important. In literature, there have been few detailed studies on modeling capacitances in devices such as LDMOS and SOI-LDMOS and some of them have resulted in model development(Frre *et al.*, 2001),(Aarts *et al.*, 2005),(Shi *et al.*, 2013),(Wang *et al.*, 2013). One of the basic principles used for modeling capacitances is charge partitioning. The charges are modeled accurately and then they are partitioned between different terminals of the device based on Ward-Dutton partition principle(Oh *et al.*, 1980). MM20 model uses a modified version of Ward-Dutton model to obtain various capacitances. It does not clearly explain the basis behind such a partition and charge modeling also has some inherent approximations. Also, the match obtained between the device and model simulations are not satisfactory.

Recently, (Aarts *et al.*, 2004),(Aarts *et al.*, 2006) and (Roy *et al.*, 2007) have shown that in the presence of lateral doping (which is inherently present in LDMOS) and field dependent mobility, it is not possible to obtain a partition function. This poses a big problem in modeling the capacitances. (Aarts *et al.*, 2006) and (Roy *et al.*, 2007) give a procedure to calculate the capacitance based on small signal analysis. Though the analysis is physically consistent, the final expressions obtained are extremely complex to be implemented in a compact model.

Therefore, there is a need for a comprehensive charge model which accounts for aforementioned effects. In this thesis, an extensive model to describe the static and dynamic characteristics of SOI-LDMOS is proposed. MM20 model serves as a starting point for describing various currents and charges in the device. The model considers field dependent mobility reduction, velocity saturation in channel and quasi saturation in the drift region. A modification to the MM20 charge partitioning scheme is proposed and physical reasoning behind such a partition is explained.

1.3 Objectives

The main objectives of this thesis are.

- To analyze the behavior of SOI-LDMOS in channel, drift region under gate oxide and drift region under field oxide for various gate and drain bias voltages.
- To analyze the charges present in the device and provide a physics based partition model to partition charges between various terminals.
- To predict various capacitances from the charge model thus developed.

1.4 Structure of the thesis

The thesis is organized as follows.

- **Chapter 2: Analysis of physical effects**

  This chapter deals with analysis of voltage drops in different regions along with various charges in the device. The device behavior is analyzed with the help of MEDICI simulation results.

- **Chapter 3: Model and Verilog-A implementation**

  In this chapter, compact model to explain these physical effects is proposed. The model uses MM20 model for channel and drift region under gate oxide and quasi-saturation model to model the region under field oxide. The charges are modeled according to MM20 model and a modification to the existing partition model is proposed.

- **Chapter 4: Results and discussions**

  Static models and various capacitances are compared with MEDICI simulation results. Various proposals to improve the charge model are proposed.

- **Chapter 5: Conclusions**

  Contributions offered by with work are presented. Scope for future work is listed.

CHAPTER 2

ANALYSIS OF PHYSICAL EFFECTS

The high voltage lateral MOSFET device, where the extension of the gate electrode works as a field plate, is one of the interesting structures in mainstream HV technologies. The structure of LDMOS is different from conventional MOSFET due to the presence of an extended drain region and non-uniform lateral doping in the channel region which makes its behavior complex compared to the normal MOSFET.

In this chapter, we focus on analyzing the physical effects which appear under static conditions. Firstly, the effect of gate and drain voltages on the static currents are analyzed. This analysis is useful when we explain the current formulations of various regions. Next, various charges that are present in the channel and the drift region will be studied under the application of various gate and drain bias. For the purpose of these studies, commercially available two-dimensional (2-D) device simulator MEDICI (Med, 2003) is used.

2.1 Device Structure

SOI-LDMOS is an asymmetric structure with a drift region located between the channel and the drain terminal. Schematic of the cross-section of device is as shown in Fig 2.1. The channel region is self aligned to the gate and is formed by p-type diffusion creating a p-well under the gate. This results in non-uniform doping in channel with doping concentration gradually decreasing from the source end to the other end of the channel region. The source is then formed by a n^+ diffusion. Since there are two lateral doping processes involved, this device is called as laterally double diffused MOSFET. One should note that the doping of the channel region is not constant throughout and decreases from source side to drain side. This causes complexity in current and charge modeling. The n-drift region sustains the reverse voltage and hence is lightly doped in comparison to channel. Thus, the depletion region at the junction of channel and drift region extends far more into the drift region to sustain high voltages. The gate electrode

covers the surface of the channel and part of the drift region. The gate oxide and the field oxide are of different thickness. A thicker field oxide helps in reducing the gate drain overlap capacitance and improves the speed of the device. The active part of the device is separated from the bulk by a thick buried oxide which improves dielectric isolation and minimizes parasitics.

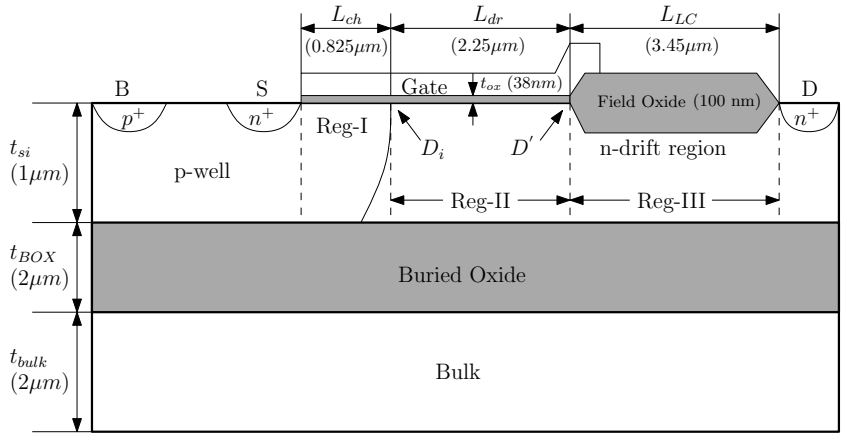

Figure 2.1: Schematic of cross section of SOI-LDMOS.

From the figure it is clear that there are three important regions marked by Reg-I, II and III. Reg-I corresponds to the channel region in the p-well, Reg-II to the drift region with the gate oxide at its surface and Reg-III to the drift region underneath the field oxide. Transition between Reg-I and Reg-II is denoted by D_i and between Reg-II and Reg-III is denoted by $D^{'}$.

The doping profile of the device along a lateral cutline close to the $Si - SiO_2$ interface is shown in Fig 2.2. Here we assume that the doping profile in the channel region is uniform though it has a lateral variation in practice. Drift region has the lowest doping to sustain high voltages. For the device under discussion, p-well has a doping concentration of $2 \times 10^{17}\ cm^{-3}$. The drift region has a doping concentration of $2 \times 10^{16}\ cm^{-3}$, ten times lower than the channel region to withstand high voltages. The length of channel region is $0.825\mu m$, length of drift region under gate oxide is $2.25\mu m$ and that under the field oxide is $3.45\mu m$. Gate oxide thickness is 38 nm and field oxide thickness is 100 nm. Total length of the device is $10\mu m$. Thickness of the active region is $1\mu m$ and thickness of buried oxide is $2\mu m$.

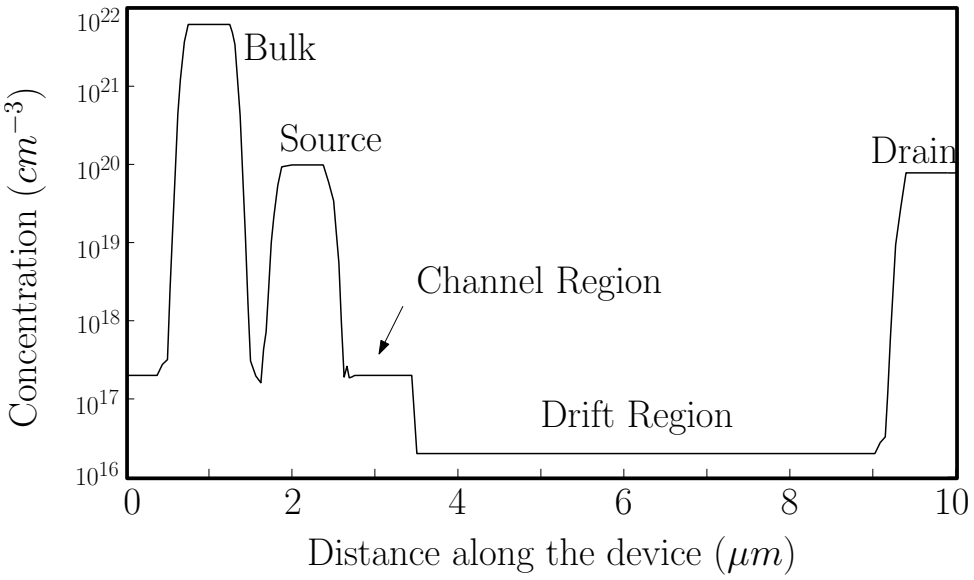

Figure 2.2: Doping profile of device along $Si - SiO_2$ interface.

2.2 Static Currents

In order to provide accurate model for the SOI-LDMOS, its electrical behavior must be thoroughly analyzed and understood. This requires separation of device structure into three distinct regions i.e. Reg-I, II and III. This separation is not physical but only to understand the model better. This helps in modeling the MOSFET currents and forms the basis for understanding various charges present in different regions. During the current and charge analysis, it is assumed that the source and bulk terminals are shorted. Hence, V_{GS} and V_{GB}, V_{DS} and V_{DB} are used interchangeably. Current modeling has been dealt in great detail in (Lekshmi, 2009) and (Radhakrishna, 2011). This thesis tries to explain the current modeling in a concise manner and gives some modifications and explanations for better clarity.

When V_{GS} is greater than the threshold voltage of the channel, electrons are attracted to form an inversion layer[1]. Since there is a gate overlap in the drift region, an accumulation region is formed. Now, if V_{DS} is applied, electrons move from the source terminal through the inversion layer in Reg-I into Reg-II and will drift through the accumulation region into Reg-III and finally into drain contact.

Potentials drops across Reg-I, II and III are studied to explain the $I_d - V_{DS}$ charac-

[1]Since doping in channel is assumed to be constant, threshold voltage is same throughout the channel. In practice, threshold voltage varies across the channel from source to drain due to lateral doping.

teristics of the device as shown in Fig 2.3.

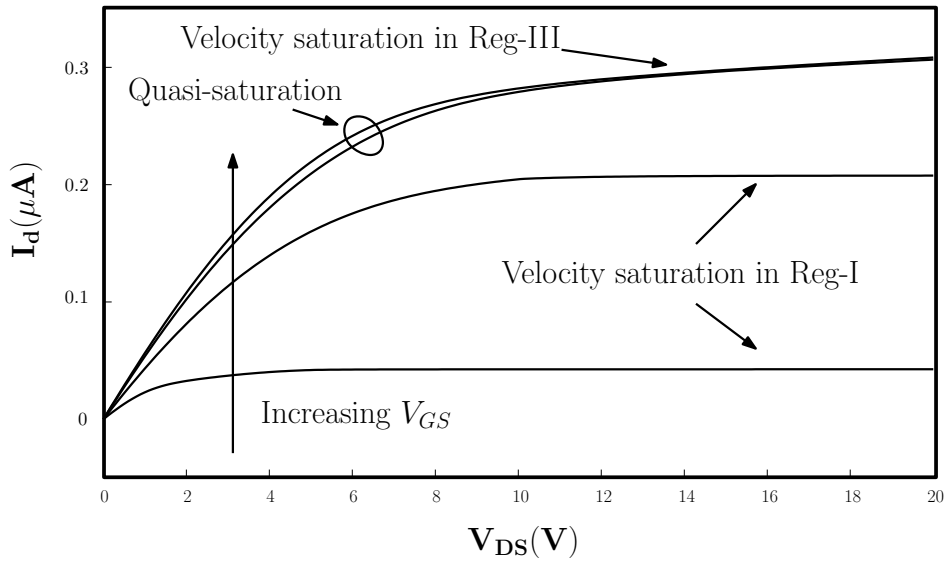

Figure 2.3: $I_d - V_{DS}$ plots simulated for V_{GS} = 5V, 10V, 15V and 20V, in MEDICI.

2.2.1 Potential drop in Reg-I

For low values of V_{GS}, as V_{DS} is increased, drop across the channel increases. This is because Reg-II is already in accumulation condition and has high conductivity. As V_{DS} is increased further, the lateral electric field in this region increases and reaches the critical value. Beyond this point, voltage in Reg-I saturates. This is velocity saturation in Reg-I which leads to current saturation. This can be seen in Fig 2.3 for V_{GS} values of 5 V and 10 V. At high values of V_{GS}, conductivity of Reg-I and Reg-II is high as these regions are in inversion and accumulation mode respectively. As V_{DS} is increased, the electric field in Reg-I does not reach the critical value because the voltage drop is really small in this regime. Thus while saturation of current at low values of V_{GS} is governed by Reg-I, saturation at higher values of V_{GS} is not governed by Reg-I.

2.2.2 Potential drop in Reg-II

For low values of V_{GS}, when V_{DS} is increased, drop in Reg-II increases but at a lower rate compared to Reg-I. This is attributed to the high conductivity of the accumulation region. After Reg-I voltage saturates, remaining potential is dropped across Reg-II and in this regime, voltage drop in Reg-II increases at a much faster rate. From this, one can conclude that current saturation at low values of V_{GS} is governed only by Reg-I and not

by Reg-II. At higher values of V_{GS}, voltage drop is really low due to high conductivity of this region. Hence, even when V_{DS} is increased, critical field is never attained in this region.

2.2.3 Potential drop in Reg-III

At low values of V_{GS}, potential drop in Reg-III increases at a reduced slope for lower values of V_{DS}. However, when V_{DS} is increased beyond 10 V, the voltage drop rate rises with V_{DS}. This is because Reg-I would have saturated by then and voltage drop across Reg-II is small. Electric field saturation is not reached at low values of V_{GS}. When V_{GS} is increased beyond 10 V, potential drop across Reg-I and II is small and most of the voltage is dropped across Reg-III. When V_{DS} is increased in this regime, velocity saturation occurs in Reg-III, which leads to current saturation. Any further increase in V_{GS} will have no effect on current as Reg-III is not affected by the gate terminal (as shown in Fig 2.3 for V_{GS} values of 15 V and 20 V). This effect is termed as quasi-saturation and is dominant in high voltage LDMOS devices. At high V_{GS}, velocity saturation occurs at the drain end of Reg-III and with increased V_{DS} saturation point moves towards source side leading to drift length modulation and slight increase in current.

2.3 Regional Charges

In order to get a reasonable model for capacitances[2] in SOI-LDMOS, one must first look at various charges present in the device. Once the charges are modeled properly, capacitances can be derived from them using the relation

$$C_{ij} = (2\delta_{ij} - 1)\,\frac{\partial Q_i}{\partial V_j} \tag{2.1}$$

where (i, j) corresponds to set of terminals (D, G, S, B) and δ_{ij} is the Kronecker delta. This calls for analyzing the charges in different bias regimes and modeling them appropriately. For current modeling, it was sufficient to look at values of V_{GS} greater than the threshold voltage. Whereas, for charge modeling one must also model for negative bias voltages[3]. In Reg-I of LDMOS, when V_{GS} is less than the flatband voltage of the channel $V_{FB,ch}$, an accumulation layer of positive charges is created. When V_{GS} goes beyond $V_{FB,ch}$, negative depletion charges are created. Inversion layer of electron appears when the gate voltage goes beyond the threshold voltage of the channel.

In Reg-II, one must note that the reference voltage is not the bulk voltage as the region is not connected to the bulk terminal. Hence one cannot use the same argument above and one must be careful in determining the condition for accumulation, inversion and depletion. The reference voltage in Reg-II is V_C, the Quasi-Fermi potential which varies from V_{DiS} at the junction of channel and drift region to $V_{D'S}$ which is at the junction of Reg-II and Reg-III. Hence, one cannot decide the region of operation without knowing the bias values of internal nodes. When V_{GC} is less than the flat band voltage of the drift region $V_{FB,dr}$, positive depletion charges are present. A positive inversion layer is created only when the bias voltage is a large negative value. When V_{GC} is greater than $V_{FB,dr}$, accumulation layer of electron is created. Since for a given value of V_{GS} and V_{DS}, V_C varies across the drift region, accumulation and depletion regions can simultaneously exist at different portions of the drift region.

[2]By capacitances, we mean the small signal capacitances defined between various terminals.

[3]C_{gg} for a MOSFET/LDMOS in the negative V_{GS} regime acts as a constant value capacitor and is used in ICs where bias independent capacitance is needed. Hence, one also models for negative bias voltages so as to accurately predict those constant capacitance values.

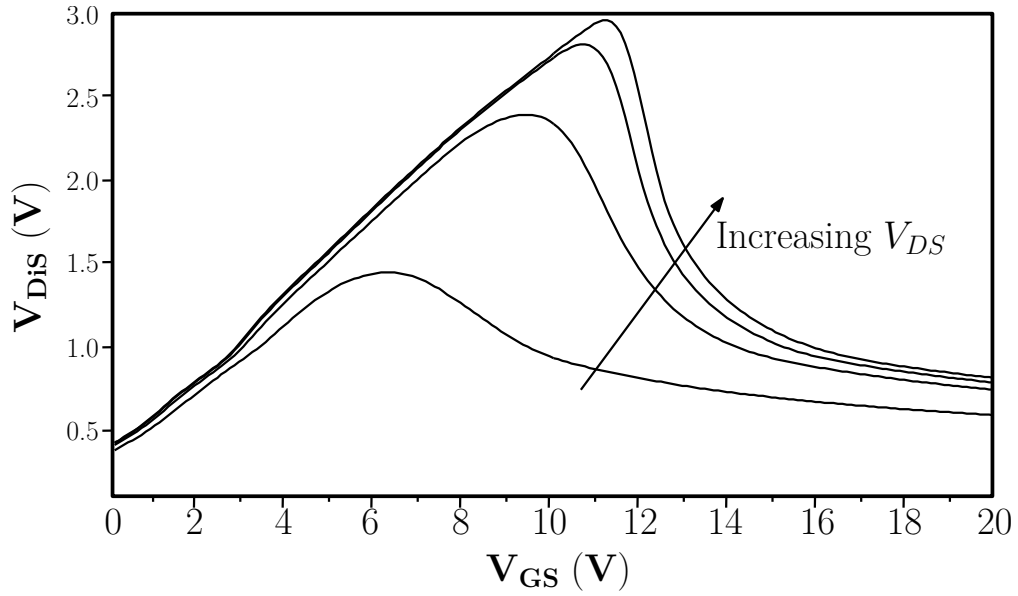

Figure 2.4: Voltage drop V_{DiS} obtained from MEDICI at V_{DS} = 5V, 10V, 15V and 20V.

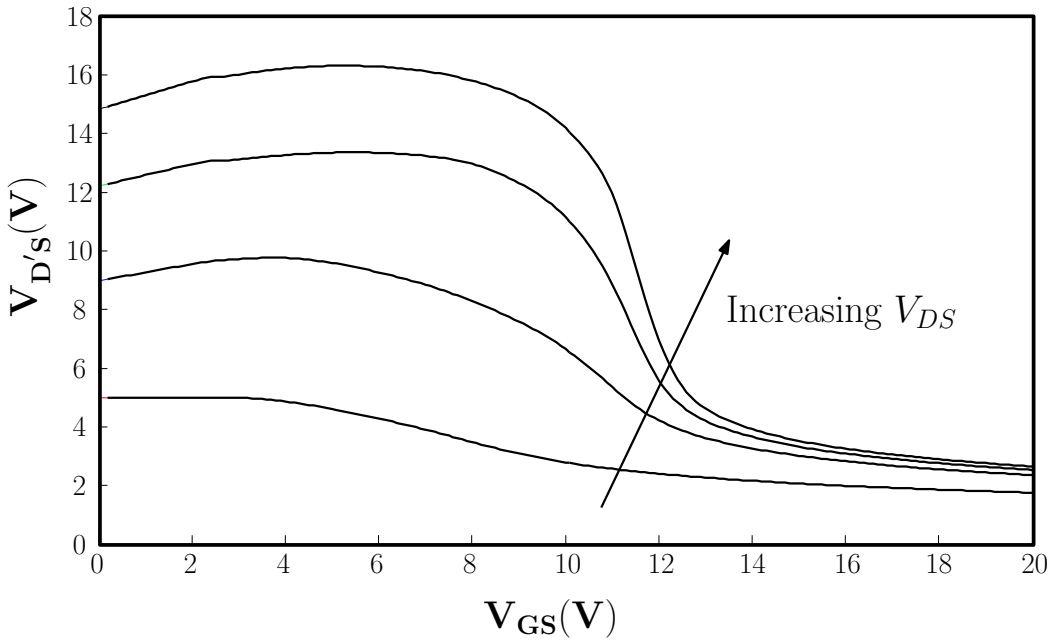

Figure 2.5: Voltage drop $V_{D'S}$ obtained from MEDICI at V_{DS} = 5V, 10V, 15V and 20V.

Fig 2.4 and 2.5 show the variation of V_{D_iS} and $V_{D'S}$ as a function of V_{GS} for various values of V_{DS}. From these two figures, one can observe that for a given value of V_{GS}, the quasi-Fermi potential V_C is higher in the case of $V_{D'S}$ than V_{DiS}. This implies that the potential drop V_{GC} would be more negative in region near $D^{'}$ than D_i. Therefore, when V_{GS} is increased, the region near D_i will develop an accumulation layer first and then this accumulation layer will spread to other regions of Reg-II as V_{GS} rises further.

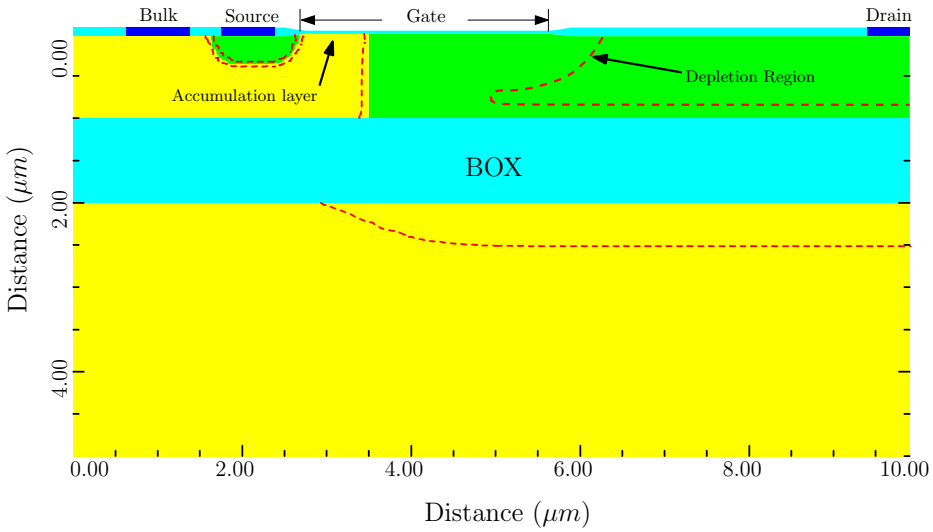

Figure 2.6: Depletion Regions for V_{GS} of -1 V and V_{DS} of 10 V.

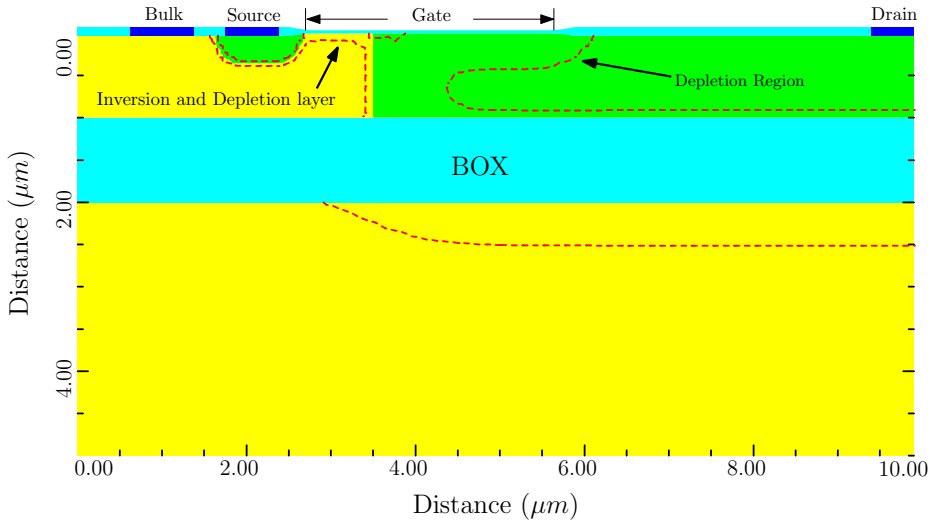

Figure 2.7: Depletion Regions for V_{GS} of 5 V and V_{DS} of 10 V.

Fig 2.6 shows the depletion layers in the device when V_{GS} = -1 V and V_{DS} = 10 V. Since the gate voltage is less than the flatband voltage in the channel region an accumulation region is created. Similarly, in the drift region a depletion region exists as V_{GC} is less than the flatband voltage of the drift region. When V_{GS} = 5 V, inversion layer is created in the channel region. Drift region, on the other hand is still in depletion mode as $V_{GC} < V_{FB,dr}$ even when the gate voltage is 5 V. This is evident from Fig 2.7.

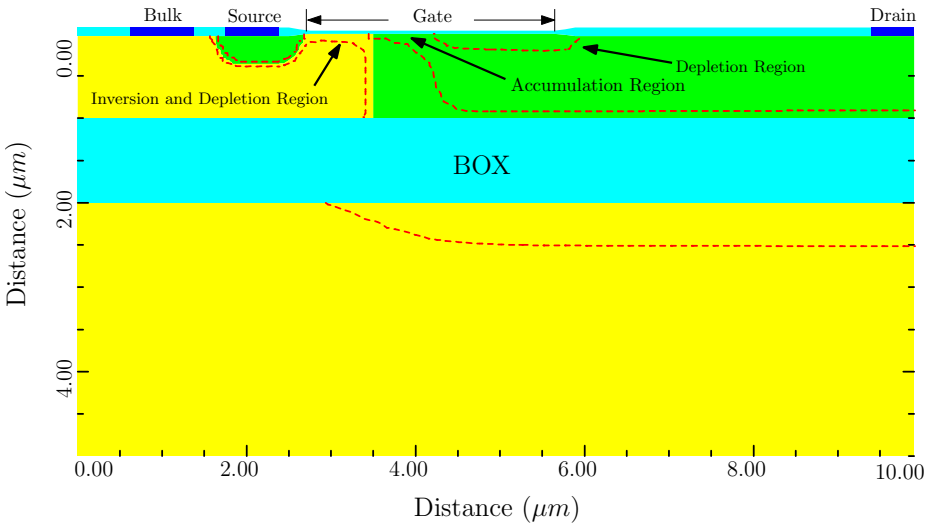

Figure 2.8: Depletion Regions for V_{GS} of 7 V and V_{DS} of 10 V.

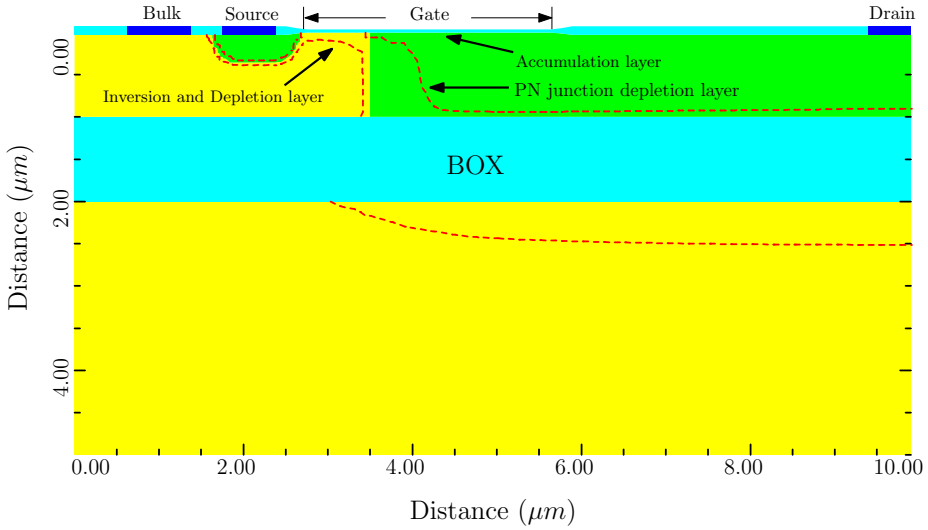

Figure 2.9: Depletion Regions for V_{GS} of 10 V and V_{DS} of 10 V.

Now, when $V_{GS} = 7$ V, drift region near the channel goes into accumulation mode whereas the region near field oxide is still in depletion mode. This is because $V_{GC} > V_{FB,dr}$ near the channel region but $V_{GC} < V_{FB,dr}$ near the field oxide region as seen in Fig 2.8. If the gate voltage is increased further to 10 V, $V_{GC} > V_{FB,dr}$ throughout the drift region. Hence, the drift region is completely in accumulation mode now as shown in Fig 2.9.

Charges in Reg-III can be neglected due to the thick field oxide present. Due to the thickness of this oxide, this region is not affected by variations in the gate voltage. It merely acts as a resistor whose value depends on the mobility and the doping concentration of the region. Apart from charges present in Reg-I and II, one must also pay attention to the depletion region formed at the junction of channel and drift region. Any

variation in gate or drain voltage affects the quasi-Fermi level in the drift region, which in turn changes the depletion charge concentration. This variation of charge in the p-n junction with respect to gate/drain voltage can contribute to the capacitance term which needs to be accounted for. From the analysis carried out in this chapter, the following conclusions can be made

- MOSFET current saturation is due to velocity saturation in Reg-I at lower V_{GS} and due to quasi-saturation at higher V_{GS}.
- In Reg-I, positive accumulation charges are present when $V_{GB} < V_{FB,ch}$ and negative inversion and depletion charges are present when $V_{GB} > V_{FB,ch}$.
- In Reg-II, positive depletion charges are present when $V_{GC} < V_{FB,dr}$ and negative accumulation charges are present when $V_{GC} > V_{FB,dr}$.
- Reg-III need not be taken into consideration for charge modeling. The depletion charges present in the junction between channel and drift region must be taken into account.

CHAPTER 3

MODEL AND VERILOG-A IMPLEMENTATION

A comprehensible model for any device must be capable of predicting the device performance over a wide range of biases, temperatures and device geometries. Since SOI-LDMOS forms an integral part of HVICs, accurate modeling of these devices is necessary to ensure fail-safe design of HVIC circuits.

Any LDMOS model must have the following features:

- Accurate modeling of AC/DC terminal currents and the nodal charges in linear, saturation and off modes.
- Continuity of device models in different regions and continuity in their derivatives and double derivatives[1].
- Conservative nature of charge model.
- Accurate modeling of capacitances to predict the dynamic behavior of the device.
- Modeling high frequency behavior where device operates in Non-Quasi static regime.
- Capability to model impact ionization and snapback and in turn predict SOA.
- Capability to model self heating which requires temperature dependence of model parameters.
- Modeling various types of noise i.e. 1/f noise, thermal noise etc.
- Scalability of the model over wide range of bias, geometries and temperatures.

Among the models available for LDMOS, one can separate them into two distinct categories - macro modeling and compact modeling. Macro model describes the behavior of the device by treating it as a combination of several discrete circuit elements. As the number of physical effects needed to model increases, the number of discrete elements also increases. This results in increase in the number of internal nodes of the device. This not only increases the computational cost but may also result in convergence issues. On the other hand, compact modeling accurately describes the device

[1]Needed to model harmonic distortion.

behavior through a set of self consistent expressions. Since the internal nodes present in the device are solved in the model itself while solving the self consistent expressions, there is a significant reduction in computation time. Also, these expressions are derived from physical principles and can accurately predict certain phenomenon like quasi-saturation, snapback. Hence, compact modeling is preferred over macro modeling.

In this chapter, a comprehensive static and dynamic model of SOI-LDMOS is presented. The model provides an improvement over one of the currently existing compact models, MM20 model. The model incorporates surface potential based approach to model MOS transistor current and charges and accurately predicts in all regions of operations such as accumulation, depletion and inversion. It also provides a modified partition function to partition the charges to get a better model for various capacitances.

3.1 Static current model

The MOSFET current is affected by Reg-I, Reg-II and Reg-III of the device. The MOSFET current is modeled using three current sources (Lekshmi, 2009), (Radhakrishna, 2011) as shown in Fig 3.1. Here, I_{ch} is the current in the channel which is a function of the potential drop, V_{DiS}. The potential drop across Reg-II is given by $V_{D'Di}$ and it determines the current flowing through Reg-II, given by I_{dr}. The current through Reg-III is I_{dr1} and it is a function of the potential drop across Reg-III, given by $V_{DD'}$. The current source models are explained in the following subsections.

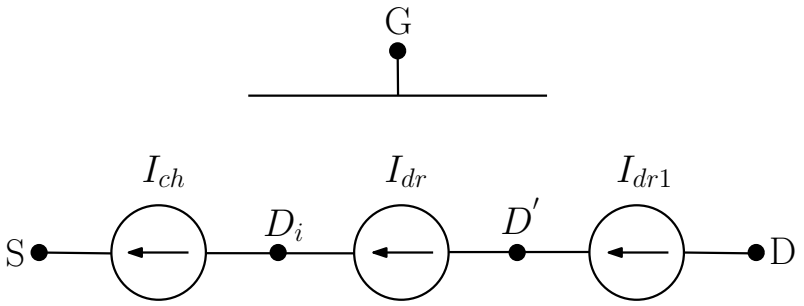

Figure 3.1: EC Model for static MOSFET currents.

3.1.1 Formulation of current in channel region

Channel current is modeled using a surface potential approach. The drift and diffusion components of the current are altogether given by

$$I_{ch} = \frac{W\mu_{ch}}{L_{ch}} \left(\int_{\psi_{s,0}}^{\psi_{s,L}} (-Q_{inv})\, d\psi_s + V_T \left(Q_{inv,L} - Q_{inv,0} \right) \right) \tag{3.1}$$

where W is the channel width, μ_{ch} is the channel mobility taking into account the effect of lateral and vertical electric fields. L_{ch} is the channel length, ψ_s is the surface potential, V_T is the thermal voltage and Q_{inv} is the inversion charge per unit area given as $Q_{inv} = -C_{ox}V_{inv}$ with $Q_{inv,0}$ and $Q_{inv,L}$ being the inversion charges at the source and the drain (D_i) terminals. Inversion potential V_{inv} is given by

$$V_{inv} = V_{GB} - V_{FB,ch} - \psi_s - k_{ch}\sqrt{\psi_s} \tag{3.2}$$

where V_{GB} is the applied gate to bulk voltage, $V_{FB,ch}$ is the flatband voltage of the channel region and k_{ch} is the channel body effect coefficient. If we use the above expression for V_{inv} to obtain the channel current, one would not be able to express the current term completely in terms of the potential drop V_{DiS}. This is due to the square root term present in the equation. Hence, one desires to linearize V_{inv} with respect to some potential. $\psi_{s,o}$, the surface potential at the source side is chosen as a reference and V_{inv} is approximated with respect to that. Upon linearizing we get

$$V_{inv} = V_{inv,0} - \zeta \left(\psi_s - \psi_{s,0} \right) \tag{3.3}$$

with $\zeta = \left(1 + \frac{k_{ch}}{2\sqrt{\psi_{s,0}}} \right)$ and the inversion potential on the source side is given by

$$V_{inv,0} = V_{inv} \mid_{\psi_s = \psi_{s,0}} = V_{GB} - V_{FB,ch} - \psi_{s,0} - k_{ch}\sqrt{\psi_{s,0}} + m_{DIBL}V_{DiS} \tag{3.4}$$

where $\psi_{s,0} = 2V_T ln\left(\frac{N_{ch}}{n_i}\right)$ [2], N_{ch} is doping concentration of the channel and n_i is the intrinsic carrier concentration. m_{DIBL} accounts for drain induced barrier lowering (applicable only in the case of short channel). Using (3.2), (3.3) and (3.4), (3.1) can be

[2] When V_{GB} is beyond the threshold voltage of the channel one can approximately write $\psi_{s,0} = 2\phi_f + V_{SB}$, where $\phi_f = V_T ln\left(\frac{N_{ch}}{n_i}\right)$.

simplified as

$$I_{ch} = \frac{W\mu_{ch}C_{ox}}{L_{ch}}\left(V_{inv,0} - \frac{1}{2}\zeta\Delta\psi_s + \zeta V_T\right)\Delta\psi_s \tag{3.5}$$

where $\Delta\psi_s = \psi_{s,L} - \psi_{s,0}$. Mobility reduction due to lateral fields which accounts for velocity saturation is given by

$$\mu_{ch} = \frac{\mu_{eff,ch}}{1 + \theta_{3,ch}\Delta\psi_s} \tag{3.6}$$

where $\theta_{3,ch} = \dfrac{\mu_{0,ch}}{L_{ch}v_{sat}}$ is the parameter that takes care of velocity saturation in the channel, where $\mu_{0,ch}$ is the zero field channel mobility and v_{sat} is the saturation velocity in channel. $\mu_{eff,ch}$ accounts for mobility reduction due to the vertical field and is given by

$$\mu_{eff,ch} = \frac{\mu_{0,ch}}{\left(1 + \theta_1 V_{inv,0} + \theta_2\left(\sqrt{\psi_{s,0}} - \sqrt{\psi_{s,0}\mid_{V_{SB}=0}}\right)\right)} \tag{3.7}$$

where θ_1 and θ_2 are model parameters. Substituting (3.6) and (3.7) in (3.5) and by replacing $\Delta\psi_s = \psi_{s,L} - \psi_{s,0}$ by V_{DiS}[3], gives the channel current as

$$I_{ch} = \frac{W\mu_{ch}C_{ox}}{L_{ch}}\left(V_{inv,0} - 0.5\zeta V_{DiS} + \zeta V_T\right)V_{DiS}. \tag{3.8}$$

This equation is true only until the onset of saturation. To incorporate saturation into the model, one must find $\dfrac{dI_{ch}}{dV_{DiS}}\mid_{V_{DiS}=V_{sat,ch}} = 0$. This gives us the channel saturation potential $(V_{sat,ch})$ as

$$V_{sat,ch} = \frac{\dfrac{2V_{inv,0}}{\zeta}}{1 + \sqrt{1 + \dfrac{2\theta_{3,ch}V_{inv,0}}{\zeta}}}. \tag{3.9}$$

The final expression of channel current then becomes

$$I_{ch} = \left(1 + \lambda_{ch}V_{DiS}\right)\frac{W\mu_{eff,ch}C_{ox}}{L_{ch}}\frac{\left(V_{inv,0} - 0.5\zeta V_{DiS,eff} + \zeta V_T\right)V_{DiS,eff}}{\left(1 + \theta_{3,ch}V_{DiS,eff}\right)} \tag{3.10}$$

where λ_{ch} is the channel modulation parameter and $V_{DiS,eff}$ is the minimum of V_{DiS} and $V_{sat,ch}$. In order to ensure that the current curve is smooth and differentiable at all points, appropriate smoothing function is used which smoothly connects the I_{ch} before $V_{sat,ch}$ with the saturation current value $I_{ch,sat}$.

[3]Note: Difference between the surface potential $\Delta\psi_s$ is equal to the applied potential V_{DiS} only beyond the threshold voltage.

3.1.2 Formulation of current under gate oxide

The drift current formulation is done in terms of the Quasi-Fermi potential as opposed to the surface potential formulation for the channel current. The current in Reg-II can be written as

$$I_{dr} = \frac{W\mu_{dr}}{L_{dr}} \int_{V_{D_i}}^{V_{D'}} \left(-Q_n^{dr}\right) dV_c \tag{3.11}$$

where W is the drift region width L_{dr} is the drift region length and μ_{dr} is Reg-II mobility taking into effect of mobility reduction due to lateral and vertical electric fields. In the channel current formulation, flow of electrons was only through the inversion layer but in Reg-II, flow of electrons is through accumulation, depletion and the bulk. Hence one must take all these charges into account while formulating Q_n^{dr}. Hence, one can express Q_n^{dr} as

$$\begin{aligned} Q_n^{dr} &= -qN_{dr}t_{si} + Q_{acc}^{dr} - Q_{dep}^{dr}\,, V_{GC} > V_{FB,dr} \\ Q_n^{dr} &= -qN_{dr}t_{si} - Q_{inv}^{dr} - Q_{dep}^{dr}\,, V_{GC} < V_{FB,dr} \end{aligned} \tag{3.12}$$

where N_{dr} is the doping concentration, t_{si} is the silicon film thickness, Q_{acc}^{dr}, the accumulation charge per unit area, Q_{inv}^{dr} is the inversion charge per unit area and Q_{dep}^{dr} is the depletion charge per unit area. The first term accounts for electron flow through the bulk of Reg-II[4], the second and third terms are for electron flow through the accumulation/inversion and the depletion layers. One must note that depending upon the value of V_C, one can have accumulation, inversion or depletion charges. Since the bias voltages are sufficiently positive, contribution from inversion charges is really negligible. One can write the potential balance equation in Reg-II as

$$V_{GC} = V_{FB,dr} + \psi_s^{dr} - \frac{\left(Q_{surf}^{dr} - Q_{dep}^{dr}\right)}{C_{ox}} \tag{3.13}$$

where Q_{surf}^{dr} is $+Q_{acc}^{dr}$ or $-Q_{inv}^{dr}$ depending upon the value of V_{GC}. One can rewrite the above expression in terms of charges as

$$\left(Q_{surf}^{dr} - Q_{dep}^{dr}\right) = Q_{gate}^{dr} = -C_{ox}\left(V_{GC} - V_{FB,dr} - \psi_s^{dr}\right). \tag{3.14}$$

[4]Note that the expression $qN_{dr}t_{si}$ is an approximation. In depletion condition most of the silicon film in Reg-II is depleted and the contribution from bulk charge will be less than $qN_{dr}t_{si}$. However, under accumulation condition, this expression holds true.

Based on the region of operation one can make appropriate approximation to the above expression. When $V_{GC} > V_{FB,dr}$, accumulation layer will be formed and depletion charge is negligible. Also, under accumulation condition, most of the voltage drop occurs across the gate oxide and value of surface potential is negligible. Hence, one can rewrite (3.14) as

$$Q_{gate}^{dr} = -C_{ox}\left(V_{GC} - V_{FB,dr}\right). \tag{3.15}$$

When $V_{GC} < V_{FB,dr}$, depletion charges will be in abundance and there will be negligible inversion charge (as long as voltage below the threshold voltage of Reg-II). One can express Q_{dep}^{dr} as $k_{dr}C_{ox}\sqrt{-\psi_s^{dr}}$ where k_{dr} is the body coefficient of Reg-II. One can rewrite (3.14) as

$$-k_{dr}C_{ox}\sqrt{-\psi_s^{dr}} = -C_{ox}\left(V_{GC} - V_{FB,dr} - \psi_s^{dr}\right). \tag{3.16}$$

Solving the above quadratic expression gives us an expression for Q_{gate}^{dr} which is

$$Q_{gate}^{dr} = k_{dr}C_{ox}\left(-0.5k_{dr} + \sqrt{(0.5k_{dr})^2 - (V_{GC} - V_{FB,dr})}\right). \tag{3.17}$$

Total charge Q_n^{dr} can now be written as

$$Q_n^{dr} = -qN_{dr}t_{si} + Q_{gate}^{dr} = -qN_{dr}t_{si} - C_{ox}\left(V_{GC} - V_{FB,dr} - \psi_s^{dr}\right). \tag{3.18}$$

Following the same approach as previous section, one can linearize the above charge with respect to the terminal D_i. If we consider $V_n^{dr} = -\frac{Q_n^{dr}}{C_{ox}}$, then one can write V_n^{dr} as

$$V_n^{dr} = V_n^{dr}\mid_{V_c = V_{D_i}} - (V_c - V_{D_i}) \tag{3.19}$$

where the linearization coefficient is one[5] The mobility reduction due to lateral and perpendicular fields is modeled similar to the channel region as follows

$$\mu_{dr} = \frac{\mu_{eff,dr}}{\left(1 + \theta_{3,dr}V_{D'D_i}\right)} \tag{3.20}$$

[5]Dependence of ψ_s on V_c is neglected to get a linearization coefficient of one. This is valid in accumulation region where the value of ψ_s is negligible. However, neglecting it in the depletion region is debatable.

where $\theta_{3,dr} = \dfrac{\mu_{0,dr}}{L_{dr} v_{sat}}$ is the parameter that takes into account velocity saturation in Reg-II, with v_{sat} being the saturation velocity[6] and $\mu_{0,dr}$ being the zero field mobility. $\mu_{eff,dr}$ account for the mobility reduction due to vertical field and is given by

$$\mu_{eff,dr} = \frac{\mu_{0,dr}}{\left(1 + \theta_{acc}\left(0.5V_{GD_i} + 0.5V_{GD'} - V_{FB,dr}\right)\right)} \tag{3.21}$$

where θ_{acc} is a model parameter. Substituting (3.19 , 3.21) in (3.11) gives Reg-II current as

$$I_{dr} = \frac{W\mu_{dr}C_{ox}}{L_{dr}}\left(V_n^{dr}\mid_{V_c=V_{D_i}} - 0.5V_{D'D_i}\right)V_{D'D_i}. \tag{3.22}$$

This model is only till the onset of saturation. To model saturation, one must compute the saturation potential by forcing $\frac{dI_{dr}}{dV_{D'D_i}}\mid_{V_{D'D_i}=V_{sat,dr}} = 0$. This gives the Reg-II saturation potential as

$$V_{sat,dr} = \frac{2V_n^{dr}\mid_{V_c=V_{D_i}}}{1 + \sqrt{1 + 2\theta_{3,dr}V_n^{dr}\mid_{V_c=V_{D_i}}}}. \tag{3.23}$$

The final expression for Reg-II is given by

$$I_{dr} = \frac{W\mu_{eff,dr}C_{ox}}{L_{dr}}\frac{\left(V_n^{dr}\mid_{V_c=V_{D_i}} - 0.5V_{D'D_{i,eff}}\right)V_{D'D_{i,eff}}}{\left(1 + \theta_{3,dr}V_{D'D_{i,eff}}\right)} \tag{3.24}$$

where $V_{D'D_{i,eff}}$ is the effective potential drop across Reg-II which is the minimum of $V_{D'D_i}$ and $V_{sat,dr}$. The transition from linear region to the saturation region is made differentiable by using appropriate smoothing function.

3.1.3 Formulation of current under field oxide

The drift region under the field oxide can be modeled as a resistor since that region is not affected by the gate potential. However, one must note that it is this region which is responsible for quasi-saturation at higher gate voltages. After the onset of quasi-saturation, drift length modulation occurs resulting in increase in current with drain voltage. Hence these two effects must be taken into account while modeling in this

[6]Note: Saturation velocity in channel and drift region are different

region. One can write the current flowing through this region as

$$I_{dr1} = \frac{\left(1+\lambda_{dr1}V_{DD'}\right) qN_{dr1}\mu_{dr1}V_{DD'}Wt_{si}}{L_{LC}\left(1+\theta_{1,dr1}\dfrac{V_{DD'}}{L_{LC}E_C}^{\theta_{dr1}}\right)^{1/\theta_{dr1}}} \tag{3.25}$$

where N_{dr1} is the drift layer doping concentration, μ_{dr1} is the effective mobility taking into account velocity saturation, $V_{DD'}$ is the potential drop in Reg-III and t_{si} is silicon film thickness. The drift length modulation parameter is given by λ_{dr1}. Model parameters $\theta_{1,dr1}$ and θ_{dr1} account for velocity saturation in this region.

The current models I_{ch}, I_{dr} and I_{dr1} derived in (3.10), (3.24) and (3.25) are used in the model circuit as shown in Fig 3.1. These three current sources are in series and under any bias, each of these current sources must converge to the same value. The potential drops V_{DiS}, $V_{D'D_i}$ and $V_{DD'}$ get adjusted so that I_{ch}, I_{dr} and I_{dr1} have the same value.

3.2 Charge model

Various capacitances of LDMOS can be calculated only if the charges in various regions are modeled appropriately. Before analyzing the charges present in LDMOS, looking at the charge formulation in a normal MOSFET is important. Once the MOSFET charge model becomes clear, one can extrapolate the same concepts to LDMOS with minor variations. Let us consider a 4 terminal NMOSFET and try calculating various capacitances present in the device. Note that by capacitance, one implies that it is the small signal capacitance which is defined as $C_{ij} = (2\delta_{ij} - 1)\dfrac{\partial Q_i}{\partial V_j}$ where $(i,j) \in (G,D,S,B)$ and Q_i is the charge associated with each terminal. From charge conservation principle, one can write

$$Q_G + Q_D + Q_S + Q_B = 0. \tag{3.26}$$

The gate charge is negative of the sum of charges present beneath the gate oxide viz. depletion and inversion/accumulation charges. Let q_{dep} be the depletion charge per unit area and q_{surf} be the surface charge per unit area. q_{surf} is the inversion charge if $V_{GB} > V_{FB}$ else is the accumulation charge q_{acc}. Gate charge Q_G can now be defined

as follows

$$Q_G = -W \int_0^{L_{ch}} (q_{surf} + q_{dep})\, dx \tag{3.27}$$

where W is the width and L_{ch} is the channel length of the device. It is assumed that the charges vary only along the length of the device and variation along the width is uniform. q_{dep} is attributed to the bulk terminal as depletion charges are fixed charges. Now, q_{surf} has to be partitioned between the drain and source terminal so that

$$Q_D + Q_S = W \int_0^{L_{ch}} q_{surf} dy. \tag{3.28}$$

Partitioning between the source and drain charge is achieved through the Ward-Dutton partition function (Ward and Dutton, 1978),(Oh *et al.*, 1980). The formulation of partition function is explained in next section.

3.2.1 Ward-Dutton (WD) Partitioning Scheme

Current transport equation for an NMOSFET can be written as

$$I(x,t) = qW\mu_n n_s(x,t)\frac{\partial V}{\partial x} \tag{3.29}$$

where n_s is the electron concentration per unit area along the length of the device and V is the quasi-Fermi level which ranges from $V = V_{SB}$ at $x = 0$ to $V = V_{DB}$ at $x = L$. This derivation assumes that mobility is constant throughout the length of the device and that the device operates in the quasi-static regime. The current continuity equation (neglecting generation and recombination) can be written as

$$\frac{\partial n_s}{\partial t} = -\frac{1}{qW}\frac{\partial I(x,t)}{\partial x}. \tag{3.30}$$

The electron concentration $n_s(x,t)$ is a function of both position and time. It can alternatively be represented in terms of the quasi-Fermi potential and gate potential as

$$n_s(x,t) \equiv n_s\left(V(x,t), V_G(t)\right) = n_s\left(V, V_G\right) \tag{3.31}$$

where the position dependence is incorporated into the quasi-Fermi potential and the time dependence is incorporated into both quasi-Fermi and gate potentials. This repre-

sentation is useful while integrating the charge in future. (3.30) is integrated from 0 to x and the obtained $I(x,t)$ is substituted back in (3.29) to get

$$qW\int_0^x \frac{\partial n_s(x^{'},t)}{\partial t}dx^{'} = -q\mu W n_s\left(V,V_G\right)\frac{\partial V}{\partial x} + I(0,t). \tag{3.32}$$

Integrating the above equation again from $x=0$ to $x=L$ and solving for $I(0)$ one gets

$$I(0,t) = \frac{q\mu W}{L}\int_{V_{SB}(t)}^{V_{DB}(t)} n_s\left(V,V_G\right)dV + \frac{qW}{L}\int_0^L\int_0^x \frac{\partial n_s(x^{'},t)}{\partial t}dx^{'}dx \tag{3.33}$$

where the first term on the RHS is the conduction current as defined in (3.29), and the second term is the displacement current. The above equation can be re-written as

$$I(0,t) = I_0(t) - \frac{d}{dt}\left\{-q\frac{W}{L}\int_0^L\int_0^x n_s(x^{'},t)dx^{'}dx\right\}. \tag{3.34}$$

Now, one can write the source transient current $I_S(t)$ as a linear combination of steady state current $I_0(t)$ and as a derivative of the source charge, where the source charge Q_S is

$$\begin{aligned} Q_S &= -q\frac{W}{L}\int_0^L\int_0^x n_s(x^{'},t)dx^{'}dx \\ &= -qW\int_0^L\left(1-\frac{x}{L}\right)n_s(x,t)dx. \end{aligned} \tag{3.35}$$

A similar derivation when done for the drain charge, gives us

$$Q_D = -qW\int_0^L\left(\frac{x}{L}\right)n_s(x,t)dx. \tag{3.36}$$

Since $n_s(x,t)$ is the electron concentration in the inversion region, $-qn_s(x,t)$ will be the inversion charge per unit area. Hence, one can write the source and drain charges as

$$\begin{aligned} Q_D &= W\int_0^L \frac{x}{L}q_{inv}dx \\ Q_S &= W\int_0^L\left(1-\frac{x}{L}\right)q_{inv}dx. \end{aligned} \tag{3.37}$$

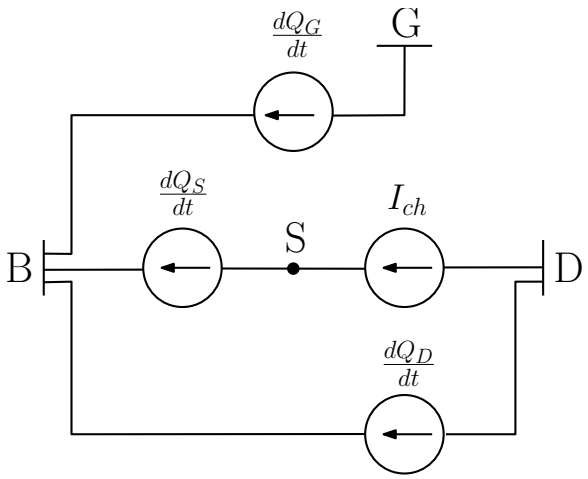

Figure 3.2: EC Model for static and dynamic currents in NMOSFET.

The x/L factor linearly partitions the inversion charge between the source and drain terminals and it is called as the Ward-Dutton (WD) partition factor. To summarise, charges associated with various terminals can be written as

$$\begin{aligned} Q_G &= -W \int_0^{L_{ch}} (q_{surf} + q_{dep})\, dx \\ Q_D &= W \int_0^{L} \frac{x}{L} q_{inv} dx \\ Q_S &= W \int_0^{L} \left(1 - \frac{x}{L}\right) q_{inv} dx \\ Q_B &= -\left(Q_G + Q_D + Q_S\right). \end{aligned} \tag{3.38}$$

The above charge model is implemented in an equivalent circuit as shown in Fig 3.2. Here the charges are represented as displacement current terms connected from respective terminals to bulk. By charge conservation, bulk displacement current term is automatically calculated. The procedure shown above for calculating charges is used in LDMOS charge modeling with slight variations as discussed in the following section.

3.2.2 Modified Ward-Dutton (MWD) partitioning scheme

WD partition deals with partitioning charges in a MOSFET. One can apply the same principle to an LDMOS which has 3 distinct internal regions present in it, namely Reg-I, II and III. Reg-I and Reg-II, show capacitive effects due to the influence of gate

terminal. Reg-III, on the other hand, is modeled purely as a resistor with no capacitive effects in that region. MEDICI simulations also agree with this conjecture. Hence, it is sufficient if one considers Reg-I and II for the charge model. LDMOS, with Reg-I and II can be thought of as a device with two distinct internal regions and an internal node designated by D_i.

Firstly, the partition scheme adopted by MM20 model(MM2, 2008),(Grabinski and Gneiting, 2010) will be discussed. This model provides a partitioning scheme known as Modified WD partitioning, but does not provide a physical basis behind it. Also, this model does not fit well with the device simulations. This section aims to derive the Modified WD partition scheme from first principles and highlight the error committed during the derivation. Apart from that, it also provides an alternative to this partition scheme which is physically sound and is shown to be reasonably accurate with device simulations.

Let us consider Reg-I and Reg-II of LDMOS with terminals S, D_i and $D^{'}$ as shown in Fig 2.1. Modified WD partitioning provides a partition scheme as follows

$$Q_G = W\left[\int_0^{L_{ch}} (qn_{ch} + qn_{dep})\, dx + \int_0^{L_{dr}} (qn_{dr})\, dx\right]$$

$$Q_{D'} = W\left[\int_0^{L_{ch}} \left(\frac{x}{(L_{ch}+L_{dr})}(-qn_{ch})\right) dx + \int_{L_{ch}}^{L_{ch}+L_{dr}} \left(\frac{x}{(L_{ch}+L_{dr})}(-qn_{dr})\right) dx\right]$$

$$\begin{aligned} Q_S = {} & W\int_0^{L_{ch}} \left(\left(1-\frac{x}{(L_{ch}+L_{dr})}\right)(-qn_{ch})\right) dx \\ & + W\int_{L_{ch}}^{L_{ch}+L_{dr}} \left(\left(1-\frac{x}{(L_{ch}+L_{dr})}\right)(-qn_{dr})\right) dx \end{aligned}$$

$$Q_B = -\left(Q_G + Q_D^{'} + Q_S\right) \tag{3.39}$$

where n_{ch} and n_{dr} are the electron densities in the channel and drift region which appear in the current formulation (n_{ch} is typically the inversion charge in the channel region and n_{dr} is the accumulation and depletion charges in the drift region) and n_{dep} is the depletion charge density in the channel region.

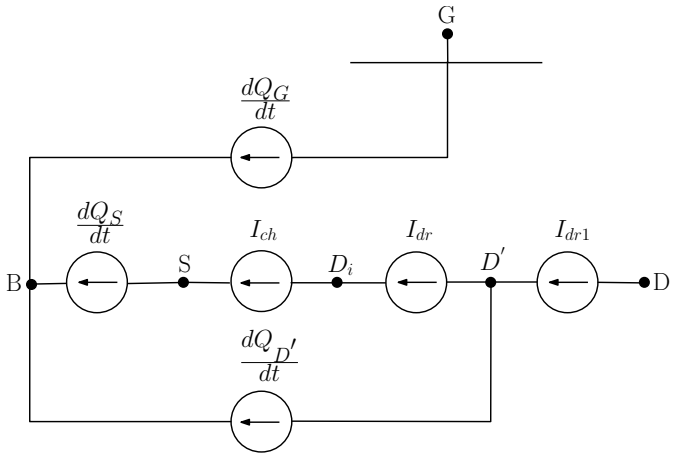

Figure 3.3: EC Model for static and dynamic MOSFET currents - MM20.

Fig 3.3 shows the equivalent circuit model of MM20 model. The charges are assigned to four terminals viz. gate, terminal $D^{'}$, source and bulk. From each of these terminals a displacement current source $\frac{dQ}{dt}$ is connected to the bulk terminal which acts as a reference for our analysis. Due to the circuit topology and by charge conservation, $\frac{dQ_B}{dt}$ is calculated automatically. Note that there is no explicit displacement current source from the drain terminal. This is because the region between terminal $D^{'}$ and drain does not contain any charge quantity that varies with bias. Though there is no explicit connection to the drain terminal, internal displacement currents ensure that a time varying current flows from drain whenever there is a variation in gate, drain or source bias.

One can try deriving the above result from fundamental equations and check its validity. Current equation for any region can be written as

$$I(x,t) = qW\mu n_s(x,t)\frac{\partial V(x,t)}{\partial x}. \tag{3.40}$$

Continuity relation (neglecting recombination and generation) is given by

$$\frac{\partial n_s(x,t)}{\partial t} = -\frac{1}{qW}\frac{\partial I(x,t)}{\partial x}. \tag{3.41}$$

Following the approach similar to sec 3.2.1, integration of the above equation is done with respect to x, with limits ranging from 0 to x and again with respect to x with limits

ranging from 0 to $L_{ch} + L_{dr}$ to give

$$\frac{qW}{(L_{ch}+L_{dr})}\int_0^{L_{ch}+L_{dr}}\int_0^x \frac{\partial n_s(x^{'},t)}{\partial t}dx^{'}dx = -\frac{qW\mu}{L_{ch}+L_{dr}}\int_{V_{SB}}^{V_{D^{'}B}} n_s(V,V_G)dV + I(0,t). \tag{3.42}$$

The above equation can be reduced to give

$$I(0,t) = \frac{(L_{ch}I_{ch}(t)+L_{dr}I_{dr}(t))}{L_{ch}+L_{dr}} - \frac{qW}{L_{ch}+L_{dr}}\frac{d}{dt}\left\{\int_0^{L_{ch}+L_{dr}}\int_0^x \frac{\partial n_s(x^{'},t)}{\partial t}dx^{'}dx\right\}. \tag{3.43}$$

The displacement current term can be reduced to give

$$\begin{aligned} I(0,t) = \frac{(L_{ch}I_{ch}(t)+L_{dr}I_{dr}(t))}{L_{ch}+L_{dr}} - W\frac{d}{dt}\left\{\int_0^{L_{ch}}\left(1-\frac{x}{L_{ch}+L_{dr}}\right)(-qn_{ch})dx\ ..\right. \\ \left. ... + \int_{L_{ch}}^{L_{ch}+L_{dr}}\left(1-\frac{x}{L_{ch}+L_{dr}}\right)(-qn_{dr})dx\right\}. \end{aligned} \tag{3.44}$$

One can observe that the displacement current term obtained in the above expression is exactly equal to the MM20 expression. Total current is equal to the sum of conduction and displacement current only if the first term can be written as $I_{conduc}(t)$. Note that only under steady state condition, $I_{ch}(t)$ is equal to $I_{dr}(t)$ and only then the first term can be written as a single current term. If the system is not in steady-state then I_{ch} need not be equal to I_{dr} and one cannot equate the second term completely to the displacement current[7]. The first expression will have some contribution to the displacement term which has been neglected in the MM20 modeling. Since they assume that $I_{ch}(t)$ and $I_{dr}(t)$ are equal at all points of time, the two current sources are in series. Now one is interested in finding out the additional term that needs to be included in the displacement current expression, given the fact that these two conduction currents are forced to be equal. The expression for source current can be written as

$$I(0,t) = \frac{(L_{ch}I_{ch}(t)+L_{dr}I_{dr}(t))}{L_{ch}+L_{dr}} - W\frac{dQ_S}{dt} \tag{3.45}$$

Under small signal analysis, let us assume that $I_{ch}(t)$ lags $I_{dr}(t)$ by a constant time delay τ. This implies that

$$I_{ch}(t) = I_{dr}(t-\tau) \tag{3.46}$$

[7]This arises because the two regions are electrostatically different and under a transient input, both the currents will achieve the same value only when the input stabilizes to a steady state value. However, these two currents will be same if Reg-I and Reg-II were electrostatically identical.

If we transform (3.45) to Fourier domain, and use the above relation then we get

$$I(0,t) = \frac{L_{ch} I_{dr} e^{-j\omega\tau} + L_{dr} I_{dr}}{L_{ch} + L_{dr}} - j\omega Q_S \tag{3.47}$$

If one operates at a frequency ω such that $\omega\tau$ is a small quantity, then $e^{-j\omega\tau}$ can be approximated as $1 - j\omega\tau$. If this approximation is invoked in (3.47), then the source current can be written as

$$\begin{aligned} I(0,t) &= I_{dr}(t) - j\omega \left\{ Q_S + \frac{L_{ch} I_{dr} \tau}{L_{ch} + L_{dr}} \right\} \\ &= I_{dr}(t) - \frac{d}{dt} \left\{ Q_S + \frac{L_{ch} I_{dr} \tau}{L_{ch} + L_{dr}} \right\} \end{aligned} \tag{3.48}$$

The above expression for source current now has been completely separated into conduction term and a displacement current with a correction to the displacement current. MM20 have neglected this correction to their equivalent circuit model. It is shown in sec 4.0.6 that adding the correction term to the MM20 model does give an improvement to the capacitance model. Note that this correction term is based on the assumption that the time delay τ is a constant. Hence, it can work only in cases where this assumption holds true and cannot be generalised for any condition.

The problem faced in MM20 model where the total current cannot be expressed as a sum of conduction and displacement current for any given condition can be overcome if we do not consider Reg-I and Reg-II together and treat each one of them separately. WD partition as seen in sec 3.2.1 can be applied to each region to get terminal charges Q_S, Q_{D_i} and $Q_{D'}$. Note that this approach never makes an assumption that the conduction currents $I_{ch}(t)$ and $I_{dr}(t)$ should be equal. Hence, the new partition model can be

expressed as

$$Q_G = W\left[\int_0^{L_{ch}} (qn_{ch} + qn_{dep})\, dx + \int_0^{L_{dr}} (qn_{dr})\, dx\right]$$

$$Q_S = W\int_0^{L_{ch}} \left(1 - \frac{x}{L_{ch}}\right)(-qn_{ch})dx$$

$$Q_{D_i} = W\int_0^{L_{ch}} \left(\frac{x}{L_{ch}}\right)(-qn_{ch})dx + W\int_0^{L_{dr}} \left(1 - \frac{x}{L_{dr}}\right)(-qn_{dr})dx \tag{3.49}$$

$$Q_{D'} = W\int_0^{L_{dr}} \left(\frac{x}{L_{dr}}\right)(-qn_{dr})dx$$

$$Q_B = -\left(Q_G + Q_D^{'} + Q_{D_i} + Q_S\right)$$

where D_i gets contribution both from channel and drift regions. This model can be implemented in an equivalent circuit as shown in Fig 3.4. The total gate charge is computed from both channel and drift regions and is modeled as a displacement current $\frac{dQ_G}{dt}$ from gate to bulk. Other terminal charges are modeled as $\frac{dQ}{dt}$ current sources from the respective terminals to bulk. Note that bulk is chosen as a reference terminal and connecting all the displacement current sources ensures that charge conservation is maintained. Q_B is not calculated explicitly and the connection of current sources in the topology given in the figure gives Q_B automatically.

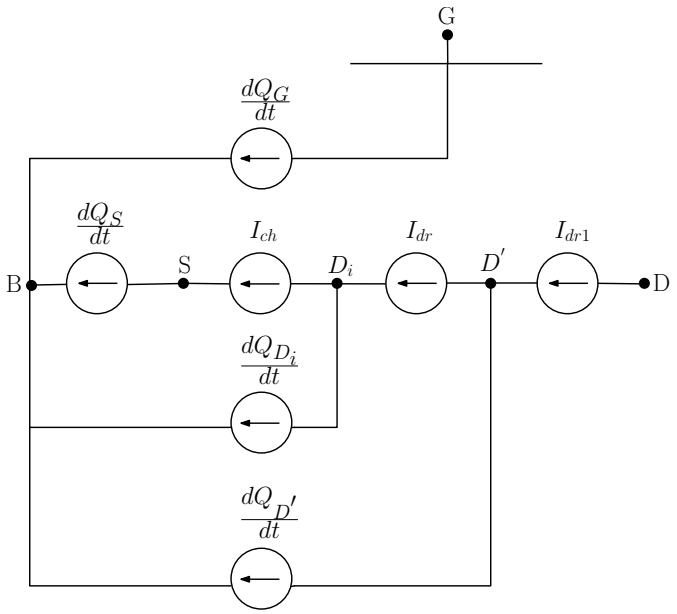

Figure 3.4: EC Model for static and dynamic MOSFET currents.

Note that this model is valid under all conditions as current in each region is expressed as a sum of conduction and displacement currents. The modification that this model offers against MM20 is the addition of an extra displacement current source from D_i terminal to the bulk.

3.2.3 Formulation of charge in channel region

Since the channel region of SOI-LDMOS is structurally similar to NMOSFET, charge modeling should be similar to MOS charge modeling. Charges that are of interest to us are the depletion and inversion/accumulation charges. Depletion charge q_{dep} can be written as

$$q_{dep} = -sgn\left(\psi_s^{ch}\right) C_{ox} k_{ch} \sqrt{abs\left(\psi_s^{ch}\right)} \tag{3.50}$$

where ψ_s^{ch} is the surface potential of the channel and sgn is the signum function. The above expression holds good for all regions of operations ranging from accumulation, depletion to inversion. Inversion/accumulation charge[8] is given as

$$q_{surf} = -C_{ox}\left(V_{GB} - V_{FB,ch} - \psi_s^{ch} - sgn\left(\psi_s^{ch}\right) k_{ch} \sqrt{abs\left(\psi_s^{ch}\right)}\right). \tag{3.51}$$

Potentials V_{dep} and V_{surf} can be defined as $V_{dep} = -\frac{q_{dep}}{C_{ox}}$ and $V_{surf} = -\frac{q_{surf}}{C_{ox}}$ so that the analysis of charges can be done completely in terms of potentials. Since V_{dep} and V_{surf} are non-linear functions of surface potential, approximations of these charges are done with respect to the source terminal (similar to Sec 3.1.1) as

$$\begin{aligned} V_{dep} &= V_{dep}\mid_{\psi_s^{ch}=\psi_{s,0}^{ch}} + (\zeta - 1)\left(\psi_s^{ch} - \psi_{s,0}^{ch}\right) \\ V_{surf} &= V_{surf}\mid_{\psi_s^{ch}=\psi_{s,0}^{ch}} - \zeta\left(\psi_s^{ch} - \psi_{s,0}^{ch}\right) \end{aligned} \tag{3.52}$$

where $\zeta = \left(1 + \frac{1}{2\sqrt{abs(\psi_{s,0}^{ch})}}\right)$. The charges have now been defined and approximated with respect to the source terminal. To obtain the final gate, source and drain expressions, one must know the variation of charge densities as a function of x. Hence, one must find the dependence of ψ_s with x so that the charges can be expressed as a function of x. To obtain that, one uses the channel current expression. The channel

[8]Shall henceforth be called as surface charge to avoid ambiguity.

current can be written as

$$I_{ch} = W\mu_{ch}C_{ox}\left(V_{surf}\frac{d\psi_s}{dx} - V_T\frac{dV_{surf}}{dx}\right) \tag{3.53}$$

where the parameters in the equations are as defined in sec 3.1.1. Only modification that has been made to this equation has been changing V_{inv} to V_{surf} to make the analysis generic for any given gate bias. Incorporating the linearization made in (3.52) and integrating the above expression from 0 to x, one obtains

$$I_{ch}x = W\mu_{ch}C_{ox}\left[\int_{\psi_{s,0}}^{\psi_s(x)}\left(V_{surf,0} - \zeta\left(\psi_s - \psi_{s,0}\right)\right)d\psi_s + \zeta V_T\int_{\psi_{s,0}}^{\psi_s(x)}d\psi_s\right]. \tag{3.54}$$

Upon replacing I_{ch} with (3.5) and simplifying one can get

$$x = L_{ch}\left[\frac{\left(V_{surf,0} + \zeta\psi_{s,0} + \zeta V_T\right)\left(\psi_s(x) - \psi_{s,0}\right) - \zeta\left(\dfrac{\psi_s(x)^2 - \psi_{s,0}^2}{2}\right)}{\left(V_{inv,0} - \dfrac{1}{2}\zeta\Delta\psi_s + \zeta V_T\right)\Delta\psi_s}\right]. \tag{3.55}$$

Instead of expressing ψ_s as a function of x, x has been represented as a function of ψ_s. This is to make future integration calculations simpler.[9] Since the drain and source terminals for the channel region in LDMOS are D_i and S terminals, charge partitioning is done between those two terminals. Now one can proceed to calculate various charges as follows

$$\begin{aligned}
Q_G^{ch} &= WC_{ox}\int_0^{L_{ch}}\left(V_{surf,0} + V_{dep,0}\right) - \left(\psi_s(x) - \psi_{s,0}\right)dx \\
Q_{D_i}^{ch} &= -WC_{ox}\int_0^{L_{ch}}\left(\frac{x}{L_{ch}}\right)\left(V_{surf,0} - \zeta\left(\psi_s(x) - \psi_{s,0}\right)\right)dx \\
Q_S^{ch} &= -WC_{ox}\int_0^{L_{ch}}\left(1 - \frac{x}{L_{ch}}\right)\left(V_{surf,0} - \zeta\left(\psi_s(x) - \psi_{s,0}\right)\right)dx.
\end{aligned} \tag{3.56}$$

[9] If ψ_s is represented as a function of x, then one encounters polynomial under square root during the integration computation which is cumbersome to solve. Writing x in terms of ψ_s results in solving quadratic expression under integral.

After integration, various charge expressions are

$$Q_G^{ch} = C_{ox} W L_{ch} \left[V_{GB} - V_{FB}^{ch} - \frac{1}{2}\left(\psi_{sD_i} + \psi_{ss}\right) + \frac{F_{ch}}{12\zeta} \Delta V_{GT} \right]$$

$$Q_{D_i}^{ch} = -\frac{C_{ox}}{2} W L_{ch} \left[\bar{V}_{GT} - \frac{\Delta V_{GT}}{6} \left(1 - \frac{F_{ch}}{2} - \frac{F_{ch}^2}{20} \right) \right] \tag{3.57}$$

$$Q_S^{ch} = -\frac{C_{ox}}{2} W L_{ch} \left[\bar{V}_{GT} - \frac{\Delta V_{GT}}{6} \left(1 - \frac{F_{ch}}{2} - \frac{F_{ch}^2}{20} \right) \right]$$

where

$$\Delta V_{GT} = V_{surf,0} - V_{surf,L_{ch}},\ \bar{V}_{GT} = \frac{V_{surf,0} + V_{surf,L_{ch}}}{2},\ F_{ch} = \frac{\Delta V_{GT}}{\bar{V}_{GT} + \zeta V_T}. \tag{3.58}$$

The surface potentials $\psi_{s,0}^{ch}$ and $\psi_{s,L_{ch}}^{ch}$ are computed using a surface potential function (Jia *et al.*, 2011). The surface potential at the source and D_i terminal can be written as

$$\begin{aligned} \psi_{s,0}^{ch} &= \psi\left[V_{GB} - V_{FB,ch}, V_{SB}, k_{ch}\right] \\ \psi_{s,L_{ch}}^{ch} &= \psi\left[V_{GB} - V_{FB,ch}, V_{DiB}, k_{ch}\right]. \end{aligned} \tag{3.59}$$

3.2.4 Formulation of charge in drift region

Charge modeling in drift region is algorithmically similar to the channel region. Since the current formulation is done in terms of quasi-Fermi potential V_c, charge modeling is also done in accordance with that. At any given bias, net charge density in the drift region can be written as

$$Q_n^{dr} = -qN_{dr}t_{si} - C_{ox}\left(V_{GC} - V_{FB,dr} - \psi_s^{dr}\right). \tag{3.60}$$

If we consider $V_n^{dr} = -\frac{Q_n^{dr}}{C_{ox}}$, and upon linearizing the potential with respect to D_i terminal, one gets

$$V_n^{dr} = V_n^{dr}\,|_{V_c = V_{D_i}} - \left(V_c - V_{D_i}\right). \tag{3.61}$$

The above expression is substituted in the drift current expression and integrated from 0 to x to obtain

$$I_{dr} x = W \mu_{dr} C_{ox} \left[\int_{V_{D_i}}^{V_c} \left(V_n^{dr}\,|_{V_c = V_{D_i}} - \left(V_c - V_{D_i}\right) \right) dV_c \right]. \tag{3.62}$$

Upon replacing I_{dr} with (3.22) and simplifying one gets

$$x = L_{dr}\left[\frac{\left(V_n^{dr}\mid_{V_c=V_{D_i}}+V_{D_i}\right)\left(V_c(x)-V_{D_i}\right)-\dfrac{V_c(x)^2}{2}}{\left(V_n^{dr}\mid_{V_c=V_{D_i}}-0.5V_{D'D_i}\right)V_{D'D_i}}\right]. \tag{3.63}$$

The analogous drain and source terminals for the drift region in LDMOS are $D^{'}$ and D_i terminals and charge partition is done between those two terminals. Now one can proceed to calculate various charges as follows

$$\begin{aligned}
Q_G^{dr} &= WC_{ox}\int_0^{L_{dr}}\left(V_n^{dr}\mid_{V_c=V_{D_i}}-(V_c-V_{D_i})\right)dx\\
Q_{D'}^{dr} &= -WC_{ox}\int_0^{L_{dr}}\left(\frac{x}{L_{dr}}\right)\left(V_n^{dr}\mid_{V_c=V_{D_i}}-(V_c-V_{D_i})\right)dx\\
Q_{D_i}^{dr} &= -WC_{ox}\int_0^{L_{dr}}\left(1-\frac{x}{L_{dr}}\right)\left(V_n^{dr}\mid_{V_c=V_{D_i}}-(V_c-V_{D_i})\right)dx.
\end{aligned} \tag{3.64}$$

After integration, various charge expressions are

$$\begin{aligned}
Q_G^{dr} &= C_{ox}WL_{dr}\left[\frac{1}{2}\left(V_{GD_i}^{dr}+V_{GD'}^{dr}-2V_{FB}^{dr}\right)-\frac{1}{2}\left(\psi_{sD_i}^{dr}+\psi_{sD'}^{dr}\right)+\frac{F^{dr}}{12}\Delta V_q^{dr}\right]\\
Q_{D'}^{dr} &= -\frac{C_{ox}}{2}WL_{dr}\left[\bar{V}_q^{dr}-\frac{\Delta V_q^{dr}}{6}\left(1-\frac{F^{dr}}{2}-\frac{F^{dr^2}}{20}\right)\right]\\
Q_{D_i}^{dr} &= -\frac{C_{ox}}{2}WL_{dr}\left[\bar{V}_q^{dr}-\frac{\Delta V_q^{dr}}{6}\left(1-\frac{F^{dr}}{2}-\frac{F^{dr^2}}{20}\right)\right]
\end{aligned} \tag{3.65}$$

where

$$\Delta V_q^{dr} = V_{nD_i}^{dr}-V_{nD'}^{dr},\ \bar{V}_q^{dr}=\frac{V_{nD_i}^{dr}+V_{nD'}^{dr}}{2},\ F^{dr}=\frac{\Delta V_q^{dr}}{\bar{V}_q^{dr}+\dfrac{qN_{dr}t_{si}}{C_{ox}}}. \tag{3.66}$$

The surface potentials $\psi_{sD_i}^{dr}$ and $\psi_{sD'}^{dr}$ are computed using the same surface potential function as discussed in previous section. The surface potential at terminals D_i and $D^{'}$ are

$$\begin{aligned}
\psi_{sD_i}^{dr} &= -\psi\left[-V_{GD_i}+V_{FB,dr},V_{D_iB},k_{dr}\right]\\
\psi_{sD'}^{dr} &= -\psi\left[-V_{GD'}+V_{FB,dr},V_{D'B},k_{dr}\right].
\end{aligned} \tag{3.67}$$

Since there are no charges in Reg-III which depend on gate or drain bias voltages,

Reg-III has been neglected from the charge formulation. Now that the charge in channel and drift region has been calculated, these charges are assigned to various terminals as follows

$$\begin{aligned} Q_G &= Q_G^{ch} + Q_G^{dr} \\ Q_S &= Q_S^{ch} \\ Q_{D_i} &= Q_{D_i}^{ch} + Q_{D_i}^{dr} \\ Q_{D'} &= Q_{D'}^{dr} \\ Q_B &= -\left(Q_G + Q_S + Q_{D_i} + Q_D^{'}\right). \end{aligned} \tag{3.68}$$

Note that no charge has been explicitly given to the drain terminal. Any variation in drain voltage is reflected as a change in the internal nodes D_i and $D^{'}$ which appropriately change the displacement current giving rise to a net displacement current from the drain terminal. These charges are modeled as $\frac{dQ}{dt}$ current sources which has been implemented in an equivalent circuit as shown in Fig 3.4.

CHAPTER 4

RESULTS AND DISCUSSION

Device simulations are carried out for HV SOI-LDMOS structure using commercially available device simulator TCAD MEDICI. The developed model is implemented in Verilog-AMS and simulated using Spectre from Cadence. In this chapter, the model results obtained from Verilog-A are compared against MEDICI results for model validation. In all the plots, solid lines represent Verilog-A model results and dotted lines represent MEDICI simulation results.

4.0.5 Static LDMOS currents

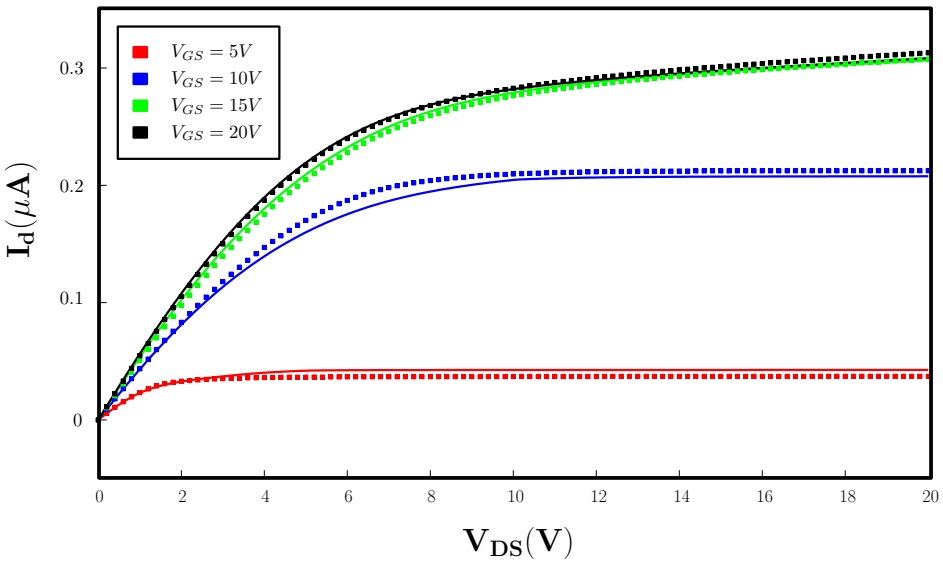

Figure 4.1: Comparison of $I_D - V_{DS}$ plots simulated for $V_{GS} = 5$, 10, 15 and 20 V, in MEDICI with the model.

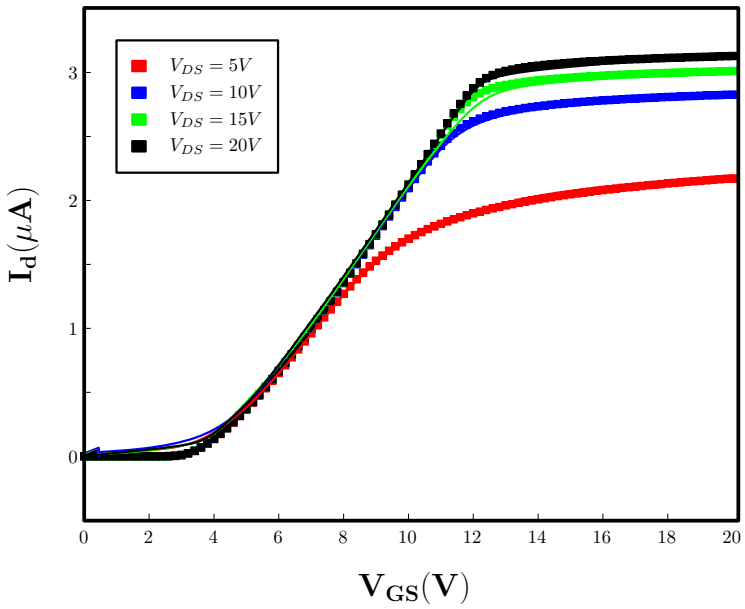

Figure 4.2: Comparison of $I_D - V_{GS}$ plots simulated for V_{DS} = 5, 10, 15 and 20 V, in MEDICI with the model.

Figures 4.1 and 4.2 show drain currents plotted against the drain and gate voltages. Up to V_{GS} = 10 V, it is velocity saturation in Reg-I which is responsible for current saturation. Beyond that, current saturation is due to quasi-saturation in Reg-III. The slight increase of drain current with V_{DS} is due to drift length modulation. From Fig 4.1 and 4.2 it can be seen that the drain current from model shows excellent agreement with the MEDICI simulation results.

4.0.6 LDMOS Charges and Capacitances

Capacitances of LDMOS are extracted by applying a small signal voltage at a frequency f to a particular terminal and extracting the imaginary part of the current flowing from different terminals. These imaginary currents arise due to the $\frac{dQ}{dt}$ current terms in the equivalent circuit model. Net small signal current flowing from a terminal can be written as

$$i_m = (g_{mn} + j\omega C_{mn})\, v_n \tag{4.1}$$

where small signal voltage is applied at terminal m and the current flowing from terminal n is measured. The capacitance can now be extracted as

$$C_{mn} = (2\delta_{mn} - 1)\, Im\left\{\frac{Y_{mn}}{2\pi f}\right\} \tag{4.2}$$

where Y_{mn} is the conductance between terminals m and n. The frequency chosen for the simulation is 100 MHz to ensure that one operates well within the quasi-static regime.

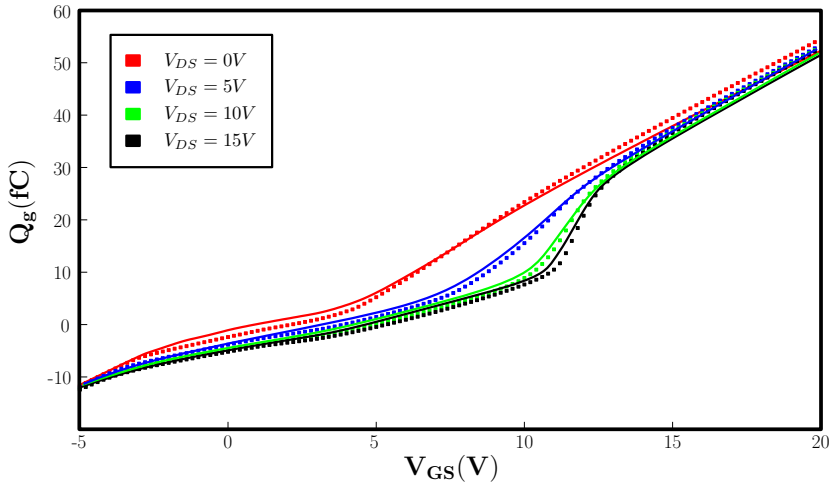

Figure 4.3: Comparison of $Q_G - V_{GS}$ plots simulated for $V_{DS} = 0$, 5, 10 and 15, in MEDICI with the model.

To ensure that a charge model is accurate, one must compare the gate charge Q_g model with the MEDICI simulations to ensure that the net charge matches well. Only when the gate charge matches well, other charges can be compared. Fig 4.3 shows Q_g as a function of V_{GS}. There is an excellent agreement of the model with MEDICI simulations. It is interesting to note that for negative values of V_{GS} and for large values of V_{GS}, the graph is linear. When V_{GS} is negative, channel is in accumulation condition and drift region is in inversion and when it is a large value, channel is in inversion and drift region is in accumulation. Accumulation/inversion region is where the charge variation is linear with respect to the gate voltage. Humps in the charge curve correspond to the case where the drift region is in transition from depletion to accumulation condition. Since V_{GC} keeps decreasing as one increases V_{DS}, this hump shifts to higher values of V_{GS} as V_{DS} is raised.

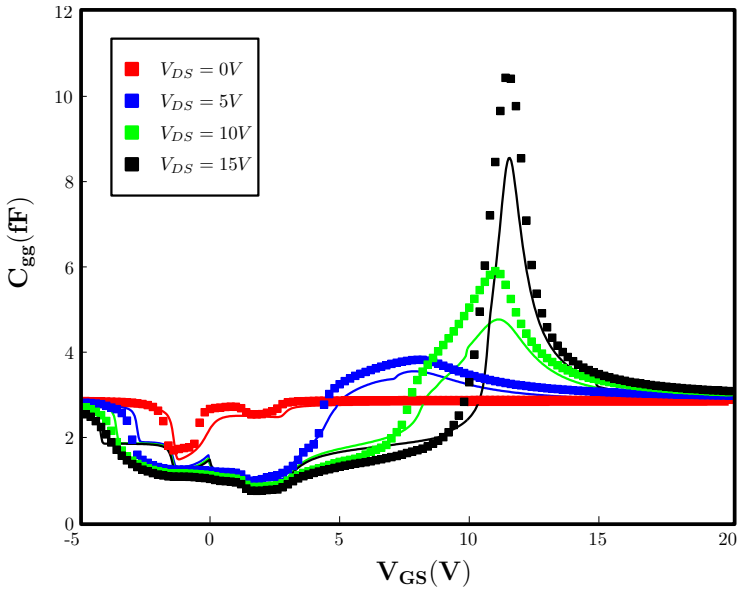

Figure 4.4: Comparison of $C_{GG} - V_{GS}$ plots simulated for $V_{DS} = 0$, 5, 10 and 15, in MEDICI with the model.

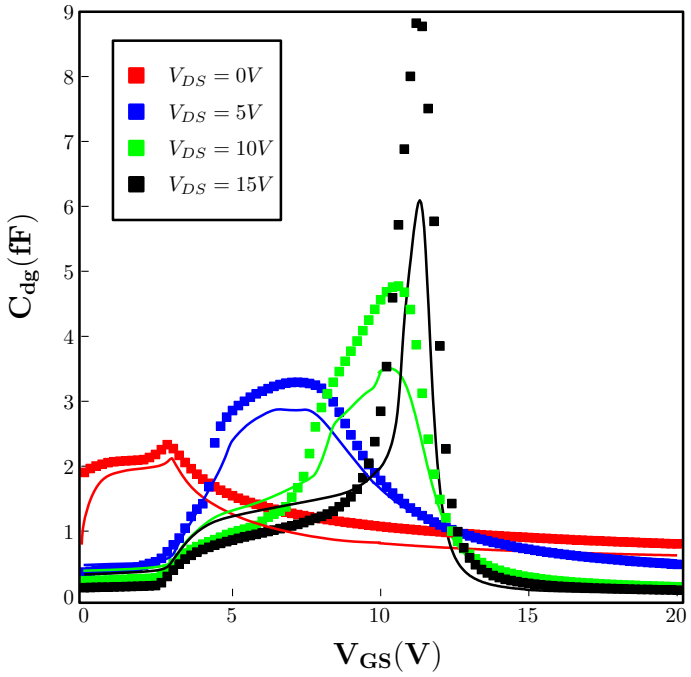

Figure 4.5: Comparison of $C_{DG} - V_{GS}$ plots simulated for $V_{DS} = 0$, 5, 10 and 15, in MEDICI with the model.

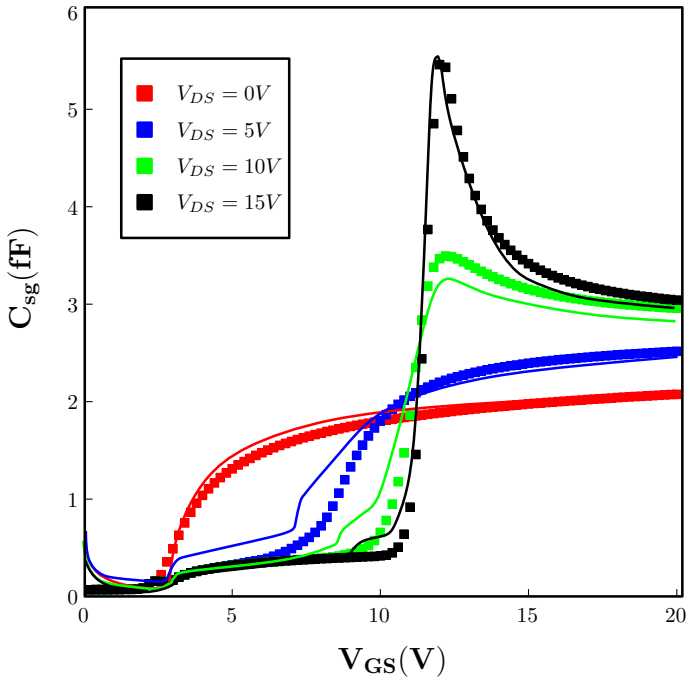

Figure 4.6: Comparison of $C_{SG} - V_{GS}$ plots simulated for $V_{DS} = 0$, 5, 10 and 15, in MEDICI with the model.

Figures 4.4, 4.6 and 4.5 show comparison of the capacitance model with MEDICI simulations. In C_{gg} curve, one can observe that for negative values of V_{GS} and for large values of V_{GS}, capacitance is constant. Since these two regions correspond to accumulation/inversion regions, charge variation is linear with respect to V_{GS}. Since C_{gg} is the derivative of the gate charge, it turns out to be constant in these two regions. The humps in the capacitance curves occur due to the transition from depletion to accumulation condition in the drift region under gate oxide.

C_{dg} and C_{sg} are the capacitances obtained from the partitioned charges. One can notice that for negative values of V_{GS}, both of them go to zero. This is because the bulk terminal is responsible for charges under negative bias and any variation in the gate bias has no effect on drain or source charges. For large values of V_{GS}, C_{dg} goes to zero whereas C_{sg} reaches a finite value. This happens because in high V_{GS} regime, the variation of internal node voltages with V_{DS} is negligible. Since the drain current depends upon the voltage difference $V_{DD'}$, there is negligible variation in the drain current. Source charge, on the other hand, is a fraction of the inversion charge present in the channel region. Any variation in the gate voltage results in a linear change in the source charge which gives rise to a constant C_{sg} curve for higher values of V_{GS}.

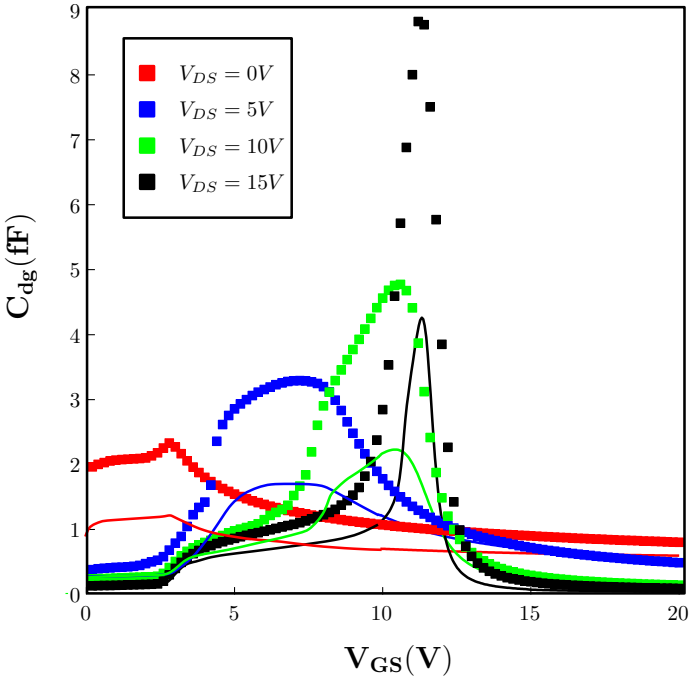

Figure 4.7: Comparison of $C_{DG} - V_{GS}$ plots simulated for V_{DS} = 0, 5, 10 and 15, in MEDICI with the MM20 model.

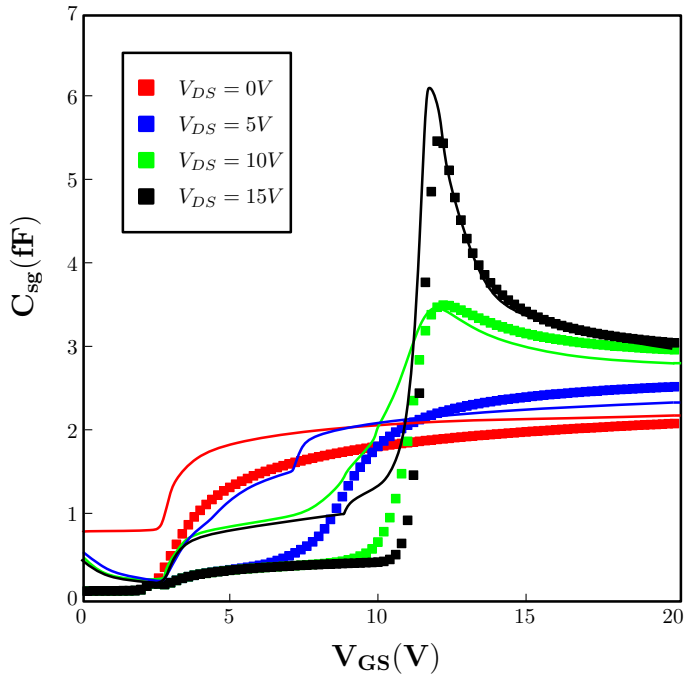

Figure 4.8: Comparison of $C_{SG} - V_{GS}$ plots simulated for V_{DS} = 0, 5, 10 and 15, in MEDICI with the MM20 model.

Figures 4.7 and 4.8 show the comparison of capacitances, C_{dg} and C_{sg} obtained from the MM20 model against MEDICI simulations. One can observe that the match is not good and this is attributed to the partitioning approach used by them. The assumption that $I_{ch}(t)$ and $I_{dr}(t)$ are equal at all points of time fails giving rise to an error in the capacitance plots. This error is mitigated by adding an extra term $\frac{d}{dt}\left(\frac{I_{dr}L_{ch}\tau}{L_{ch}+L_{dr}}\right)$

to terminals S and D' as discussed in 3.2.2. Figures 4.9 and 4.10 show the capacitance curves after the addition of the above extra term. One can observe there is an improvement in the capacitance plots, thereby showing the validity of claim made in 3.2.2.

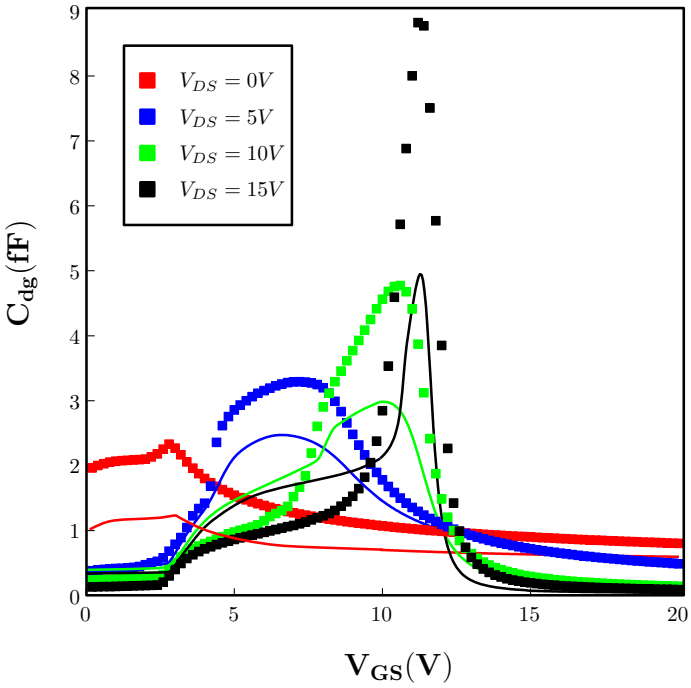

Figure 4.9: Comparison of $C_{DG} - V_{GS}$ plots simulated for V_{DS} = 0, 5, 10 and 15, in MEDICI with the modification done to MM20 model.

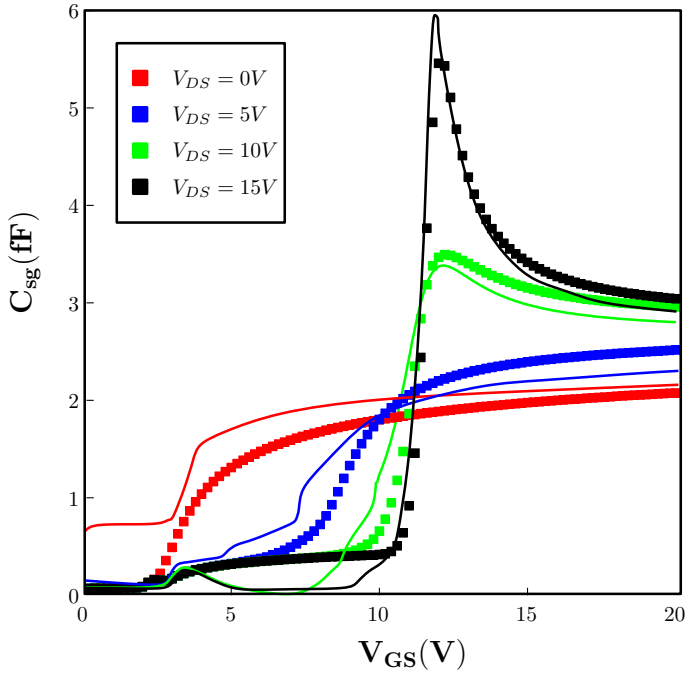

Figure 4.10: Comparison of $C_{SG} - V_{GS}$ plots simulated for V_{DS} = 0, 5, 10 and 15, in MEDICI with the modification done to MM20 model.

Figures 4.11 - 4.18 show plots of various capacitance models against MEDICI simulations. There is reasonable accuracy in the model and it is successfully able to predict capacitance between any two terminals for any given set of bias values.

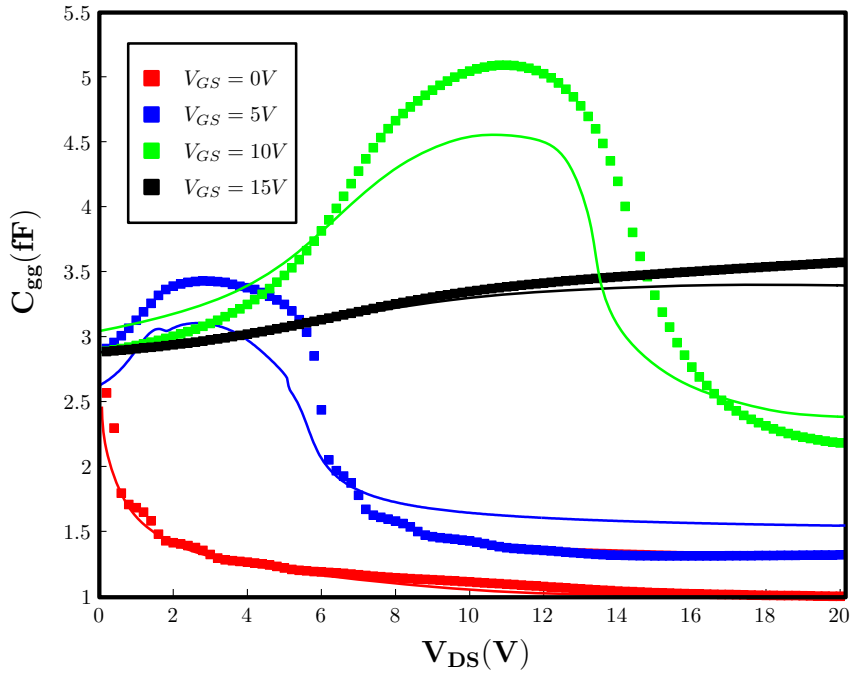

Figure 4.11: Comparison of $C_{GG} - V_{DS}$ plots simulated for $V_{GS} = 0$, 5, 10 and 15, in MEDICI with the model.

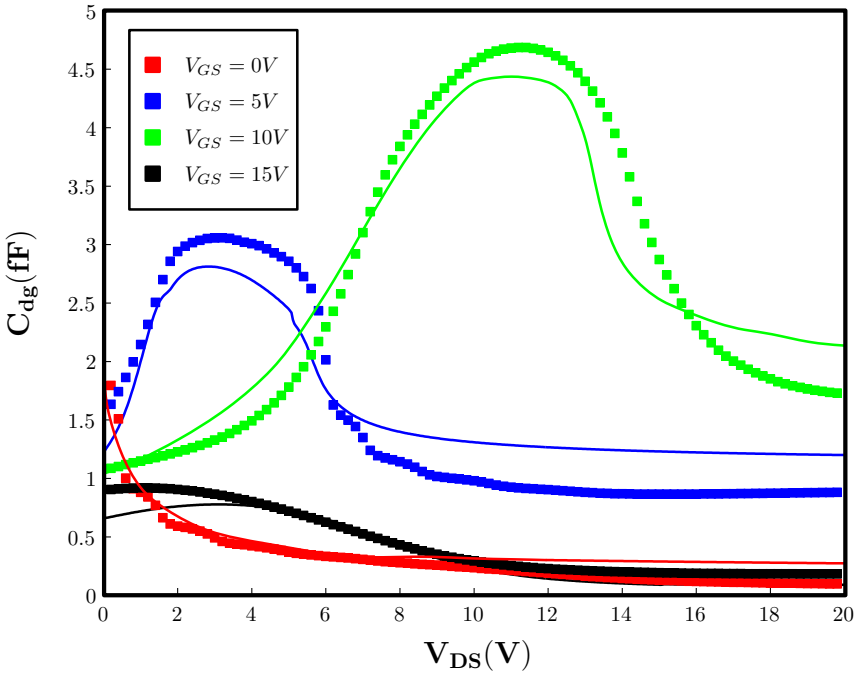

Figure 4.12: Comparison of $C_{DG} - V_{DS}$ plots simulated for $V_{GS} = 0$, 5, 10 and 15, in MEDICI with the model.

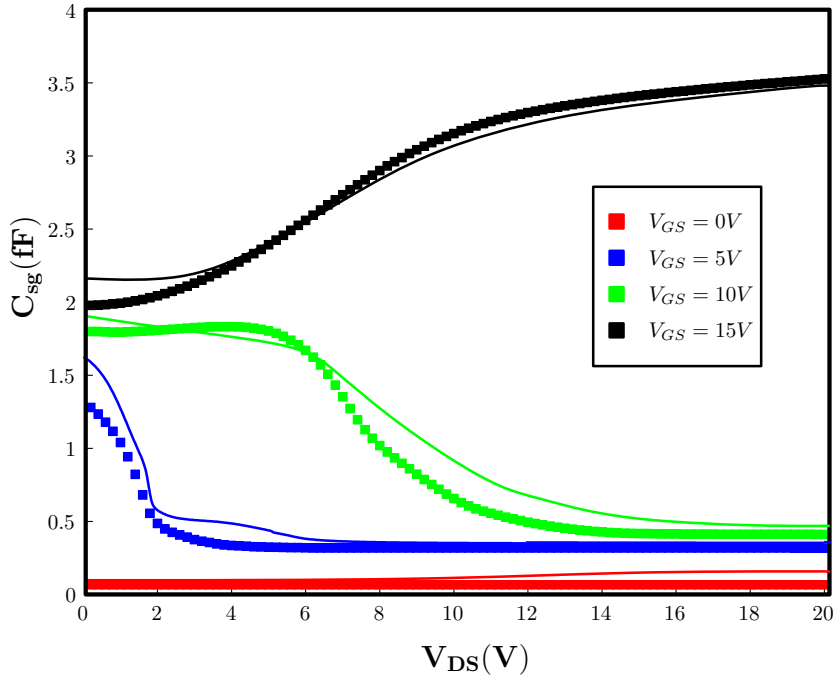

Figure 4.13: Comparison of $C_{SG} - V_{DS}$ plots simulated for $V_{GS} = 0$, 5, 10 and 15, in MEDICI with the model.

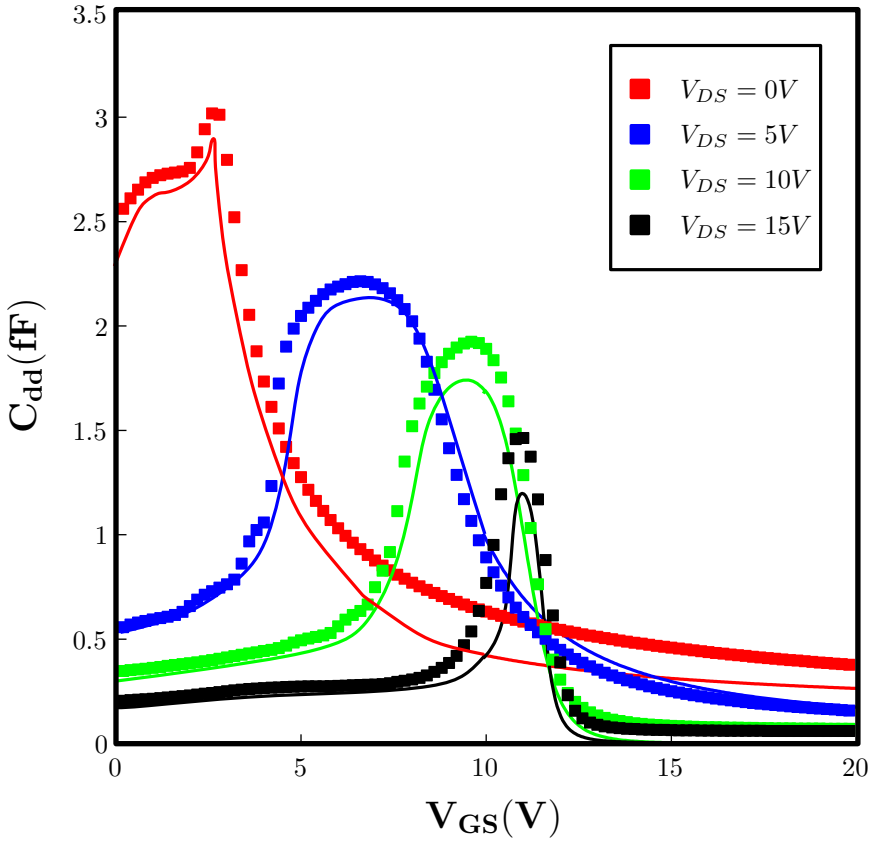

Figure 4.14: Comparison of $C_{DD} - V_{GS}$ plots simulated for $V_{DS} = 0$, 5, 10 and 15, in MEDICI with the model.

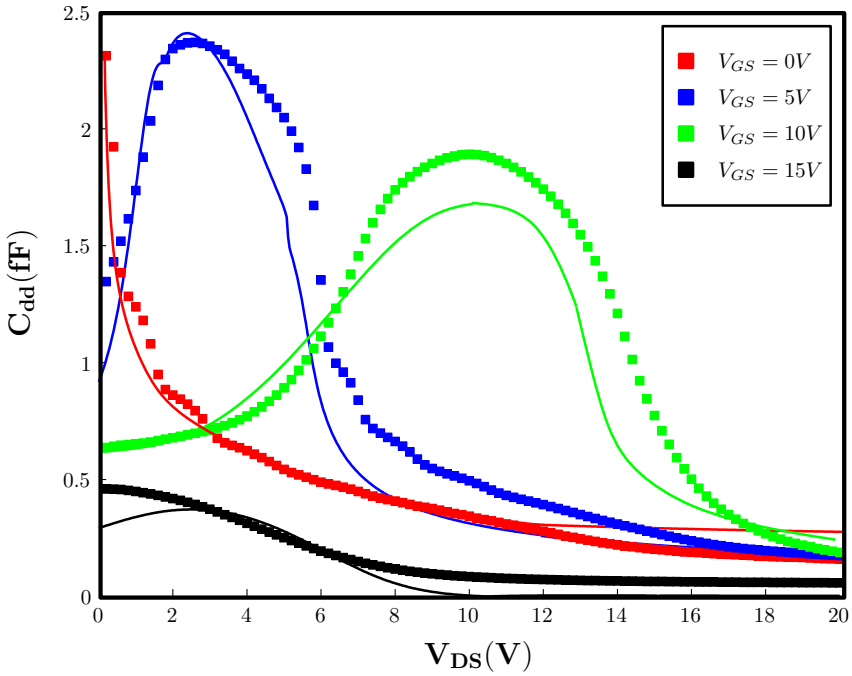

Figure 4.15: Comparison of $C_{DD} - V_{DS}$ plots simulated for $V_{GS} = 0$, 5, 10 and 15, in MEDICI with the model.

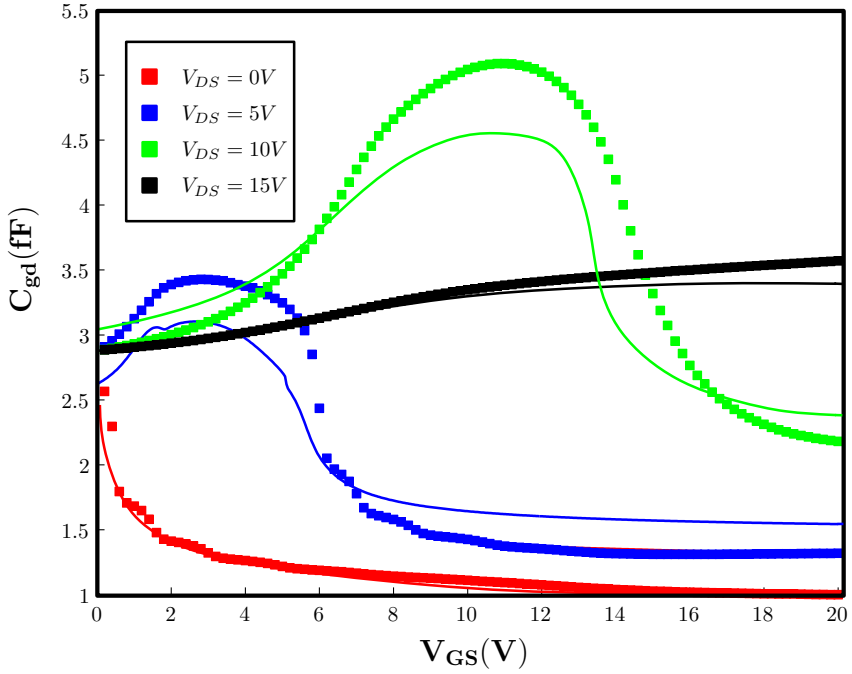

Figure 4.16: Comparison of $C_{GD} - V_{GS}$ plots simulated for $V_{DS} = 0$, 5, 10 and 15, in MEDICI with the model.

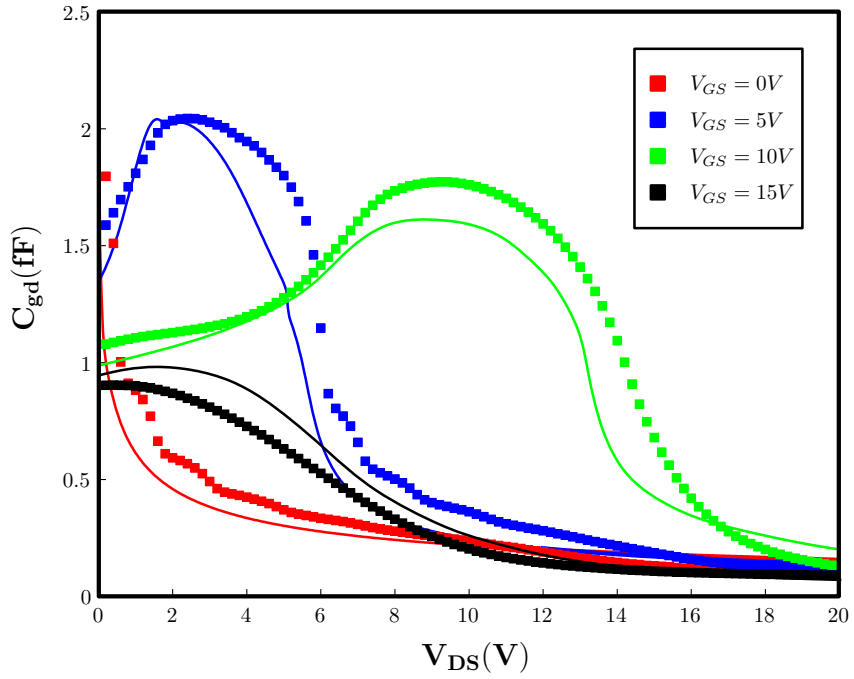

Figure 4.17: Comparison of $C_{GD} - V_{DS}$ plots simulated for $V_{GS} = 0$, 5, 10 and 15, in MEDICI with the model.

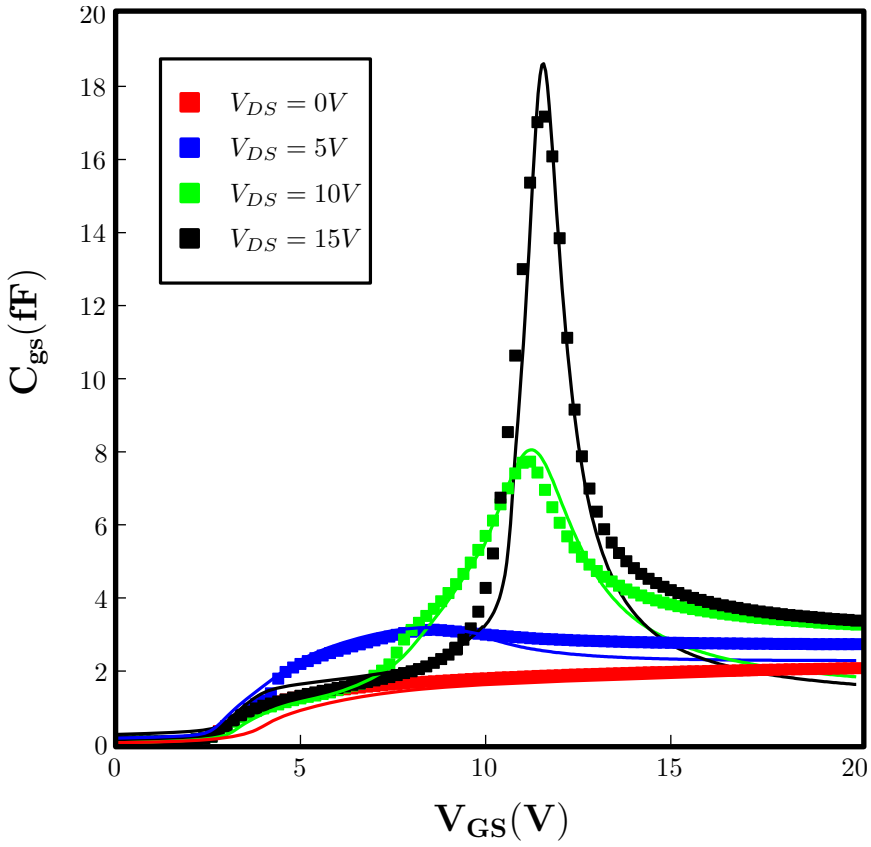

Figure 4.18: Comparison of $C_{GS} - V_{GS}$ plots simulated for $V_{DS} = 0$, 5, 10 and 15, in MEDICI with the model.

4.0.7 Transient Currents

In order to test the validity of our claim that the conduction currents in Reg-I and Reg-II need not be identical at all points of time, a transient simulation is done in MEDICI and compared with the results obtained from Verilog-A with the equivalent circuit as shown in Fig 3.4. The drain voltage is held constant and the gate voltage is ramped up from 0 to 20V, held constant at 20V and ramped down to 0V (Fig 4.19).

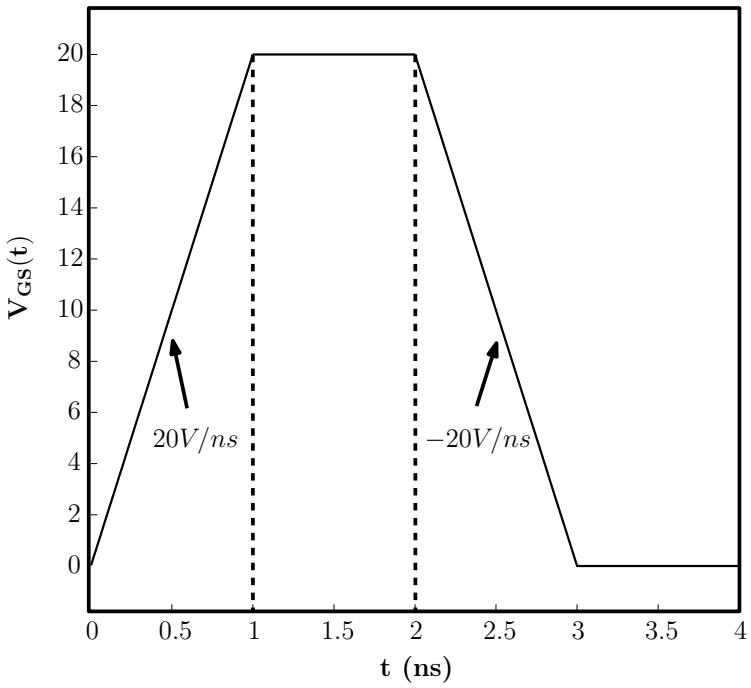

Figure 4.19: Gate voltage ramped up to 20 V and ramped down again to 0 V.

The conduction currents I_{ch} and I_{dr} are extracted from transient simulations and compared against the transient simulation results from Verilog-A. Fig 4.20 shows the transient response of the conduction currents when V_{DS} is held at 5V. The plot indicates that there is good agreement between the simulation and MEDICI results proving that our claim is correct. It can be observed that $I_{ch}(t)$ is different from $I_{dr}(t)$ during the rising and falling part of the current. This is because Reg-I and II are electrostatically different from each other. Any sudden rise in voltage will result in unequal conduction currents flowing in Reg-I and II. The difference in the two currents is the displacement current that flows from terminal D_i to bulk. However, they are equal during the steady state portion where V_{GS} is held constant. This clearly shows that the conduction currents can be equal only under steady state and not under any given condition.

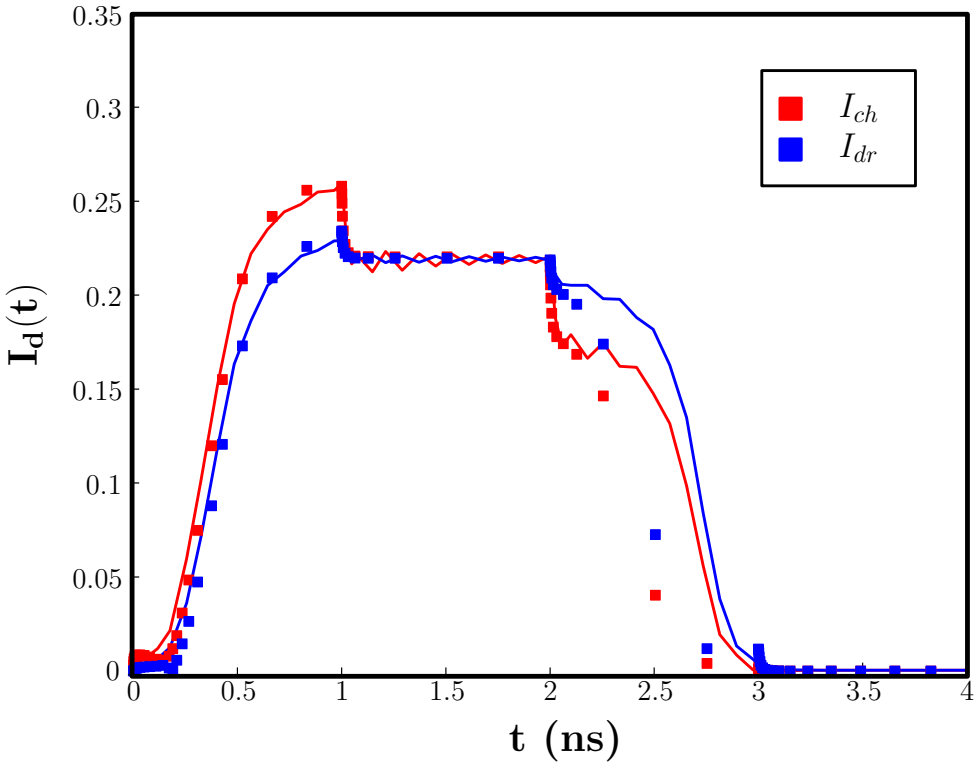

Figure 4.20: Response of I_{ch} and I_{dr} when V_{GS} is ramped up and ramped down keeping V_{DS}=5V.

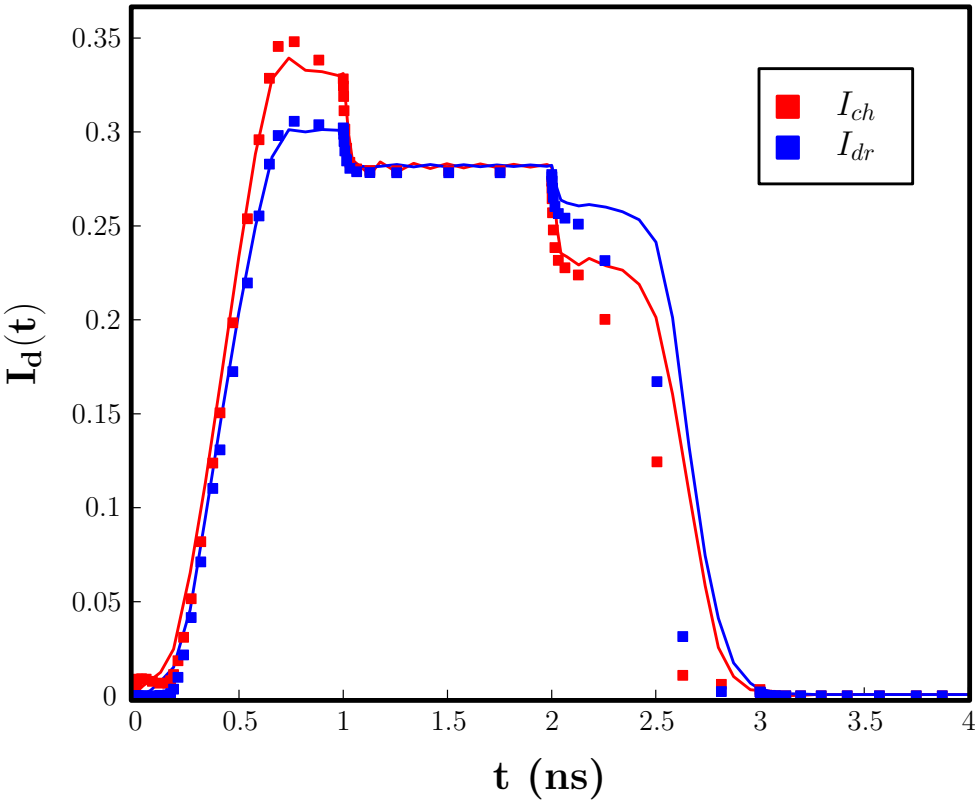

Figure 4.21: Response of I_{ch} and I_{dr} when V_{GS} is ramped up and ramped down keeping V_{DS}=10V.

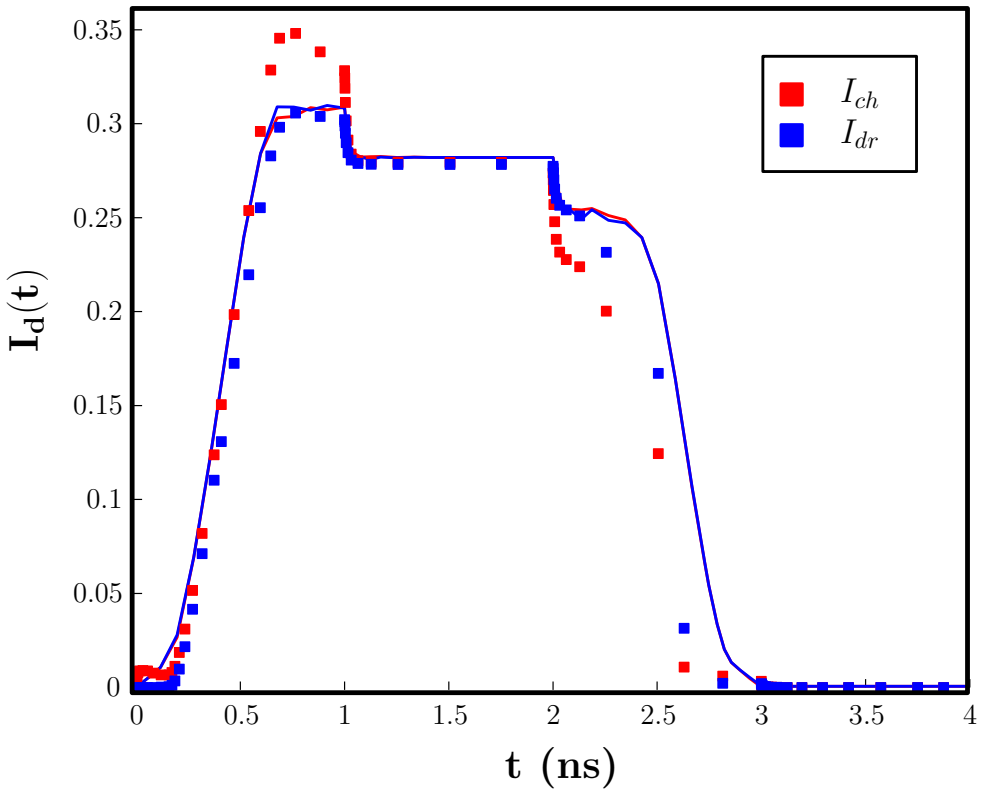

Figure 4.22: Response of I_{ch} and I_{dr} from MM20 model when V_{GS} is ramped up and ramped down keeping V_{DS}=10V.

Fig 4.21 and 4.22 show the comparison between the results obtained using our equivalent circuit and MM20 equivalent circuit. Since the MM20 model forces the two conduction currents to be equal, the Verilog-A result shows both the currents to be same. This results in I_{ch} being underestimated during the rise time and overestimated during the fall time. This clearly demonstrates the need for an additional displacement current source from D_i to bulk to account for the difference in these conduction currents. Fig 4.23 and Fig 4.24 show the current response when V_{DS} is maintained at 15V and 20V. There is good agreement between simulation and MEDICI plots indicating that the model is valid even for high values of V_{DS}. One common trend in all these plots is that the rising part of the curve matches perfectly whereas there is a mismatch in the falling portion of the curve. This is because the charge model still is not perfect. This is evident from the capacitance curves seen in the previous section where the match is not perfect.

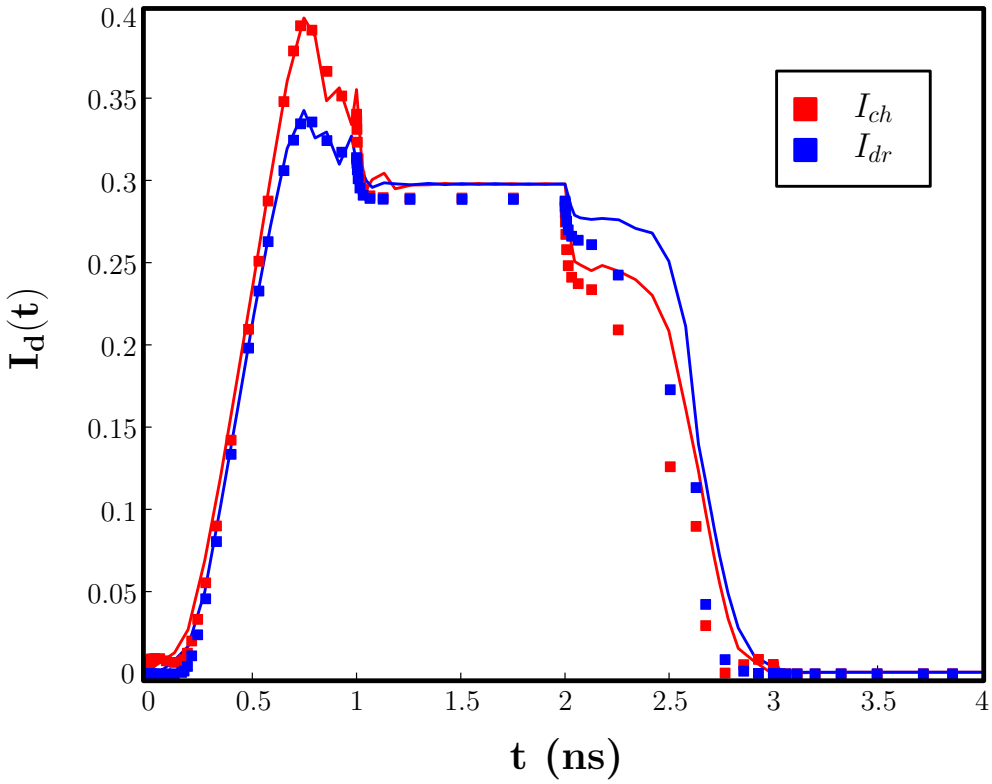

Figure 4.23: Response of I_{ch} and I_{dr} when V_{GS} is ramped up and ramped down keeping V_{DS}=15V.

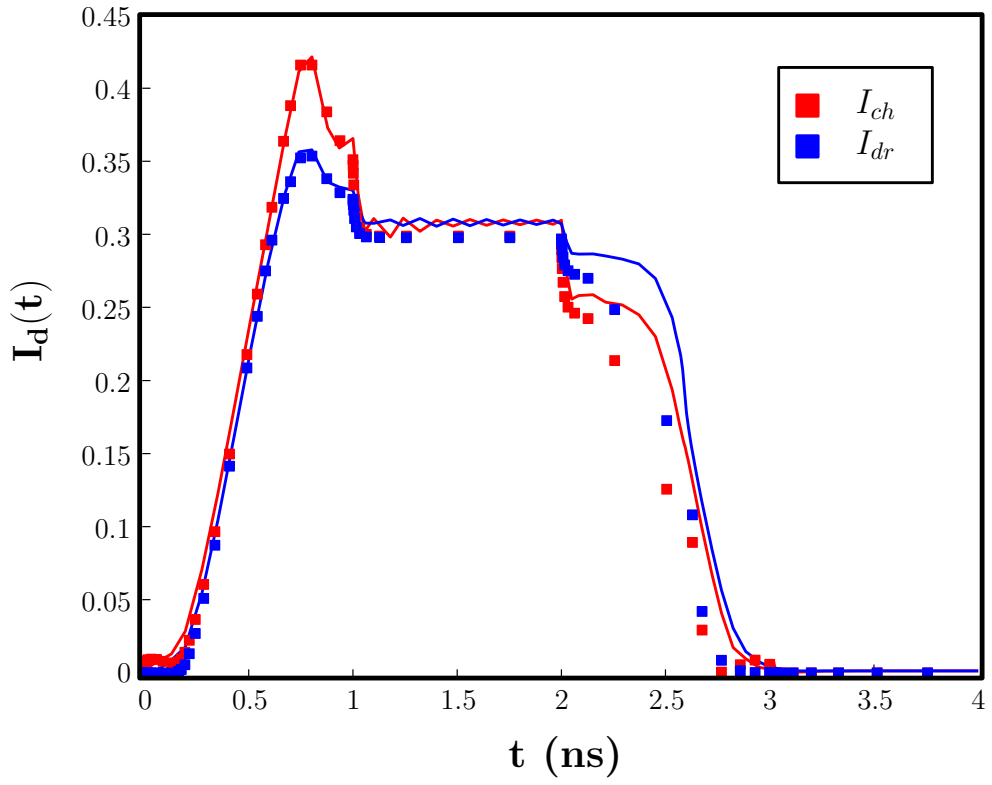

Figure 4.24: Response of I_{ch} and I_{dr} when V_{GS} is ramped up and ramped down keeping V_{DS}=20V.

4.0.8 Reasons for inaccuracies in the capacitance plots

Though the capacitance model curves follow the trend of MEDICI simulation curves, the match is still not perfect. Some of the reasons for the inaccuracies are

1. **Non-existence of a large signal partition function in the presence of field dependent mobility**

   (Aarts *et al.*, 2006) and (Roy *et al.*, 2007) clearly state the non-existence[1] of a large signal partition function for MOSFET in the presence of field dependent mobility or lateral doping gradient. In our analysis, we have neglected the doping gradient but we still have field dependent mobility. So, strictly speaking WD type partitioning cannot be applied to LDMOS. The only reason we have adopted it is due to its ease of integration into Verilog-A and its relatively small error in computing various charges. If one has to be rigorous, one must do a small signal analysis and find the capacitances or use the expression for capacitances as given in the above references. Both these approaches are computationally expensive and implementing them in Verilog-A is not at all easy.

   One approach that has been tried out is to use the small signal partition function $\frac{F(x)}{F(L)}$ as discussed in (Roy *et al.*, 2007) and try extending it to the large signal case. The small signal partition is given as

   $$F(x) = \int_0^x \left(\frac{g_0}{g_{eff}} exp\left(- \int_0^x \frac{1}{g_0} \left(\frac{g_0}{g_{eff}} \frac{\partial g_0}{\partial x} dx \right) \right) \right) dx \tag{4.3}$$

   where $g = W\mu Q_i$ and $g_{eff} = \left(g_0 + \frac{\partial g_0}{\partial E_0} E_0 \right)$. In case of the LDMOS under investigation, we have neglected lateral doping. Hence the exponential term is reduced to 1 and we are left with

   $$F(x) = \int_0^x \left(\frac{g_0}{g_{eff}} \right) dx \tag{4.4}$$

   If we assume a simple mobility field relation

   $$\mu = \frac{\mu_0}{1 + \left| \frac{E}{E_c} \right|} \tag{4.5}$$

   then it is possible to reduce $F(x)$ to a simple expression as follows.

   $$F(x) = \int_0^x \left(\frac{\mu}{\mu + \frac{\partial \mu}{\partial E} E} \right) dx = \int_0^x \left(1 + \frac{E}{E_c} \right) dx \tag{4.6}$$

   If we replace $E = -\frac{d\psi_s}{dx}$ in the channel region and substitute in the above expres-

[1] Non-existence should be interpreted as inability to find a function. It has not been proved until now, that such a function cannot exist.

sion, we get the partition function as

$$\frac{F(x)}{F(L)} = \frac{x + \dfrac{\psi_s(x) - \psi_{s,0}}{E_c}}{L + \dfrac{\psi_{s,L} - \psi_{s,0}}{E_c}} \tag{4.7}$$

One can observe that as E_C tends to infinity (implying constant mobility), then the partition function reduces to the WD function $\frac{x}{L}$. This function along with the charge expressions is integrable and one can get a closed form expression for Q_S, Q_{D_i} and $Q_{D'}$. However, on implementing the above expressions in Verilog-A, no significant improvement could be seen in the capacitance plots. This could be due to the simplified form of mobility model.

2. **Expressing mobility as a global function of Electric fields**

   It can be seen from 3.1.1 and 3.1.2 that the mobility model is defined in terms of potential drop across the region and no x dependence has been included in it. For example, if we assume a mobility model $\mu = \dfrac{\mu_0}{1 + \dfrac{E}{E_c}}$, then the electric field can be written either locally as $E = \dfrac{d\psi_s(x)}{dx}$ or globally as $E = \dfrac{V_{DiS}}{L_{ch}}$. These two approaches will yield different results during charge formulation. While computing the charges one integrates the potential with respect to x. If one has a mobility model which explicitly depends on x, then one needs to do a rearrangement of terms and then integrate it. If we consider 3.54 and try incorporating the mobility model above, it becomes clear that the final expression will be different. We tried using the local mobility model shown above and derived various charges from it With the charge expressions being implemented in Verilog-A, no improvement could be observed in the capacitance plots. This could be due to the simplified form of mobility model assumed. If one assumes a complex mobility model, then one cannot get a closed form expression. This poses serious problem in LDMOS capacitance modeling.

3. **Approximating the drift region with a 1D Poisson equation**

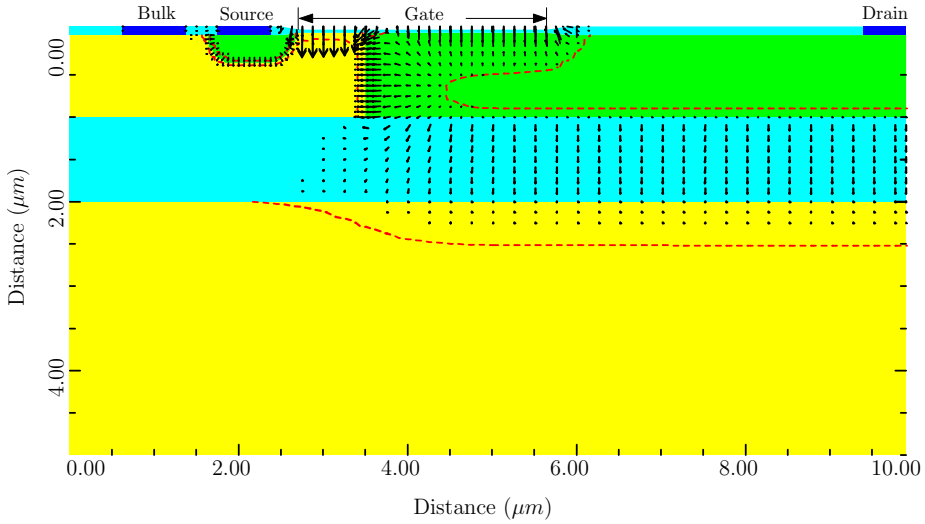

Figure 4.25: Electric Field lines for V_{GS} of 4 V and V_{DS} of 10 V.

Drift region under field oxide is under the effect of two dimensional electric field when it is in the depletion region. The vertical electric field is due to the gate terminal whereas the horizontal electric field is due to the depletion charges at the PN junction of channel and drift region. This implies that the total charge present in that region must be calculated using a 2D Poisson equation. But, the present model only considers the effect of gate terminal. One can observe from Fig 4.25 that the region near channel drift junction has electric fields at 45 degree angle. This means that the charge present in that region will be due to the combined contribution of gate and PN junction. Currently, this charge is assumed to come solely from gate. This means that the gate charge during the depletion mode in Reg-II is being overestimated. However, in accumulation mode all the charges are associated with the gate terminal. This is evident from the capacitance plots where the peaks of C_{GG} and C_{DG} do not match well (depletion mode) but the curve beyond $V_{GS} = 10$ V match well (accumulation mode).

4. **Bulk charge consideration in Reg-II**

   The charges that are taken into consideration in Reg-II are the depletion, accumulation and bulk charges. Under accumulation condition, current flows both through the accumulation layer and the bulk of Reg-II. In depletion condition, since the silicon film in Reg-II is either completely or partially depleted, total bulk charge $qN_{dr}t_{si}$ should not be taken into account. But in the current and charge formulation, total bulk charge has been considered both in accumulation as well as in depletion condition. In reality, the bulk charge tends to zero when Reg-II is in depletion mode and is equal to $qN_{dr}t_{si}$ when it is in accumulation mode. This could be one of the reasons for the inaccuracies in the capacitance plots. Including a bias dependence to the bulk charge term to account for the contribution made by it in depletion/accumulation mode could help resolving the issue.

CHAPTER 5

CONCLUSIONS AND SCOPE FOR FUTURE WORK

5.1 Findings of the thesis

In this work, the operation of HV SOI-LDMOS has been analyzed using results obtained from MEDICI simulations and a comprehensive physics based static and dynamic model to include static currents and capacitances has been proposed. The developed model has been implemented in Verilog-A.

The major contributions of the work are listed as following:

1. A comprehensive charge model has been proposed to model various capacitances. The device is separated into three regions and charges in each region are analyzed. It has been observed that channel region stays either in inversion/depletion or in accumulation mode and drift region stays in accumulation or in depletion mode depending upon the gate bias.

2. Charge partitioning theory has been analyzed and it has been found that the MM20 charge partitioning scheme is physically inconsistent. This inconsistency arises because conduction currents in different regions of the device have been assumed to be equal under any condition.

3. A modification to this partition scheme is proposed wherein an extra displacement current source is connected from the internal node D_i to bulk to account for the difference in the conduction currents. Capacitances derived from this modified equivalent circuit show good agreement with MEDICI simulations.

4. Reasons for imperfections in capacitance match have been discussed. Some of the important reasons are
   - Non-existence of large signal partition function in the presence of field-dependent mobility or lateral doping gradient.
   - Expressing mobility as a global function of electric fields.
   - Approximating the drift region with a 1D Poisson equation.
   - Bulk charge consideration in Reg-II

5.2 Scope for future work

1. The model assumes uniform doping concentration in the channel region. In practice, the doping varies laterally from source to drain end. This effect must be included for an efficient model.

2. There exists no large signal partition function in the presence of field dependent mobility and lateral doping gradient. Finding the capacitance through the small signal approach or using an approximate large signal partition function should help improve the capacitance model.

3. Charge in the drift region is modeled based on 1D electrostatic assumption. Due to the presence of PN junction, drift region charge will be due to the result of a 2D electric field. One must solve a 2D Poisson equation in the drift region to exactly arrive at the drift region charge value.

4. Dynamic model to explain the non-quasi static behavior and a comprehensive noise model to model various noise sources in LDMOS are two major areas yet to be explored.

5. Work in the direction of device scalability and parameter extraction is yet to be carried out. Device scalability ensures that the model is applicable for various lengths of Reg-I, II and III. Parameter extraction tries to extract various mobility and empirical parameters to be used in the model for a given device dimension.

APPENDIX A

MODEL PARAMETERS

Model parameters for SOI-LDMOS

($L_{ch} = 0.825\mu m$**,** $L_{dr} = 2.25\mu m$**,** $L_{LC} = 3.45\mu m$**)**

Model parameters	Dimension	Value
Oxide thickness (t_{ox})	nm	38
Silicon film thickness (t_{si})	μm	1
Reg-I mobility ($\mu_{0,ch}$)	cm^2/Vs	457
Reg-II mobility ($\mu_{0,dr}$)	cm^2/Vs	1100
Reg-III mobility (μ_{dr1})	cm^2/Vs	1100
Length of channel region (L_{ch})	μm	0.825
Length of Reg-II (L_{dr})	μm	2.25
Length of Reg-III (L_{dr1})	μm	3.45
Width (W)	μm	1
Doping concentration in Reg-I (N_{ch})	cm^{-3}	2×10^{17}
Doping concentration in Reg-II (N_{dr})	cm^{-3}	2×10^{16}
Flatband voltage in Reg-I ($V_{FB,ch}$)	V	-0.5
Flatband voltage in Reg-II ($V_{FB,dr}$)	V	-0.1
Velocity saturation parameter in channel ($\theta_{3,ch}$)	$1/V$	0.52
Channel mobility reduction parameter (θ_1)	$1/V$	0.025
Channel mobility reduction parameter (θ_2)	$1/\sqrt{V}$	0.03
Channel length modulation factor (λ_{ch})	$1/V$	0.005
DIBL factor in channel (m_{DIBL})	$1/V$	0
Velocity saturation parameter in Reg-II ($\theta_{3,dr}$)	$1/V$	0.24
Reg-II mobility reduction parameter (θ_{acc})	$1/V$	0.205
Velocity saturation parameter in Reg-III (θ_{dr1})	$-$	2.55
Velocity saturation parameter in Reg-III ($\theta_{1,dr1}$)	$-$	1.42
Drift length modulation parameter (λ_{dr1})	$1/V$	0.0062

Table A.1: Model parameters

APPENDIX B

MEDICI SOURCE CODE

MEDICI source code for SOI-LDMOS
($L_{ch} = 0.825\mu m$**,** $L_{dr} = 2.25\mu m$**,** $L_{LC} = 3.45\mu m$**)**

```
MESH  SMOOTH=1
X.MESH WIDTH=9.9 H1=0.125
Y.MESH N=1 L=-0.038
Y.MESH N=3 L=0.0
Y.MESH DEPTH=2.0 H1=0.125
Y.MESH DEPTH=3.0 H1=0.125
ELIMIN COLUMNS Y.MIN=1.1

SPREAD LEFT WIDTH=2.625 UP=1 LO=3 THICK=0.1 ENC=2
SPREAD RIGHT WIDTH=4.125 UP=1 LO=3 THICK=0.1 ENC=2
SPREAD LEFT WIDTH=100 UP=3 LO=4 Y.LO=0.125

REGION SILICON Y.MIN=0.0 Y.MAX=1.0 X.MIN=0 X.MAX=9.9
REGION OXIDE Y.MIN=1.0 Y.MAX=2.0 X.MIN=0 X.MAX=9.9
REGION SILICON Y.MIN=2.0 Y.MAX=5.0 X.MIN=0 X.MAX=9.9
REGION OXIDE IY.MAX=3

ELECTR NAME=GATE X.MIN=2.625 X.MAX=5.8 TOP
ELECTR NAME=SUBSTRATE X.MIN=0.6 X.MAX=1.5 IY.MAX=3
ELECTR NAME=SOURCE X.MIN=1.7 X.MAX=2.5 IY.MAX=3
ELECTR NAME=DRAIN X.MIN=9.3 IY.MAX=3.0

PROFILE N-TYPE N.PEAK=2.0E16 UNIFORM
+Y.MIN=0.0 Y.MAX=1.0 X.MIN= 3.5 X.MAX=9.9 OUT.FILE=M1
PROFILE P-TYPE N.PEAK=2.0E17 UNIFORM
+Y.MIN=0.0 Y.MAX=1.0 X.MIN= 0.0 X.MAX=3.5
PROFILE P-TYPE N.PEAK=3E15 UNIFORM
+Y.MIN=2.0 Y.MAX=5.0 X.MIN= 0 X.MAX=9.9
PROFILE N-TYPE N.PEAK=2E20 Y.JUNC=.34 X.MIN=1.9 WIDTH=0.5
+ XY.RAT=0.75
PROFILE P-TYPE N.PEAK=2E22 Y.JUNC=.34 X.MIN=0.75 WIDTH=0.5
+ XY.RAT=0.75
PROFILE N-TYPE N.PEAK=2E20 Y.JUNC=.34 X.MIN=9.4 WIDTH=0.5
+ XY.RAT=0.75

REGRID DOPING LOG IGNORE=OXIDE RATIO=2 SMOOTH=1
+ IN.FILE=M1
PLOT.2D GRID TITLE="DOPING REGRID" FILL SCALE
CONTACT NAME=GATE N.POLY
```

```
MODELS ANALYTIC FLDMOB CONSRH AUGER BGN PRPMOB
SYMB CARRIERS=0
METHOD ICCG DAMPED
SOLVE

REGRID POTEN IGNORE=OXIDE RATIO=0.2 MAX=1 SMOOTH=1
+ IN.FILE=M1
+ OUT.FILE=M2
PLOT.2D GRID TITLE="POT REGRID" FILL SCALE
+DEVICE =POSTCRIPT PLOT.OUT=ldmos-regrid.ps
SYMB CARRIERS=0
SOLVE OUT.FILE=M3

MESH IN.FILE=M2
LOAD IN.FILE=M3
MODELS   ANALYTIC FLDMOB CONSRH AUGER BGN PRPMOB
SYMB CARRIERS=0
METHOD ICCG DAMPED
SOLVE V(SOURCE)=0.0
SOLVE V(GATE)=0.0
SOLVE V(SUBSTRATE)=0.0
SOLVE V(DRAIN)=0
COMMENT SOLVE V(SUBSTRATE1)=0.0

MODELS ANALYTIC FLDMOB CONSRH AUGER BGN PRPMOB
SYMB NEWTON CARRIERS=2
SOLVE V(SOURCE)=0.0
SOLVE V(GATE)=20
SOLVE V(SUBSTRATE)=0.0
SOLVE V(DRAIN)=0

SOLVE  ELEC=DRAIN VSTEP=0.2 NSTEP=100 AC.ANAL FREQ=1E8 VSS=0.1
+TERM="(GATE,DRAIN,SOURCE,SUBSTRATE)"

PLOT.1D Y.AXIS="C(GATE,GATE)" X.AXIS=V(DRAIN) POINTS COLOR=2
+OUT.FILE= cgg-vds-vgs-20.dat
PLOT.1D Y.AXIS="C(DRAIN,GATE)" X.AXIS=V(DRAIN) POINTS COLOR=2
+OUT.FILE= cdg-vds-vgs-20.dat
PLOT.1D Y.AXIS="C(SOURCE,GATE)" X.AXIS=V(DRAIN) POINTS COLOR=2
+OUT.FILE= csg-vds-vgs-20.dat
PLOT.1D Y.AXIS="C(SUBSTRATE,GATE)" X.AXIS=V(DRAIN) POINTS COLOR=2
+OUT.FILE= cbg-vds-vgs-20.dat
PLOT.1D Y.AXIS="C(DRAIN,DRAIN)" X.AXIS=V(DRAIN) POINTS COLOR=2
+OUT.FILE= cdd-vds-vgs-20.dat
PLOT.1D Y.AXIS="C(GATE,DRAIN)" X.AXIS=V(DRAIN) POINTS COLOR=2
+OUT.FILE= cgd-vds-vgs-20.dat
PLOT.1D Y.AXIS="C(GATE,SOURCE)" X.AXIS=V(DRAIN) POINTS COLOR=2
+OUT.FILE= cgs-vds-vgs-20.dat
```

APPENDIX C

VERILOG-A SOURCE CODE

Verilog-A source code for SOI-LDMOS with static current and charge model ($L_{ch} = 0.825\mu m$, $L_{dr} = 2.25\mu m$, $L_{LC} = 3.45\mu m$)

```
`include "discipline.h"
`define LocalModel

module test(d, g, s, b);



`define GMIN        8E-8
`define GMIN1       9E-8
`define EPS1        2.0E-2
`define EPS2        1.0E-2
`define EPS3        4.0E-2
`define EPS4        1.0E-1
`define EPS5        1.0E-4
`define EPS6        2.02E-2
`define EPS7        2.0E-1

inout      d, g, s, b;
electrical d, g, s, b;
electrical di,d1;

`ifdef LocalModel
parameter real tox = 38e-7; //Oxide Thickness (cm)
parameter real tsi = 1e-6; //Silicon Film Thickness (m)
parameter real uc = 457; //Reg-I Mobility (cm^2/Vs)
parameter real ud = 1100; //Reg-II Mobility (cm^2/Vs)
parameter real udr = 1100e-4; //Reg-III Mobility (m^2/Vs)
parameter real llocos = 3.45e-6; //Reg-III length (m)
parameter real eox = 34.515e-14; //oxide epsilon (F/cm)
parameter real esi = 104.43e-14; //silicon epsilon (F/cm)
parameter real Cox = eox/tox; //Capacitance (F/cm^2)
parameter real w = 1e-6; //Width (m)
parameter real lc = 0.825e-6; //Reg-I length (m)
parameter real ld = 2.25e-6; //Reg-II length (m)
parameter real nc = 2e17; //P doping (/cm^3)
parameter real nd = 2e16; //N doping (/cm^3)
parameter real ndr = 2e22; //N doping near drain (/cm^3)
parameter real q = 1.6e-19; //Charge
parameter real phiT = 0.025; //Thermal voltage
parameter real phib_id = 0.820289; // = 2*V_T*ln(Nch/ni) (V)
```

```
parameter real phibd_id = 0.70516; // = 2*V_T*ln(Ndr/ni) (V)
parameter real ko_id = sqrt(2*esi*q*nc)*tox/eox;
//Body factor in Reg-I (V^0.5)
parameter real kod_id = sqrt(2*esi*q*nd)*tox/eox;
//Body factor in Reg-II (V^0.5)
parameter real vfb_i = -0.5; //Flatband voltage in Reg-I (V)
parameter real vfbd_i = -0.1; //Flatband voltage in Reg-II (V)
parameter real mexp_i =1.0;
parameter real the3_1 = 0.52; // \theta_{3,ch}
parameter real the1_i = 0.025; // \theta_1
parameter real the2_i = 0.03; // \theta_2
parameter real lamd_i = 0.005; // Drain length mod. factor
parameter real rd_id = ld/(w*ud*q*nd*tsi);
parameter real bet_id = uc*eox*w/(tox*lc);
//Constant coefficient appearing in Ich
parameter real betacc_id = ud*eox*w/(tox*ld);
//Constant coefficient appearing in Idr
parameter real the1acc_i = 0.205; // \theta_{1,acc}
parameter real the3d = 0.24; // \theta_{3,dr}
parameter real mexpd_i = 1.0;
parameter real sdibl_i = 0.001; // DIBL factor
parameter real ssf_i = 1e-12;
parameter real msdibl_i = 3.0; // DIBL factor
parameter real vp_i=0.05;
parameter real Vth=12;
parameter alp_i = 0.02;
parameter real rdrift1 =20000;
//rdrift1 is the resistance for thick locos part
parameter real thetax = 2.55; // \theta_{dr1}
parameter real kdrift = 1.0;
parameter real kch = 1.0;
parameter real kdr = 1.0;
//Above three parameters are for matching dimensions
parameter real thetax1 = 1.42; // \theta_{1dr1}
parameter real thetax3 = 0.0062;
// Drain length mod. factor in Reg-III
`else
`endif

//Definition of variables to be used later

real Vds,Vgs,Vsb,Vds2;
real absd, hyp_a, hyp_b, hyp_c, hyp_d, hyp_x;
real absx, absy, iabs, hypm_q, hypm_t, hypm_tm,
hypm_itm, hypm_it,mo_i;
real x,y;
real Vlimit, phio,Acc1,AccD,ko_2,ko2_4,kod_2,
kod2_4,i16phph;
real Vgb_t0,Vsb_t,Vds1,Vgs_t,Vgd_t,Vinv0_v,delta_v,
ksi_v,Vdis_sat0_v,Vsb_t0;
real Vdep0_v,Vdep00_v,Fmob_v,r,ro,f_lin,Voxp,Fmobacc,
```

```
bet_Fmob,bet_Facc,Gminko2,Gminkod2;
real denom1,Vdis_eff;
real Vgb,Vgdi_t,Vgdi_t_eff,Vdib_t,hypmarg,Vq_dr_eff,
tmp,denom,Vddi_eff,rd_i;
real Vddi;
real Vdis, Vd1s;
real Vddi_sat;
real  Vdis_sat_v,Vgb_eff0;
real ko_i,kod_i,betacc_i,bet_i,phib_i,phibd_i;
real Vdep0,Vinv0,psi_s00,Vdep00,Fmob,delta,ksi,Vdis_sat0,
Vdis_sat,Vdis_sat_eff,Vdibt_eff,psi_sL;
real psi_sat0,D,Vds_eff,delta_Vg,Vgb_t,Vgb_eff,
Dacc,psi_sat,psi_s0;
real Vinv_ex0,Vinv_exL,delta_psi_s,Vinv_av,Fmobsat,Gmob,
GdelL,G,invGtot,Idrift,rdrift,the3d_i1,i,H0,H1,
H2,H3,H,Vdisl,Vdish,delH,delVdis,Vdis0,error,Ich,Idr,the3d_i,the3_i;
real Ec,Vdd1,Idrift1,the3_i1,Vdis1,Idrift2,Idrift3;
real psis, psid, psisdr, psiddr,psim, psidiff,
delpsimepsm, qim, alpham, eh, psiprime, Qg,Qpn,
Qdi,Qb,Qdprime, delpsi1, delpsi2, term3, denomqim,
lchtilda,ldrtilda,Ecritch,Ecritdr,lcnew,ldnew;
real Vq_dr_di, Vq_dr_dig, Vq_dr_d1, Vq_dr_del, Vq_dr_delg,
Vq_dr_avg, Vq_dr_avgg, Fdr, Fdrg, Q_dr_di, zeta, Qgch, Qgdr,
Qddrmos, Qsdrmos, Qdchmos, Qschmos, Fact1, Fact2, Qs, Qd,
vinvo, vinvL, vgtdel, vgtavg, Fch, fact1ch, fact2ch, fact3ch,
fact1dr, fact2dr, fact3dr, psidiffdr, efactch, efactdr,
Igtran, Iditran, Id1tran, Istran, tau, Delaycharge;


//---------- Smoothing functions--------------

analog function real hyp;
        input x, eps;
        real  x, eps;
        real  absx, absd, a, b, d;
        begin
            absx  = (x>=0.0) ? x : -x;
            absd  = 2.0 * eps;
            if (absx < absd) begin
                d = x / absd;
                b = 1.0 + d * d;
                a = sqrt(b);
                if (x < 0.0)
                    hyp = eps / (a - d);
                else
                    hyp = x + eps / (a + d);
            end else begin
                d = absd / absx;
                b = 1.0 + d * d;
                a = sqrt(b);
                if (x < 0.0)
```

```
                    hyp = eps * d / (a + 1.0);
                else
                    hyp = x + eps * d / (a + 1.0);
            end
        end
endfunction

`define hypm(h,x,y,m) \
    if (x == 0.0 && y == 0.0) begin \
        h = 0.0; \
    end else begin \
        absx = (x>=0.0) ? x : -x; \
        absy = (y>=0.0) ? y : -y; \
        if (absx > absy) begin \
            hypm_q  = absy/absx; \
            hypm_t  = pow(hypm_q, 2.0*m); \
            hypm_tm = pow(1.0 + hypm_t, 0.5 / m); \
            h       = (x/absx) * (y/hypm_tm); \
        end else begin \
            hypm_q  = absx/absy; \
            hypm_t  = pow(hypm_q, 2.0*m); \
            hypm_tm = pow(1.0 + hypm_t, 0.5 / m); \
            h       = (y/absy) * (x/hypm_tm); \
        end \
    end

//-----------Surface Potential Calculation Function---------------


analog function real hfunc;
input term1, term2;
real term1, term2;
begin
hfunc = 1 - pow((0.5+0.5*cos(3.14*term1/term2)),4);
end
endfunction

analog function real ifunc;
input term1, term2;
real term1, term2;
begin
ifunc = 1 - pow((0.5-0.5*cos(3.14*term1/term2)),4);
end
endfunction

analog function real psi;
input Vgb, Vdb, vfb, phib, gamma;
real Vgb, Vdb, vfb, phib, gamma;
real z, a, A, Vt, td, tds, fd, fds;
real xo, x1, x2, expfunc, z2, z2d, z2dd, Fz, Gx1;
begin
```

```
z = (Vgb-vfb)/phiT;
a = gamma/sqrt(phiT);
A = (phib + Vdb)/phiT;
Vt = A + a*sqrt(A);
td = sqrt(A)/(sqrt(A)+a);
tds = -a*(A-2)/(2*pow((sqrt(A)+a),3));
fd = sqrt(2)/(sqrt(2)+a);
fds = 2*a/(3*pow((sqrt(2)+a),3));

if (z > Vt | z == Vt) begin
    xo = ln(1+td*(z-Vt)+0.5*(td*td+tds)*(z-Vt)*(z-Vt))+A;
    x1 = ln(xo*xo/(a*a) - (1+2*z/(a*a))*xo + z*z/(a*a) + 1) + A;
    x2 = x1 - (x1-xo)*exp(-0.1*(z-Vt));
    expfunc = exp(x2-A);
    z2 = x2 + a*sqrt(expfunc+x2-1);
    z2d = 1 + a*(expfunc+1)/(2*sqrt(expfunc+x2-1));
    z2dd = (2*a*expfunc*sqrt(expfunc+x2-1) -
     a*(expfunc+1)*(expfunc+1)/(sqrt(expfunc+x2-1)))/(4*(expfunc+x2-1));
    psi = phiT*(x2 + ((z-z2)/z2d)*(1-(z-z2)*z2dd/(2*z2d*z2d)));
end else  if (z < Vt & z > 0) begin
        Fz = 1 - hfunc(z,Vt)*exp(td*(z-Vt)+0.5*tds*(z-Vt)*(z-Vt))
         - ifunc(z,Vt)*exp(-fd*z - 0.5*fds*z*z);
        x1 = z + a*a/2 - 0.5*a*sqrt(4*z+a*a - 4*Fz);
        Gx1 = 1 - hfunc(x1,A)*exp(x1-A) - ifunc(x1,A)*exp(-x1);
        psi = phiT*(z + a*a/2 - 0.5*a*sqrt(4*z + a*a - 4*Gx1));
    end  else if (z < 0 | z == 0) begin
            xo = -ln(1-fd*z+0.5*(fd*fd+fds)*z*z);
            x1 = -ln(xo*xo/(a*a) - (1+2*z/(a*a))*xo + z*z/(a*a) + 1);
            x2 = x1 - (x1-xo)*exp(0.1*z);
            expfunc = exp(-x2);
            z2 = x2 - a*sqrt(expfunc+x2-1);
            z2d = 1 - a*(-expfunc+1)/(2*sqrt(expfunc+x2-1));
            z2dd = -(2*a*expfunc*sqrt(expfunc+x2-1) - a*(-expfunc+1)*(
            -expfunc+1)/(sqrt(expfunc+x2-1)))/(4*(expfunc+x2-1));
            psi = phiT*(x2 + ((z-z2)/z2d)*(1-(z-z2)*z2dd/(2*z2d*z2d)));
        end
 end
endfunction


analog function real delpsieps;
input psival, eps1;
real psival, eps1;
begin
delpsieps = exp((psival - phib_id - eps1)/phiT);
end
endfunction
```

```
//---------------- Beginning of actual model calculations--------------------

analog begin
          Vlimit      =       4.0 * phiT;
            phio        =       0.5 * (phib_id + phibd_id);
            Acc1        =       1.0 / (1.0 + ko_id  / sqrt(2.0 * phiT));
            AccD        =       1.0 / (1.0 + kod_id / sqrt(2.0 * phiT));
            ko_2        =       0.5 * ko_id;
            ko2_4       =       ko_2 * ko_2;
            kod_2       =       0.5 * kod_id;
            kod2_4      =       kod_2 * kod_2;
            i16phph     =       1.0 / (16.0 * phiT * phiT);
            phib_i      =       phib_id ;
            phibd_i     =       phibd_id ;
            ko_i        =       ko_id ;
            kod_i       =       kod_id ;
            bet_i       =       bet_id;
            betacc_i    =       betacc_id;
            rd_i        =       rd_id/kdr ;
            rdrift      =       rdrift1;

           //-------------- Branch voltages assigned to variables-----------

            Vds         =       V(d,s);
            Vgb     =     V(g,b);
        Vgs         =       V(g,s);
            Vsb         =       V(s,b);
        Vdis        =       V(di,s);
        Vddi        =       V(d1,di);
            Vdd1        =       V(d,d1);
        Vd1s     =     V(d1,s);
        Vgb_t0      =       Vgs + Vsb - vfb_i;
            Vsb_t       =       hyp(Vsb + 0.9*phib_i, `EPS2) + 0.1*phib_i;

     if (Vds < 0.0) begin
`hypm(Vds1, Vds, Vsb_t, mexp_i)
        end else begin
            Vds1        =       Vds;
        end

            Vgs_t       =       Vgs - vfbd_i;
            Vgd_t       =       Vgs_t - Vds1;

           //---------- Channel region quantities----------------------------

            Vinv0_v     =       hyp(Vgb_t0 - Vsb_t - ko_i * sqrt(Vsb_t), `EPS2);
            delta_v     =       ko_2 / sqrt(1.0 + Vsb_t);
            ksi_v       =       1.0 + delta_v;
            Vdis_sat0_v =       Vinv0_v / ksi_v;
            Vdis_sat_v  =       2.0 * Vdis_sat0_v / (1.0 + sqrt(1.0 + 2.0 * the3_1 *
             Vdis_sat0_v));
```

```
            Vsb_t0      =       hyp(0.9*phib_i, 'EPS2) + 0.1*phib_i;
         Vdep0_v     =       ko_i * sqrt(Vsb_t);
            Vdep00_v    =       ko_i * sqrt(Vsb_t0);
            Fmob_v      =       1.0 + the1_i * Vinv0_v + the2_i * (
            Vdep0_v - Vdep00_v) / ko_i;


            r           =       sqrt(phio + hyp(Vsb, 'EPS1));
            ro          =       sqrt(phio);
            f_lin       =       hyp(1.0 - lamd_i * (r - ro) / ro, 'EPS2);
            Voxp        =       f_lin / (rd_i * betacc_i);
            Fmobacc     =       1.0 + 0.5 * the1acc_i * (hyp(Vgs_t, 'EPS2) +
             hyp(Vgd_t, 'EPS2));
            bet_Fmob    =       bet_i / Fmob_v;
            bet_Facc    =       betacc_i / Fmobacc;
            Gminko2     =       'GMIN * ko_i  * ko_i;
            Gminkod2    =       'GMIN1 * kod_i * kod_i;


 //------------ Channel Current calculation: Ich---------------------


if (Vdis < 0.0) begin
       denom1      =       1.0 / (1.0 -the3_1* Vdis);
       Ich         =       bet_Fmob * (Vinv0_v - 0.5*ksi_v*Vdis)* Vdis * denom1+
        Gminko2 *Vdis;
   end else begin
       'hypm(Vdis_eff,Vdis, Vdis_sat_v, mexp_i)
    denom1      =       1.0 / (1.0 + the3_1*Vdis_eff);
            Ich         =      (1+lamd_i*Vdis)*kch*bet_Fmob * (Vinv0_v -
            0.5*ksi_v*Vdis_eff)*Vdis_eff*denom1+ 10*Gminko2*Vdis;
end

//---Drift Current calculation under the thin oxide region: Idr-----

         Vgdi_t      =       Vgs_t - Vdis;

    if (Vgdi_t > 0.0) begin
    Vgdi_t_eff  =       Vgdi_t;
    end else begin
      Vdib_t      =       hyp(Vsb + Vdis + 0.9*phibd_i, 'EPS2) + 0.1*phibd_i;
                hypmarg     =       Vdib_t + kod_i * sqrt(Vdib_t);
                'hypm(Vgdi_t_eff, Vgdi_t, hypmarg, 8)
            end
        if (Vgdi_t_eff >= 0.0) begin
             Vq_dr_eff   =       hyp(Voxp + Vgdi_t_eff, 'EPS2);
            end
            tmp         =       sqrt(1.0 + 2.0*the3d*Vq_dr_eff);
            denom       =       1.0 / (1.0 + tmp);
        Vddi_sat    =       2.0 * Vq_dr_eff * denom;
    'hypm(Vddi_eff,Vddi,Vddi_sat, mexpd_i)
```

```
            the3d_i     =       the3d;


        if (Vddi < 0.0) begin
    denom       =       1.0 / (1.0 + the3d * Vddi);
    Idr         =       bet_Facc * (Vq_dr_eff - 0.5 *Vddi)*
     Vddi * denom+ Gminkod2  * Vddi ;
end else begin
    denom       =       1.0 / (1.0 + the3d * Vddi_eff);
    Idr         =       kdr*bet_Facc * (Vq_dr_eff -
    0.5 *Vddi_eff)* Vddi_eff * denom + 8e-1*Gminkod2*Vddi;
  end

 //---Drift Current Formulation under the thick oxide region:Idrift---

            Ec          =       (1.0E5)/(kdrift*udr);
            if(Vdd1 < 0.0) begin
            Idrift=    (q*w*tsi*ndr*udr*Vdd1/llocos);
            end else begin
            Idrift      =        (1+thetax3*Vdd1)*(kdrift*q*w*tsi*ndr*udr*Vdd1/llocos)
            /pow((1+thetax1*pow((Vdd1/(llocos*Ec)),thetax)),1/thetax);
            //+ thetax1*pow(Vdd1,2)/pow((llocos*Ec),2));
            end


    //-------- Gate, Drain and bulk charge formulation-----------------

Ecritch = 2.0*1e20;
Ecritdr = 0.5*1e20;
Fact1 = lc/(lc+ld);
Fact2 = 0*(llocos+ld)/(lc+ld+llocos);

//--------- Channel Region Forumulation------------------------------

psis = psi(Vgb,Vsb,vfb_i,phib_id,ko_id);
    psid = psi(Vgb,Vdis+Vsb,vfb_i,phib_id,ko_id);
      psim = (psis+psid)/2;
      psidiff = psid - psis;

vinvo = Vgb - vfb_i - psis - (psis/abs(psis))*ko_id*sqrt(abs(psis));
vinvL = Vgb - vfb_i - psid - (psid/abs(psid))*ko_id*sqrt(abs(psid));
zeta = (1 + ko_id/(2*sqrt(abs(psis))));
vgtdel = vinvo - vinvL;
vgtavg = (vinvo + vinvL)/2;
  Fch  = vgtdel/(vgtavg+zeta*phiT);

//---------- Drift Region Formulation---------------------------------

psisdr = psi(-Vgb+Vdis,Vdis,vfbd_i,phibd_id,kod_id);
  psiddr = psi(-Vgb+Vddi+Vdis,Vddi+Vdis,vfbd_i,phibd_id,kod_id);
psidiffdr = psiddr - psisdr;
```

```
Vq_dr_dig = (Vgb - vfbd_i - Vdis - (-psisdr));
Vq_dr_di = (Vgb - vfbd_i - Vdis - (-psisdr));
Vq_dr_d1 = (Vgb - vfbd_i - Vdis - Vddi - (-psiddr));
Vq_dr_delg = Vq_dr_dig - Vq_dr_d1;
Vq_dr_del = Vq_dr_di - Vq_dr_d1;
Vq_dr_avgg = (Vq_dr_dig + Vq_dr_d1)/2;
Vq_dr_avg = (Vq_dr_di + Vq_dr_d1)/2;
Fdrg = Vq_dr_delg/(Vq_dr_avgg + 35.56);
Fdr = Vq_dr_del/(Vq_dr_avg + 35.56);

//--------- Multiplication factors due to E-dependent mobility------

efactch = 1/(Ecritch*lc);
efactdr = 1/(Ecritdr*ld);
// efactch = the3_1;
// efactdr = the3d;
// fact1ch = (1 + 2*efactch*psidiff - 2*efactch*vinvo/(zeta));
// fact2ch = 1;
// fact3ch = (1 + 2*efactch*vinvo/(zeta));
// fact1dr = (1 + 2*efactdr*Vddi_eff - 2*efactdr*Vq_dr_di);
// fact2dr = 1;
// fact3dr = (1 + 2*efactdr*Vq_dr_di);

fact1ch = 1/(1 + efactch*psidiff);
fact2ch = (1 + 2*efactch*psidiff - 2*vinvo*efactch/zeta)*fact1ch;
fact2ch = (1 + 2*vinvo*efactch/zeta)*fact1ch;
fact1dr = 1/(1 + efactdr*Vddi);
fact2dr = (1 + 2*efactdr*Vddi - 2*Vq_dr_di*efactdr)*fact1dr;
fact3dr = (1 + 2*Vq_dr_di*efactdr)*fact1dr;



//--------- Gate, Drain, Source, Bulk charge terms------------------

Qgch = 1e4*Cox*w*lc*(Vgb - vfb_i - 0.5*(psis+psid) +
 Fch*vgtdel/(12*zeta)*fact2ch)/(1+lamd_i*Vdis);
Qgdr = 1e4*Cox*w*ld*(Vq_dr_avgg + Fdrg*(Vq_dr_delg/12)
            *fact2dr);
            Qpn = 1e4*w*tsi*sqrt(2*esi*0.75*q*nd*10/11)*pow((1 + (Vdis)/0.75),0.5);
      Qdchmos =-1e4*Cox*w*lc*0.5*(vgtavg - (vgtdel/6)*(1 - (Fch/2)*fact2ch -
 (Fch*Fch/20)*fact1ch))/(1+lamd_i*Vdis);
Qschmos =-1e4*Cox*w*lc*0.5*(vgtavg + (vgtdel/6)*(1 + (Fch/2)*fact3ch -
 (Fch*Fch/20)*fact1ch))/(1+lamd_i*Vdis);
Qddrmos =-1e4*Cox*w*ld*0.5*(Vq_dr_avg - (Vq_dr_del/6)*(1 - (Fdr/2)*fact2dr -
 (Fdr*Fdr/20)*fact1dr));
Qsdrmos =-1e4*Cox*w*ld*0.5*(Vq_dr_avg + (Vq_dr_del/6)*(1 + (Fdr/2)*fact3dr -
 (Fdr*Fdr/20)*fact1dr));

Qg = Qgdr + Qgch;
Qd = Fact1*Qdchmos + (1-Fact2)*Qddrmos + Fact1*Qsdrmos;
Qs = Qschmos + (1-Fact1)*Qdchmos + Fact2*Qddrmos + (1-Fact1)*Qsdrmos;
Qb = -(Qschmos+Qdchmos+Qsdrmos+Qddrmos+Qg);
```

```
Igtran = ddt(Qg);
Iditran = ddt(Qdchmos)+ddt(Qsdrmos);
Id1tran = ddt(Qddrmos);
Istran = ddt(Qschmos);
tau = 1e-10;
Delaycharge = Idr*lc*tau/(lc+ld);


    //--------- load the currents into the EC --------------

             I(di,s) <+  Ich;    //Our Model
             I(d1,di)<+  Idr;
             I(d,d1) <+  Idrift;
             I(g,b) <+  Igtran;
             I(di,b) <+  Iditran;
             I(d1,b) <+  Id1tran;
             I(s,b) <+  Istran;

//          I(di,s) <+  Ich;   //MM20 Model
//          I(d1,di)<+  Idr;
//          I(d,d1) <+  Idrift;
//          I(g,b) <+  ddt(Qg);
//          I(d1,b) <+  ddt(Qd) - ddt(Delaycharge);
//          I(s,b) <+  ddt(Qs) + ddt(Delaycharge);

//           I(di,s) <+  Ich;  //DC Model
//           I(d1,di)<+  Idr;
//           I(d,d1) <+  Idrift;


end
endmodule
```

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