Analog Front End Design and Layout of Bluetooth Transmitter

A project report

submitted by

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in partial fulfillment of the requirements

for the award of the degree of

Master of Technology

Under the guidance of

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Thesis Certificate

This is to certify that the thesis titled **Analog Front End Design and Layout of Bluetooth Transmitter**, submitted by **T L Vivek**, to the Indian Institute of Technology, Madras, for the award of the degree of **Master of Technology**, is a bonafide record of the research work done by him under our supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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I thank my beloved friends at IIT Madras for a great experience. I would like to thank my parents for supporting and encouraging me throughout my stay at IIT Madras and I dedicate this project to my family and friends.

Abstract

A direct conversion transmitter complying with the IEEE 802.15.1 (Bluetooth) standard is designed. The radio frequency (RF) analog front-end blocks of the transmitter are power amplifier (PA), quadrature upconversion mixer and baseband filter. The main idea of this work is to reduce the power consumption and the area of chip. By choosing the passive mixer as upconverter the power is majorly dissipated in power amplifier only. For the op-amps used in the design only single CMFB loop is used so as to reduce the number of capacitors required for compensation, in turn reducing the area of the chip. The transmitter is designed and verified through simulations, in UMC 65 nm CMOS process, and found to satisfy the system requirements with sufficient margin.

ABBREVIATIONS

ACPR	Adjacent Channel Power Ratio
AM	Amplitude Modulation
APC	AM/PM conversion
BPF	Band Pass Filter
BR	Basic Rate
CMFB	Common Mode FeedBack
DAC	Digital to Analog Converter
dB	decibel
DC	Direct Current
DPSK	Differential Phase-Shift Keying
DQPSK	Differential Quadrature Phase-Shift Keying
EDR	Enhanced Data Rate
EMR	Electro-Migration Rules
FDD	Frequency Division Duplexing
IEEE	Institute of Electrical and Electronics Engineers
IF	Intermediate Frequency

ISM	Industrial, Scientific and Medical
LO	Local Oscillator
LTI	Linear Time-Invariant
MFB	Multiple FeedBack
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
P1dB	Power at 1 dB compression
PA	Power Amplifier
PAE	Power Added Efficiency
PAPR	Peak-to-Average Power Ratio
PAR	Peak-to-Average Ratio
PM	Phase Modulation
RF	Radio Frequency
TDD	Time-Division Duplexing
UGB	Unity Gain Bandwidth
UMC	United Microelectronics Corporation
VCO	Voltage-Controlled Oscillator

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Chapter 1

Introduction

The Bluetooth is a short-range wireless connection between different electronic devices. The distance among the communicating devices is small in comparison to other modes of wireless communication. Bluetooth operates in the 2.4-2.48 GHz band which is the globally unlicensed but regulated Industrial, Scientific and Medical (ISM) band. The radio technology used in Bluetooth is frequency-hopping spread spectrum. The transmitted data are divided into packets and each packet is transmitted on any one of the designated Bluetooth channels. The transceiver architecture is based on time-division duplexing (TDD) scheme, which in turn effects some design specifications of transmitter. In TDD systems, transmitter and receiver do not operate at same time.

1.1 Modulation schemes of Bluetooth

Initially Gaussian Frequency Shift Keying (GFSK) modulation was the only modulation scheme available. GFSK is a constant envelope modulation where information is sent only in phase. Devices functioning with GFSK are said to be operating in basic rate (BR) mode with an instantaneous data rate of 1 Mbit/s. Since the

Class	Max. permitted power	Typ. range(m)
1	100 mW (20 dBm)	~ 100
2	**2.5 mW (4 dBm)**	$\sim$ **10**
3	1 mW (0 dBm)	~ 1

Table 1.1: Different classes of Bluetooth

introduction of Bluetooth 2.0, $\pi/4$-DQPSK and 8DPSK with a data rate of 2 and 3 Mbits/s respectively are also used. These two are variable envelope modulations where information is sent in both amplitude and phase. These Bluetooth devices use spectrum efficiently by transmitting more data in the available frequency band. So these Bluetooth versions are said to be operating in Enhanced Data Rate (EDR). The combination of BR and EDR modes in Bluetooth radio technology is classified as a BR/EDR radio. With channel bandwidth of 1 MHz, Bluetooth has 79 designated channels in the 2.4-2.48 GHz band. The latest Bluetooth v4.0 allows for 40 channels with 2 MHz channel spacing. In the present design, transmitter is implemented for Bluetooth 4.0.

1.2 Types of Bluetooth devices

There are three different types of Bluetooth devices available based on the distance between the two communicating ends. The classification is shown in Table 1.1. In this work, transmitter is designed for class 2 Bluetooth. The maximum and minimum permitted powers of class 2 Bluetooth are 4 dBm and -6 dBm respectively.

1.3 Design Objective

The main objective of this work is to design an analog front end transmitter for Bluetooth with low power and minimum area.

1.4 Thesis organization

The rest of the thesis is organized as described below.

Chapter 2 discusses the architectural considerations of RF transmitter

Chapter 3 discusses the design of Power Amplifier and the principle behind the choice of power amplifier in detail

Chapter 4 deals with the design of the voltage mode passive mixer with 25% duty cycle LO signal and LO generator circuit

Chapter 5 deals with the base-band filter and op-amps used for implementation of filter

Chapter 6 summarizes the integration of different blocks in the transmitter and final results of entire chain

Chapter 2

Transmitter Architecture

2.1 Types of transmitter architectures

An RF transmitter performs upconversion and power amplification. A good understanding of modulation schemes is necessary for transmitter design because of their influence on the choice of architecture and building blocks such as upconversion mixers and power amplifiers (PAs) [1]. There are two types of modulation formats available:

a) Constant Envelope (Non-Linear)

b) Variable Envelope (Linear)

Any modulation signal x(t) can be represented in two ways. They are

Polar form

$$x(t) = A\cos\left(\omega_{LO}t + \phi(t)\right) \tag{2.1}$$

Cartesian form

$$x(t) = x_I(t)\cos\omega_{LO}t + x_Q(t)\sin\omega_{LO}t \tag{2.2}$$

A third representation called complex envelope representation is also there, but the above two are sufficient in the present context.

Constant envelope modulation schemes have constant amplitude with respect to time. Information will be carried in only the zero-crossing points. Phase and frequency modulations are constant envelope modulations. A phase locked loop can be used as upconverter in this case and the RF signal can be processed by a nonlinear power amplifier. This type of transmitter architecture is called as polar architecture. The very first Bluetooth versions have GFSK as the only modulation scheme. As mentioned earlier, these Bluetooth devices are said to be operating in basic rate. So there were some published implementations reporting polar architecture for basic rate Bluetooth transmitter.

Variable envelope modulation schemes have information in amplitude also due to which the amplitude varies with time. Modulation schemes such as QPSK have information in both amplitude and phase. This is done in order to utilize the spectrum efficiently. In such cases, polar architecture will not be sufficient as it is not possible to track the amplitude variations with polar architecture. Cartesian architecture on the other hand can track both amplitude and phase variations. In Cartesian architecture, two signals (in phase and quadrature phase) coming from DAC are given to two separate mixers with LO signals in quadrature phase. Here mixer will be used as upconverter. The two upconverted RF signals from mixers are added to get the required modulated signal. In general DAC is implemented in fully differential structure, so four output lines will be sent into analog front end. Cartesian architecture can handle both constant envelope and variable envelope modulation signals. But for constant envelope modulation schemes, polar architecture is generally preferred.

2.2 Homodyne and Heterodyne architectures

Based on the number of steps for upconversion, two types of transmitter architecture are possible. They are homodyne and heterodyne architectures. Homodyne architecture is also called as direct conversion architecture. In homodyne architecture, upconversion will be happening in a single step. It is simple and high levels of integration will be achieved with this architecture. But there is a serious problem with this homodyne architecture. The power amplifier and LO generator will be operating at the same frequency. The modulated spectrum output of PA will corrupt the pure sinusoid that is coming from LO generator (VCO) and it will give very noisy LO. This effect is called as PA pulling. It will happen either through electromagnetic coupling if they are close enough or through supply if they share same supply or through substrate if they are on same chip. It is like a parasitic feedback. The phenomenon of pulling the VCO is called injection locking. If PA output is just a single tone, then it's not a serious problem. But as PA output will never be a single tone, the VCO will produce side bands also.

This problem can be eliminated by performing upconversion in two steps. The mixers in the two steps will be operating with different LO frequency than that of power amplifier. So PA pulling problem will not arise here. This type of architecture is called as heterodyne architecture. The second mixer in this architecture will produce two sidebands here. One sideband has to be eliminated as the information in it is redundant. But to eliminate this frequency, the band-pass filter needed should have high quality factor, where it is very difficult to implement a BPF with high Q value at GHz of frequency. So this type of architecture will not result in high levels of integration like in the case of homodyne architecture.

2.3 Direct conversion architecture

The major problem of the direct conversion architecture is PA pulling. The LO generator which is operating at the same frequency as that of PA is the main reason for this problem. If it is managed to design VCO at a different frequency than that of PA, then this problem will not arise at all. This can be done by designing VCO at double the operating frequency as that of PA, followed by a frequency divide by two circuit. Nowadays frequency divide by two circuits that are giving in phase and quadrature phase are widely used in the transceiver architectures. As the PA pulling problem is solved by this technique, direct conversion architecture is widely used in RF transmitters. So this architecture is implemented here. The block diagram of transmitter chain is shown in Fig. 2.1.

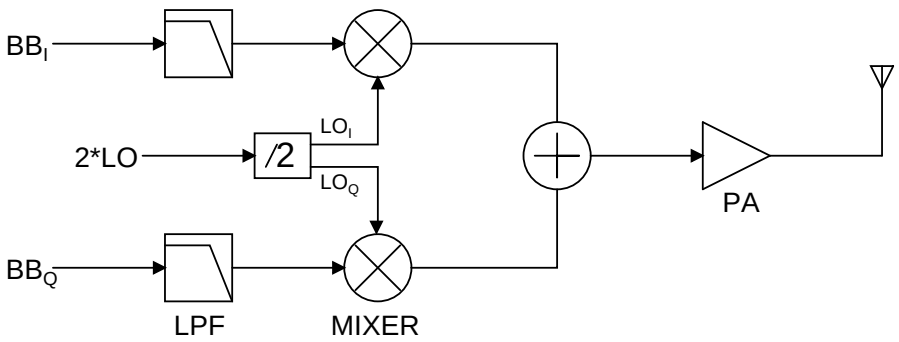

Figure 2.1: Direct-Conversion Architecture

As the antenna at the output of the transmitter as shown in Fig. 2.1 is single-ended, differential signal should be converted to single-ended. For this the PA itself could be single-ended or the PA can be fully differential but then a balun is required in between the PA and antenna to convert the differential signal into

single-ended.

2.3.1 Single-Ended PA

From the output of the mixer as shown in Fig. 2.1 there are two output lines because, upto mixer, in the transmitter chain, all the blocks are fully differential. There are two ways in which a transmitter can be implemented with single-ended PA. One way is to give only one of the output lines of mixer as input to the PA as shown in Fig. 2.2.

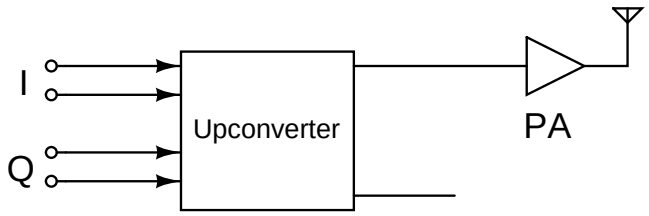

Figure 2.2: Upconverter/PA Interface Without Balun

The drawback of this architecture is that half of the transmitter voltage gain is lost because the PA here senses only one output of the upconverter.

The second way alleviates the above issue by interposing a balun between the upconverter and the PA as shown in Fig. 2.3.

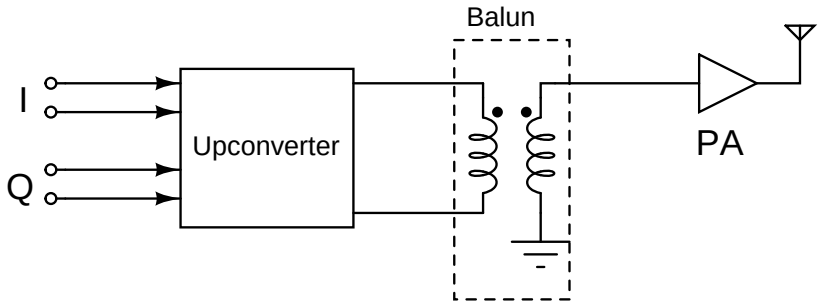

Figure 2.3: Upconverter/PA Interface With Balun

But in this architecture, the balun introduces its own loss as it has to be integrated on the chip, so the improvement in voltage gain is a few decibels, rather than 6 dB.

Another drawback of the single-ended PA is that, the PA circuit pulls large transients from supply to ground. As the PA is now single-ended, it will be sensitive to the package parasitics.

2.3.2 Differential PA

The differential implementation of PA as shown in Fig. 2.4 will resolve the two issues of the single-ended PA. Also, such a topology draws much smaller transient currents from supply lines. With differential PA, the entire transmitter is fully differential, making the design insensitive to package model parasitics.

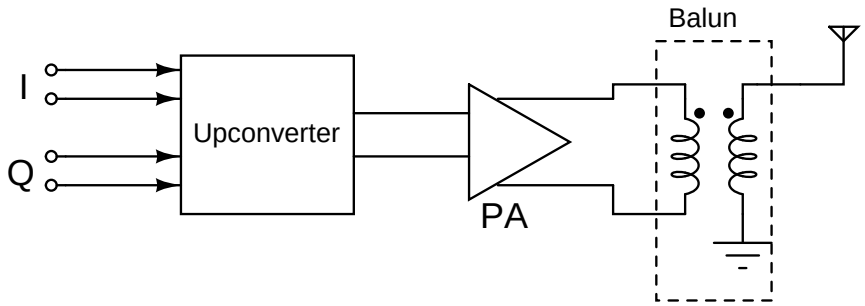

Figure 2.4: Differential PA with Balun at Output

Comparing the two architectures shown in Fig. 2.3 and Fig. 2.4, for the same loss of balun used in both the architectures, the balun used in the latter case experiences the entire power delivered by the PA to the load thus dissipating more power than when balun is at output of mixer. So in this case the transmitter efficiency degrades more significantly for the same loss in balun [1].

In this work both the architectures shown in Fig. 2.3 and Fig. 2.4 are implemented.

Chapter 3

Power Amplifier

3.1 Choice of power amplifier

Broadly, power amplifiers can be categorized into two major types. They are linear and nonlinear (switching) power amplifiers. Linear power amplifiers are used for handling variable envelope modulation formats having a trade-off with efficiency. Nonlinear power amplifiers are used for handling constant envelope modulation formats with high efficiency. Efficiency (Drain Efficiency) is one of the important metrics of power amplifier. It is the ratio of PA output power to its DC power dissipation. Nonlinear power amplifiers cannot be used for variable envelope modulation schemes as their output is saturated. To track the incoming amplitude variations, the power amplifier output amplitude should vary in accordance with the input. So the use of linear power amplifier is inevitable in the case of variable envelope modulation schemes even though it results in poor efficiency. Here, linear power amplifier is used because $\pi/4$-DQPSK and 8DPSK are variable envelope modulation schemes. In any RF power amplifier, inductor is used as load to facilitate the output to swing above the supply. This will help in getting more output power for the given power supply.

In linear power amplifiers, there are sub categories based on the conduction angle. They are class A, B, AB and C power amplifiers. The class A conducts for full cycle (360°), class B conducts for half cycle (180°), class AB conducts for more than half cycle, class C conducts for less than half cycle. Obviously class A power amplifier is superior in terms of linearity. As linearity is an important concern in the case of variable envelope modulation, class A topology is implemented here.

3.2 Class A power amplifier

As per the definition of class-A power amplifiers, some minimum amount of DC current should be there in the MOSFETs so as to ensure 360° conduction angle. The PAR or PAPR which is an important factor of modulation schemes in the context of power amplifier is defined as follows:

$$PAPR = \frac{|\ x\ |_{peak}{}^2}{x_{rms}{}^2} \tag{3.1}$$

If PAPR is high, then the DC current will be high, and for a given output power, the efficiency of the PA decreases. Among all the three modulation schemes used for Bluetooth, 8DPSK has high PAPR of 6.3 dB. So this value of the PAPR decides the DC current in the power amplifier.

The design here is implemented in UMC 65 nm CMOS process in which the MOS transistors used are 1.2 V transistors. To deliver an output power of 2.5 mW to a 50 Ω antenna, the RMS voltage required is 353.55 mV and from the equation 3.1 the peak voltage required is 730.22 mV. If only one transistor is used for PA, due to this large swing at the drain of the MOSFET, the transistor will breakdown. So cascode configuration has to be used. In cascode structure, swings of output will be shared by the two transistors so that none of them will breakdown. Both common source and common gate transistors used are thin oxide transistors only.

3.2.1 Important Metrics for the class-A PA

The two important metrics which characterize the PA are efficiency and linearity. The efficiency and the linearity of the PA have a trade-off. An efficient PA consumes very less DC power for a given output power requirement as drain efficiency is inversely proportional to DC power for a given PA output power.

For a linear power amplifier, the output power should vary linearly in accordance with the input power. Gain should be same for all levels of input powers. But the output voltage levels will be limited by power supply and inherent nonlinearity of the device. Because of these reasons, gain compression will happen at higher output power levels.

3.2.1.1 Efficiency

Drain Efficiency : Drain Efficiency (η) can be calculated as follows,

$$\eta = \frac{Output\ Signal\ Power(P_{sig})}{DC\ Power(P_{DC})} \tag{3.2}$$

The theoretical maximum efficiency of a class-A PA is 50%. If the drain swing is less than the maximum (V_{DD}) and if there are additional losses anywhere else, the efficiency drops. As the swing approaches zero, which means the signal power approaches zero, the drain efficiency also approaches zero while the transistor continues to burn DC power.

Power Added Efficiency (PAE) : The definition of drain efficiency involves only the RF output power and the DC input power, so it can assign a high efficiency to a PA that has no power gain. So another measure of efficiency is developed which takes the power gain also into account. This is called Power Added Efficiency (PAE) which replaces RF output power with difference between output and input power in the drain efficiency equation 3.2. It is calculated as follows:

$$PAE = \frac{P_{sig} - P_{in}}{P_{dc}} \tag{3.3}$$

$$= \eta\left(1 - \frac{1}{gain}\right) \tag{3.4}$$

where P_{in} is the input power. If the gain of power amplifier is not high, then PAE is not same as drain efficiency.

3.2.1.2 Linearity

Linearity is a very important concern in RF transmitters and it is mainly limited by power amplifier. To model the nonlinearity of PA, three different parameters are used here. They are output referred P1dB, AM/PM conversion and ACPR.

Output Referred P1dB Compression : The P1dB point refers to the gain compression by 1 dB. The P1dB point will set a limit to the region of power amplifier operation where the power levels above this point are prohibited to operate. The input power corresponding to the output referred P1dB is input referred P1dB. The output referred P1dB will be decided by both maximum output power of transmitter chain and PAPR of modulation scheme. For Bluetooth,

$$\begin{aligned} Required\ Output\ referred\ P1dB &= Maximum\ P_{out} + PAPR \\ &= 4\ dBm + 6.3\ dB \\ &= 10.3\ dBm \end{aligned}$$

So this is the specification on the entire transmitter chain that the output referred P1dB compression point should be greater than 10.3 dBm

AM/PM Conversion : AM/PM conversion is one more metric to quantify the nonlinearity of RF circuits. In power amplifiers, amplitude modulation may be converted to phase modulation, thus producing undesirable effects. Because of AM/PM conversion, output has amplitude-dependent phase shift. This does not occur in LTI system. It arises if a system is both dynamic and nonlinear. So AM/PM conversion has to be considerably less for good performance.

Adjacent Channel Power Ratio (ACPR) : ACPR is very important parameter to quantify the nonlinearity of PA. The transmitter should produce a band limited output with sidebands at considerably low level. ACPR is the ratio of in-band power to sideband power. ACPR requirement is specified for any transmitter through spectrum mask definition. As power amplifier is the most nonlinear block in the transmitter chain, the ACPR of PA alone also should be verified. The ACPR of Bluetooth transmitter from its spectrum emission mask, has to be more than 26 dBc. The ACPR of PA alone should be set to a value so that the entire transmitter chain meets the 26 dBc requirement. As the ACPR degrades with increasing main channel power, here class-2 Bluetooth is implemented, so as per the table 1.1 the specification on APCR has to be met for maximum output power which is 4 dBm.

3.3 Class A Differential Power Amplifier

Following the architecture explained in section 2.3.2, a fully differential class-A PA is implemented. The corresponding schematic is shown in Figure 3.1.

The antenna is single ended so balun is needed to perform the differential to single ended conversion. A scalable rectangular transformer with center tap from UMC 65 nm is used as balun here. The transformer converts the 50 Ω antenna impedance to 35 Ω at the output of each half of power amplifier. Capacitors are connected across the transformer to tune out the parasitics at the differential output

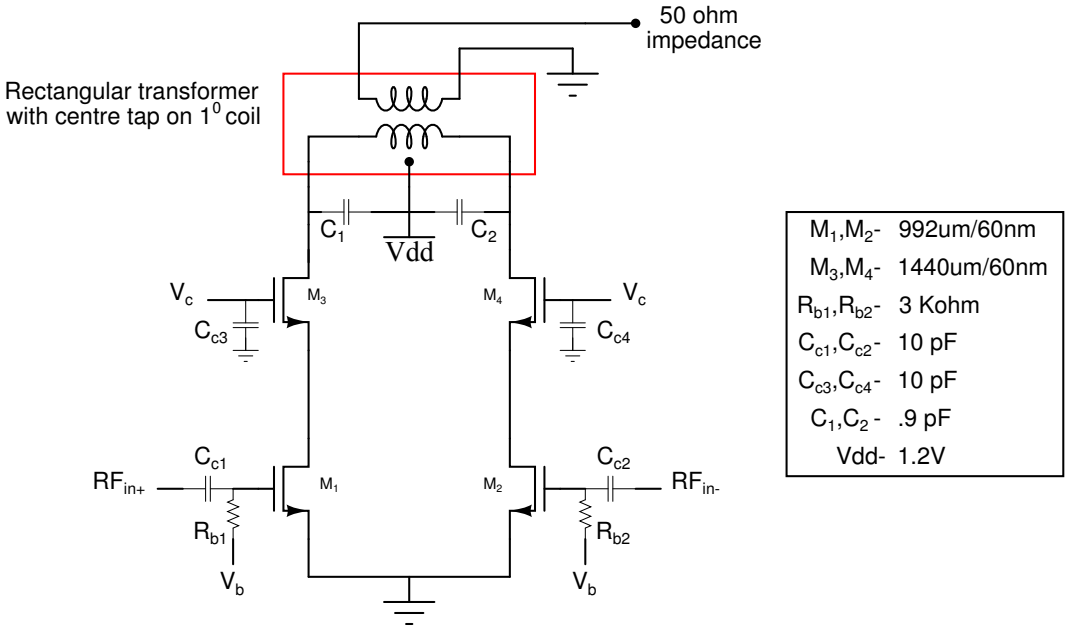

Figure 3.1: Differential PA - Schematic

nodes. The bias potentials V_b and the V_c shown in Figure 3.1 are chosen so that the specification on output compression point is met. The DC current is decided by the PAPR and the maximum output power to be delivered to the antenna. The DC current for this circuit is around 22 mA with 11 mA in each leg.

3.3.1 Layout and Post-layout Simulations of Differential PA

The layout of differential PA (in Figure 3.1) is shown in Figure 3.2.

In the Figure 3.2, the lines to the extreme top and bottom are the 'V_{DD}' lines for connecting to the capacitors C_1 and C_2 shown in Figure 3.1. The transformer is in between these two lines with the primary terminals towards right and the secondary terminals towards left. The center tap (CTP) connection of the transformer to 'V_{DD}' is also towards the secondary side. To the extreme right, the capacitors on

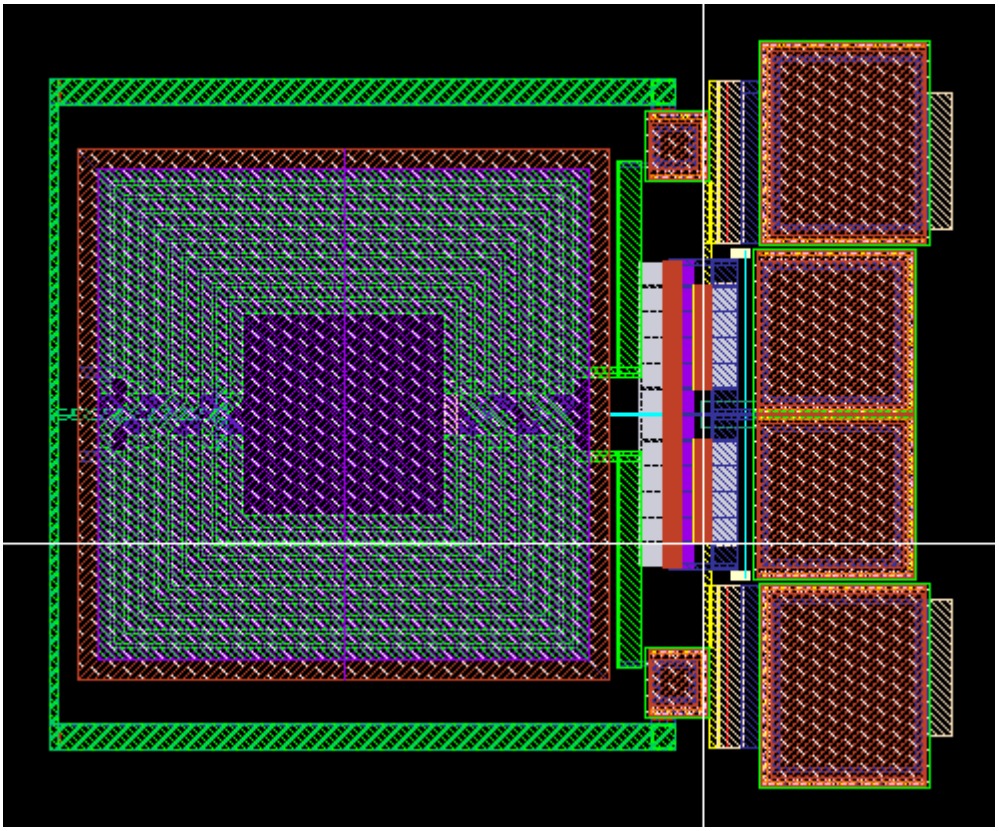

Figure 3.2: Differential PA - Layout

the top and bottom are the C_{c1} and C_{c2} of Figure 3.1, and the capacitors in between are those at the gates of the cascode transistors C_{c3} and C_{c4}. The supply lines are chosen wide enough as per the Electro-Migration Rules(EMR) for the total current of 22 mA between the supply lines. The area consumed by this layout is 445 μm x 370 μm. After extracting the parasitics of the layout shown in Figure 3.2 the simulation results are given below:

Output Power vs Input Power : The output power of the PA versus the input power of PA is plotted in Figure 3.3.

As in the Figure 3.3 the input power required for a maximum output power of

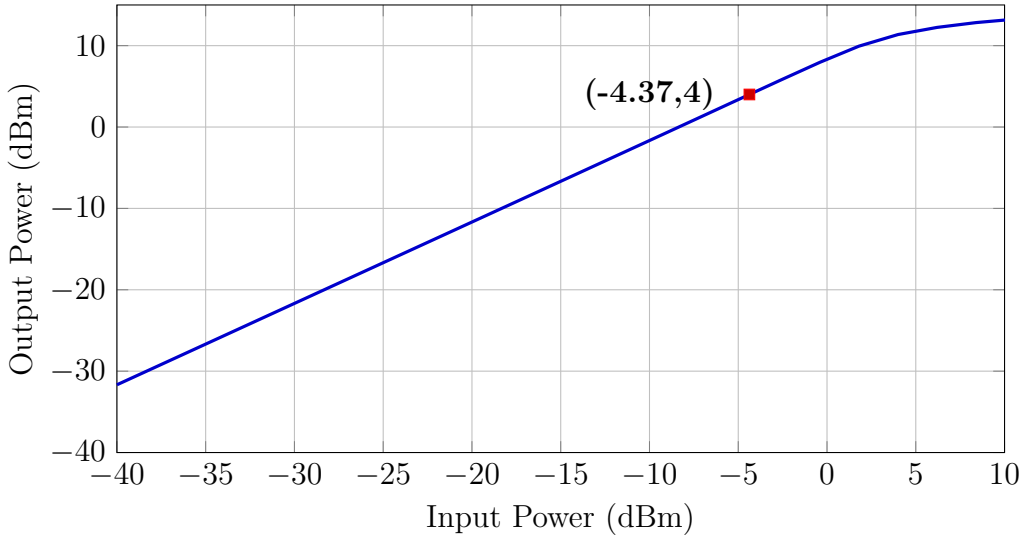

Figure 3.3: Differential PA - Output Power vs Input Power

4 dBm is -4.37 dBm. Thus the gain of the PA is 8.37 dB. Also in the same plot the gain compression can be observed.

Drain Efficiency : The Drain efficiency can be calculated as:

$$\begin{aligned} \eta &= \frac{Output\ Signal\ Power(P_{sig})}{DC\ Power(P_{dc})} \\ &= \frac{2.5\ mW}{1.2\ V \times 22\ mA} \\ &= 9.47\% \end{aligned}$$

Fig.3.4 shows the drain efficiency of power amplifier. As in the Figure 3.4 the maximum drain efficiency is 8%. This is lesser than the theoretical value as there will be loss across the balun and also the swing at the drain is not the maximum (V_{DD}).

Power Added Efficiency (PAE) : From the equation 3.4, gain in Figure 3.3 and drain efficiency in Figure 3.4 the PAE is 6.85%. This is shown in Figure 3.5.

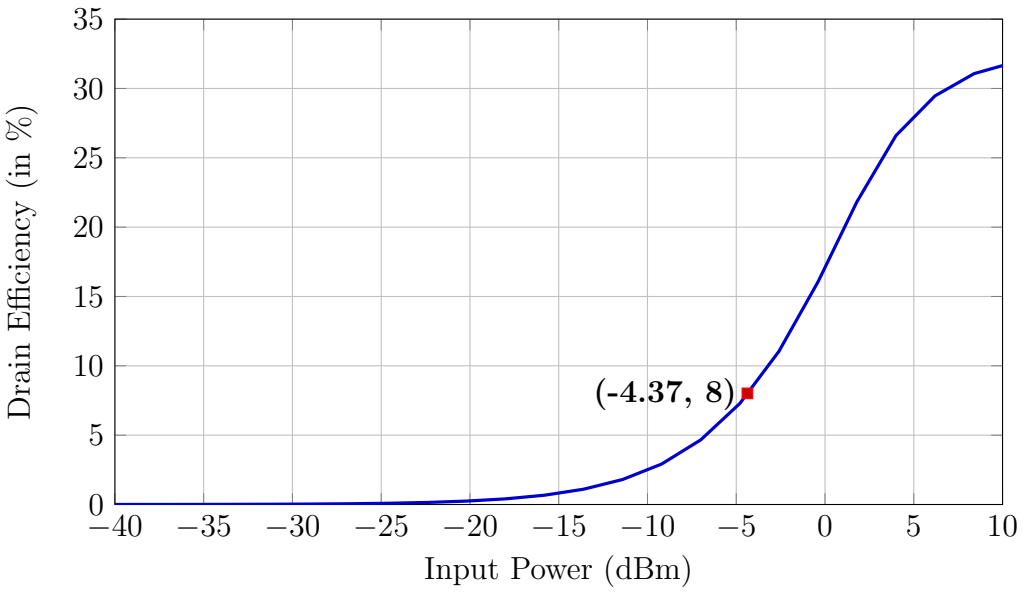

Figure 3.4: Differential PA - Drain Efficiency

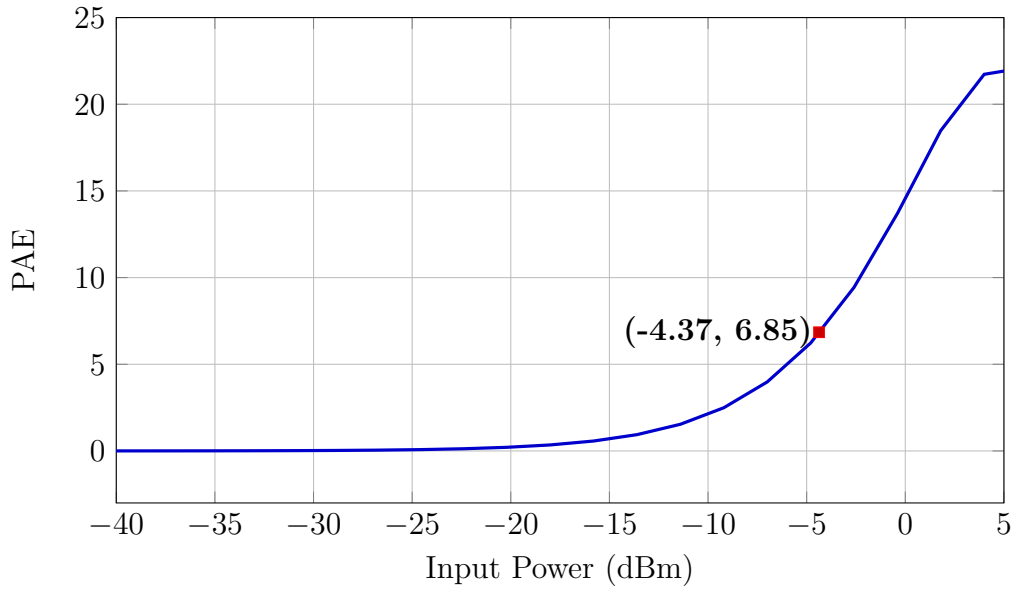

Figure 3.5: Differential PA - Power Added Efficiency

Output Referred P1dB Compression Point : To obtain the the output referred P1dB point, output power is plotted with respect to the input power and

the output power where the gain compresses by 1 dB is the output referred P1dB compression point. The Figure 3.6 shows the output compression curve of power amplifier alone. Thus the output referred P1dB compression point of PA alone is 11.4 dBm.

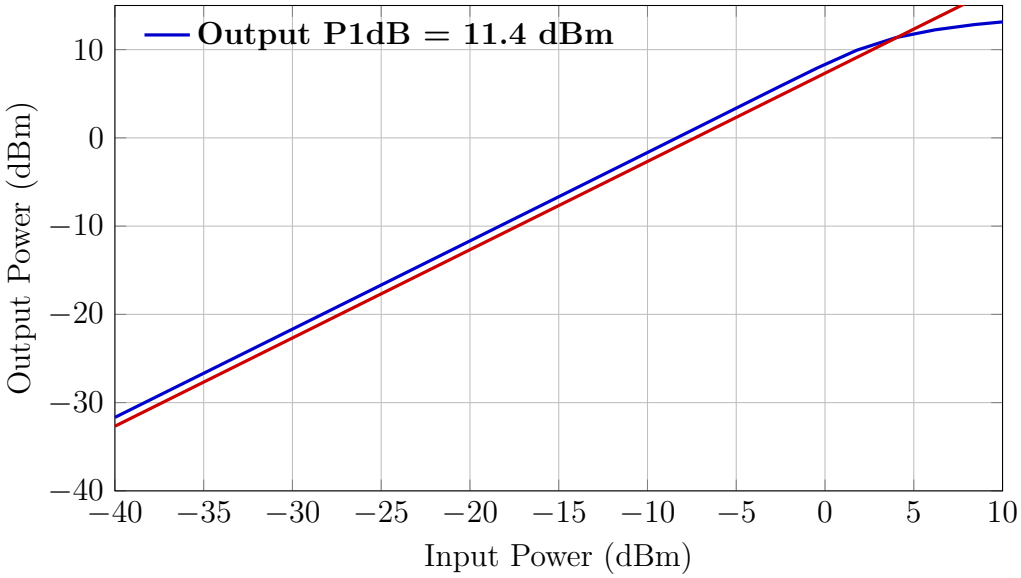

Figure 3.6: Differential PA - Output Compression Curve

AM/PM Conversion : The phase of the output voltage is plotted with respect to the input power. This is shown in the Figure 3.7.

From the Figure 3.7 the phase of the output voltage remains constant only for low input power levels. As the input power levels increase the output phase starts changing. The phase of the output voltage at low input power levels is -142.225°. The maximum phase change occurs for that input power at which maximum output power is obtained. Thus the phase at -4.37 dBm is -141.844°. So the maximum change in output phase is 0.38°.

Adjacent Channel Power Ratio (ACPR) : For the main channel power

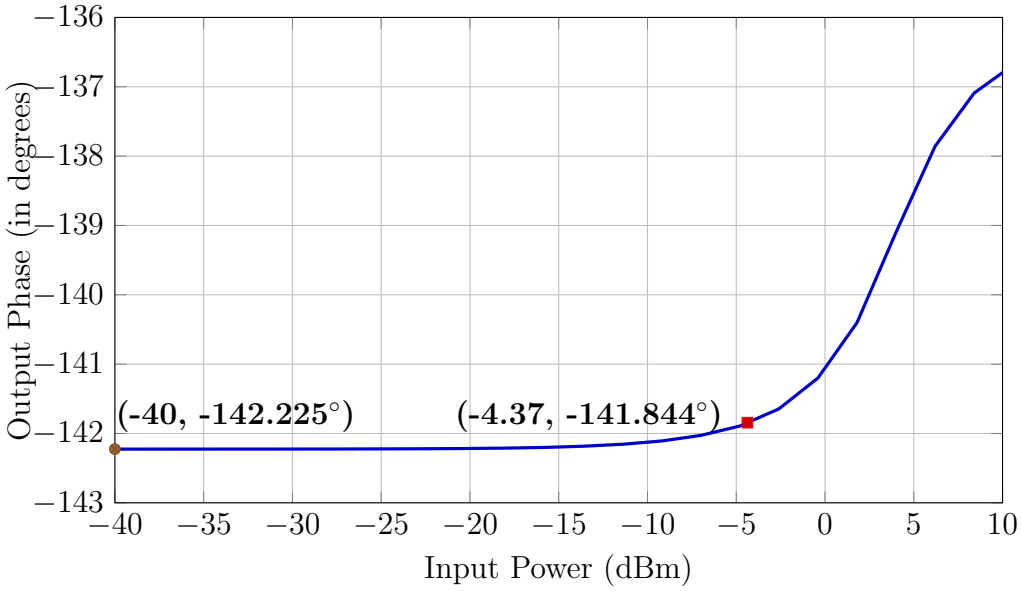

Figure 3.7: Differential PA - AM/PM Conversion

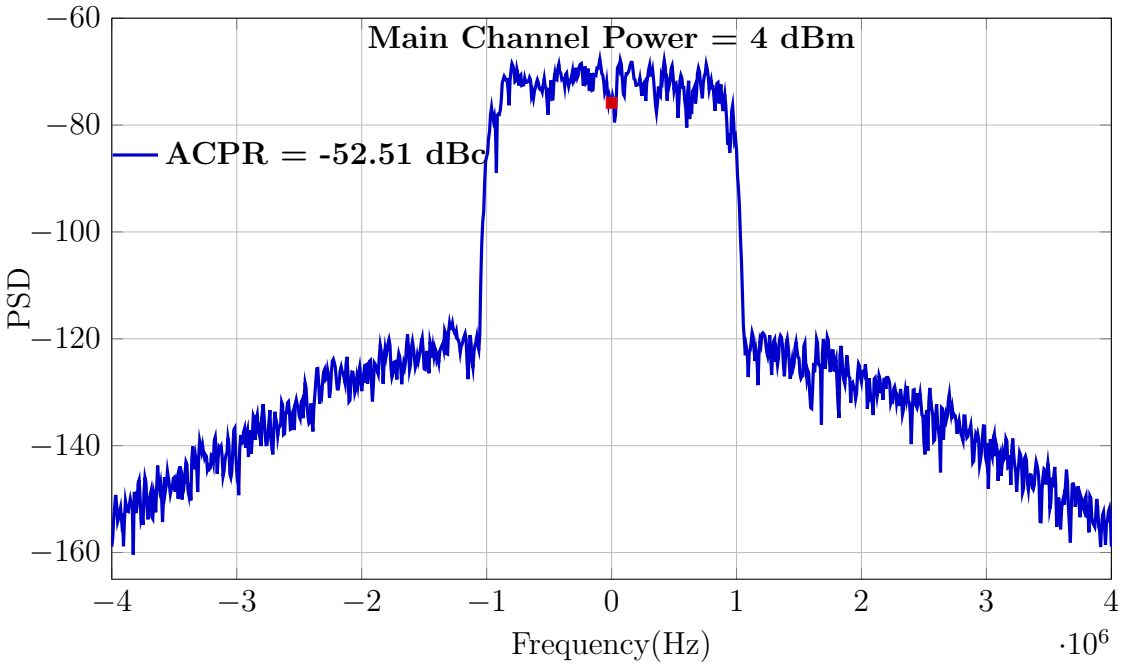

Figure 3.8: Differential PA - ACPR

of maximum output power, the ratio of in-band power to sideband power is the measure for ACPR. For class-2 of Bluetooth, the main channel power should be 4 dBm, main channel bandwidth is 2 MHz, the ACPR thus measured of PA alone is shown in Fig .3.8 and the value is -52.51 dBc.

3.4 Class A Single-Ended Power Amplifier

Following the architecture explained in section 2.3.1, a single-ended class-A PA is implemented. The schematic of single-ended PA is shown in Figure 3.9. A cascode

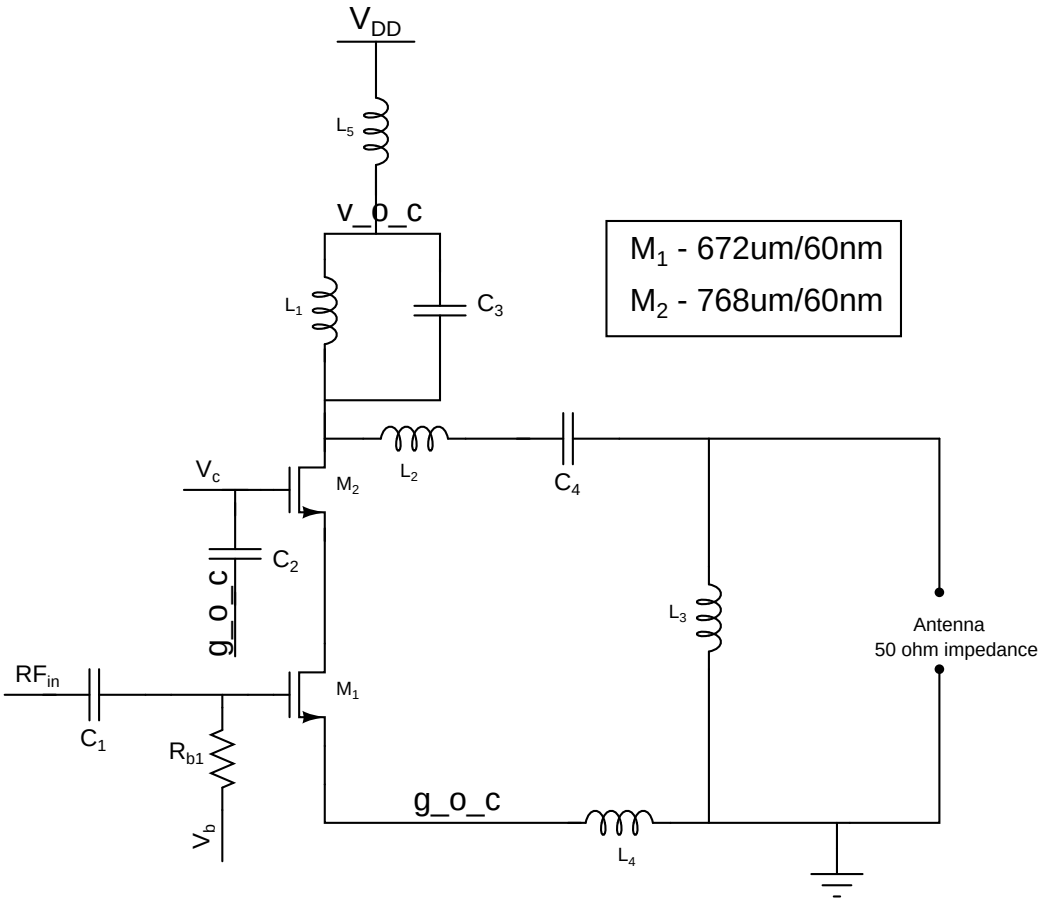

Figure 3.9: Single-Ended PA - Schematic

configuration is implemented to share the swings of the output so as to avoid break down of transistor. The DC current of the designed single-ended PA is 13.93 mA.

3.4.1 Passive Components of Single-Ended PA

At Input : At the input the capacitor C_1 is to block the DC voltage coming from the mixer output and the value is selected such that the entire signal appears across the C_{GS} of M_1 and there is no signal drop across C_1. The resistor R_{b1} is to provide the DC bias voltage to M_1 and the value is chosen such that the parallel combination of R_{b1} and C_{GS} of M_1 is mostly capacitive. The final value of C_1 is 12.8 pF and R_{b1} is 23.7 KΩ. The value of C_2 is chosen so that the gate of M_2 will be a signal ground and also to get the desired output compression. The value is 37.5 pF. As this capacitor is not in the signal path a MOS capacitor is used as it has better density and thus consumes lesser area. The bias voltages V_b and V_c are chosen so as to meet the specification on linearity.

Output Tank Circuit : An inductor is required at the output of PA to allow the voltage at the drain to swing above the supply. This inductor is placed on-chip and a spiral inductor from UMC 65 nm is used. The value is chosen high enough such that current through it is substantially constant (so as to act as a current source) and it has a high Quality factor as any series resistance to the inductor will dissipate the power which will degrade the efficiency. The value is 2.8 nH with a Q of 10.75. As there will be parasitic capacitance at the output node, it can be resonated with L_1. To resonate at the operating frequency an extra capacitance C_3 of value 1.6 pF is required. This tank circuit ensures that only the current at resonant frequency goes to load and all other currents are bypassed.

Output Matching Network : If 50 Ω is directly driven by the PA, for the output power requirement of 2.5 mW, the swing at the output is high and the output compression specification is not met. So an L-match network is used to down convert the 50 Ω to 16 Ω. To block the DC power into the load a series capacitor is required at output. Thus High-Pass L-match network is implemented with C_4 and L_3 of which L_3 transforms 50 Ω to 16 Ω and a series capacitor is required to resonate with L_3.

Bond Wires : As explained in section 2.3.1 the single-ended PA is sensitive to bond wires. So circuit level techniques have to be implemented to remove the effects of the bond wires. As shown in the Figure 3.9 the inductor L_4 of value 400 pH is used to model bond wire on the ground line. Here 'g_o_c' means 'ground_on_-chip'. As the series capacitance of matching network is in series with this bond wire, the value of the capacitor C_4 can be tuned so that it can be used to resonate with L_4. The matching network is chosen to be off the chip as tuning of the capacitor C_4 is required for a different value of L_4. As the matching network is off the chip, another bond wire L_2 is required at the output node of the cascode and C_4 can be used to resonate with this too. The values that are used here are, L_2 is 1 nH, C_4 is 2 pF, L_3 is 2.2 nH, L_4 is 400 pH.

The inductor L_5 of value 1 nH is used to model the bondwire on the V_{DD} line. Here 'v_o_c' means 'V_{DD}_on_chip'. To reduce the effect of the bond wires, a bypass capacitor of value 40 pF is placed between 'v_o_c' and 'g_o_c' to provide an alternate path for high-frequency transients. A MOS capacitor is used for this purpose as it has better density and its nonlinearity doesn't affect the performance as this is not in the signal path.

3.4.2 Layout and Post-layout Simulations of Single-Ended PA

The layout of single-ended PA (in Figure 3.9) is shown in Figure 3.10. In the

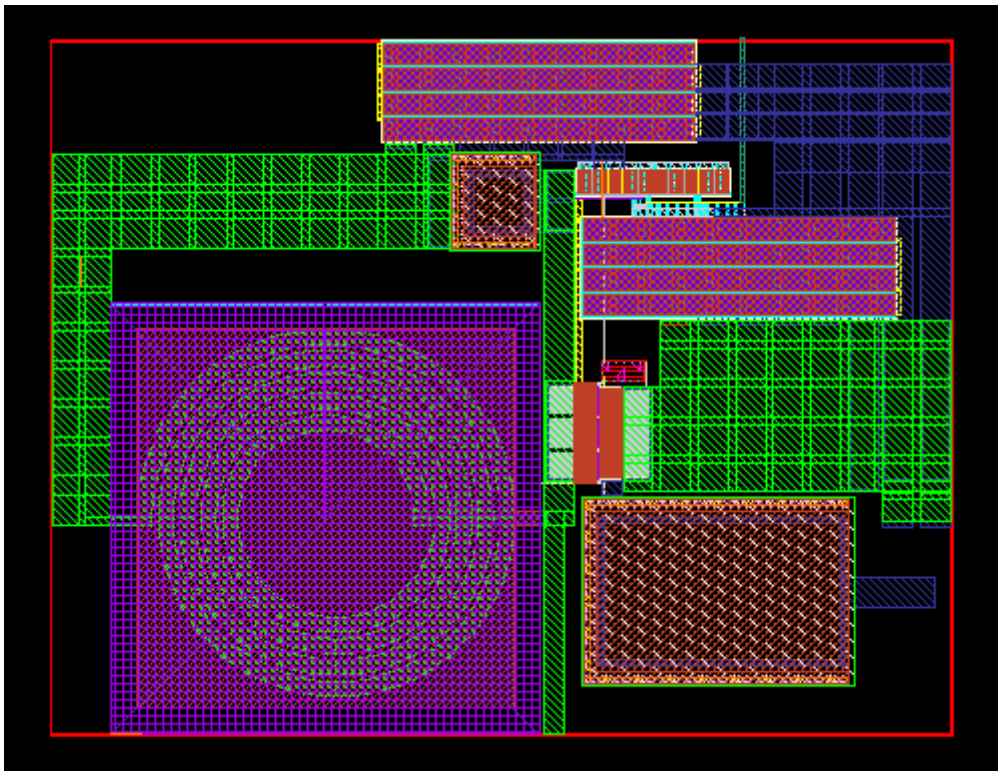

Figure 3.10: Single-Ended PA - Layout

layout shown, the spiral inductor is to the left with V_{DD} connection to its left. The capacitor C_3 is placed on the top of the inductor. The V_{DD} connection for these two is made with highest metal as any series resistance will decrease the Q of the tank circuit resulting in power dissipation. Towards the right hand bottom side of the inductor, is the input capacitor C_1. The MOS capacitor between the supply lines is at the top. Below that is the biasing circuitry and then another MOS capacitor (at the gate of cascode) C_2 is placed. The ground line connection is

made with the top 2 metals, again to reduce any series resistance. Both the supply lines are chosen wide enough as per the EMR to carry the current of 14 mA. A guard ring is placed enclosing the entire PA layout. The area consumed by this layout is 360 μm x 280 μm. After extracting the parasitics of the layout shown in Figure 3.10 the simulation results are given below:

Output Power vs Input Power : The output power of the PA versus the input power of PA is plotted in Figure 3.11. As shown in the figure, the input power required for a maximum output power of 4 dBm is -7.89 dBm. Thus the gain of the PA is 11.89 dB. Also in the same plot the gain compression can be observed.

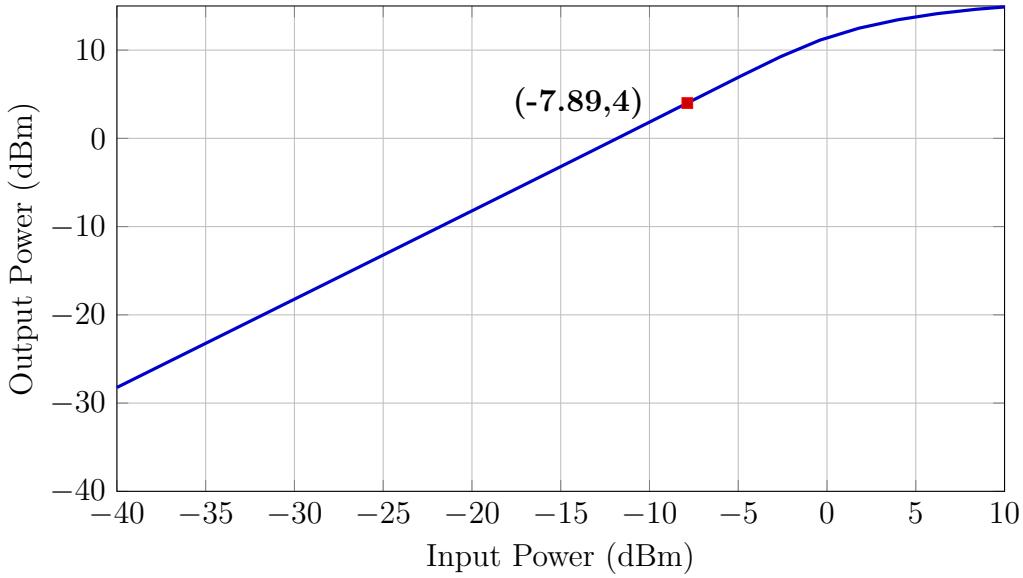

Figure 3.11: Single-Ended PA - Output Power vs Input Power

Comparing this with result of Differential PA shown in Figure 3.3 the single-ended PA is giving more gain as here the g_m of the input transistor is more than that of the Differential PA.

Drain Efficiency : The Drain efficiency can be calculated as:

$$\begin{aligned} \eta &= \frac{Output\ Signal\ Power(P_{sig})}{DC\ Power(P_{dc})} \\ &= \frac{2.5\ mW}{1.2\ V \times 14\ mA} \\ &= 14.88\% \end{aligned}$$

Fig.3.12 shows the drain efficiency of power amplifier.

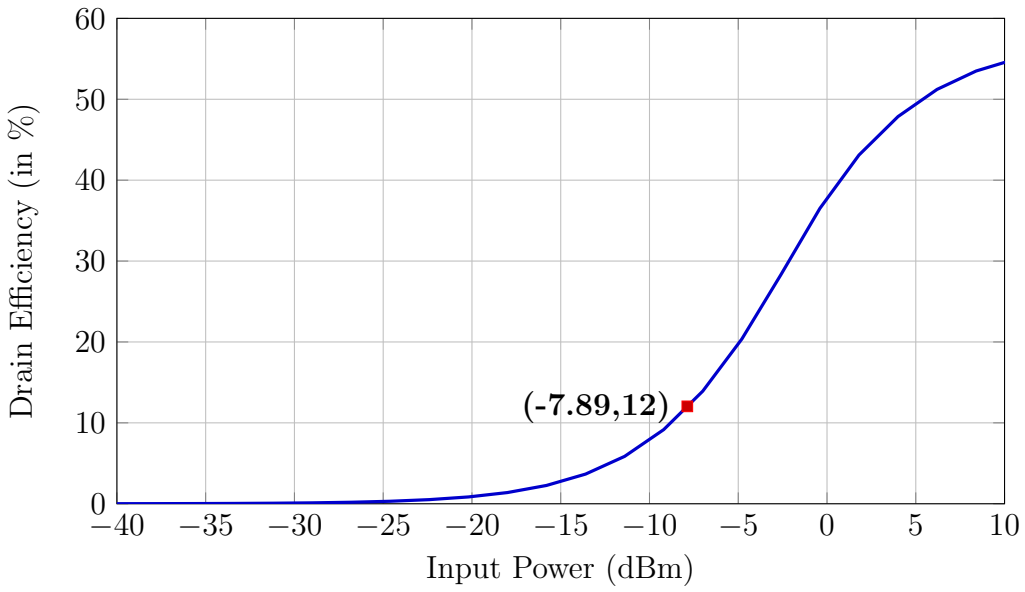

Figure 3.12: Single-Ended PA - Drain Efficiency

As in the Figure 3.12 the maximum drain efficiency is 12%. This is lesser than the theoretical value as there will be loss across the matching network, tank circuit and also the swing at the drain is not the maximum (V_{DD}). As compared to the result of differential PA shown in Figure 3.4, the single-ended PA is more efficient as the DC current required is a lesser and thus the power consumption is also reduced.

Power Added Efficiency (PAE) : From the equation 3.4, gain in Figure 3.11 and drain efficiency in Figure 3.12 the PAE is 10.93%. This is shown in Figure

3.13. This also is better than that of differential PA shown in Figure 3.5.

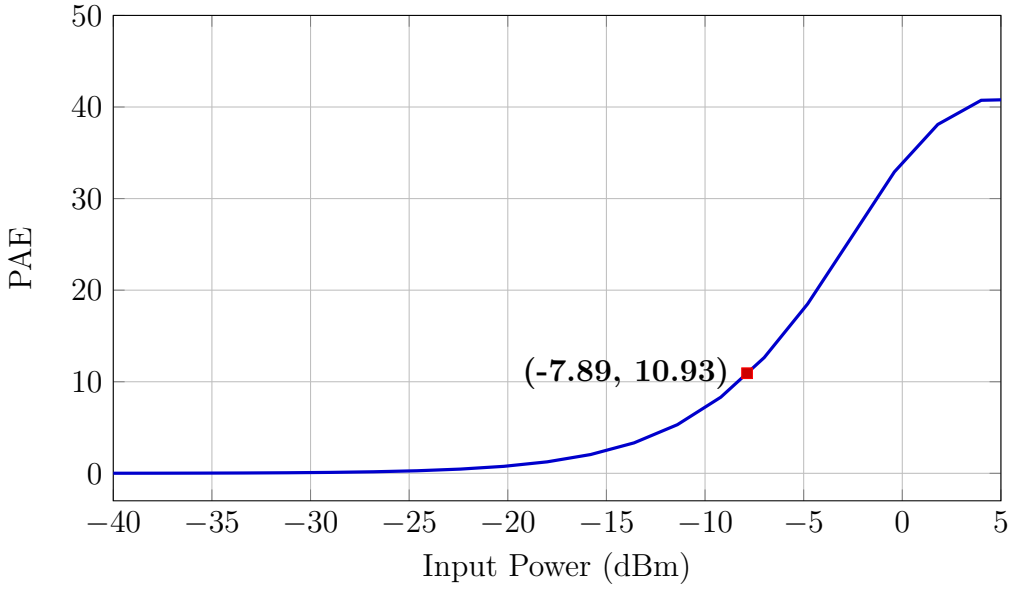

Figure 3.13: Single-Ended PA - Power Added Efficiency

Output Referred P1dB Compression Point : The Figure 3.14 shows the output compression curve of power amplifier alone. Thus the output referred P1dB compression point of PA alone is 13.34 dBm which is more than that of the differential PA shown in Figure 3.6.

AM/PM Conversion : The phase of the output voltage is plotted with respect to the input power. This is shown in the Figure 3.15.

The phase of the output voltage at low input power levels is -111.802°. The maximum phase change occurs for that input power at which maximum output power is obtained. Thus the phase at -7.89 dBm is -111.83°. So the maximum change in output phase is 0.028°. Compared to the result of differential PA shown in Figure 3.7 the phase change is smaller as in this configuration the gain is higher

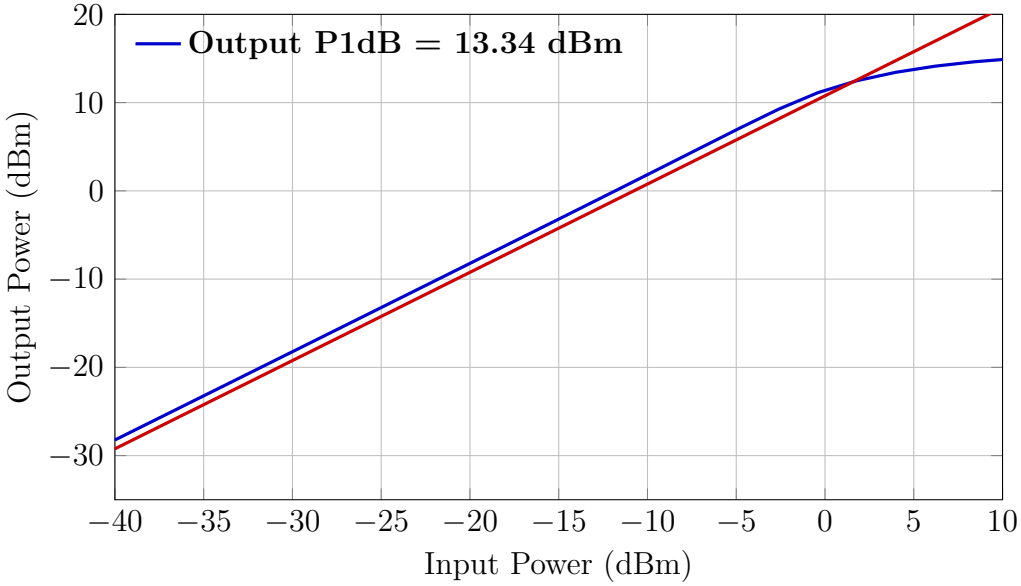

Figure 3.14: Single-Ended PA - Output Compression Curve

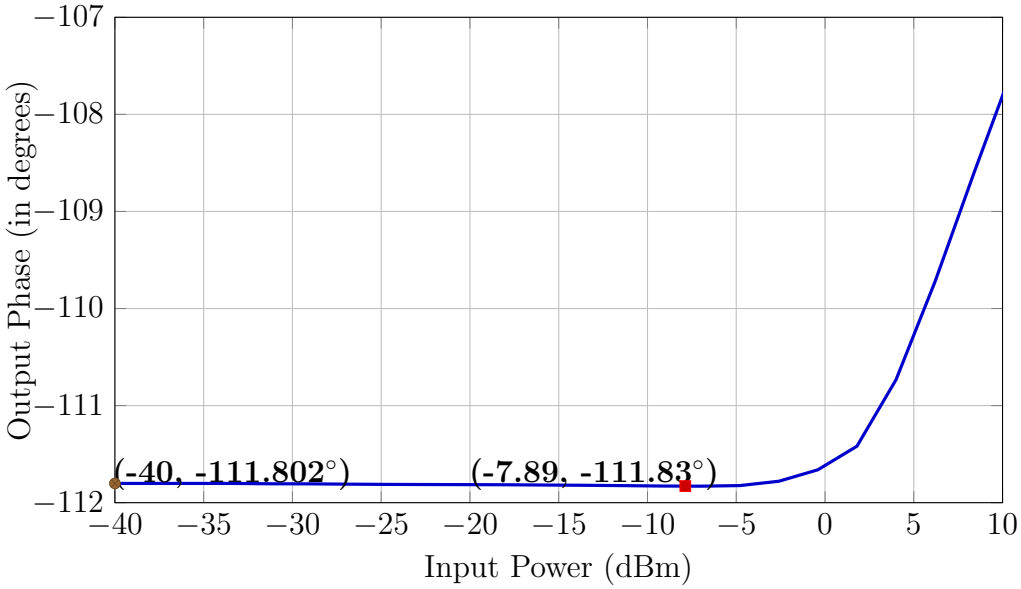

Figure 3.15: Single-Ended PA - AM/PM Conversion

and the input power required for the same output power is lesser so the change in phase is lesser.

Adjacent Channel Power Ratio (ACPR) : For the main channel power of 4 dBm, main channel bandwidth of 2 MHz, the ACPR thus measured of single-ended PA alone is shown in Figure 3.16 and the value is -56.13 dBc. Thus, the ACPR of the single-ended PA is better than that of the differential PA shown in Figure 3.8.

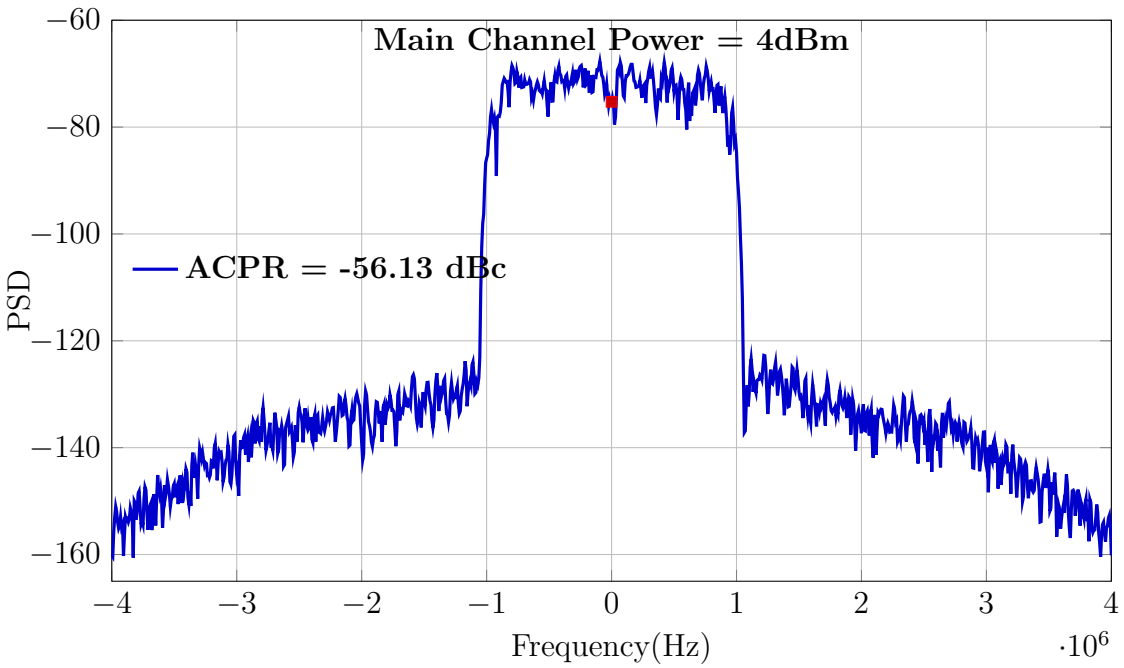

Figure 3.16: Single-Ended PA - ACPR

3.5 Comparing the Differential and Single-Ended PA

All the post-layout simulations of both differential and single-ended PA explained in sections 3.3 and 3.4 are in the table 3.1 for comparing the performance of the two configurations. From the table 3.1 for a lower DC current the single-ended PA

Metric	**Differential PA**	**Single-Ended PA**
DC current	22 mA	14 mA
Gain	8.37 dB	11.89 dB
Drain Efficiency	8%	12%
PAE	6.85%	10.93%
Output P1dB Compression	11.4 dBm	13.34 dBm
AM/PM	0.381°	0.028°
ACPR	-52.51 dBc	-56.13 dBc

Table 3.1: Comparison between Differential and Single-Ended PA

is giving better results. Also as per the architecture shown in Figure 2.4, the PA input capacitance, mixer switch ON resistance and filter output impedance form an RC network and the base-band filter needs to drive the mixer and PA (as in Figure 2.1). The transistors of the mixer switch at the LO frequency. The mixer output capacitance or the PA input capacitance has to be charged with in this period. This will set a constraint on filter output impedance, mixer switch ON resistance and the minimum filter op-amp DC current required to drive a given capacitive load else the mixer gain will decrease drastically which reduces the overall transmitter chain gain.

If the architecture shown in Figure 2.3 is implemented, the differential to single-ended conversion is done at the output of the mixer by using a trans-

former. With the inductance on the secondary side of the transformer, the PA input capacitance can be resonated out. With this the impedance seen on primary side will also be very large (ideally infinite). Then there is no need to have a high operating DC current for the MOSFETs of the filter op-amp as the mixer gain in this case doesn't degrade much, thus comparatively reducing the power consumption. Also as explained in the section 3.3 for the same balun, it is better to place it after the mixer rather than at the output of PA for better efficiency as the balun here reduces only the voltage gain but does not consume much power. So the architecture followed in this work is that shown in Figure 2.3 as the main objective is to reduce the area and power of the Bluetooth transmitter. Another advantage with this architecture is that the PA is isolated from the filter and mixer. But here as the PA is single-ended, it will be sensitive to package parasitics. As explained in section 3.4 all the effects due to bond wires are considered and the results mentioned are meeting the requirements.

Chapter 4

Mixer

4.1 Choice of mixer

Baseband information is shifted to RF band by mixer. Mixer performs frequency translation by multiplying two waveforms. They can be broadly categorized into passive and active topologies. Active mixers consume DC power whereas passive mixers do not. Passive mixer is implemented here to reduce the power consumption of transmitter chain. It is superior in terms of noise and linearity also. Baseband filter and mixer are fully differential, so the signal at output of mixer is fully differential. Hence a transformer is required after the mixer to perform differential to single-ended conversion as the PA implemented is single-ended.

4.2 Upconversion passive mixer

In passive mixer, the MOS transistor operates in either triode or cutoff region. It does not operate in saturation region. Mixer is a three terminal device. They suffer from unwanted coupling (feedthrough) from one port to another because of device capacitances. The gate-source and gate-drain capacitances create feedthrough from

the LO port to the RF and IF ports. The LO-RF feedthrough produces LO signal at the mixer output which is considerably large. Similarly all other feedthroughs are undesirable. To eliminate feedthroughs caused by capacitances, double balanced structure is implemented.

In double balanced passive mixer, the baseband and LO signals (ω_{IF} and ω_{LO}) are applied as inputs. The two upconverted signals ($\omega_{LO} \pm \omega_{IF}$) are produced at the output of mixer. One band has to be eliminated as both contain the same information. It is possible to get single sideband output with Cartesian architecture. Double balanced IQ passive mixer with the transformer at output for differential to single-ended conversion is shown in Fig. 4.1. It has two double balanced mixers one each for I and Q channel. The outputs of the mixers are added directly because of the 25% duty cycle of LO waveform. With 50% duty cycle LO, it is not possible to add the two outputs directly, because both I and Q channels will simultaneously be ON for some part of time. But with 25% LO duty cycle, I-channel and Q-channel MOS switches will not be ON at same instant. For this to happen, the overlap between the 25% duty cycle waveforms must occur at a voltage lesser than the threshold voltage of the MOS switches of the mixer. A baseband active RC filter is going to drive the mixer. Mixer operates in voltage mode as the follow up circuit is of high impedance because of the resonating network on the secondary side of the transformer.

A scalable rectangular transformer without center tap from UMC 65 nm process is used as the balun as shown in Figure 4.1. The transformer is selected such that it has high coupling factor(k). The capacitor C_1 is the capacitance additional to the C_{GS} of the PA required for resonance at the operating frequency. The value of this capacitor is 225 fF.

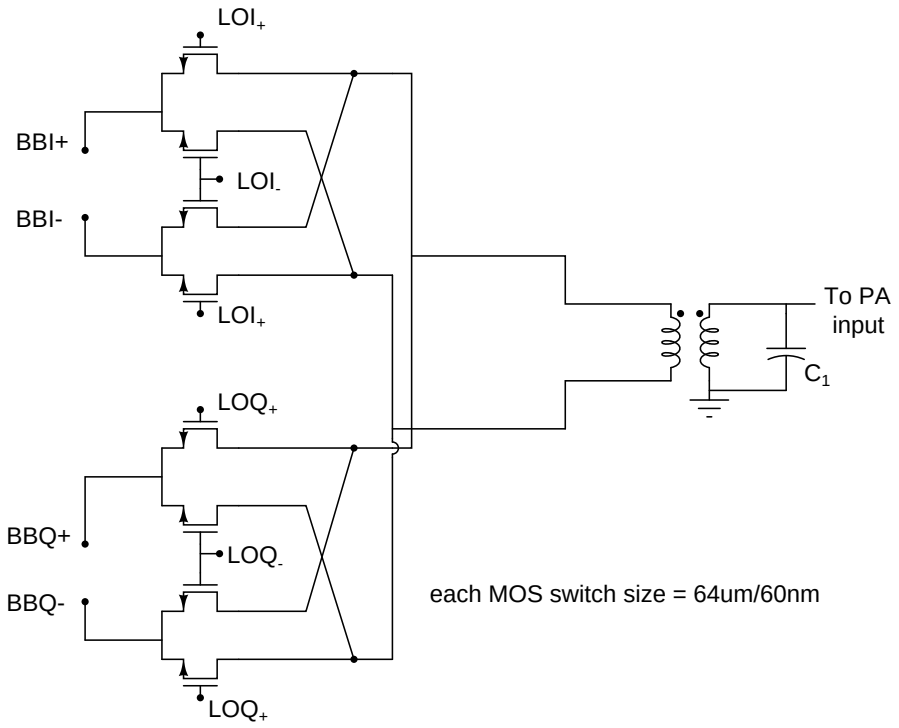

Figure 4.1: Double-Balanced Upconversion Passive Mixer with Transformer

4.3 Frequency divider with 25% duty cycle outputs

The frequency divider employs two D-latches in a master-slave configuration with negative feedback. The two identical D-latches are driven by complementary clocks. The basic principle of divider circuit is shown in Fig. 4.2. It looks like a counter operating at GHz of frequency. As there are two latches, there can be four possible outputs.

The circuit implementation for the frequency divider proposed by Razavi [3]. is shown in Fig. 4.3. Each latch consists of two sense devices (M_{s1} and M_{s2} in the master and M_{s3} and M_{s4} in the slave), a regenerative loop (M_{c1} and M_{c2} in the master and M_{c3} and M_{c4} in the slave), and two pull-up devices (M_{p1} and M_{p2}

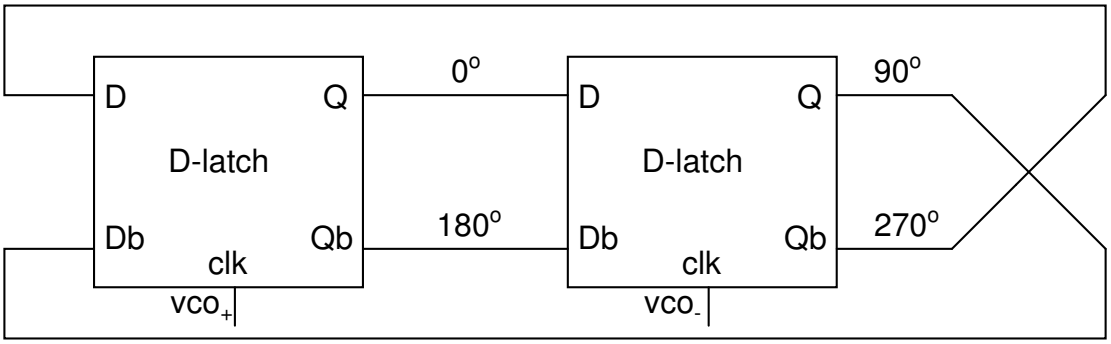

Figure 4.2: Basic Principle of Frequency Divider

in the master and M_{p3} and M_{p4} in the slave). A 4.8 GHz square signal drives the four PMOS transistors. When CLK is high, M_{p1} and M_{p2} are OFF and the master is in the sense mode, while M_{p3} and M_{p4} are ON and the slave is in the store mode. When CLK goes low, the reverse occurs. Out of four, two PMOS transistors turn ON at a time. They try to pull their drain terminals to V_{DD}. But a cross coupled NMOS in the same latch, tries to pull only one of them to V_{DD} and other to ground. The V_{DD} output is decided by the sense MOS transistors. Thus the circuit inherently generates a four-phase clock with 25%-duty-cycle signal.

To remove the ripple in the zero state and for proper pulse shaping, four buffers are added next to the divider, one for each output line of the divider circuit. The entire block diagram of LO generator circuit is given in Fig. 4.4. The buffer is a two-stage inverter to enhance the drive capability. The sizes of the MOSFETs are chosen such that the overlap voltage is lesser than 300 mV (threshold voltages of MOS switches is 450 mV) and the rise/fall time is lesser than 40 psec. VCO produces differential 4.8 GHz sinusoidal signals. Two buffers follow the VCO and convert sinusoidal wave into rail-rail square waves for the complementary clocks to the divider circuit.

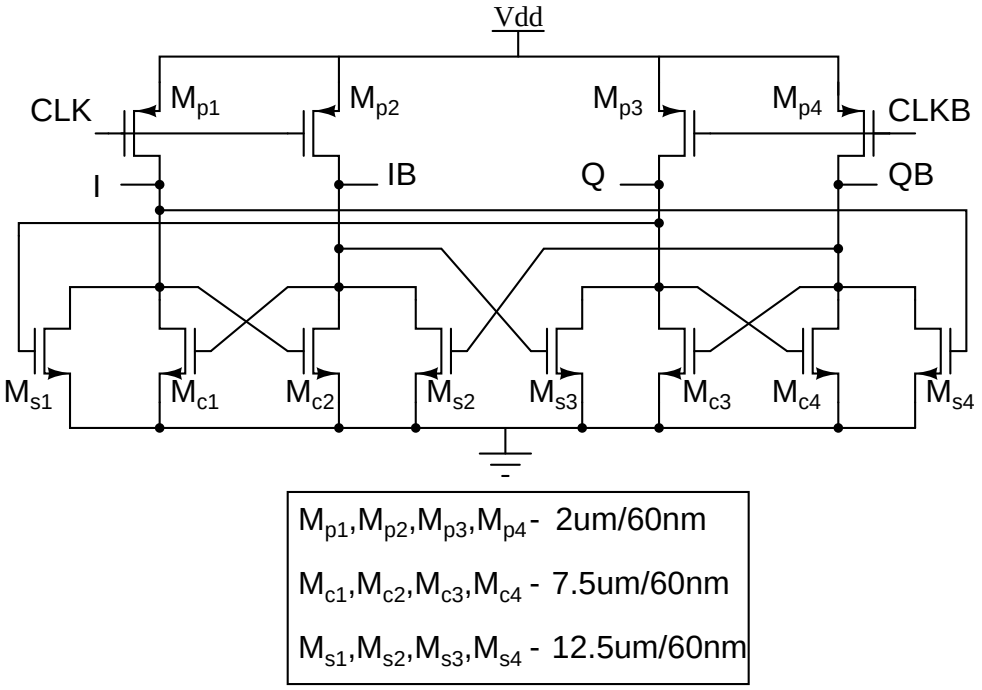

Figure 4.3: 25% Duty Cycle LO Generator

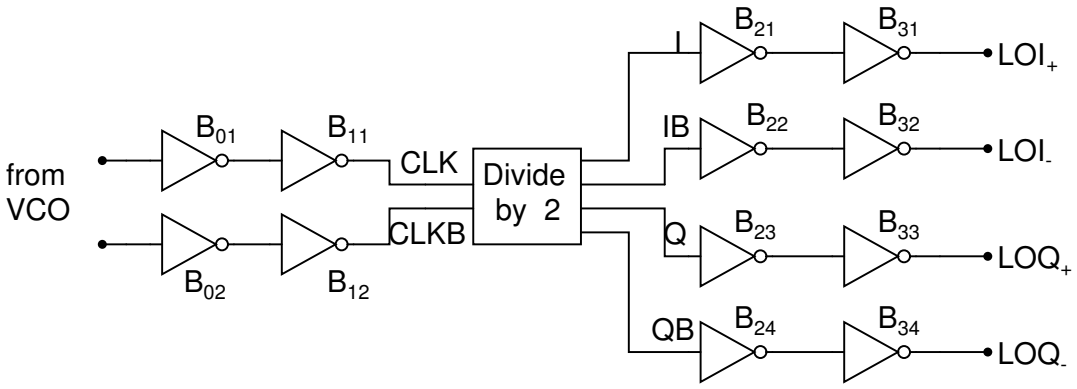

Figure 4.4: Complete LO Generator

4.4 Layout and Post-Layout simulation of Mixer and Frequency Divider

The layout of the passive mixer with 25% duty cycle LO generator along with the buffers is shown in the Figure 4.5. In the Figure 4.5 to the extreme left is the clock buffer. To its right, in the center, divide by 2 circuit is placed with master on top and slave at bottom. The buffers after the divide by 2 circuit shown in Figure 4.4 are placed above and below the divide by 2 circuit .To the extreme right, the 8 MOSFETs of the passive mixer shown in Figure 4.1 are laid out.

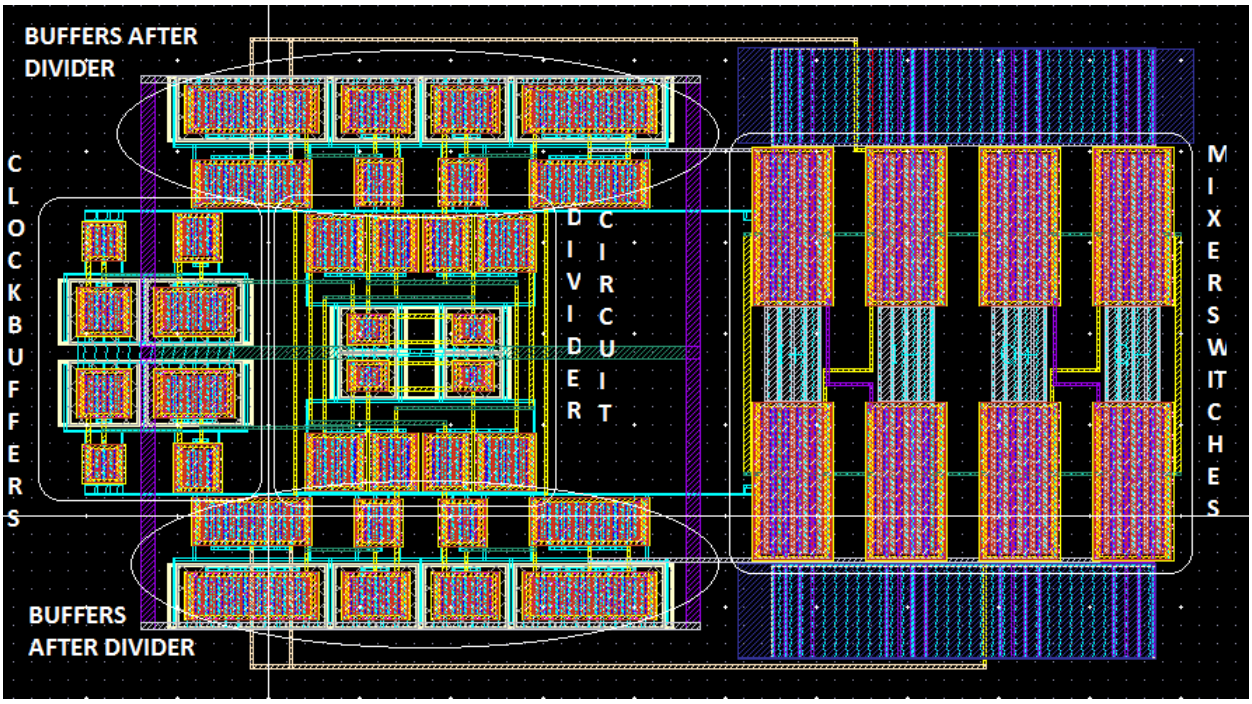

Figure 4.5: Layout of Mixer and Frequency Divider

The layout of the mixer, frequency divide by 2 circuit including the transformer and the capacitor of the Figure 4.1 is shown in Figure 4.6. The area consumed by this layout is 380 μm x 275 μm. After extracting the parasitics of the layout shown

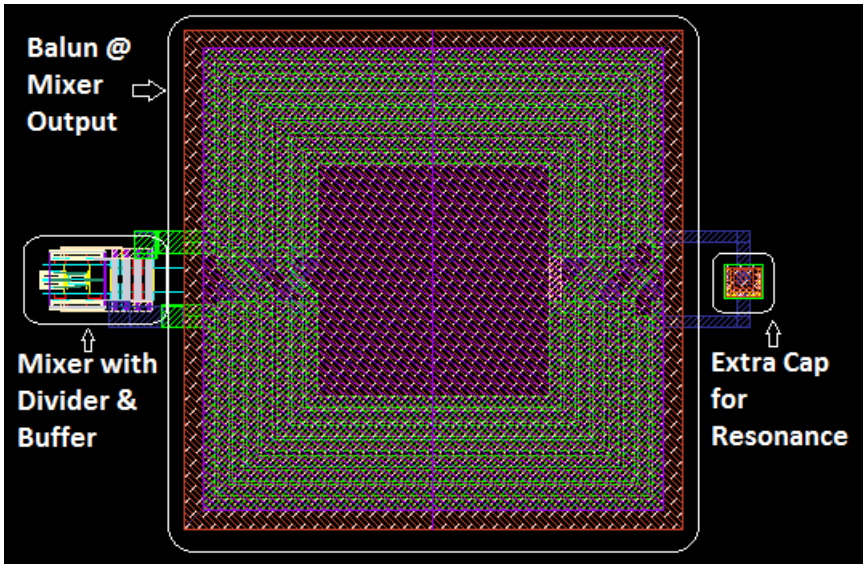

Figure 4.6: Layout of Mixer and Frequency Divider with Transformer and Capacitor

in Figure 4.6 the simulation results are:

4.4.1 25% LO Waveforms

The output waveforms of the frequency divide by 2 circuit with 25% duty cycle are shown in the Figure 4.7.

As explained in the section 4.3, the buffer circuit removes the ripple in the zero state and does pulse shaping. The output of the buffer circuit is shown in the Figure 4.8.

In the Figure 4.8 the waveforms from top are LOI_+, LOQ_+, LOI_-, LOQ_- respectively with reference to the Figure 4.4. The overlap between every two waveforms is around 247 mV as shown in Figure 4.9. The rise/fall times of all the waveforms is 36.3 psec. Thus the waveforms meet all the requirements. The average DC current drawn by the frequency divide by 2 circuit and all the buffers is 3.6 mA.

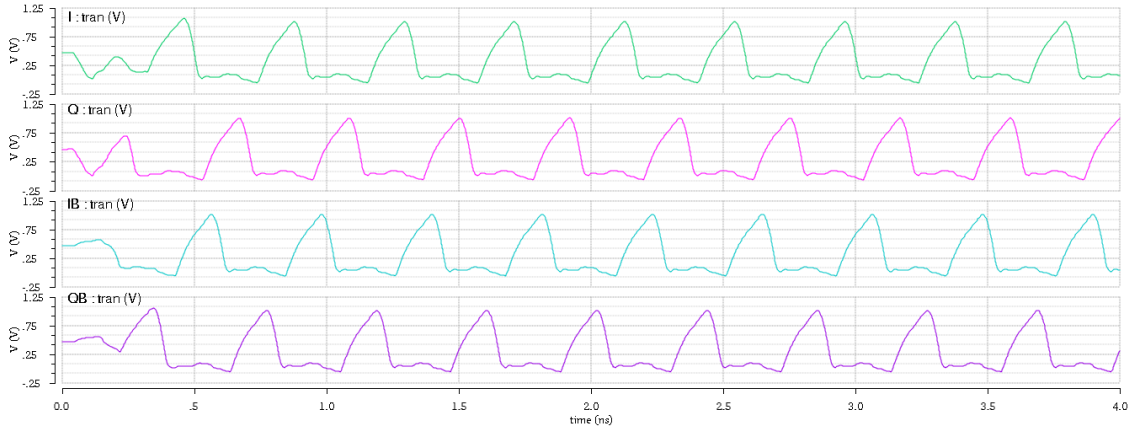

Figure 4.7: Output Waveforms of Frequency Divider Circuit

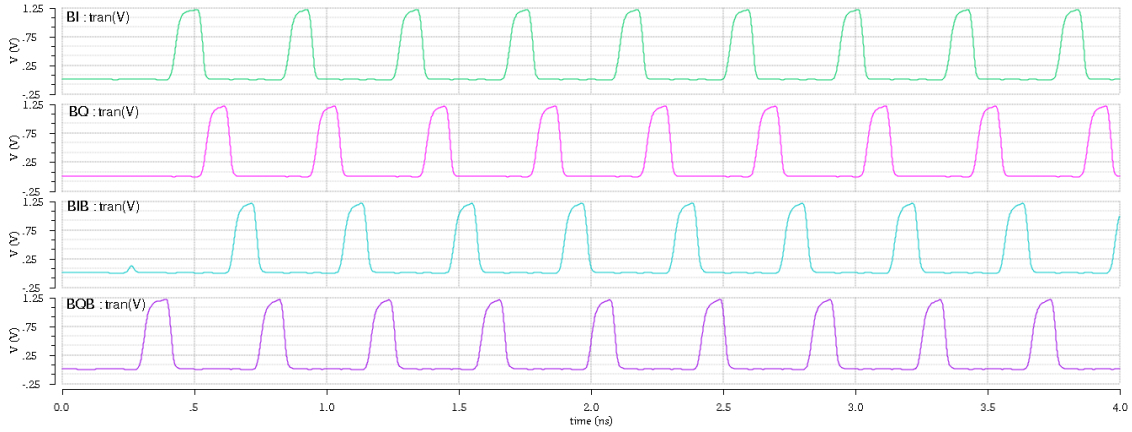

Figure 4.8: Output Waveforms of Complete LO Generator

4.4.2 Mixer Gain

The Fourier series expansion of ideal 25% duty-cycle LO waveform shown in Fig. 4.10, with frequency ω_{LO} is given by,

$$x_{LO}(t) = \frac{2\sqrt{2}}{\pi}\left\{\sin\omega_{LO}t - \frac{1}{3}\sin 3\omega_{LO}t + \frac{1}{5}\sin 5\omega_{LO}t - \frac{1}{7}\sin 7\omega_{LO}t + \ldots\right\} \quad (4.1)$$

Ideally the gain of IQ mixer should be -0.9 dB. The LO waveforms are not ideal

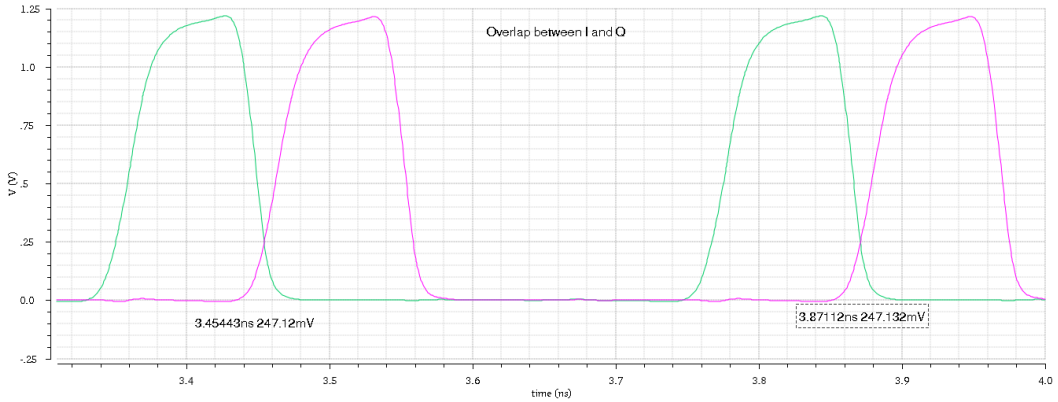

Figure 4.9: Overlap Voltage between LOI_+ and LOQ_+

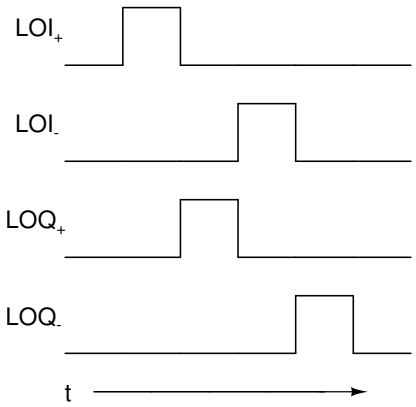

Figure 4.10: Quadrature LO Waveforms

as shown in Figure 4.8 with non-zero rise/fall times and overlap voltage. Also there is a finite switch ON resistance (8 Ω), filter also has non-zero output resistance, and as Q of the resonating network on the secondary side of the transformer is not infinite, the resistive part will get reflected to the primary side. All these resistances cause a decrease in gain and the gain obtained is shown in Figure 4.11.

Thus the volatge conversion gain of the passive mixer is around -2 dB. The X-axis in the Figure 4.11 is frequency varying from 2.4 GHz to 2.401 GHz.

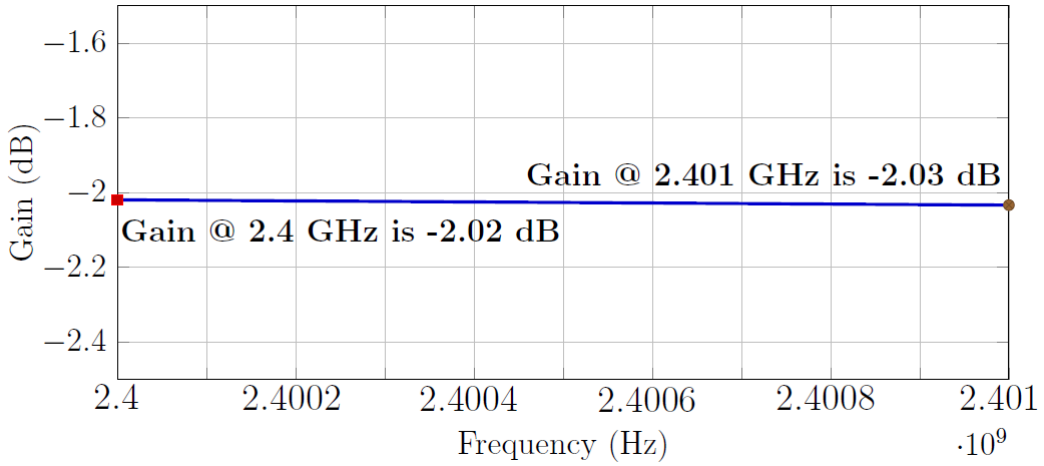

Figure 4.11: Passive Mixer Voltage Conversion Gain

4.4.3 Mixer Output P1dB Compression Point

At power amplifier output P1dB required is 10.3 dBm. The gain of PA is 11.89 dB. So at the mixer output, gain compression should not happen till -1.59 dBm (10.3 dBm - 11.89 dB). From the Fig. 4.12, it is clear that there is no gain compression till the output power of -1.59 dBm.

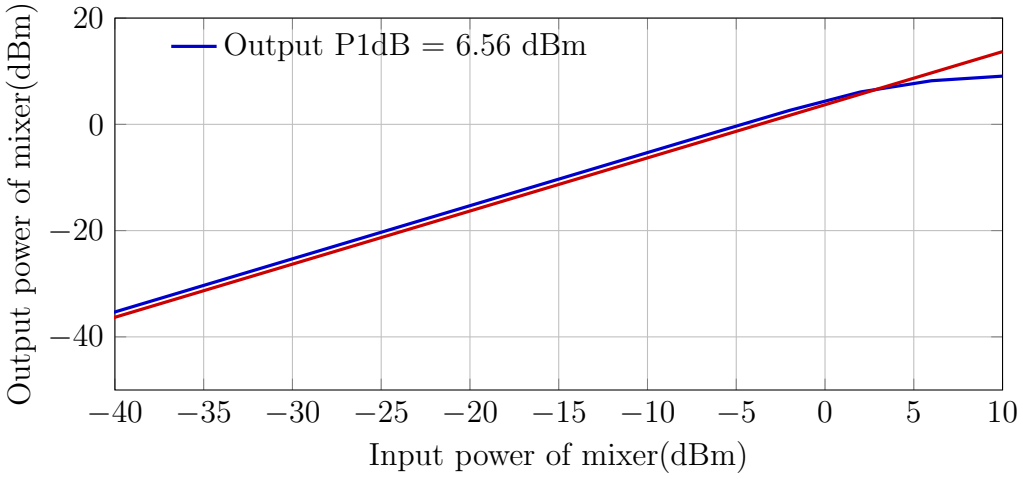

Figure 4.12: Mixer Output Compression Curve

Chapter 5

Baseband Filter

5.1 Role of Baseband Filter

A DAC drives the transmitter analog front end. It converts digital baseband information to analog form. But it produces images also at the multiples of conversion frequency. They are undesired and have to be attenuated. The role of the filter is to suppress all these DAC images. Filter has to provide required attenuation at conversion frequency without attenuating any in-band information. The amount of attenuation required can be calculated from the spectrum mask defined for transmitter. Spectrum emission mask for Bluetooth is given in Fig. 5.1 From the spectrum mask figure, it is clear that the ACPR requirement of Bluetooth transmitter is 26 dBc.

$$\begin{aligned} Maximum\ in\ band\ signal\ level &= 4\ dBm \\ Maximum\ out\ of\ band\ signal\ level &= -40\ dBm \\ Attenuation\ required\ at\ an\ offset\ of\ DAC\ conversion\ frequency &= 4 + 40 \\ &= 44\ dB \end{aligned}$$

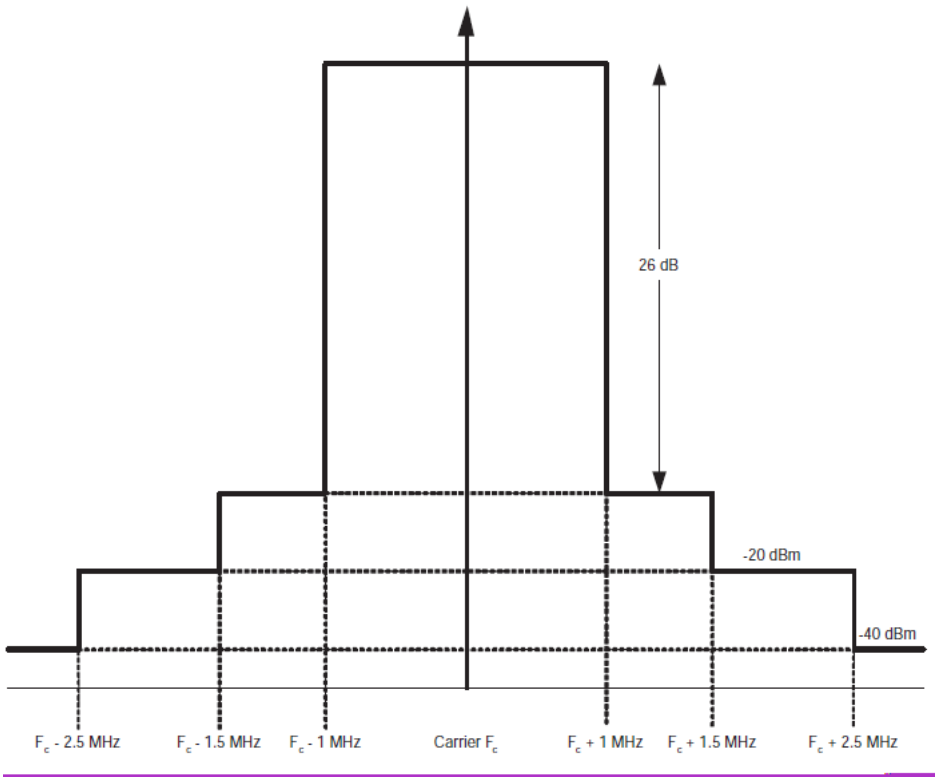

Figure 5.1: Spectrum Emission Mask

In most of research works for Bluetooth, DAC operating at 50 MHz conversion frequency is used. So the baseband filter has to provide a minimum attenuation of 44 dB at 50 MHz. At the same time, filter cutoff frequency should be sufficiently larger than 1 MHz.

5.2 Filter architecture

Typical topologies of filter implementation include the Gm-C and Active-RC architectures. The poles of Gm-C filter depend on the transconductance value which in turn is a non-linear function of the input. So Gm-C architecture based filters suffer from nonlinearity at high signal swings. Compared to Gm-C, Active-RC architec-

tures are more linear, less noisy and result in lesser distortion for the same amount of power consumption. In RF transmitters, linearity is very important concern. For these reasons, an Active-RC topology is chosen in the design of filter as the filter has to handle large swings in the order of hundreds of millivolts. Op-amp is the main block in active-RC filters. Fully differential op-amp is implemented to reject the common node noise. A fully differential implementation requires CMFB loop to ensure desired common mode voltages. A resistive common mode detector is used at the output for better linearity. A two stage op-amp is generally preferred, as single stage op-amps do not provide sufficient gain with resistive loading. Design of two-stage op-amp requires frequency compensation techniques for stability.

Feed forward technique and Miller compensation are the two different types of frequency compensation techniques. In the Feed forward technique, a zero is introduced by adding a parallel path from the input to the output. Then op-amp behaves as a second order system at low frequencies and as a first order system near its unity gain frequency. In the Miller compensation technique, the op-amp is stabilized by pole-splitting. By means of pole-splitting, the op-amp behaves mainly as a first order system. This technique results in a lesser bandwidth compared to the former, but the output swings are limited in the feedforward architecture. So the two-stage Miller compensated op-amp is used to realize the filter.

The design is started with a second order filter. Chebyshev filter is superior in terms of stop band performance. But even a 2^{nd} order Chebyshev filter with small ripple (0.1 dB) in the pass band fails to provide an attenuation of 44 dB in R_{min}-C_{min} corner. A 3^{rd} order filter is providing the required attenuation across all process, temperature, resistor and capacitor corners. Butterworth filter is implemented for maximally flat magnitude response in the pass-band.

5.2.1 3^{rd} order Butterworth filter

3^{rd} order filter is realized by cascade of one RC filter and one biquad. For the Butterworth filter,

$$\begin{aligned} The\ denominator\ of\ filter\ transfer\ function &= (s+1)(s^2+s+1) \\ Q\ of\ the\ biquad &= 1 \end{aligned}$$

The 3^{rd} order baseband filter is shown in Fig. 5.2. A_1 and A_2 are the two stage miller compensated op-amps. The first filter is a single pole RC filter. The second filter is a biquad. Biquad is implemented with single op-amp to minimize the power consumption. Active Rauch or Multiple Feed Back (MFB) topology is used to build the biquad because active RC filter can be implemented in fully differential structure.

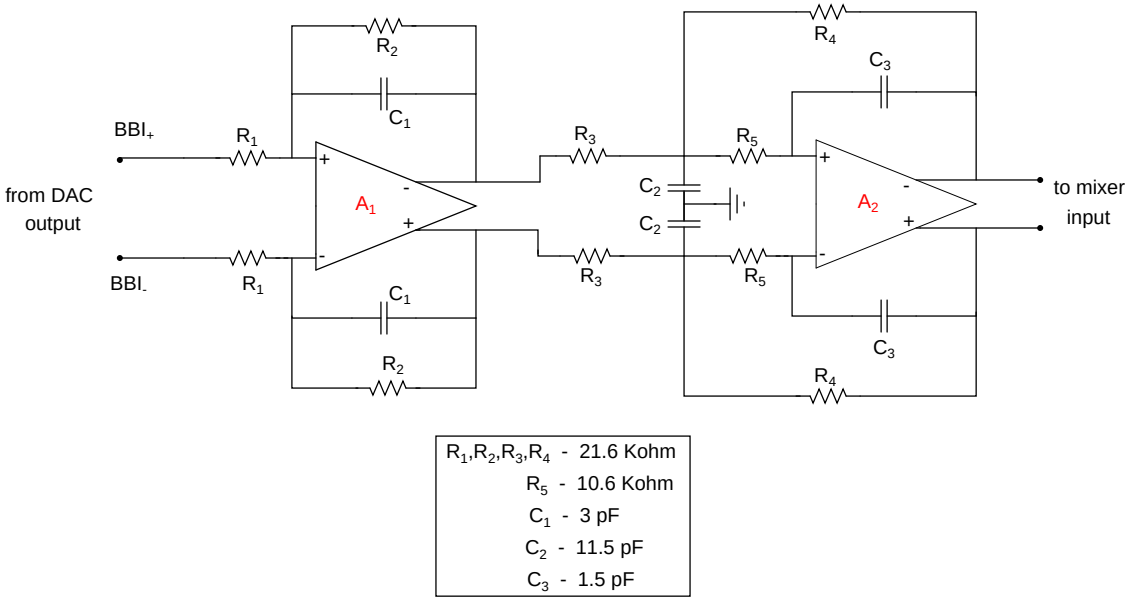

Figure 5.2: 3^{rd} Order Low Pass Filter

As explained in section 3.5 the baseband filter should drive the mixer. As the current into the mixer will be coming from the 2^{nd} stage of the 3^{rd} order filter, the op-amp A_2 (as in Figure 5.1) used in this stage should be biased such that the current required by mixer is delivered without saturating the op-amp output. Also the bandwidth of this op-amp must be selected such that the output impedance is as low as possible so that the mixer gain is not reduced. To reduce the power consumption and area, the op-amp A_1 is not maintained same as A_2 but is a scaled version so that the DC bias current is reduced.

5.3 Opamp Design

To reduce the flicker noise of the op-amp, PMOS transistors are used as the input pair for first stage. If the op-amp is implemented with two common mode feed back loops, then eight capacitors are required (two for $CMFB_1$, two for $CMFB_2$, two for Miller compensation, two for resistive common mode detection at $CMFB_2$ loop). These eight capacitors will occupy large area. To decrease the number of capacitors, single CMFB loop is used. Here only four capacitors are required. But this op-amp might face start up problems. To eliminate the start up problem, one half of the error amplifier of CMFB loop can be implemented as a part the first stage. Two stage Op-amp circuit diagram is shown in Fig. 5.3.

Common Mode Feedback Loop used for the two stage op-amp is shown in Fig. 5.4. The CMFB loop is a three stage amplifier. The same set of Miller compensating capacitors used for main op-amp are used for compensating in the CMFB circuit, with this the number of capacitors are reduced. It is already mentioned that resistive common mode detector is used to enhance linearity. But with only resistors R_{cm} (as in Figure 5.4), the parasitic capacitance at the input of the amplifier adds phase lag and degrades stability. So capacitors C_{cm} are connected in

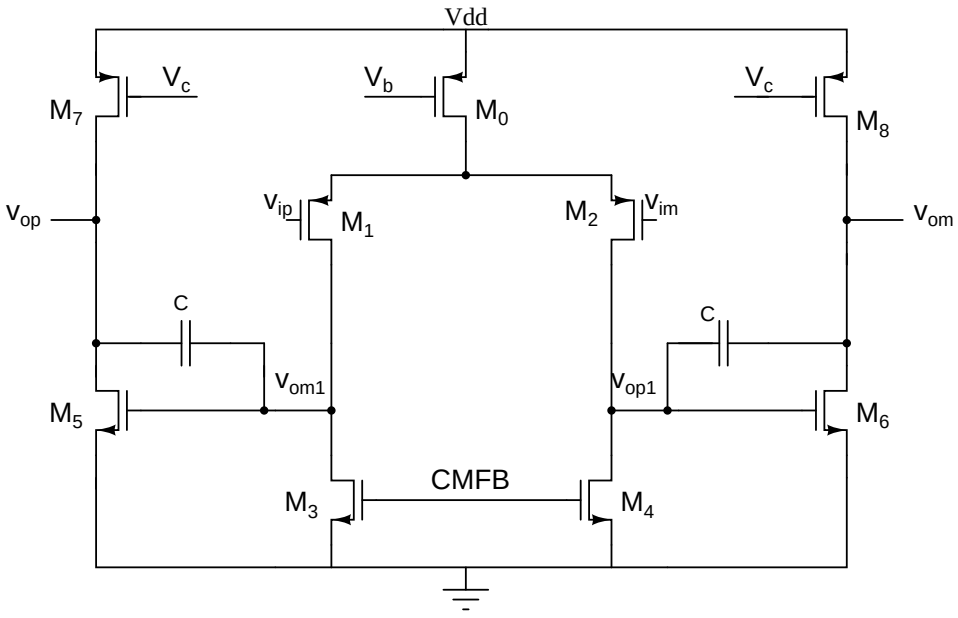

Figure 5.3: Two Stage Op-Amp

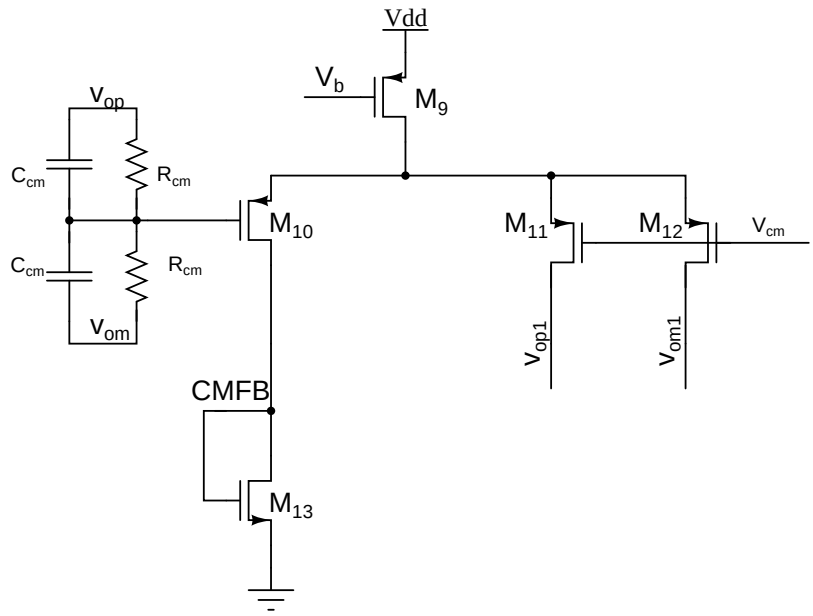

Figure 5.4: Schematic of the Common Mode FeedBack Loop

parallel to each resistor to introduce phase lead and ensure stability of the CMFB loop. With this the common mode voltage of the 2^{nd} stage is detected and that is compared with the a reference voltage V_{cm}. Based on the difference, currents are pumped into the output nodes of the 1^{st} stage and the CMFB is set to a voltage such that the current through M_3 of Figure 5.3 is equal to the current through M_1 of the main opamp and M_{12} of the CMFB circuit as in Figure 5.4. Similarly the current through M_4 is equal to current through M_2 and M_{11}.

5.4 Layout and Post-Layout Simulations of the Base-Band Filter

In this section, the component values, the corresponding layout and post-layout simulation results of the two op-amps and the filter in total are mentioned.

5.4.1 1^{st} Op-amp of the Base-Band Filter

The circuit diagram used for the 1^{st} op-amp is shown in Figure 5.3 and the CMFB circuit is shown in Figure 5.4. Following the same reference designation as in the schematic, the values of the components of 1^{st} op-amp is given in Table 5.1. The layout of this op-amp is shown in the Figure 5.5. In this figure, on the top is the first stage, next to it is the CMFB stage and towards the bottom is the second stage. The CMFB circuit is placed such that the entire layout is symmetric so that the frequency response on both the output lines is exactly the same. The area consumed by this layout is 90 μm x 50 μm. After extracting the parasitics of the layout shown in Figure 5.5, the simulation results are mentioned below:

Open Loop Response : The open loop magnitude response is shown in the Figure 5.6. The open loop phase response is shown in the Figure 5.7. The results

Table 5.1: Component values of the 1^{st} Op-amp

Circuit	Component Reference	Value
Main Op-Amp	M_0	10 μm/360 nm
	M_1,M_2	5 μm/360 nm
	M_3,M_4	2.5 μm/360 nm
	M_5,M_6	2.5 μm/180 nm
	M_7,M_8	5 μm/180 nm
	C	130 fF
CMFB	M_9	4 μm/360 nm
	M_{10}	2 μm/360 nm
	M_{11},M_{12},M_{13}	1 μm/360 nm
	R_{cm}	21.8 KΩ
	C_{cm}	51.2 fF

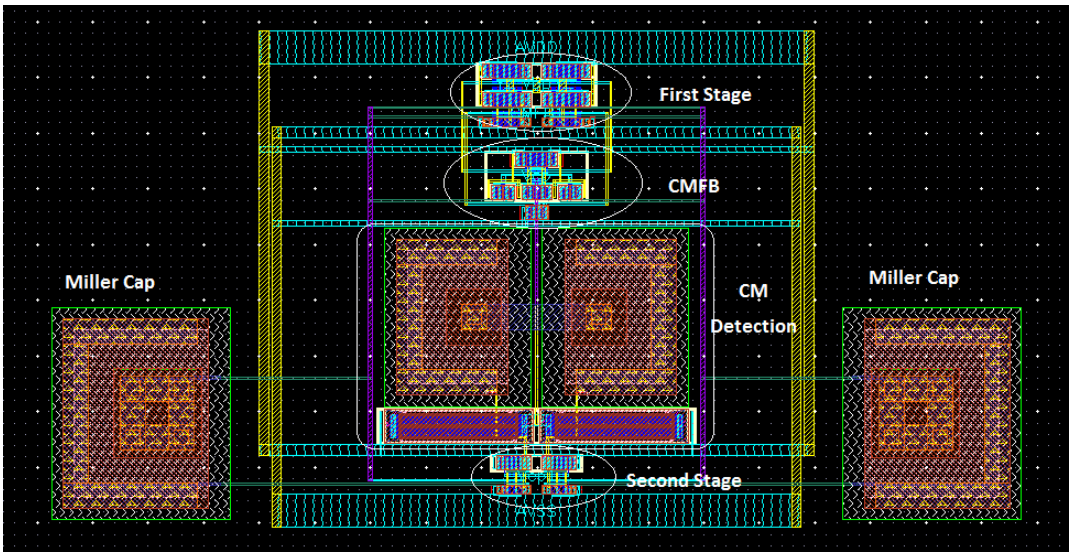

Figure 5.5: Layout of the 1^{st} Op-amp of the Base-Band Filter

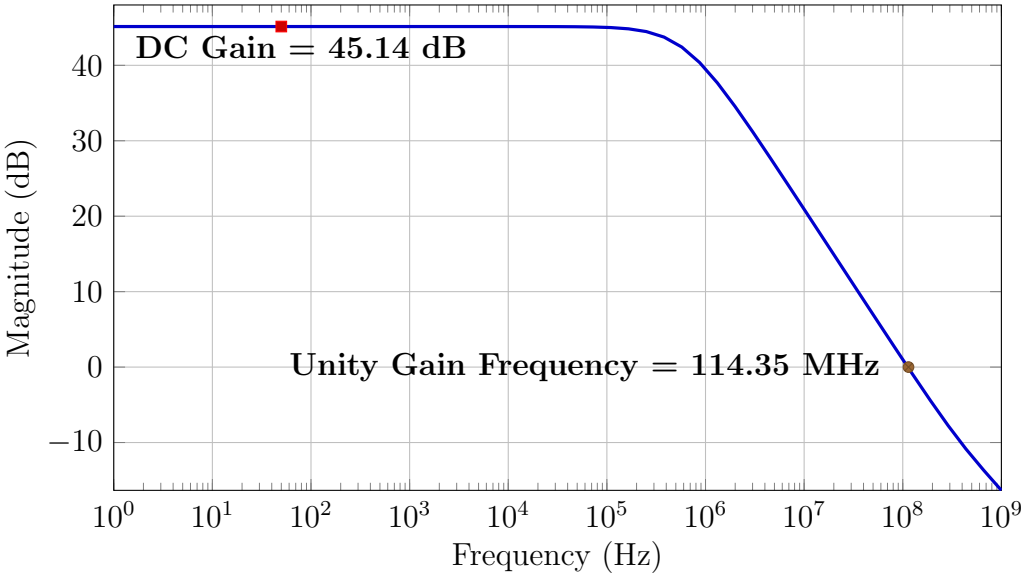

Figure 5.6: 1^{st} Op-Amp - Open Loop Magnitude Response

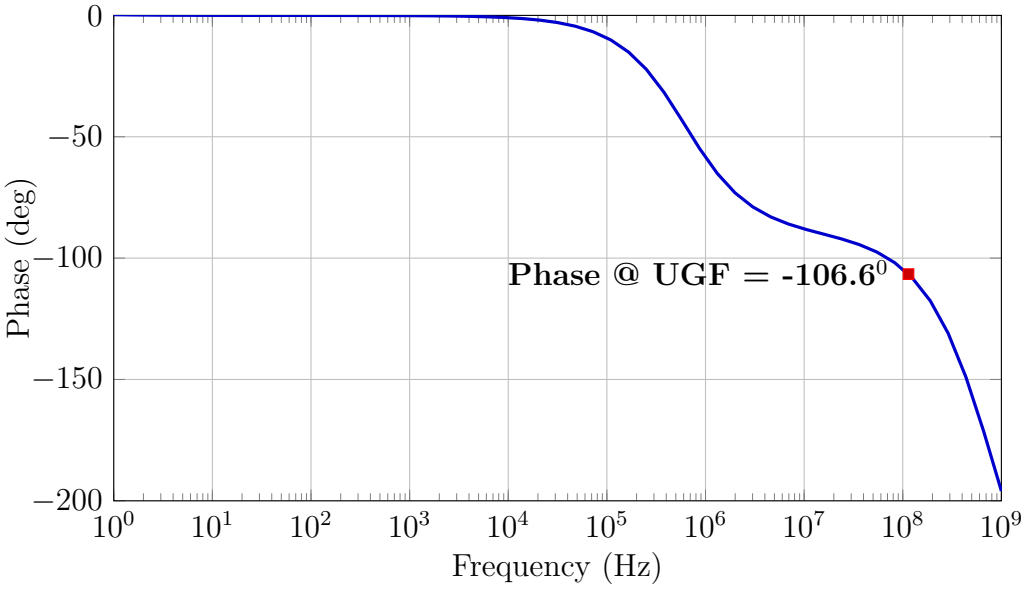

Figure 5.7: 1^{st} Op-Amp - Open Loop Phase Response

of the above are in table 5.2.

The op-amp feedback network is also included and the results of both the Dif-

Table 5.2: 1^{st} Op-Amp Open Loop Results

DC gain	45.14 dB
Unity gain frequency	114.35 MHz
Phase @ UGF	-106.6°
Total DC current	126.3 μA

ferential Mode(DM) and Common Mode(CM) loops are mentioned below:

Differential Mode Loop : The DM magnitude response is shown in Figure 5.8.

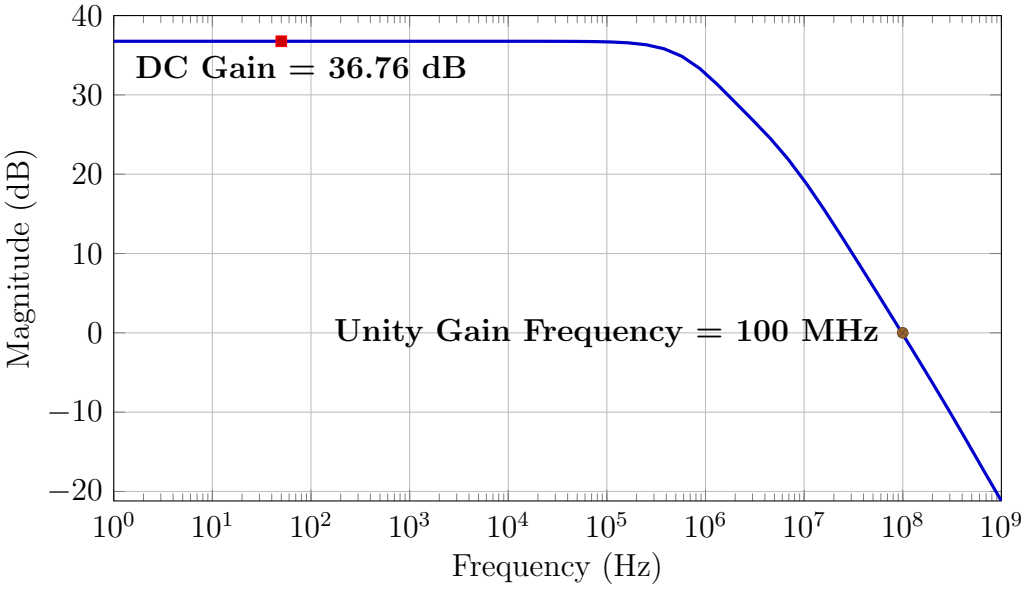

Figure 5.8: 1^{st} Op-Amp - DM loop Magnitude Response

The DC gain and the unity gain frequency here are less as compared to the open loop magnitude response shown in Figure 5.6 because the loop gain here includes the potential divider in the feedback circuit. The DM loop phase response is shown in the Figure 5.9.

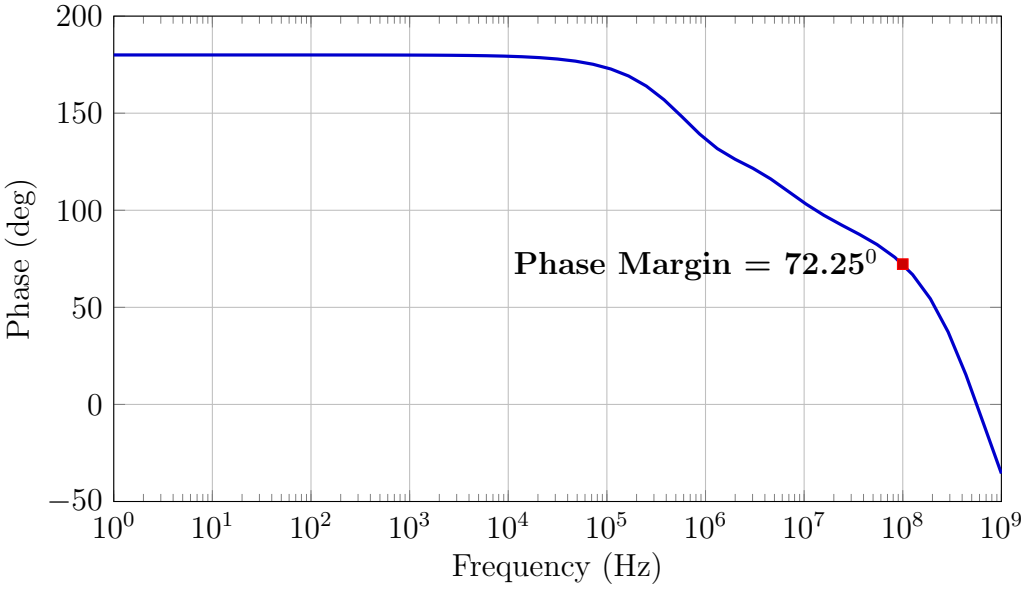

Figure 5.9: 1^{st} Op-Amp - DM Loop Phase Response

Common Mode Loop : The CM magnitude response is shown in Figure 5.10.

The CM loop phase response is shown in the Figure 5.11. The results of both the CM and DM loop are in table 5.3.

Table 5.3: 1^{st} Op-Amp - Phase Margin of Cm and DM Loops

Loop	**Unity Gain Frequency**	**Phase Margin**
CM	74.13 MHz	53.4°
DM	100 MHz	72.25°

From the phase margin values, it is concluded that both the CM and DM loops are stable.

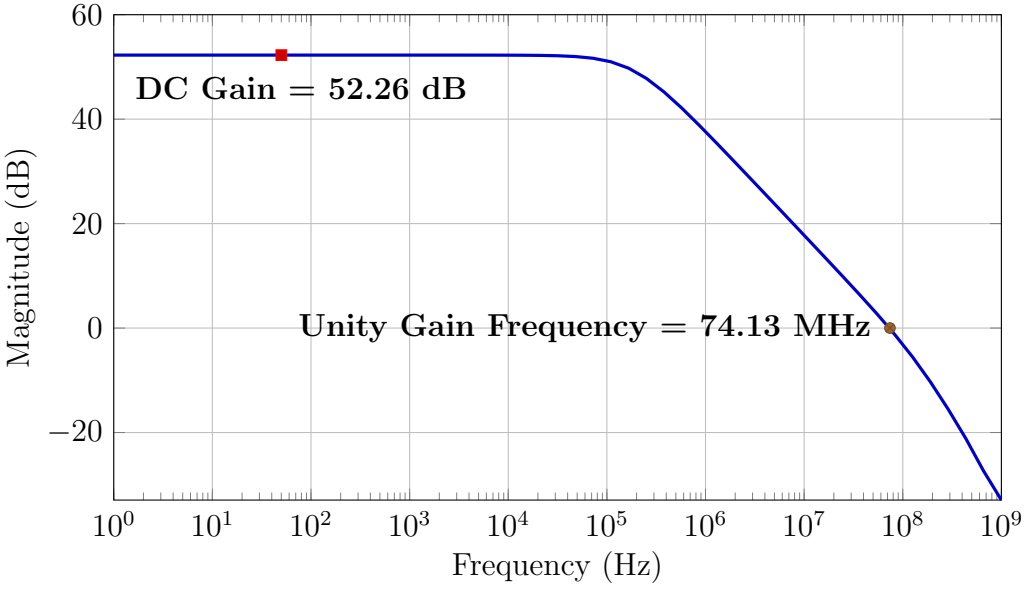

Figure 5.10: 1^{st} Op-Amp - CM loop Magnitude Response

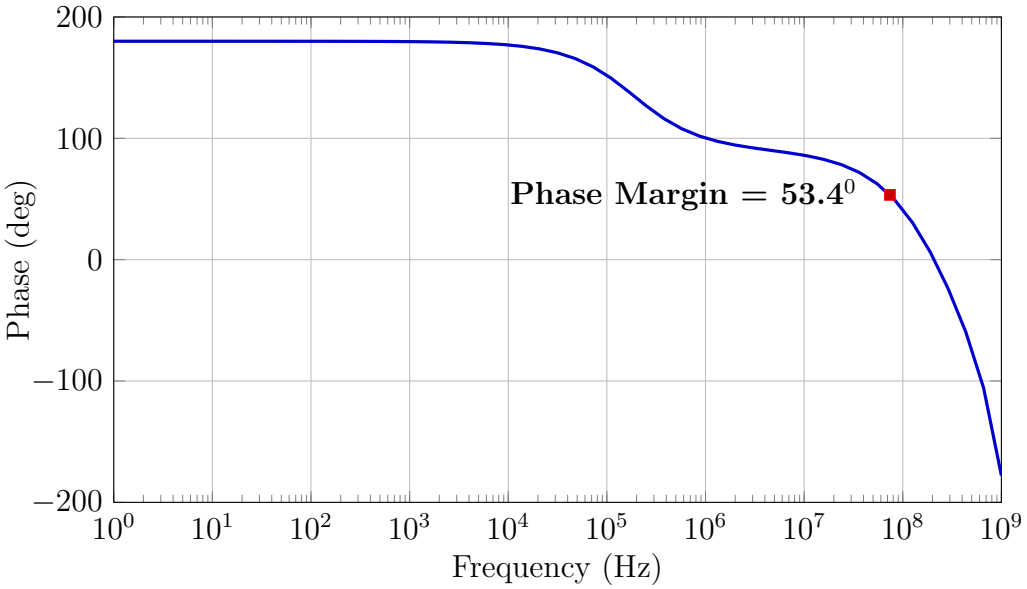

Figure 5.11: 1^{st} Op-Amp - CM Loop Phase Response

5.4.2 2^{nd} Op-amp of the Base-Band Filter

The circuit diagram used for the 2^{nd} op-amp is shown in Figure 5.3 and the CMFB circuit is shown in Figure 5.4. Following the same reference designation as in the schematic, the values of the components of 2^{nd} op-amp is given in Table 5.4. The

Table 5.4: Component values of the 2^{nd} Op-amp

Circuit	Component Reference	Value
Main Op-Amp	M_0	250 μm/360 nm
	M_1,M_2	125 μm/360 nm
	M_3,M_4	62.5 μm/360 nm
	M_5,M_6	25 μm/180 nm
	M_7,M_8	50 μm/180 nm
	C	5 pF
CMFB	M_9	50 μm/360 nm
	M_{10}	15 μm/90 nm
	M_{11},M_{12},M_{13}	7.5 μm/90 nm
	R_{cm}	21.8 KΩ
	C_{cm}	51.2 fF

layout of this op-amp is shown in the Figure 5.12. In this figure, on the top is the first stage, next to it is the CMFB stage and towards the bottom is the second stage. The CMFB circuit is placed such that the entire layout is symmetric so that the frequency response on both the output lines is exactly the same. The area consumed by this layout is 175 μm x 70 μm. After extracting the parasitics of the layout shown in Figure 5.12, the simulation results are mentioned below:

Open Loop Response : The open loop magnitude response is shown in the Figure 5.13. The open loop phase response is shown in the Figure 5.14. The results

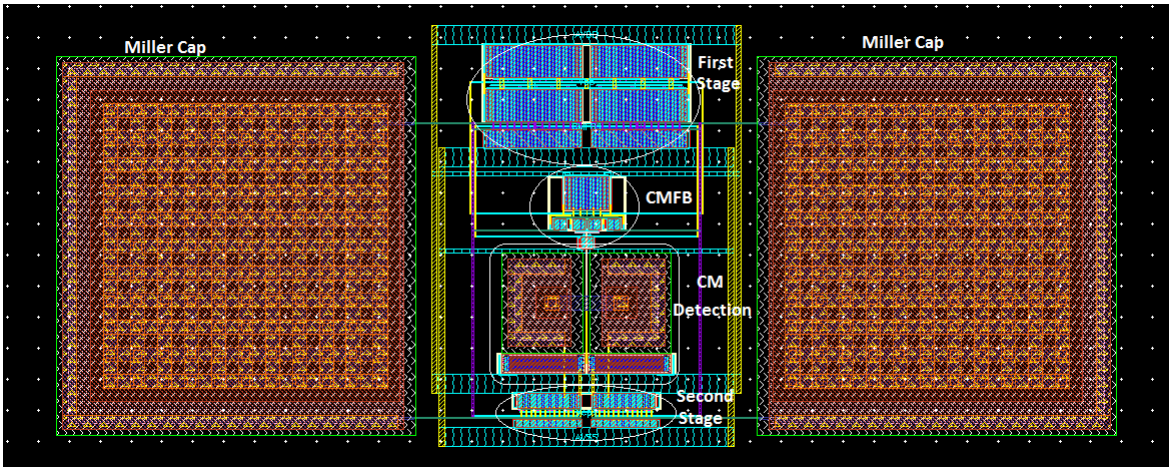

Figure 5.12: Layout of the 2^{nd} Op-amp of the Base-Band Filter

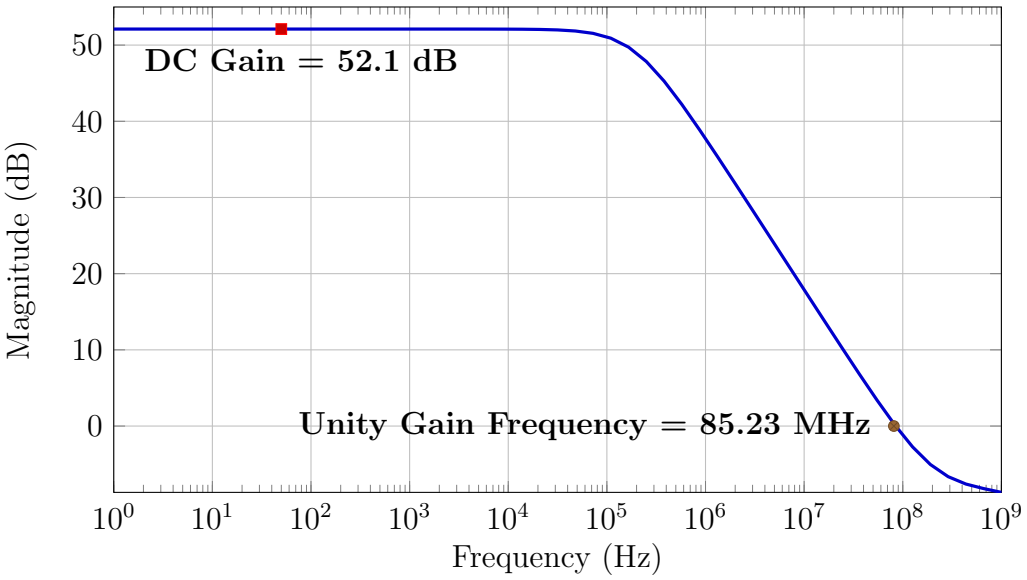

Figure 5.13: 2^{nd} Op-Amp - Open Loop Magnitude Response

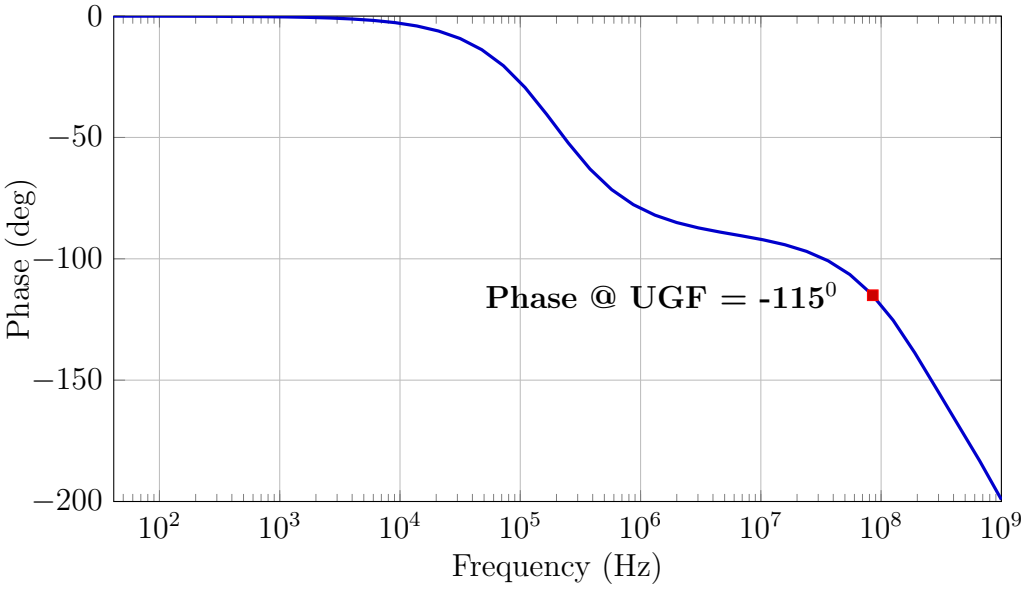

Figure 5.14: 2^{nd} Op-Amp - Open Loop Phase Response

of the above are in table 5.5.

Table 5.5: 2^{nd} Op-Amp Open Loop Results

DC gain	52.1 dB
Unity gain frequency	85.23 MHz
Phase @ UGF	-115°
Total DC current	1.55 mA

As explained in section 5.2.1 the DC current in the 2^{nd} Op-Amp is kept enough to drive the subsequent stages of the transmitter chain. Also of this current 600 μA is through each leg of the 2^{nd}stage of the op-amp as the current required by the subsequent stages of the transmitter chain will have to be delivered by this stage.

The op-amp feedback network is also included and the results of both the Differential Mode(DM) and Common Mode(CM) loops are mentioned below:

Differential Mode Loop : The DM magnitude response is shown in Figure 5.15.

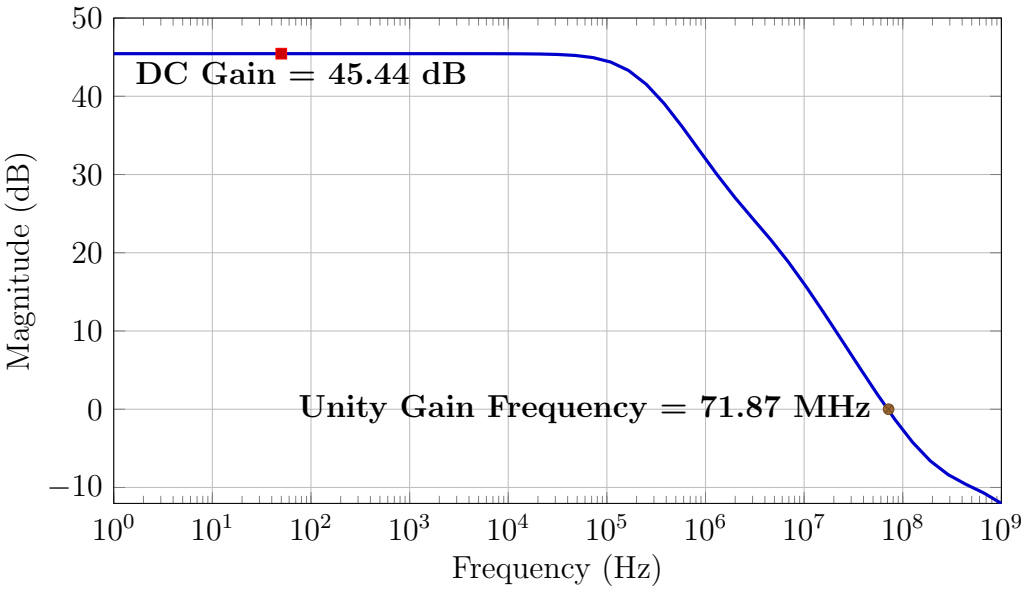

Figure 5.15: 2^{nd} Op-Amp - DM loop Magnitude Response

The DC gain and the unity gain frequency here are less as compared to the open loop magnitude response shown in Figure 5.13 because the loop gain here includes the potential divider in the feedback circuit. The DM loop phase response is shown in the Figure 5.16.

Common Mode Loop : The CM magnitude response is shown in Figure 5.17.

The CM loop phase response is shown in the Figure 5.18. The results of both the CM and DM loop are in table 5.6.

From the phase margin values, it is concluded that both the CM and DM loops of the 2^{nd} Op-Amp are also stable.

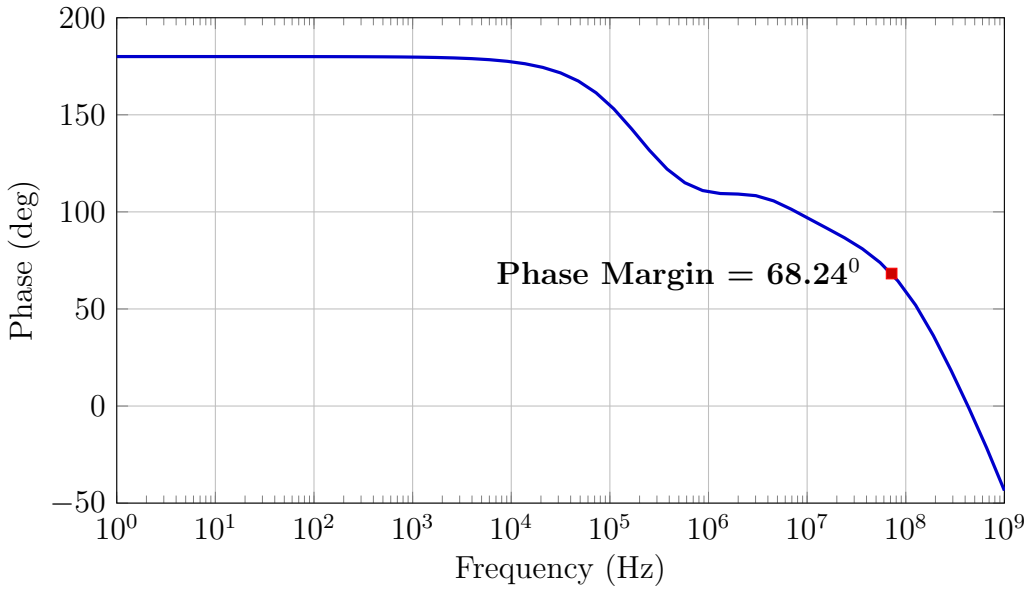

Figure 5.16: 2^{nd} Op-Amp - DM Loop Phase Response

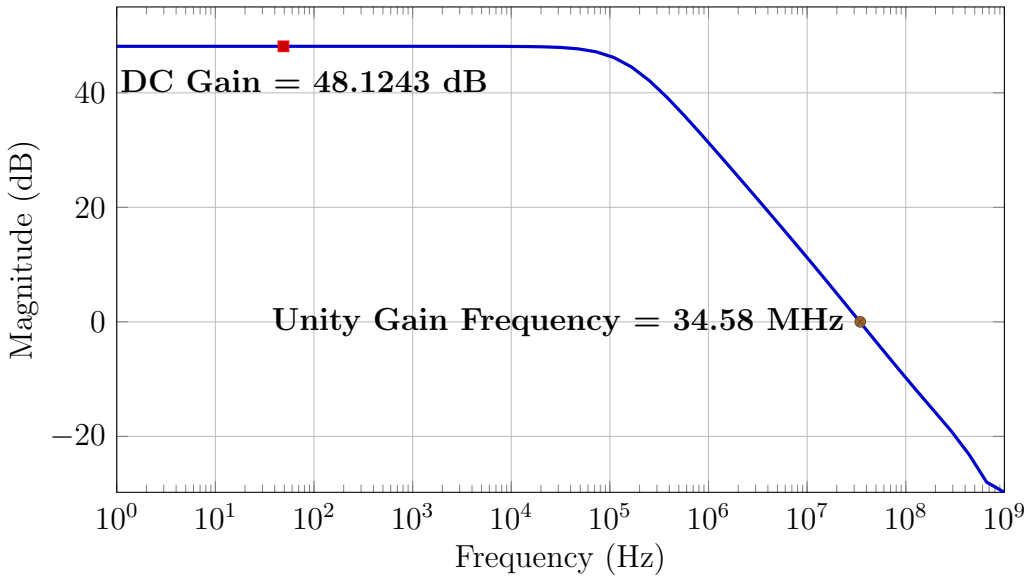

Figure 5.17: 2^{nd} Op-Amp - CM loop Magnitude Response

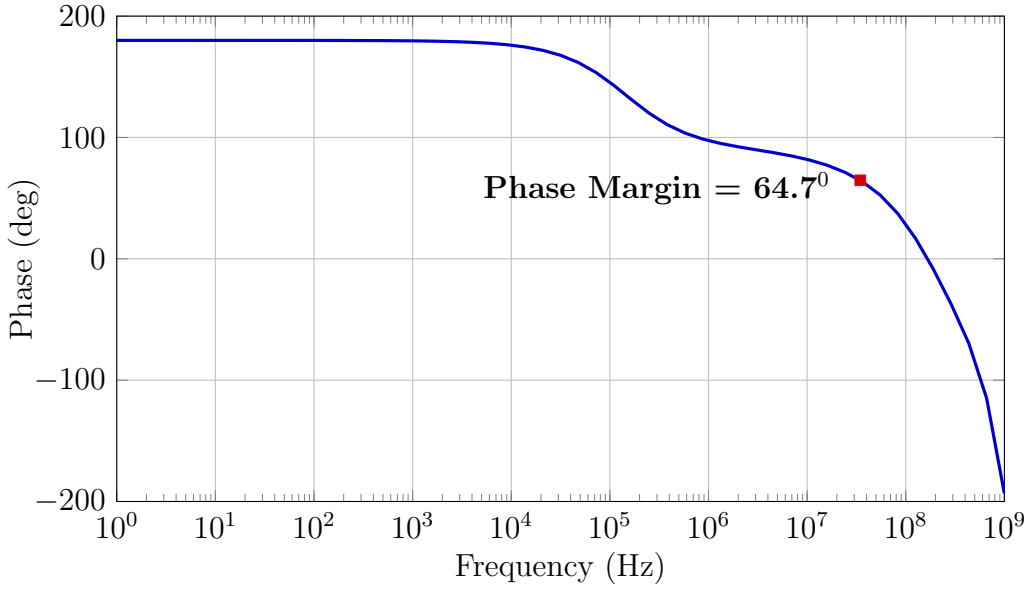

Figure 5.18: 2^{nd} Op-Amp - CM Loop Phase Response

Table 5.6: 2^{nd} Op-Amp - Phase Margin of CM and DM Loops

Loop	**Unity Gain Frequency**	**Phase Margin**
CM	34.58 MHz	64.7°
DM	71.87 MHz	68.24°

5.4.3 3^{rd} order Butterworth filter

The layout of the baseband filter (in Figure 5.2) is shown in Figure 5.19.

In the Figure 5.19 the 1^{st} op-amp is to the extreme left and towards the right is the 2^{nd} op-amp. The passive elements of the feedback circuit are all placed such that the circuit is exactly symmetric so that the frequency response on both the output lines is same. The area consumed by this layout is 250 μm x 230 μm. After extracting the parasitics of this layout, the simulation results are mentioned below:

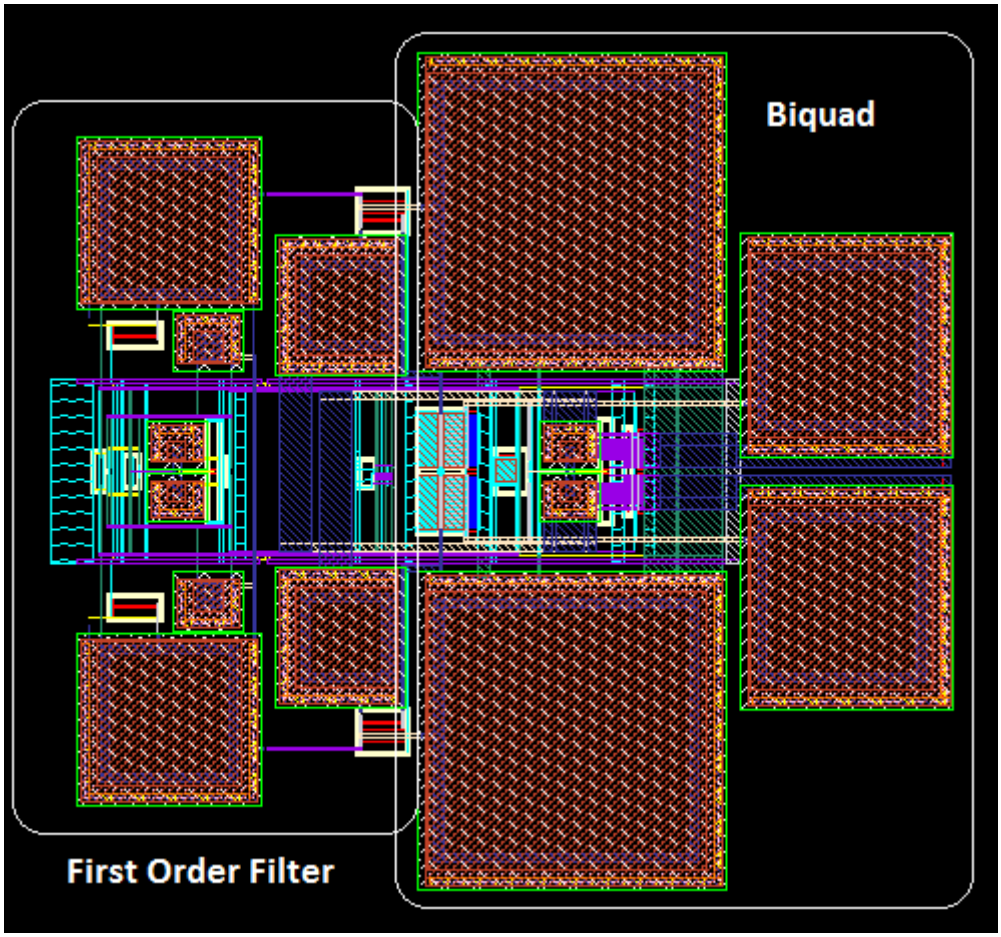

Figure 5.19: Layout of the 3^{rd} Order Butterworth filter

Filter Magnitude Response : The magnitude response of the filter is shown in the Figure 5.20.

The results obtained are in the table 5.7. The minimum attenuation required by the filter is 44 dB at 50 MHz. The attenuation obtained by the filter is 75.34 dB and the cutoff frequency is 2.17 MHz. Thus the designed filter is meeting the requirement of passing the information till 1 MHz and suppresses the DAC images.

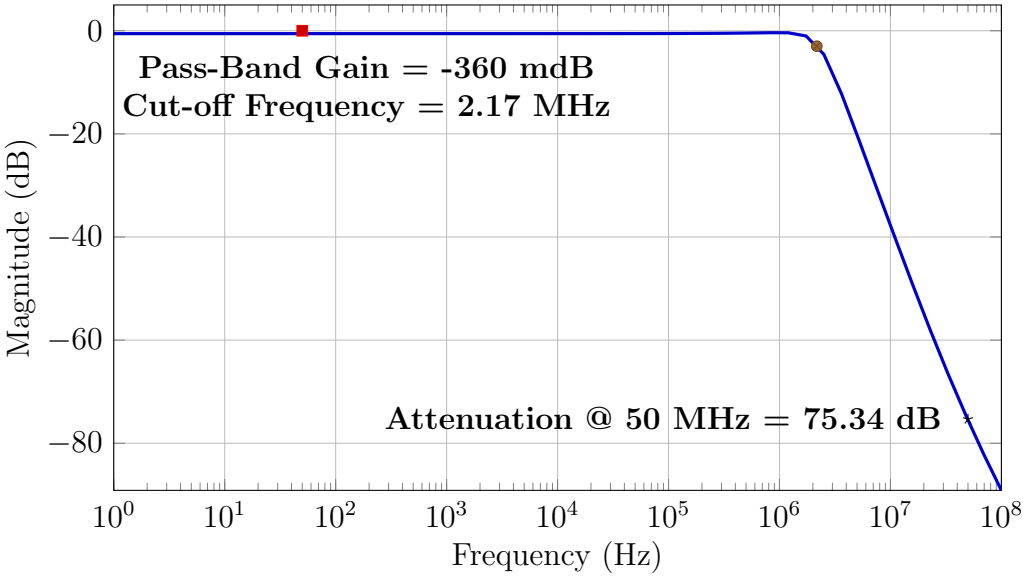

Figure 5.20: Magnitude Response of Base-Band Filter

Table 5.7: 3^{rd} order Butterworth filter Characteristics

Parameter	Value
Pass-Band Gain	-360 mdB
3dB Cut-off frequency	2.17 MHz
Attenuation @ 50 MHz	75.34 dB

Filter Phase Response : All the three Bluetooth modulation schemes have information in phase also. So the filter should not disturb the relative positions of zero crossing points of modulated signal. All the zero crossing points should get equal delay. For this reason, filter should have linear phase. Fig. 5.21, Phase response of the filter is reasonably linear in the 1 MHz signal band.

Filter Output P1dB Compression Point : At power amplifier output P1dB required is 10.3 dBm. The gain of PA and mixer is 11.89 dB and -2 dB respectively. So at the filter output, gain compression should not happen till 0.5 dBm

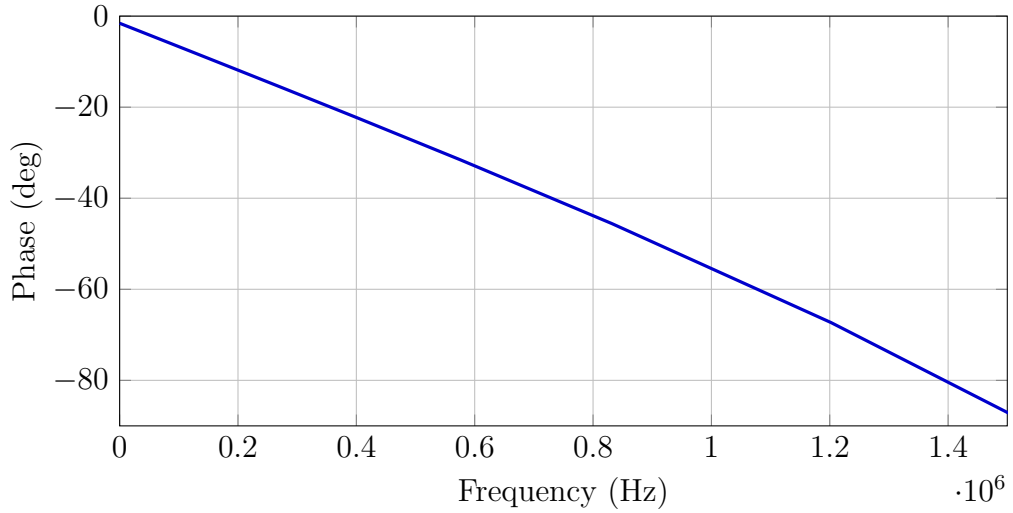

Figure 5.21: Phase Response of Base-band Filter

(10.3-11.89+2). From the Fig. 5.22, it is clear that there is no gain compression till the output power of 0.5 dBm. So it is concluded that active RC filter is very good in terms of linearity. The nonlinearity at the transmitter output is mainly caused by the power amplifier.

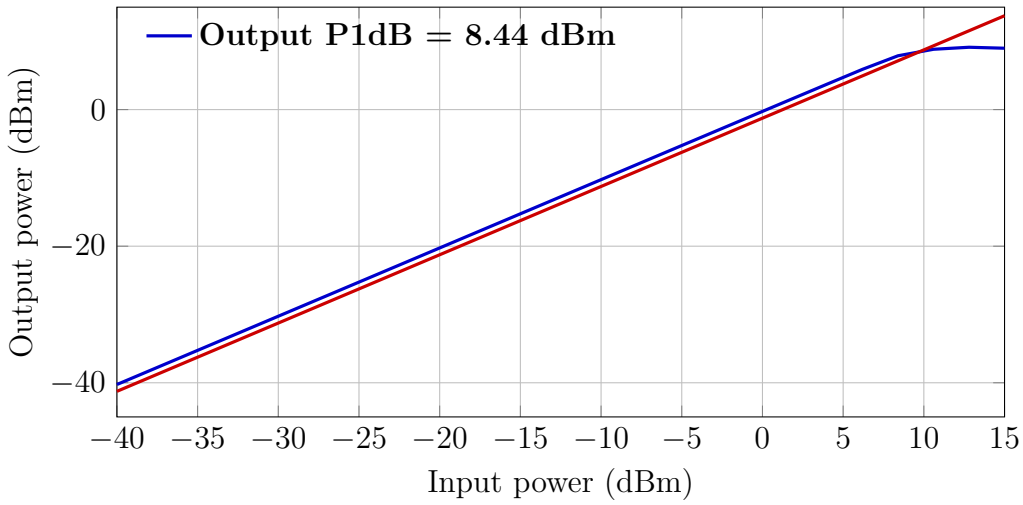

Figure 5.22: Output Compression Curve of Baseband Filter

Chapter 6

System Level Simulation Results and Conclusion

6.1 System Level Post-Layout Simulation Results

6.1.1 Layout of the Transmitter Chain

The layout of the entire transmitter chain is shown in the Figure 6.1. From left to right in the layout, first are the base-band filters for I and Q channels. Then is the mixer with the transformer. Followed by the single-ended PA. The PA's layout is placed such that the inductor used in the PA is as far as possible from the transformer used at the output of the mixer so that the magnetic coupling between the two is as less as possible. The total area consumed is 950 μm x 500 μm. The post-layout simulations after extracting the parasitics of the layout shown in 6.1 are mentioned below:

6.1.2 Transmitter Chain - Voltage Gain

For the entire transmitter, the voltage gain plot is shown in the Figure 6.2.

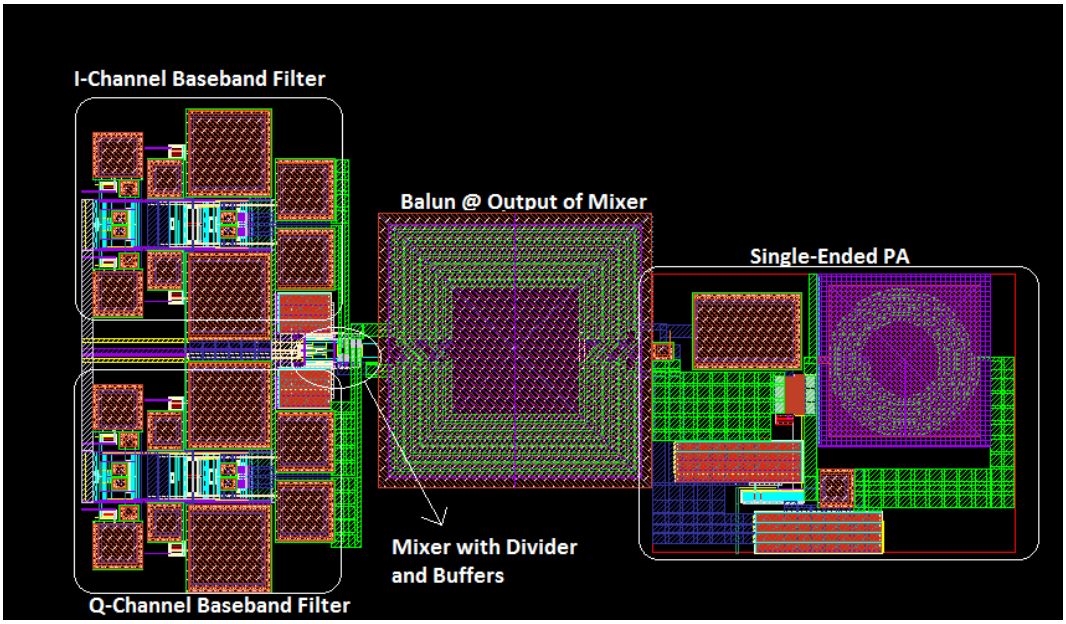

Figure 6.1: Layout of the Entire Transmitter Chain

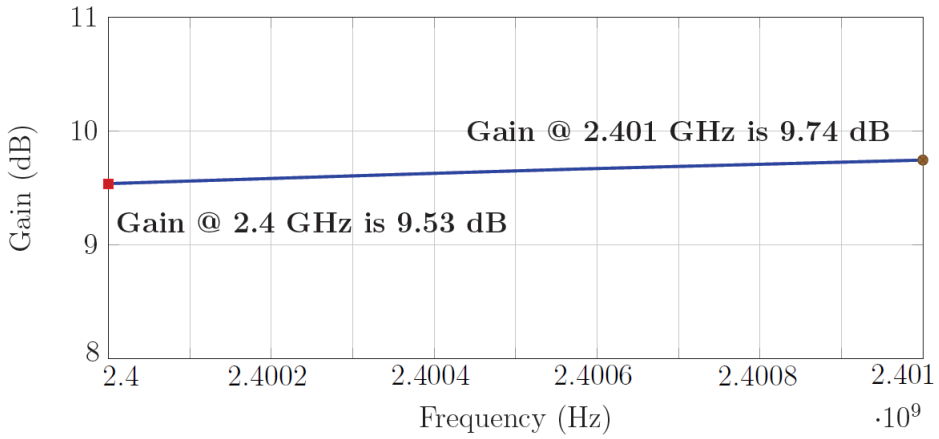

Figure 6.2: Transmitter Chain - Voltage Conversion Gain

Voltage gain of PA is 11.89 dB, Conversion gain of mixer is -2 dB and the pass-band gain of the base-band filter is -360 mdB. The X-axis in the Figure 6.2 is frequency varying from 2.4 GHz to 2.401 GHz.

6.1.3 Output Referred P1dB Compression Point

As explained in the section 3.2.1.2 the specification is that the output referred P1dB compression point should be greater than 10.3 dBm. The post-layout simulation result for the output compression of the transmitter is shown in Figure 6.3. So the specification is met.

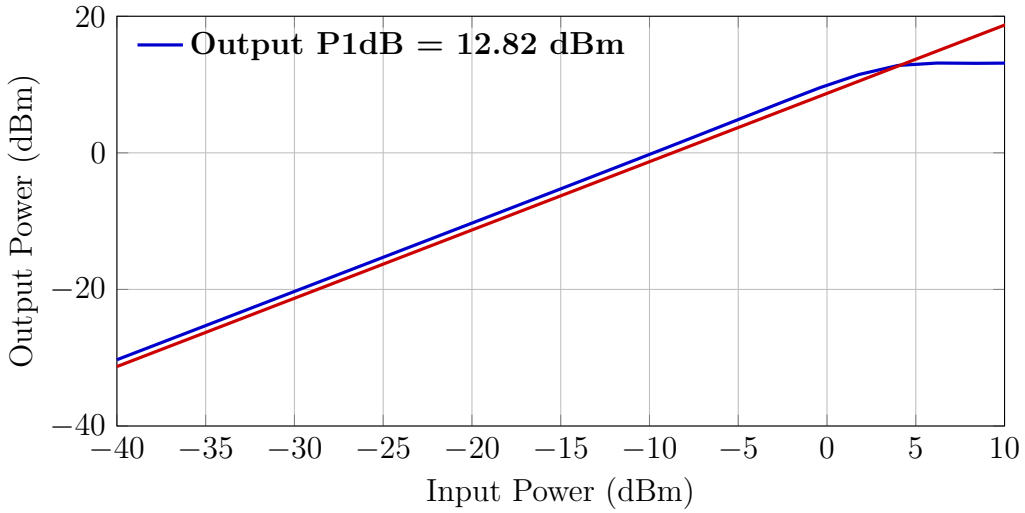

Figure 6.3: Transmitter Chain - Output Compression Curve

6.1.4 AM/PM Conversion

In the official document for Bluetooth, there is no specification mentioned for the AM/PM conversion. Here it is mentioned as this is used as a metric to model the non-linearity and the ACPR depends on the AM/PM conversion. The maximum phase change occurs for that input power at which maximum output power of 4 dBm is obtained. For this the output power is plotted against the input power in Figure 6.4. As in the Figure 6.4 the input power required for a maximum output power of 4 dBm is -5.85 dBm. The output phase is plotted against the input power in the Figure 6.5. The phase of the output voltage at low input power levels is

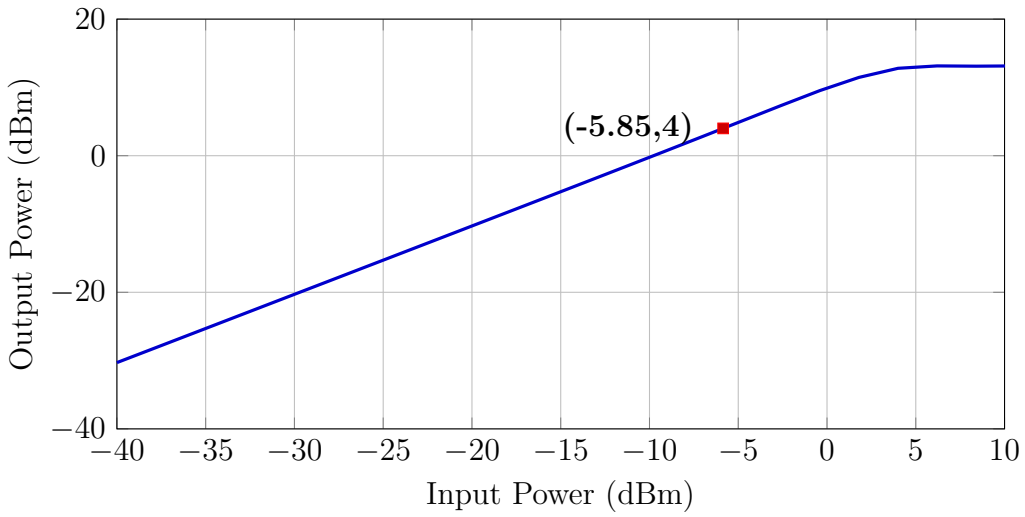

Figure 6.4: Transmitter Chain - Output Power vs Input Power

-148.914°. The phase at -5.85 dBm is -148.849°. So the maximum change in output phase is 0.065°.

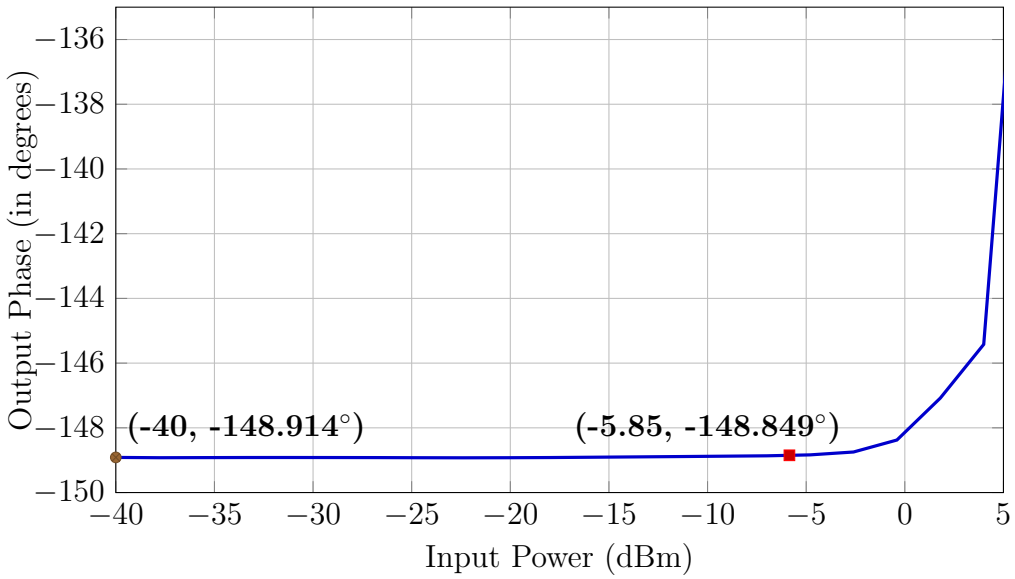

Figure 6.5: Transmitter Chain - AM/PM Conversion

6.1.5 Adjacent Channel Power Ratio (ACPR)

The class A single-ended PA, double balanced voltage mode upconversion passive mixer and the 3^{rd} order low pass Butterworth filter are cascaded for transmitter chain of Bluetooth. ACPR of the entire transmitter is found to be 40.1 dBc, whereas the required ACPR value is 26 dBc. So the ACPR specification is met with good margin. ACPR plot of entire transmitter is shown in Fig. 6.6.

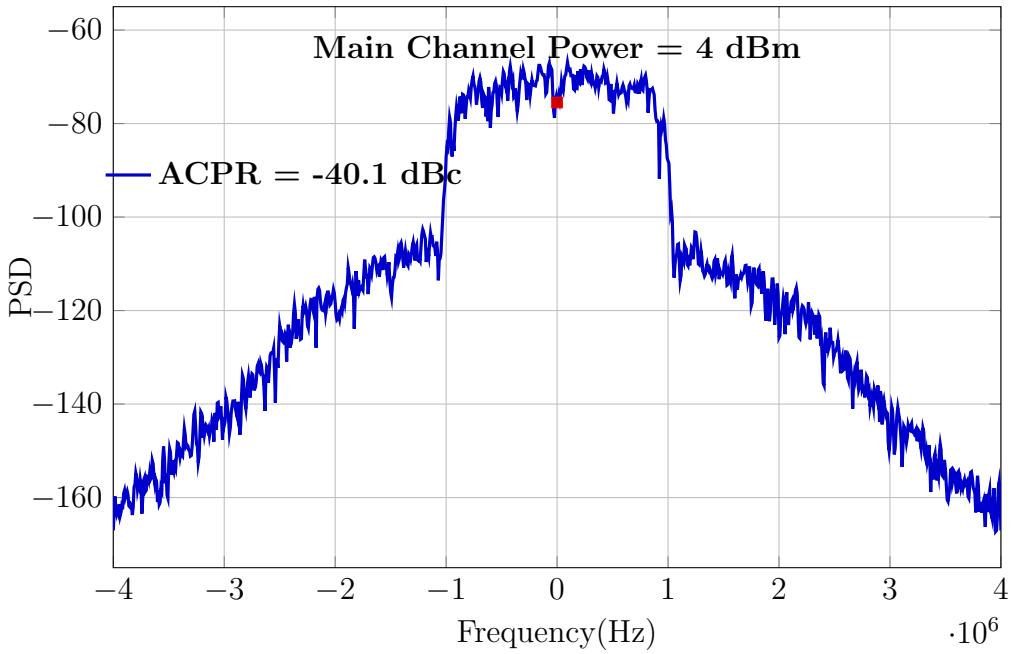

Figure 6.6: Transmitter Chain - ACPR

6.1.6 Phase noise at transmitter output

Generally in transmitters, linearity is the important concern than noise, because the signals coming from DAC itself are several hundreds of millivolts. But noise of transmitter is also an important concern for FDD systems because of the limited isolation provided by the duplexer filter. In FDD systems, transmitter and receiver are working at same time with a frequency offset. The transmitter output noise

should not rise the noise floor of receiver. That's why FDD transmitters have an important output phase noise specification. In TDD systems, transmitter and receiver are not working at same time. A RF switch connects any one of the transmitter and the receiver to antenna. So the output noise of TDD transmitter doesn't effect on noise floor of its corresponding receiver. But it is not supposed to desensitize some other user's receiver. So generally the noise specification for TDD transmitters is much more relaxed than compared to that of FDD transmitters.

Bluetooth is a TDD system. There is no specification mentioned for output phase noise of transmitter in Bluetooth official document. But for completeness sake, the transmitter output noise is measured at offsets of 1 MHz and 20 MHz. The phase noise plot is shown in Fig. 6.7. As the VCO is not implemented for this design, the phase noise is measured with ideal LO source.

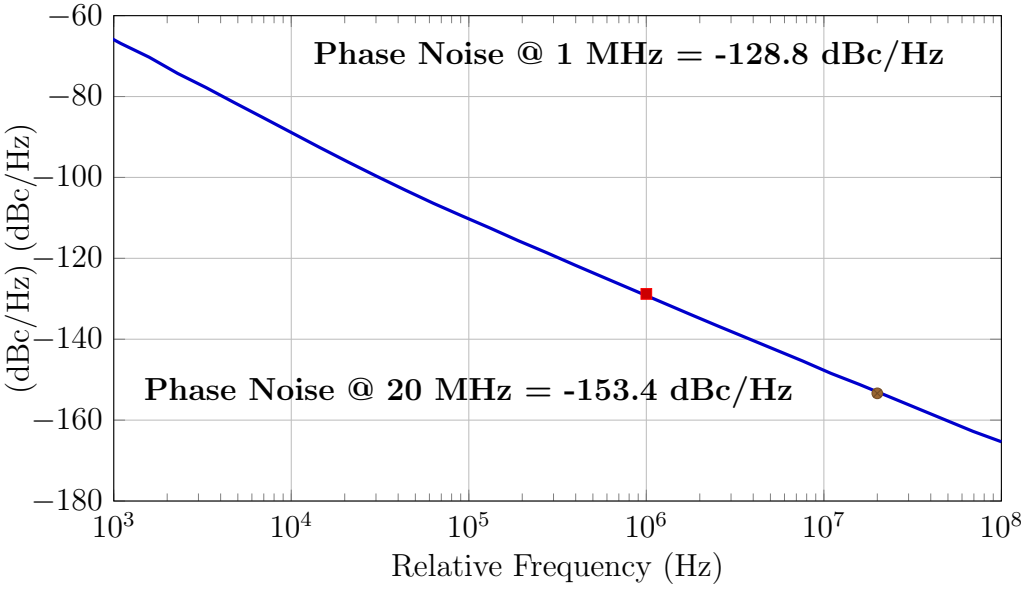

Figure 6.7: Transmitter Chain - Output Phase Noise

6.1.7 Corner simulations

The important results of entire transmitter is simulated across all corners. Five process corners (tt, ss, ff, snfp, fnsp) and three temperature corners (-40°, 27°, 110°,) give a total of 15 corners.

Output P1dB Compression Point : The output P1dB compression point of the entire transmitter chain across the corners is shown in the Figure 6.8. From

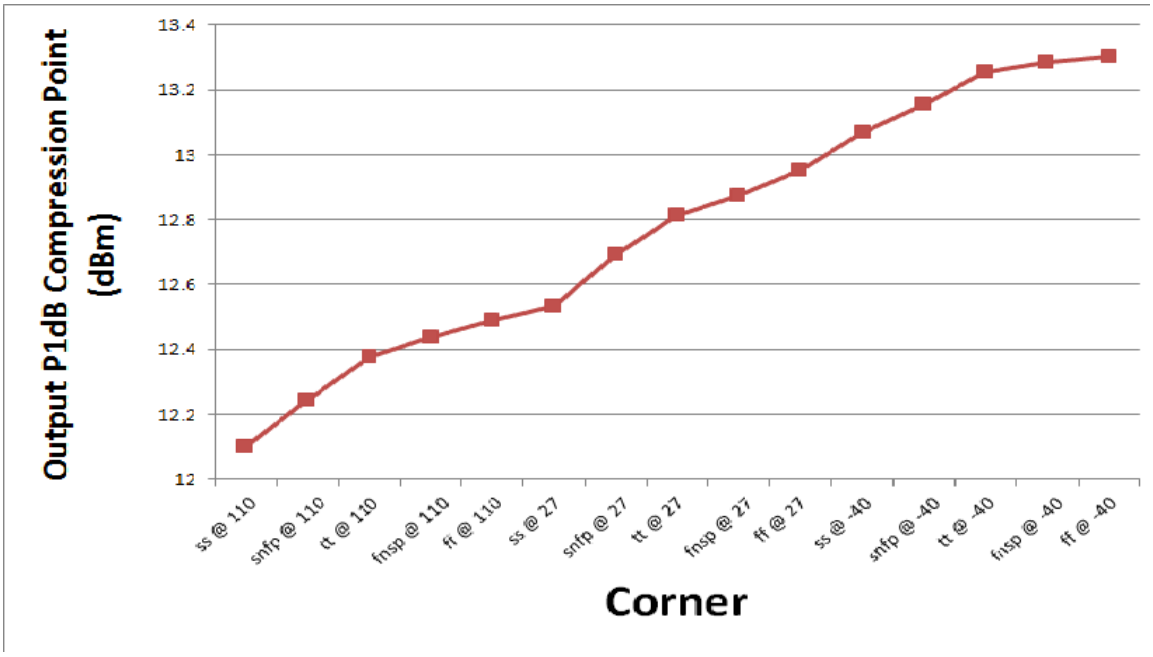

Figure 6.8: Tx Chain : Output P1dB variation across corners

the above figure, the output P1dB compression point is more than 12.1 dBm across all the corners.

ACPR : The ACPR of the entire transmitter chain across the corners is shown in the Figure 6.9. From this figure, the ACPR is more than 37.5 dBc across all the corners.

Tx Chain Gain : The voltage gain of the entire transmitter chain across the corners is shown in the Figure 6.10.

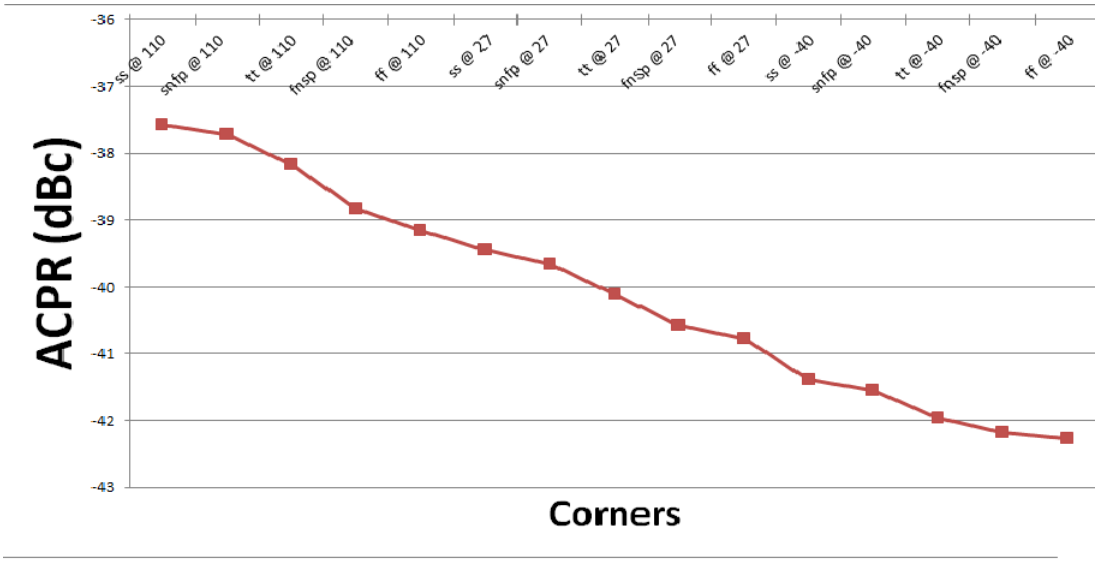

Figure 6.9: Tx Chain : ACPR variation across corners

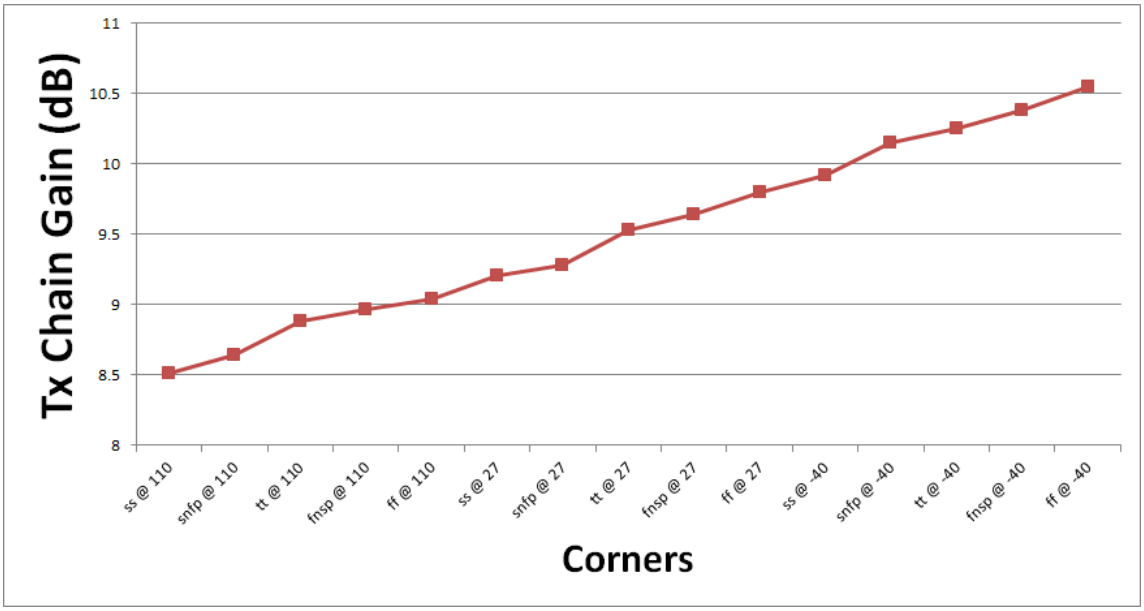

Figure 6.10: Tx Chain : Voltage Gain variation across corners

From this figure, the transmitter chain gain is more than 8.5 dB across all the corners.

DC Power : The amount of DC power consumed by the entire transmitter chain across the corners is shown in the Figure 6.11. From this figure, the maximum DC power consumption of the entire transmitter chain is 26.5 mW across all the corners.

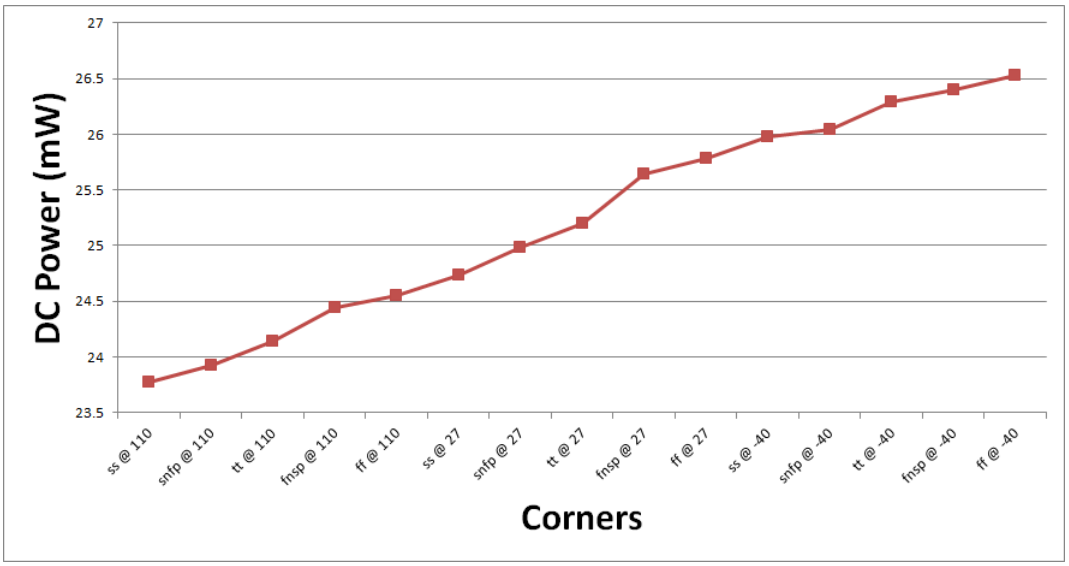

Figure 6.11: Tx Chain : DC Power variation across corners

Other important results of the transmitter chain at nominal conditions is given in Table 6.1. In this table the average current for divider circuit is the average current drawn from the supply by the frequency divide by 2 circuit and the buffers used in this circuit.

6.1.8 Package model parasitics

In this work single-ended PA and baseband filter with upconverter are given separate power supply lines. All the results mentioned above are with 1 nH bond wire

Table 6.1: Other Important Results

Parameter	Value
Power Supply	1.2 V
PA gain	11.89 dB
Mixer gain	-2 dB
Filter gain	-0.36 dB
Total gain	9.5 dB
PA DC current	14 mA
Filter DC current	3.4 mA
Average current for Divider	3.6 mA
Total Average current	21 mA

inductance at supply, ground, and input nets for filter and upconverter. For PA, at supply and at output 1 nH bond wire inductance is used and 400 pH bond wire inductance is used at ground net. As explained in section 3.4.1 the series capacitance of the off-chip matching network at the output, can be tuned for a different value of bond wire inductance on the ground net.

6.2 Conclusion

The transmitter parameters are compared with other published transmitters in Table 6.2. The entries in this table corresponding to this work are the extreme cases obtained across the corners.

Power consumption is optimized by considerable amount. The main reason for power optimization is the use of 1.2 V supply for power amplifier. Other published implementations used higher supply voltage for power amplifier whereas it is the

Table 6.2: Comparison of Performance to published transmitters

Parameter	This Work	[4]	[5]	[6]	[7]
Technology	65 nm	0.18-μm	0.13-μm	0.18-μm	65 nm
Supply (V)	1.2	1.5/2.5	1.2/3.3	1.8/2.5	1.2/3.3
Power Diss. (mW)	26.5	100	89	91	78
ACPR (dBc)	37.5	50	35	36	Not specified
Area (mm^2)	0.475[a]	1.2[a]	3[b]	4[b]	1.5[b]

[a] Area of Transmitter

[b] Area of Transmitter and Receiver

same supply used for entire transmitter here. Also the capacitance at the input of the PA is resonated with the secondary inductance of the transformer used at output of mixer. With this the baseband filter DC current is reduced. The transformer and the inductor occupy considerable area but their usage is inevitable as per the architecture followed.

EVM is another important specification of transmitters like ACPR. The peak EVM of Bluetooth transmitter has to be less than 25% and RMS EVM has to be less than 15%. EVM is not measured for the transmitter here, because of the unavailability of the set up to measure it.

6.2.1 Other possible implementation - balun less transmitter

If single ended power amplifier is implemented with single balanced passive mixer, then balun can be removed from the transmitter [8]. The transmitter then contains only one inductor at the output of PA. Here also circuit level techniques are required to eliminate the effect of package model parasitics.

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