Analog Front End Design and Layout of Bluetooth Receiver

A project Report
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Under the guidance of
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Thesis Certificate

This is to certify that the thesis titled **Analog Front End Design and Layout of Bluetooth Receiver**, submitted by **Santosh Kumar Dasari**, to the Indian Institute of Technology, Madras, for the award of the degree of **Master of Technology**, is a bonafide record of the research work done by him under our supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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Abstract

The project is aimed at designing the Analog front end of a bluetooth receiver. The motivation behind the design is to achieve the most important requirements for a bluetooth receiver namely compactness, high sensitivity, high linearity, low power consumption. A Direct conversion Receiver architecture is chosen to achieve compactness by eliminating need for off chip Image rejection Filter. The front end contains a Broadband noise cancellation low noise amplifier which doesn't use any inductor's thereby saving the area on the chip and making it more compact. The receiver architecture is current mode, which avoids voltage compression at various internal nodes in the circuit and thereby helps in achieving high linearity. The bluetooth receiver designed achieves a Noise figure of 4 dB giving a high sensitivity of -96 dBm and an IIP3 of -10.3 dBm. Power consumption is just 20.4 mW (Vdd =1.2 V), which is very less as compared to bluetooth receivers designed so far.

Abbreviations

DCR	Direct Conversion Receiver
DPSK	Differential Phase Shift Keying
LNA	Low Noise Amplifier
NF	Noise Figure
IRF	Image Rejection Filter
LO	Local Oscillator
PSD	Power Spectral Density
SNR	Signal to Noise Ratio
TCA	TransConductance Amplifier
TIA	TransImpedance Amplifier

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Chapter 1

INTRODUCTION

Bluetooth is a wireless technology standard for exchanging data over short distances (from 5cm to 10m). Bluetooth operates in ISM (Industrial,Scientific,Medicine) frequency band from 2.4 GHz to 2.48 GHz. A total of 79 channels are present, with each channel having a bandwidth of 1 MHz.Accurately, the carrier frequency of the 79 channels can be shown as: (2402 + k)MHz, k= 0.....78. Modulation schemes used for bluetooth are:

- GFSK- It is the Basic date rate modulation scheme, having a date rate of 1Mbps. It is the conventional modulation scheme used.
- 8-DPSK and Π/4 DQPSK with data rate of 3 and 2 Mbps respectively.They constitute the Enhanced data rate modulation schemes.

As stated in the abstract the main metrics of a bluetooth receiver are its compactness (high level of integration on Silicon), low power consumption, high sensitivity and good linearity, in order to have large dynamic range. A small explanation of how these are achieved in design is given in the introduction. Section 1.1 describes the Specifications given in the Bluetoothstandard document version 4.0. In section 1.2 these standard specifications are translated to system level specifications for easy understanding and design at the circuit level. Section 1.3 describes the architecture of the Bluetooth receiver at block level.

1.1 Bluetooth standard document version 4.0 specifications

- **Sensitivity :** The reference sensitivity for a Bluetooth signal shall be better than or equal to -70 dBm at a bit error rate 10^{-3}.
- **Interference performance :** The interference performance is measured with the wanted signal at -67 dBm. The magnitude of the interferer is given in the Table 1.1

Frequency of interference	**Ratio**
Co-Channel	21 dB
Adjacent Channel(1 MHz)	15 dB
Adjacent Channel(2 MHz)	-17 dB
Adjacent Channel(>3 MHz)	-27 dB

Table 1.1: The table shows the position of the interferers and the corresponding ratio of the interferers to the signal (which is at -67dbm)

- **Out of Band Blockers :** The out of band blockers applies to signals outside the band 2400- 2483.5 MHz.In the table 1.2, information on the out of band blockers power levels and their respective band is given:

Frequency of interference	**Interferer power level**
30 MHz - 2000 MHz	-30 dBm
2003 MHz - 2399 MHz	-35 dBm
2484 MHz - 2997 MHz	-35 dBm
3000 MHz - 12.75 GHz	-30 dBm

Table 1.2: The table shows the frequency of interferers and corresponding magnitude of the interferers.

- **Intermodulation Characteristics :** The intermodulation characteristics are checked in the following way:

  1. The wanted signal is kept at 6 dB above the reference sensitivity level, i.e at -64 dBm.It's frequency is f_0.
  2. Static sine wave signal shall be at a frequency f_1 with a power level of -50 dBm.
  3. An interfering signal shall be at a frequency f_2 with a power level of -50 dBm . f_0 is frequency in the band of interest , i.e 2.402 GHz - 2.48 GHz f_1,f_2,f_0 are chosen such that $2 * f_1$ -f_2 = f_0 and $|f_1 - f_2|$=n * 1 MHz, where n can be 3,4 or 5.

- **Maximum usable level :** The maximum usable input power level shall be -20 dBm or better.

1.2 Translating Bluetooth standards to system level specifications

- **Deriving Noise Figure(NF) from Sensitivity :** The sensitivity expected out of a bluetooth receiver is -70 dBm or less. The project aims at a sensitivity of -96 dBm. Sensitivity (S) of any receiver chain is given in 1.1

$$S = -174\,dBm/Hz + NF + 10\log(B.W) + (SNR)_o \tag{1.1}$$

  B.W is the bandwidth of bluetooth signal (1 MHz), NF is the integrated Noise figure of the receiver (from corner frequency to 1 MHz), $(SNR)_o$ is minimum signal to noise ratio required at the output of the receiver. This number is typically 14 dB for bluetooth signal (with GFSK modulation scheme). Therefore, S = -100 + NF, in order to achieve S of -96 dBm or less, NF must be less than or equal to 4 dB.

- **Deriving 1 dB Compression point from out of band interferer level:** As can be seen in Table 1.1 and Table 1.2 the largest blocker is an out of band blocker of magnitude -30 dBm in frequency range 30 MHz to 2000 MHz. In

order to avoid compression due to the blocker the 1 dB compression point of the bluetooth receiver must be more than -30 dBm.

- **Input referred third order intercept point (IIP3) :** The derivation of the required IIP3 is a little complicated. Referring to standard specifications of bluetooth on intermodulation, the input bluetooth signal should be at -64 dBm. From the input signal level, we can find the magnitude of the integrated noise floor, which is -64 - SNR_o= -64 - 14 = -78 dBm.

  In a two tone test to determine the IIP3, two tones (very closely spaced in-band interferers) are applied and their levels are raised until the third order inter-modulation components equals the integrated noise floor. In our case, the closely spaced tones are at frequency f_1 and f_2 which are given as: f_1, f_2, f_0 are chosen such that $2 * f_1$ -f_2 = f_0 and $|f_1 - f_2|$=n * 1 MHz, where n can be 3,4 or 5 (f_o is the frequency of the input bluetooth signal).

$$IIP3 = P_{\text{int}} + \frac{P_{\text{int}} - IM_{\text{int}}}{2} \tag{1.2}$$

P_{int} = Level of interferer is specified in the intermodulation test as -50 dBm.
IM_{in} = integrated noise floor which is -78 dBm.
Therefore, IIP_3 = -36 dBm.

1.3 Block level Architecture of the Bluetooth receiver

The architecture of the analog front end of bluetooth receiver is shown in fig. 1.1

The architecture chosen for bluetooth receiver here is a Direct Conversion Receiver (DCR) architecture. This architecture is chosen for the following reasons:

1. There is no concept of image in DCR, so there is no requirement of an Image rejection filter. Generally, the image rejection filter is placed before the mixer and needs a Q factor of more than 2400(i.e 2.4 GHz/1 MHz) for very high IF receiver and to even high values for low I.F receivers. Such high Q bandpass filters cannot be designed on chip and hence implemented off chip. Hence, non requirement of an Image Reject Filter helps in implementing the entire receiver(RF plus baseband blocks) on chip, hence making the receiver compact.

   In the case of non zero I.F receiver,the LNA has to drive an off chip Image reject filter, where issues of maximum power transfer arise between the on chip

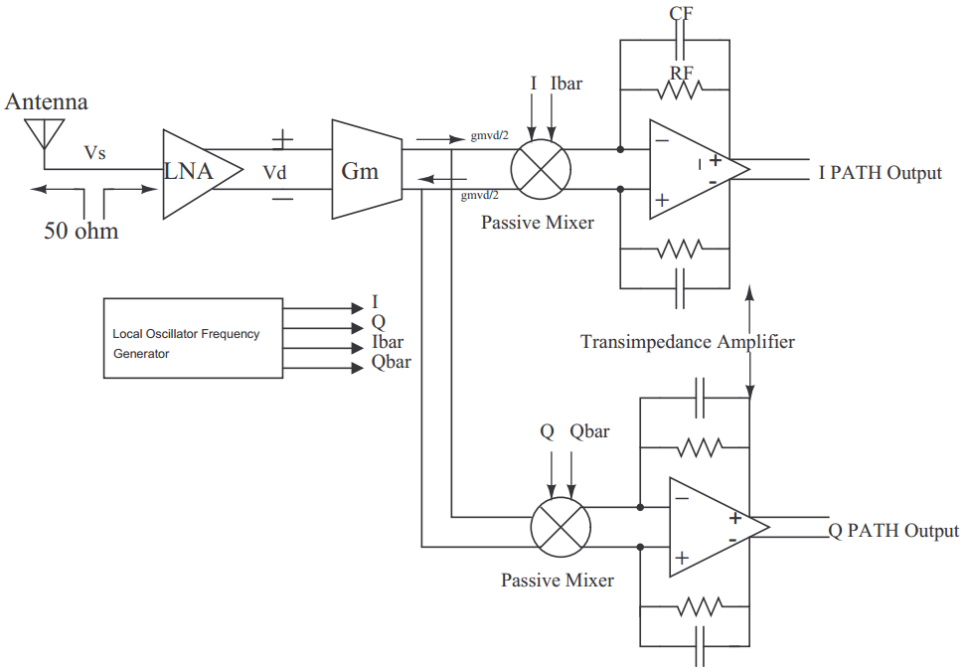

Figure 1.1: Architecture of the Bluetooth receiver

LNA and off chip image reject filter. Image rejection filter has to drive the mixer which should be designed to have an input impedance of 50 ohm for matching. This makes the design of a non-zero I.F complex compared to a DCR architecture.

2. In baseband part of the architecture the channel selection filtering is done by simple low pass filter with cutoff frequency of 2-3 MHz which are easily implemented on chip. Whereas in case of a high I.F receiver, a high Q channel select bandpass filter would be needed, though a high I.F will help in a better image rejection. Similarly a low I.F will make the channel selection filtering easy but it leads to requirement of very high Q Image reject filter.So, there are trade offs in Image reject filtering and Channel select filtering. In DCR we avoid playing with these trade offs as a simple low pass filter is needed for channel select filtering.

If the spectrum of the signal received is anti-symmetric, then direct frequency translation to baseband will lead to self corruption of the signal, hence two paths are chosen for the output namely In-phase path(I- path) and Quadrature-phase path(Q-path). With I path and Q path amplitude and phase can be attained correctly. A current mode architecture is used as it helps us reduce the voltage swings to ideally zero at some of the internal nodes in the receiver. This helps in avoiding compression of signal at the input for some of the blocks, thereby giving a higher 1-dB compression point. A brief qualitative overview on the presence of LNA, transconductor, Mixer and TIA is explained in the following paragraphs.

The signal received by the antenna has to travel a considerable distance on the chip before reaching the LNA, and as the distance which the RF signal has to travel becomes comparable to the wavelength of the signal, we have care about signal reflections at the input of the R.F front end. Low noise amplifier provides impedance matching at the input so that maximum power is transferred from the antenna and the reflections are minimized.

One of the aim of the project is to avoid usage of inductors in the R.F front end. So, a broadband LNA is chosen. But as compared to conventional LNA designs which consist of cascode Common Source LNA, the broadband LNA doesn't have a tuned input, and can't reject a lot of out of band noise(S/N noise ratio is enhanced by passive signal amplification at the input in Common source cascode LNA's)which

intuitively leads to higher noise figure contribution by LNA. So, a technique known as Noise cancellation is implemented which helps in achieving a low Noise figure contribution from LNA at the cost of little higher current consumption. The LNA can be modified to have variable gain step of 6 dB to achieve a higher dynamic range. Detailed design of variable gain LNA is explained in Chapter 2.

As the LNA is pseudo differential its output impedance in each output path is different, hence the output R.F currents from LNA can't be fed directly to a current mode passive mixer. So, a fully differential transconductor is used to feed equal signal currents to the current mode passive mixer. The current mode passive mixer translates the incoming R.F signal to the baseband signal. As the R.F currents from the transconductor are differential a fully differential passive mixer is chosen. Also the mixer chosen is of 25% duty cycle in order to avoid I-Q crosstalk. It will be discussed in detail in chapter 4 that a 25% has a better noise performance as compared to a 50% duty cycle mixer. The switches in the mixer are sized in such a way that the mixer contributes low noise and high linearity to the receiver. A detailed noise analysis of a current mode passive mixer is discussed in chapter 4.

The down converted currents are converted to differential output voltages using a transimpedance amplifier(TIA). As bluetooth signal has frequency component at dc the TIA is dc coupled to the mixer. Because the TIA is dc coupled to the mixer, flicker noise of input transistors in the TIA becomes important in it's design. This leads to sizing the input transistors in the TIA in a way to minimize the flicker noise, otherwise the flicker noise may completely drown out the signal near dc to few hundred kilohertz. TIA is also designed for the receiver to have a high dynamic range, as the input baseband currents are converted to the voltages at the output stage of the two-stage op-amp. Hence, if we ensure a high 1-db compression point of the output stage the linearity of the receiver can be improved.

Also ideally a TIA has zero input impedance due to which there are zero input voltage swings at it's input, hence there is no compression caused to the input differential pair in TIA. This enhances the overall linearity of the receiver chain. A simple first order low pass filter is implemented with the TIA to have a cut-off frequency of 2.5 MHz to pass the bluetooth signal of bandwidth 1 MHz.

Chapter 2

Low Noise Amplifier (LNA)

The LNA chosen for the receiver is a broadband LNA to avoid usage of inductors in the design (i.e one with tuned input and output). The circuit diagram of the noise cancellation LNA is shown in fig 2.1

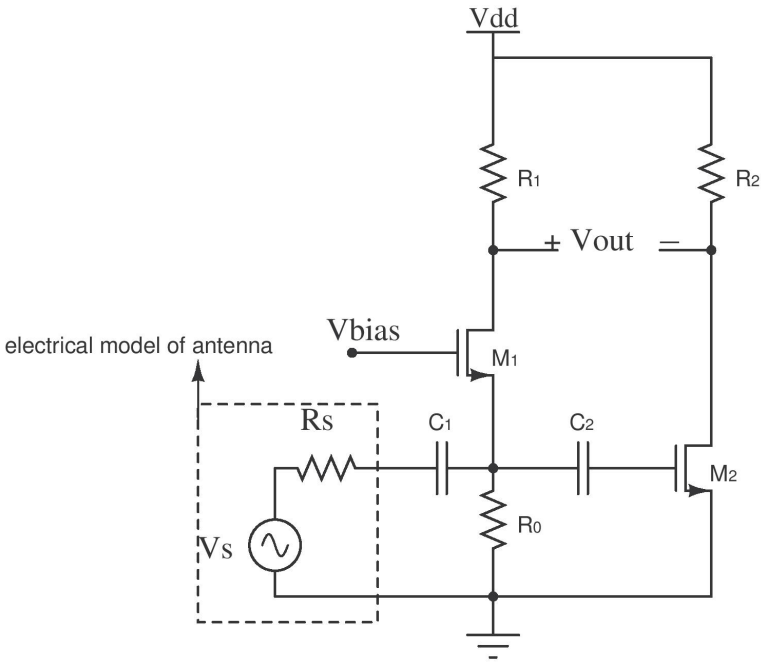

Figure 2.1: Low noise amplifier

The following are the key design aspects of an LNA:

2.1 Input Return Loss

The signal received by the antenna has to travel considerable distance on the PCB before reaching the receiver front end, which may result in voltage reflections and thereby attenuating the input signal. If the antenna is terminated in a 50 ohm load then the reflections can be minimized, just similar to terminating a transmission line (let's say of characteristic impedance of 50 Ω) to a 50 Ω load to make reflections zero. Hence input impedance matching is of prime concern in design of LNA. The quality of the input match is expressed by the "input return loss" (Γ) defined as ratio of reflected power to incident power with the output of LNA matched to 50 ohm. Γ is given as:

$$\Gamma = \frac{(Z_{in} - R_s)^2}{(Z_{in} + R_s)^2} \tag{2.1}$$

where Z_{in} is the input impedance of the LNA and R_s is the source impedance, in this case antenna's source impedance is 50 Ω. The input impedance matching is explained with help of figure 2.2

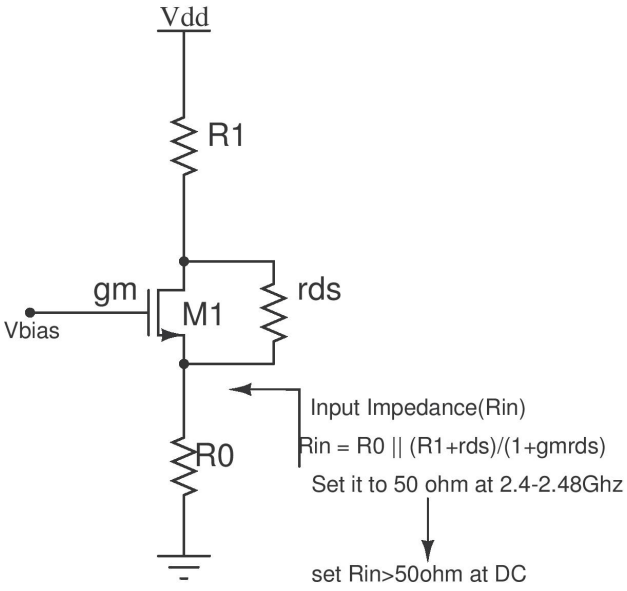

Figure 2.2: Low noise amplifier

The LNA is designed with minimum channel length of 60 nm in order to preserve nodal bandwidths to at least equal to signal frequency (i.e 2.4 - 2.48 GHz). The common gate (CG) and common source (CS) transistors M1 and M2 respectively in figure 2.1 are biased at a current density of 12.5 μA/μm which gives a maximum dc gain of 10 and f_t of 30 GHz. The importance of biasing the transistor at high dc gain is described in the design aspect of "Noise figure" in this chapter. The input and output nodal bandwidths of the LNA are about 4 GHz, i.e., little higher than the frequency of operation (2.4-2.48 GHz). Had the channel lengths been higher we could have lost out on nodal bandwidths in the LNA because the nodal capacitors would be quadrupled in order to keep the same G_m.

The input matching is done by the Common Gate structure of the LNA in fig 2.1. As the channel length chosen is 60 nm channel length modulation effect also plays a role in determining the input impedance of the LNA. The input impedance R_{in} of the circuit in fig . 2.2 at D.C is given as:

$$R_{in} = \frac{(R_1 + r_{ds})}{(1 + g_m r_{ds})} || R_0 \tag{2.2}$$

A maximum d.c gain ($g_m r_{ds}$) is chosen according to the below plot of dc gain versus current density (I/W) for a 60 nm channel length transistor set for V_{ds} = 600 mV.

Choice of g_m: It looks from the formula of R_in that g_m can be chosen in a way to minimize the current consumption in common gate part of LNA. But, the input referred noise of R_1 is inversely proportional to the square of g_m hence g_m can't be made arbitrarily small to reduce current consumption.

How to choose g_m**?** Looking at the long channel counterpart of figure 2.2, the input impedance is simply $\frac{1}{g_m}$. To have R_{in} of 50 Ω,g_m is set to 20 mS. Taking this as hint, the g_m of M_1 is chosen to be 20 mS.

M_1 is biased at a Vd_{sat} of approximately 75 mV to maximize IIP_3. So the current required in M_1 can be calculated from : $g_m = \frac{I_d}{Vd_{sat}}$ (g_m for a short channel transistor) which comes out to be 1.5 mA. R_1 and R_0 is chosen as 410 Ω and 300 Ω in order to minimize their noise figure contribution and also in such a way, that a current consumption of 1.5 mA gives a V_{ds} of at least 200 mV for M_1. Hence from equation 1, R_{in} is 85 Ω at DC. R_{in} is purposefully kept higher at DC to get the required(with some additional room of 10 Ω for to burn more current in M_2 to lower it's noise

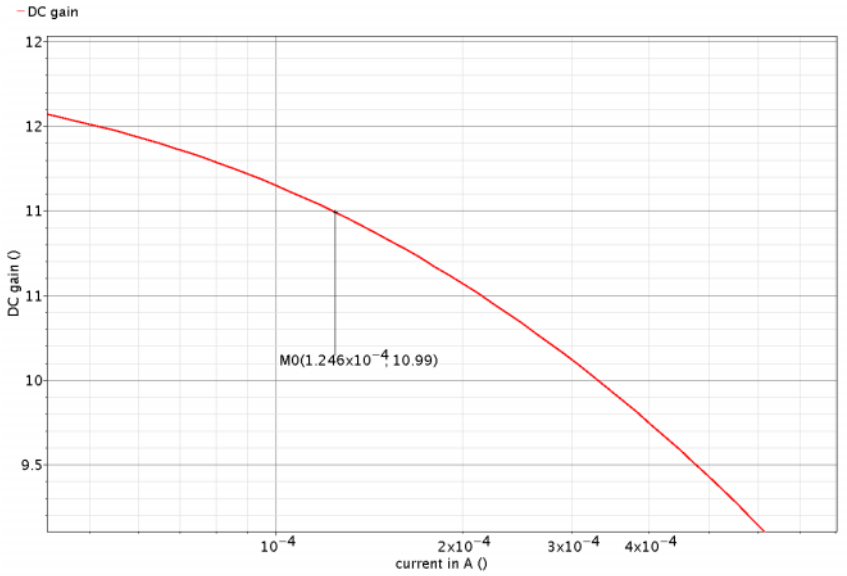

Figure 2.3: DC gain versus current plot in a 10u/60nm transistor

figure contribution) 50 Ω input impedance at the frequency band of interest (2.4 - 2.48 GHz).

The plots for input impedance and S_{11} (input reflection coefficient) can be seen below respectively:

2.2 Noise Figure

The LNA chosen is a broadband LNA, i.e without any tuned input and output. So, we are using noise cancellation technique by which the drain thermal noise of common gate transistor M_1 is canceled. Then the components that contribute to the noise figure are M_2, R_1,R_2. The design of these components to minimize the overall noise figure of LNA is discussed in detail.

Noise cancellation of M_1 is explained with the help of figure 2.6

The aim is to identify two nodes in the circuit (node A and B) where the drain thermal noise of M_1 appears in the same polarity and the the signal V_s appears with opposite polarity, so that when a differential output is taken across these two nodes, then noise of M_1 is canceled and signal is added.

The figure shows only the signal picture, biasing details of the transistors is not

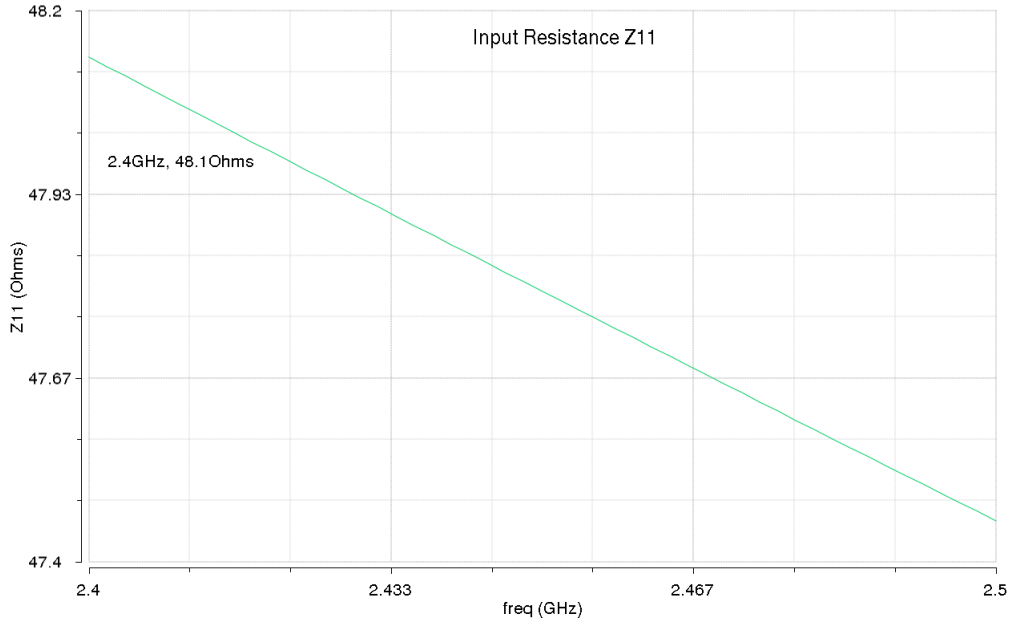

Figure 2.4: Input impedance of LNA matched to 50 ohm

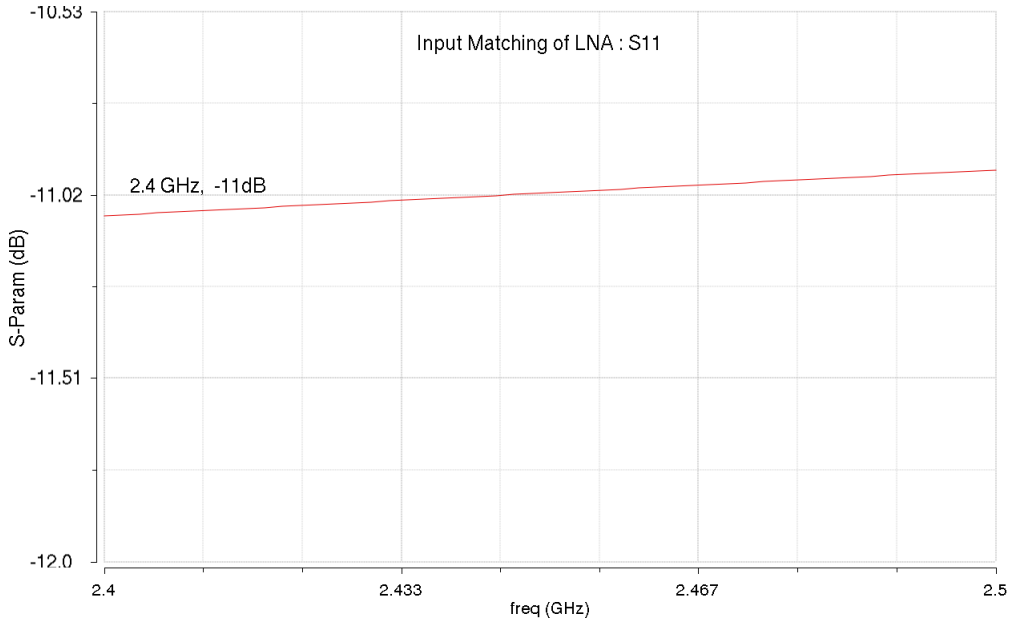

Figure 2.5: Input matching of LNA S_{11}

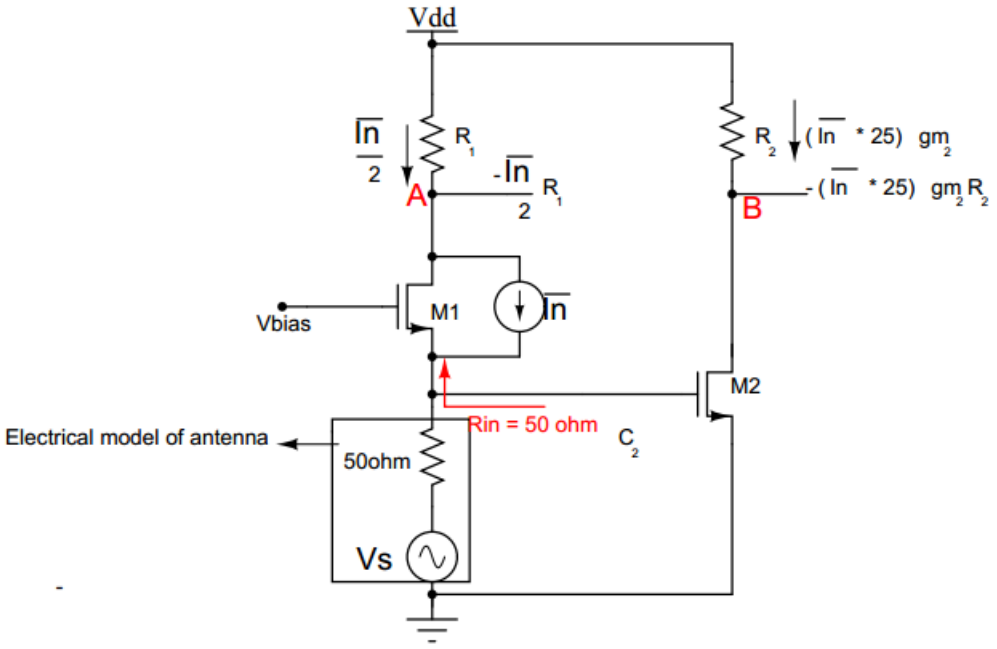

Figure 2.6: Noise cancellation of M_1

shown. Neglecting channel length modulation, the input impedance looking into the source node of M_1 is matched to antenna's 50 Ω impedance. As shown in the figure, the noise of M_1 appears as -$\frac{I_n}{2}$ R_1 on node A and as (I_n * 25) g_{m2} R_2 on node B. If we set $R_1 = 50$ g_{m2} R_2 the drain thermal noise of M_1 is canceled. The result can also be formulated as $R_1 = R_s$ g_{m2} R_2 as R_s is the antenna's resistance of 50 Ω, but $g_{m1} = \frac{1}{R_s}$. Hence, if gains of the two sides that is the Common Gate side (g_{m1} R_1) and Common source side(g_{m2} R_2) are equal then the noise of M_1 is canceled. As the output is differential the gains in both the paths i.e., CG and CS should be same, this helps in canceling the noise from M_1. Hence, our aim is to make the gains of the CG side and CS side in figure 2.1 as exact as possible to cancel the noise of M_1. After canceling the noise of M_1 the noisy components are R_0,R_1,M_2 and R_2.

How to decide a value for the biasing resistor R_0 to minimize it's noise contribution? Let the thermal noise current power spectral density(PSD) of R_0 be ${I_{R0}}^2$. The contribution of noise of R_0 to the NF of the LNA is given as $\frac{Rs}{R_0}$. Therefore, R_0 is selected large as compared to R_s(antenna source resistance 50 ohm). The upper

limit of R_0 is fixed by the voltage headroom assigned to it. The voltage headroom assigned to it is around 400 mV. The voltage headroom is so assigned because, we need a larger headroom for R_1 as it is the dominant noise contributor in the LNA and it has to be made larger for reducing it's noise contribution. In our design R_0 is fixed to a value of 300 ohm.Thus R_0 contributes only 16 % to the NF of the LNA.

How to decide a value for the biasing resistor R_1 to minimize it's noise contribution? The contribution of R_1 to the NF of the LNA is $\frac{1}{g_{m1}R_1}$. For a fixed g_{m1} of 20 mS, only way to reduce the noise of R_1 is to keep it to a value of $\frac{600mV}{1.4mA}$= 428 Ω. So, R_0 is set to a value around 420 Ω.

How to bias M_2 to minimize it's noise contribution? The V_{dsat} of M_2 is fixed to a value of 75 mV to maximize it's IIP_3. It's contribution to the NF of the LNA is given as:$\frac{4kT\gamma}{g_{m2}}$. Hence, only way to minimize the Noise figure contribution of M_2 , is to increase g_{m2} which means we have to burn more current in CS side of the LNA. A current consumption of up to 6 mA is allowed on the CS side.Therefore, the g_{m2} of M_2 is given as $\frac{6mA}{75mV}$ = 80 mS. The gain on the CG side is fixed to 4 because of limited headroom of just 200 mV to M_1 and channel length modulation effect. So, R_2 is chosen such that equivalent output resistance of M_1 i.e $\frac{r_{ds2}}{R_2}$ is equal to $\frac{4}{80mS}$ = 50 ohm. Biased at a current density of $12.5uA$/um r_{ds2}=100 Ω, so R_2 is chosen as 100 Ω to have an equivalent output resistance of 50 Ω for M_2.

Contribution of R_2 together noise figure of LNA is given as : $\frac{1}{g_{m2}^2R_2R_s}$= $\frac{1}{4*80mS*50}$, which is only 6.25%.

To show the effect of Noise cancellation two plots for Noise figure are shown. First plot figure 2.7 shows the Noise figure of CG LNA alone, without noise cancellation to be 4.5 dB with contribution of CG transistor M_1 as 41%. The second plot(figure2.8) shows the noise figure of LNA with noise cancellation of M_1. The contribution of M_1 to the NF is just less than 10%. The NF is 2.38 dB.The table 2.2 following the Noise figure plots shows the noise contribution of each component in LNA before and after noise cancellation.

M_1	41	9.35
R_1	16.4	12.14
R_0	6.1	9.9
M_2	X	9.15
R_2	X	1.3
$R_s(antenna)$	35	57.76

2.3 Voltage Gain

The gain of the LNA defines the overall IIP_3 of the bluetooth receiver. This is because the transconductor, mixer and TIA does not undergo much input compression as input impedance of both the blocks is very small, approximately 9 ohm for the switch and 0.6 ohm for the TIA. Let IIP_{3LNA} and IIP_{3TCA} be the IIP_3 of the LNA and the transconductor respectively. Let the gain of LNA be A_{LNA} in dB. Then the IIP_3 of the LNA referred back to the input of LNA is IIP_{3TCA} - A_{LNA}. So, keeping a low gain in the LNA is desirable. The LNA is designed for a gain of 12 dB. It can have a variable gain step of 6 dB, which makes it's gain 6 dB lower when the input

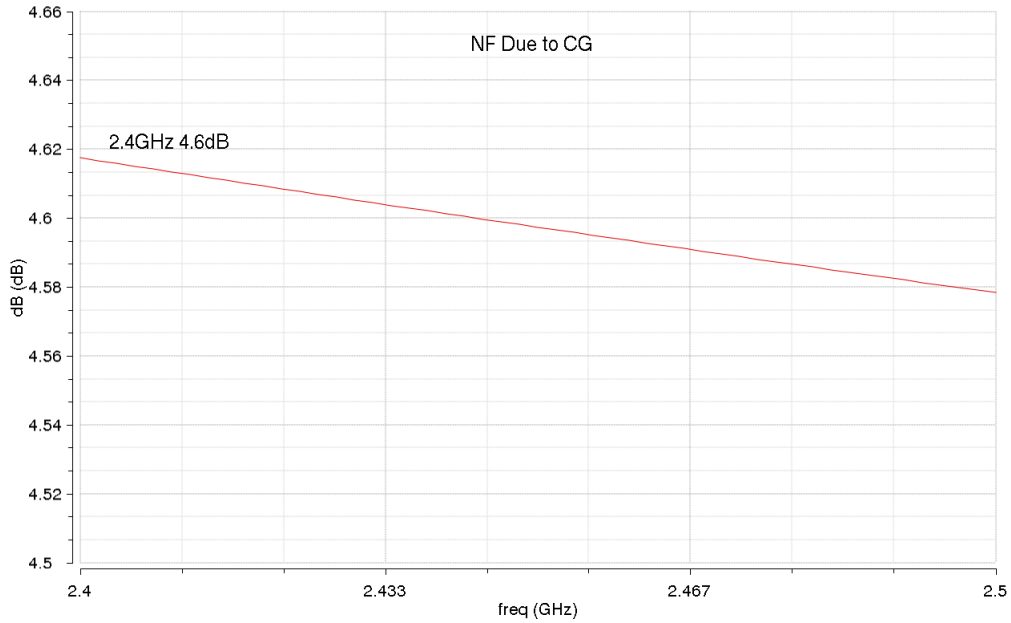

Figure 2.7: Noise figure of LNA without noise cancellation of M_1

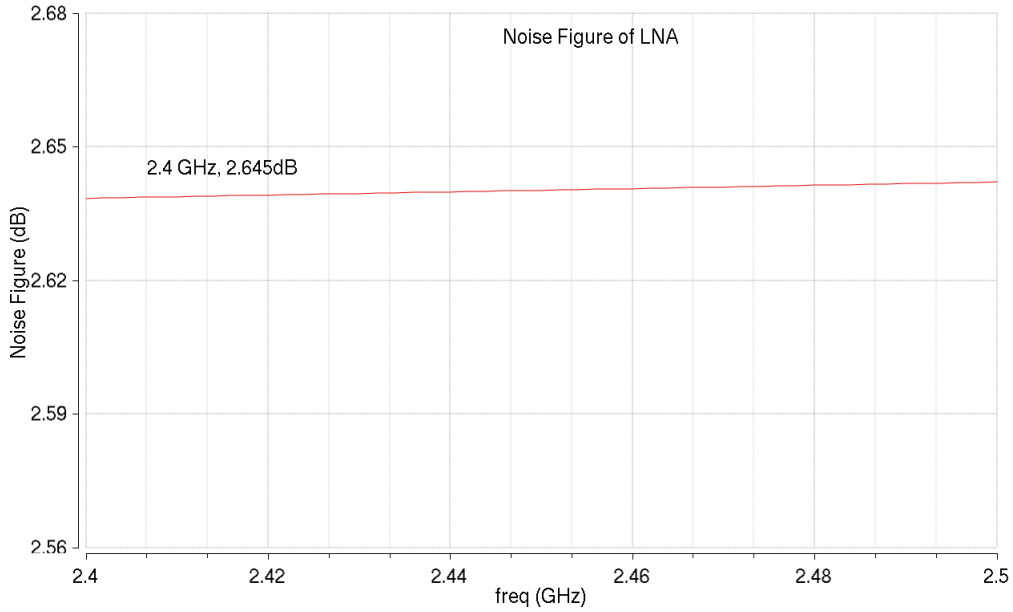

Figure 2.8: Noise figure of LNA with noise cancellation of M_1

signal power is between -77 dBm and -14 dBm.

Derivation of the Voltage Gain for the Noise Cancellation LNA: In figure 2.9, first neglecting the channel length modulation effect for M_1 and M_2, the gain of the Common Gate side can be written as $\frac{V_{op}}{V_{in}} = g_{m1}\ R_1$ and that of the Common source side can be written as $\frac{V_{op}}{V_{in}} = g_{m2}\ R_2$.

So, the overall gain of the circuit is $\frac{V_{op}-V_{in}}{V_{in}} = g_{m1}\ R_1 + g_{m2}\ R_2$. But as the transistors M_1 and M_2 are short channel transistors, the gain is a major function of channel length modulation. The only advantage the choice of short channel length offers is, sufficient bandwidth is available on the input and output nodes in the circuit.

So, for the short channel case voltage gain is found in the following way:
The input impedance of the R_{in} is given as:
$R_{in} = \frac{(R_1+r_{ds1})}{(1+g_{m1}r_{ds1})}||R_0$. The input current $I_{in} = \frac{V_in}{R_{in}}$. The output impedance R_{out1} looking into node A is given as:$R_{out1} = (g_{m1}\ r_{ds1}\ R_0) + R_0 + r_{ds1}$ in parallel with R_1. Therefore voltage at node A is given as $I_{in}\ R_{out2}$ and hence voltage gain for the Common gate section is given as :

$$\frac{V_{op}}{V_{in}} = \frac{R_{out1}}{R_{in}}$$

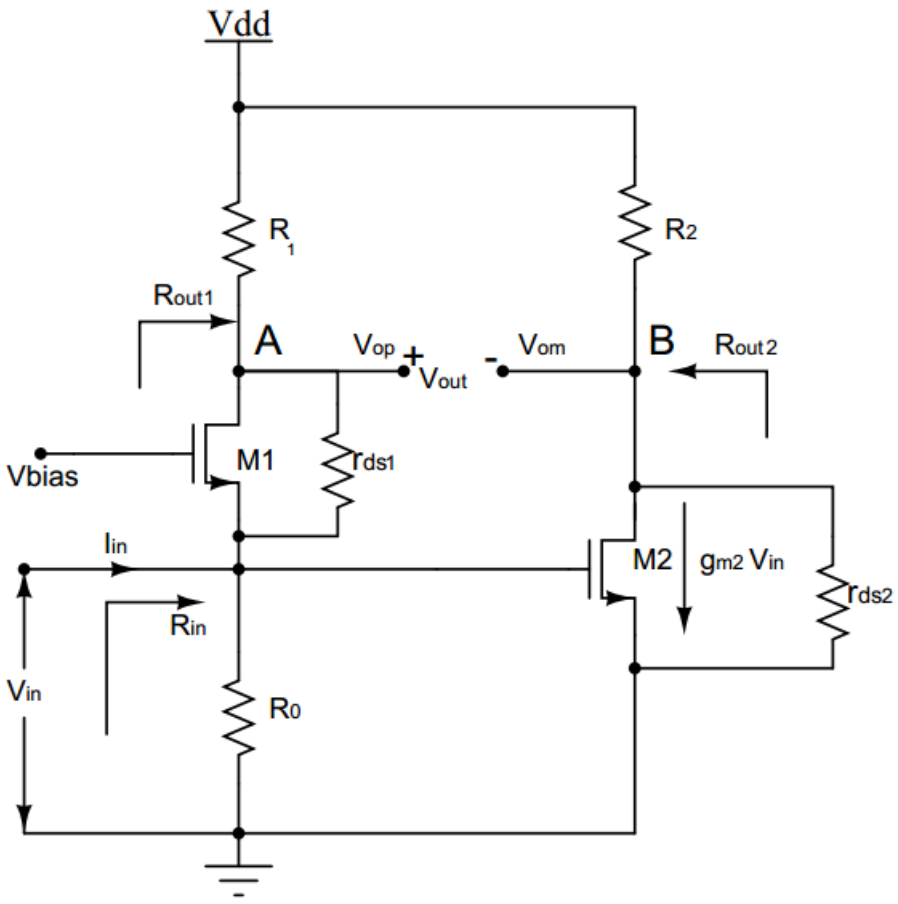

Figure 2.9: Understanding Voltage gain of the LNA

In the design: $(g_{m1}\ r_{ds1}) = 4.37$, r_{ds1}= 228 Ω , R_1 = 424 Ω , R_0 = 300 Ω. R_{out1} = 344.5 Ω and R_{in} = 120 ∥ 300 = 85 Ω. Hence, the gain is $\frac{344.5}{85} = 4$.

The gain of the Common Source side is simply written as :

$g_{m2} * (R_2 \parallel r_{ds2})$ = 80 mS * (100 ∥ 100) = 4. The overall voltage gain $\frac{(V_{op}-V_{om})}{V_{in}}$ for the figure 2.9 is 8, when referred to the antenna input with thevenin resistance of 50 Ω the gain becomes 4 (12 dB). A plot for the voltage gain of LNA (= 12 db) is shown below.

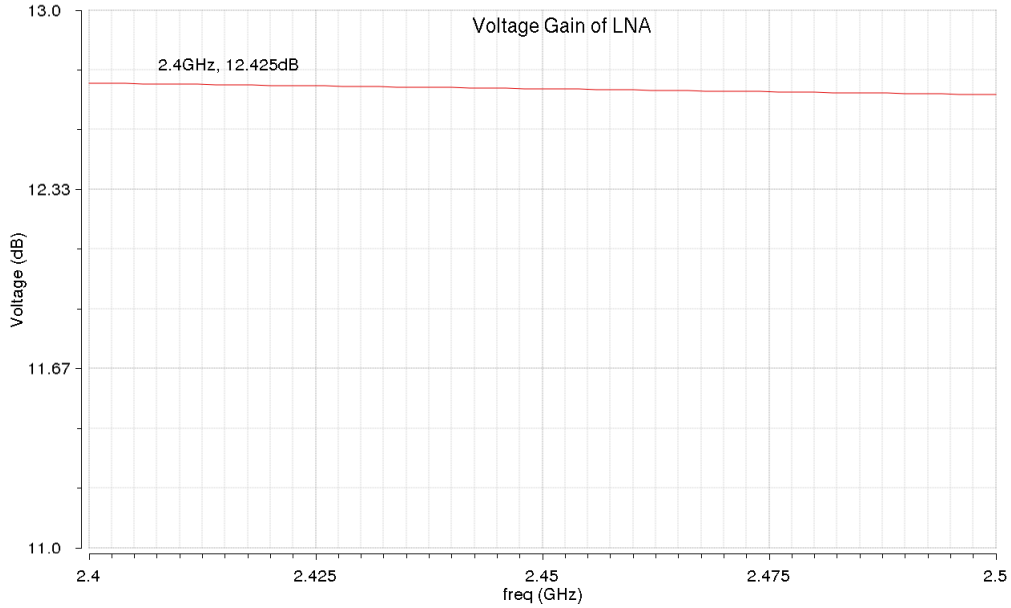

Figure 2.10: Gain for LNA

2.4 Third order Input intercept point(IIP_3)

The drain current of a transistor can be approximated as a weak cubic non linearity in the following way:

$i_{ds} = a_1\ v_{gs} + a_2\ v_{gs}^2 + a_3\ v_{gs}^3$

a_1 is the transconductance (g_m) of the transistor. Within the input dynamic range, it is desired that i_d should only be a function of v_{gs} not it's powers. If two interferers at frequencies f_1 and f_2 appear in the frequency band of operation (2.4-2.48 GHz) in such a way that $|2 * f_2 - f_1| = f_0$, (where f_0 is the frequency of the channel of interest in the band), then with the presence of cubic non linearity these interferes fall on the bluetooth signal of interest at f_0, thus corrupting it. The magnitude of the third order intermodulation components is directly proportional to a_3. Therefore, it is essential that the coefficient a_3 of v_{gs}^3 be minimized at the biasing point of the transistor.

Second order non-linearity arises because of presence of v_{gs}^2 term. Looking at the receiver chain in figure 1.1, we find that if two interferers at f_1 and f_2 undergo second order non - linearity in the LNA and TCA, second order intermodulation components

appear at $f_1 + f_2$, $f_1 - f_2$ is frequency of the order of a few MHz and doesn't makes it's way significantly into the baseband after downconversion, because the transconductor is A.C coupled to the mixer and low frequency components are high pass filtered. The high frequency component is approximately double the frequency of operation and is down converted to around a value of few GHz. Such a high frequency second order intermodulation component is filtered by the channel select low pass filter in the baseband, in this case first order low pass filter shown with the TIA. Hence, less focus is made on minimizing the second order intermodulation components.

How to minimize third order intermodulation components and achieve a good IIP_3 for the LNA and transconductor?

The IIP_3 of a source-degenerated Common Gate transistor is given in volts (peak value) as: $3.26\,V_{dsat}$. Therefore, if we choose a V_{dsat} such that a_1 is maximum at that point and a_3 is minimum then we can ensure, that the magnitude of the IM_3 components will be minimum and the transistor will have the desired linearity between i_d and v_{gs}.

Differentiating the equation w.r.t v_{gs} three times, $i_d s = a_1\ v_{gs} + a_2\ v_{gs}^2 + a_3\ v_{gs}^3$, we get $a_3 = 1/6\ (\frac{d^3 i_{ds}}{dx^3})$ or $\frac{1}{6}$ of the second derivative of g_m.

How to find a_3 by simulation?

We first choose a transistor of channel length 60 nm and bias the drain at V_{dd} such that there is no compression at the drain(due to the transistor going into triode region).Choose an arbitrary Width, let's say 10 um.

Sweep the V_{gs} of the transistor from 0 to V_{dd} and plot the g_m of the transistor. Then, take the second derivative of g_m and divide by 6, which gives us a_3. Select the point where a_3 is minimum and g_m (or a_1) is maximum. In the design of LNA and the transconductor, the channel length of the input transistors is set as 60 nm. The optimum valueof $V_g s$, is selected as 500 mV (giving a V_{dsat} of 75 mV). The below figure shows the maximum and minimum point of g_m and a_3 respectively.

The blue plot is for a_3 and red plot is for g_m. The below figure shows the IIP_3 for the LNA.It is +1.5 dm.

The blue plot is for a_3 and red plot is for g_m.

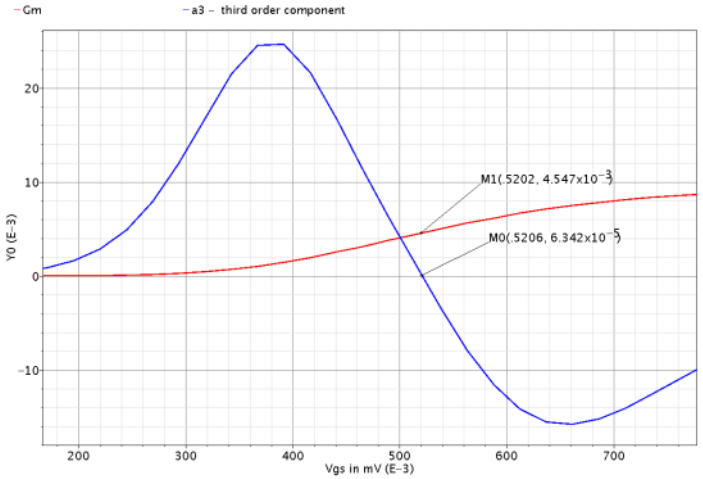

Figure 2.11: Maximising IIP_3 of LNA by careful selection of V_{gs}

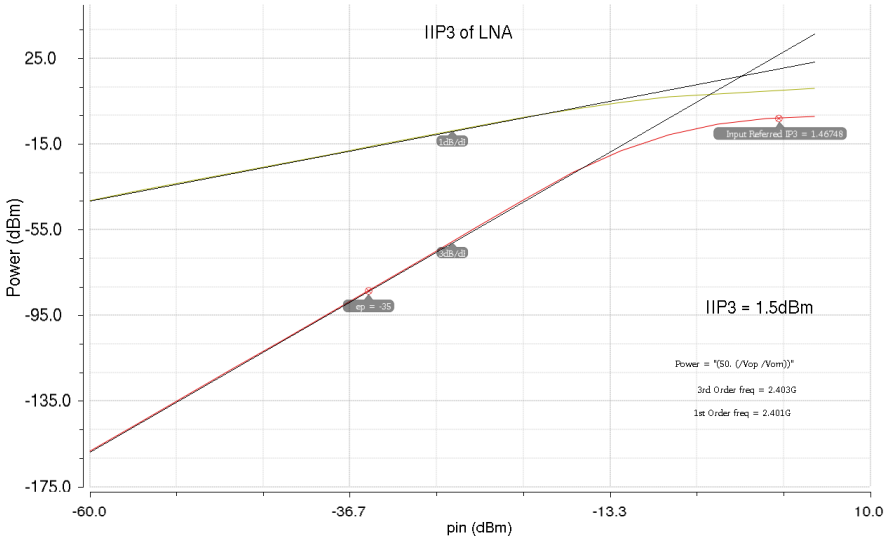

Figure 2.12: IIP_3 for LNA

2.5 Layout of LNA

The layout of the Low Noise Amplifier is shown in the figure 2.13. The layout shown below includes the Common Gate stage, Common Source stage, load resistors, and coupling capacitors which are used to isolate the DC voltages and the biasing circuit for LNA. The capacitors are not completely shown in the figure 2.13. To the left is

the common gate stage and to the right is the common source stage. In the layout, the biasing circuit of this LNA is above CG and CS stages. The area occupied by LNA is 40 um X 20 um.

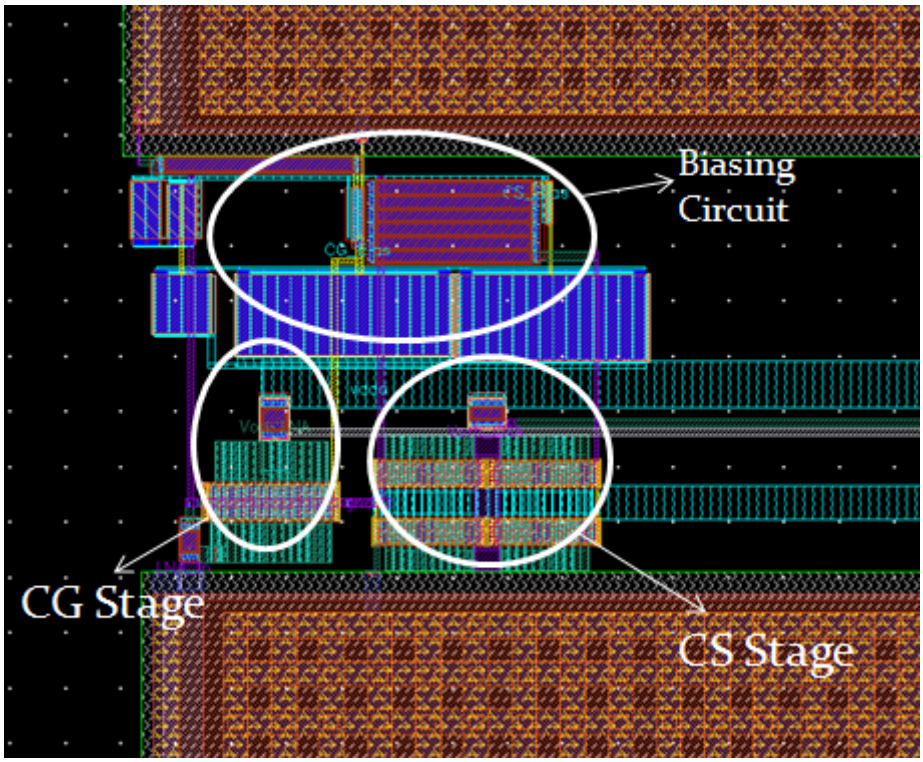

Figure 2.13: Layout of LNA

Chapter 3

Fully differential Transconductor

A simple model of the transconductor highlighting it's G_m and its output impedance at the frequency of operation(2.4 - 2.48 GHz) is shown below:

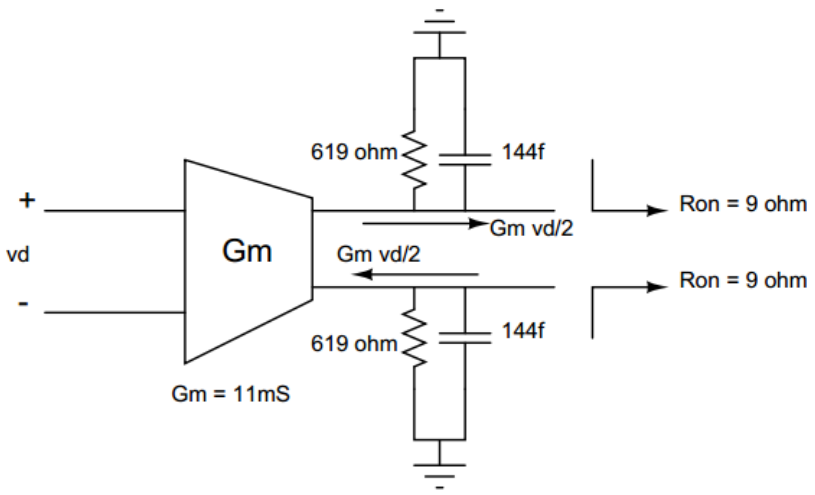

Figure 3.1: Model of a fully differential transconductor

The design aspects of the Transconductor are as follows:

3.1 Noise figure

The figure of the transconductor figure 3.2 is shown below:

The input referred voltage squared noise of the transconductor is given as:

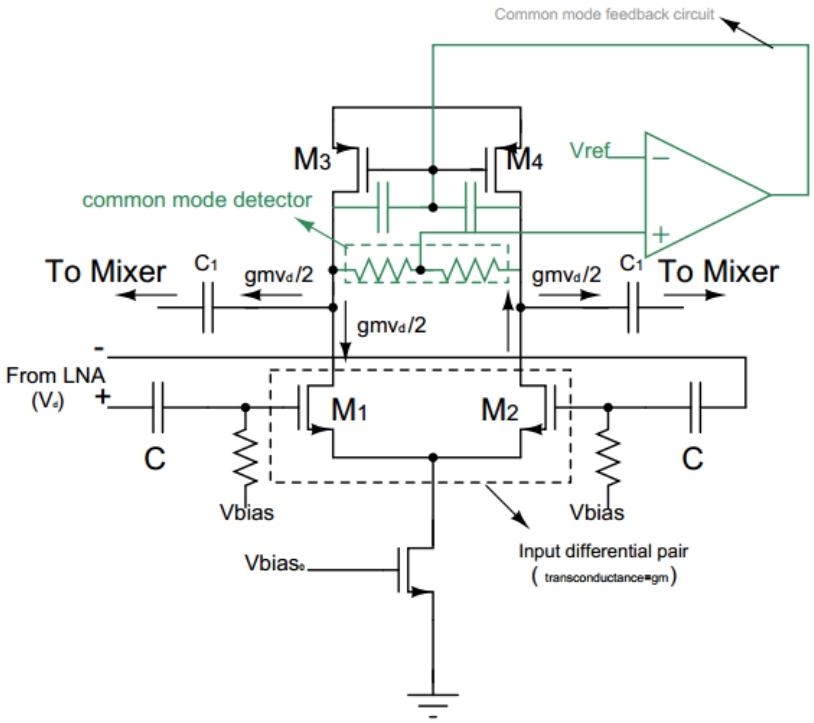

Figure 3.2: Fully Differential transconductor

$$V_{nTCA}^2 = \frac{(8kT\gamma_n)}{g_{m1}} + \frac{(8kT\gamma_p g_{m3})}{g_{m1}^2}$$

Usually g_{m3} is kept at least 4 times less than g_{m1} and M_3 and M_4 are designed with long channel lengths so that γ_p is usually the minimum, i.e $\frac{2}{3}$. So, the noise due to the M_3 and M_4 can be ignored. So, $V_{nTCA}^2 = \frac{(8kT\gamma_n)}{g_{m1}}$. When referred to the input the LNA of gain 4 , the input referred noise due to TCA becomes $\frac{V_{nTCA}^2}{16}$. k = 1.38 * 10^{23} , T = 300 K , excess drain thermal noise factor γ_n for 60 nm length transistor = 1.2.

We have to assign a noise budget to the transconductor, such that it contributes lesser noise as compared to LNA, so that the stages ahead of LNA contributes less to the NF. Let V_{nLNA}^2 be the input referred noise of LNA and let $V_{nR_s}^2$ be the input noise due to the antenna's source resistance R_s of 50 Ω. Below figure shows the total input referred noise of LNA and antenna alone :

From section 2.2, the contribution of the antenna to the input referred noise as

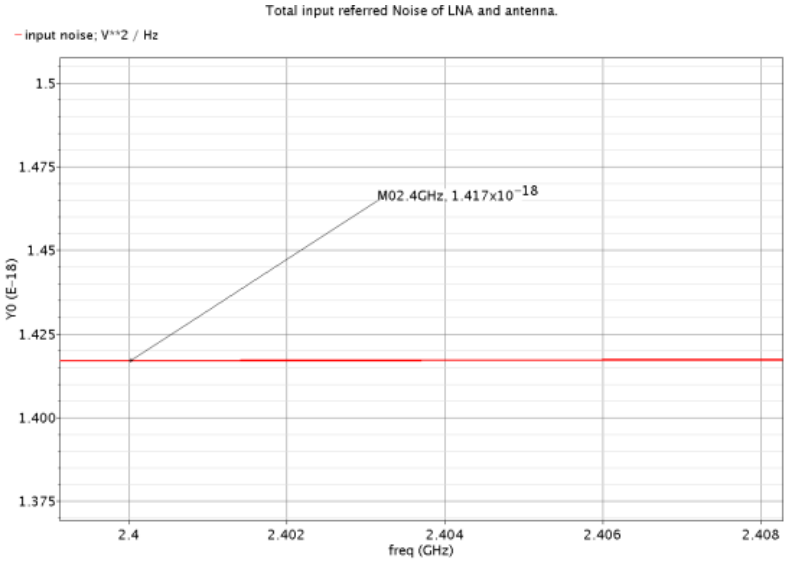

Figure 3.3: Input referred noise voltage PSD of LNA and antenna

shown in figure 3.3 is 57.76 % of which contribution of antenna is $8 * 10^{-19}\ V^2/Hz$.

Therefore,$V^2_{nLNA} = 6 * 10^{-19}\ V^2/Hz$. A noise budget of half the input referred noise of LNA is assigned to the transconductor. Therefore, $V^2_{nTCA} = \frac{(8kT\gamma_n)}{g_{m1}}$ must be less than $3 * 10^{-19}\ V^2/Hz$. Doing the calculations, we get $g_{m1} > 8$ mS. For a fixed V_{dsat} of 75 mV to get a good IIP_3, minimum current consumption of $g_{m1}\ V_{dsat} = 8$ mS * 75 mV = 0.6 mA is required in each transistor(M_1 and M_2). So, minimum total current consumption in the transconductor is 1.2 mA.

In our design we have set g_{m1} as 11 mS and g_{m3} as 3.8 mS. From equation 2 the total input referred noise of transconductor to the LNA input input comes out to be $2.5 * 10^{-19}\ V^2/Hz$, which is less than the assigned budget of $3 * 10^{-19}\ V^2/Hz$. V^2_{nLNA} $= 6 * 10^{-19}\ V^2/Hz\ V^2_{nTCA} = 2.5 * 10^{-19}\ V^2/Hz\ V^2_{nR_s} = 8 * 10^{-19}\ V^2/Hz$

The total input referred noise of the LNA-Transconductor-antenna is $16.5 * 10^{-19}$ V^2/Hz. The same can be also be seen in the below plot of the total input referred noise of LNA-TCA-antenna. Now, the total noise factor of LNA-Transconductor cascade is $(V^2_{nLNA} + V^2_{nTCA} + V^2_{nR_s})\ /(V^2_{nR_s}) = 2.1$, which is 3.34 dB.

Now we understand that, the Mixer and TIA must be designed such that they contribute only 1 dB to the Noise Figure, so that overall Noise Figure will be around 4 dB. The Noise Figure plot of the LNA-Transconductor is shown below:

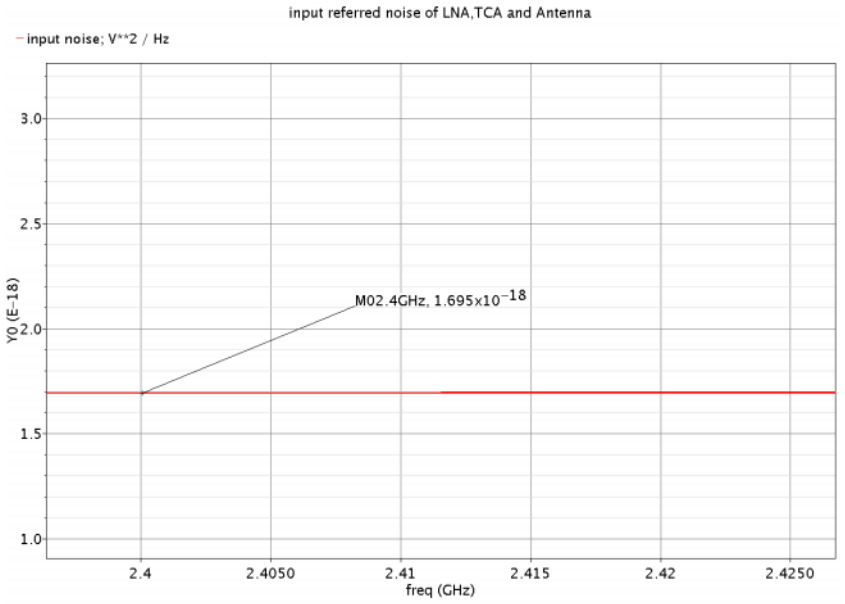

Figure 3.4: Input referred noise voltage PSD of LNA-Transconductor-antenna together

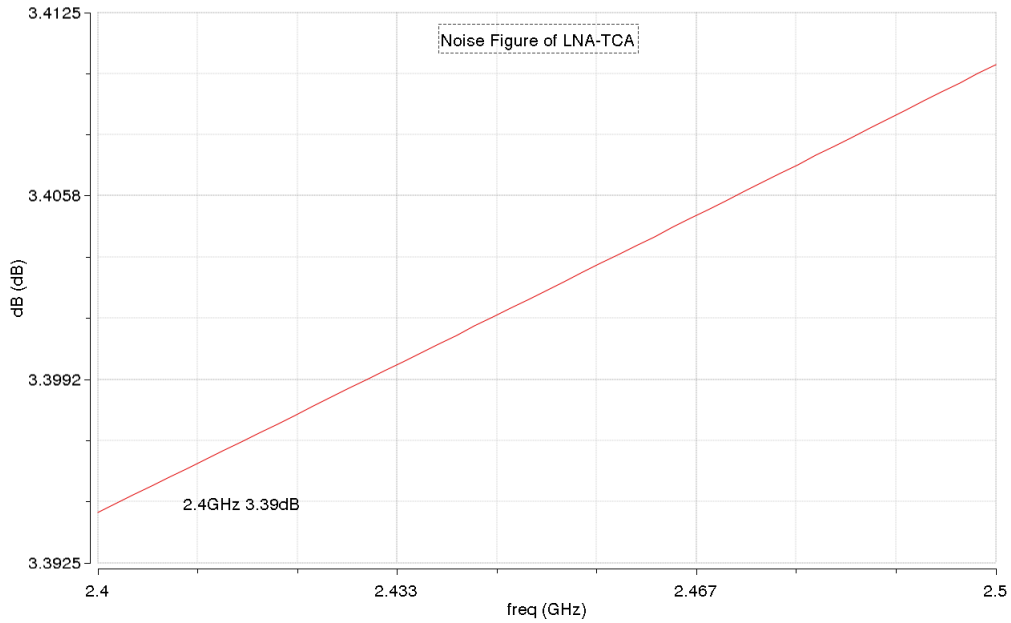

Figure 3.5: Noise figure of LNA-Transconductor cascade

3.2 IIP_3 of Transconductor

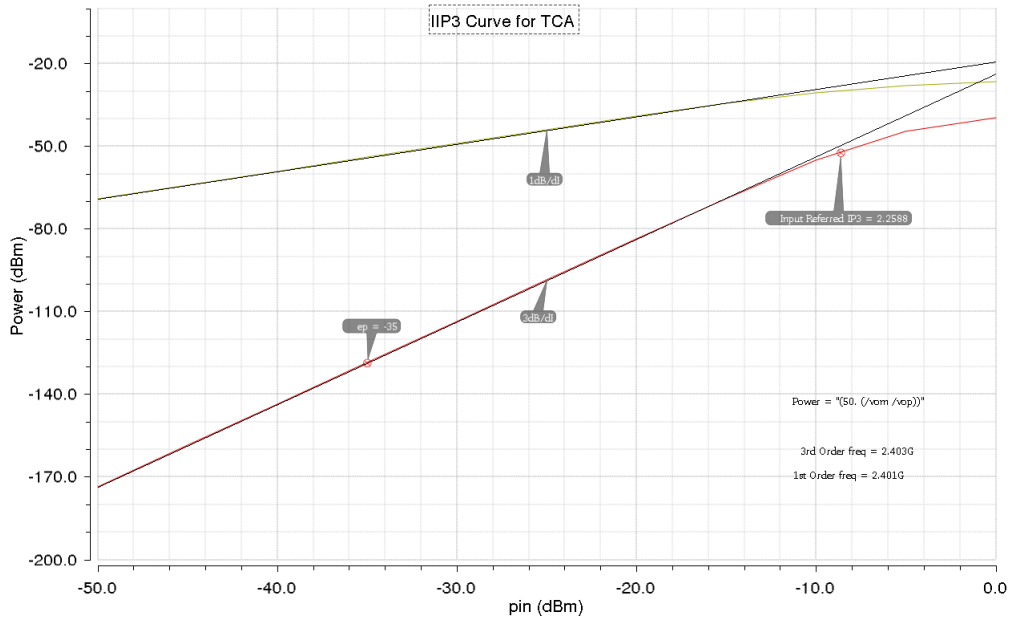

Figure 3.6: IIP_3 of transconductor

As the transconductor is driving the mixer and the TIA, the output impedance of the transconductor is ideally the R_{on} of the switch in the mixer (approximately 10 ohm), the voltage swings at the output of the transconductor are negligible. Therefore, there is no compression faced by the transconductor at it's output. However, there can be compression at the input, because it's input is the amplified voltage output of the LNA. Therefore, we have to bother about the maximizing the IIP_3 of the TCA. Referring to section 2.4, an optimum Gate-source bias voltage is chosen for the input differential pair. The input differential pair is designed with channel length of 60 nm and hence from figure 2.11, the optimum point of V_{gs} is at 500 mV, giving a V_{dsat} of 75 mV.

A transconductor is a voltage controlled current source and needs a very high output impedance. So, the output common mode drain voltages of the input differential pair transistors M_1 and M_2 in figure 3.2 is selected as high as possible, such that a minimum headroom of little more than V_{dsat} is maintained for the active PMOS loads. The active PMOS loads are designed with larger channel lengths to have a high output resistance.

In the design, the output common drain voltages are set at 800 mv. The output common mode voltages are set using a resistive common mode detector and an op-amp connected in negative feedback (shown in green colour in figure 3.1). The IIP_3 of the transconductor is 2.28 dBm and plot for the same is shown below in figure 3.6. The plots for common mode loop gain and phase is shown in figure 3.7:

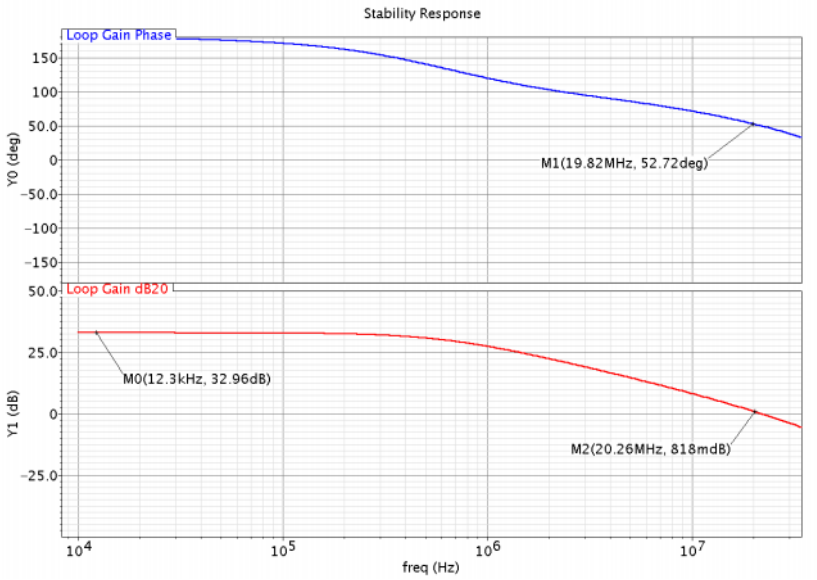

Figure 3.7: Stability of the common mode feedback loop in transconductor

3.3 Layout of TCA stage :

The layout of the transconductance stage is shown in the figure 3.8. The layout shown includes the single stage OP-AMP which is used as transconductor, the common mode circuit, and biasing circuit. The capacitors placed above are the compensation capacitors. The area occupied by TCA is 90 um X 53 um.

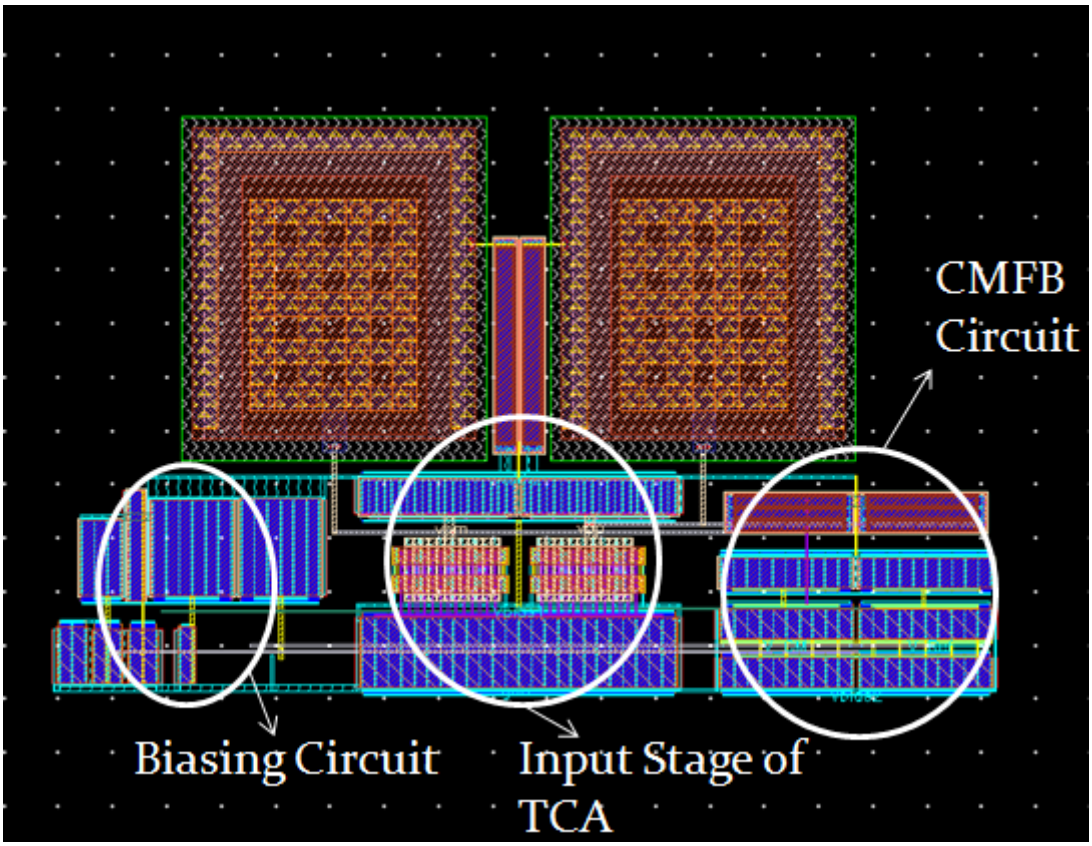

Figure 3.8: Layout view of Transconductor Amplifier

Chapter 4

Current mode 25 % duty cycle double balanced passive Mixer

A 25 % duty cycle passive mixer is chosen because of two reasons:

- To avoid crosstalk between I-path and Q-path. If the spectrum of the signal is anti symmetric then the crosstalk may lead to self corruption of the signal.

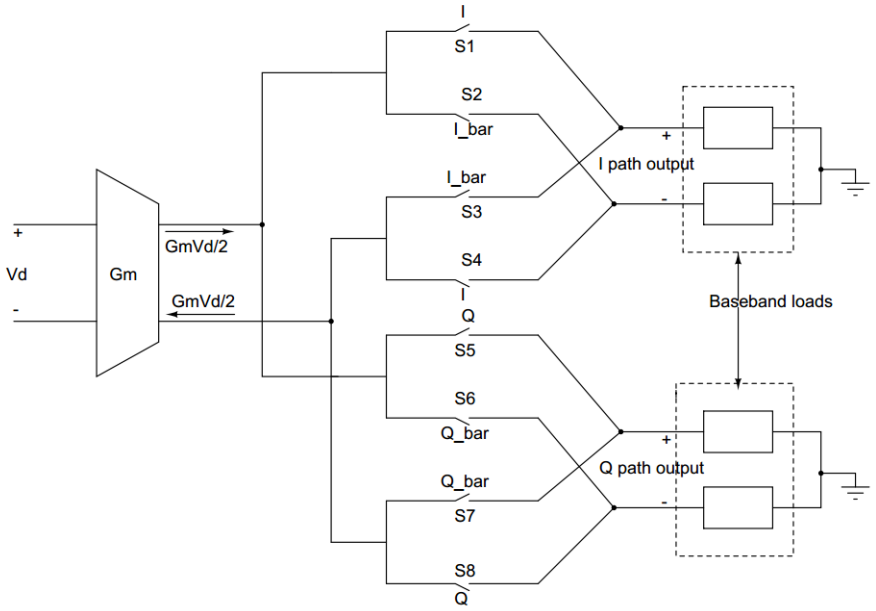

Figure 4.1: A current mode passive mixer

The crosstalk also leads to an increased noise from the mixer.

- The Noise figure of a 25 % duty cycle passive mixer is 3 dB less than the noise figure of a 50 % duty cycle passive mixer.

Both the above points are explained in detail with the help of the diagram shown in Fig. 4.1. The crosstalk can be identified by knowing which switches of the I and Q path are simultaneously ON during the time period 'T' of the L.O (local oscillator) waveforms.

The figure below shows the In-phase and Quadrature-phase waveforms in the case of a 50 % duty cycle passive mixer:

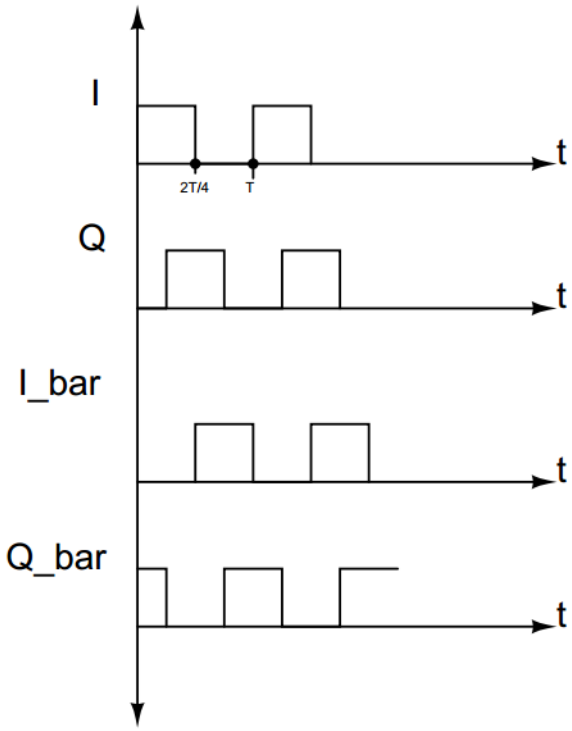

Figure 4.2: 50 % duty cycle I and Q waveforms

During the period 0 < t < T/4 , I and Q_{bar} are ON, causing crosstalk between switches S1, S4 in the I path and S6, S7 in the Q path.
During the period T/4 < t < T/2 , I and Q are ON , causing a crosstalk between switches S1, S4 in I path and S5, S8 in the Q path.

During the period T/2 < t < 3T/4 , I_{bar} and Q are ON , causing a crosstalk between switches S2, S3 in I path and S5, S8 in the Q path.
Similarly during the period 3T/4 < t < T, I_{bar} and Q_{bar} are ON and relevant switches are ON.
It can be easily observed that in every 1/4 part of the time period 'T' both I and Q paths are ON simultaneously, so the input currents $G_m v_d/2$ and -$G_m v_d/2$ each split equally into I path and Q path 'mixer switches' causing only half of the current to be down converted. So, in real only $G_m\ v_d\ /4$ is down converted instead of $G_m\ v_d/2$ resulting in the half the gain of the mixer in either of the paths i.e $1/\pi$

The above problem of the gain and I-Q crosstalk can be solved if two transconductors are used, one for I path and other for Q path. The drawback here is, the output of the LNA is loaded by double the gate capacitance, reducing nodal bandwidth and hence reducing the gain of the LNA, which increases the noise contributions of all the stages after the LNA. This results in an overall increase in the Noise Figure. The next solution without compromising any increase in the Noise Figure of the receiver and to avoid I-Q crosstalk is to use a 25 % duty cycle mixer. The ideal 25 % duty cycle I,Q waveforms are shown in figure 4.3

As we can see in the waveforms, in $1/4th$ of time period T, only one of the phase i.e either I or Q or I_bar or Q_Sbar is active and hence is no crosstalk between I and Q paths. Also as either I or Q path is ON in every quarter of a cycle, complete R.F current $G\_m\ v\_d/2$ is down converted. The current gain of a 25 % duty cycle passive mixer is $\sqrt{2}/\pi$ and it's 3 dB higher than the receiver with a 50 % duty cycle passive mixer with a single transconductor. Therefore the stages after the mixer and mixer itself will contribute less to the overall input referred noise at the LNA input.

4.1 Conversion Gain of a 25 % duty cycle passive mixer

The conversion gain of a double balanced passive mixer is $\sqrt{2}/\pi$, because the magnitude of the fundamental component of a waveform (I - Q) is 2 $\sqrt{2}/\pi$.

$$x_{LO}(t) = \frac{2\sqrt{2}}{\pi}\left\{\sin\omega_{LO}t - \frac{1}{3}\sin 3\omega_{LO}t - \frac{1}{5}\sin 5\omega_{LO}t + \frac{1}{7}\sin 7\omega_{LO}t + \dots\right\} \quad (4.1)$$

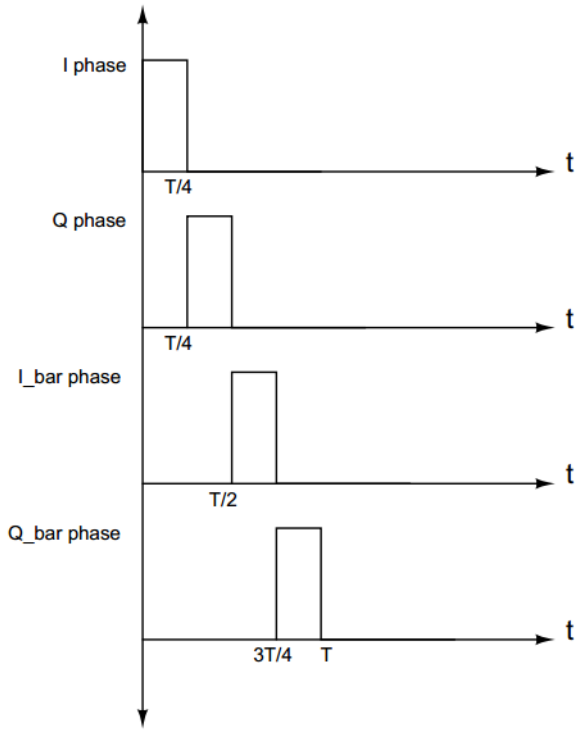

Figure 4.3: 25 % duty cycle I and Q waveforms

On multiplication with an R.F sinusoid the gain becomes $\sqrt{2}/\pi = 0.45$. The figure 4.4 shows the necessary biasing for a passive mixer. The drain of the mixer is directly coupled to the TIA and hence input common mode voltage of the TIA becomes the drain bias voltage for the switches in the mixer. It is at 600 mV in the design. The source node of the switches are biased at 600 mV so that it always operates in heavy triode region when ON. As a NMOS switch passes low voltages very easily, the Gates of all the switches are biased above the drain by one Threshold voltage , i.e approximately 600 mV.

To Test the conversion gain of the mixer a 1 V input is applied to the LNA, it's output is 3.55 V(loaded voltage gain of the LNA is 3.55). The differential input R.F current to the mixer is I_in+- I_{in-} =1 * 3.5 * 11 mS = 38.5 mA. Expected differential output baseband current is I_{out+} - I_{out+}= 0.45 * 38.5 mA = 17.3 mA. The ratio of the currents = 16.72/37.1 = 0.45. The below plots figure 4.5 and figure 4.6shows the differential R.F current input to the mixer and output differential baseband current of the mixer

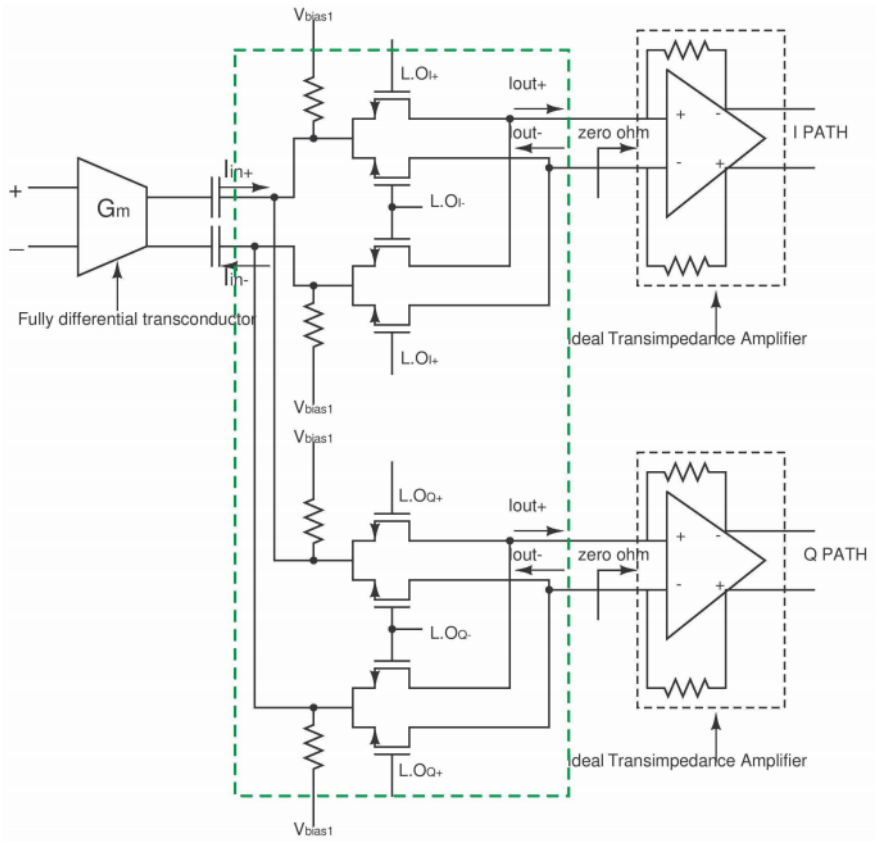

Figure 4.4: Biasing of a passive Mixer

4.2 Noise analysis of a passive mixer by Switched capacitor approach

The noise analysis for a passive mixer is shown with the help of figure 4.7

The thermal noise of a switch with ON resistance of R_{on} is ${I_{Ron}}^2 = \frac{4KT}{R_{on}}$. During the I phase, (switches driven by $L.O_{I+}$ are ON)the nodal capacitors C_T are charged with the noise current PSD of the ON resistances of the two switches. The charging process is shown by green and red arrows for the two capacitors C_T. During the Q phase, (switches driven by $L.O_{Q+}$ are on)the capacitors discharge through the ON switches in the Q path into the virtual ground nodes of the TIA. A capacitor C_T charged by an I phase switch and discharged through a Q phase switch gives an

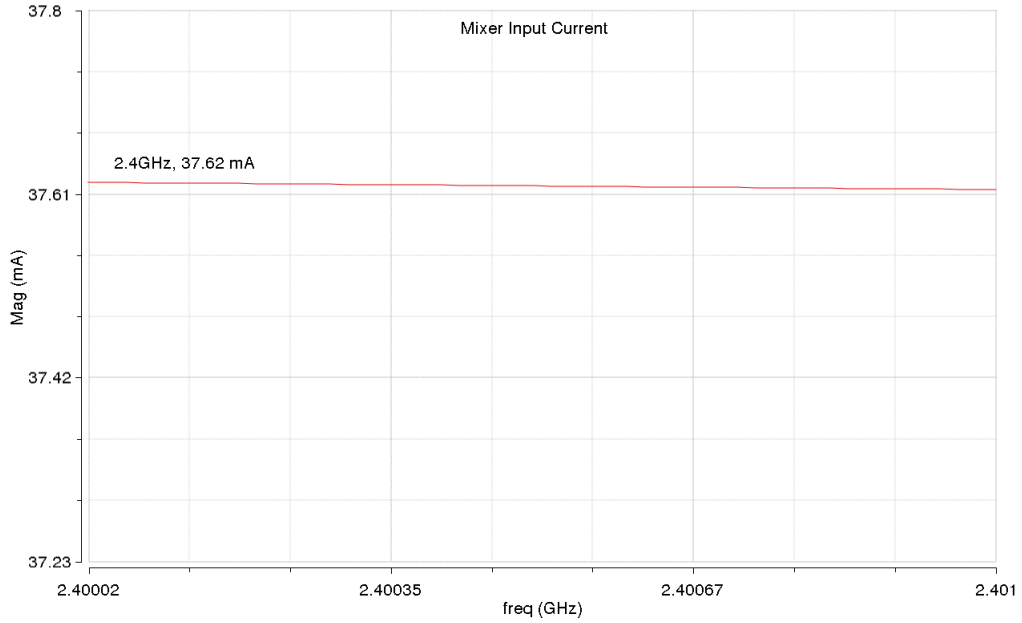

Figure 4.5: Differential R.F current input to the mixer in mA

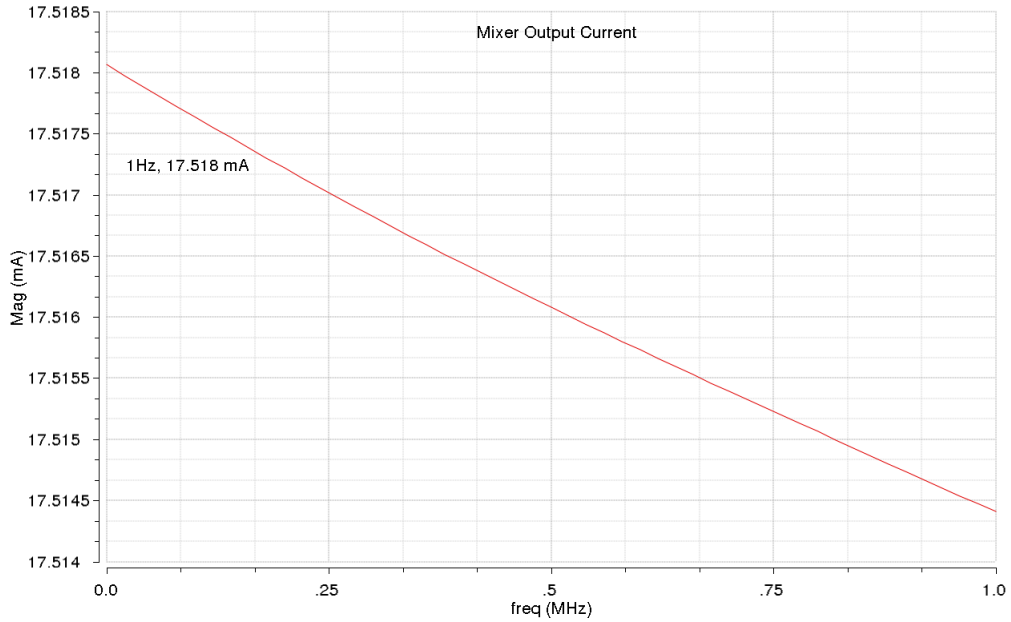

Figure 4.6: Differential Baseband current input to the mixer in mA

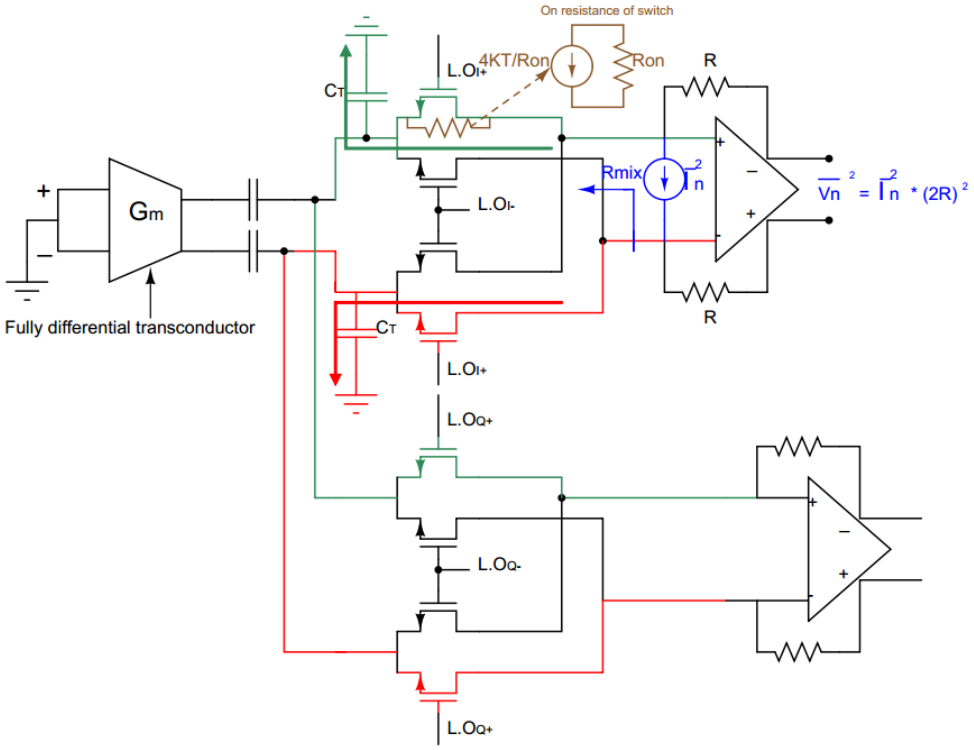

Figure 4.7: Noise analysis in a passive mixer

equivalent resistance of $\frac{1}{f_0 C_T}$, according to switched capacitor analysis looking into the single output node of Q path mixer. Since, there are two charge and discharge process going on simultaneously, the equivalent output resistance of the mixer in I or Q path is $\frac{2}{f_0 C_T}$. This process of charge and discharge of nodal capacitor C_T leads to the noise contribution by the passive mixer. The amount of noise charge deposited on the capacitors is proportional to the R_{on} C_T time constant. So, if C_T is higher then the amount of noise charged sampled by the switches is higher and hence a higher noise contribution from the mixer.

The switched capacitor output resistance(for the I or Q mixer) $R_{mix} = \frac{2}{f_0 C_T}$ is shown in blue colour in figure 4.7. The current noise PSD due to R_{mix} is $I_n^2 = 4\text{KT}/R_{mix}$. Thus, the output voltage squared noise PSD in the I path(or Q path) is $V_n^2 = I_n^2\,(2R)^2$. In our design the noise due the mixer is tracked by hand calculations, with the help of the switched capacitor analysis.

The hand calculation tracking is done as follows: **What is the value of C_T?**

The below figure shows, how to calculate the value of C_T. The switches are sized

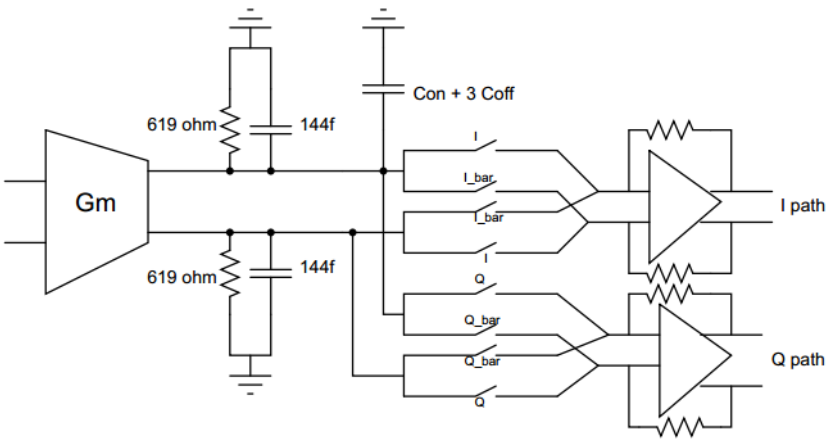

Figure 4.8: Estimating the value of capacitor C_T

such that with a gate swing of 600 mV to 1.8 V(the L.O swing is 1.2 V but the gate is biased at 600 mV), the on resistance of the switch is at 10 ohm. The W/L of a switch is selected as 64 u/60 nm. Each output node of the TCA is connected to four switches, and as only one of the switch is ON in a time period of the L.O, the total capacitance contributed by the mixer at each node is given as C_{on} + C_{off}.In the design, C_{on} = 63.5 fF and C_{off} =25.6 fF. A total of 140.3 fF is contributed by mixer to each output node of the TCA.Thus, C_T = 144 + 140.3 = 284.3 fF. R_{mix} = $\frac{2}{f_0 C_T}$ = 2924 ohm. The current noise PSD of R_{mix} is referred to the LNA as $\frac{4kT/R_{mix}}{(gainofLNA)^2 G_m^2 (gainofmixer)^2}$ which is $\frac{4kT/R_{mix}}{16*11mS^2*0.45^2}$ = 1.375 * 10^{-20} V^2/Hz per switch. For four switches, it is 4 times and hence the input referred noise voltage at the input LNA due to the I path is 5.5 * 10^{-20} V^2/Hz. According to the noise summary in the pnoise analysis, the contribution due to the mixer is 6 * 10^{-20} V^2/Hz, which is approximately equal to the hand calculated result.

4.3 Frequency Divider with 25% LO Waveforms

The frequency divider employs two D-latches in a master-slave configuration with negative feedback. The two identical D-latches are driven by complementary clocks. It looks like a counter operating at GHz of frequency. As there are two latches, there

can be four possible outputs.

The circuit implementation for the frequency divider proposed by Razavi [7]. is shown in Fig. 4.9. Each latch consists of two sense devices (M_{s1} and M_{s2} in the master and M_{s3} and M_{s4} in the slave), a regenerative loop (M_{c1} and M_{c2} in the master and M_{c3} and M_{c4} in the slave), and two pull-up devices (M_{p1} and M_{p2} in the master and M_{p3} and M_{p4} in the slave). A 4.8 GHz square signal drives the four PMOS transistors. When CLK is high, M_{p1} and M_{p2} are OFF and the master is in the sense mode, while M_{p3} and M_{p4} are ON and the slave is in the store mode.

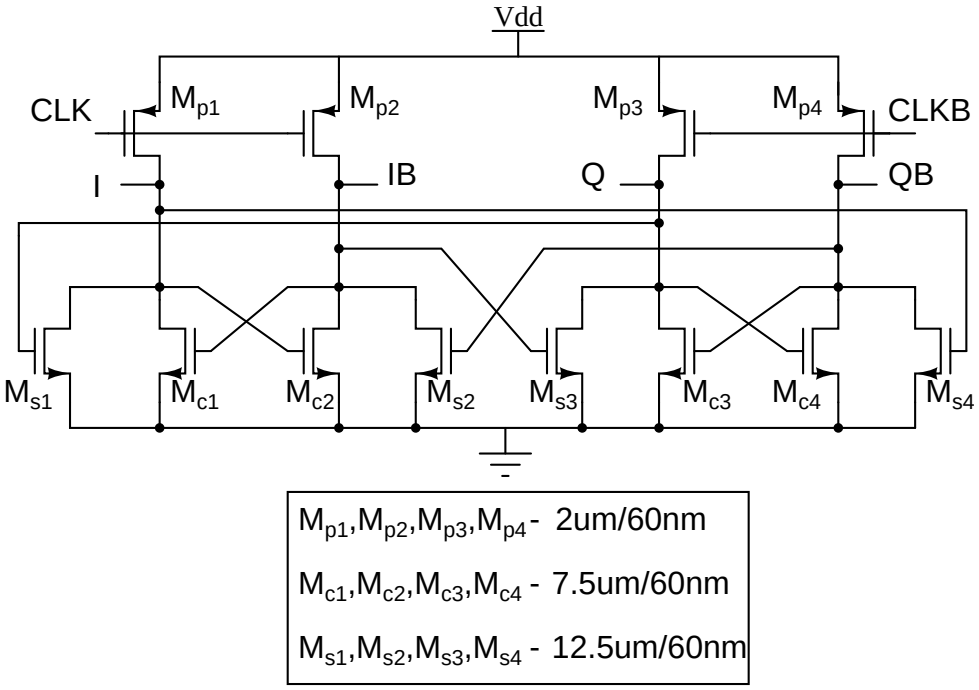

Figure 4.9: 25%-duty-cycle LO generator

When CLK goes low, the reverse occurs. Out of four, two PMOS transistors turn ON at a time. They try to pull their drain terminals to V_{DD}. But a cross coupled NMOS in the same latch, tries to pull only one of them to V_{DD} and other to ground. The V_{DD} output is decided by the sense MOS transistors. Thus the circuit inherently generates a four-phase clock with 25%-duty-cycle signal.

To remove the ripple in the zero state and for proper pulse shaping, four buffers are added next to the divider on for each output of the divider circuit. The entire

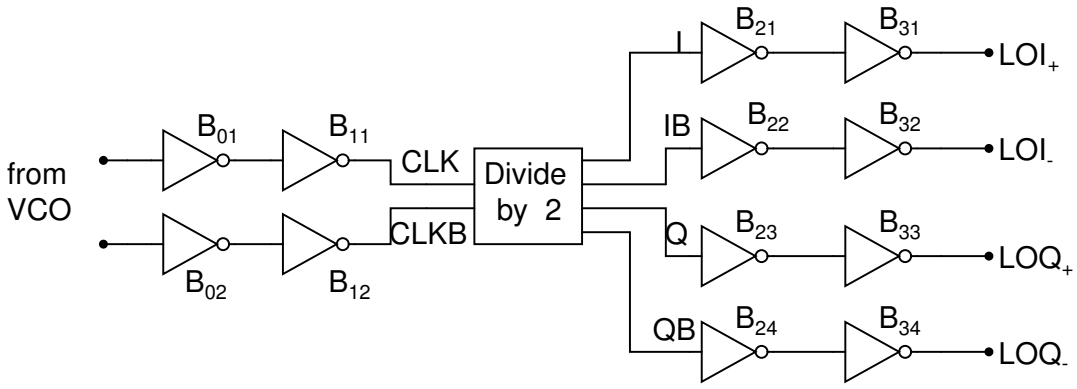

Figure 4.10: Complete LO generator

block diagram of LO generator circuit is given in Fig. 4.10. The buffer is a two-stage inverter to enhance the drive capability. The sizes of the MOSFETs are chosen such that the overlap voltage is lesser than 300mV (threshold voltages of MOS switches is 450mV) and the rise/fall time is lesser than 40psec. VCO produces differential 4.8 GHz sinusoidal signals. Two buffers follow the VCO and convert sinusoidal wave into rail-rail square waves for the complementary clocks to the divider circuit.

The output waveforms of the frequency divide by 2 circuit with 25% duty cycle are shown in the Figure 4.11.

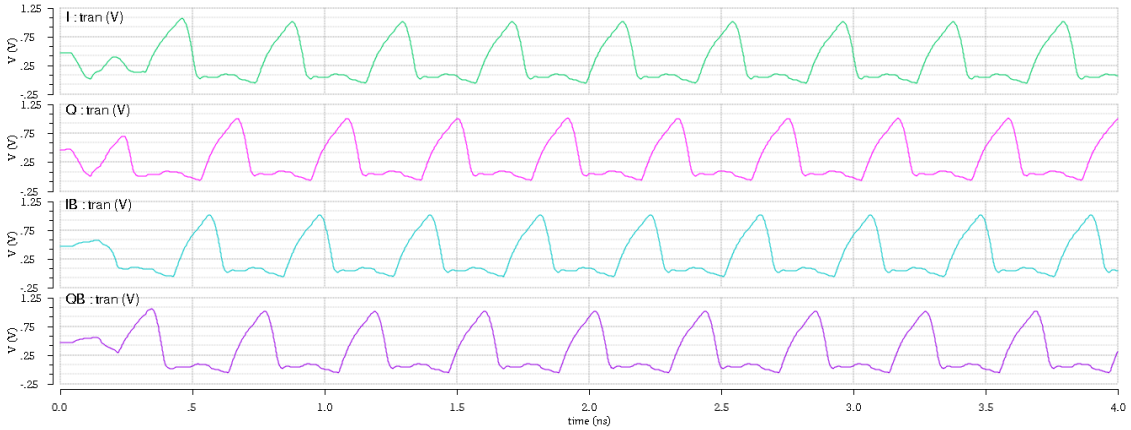

Figure 4.11: Output waveforms of frequency divider circuit

As explained in the section 4.3, the buffer circuit removes the ripple in the zero state and does pulse shaping. The output of the buffer circuit is shown in the Figure

4.12.

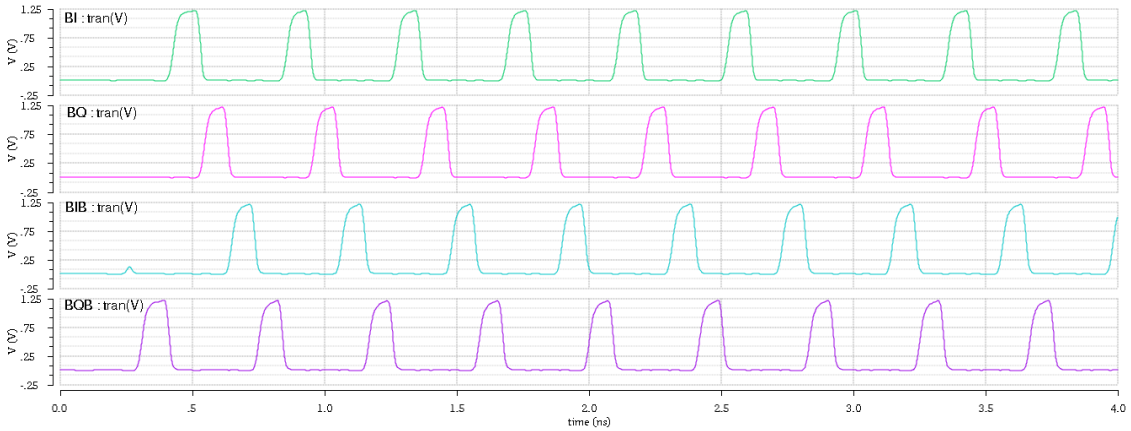

Figure 4.12: Output waveforms of Complete LO Generator

In the Figure 4.12 the waveforms from top are LOI_+, LOQ_+, LOI_-, LOQ_- respectively with reference to the Figure 4.10. The overlap between every two waveforms is around 247mV as shown in Figure 4.13. The rise/fall times of all the waveforms is 36.3psec. Thus the waveforms meet all the requirements.

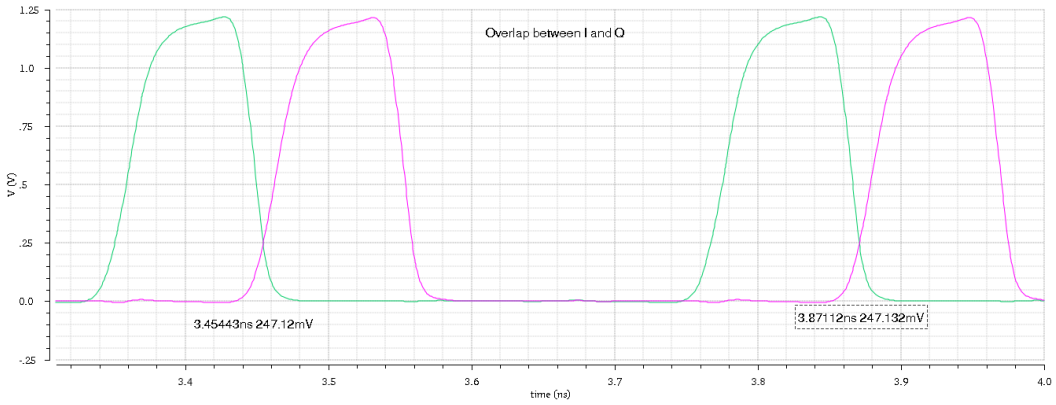

Figure 4.13: Overlap Voltage between LOI_+ and LOQ_+

4.4 Layout of Mixer and Frequency Divider Circuit :

The layout of the passive mixer with 25% duty cycle LO generator along with the buffers is shown in the Figure 4.14. In the Figure 4.14 to the extreme left is the input clock buffers. To its right, in the center, the buffers after the divide by 2 circuit shown in Figure 4.10 are placed. The divide by 2 circuit is placed in the center and bottom with master on top and slave at bottom. To the extreme right, the 8 MOSFETs of the passive mixer shown in Figure 4.1 are laid out. The area occupied by Mixer and Frequency Divider is 100 um X 80 um.

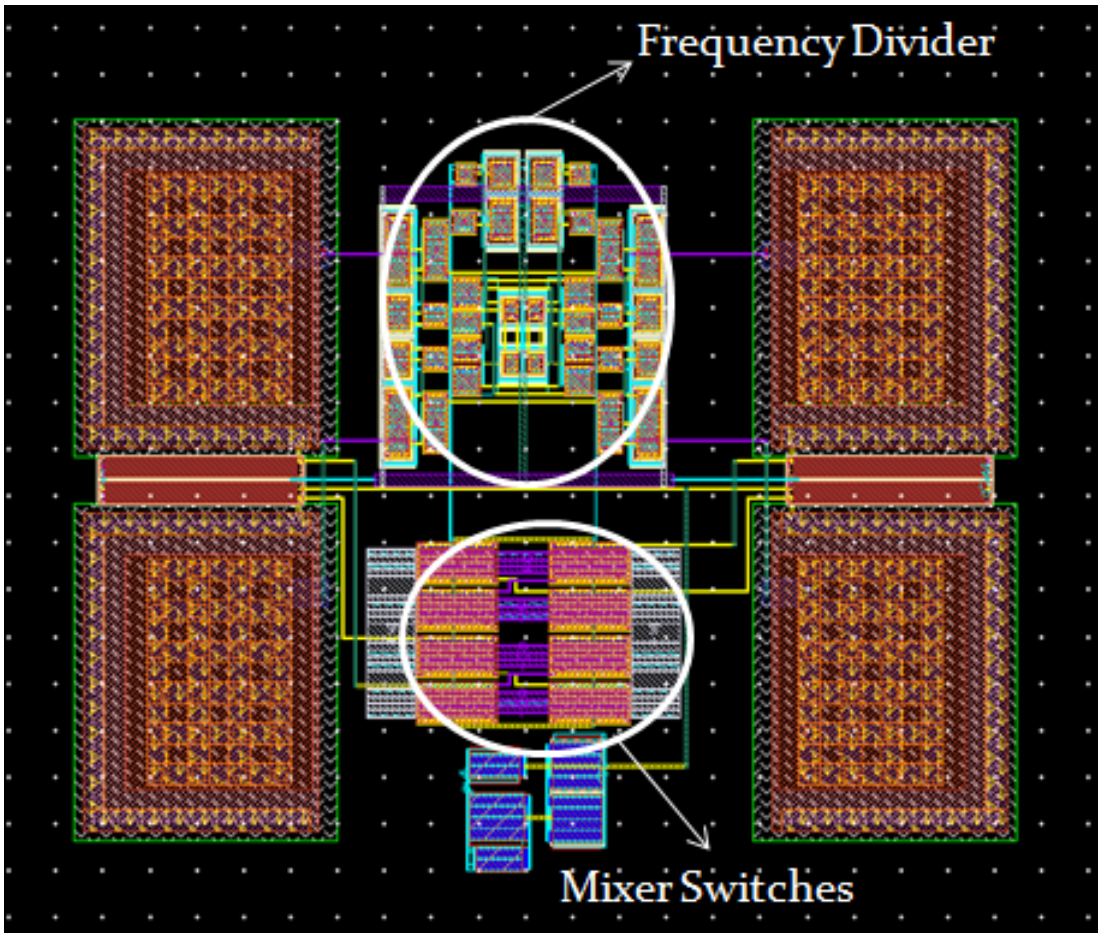

Figure 4.14: Layout of the current mode passive mixer and Frequency Divider Circuit

The layout of Low Noise Amplifier, TransConductor stage and the mixer along with frequency divider circuit is shown in figure 4.15. In the fig 4.15, towards left is the layout of the Low Noise Amplifier and in the center the TrasnConductance Amplifier stage is placed and to the rignt side is the layout of Mixer circuit along with the Frequency divide by 2 circuit. The area occupied by LNA, TCA, and Mixer is 290 um X 200 um.

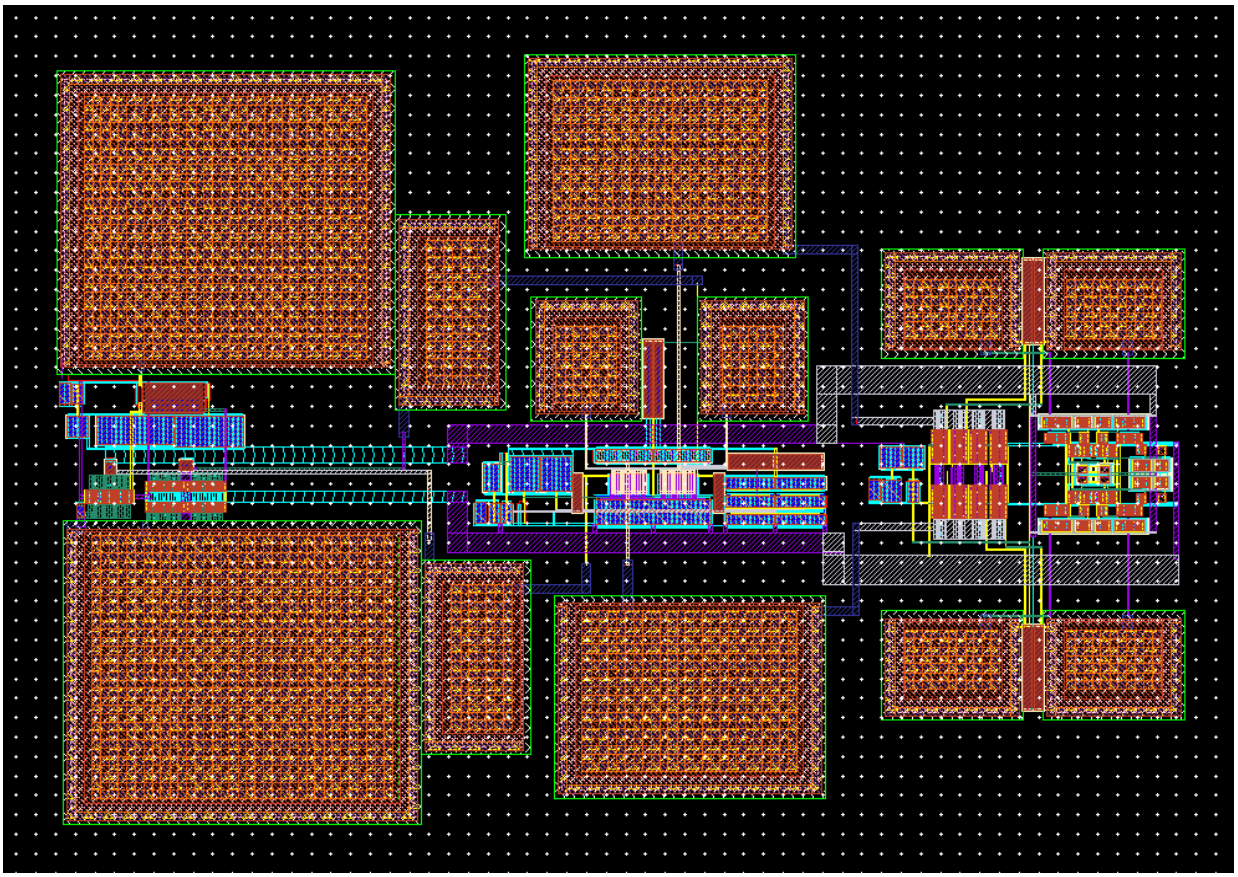

Figure 4.15: Layout of the LNA - TCA - Mixer along with Frequency Divider Circuit

Chapter 5

Transimpedance amplifier (TIA)

The current mode passive mixer down converts the RF signal to the baseband signal, and this down converted current at baseband frequencies is to be converted in to voltage signal. For this purpose Trans Impedance Amplifier is used. Trans Impedance Amplifier is designed using a two stage fully differential OP-AMP operated in negative feedback with a resistance in the feedback. A capacitor is also placed in parallel to this resistance for low pass filtering action. We use two such Trans Impedance Amplifiers one for I-channel and another for Q-channel.

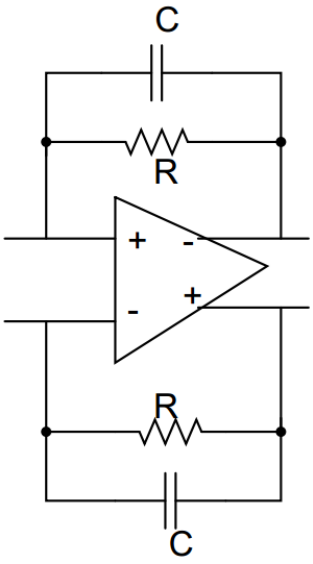

Figure 5.1: TIA:Opamp with a first order low pass filter

TIA is designed using a 2 stage opamp Fig. 5.2

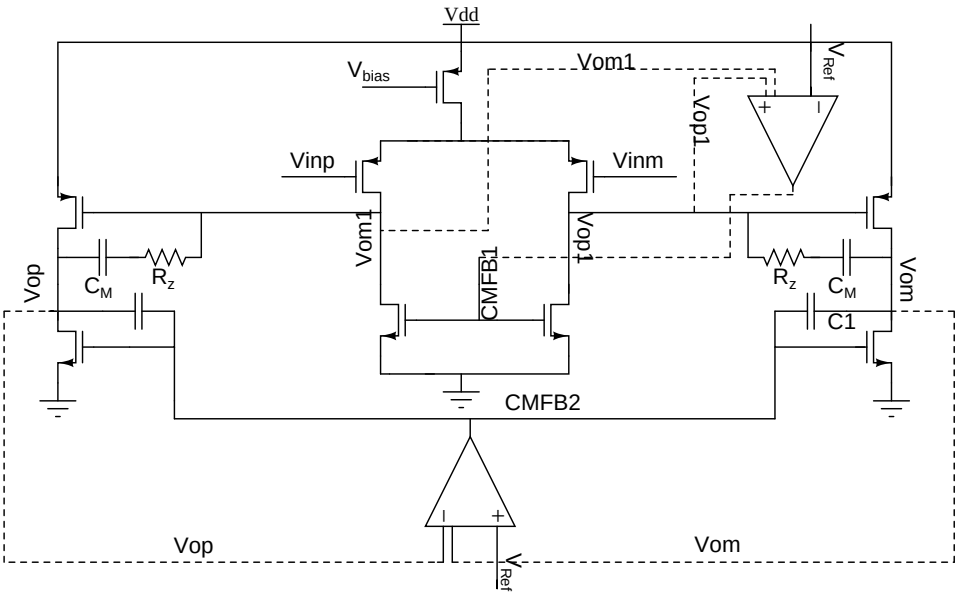

Figure 5.2: Two Stage OPAMP

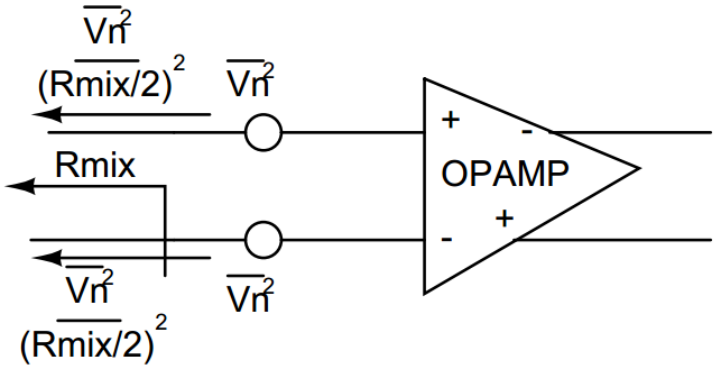

Figure 5.3: Specification on input referred noise of opamp

The main concerns in designing the Trans Impedance amplifier are Input referred Noise, Input Impedance of the TIA stage which is governed by Unity Gain Frequency, Open loop DC gain of the OP-AMP, Flicker Noise from the OP-AMP, Corner Frequency and Power Consumption.

Specification on the input referred noise of the OP-AMP is derived as follows figure 5.3: $I_n^2 = \frac{V_n^2}{(R_{mix}/2)^2}$, $R_{mix} = 2924\Omega$. I_n^2 when referred to the input of LNA is, $\frac{\bar{I_n^2}}{A_{LNA} * g_m * 0.45} < 2.5 * 10^{-19}$, which is the noise budget for the TIA.
The input referred Noise of a differential OP-AMP is given in the below equation 5.1

$$\bar{V_{in}^2} = 8KT\gamma \left(\frac{1}{g_{m1}} + \frac{g_{m3}}{{g_{m1}}^2} \right) \tag{5.1}$$

By completing the calculations we get $V_n^2 << 8 * 10^{-17}$. The Input referred voltage noise PSD of a differential input pair ignoring the Noise PSD due to active loads, is $\frac{(8KT\gamma)}{g_m}$ which is 2 * V_n^2 . To have lesser thermal noise the g_m of the input pair should be sufficiently high and the g_m of the active load transistors should be atleast 4 times lesser than the transconductance of input pair. From this we get that g_m should be more than 138 μS. But, the flicker noise corner at this g_m is more than 1 MHz, which will drown the complete bluetooth signal.

Also, to have lesser Flicker Noise the input pair transistors are preferable larger in dimensions and the channel length is selected to be 1 μm. A 1 μm channel length device gives a maximum dc gain of 100 , when biased at a V_{dsat} of 70 mV.
The Trans Conductance of the input pair is selected such that the thermal noise of the input pair is very less and the corner frequency is around 1 KHz.
The current density in the input diff pair is selected to have maximum dc gain.

The trans resistance of the Trans Impedance amplifier is 1 KΩ. The impedance of the mixer looking in from TIA stage is around 2.5 KΩ. As mixer used is in current mode the TIA should offer very less input impedance (ideally it should be zero) so that all the signal current flows through TIA stage. But the input impedance of the Trans Impedance Amplifier depends on Unity Gain Frequency and Open loop DC gain of OP-AMP. The relation is given in the equation 5.2 below.

$$R_{in} \approx R_F \left(\frac{1}{A} + \frac{s}{\omega_u} \right) \tag{5.2}$$

R_{in} is input impedance of TIA, R_F is the feedback resistor and ω_u is the Unity Gain Frequency.
From the above relation we can observe that the Unity Gain Frequency and DC Gain of the OP-AMP should be as high as possible. For the OP-AMP used in TIA, unity gain frequency of 100 MHz, and DC gain of 63 dB is sufficient. With this

specifications the input impedance of the TIA is around 10 Ωs, which is reasonable good. The plot in figure 5.4 shows the variation of Input Impedance w.r.t Unity Gain frequency. The plot for the Input impedance of the TransImpedance amplifier at open loop gain of 63 dB at various unity gain frequencies is shown in the figure

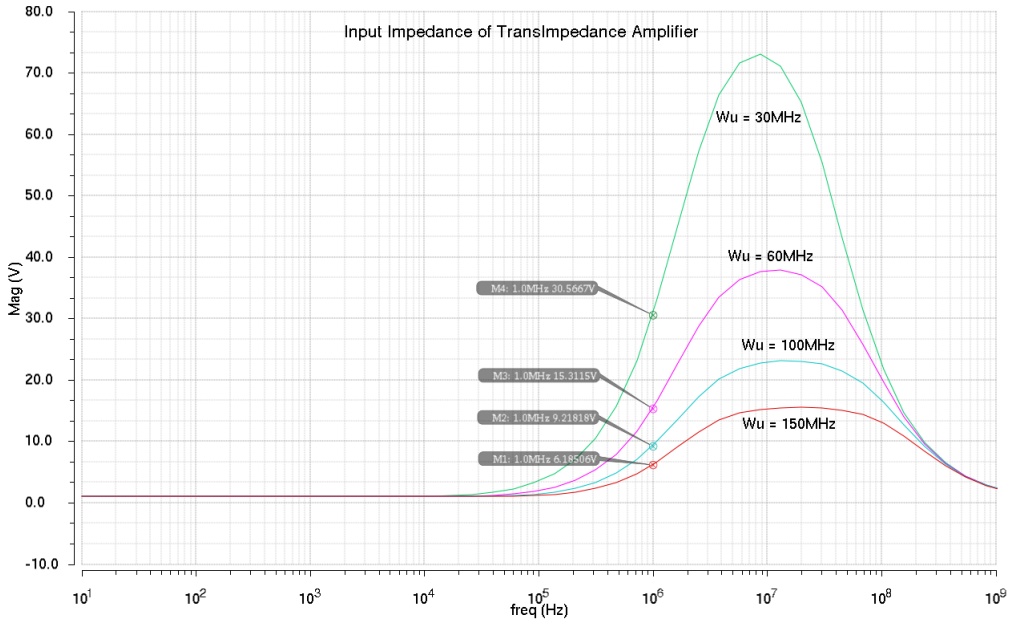

Figure 5.4: Input Impedance of Trans Impedance Amplifier

5.1 Layout of Trans Impedance Amplifier and results:

The figure 5.5 shown is the layout of the transimpedance amplifier. In the layout the larger transistors are input pair transistors below that is the second stage, the biasing circuit is placed to the right side. The larger capacitors on the either side of input differential pair are miller compensation capacitors. The capacitors placed below are the compensation capacitors used to stabilize the common mode feedback loops. The area occupied by Trans Impedance Amplifier is 300 um X 200 um.

Plot for DC gain and phase margin are shown in Figure:5.6 The Open Loop DC gain of the OP-AMP is around 65 dB. The Unity Gain frequency is 130 MHz, and

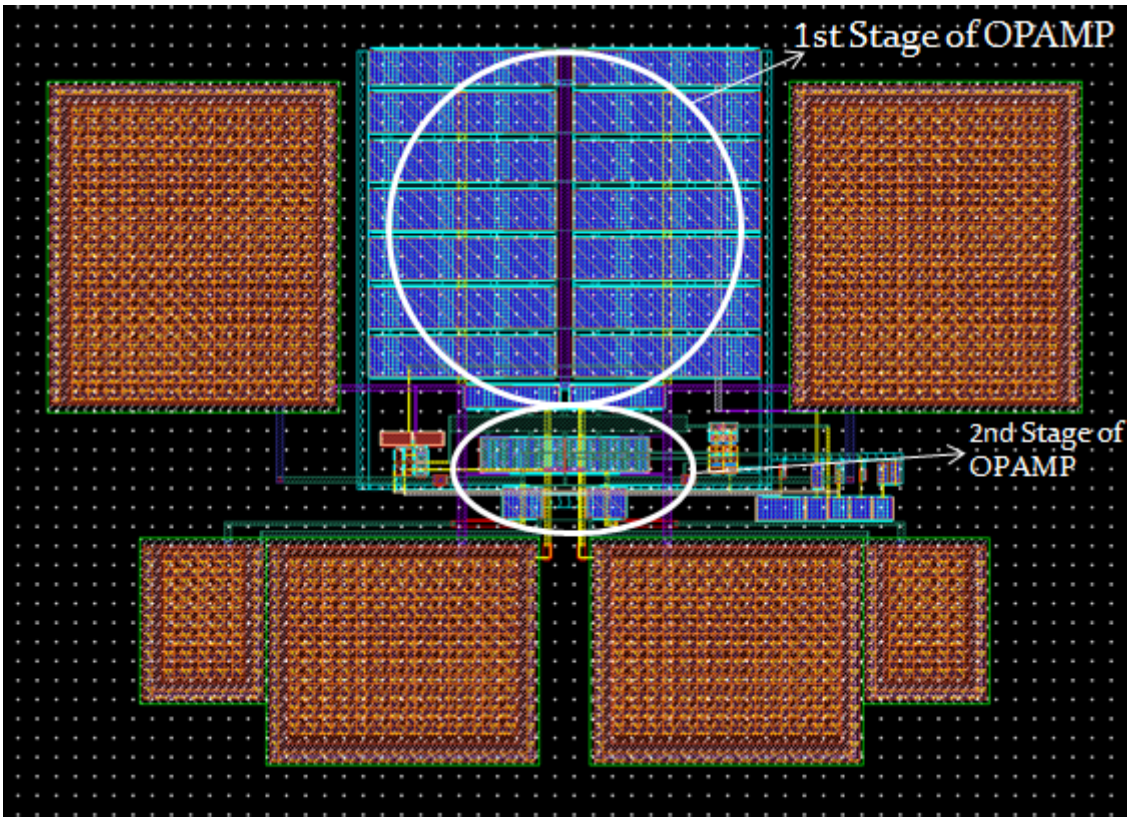

Figure 5.5: Layout of the Transimpedance Amplifer

the phase margin of the OP-AMP is 61 degrees.

Plot for Stability of Common Mode Feedback Loop 1 is shown in figure 5.7. The DC gain of the common mode loop is 58 dB, and the corresponding phase margin is 75.2 degrees.

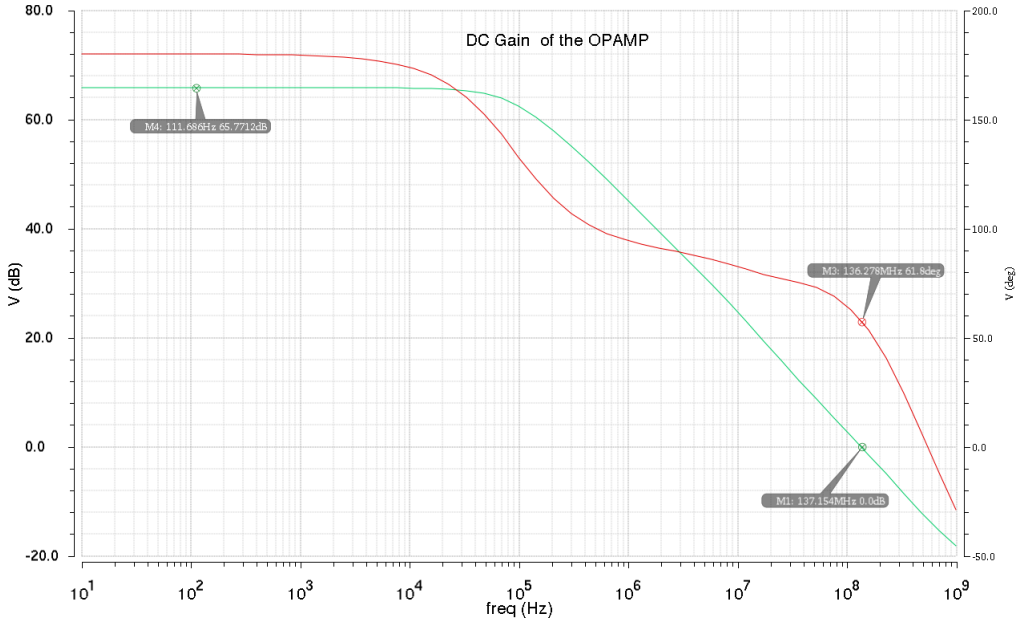

Figure 5.6: DC gain of the opamp

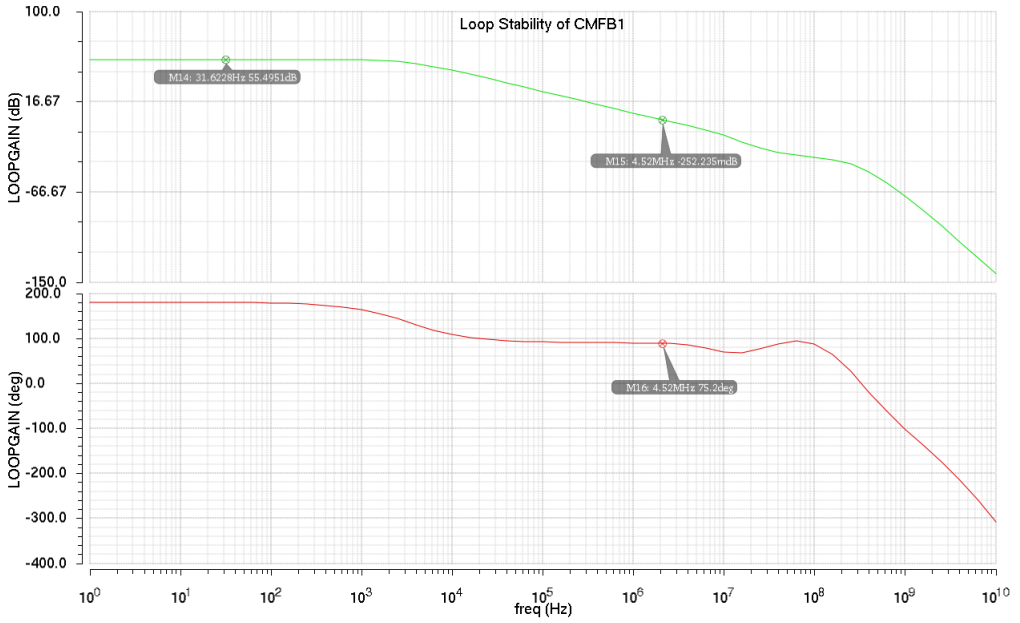

Figure 5.7: Stability of CMFB1

Plot for Stability of Common Mode Feedback Loop 2 is shown in figure 6.2. The DC gain of the common mode loop is 60 dB, and the corresponding phase margin is 74.5 degrees.

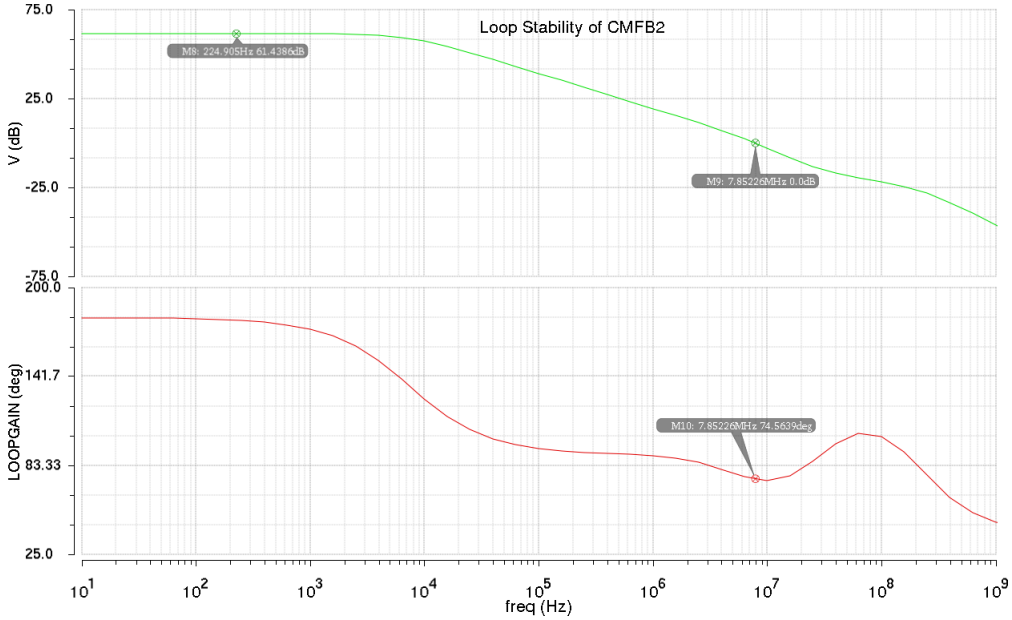

Figure 5.8: Stability of CMFB2

The cutoff frequency of the low pass filter can't be selected at 1MHz, as the droop will be 3dB then. Hence, a cutoff of 2.5 MHz is selected, which demands capacitor of 63.6 pF in parallel to the 1K Ω resistor.

Chapter 6

Layout and the Results of the complete Receiver Chain

6.1 Layout of the complete receiver chain :

The layout of the complete receiver chain is shown in the figure 6.1

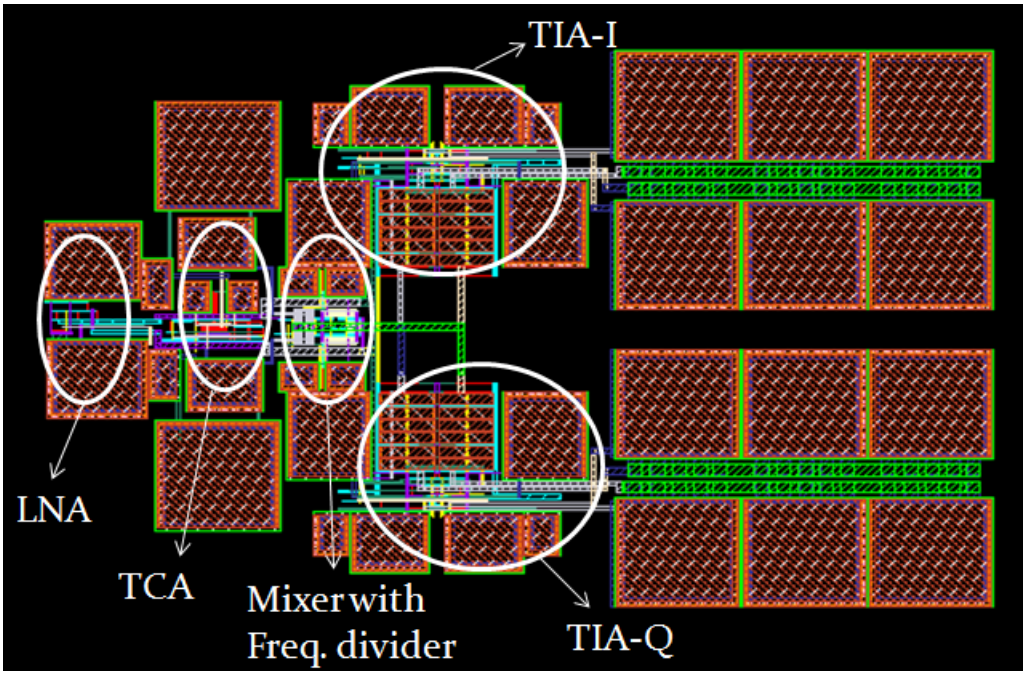

Figure 6.1: Layout of the Complete Receiver Chain

The layout of Low Noise Amplifier, TransConductor, mixer along with frequency divider circuit and the Trans Impedance Amplifier stages is shown in figure 6.1. In the layout shown in figure. 6.1, towards left is the layout of the Low Noise Amplifier and after that in the center the TrasnConductance Amplifier stage is placed and beside that layout of Mixer circuit along with the Frequency divide by 2 circuit is kept and to the right is the Trans Impedance Amplifier stage. In this receiver chain we use two TIA blocks, one for I-channel and another for Q-channel. These two are placed symmetric to the mixer circuit. In this TIA stage, in feedback we use 1 KΩ resistor and 63.6 pF capacitor in parallel, as we are having two such stages totally we need 4 such 63.6 pF capacitors which are placed to the extreme right side in the layout. The area occupied by Entire Receiver Chain is 570 um X 850 um.

6.2 Voltage Gain, Noise Figure and IIP3

1. **Voltage Gain of the Receiver Chain:**
   The voltage Gain of the LNA loaded by the TCA is 3.55, followed by transcon-

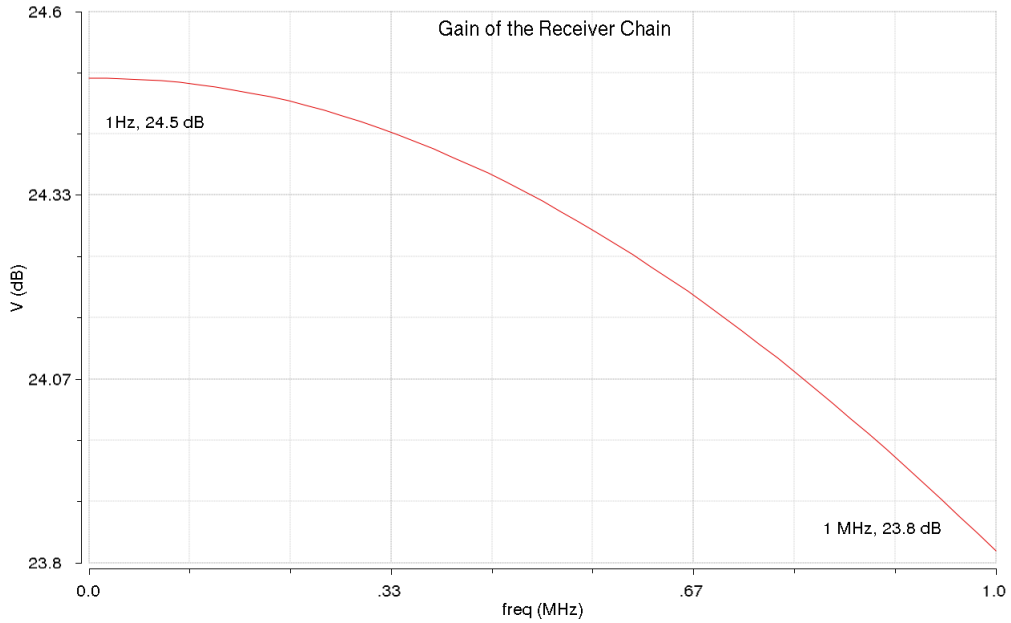

Figure 6.2: Voltage Gain of the receiver

ductance gain g_m = 11mS, followed by a mixer with a current conversion Gain

=0.45 and a TIA with transresistance of 1KΩ. So the Overall Conversion Gain of the receiver chain is 3.55 * 11 mS * 0.45 * 1000 Ω = 17.5 = 24.8 dB.
The plot for the voltage Gain of the receiver is shown in the figure

2. **Noise Figure of the Receiver :** The integrated Noise figure of the receiver from a corner frequency of 10 KHz to 1 MHz is 4.28 dB. Table 6.1 representing noise contributions of different blocks in the receiver is shown below: The plot

Name of the block	NF percentage contribution
Antenna	39
Low Noise Amplifier	30
Fully Differential transconductor	13
Mixer	9
Transimpedance Amplifier	6

Table 6.1: Noise contribution by various blocks in receiver chain

for the Noise Figure is shown below:

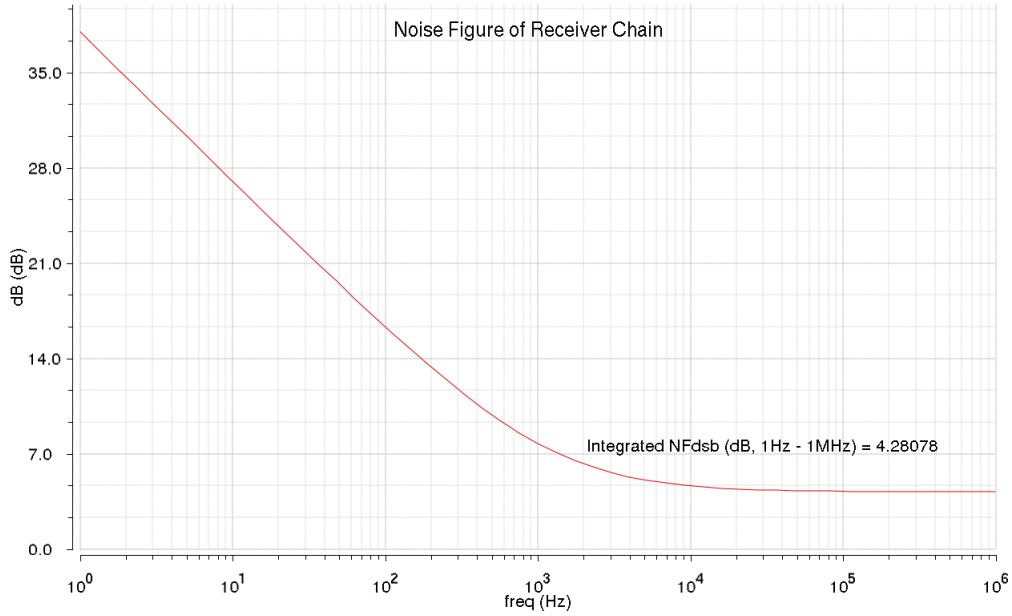

Figure 6.3: Noise Figure of the receiver

3. **IIP3 of the receiver chain :** The IIP_3 of the RX chain is -10.3 dB. This result is evident because, the gain of the LNA is 11.5 dB (LNA loaded) and the IIP_3 of the TCA as shown in chapter on TCA is approximately +2 dBm. So, the overall IIP_3 of the Chain has to be less than $(2 - 11.5) = -9.5$ dBm. And the IIP_3 of the chain is -10.3 dBm. The plot for IIP_3 is shown below. Also,

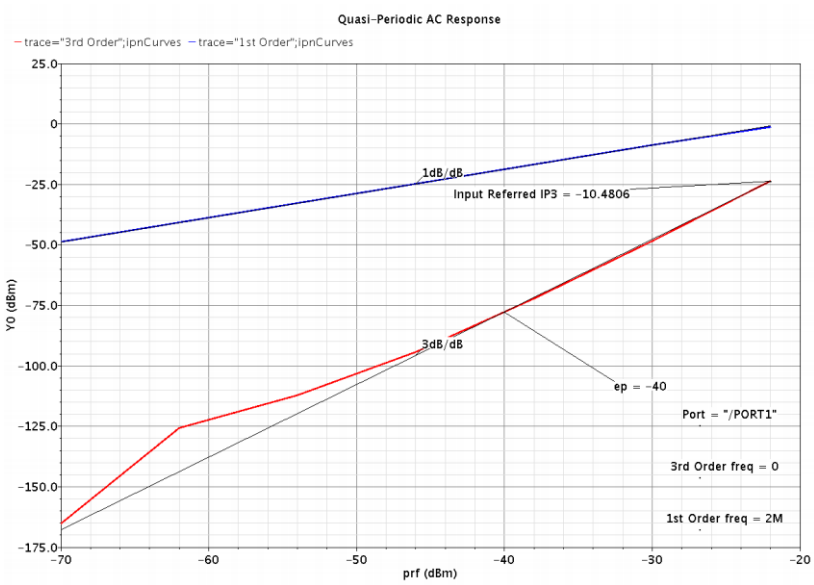

Figure 6.4: IIP_3 of the receiver

an interesting point can be absorbed from this result, i.e., the passive mixer and the TIA hardly undergoes any compression. This shows that a current mode architecture is best suited to obtain good IIP_3 or a good linearity. Also,the 1-dB compression point according to the relation between IIP_3 and the 1-db compression point, i.e., P1-dB = IIP_3 - 9.6 dB, is -19.6 dBm. The P1-dB, can also be understood intuitively as: The transistors in the 2^{nd} stage in the two stage OP-AMP,are designed to have a V_{dsat} of, 100 mV. The output common mode is set at 600 mV, therefore allowable output signal swing is V_{dd} - V_{dsat} = 600 mV - 100 mV = 500 mV. When referred back to the input of the LNA, corresponding input signal is 500 mV/16 = 31.2 mV = -20 dBm. After -20 dBm of input, there is voltage compression at the output as the transistors in the output stage go from saturation to triode region, so it makes sense to say that P1 db point of the receiver is at -20 dBm.

6.3 Voltage Gain, Noise Figure and IIP_3 across process corners

The plot of Voltage Gain across process corners is shown below in figure 6.5

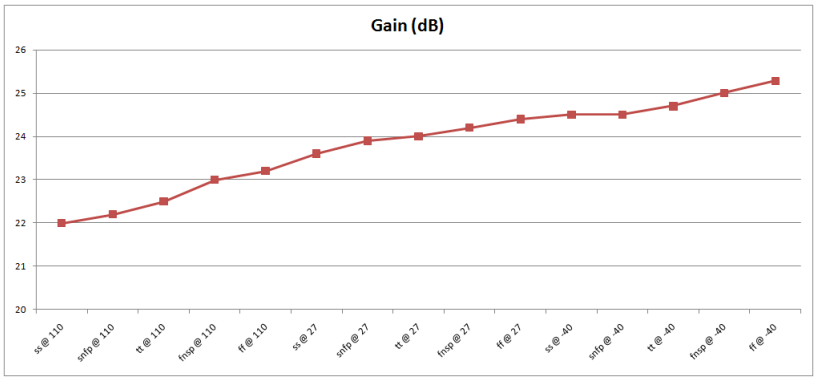

Figure 6.5: Voltage gain across process corners

The plot of Noise figure across process corners is shown below in figure 6.6.

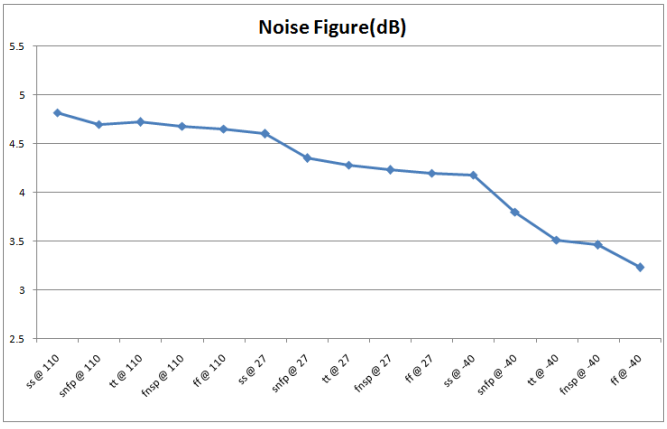

Figure 6.6: NF across process corners

The plot of IIP_3 across process corner is shown below in figure 6.7:

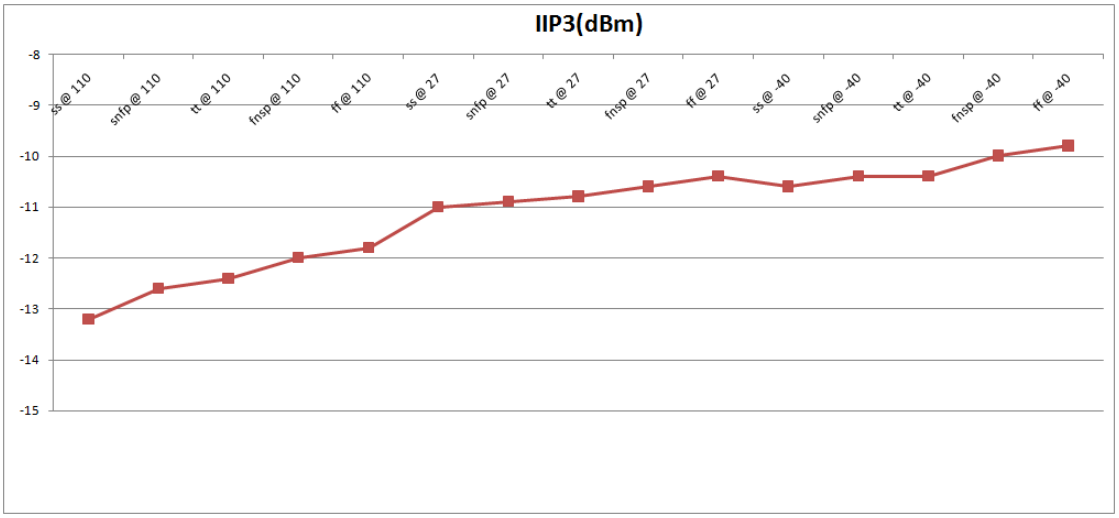

Figure 6.7: IIP_3 across process corners

6.4 Results Summary

Specifications of all the blocks and their power consumptions are given below in tabular form.

- **Low Noise Amplifier**

Characteristic	Value
$S11$	-11.1 dB
Voltage Gain(unloaded)	12.4 dB
NF	2.64 dB
IIP_3	5.4 dBm
Current Drawn	6.87 mA
Power consumption(V_{dd} =1.2 V)	8.2 mW

Table 6.2: Summary of LNA

- **Trans Conductane Amplifier**

Characteristic	**Value**
Transconductance	$11mS$
NF	12 dB
Output impedance	619 Ω ‖ 144 fF
Current Drawn	1.9 mA
Power consumption(V_{dd} =1.2 V)	2.28 mW

Table 6.3: Summary of TCA

- **Mixer and Frequency Divider**

Characteristic	*Value*
Conversion Gain	0.45
On resistance of the switch	9 ohm
Contribution to capacitance C_T	140 fF
Current Drawn by Frequency Divider(V_{dd} =1.2 V)	3.7 mA
Power consumption by Frequency Divider(V_{dd} =1.2 V)	4.4 mW

Table 6.4: Summary of Mixer and Frequency Divider

- **Trans Impedance amplifier**

Characteristic	*Value*
Transimpedance	1K Ω ‖ 63.6 pF
Unity Gain frequency	120 MHz
Unity loop Gain frequency	70 MHz
Current Drawn	2.25 mA(in each channel)
Total Power consumption(V_{dd} =1.2 V)	5.4 mW (I + Q)

Table 6.5: Summary of TIA

6.5 Comparison with recent work on Bluetooth

Characteristic	This work	IEEEJSSC [3]	IEEEJSSC [9]	ISSCC [8]
Sensitivity(dBm)	-95.8	-95.5	−91	-88
Current(mA)	17(high gain)	35	21	29.7
S11(dB)	-10.8	−20	-	-
Inductors used in LNA	No	Input Balun used	Yes	Yes
Dynamic range	-95.8 to -20 dBm	-95.5 to -4 dBm	-	-
IIP_3(dBm)	-10.3	>20	-	-
Technology(nm)	65	110	65	130
V_{dd}(V)	1.2	1.5	1.2	12

6.6 Conclusions

The Bluetooth receiver is designed without using any inductors thereby saving lot of area on the chip. It has sensitivity of -95.8 dBm and good linearity. The receiver has a Integrated Noise Figure of 4.2 dB. The Power consumed by the receiver is also very less.

Bibliography

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